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DATA SHEET

SURFACE-MOUNT CERAMIC MULTILAYER CAPACITORS

C-Array: Class 2, X7R

16/25/50 V

size 0612 (4 × 0603)



Phycomp

Product Specification – Jul 21, 2003 V.6



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Surface-mount ceramic multilayer capacitors

C-Array: Class 2, X7R 16/25/50 V size 0612 (4 × 0603)

FEATURES

- 0612 (4 × 0603) capacitors (of the same capacitance value) per array
- Less than 50% board space of an equivalent discrete component
- High volumetric efficiency
- Dense dielectric layers
- Supplied in tape on reel or loose in bag
- Increased throughput, by time saved in mounting
- Cost savings on manufacturing time.

APPLICATIONS

- Professional electronics
- High density consumer electronics
- Automotive.

DESCRIPTION

Each capacitor element consists of a rectangular block of ceramic dielectric in which a number of interleaved precious metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two terminations, copper dipped with a barrier layer of plated nickel and finally covered with a layer of plated tin (NiSn). An outline of the structure is shown in Fig.1.

QUICK REFERENCE DATA

DESCRIPTION	VALUE
Rated voltage U_R (DC)	16 V; 25 V; 50 V (IEC)
Capacitance range (E6 series) 16 V 25 V 50 V	 10 nF to 100 nF 10 nF to 68 nF 220 pF to 10 nF
Tolerance on capacitance	±10% (K); ±20% (M)
Sectional specifications	IEC 60384-10, second edition 1989-04; also based on CECC 32 100
Detailed specification	based on CECC 32 101-801
Climatic category (IEC 60068)	55/125/56

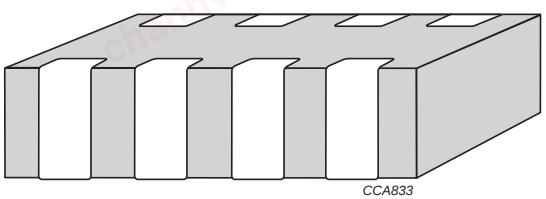


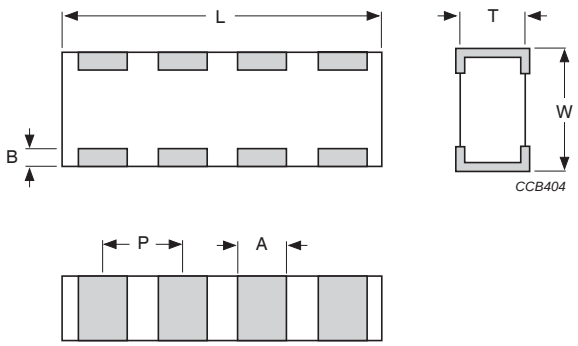
Fig.1 Simplified outline.

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MECHANICAL DATA



For dimensions see Table 1.

Fig.2 Dimensional outline.

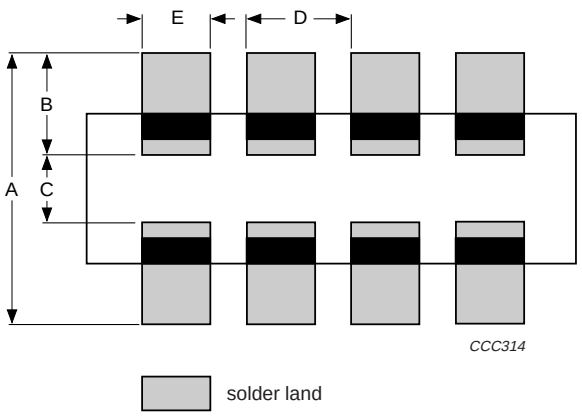
Physical dimensions

Table 1 Capacitor dimensions for product size 0612 (4 × 0603); see Fig. 2

CASE SIZE	L	W	T		A	B	P
			MIN.	MAX.			
Dimensions in millimetres							
0612 (4 × 0603)	3.20 ±0.15	1.60 ±0.15	0.70	1.30	0.40 ±0.1	0.30 ±0.2	0.80 ±0.1
Dimensions in inches							
0612 (4 × 0603)	0.125 ±0.006	0.063 ±0.006	0.028	0.051	0.0016 ±0.004	0.012 ±0.008	0.031 ±0.004

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DIMENSIONS OF SOLDER LANDS



For dimensions see Table 2.

Fig.3 Recommended dimensions of solder lands.

Table 2 Solder land dimensions; see Fig.3

CASE SIZE	FOOTPRINT DIMENSIONS (mm)				
	A	B	C	D	E
0612 (4 × 0603)	2.54 ±0.15	0.89 ±0.10	0.76 ±0.10	0.80 ±0.10	0.45 ±0.10

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SELECTION CHART

C (pF)	LAST TWO DIGITS OF 12NC	0612 (4 × 0603)		
		16 V	25 V	50 V
220	14			
330	16			
470	18			
680	21			
1 000	23			
1 500	25			0.8 ±0.1
2 200	27			
3 300	29			
4 700	32			
6 800	34			
10 000	36			
15 000	38			
22 000	41		0.8 ±0.1	
33 000	43	0.8 ±0.1		
47 000	45			
68 000	47		1.2 ±0.1	
100 000	49			

Thickness classification and packing quantities

THICKNESS CLASSIFICATION (mm)	8 mm TAPE WIDTH QUANTITY PER REEL	
	∅180 mm; 7"	
	PAPER	BLISTER
0.8 ±0.1	4 000	–
1.2 ±0.1	–	4 000

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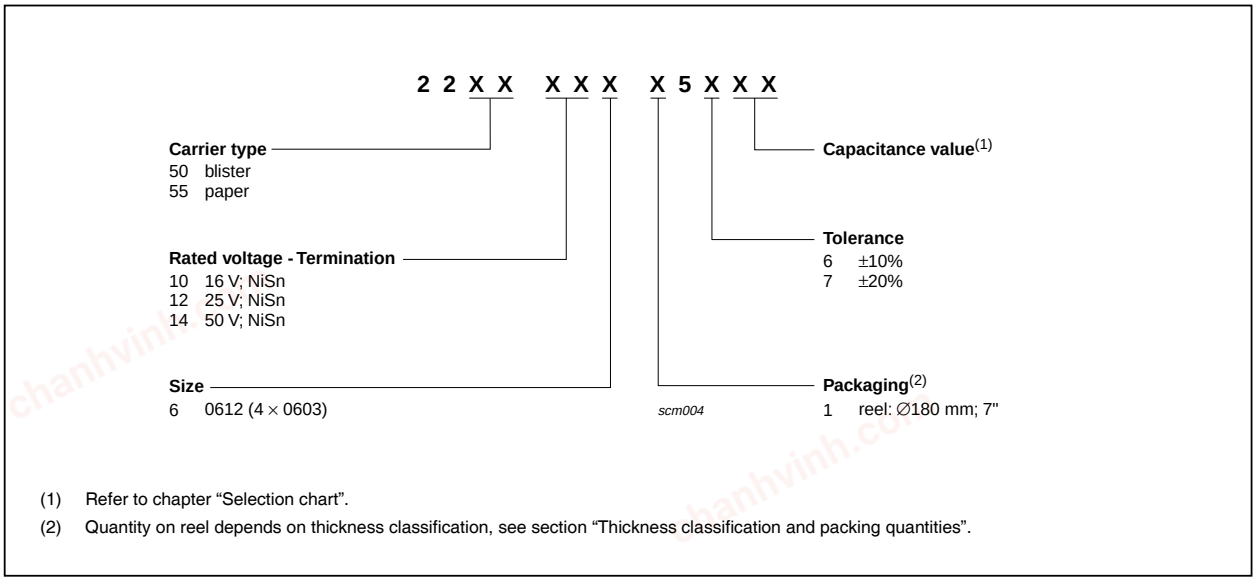
Surface-mount ceramic multilayer capacitors

C-Array: Class 2, X7R 16/25/50 V size 0612 (4 × 0603)

ORDERING INFORMATION

Components may be ordered by using either Phycomp's unique 12NC or a simple 15-digit clear text code.

Ordering code 12NC (preferred)



(1) Refer to chapter "Selection chart".

(2) Quantity on reel depends on thickness classification, see section "Thickness classification and packing quantities".

Clear text code

EXAMPLE: 06122R104K7B20D

Size Code	Temp. Char.	Capacitance	Tol.	Vol.	Termination	Packing	Marking	Series
0612 (4×0603)	2R = X7R	104 =1000000 pF; the third digit signifies the multiplying factor: 1 = × 10 2 = × 100 3 = × 1 000 4 = × 1 0000	K = ±10% M = ±20%	7 = 16 V 8 = 25 V 9 = 50 V	B = NiSn	2 = 180 mm; 7" paper B = 180 mm; 7" blister	0 = no marking	D = BME

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ELECTRICAL CHARACTERISTICS

Class 2 capacitors; X7R dielectric; NiSn terminations

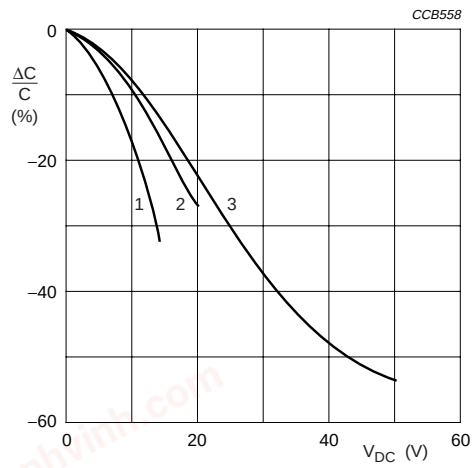
Unless otherwise stated all electrical values apply at an ambient temperature of 20 ±1 °C, an atmospheric pressure of 86 to 106 kPa, and a relative humidity of 63 to 67%.

DESCRIPTION	VALUE
Capacitance range (E6 series); note 1 16 V 25 V 50 V	 10 nF to 100 nF 10 nF to 68 nF 220 pF to 10 nF
Tolerance on capacitance after 1000 hours	±10%; 20%
Test voltage (DC) for 1 minute	$2.5 \times U_R$
Tan δ; note 1 16 V 25 V and 50 V	 ≤ 3.5% ≤ 2.5%
Insulation resistance after 1 minute at U_R (DC):	$R_{ins} \geq 10$ GΩ or $R_{ins} \times C \geq 500$s whichever is smaller
Ageing	typical 3% per time decade

Note

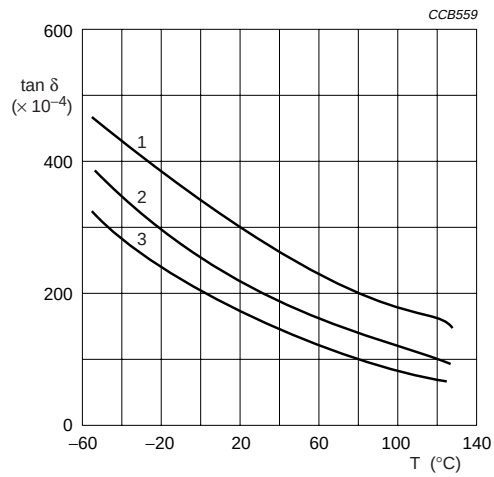
1. Measured at 1 V, 1 kHz, using a four-gauge method.

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Curve 1 = 16 V product.
Curve 2 = 25 V product.
Curve 3 = 50 V product.

Fig.4 Typical capacitance change with respect to the capacitance at 1 V as a function of DC voltage at 25 °C.



Curve 1 = 16 V product.
Curve 2 = 25 V product.
Curve 3 = 50 V product.

Fig.5 Typical tan δ as a function of temperature.

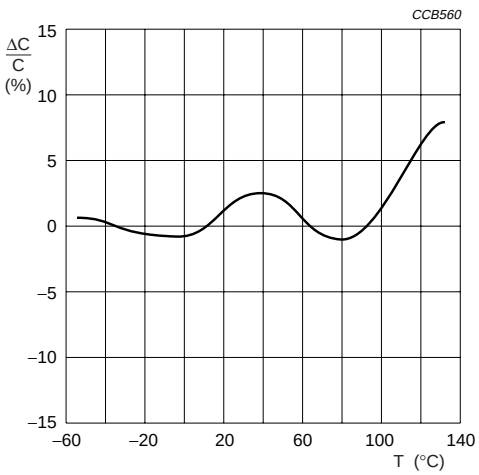


Fig.6 Typical capacitance change as a function of temperature.

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TESTS AND REQUIREMENTS

Table 3 Test procedures and requirements

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.4		mounting	the capacitors may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering (including vapour phase soldering) or conductive adhesive	no visible damage
4.5		visual inspection and dimension check	any applicable method using ×10 magnification	in accordance with specification
4.6.1		Capacitance (measured 1000 hours after date of manufacture)	f = 1 kHz; measuring voltage 1 Vrms at 20 °C	within specified tolerance
4.6.2		tan δ	f = 1 kHz; measuring voltage 1 Vrms at 20 °C	in accordance with specification
4.6.3		insulation resistance	at U_R (DC) for 1 minute	in accordance with specification
4.6.4		voltage proof	2.5 × U_R for 1 minute;	no breakdown or flashover
4.7.1		Temperature characteristic	between minimum and maximum temperature	in accordance with specification
4.8		adhesion	a force of 5 N applied for 10 s to the line joining the terminations and in a plane parallel to the substrate	no visible damage
4.9		bond strength of plating on end face	mounted in accordance with IEC 60384 10, paragraph 4.4 conditions: bending 1 mm at a rate of 1 mm/s, radius jig. 340 mm	no visible damage $\Delta C/C$: ±10%
4.10	Tb	resistance to soldering heat; jig clamps to the second component in the longitudinal line	260 ±5 °C for 10 ±0.5 s in a static solder bath	the terminations shall be well tinned after recovery $\Delta C/C$: ≤ ±10%
		resistance to leaching; jig clamps to the second component in the longitudinal line	260 ±5 °C for 30 ±1 s in a static solder bath	using visual enlargement of ×10, dissolution of the terminations shall not exceed 10%

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IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.11	Ta	solderability; jig clamps to the second component in the longitudinal line	zero hour test, and test after storage (20 to 24 months) in original packing in normal tmosphere; unmounted hips completely immersed for 2 ±0.5 s in a solder bath at 235 ±5 °C	the terminations shall be well tinned
4.12	Na	rapid change of temperature	preconditioning: between minimum and maximum temperature, 5 cycles	no visible damage after 24 hours recovery: $\Delta C/C$: ±15%
4.14	Ca	damp heat	preconditioning: 56 days; 40 °C; 90 to 95% RH; U_R applied	after 48 hours recovery: $\Delta C/C$: ±15% tan δ: 7% R_{ins}: 1000 MΩ or $R_i C_R \geq 25$ s, whichever is less
4.15		endurance	preconditioning: 2 × U_R at 125 °C for 1000 hours, recovery 48 ±4 hours at room temperature	after 48 hours recovery: $\Delta C/C$: ±20% tan δ: 7% R_{ins}: 2000 MΩ or $R_i C_R \geq 50$ s, whichever is less

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REVISION HISTORY

Revision	Date	Change Notification	Description
Rev.4	2001 May 30	-	- Converted to Phycomp brand
Rev.5	2003 Feb 13	-	- Updated company logo
Rev.6	2003 Jul 21	-	- Cover page revised