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WPMDH1100601 / 171010601

MagI³C Power Module
VDRM – Variable Step Down Regulator Module

6V – 42V / 1A / 0.8V – 6V Output

DESCRIPTION

The VDRM series of the MagI³C Power Module family provides a fully integrated DC-DC power supply including the buck switching regulator and inductor in a package.

The 171010601 offers high efficiency and delivers up to 1A of output current. It operates from 6V input voltage up to 42V. It is designed for fast transient response.

It is available in an innovative industrial high power density TO263-7EP (10.16 x 13.77 x 4.57mm) package that enhances thermal performance and allows for hand or machine soldering.

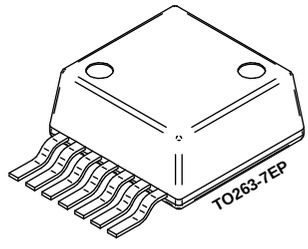
The VDRM regulators have an integrated protection circuit that guards against thermal overstress and electrical damage by using thermal shut-down, overcurrent, short-circuit, overvoltage and undervoltage protection.

TYPICAL APPLICATIONS

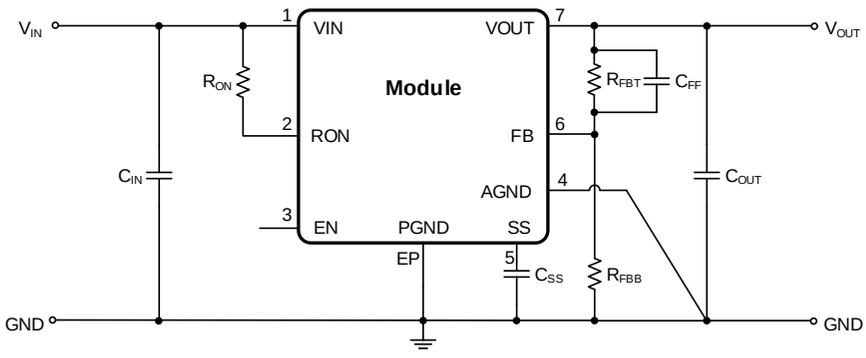
- Point-of-Load DC-DC applications from 9V, 12V, 18V and 24V industrial rails
- Industrial, test & measurement, medical applications
- System power supplies
- DSPs, FPGAs, MCUs and MPUs supply
- I/O interface power supply

FEATURES

- Peak efficiency above 90%
- Current capability up to 1A
- Input voltage range: 6V to 42V
- Output voltage range: 0.8V to 6V
- Reference accuracy: ±2%
- No minimum load required
- Integrated shielded inductor solution for quick time to market and ease of use
- Single exposed pad for best-in-class thermal performance
- Low output voltage ripple (< 10mV$_{pp}$)
- Adjustable switching frequency: 0.2 to 0.8 MHz
- Low ripple Constant On-Time control
- Synchronous operation
- Automatic power saving operation at light load
- Undervoltage lockout protection (UVLO)
- Adjustable soft-start
- Thermal shutdown
- Short circuit protection
- Cycle-by-cycle current limit
- Output overvoltage protection
- Pin compatible with 171012401, 171012402, 171032401, 171020601 and 171030601
- Operating ambient temperature up to 105°C
- RoHS and REACh compliant
- Operating junction temp. range: -40 to 125°C
- Mold compound UL 94 Class V0 (flammability testing) certified
- Complies with EN55022 class B radiated emissions standard



TYPICAL CIRCUIT DIAGRAM



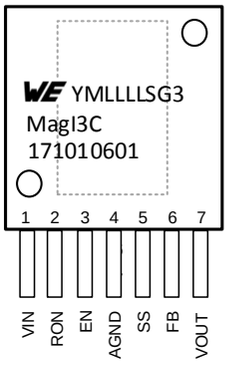
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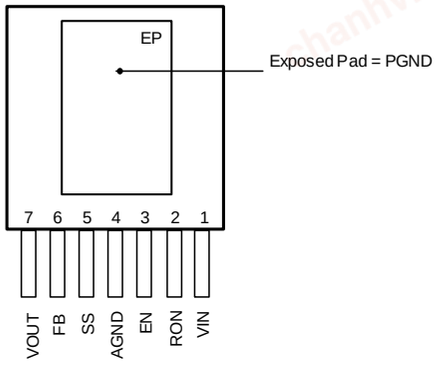
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PACKAGE



Top View



Bottom View

MARKING DESCRIPTION

Marking	Description
WE	Würth Elektronik tradename
Y	Year
M	Month
LLLL	Assembly lot code
S	Assembly site code per QSS 050-120
G3	Lead finish code per Jedec Norm (green 3 mat sin)
MagI3C	MagI³C logo
171010601	Order code

PIN DESCRIPTION

SYMBOL	NUMBER	TYPE	DESCRIPTION
VIN	1	Power	The supply input pin is a terminal for an unregulated input voltage source. It is required to place the input capacitor nearby the VIN pin and PGND.
RON	2	Input	An external resistor from R_{ON} to VIN pin sets the on-time and frequency of the application.
EN	3	Input	Connecting this pin to GND disables the device. Connecting this pin to a voltage higher than 1.18V typ. (but <6.5V) or leaving it floating enables the device. This pin can be used in order to set an external UVLO through a resistor divider. If this pin is left floating the device is always on.
AGND	4	Supply	The analog ground pin is the reference point for all stated voltages. It is internally connected to PGND.
SS	5	Input	For the soft-start function there is an internal 8µA current source which charges an external capacitor (C_{SS}) to generate the soft-start. A minimum capacitance is required
FB	6	Input	The feedback pin is internally connected to the regulation circuitry, the overvoltage and short-circuit comparators. The regulation reference point is 0.8V at this input pin. Connect the feedback resistor divider between the output and AGND to set the output voltage.
VOUT	7	Power	The output voltage pin is connected to the internal inductor. For the best stability and operation connect the output capacitor between this pin and PGND.
PGND	EP	Power	Exposed Pad – Main node for switch current of the internal low-side MOSFET. Used as heat sink for power dissipation during operation.

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ORDERING INFORMATION

ORDER CODE	PART DESCRIPTION	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
171010601	WPMDH1100601JT	1A / 0.8-6Vout version	TO263-7EP	Tape and Reel, 250 pieces
178010601	WPMDH1100601JEV	1A / 0.8-6Vout version	Eval Board	1

PIN COMPATIBLE FAMILY MEMBERS

ORDER CODE	PART DESCRIPTION	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
171012401	WPMDH1102401JT	1A / 5-24Vout version	TO263-7EP	Tape and Reel, 250 pieces
178012401	WPMDH1102401JEV	1A / 5-24Vout version	Eval Board	1
171012402	WPMDH1152401JT	1.5A / 5-24Vout version	TO263-7EP	Tape and Reel, 250 pieces
178012402	WPMDH1152401JEV	1.5A / 5-24Vout version	Eval Board	1
171032401	WPMDH1302401JT	3A / 5-24Vout version	TO263-7EP	Tape and Reel, 250 pieces
178032401	WPMDH1302401JEV	3A / 5-24Vout version	Eval Board	1
171020601	WPMDH1200601JT	2A / 0.8-6Vout version	TO263-7EP	Tape and Reel, 250 pieces
178020601	WPMDH1200601JEV	2A / 0.8-6Vout version	Eval Board	1
171030601	WPMDH1300601JT	3A / 0.8-6Vout version	TO263-7EP	Tape and Reel, 250 pieces
178030601	WPMDH1300601JEV	3A / 0.8-6Vout version	Eval Board	1

SALES INFORMATION

SALES CONTACTS
Würth Elektronik eiSos GmbH & Co. KG EMC & Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 7942 945 0 www.we-online.com powermodules@we-online.com

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ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN (1)	MAX (1)	
VIN, RON	Input voltage, On-time resistor	-0.3	43.5	V
EN, FB, SS	Enable, Feedback, Soft-start input	-0.3	7.0	V
V_{ESD}	ESD voltage (Human Body Model), according to EN61000-4-2 (2)	-	±2000	V
T_J	Junction temperature	-	150	°C
$T_{storage}$	Assembled, non-operating storage temperature	-65	150	°C
T_{SOLDER}	Peak case/leads temperature during reflow soldering, max. 20sec (3)	235	245	°C

OPERATING CONDITIONS

Operating conditions are conditions under which operation of the device is intended to be functional. All values are referenced to GND.

SYMBOL	PARAMETER	MIN (1)	TYP (4)	MAX (1)	UNIT
V_{IN}	Input voltage	6	-	42	V
V_{OUT}	Regulated output voltage	0.8	-	6	V
V_{EN}	Enable input voltage	0	-	6.5	V
T_A	Ambient temperature range	-40	-	105(5)	°C
T_J	Junction temperature range	-40		125	°C
I_{OUT}	Nominal output current			1	A

THERMAL SPECIFICATIONS

SYMBOL	PARAMETER	TYP (4)	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance (6)	19.3	°C/W
Θ_{Jc}	Junction-to-case thermal resistance	1.9	°C/W
T_{SD}	Thermal shutdown, rising	165	°C
	Thermal shutdown hysteresis, falling	15	°C

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ELECTRICAL SPECIFICATIONS

MIN and MAX limits are valid for the recommended junction temperature range of **-40°C to 125°C**. Typical values represents statistically the utmost probability at following conditions: V_{IN} = 24V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (4)	MAX (1)	UNIT
Output current						
I_{CL}	Current limit threshold		1.10	1.18	1.25	A
Output voltage						
V_{FB}	Reference voltage	V_{SS}>0.8V, T_J=25°C, I_{OUT} = 10mA	0.786	0.802	0.818	V
	Reference voltage over temperature	V_{SS}>0.8V, -40°C≤T_J≤125°C, I_{OUT} = 1A	0.777	0.798	0.818	V
I_{FB}	Feedback input bias current		-	5	-	nA
V_{OUT}	Line regulation	V_{IN} = 12V to 42V I_{OUT}=1A	-	±0.01	-	%
	Load regulation	V_{IN} = 24V I_{OUT} = 0A to 1A	-	1.5	-	mV/A
	Output voltage ripple	V_{OUT}=5V C_{OUT}=100µF 6.3V X7R 20MHz BWL	-	8	-	mV_{pp}
Protections						
V_{FB-OVP}	Feedback overvoltage protection threshold		-	0.92	-	V
Switching frequency						
f_{SW}	Switching frequency	Continuous Conduction Mode (CCM)	0.2	-	0.8	MHz
t_{ON-MIN}	ON timer minimum pulse width		-	150	-	ns
$t_{OFF-MIN}$	OFF timer minimum pulse width		-	260	-	ns
Enable						
V_{ENABLE}	EN threshold trip point	V_{EN} rising	1.10	1.18	1.25	V
	EN threshold hysteresis	V_{EN} falling	-	90	-	mV
Soft-Start						
t_{SS}	Soft-start time	C_{SS} = 0.022µF	-	2.2	-	ms
I_{SS}	SS pin source current	V_{SS} = 0V	5	8	11	µA
I_{SS-DIS}	SS discharge current		-	-200	-	µA

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MIN and MAX limits are valid for the recommended junction temperature range of **-40°C to 125°C**. Typical values represents statistically the utmost probability at following conditions: V_{IN} = 24V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (4)	MAX (1)	UNIT
Efficiency						
η	Efficiency	V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0.5A, f_{SW} = 500kHz	-	83	-	%
		V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1A, f_{SW} = 500kHz	-	86	-	%
		V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0.5A, f_{SW} = 500kHz	-	85	-	%
		V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A, f_{SW} = 500kHz	-	89	-	%
Input current						
I_Q	Input quiescent current	V_{FB} = 0.86V (7)	-	1	-	mA
I_{SD}	Shutdown quiescent input current	V_{ENABLE} = 0V	-	25	-	µA

RELIABILITY

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (4)	MAX (1)	UNIT
MTBF(8)	Mean Time Between Failures	- Confidence level 60% - Test temperature: 125°C - Usage temperature: 55°C - Activation energy: 0.7eV - Test duration: 1000 hours - Sample size: 6471 - Fail: 0	$5.54 \cdot 10^8$			h

RoHS, REACh

RoHS directive	COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK	Directive 2011/65/EU of the European Parliament and the Council of June 8th, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
REACh directive		Directive 1907/2006/EU of the European Parliament and the Council of June 1st, 2007 regarding the Registration, Evaluation, Authorization and Restriction of Chemicals (REACh).

PACKAGE SPECIFICATIONS

MOLD COMPOUND				WEIGHT
Part Number	**Material**	**UL Class**	**Certificate Number**	
171020601	EME-G760	UL94V-0	E41429	0.54g

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NOTES

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

(2) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

(3) JEDEC J-STD020

(4) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.

(5) Depending on heat sink design, number of PCB layers, copper thickness and air flow.

(6) Measured on a 8cm x 8cm four layer PCB, 35µm copper, thirty-six 10mil (254µm) thermal vias, no air flow (see "OUTPUT POWER DERATING" section on page 13).

(7) Module ON (Enable floating or high), feedback voltage applied by external source → no PWM switching

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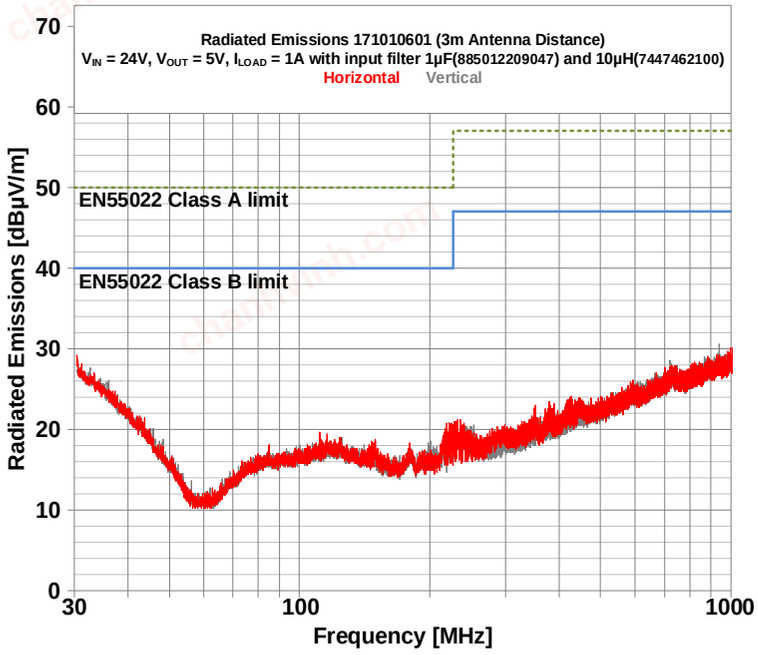
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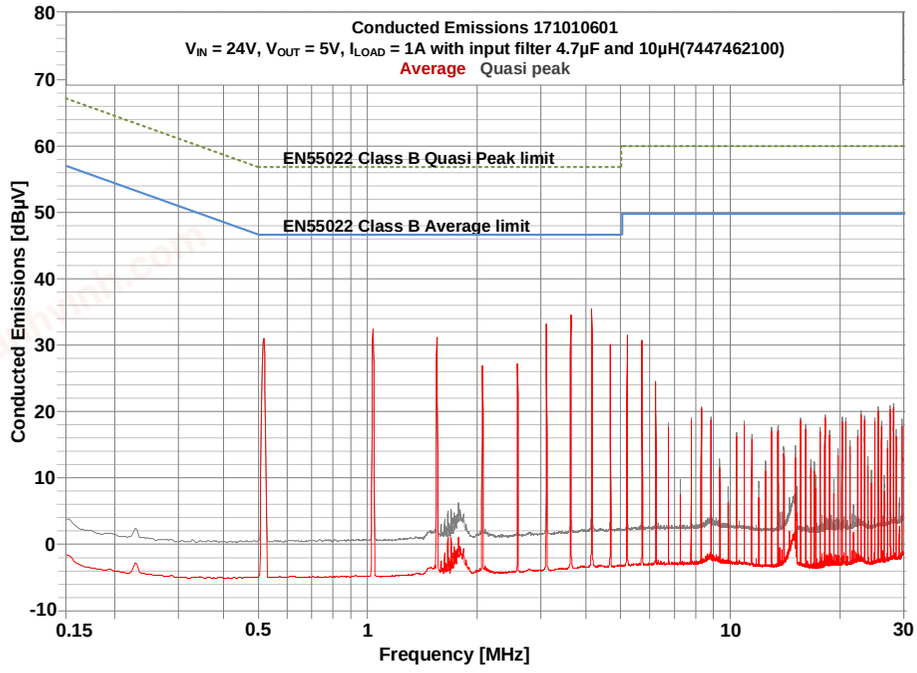
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TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R ceramic; C_{OUT} = 100µF X7R ceramic, T_{AMB} = 25°C.

RADIATED AND CONDUCTED EMISSIONS



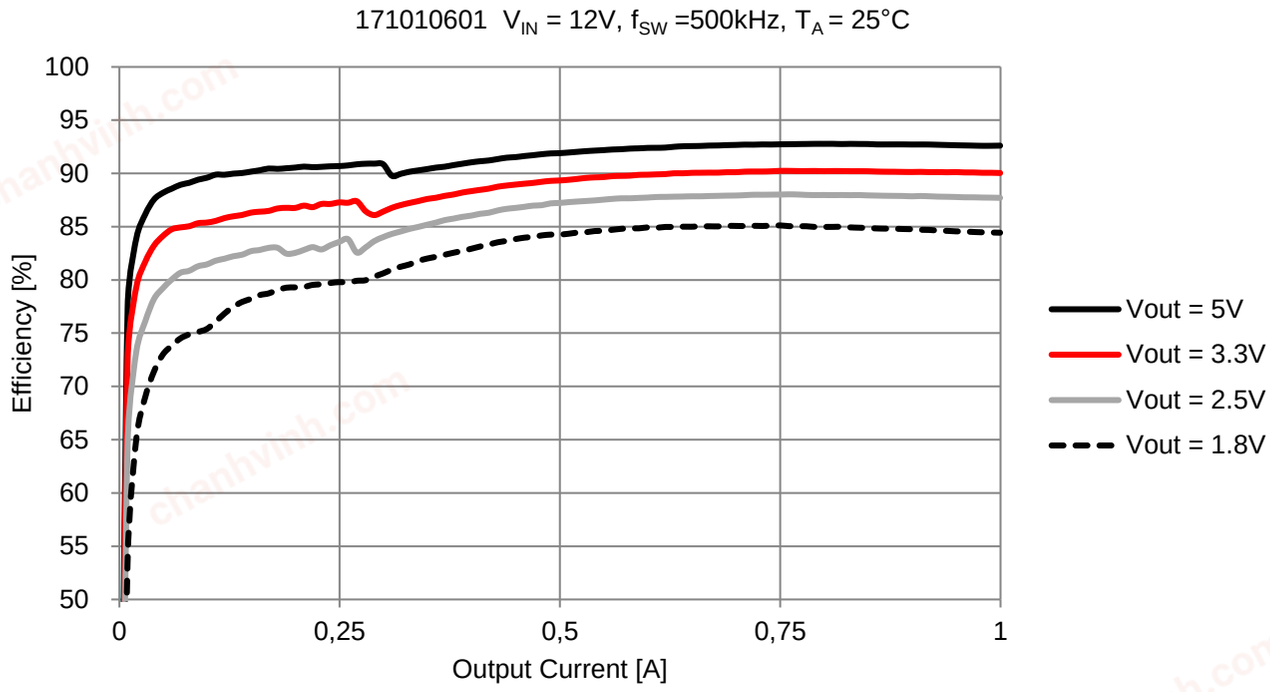


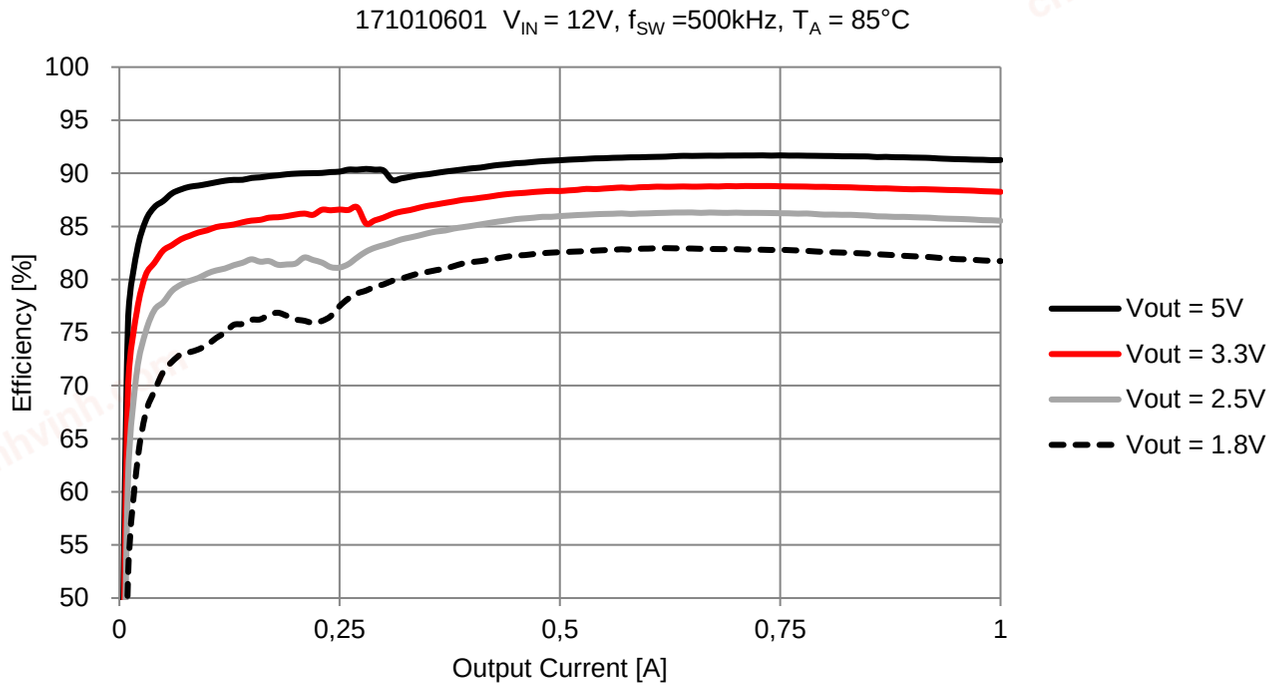
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EFFICIENCY



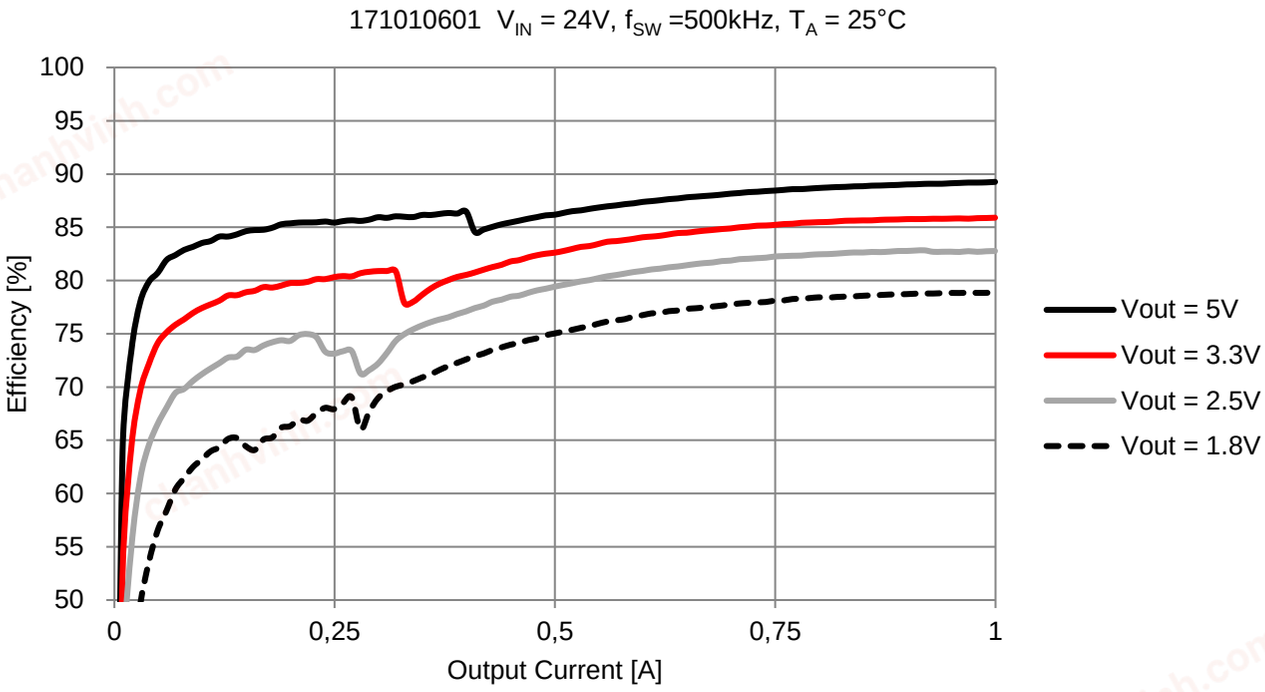


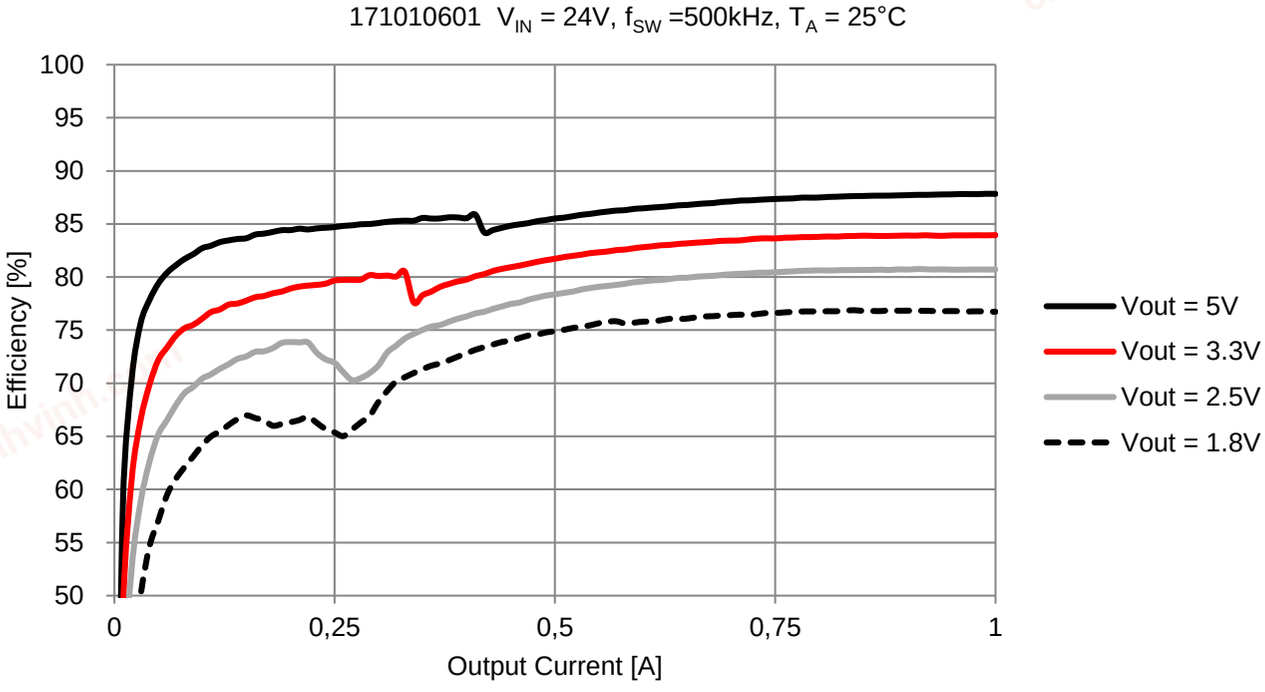
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EFFICIENCY





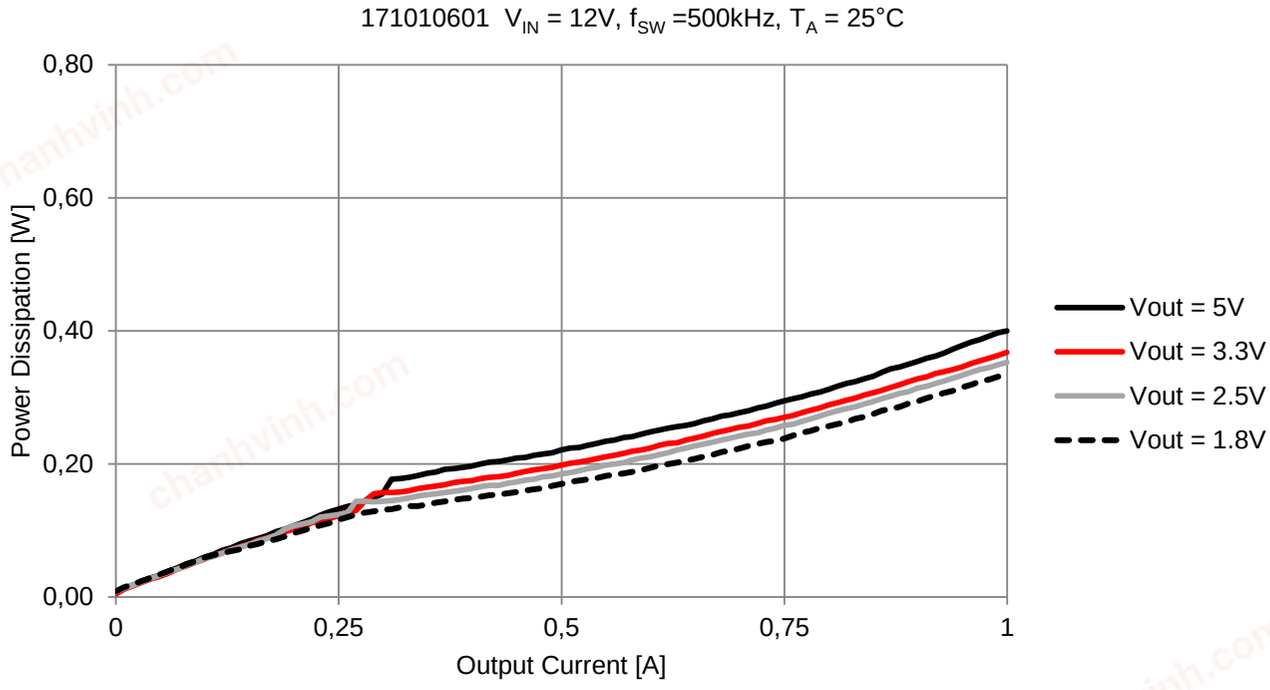
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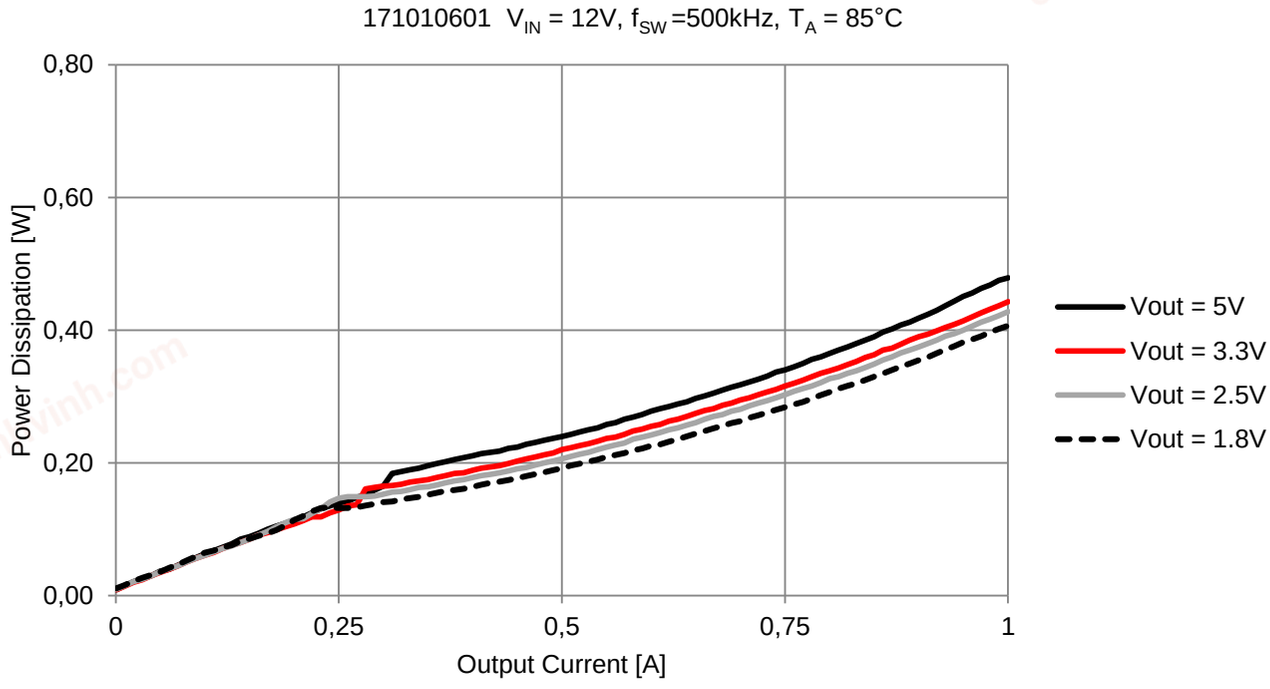
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POWER DISSIPATION



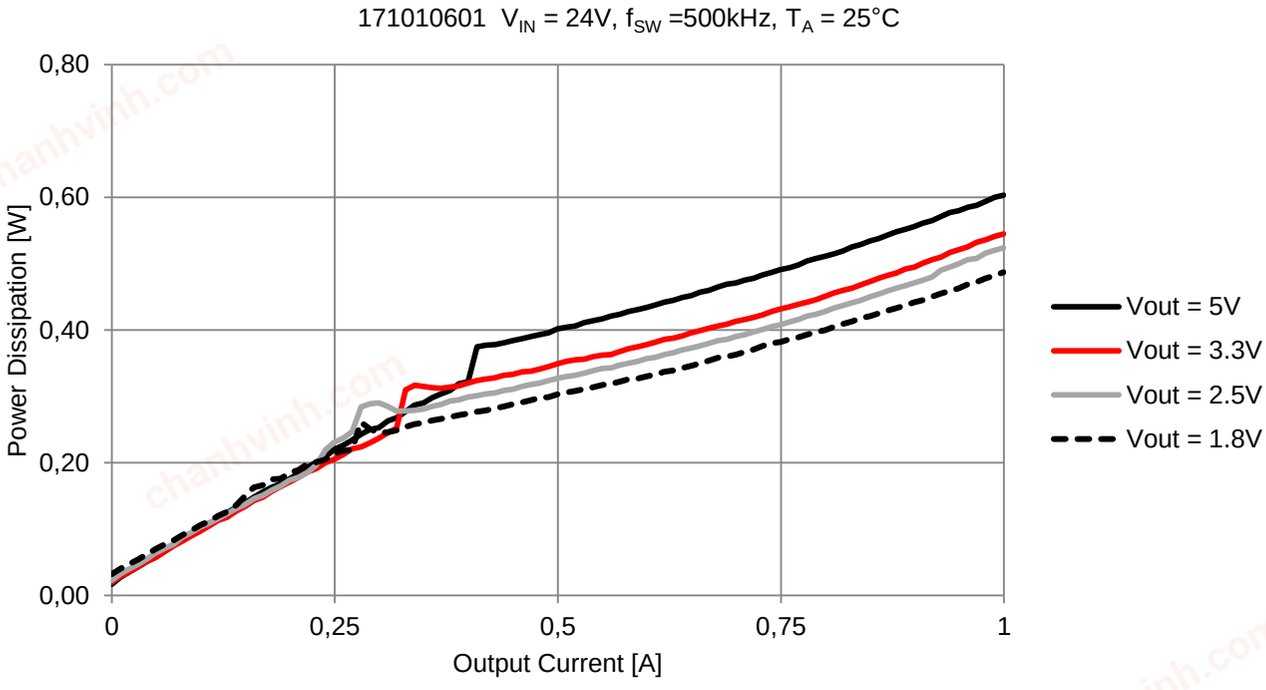


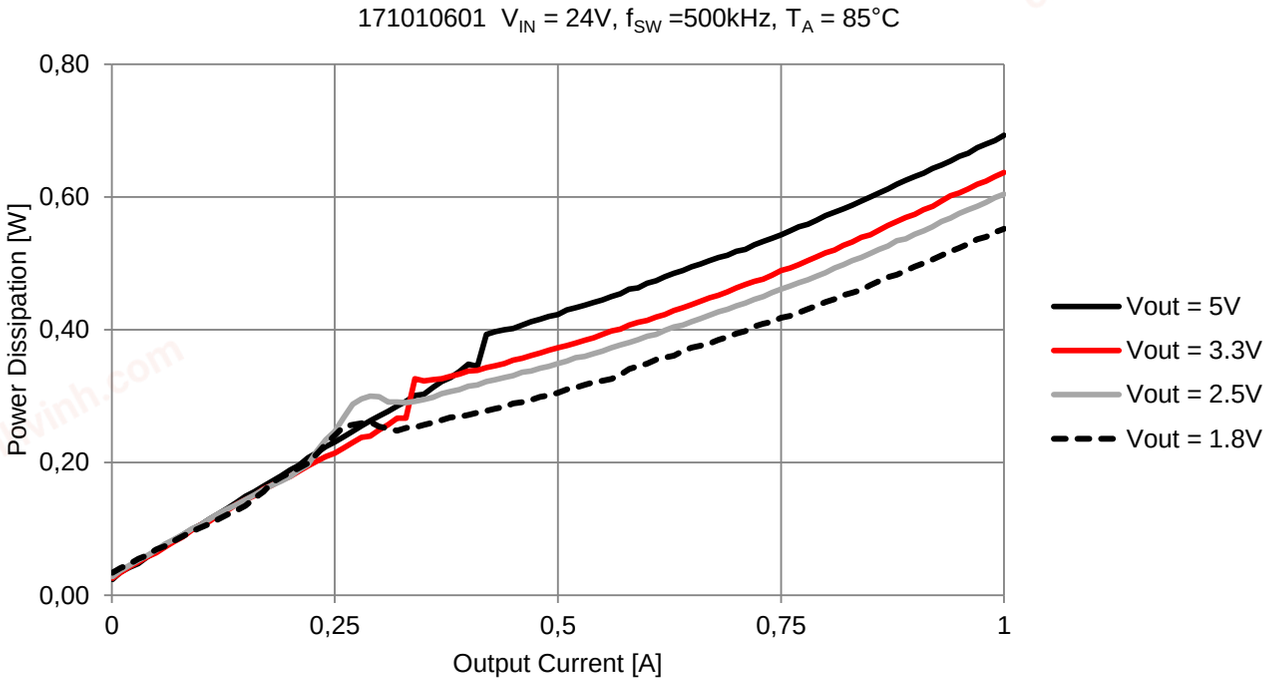
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POWER DISSIPATION



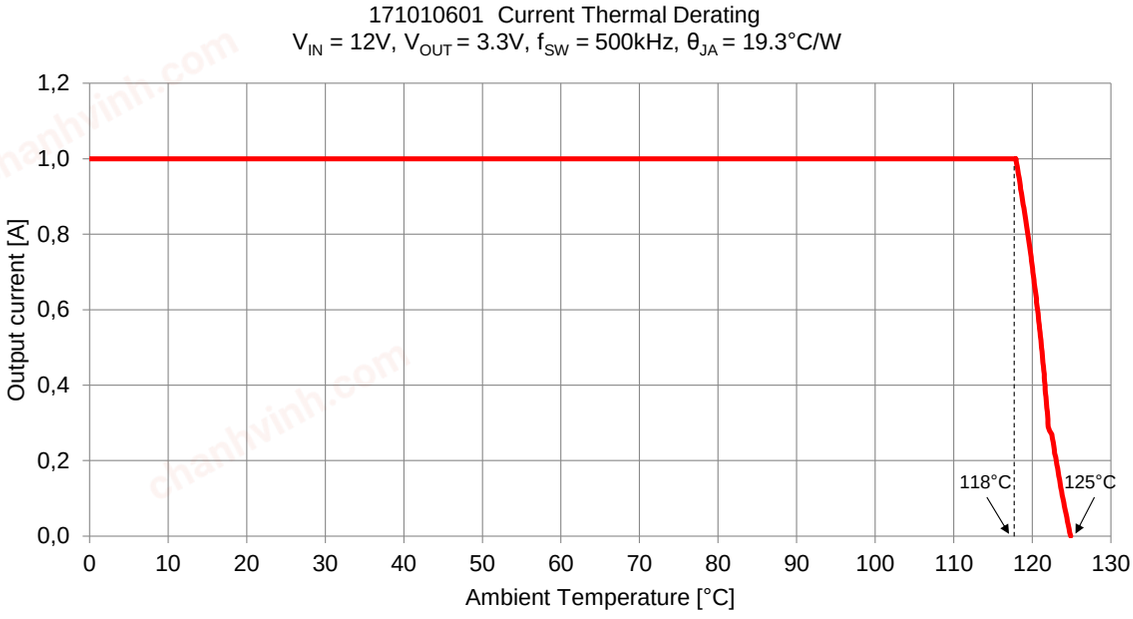


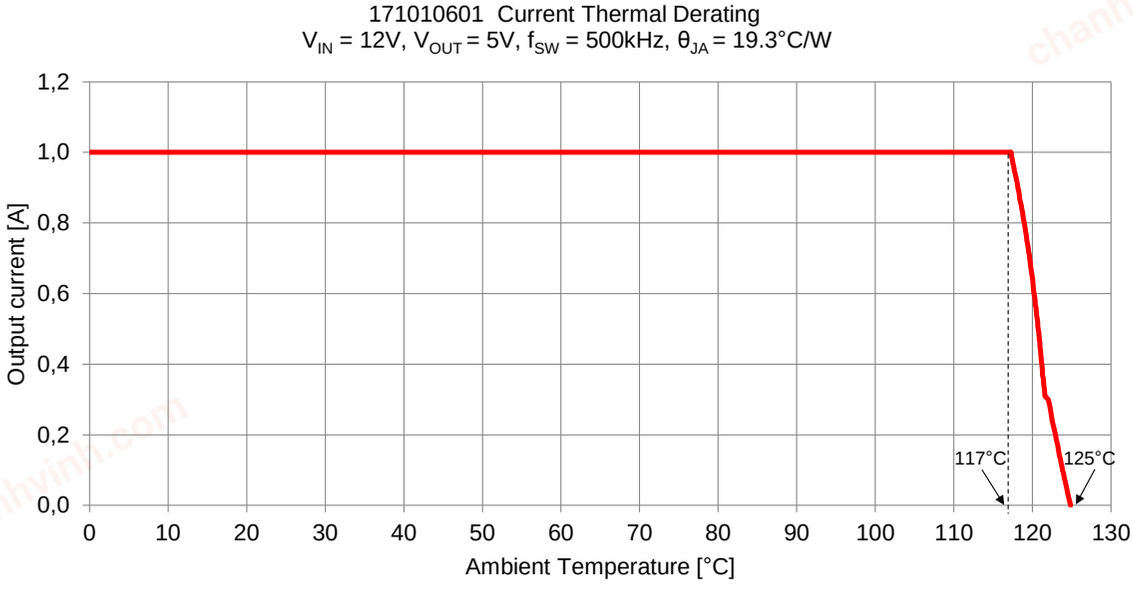
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OUTPUT POWER DERATING





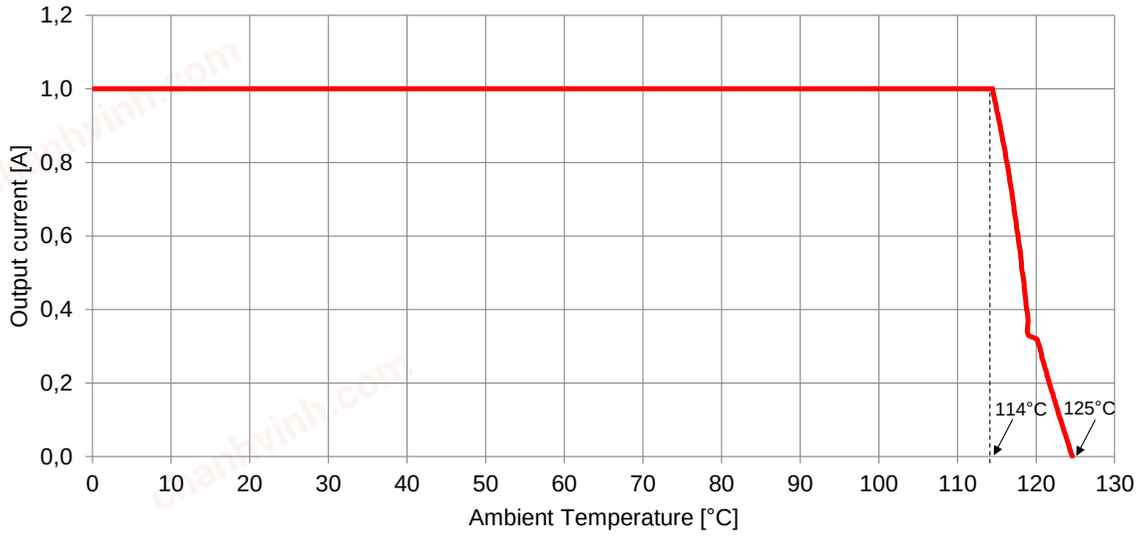
The ambient temperature and the power limits of the derating curve represent the operation at the max junction temperature specified in the “Operating Conditions” section on page 4.

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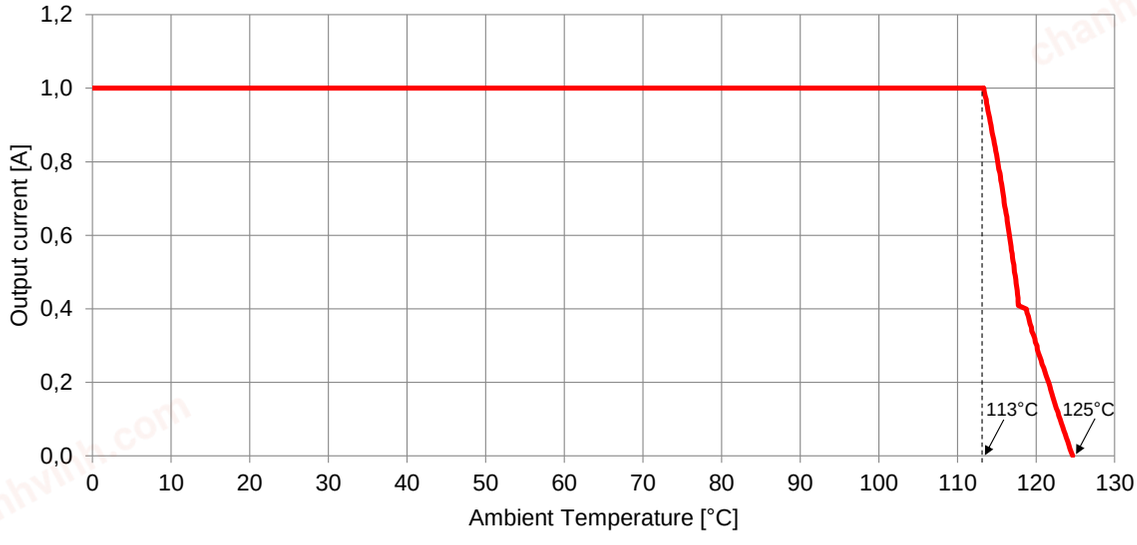
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MagI³C Power Module
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171010601 Current Thermal Derating
V_{IN} = 24V, V_{OUT} = 3.3V, f_{SW} = 500kHz, θ_{JA} = 19.3°C/W



171010601 Current Thermal Derating
V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 500kHz, θ_{JA} = 19.3°C/W



The ambient temperature and the power limits of the derating curve represent the operation at the max junction temperature specified in the "Operating Conditions" section on page 4.

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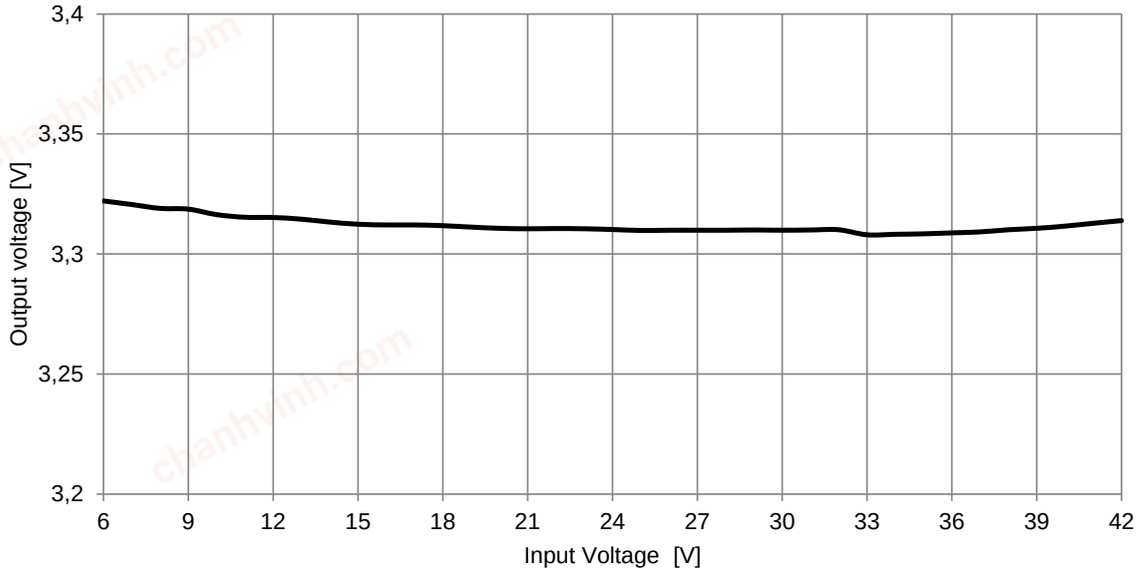
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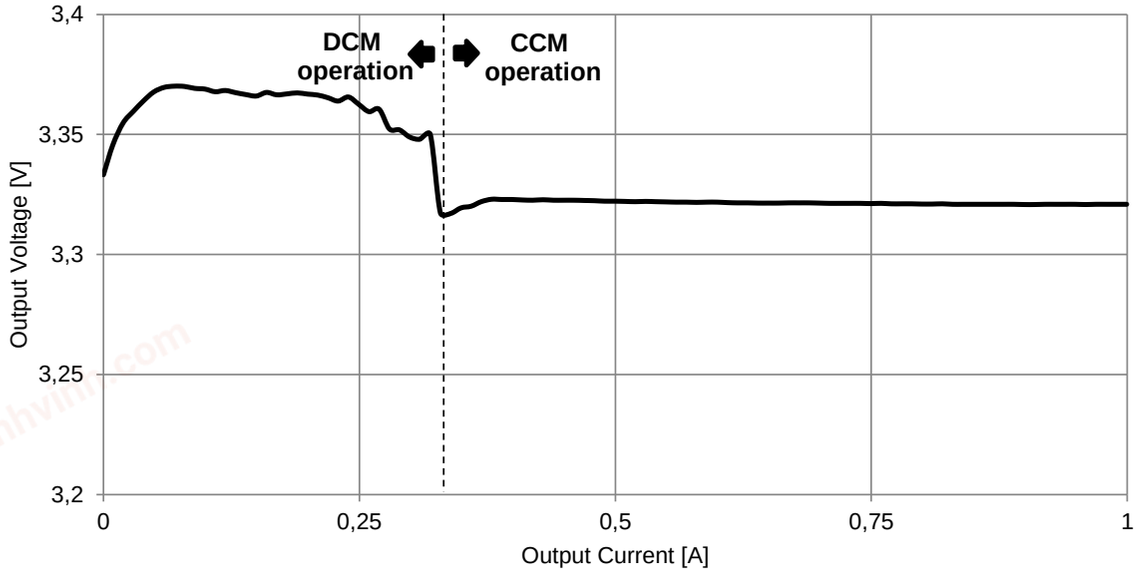
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LINE AND LOAD REGULATION

171010601 Line Regulation V_{OUT} = 3.3V, I_{OUT} = 1A, T_A = 25°C



171010601 Load Regulation V_{IN} = 24V, V_{OUT} = 3.3V, T_A = 25°C



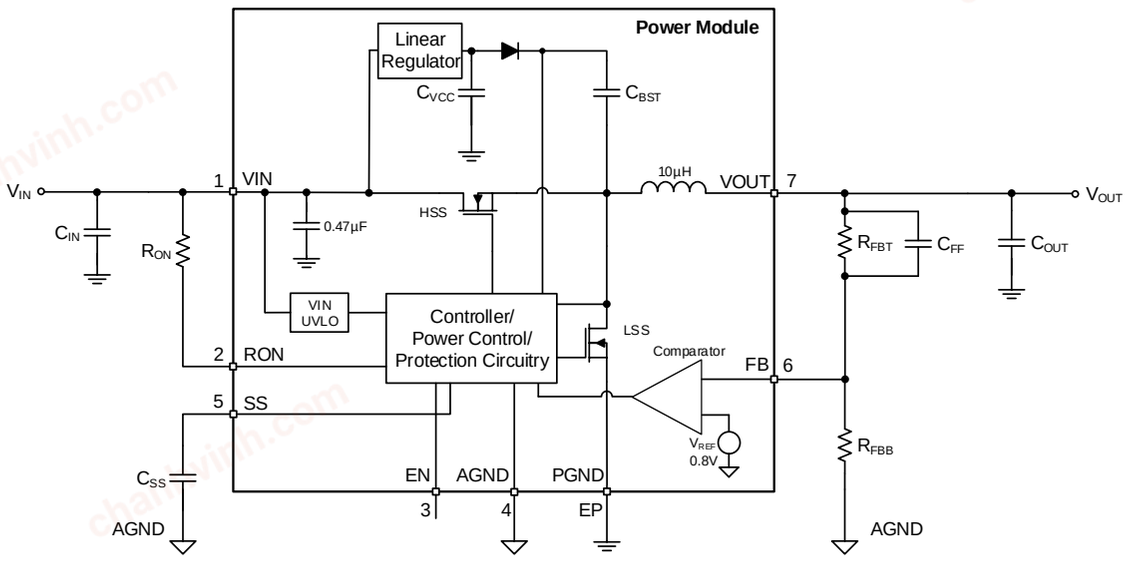
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BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MagI³C Power Module 171010601 is based on a synchronous step-down regulator with integrated MOSFETs and a power inductor. The control scheme uses a Constant On-Time (COT) low ripple hysteretic regulation loop.

The V_{OUT} of the regulator is divided by the feedback resistor network R_{FBT} and R_{FBB} and fed into the FB pin. The internal comparator compares this signal with the internal 0.8V reference. If the feedback voltage is below the reference, the high side MOSFET is turned on for a fixed on-time.

To achieve a regulated output voltage the off-time is modulated. At stable V_{IN} to V_{OUT} condition the relation between on-time and off-time is constant. The on-time is preset by the value of the RON resistor. The switching frequency is directly proportional to this value. The connection of the R_{ON} resistor to V_{IN} results into an additional compensation of V_{IN} variations, (V_{IN} feed-forward) so the switching frequency will remain almost constant even during V_{IN} transients.

A load current transient (low to high current) allows the off-time to immediately transition to the minimum of 260 ns. This results in a short term higher switching frequency which ensures an extremely quick regulation response. As soon as the output capacitor is recharged to the nominal output voltage the switching frequency will return to the original value even though the load current is higher.

The constant on-time control scheme does not require compensation circuitry which makes the overall design very simple. Nevertheless, it requires a certain minimum ripple at the feedback pin. The MagI³C Power Module 171010601 generates this ripple internally and is supported by the C_{FF} capacitor which bypasses AC ripple directly to the feedback pin from the output. With this architecture very small output ripple values of around 10mV (similar to current or voltage mode devices) are achieved.

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DESIGN FLOW

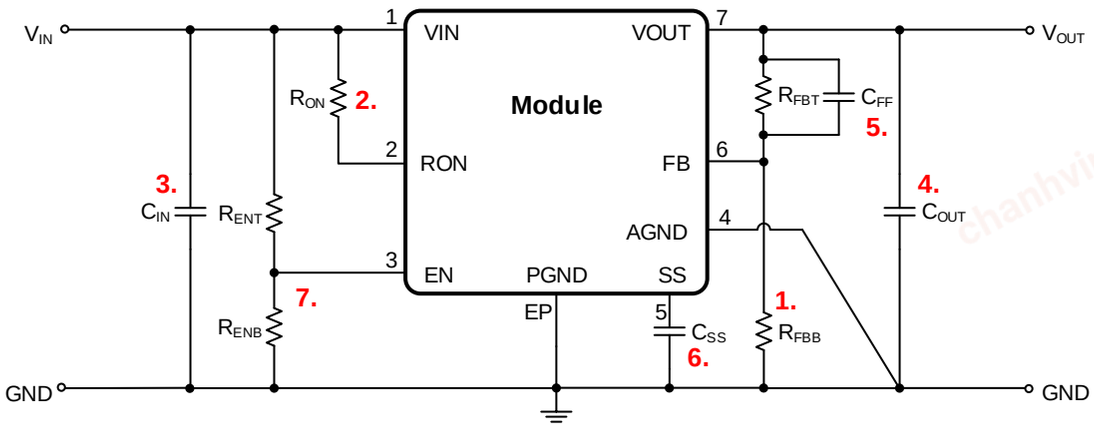
The next 7 simple steps show how to select the external components to design your power application.

Essential Steps

1. Set the output voltage
2. Set the operating frequency with R_{ON}
3. Select the input capacitor
4. Select the output capacitor
5. Select the feed forward capacitor
6. Select the soft-start capacitor

Optional Steps

7. Select the undervoltage lockout divider



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Step 1 Set the output voltage (V_{OUT})

The output voltage is determined by a divider of two resistors connected between V_{OUT} and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8V internal reference. In normal operation, an on-time cycle is initiated when the voltage on the FB pin falls below 0.8V. The high-side MOSFET on-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8V. As long as the voltage at FB is above 0.8V, on time cycles will not occur.

The ratio of the feedback resistors for the desired output voltage is:

$$\frac{R_{FBT}}{R_{FBB}} = \left(\frac{V_{OUT}}{V_{FB}}\right) - 1 \quad (1)$$

These resistors should be chosen from values in the range of 1kΩ to 20kΩ.

A table of values for R_{FBT}, R_{FBB}, and R_{ON} is included in the "TYPICAL SCHEMATIC" section (page 38).

Step 2 Set the operating frequency (f_{SW}) with R_{ON}

Many designs begin with a desired switching frequency in mind. For that purpose the following equation can be used:

$$R_{ON} \approxeq \frac{V_{OUT}}{(k \cdot f_{SW(CCM)})} \quad (2)$$

where $k = 1.3 \cdot 10^{-10}$ C and $f_{SW(CCM)}$ is the switching frequency when the device is working in CCM (Continuous Conduction Mode). While selecting the R_{ON} and the $f_{SW(CCM)}$, the limitations in terms of minimum on-time and off-time must be taken into account. The on-time of the MagI³C power module timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = \frac{(k \cdot R_{ON})}{V_{IN}} \quad (3)$$

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. The T_{ON} is internally limited to a minimum value of 150ns. Therefore R_{ON} should be selected such that the on-time at maximum V_{IN} is greater than 150ns, as the following formula describes:

$$R_{ON} \geq \frac{V_{IN(MAX)} \cdot t_{ON\text{-}MIN}}{k} \quad (4)$$

This limits the maximum operating frequency, which is governed by the following equation:

$$f_{SW(MAX)} = \frac{V_{OUT}}{(V_{IN(MAX)} \cdot t_{ON\text{-}MIN})} \quad (5)$$

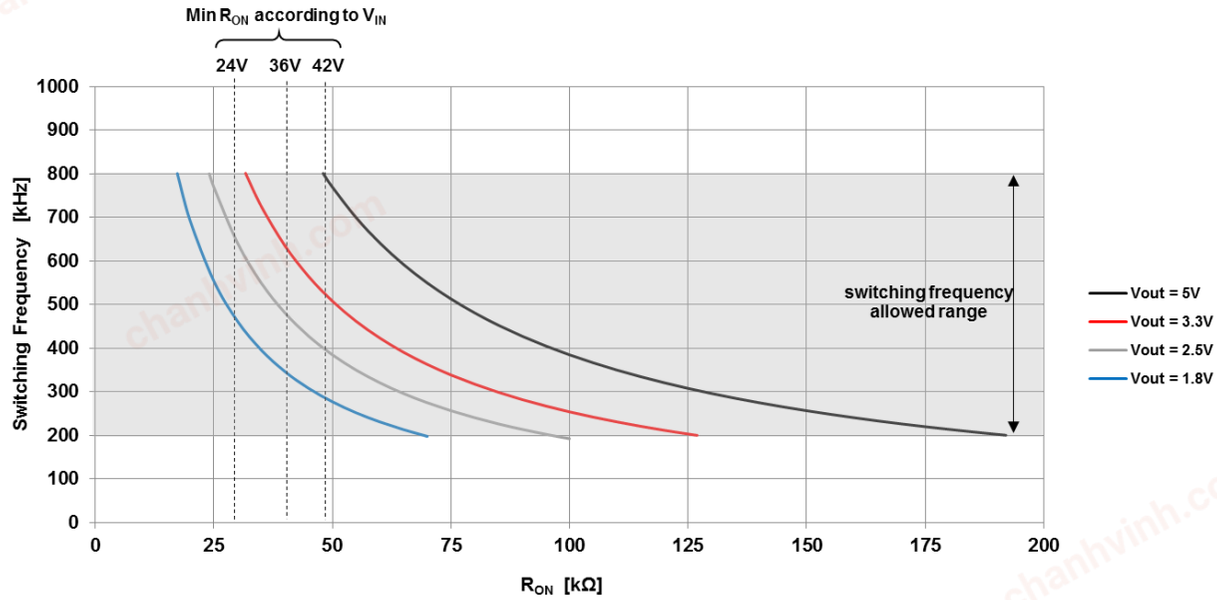
If the R_{ON} calculated in equation (2) is less than the minimum value determined in equation (4) a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.

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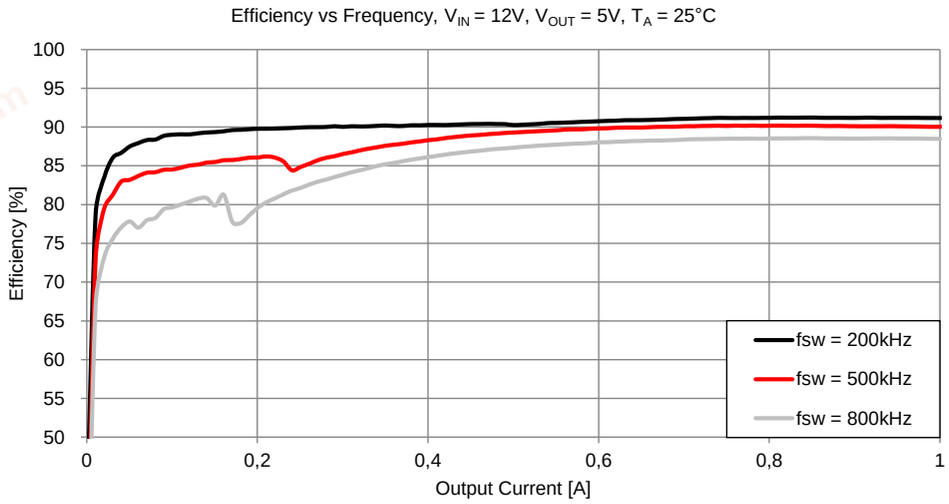
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All considerations mentioned above are summarized in the diagram below. The curves depict the relation between the switching frequency and the R_{ON} for some typical output voltages. For the switching frequency, only the range indicated in the "ELECTRICAL SPECIFICATIONS" section on page 5 (from 200kHz to 800kHz) is considered. Due to the minimum on-time previously mentioned, under low duty cycle conditions, there are some limitations in the minimum selectable R_{ON}. These limits are shown below with a dotted line and they refer to some typical input voltages (24V, 36V and the maximum operating voltage of 42V).



As stated above, the off-time is also limited to a minimum value of 260 ns, which limits the maximum duty cycle. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

The choice of the switching frequency influences the efficiency of the system, especially at low currents, as the picture below depicts.



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Step 3 Select the input capacitor (C_{IN})

The MagI³C power module contains an internal 0.47µF input ceramic capacitor. The module requires additional, external input capacitance to handle the input current ripple. This input capacitance should be located as close as possible to the MagI³C power module. Input capacitor selection is generally based on different requirements. The first criteria is the input current ripple. Worst case input current ripple rating is dictated by the equation:

$$I_{C_{INRMS}} \approx \frac{1}{2} \cdot I_{OUT} \cdot \sqrt{\frac{D}{1-D}} \qquad (6) \qquad \text{where} \quad D \approx \frac{V_{OUT}}{V_{IN}}$$

As a point of reference, the worst case current ripple will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_{OUT}$.

Recommended minimum input capacitance is 10µF (including derating) ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is strongly recommended to pay attention to the voltage and temperature deratings of the capacitor selected. It should be noted that current ripple rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

The second criteria is the input voltage ripple.
If the system design requires a certain minimum value of peak-to-peak input voltage ripple ($V_{IN\ ripple}$) then the following equation may be used:

$$C_{IN} \geq \frac{I_{OUT} \cdot D \cdot (1-D)}{f_{SW(CCM)} \cdot V_{IN\ ripple}} \qquad (7)$$

As example, if ΔV_{IN} is 1% of V_{IN} for a 24V input to 3.3V output application, and f_{SW} = 400 kHz this leads:

$$C_{IN} \geq \frac{1A \cdot \frac{3.3V}{24V} \cdot (1-\frac{3.3V}{24V})}{400000 \cdot 0.240V}$$

$$C_{IN} \geq 1.25\mu F$$

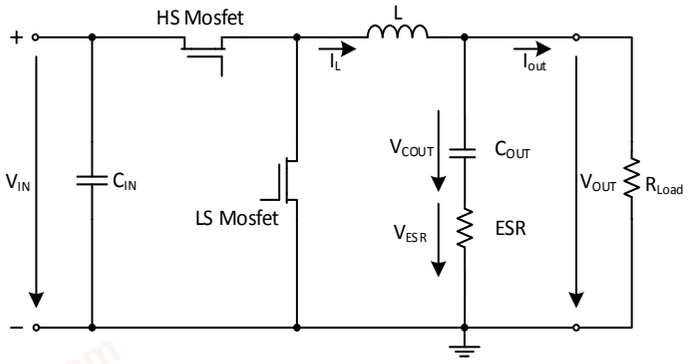
Additional bulk capacitance with higher ESR may be required to damp any resonant effects between the input capacitance and parasitic inductance of the incoming supply lines.

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Step 4 Select output capacitor (C_{OUT})



None of the required output capacitors are integrated within the module. A general recommendation in order to guarantee a stable behavior is to place at least a capacitance of 10µF (MLCC recommended) at the output.
The output capacitor must meet the worst case RMS current rating, as calculated by equation (8):

$$I_{C_{OUTRMS}} = \frac{\Delta I_L}{\sqrt{12}} \quad (8)$$

where ΔI_L is the inductor current ripple calculated with the equation (9)

$$\Delta I_L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{f_{SW} \cdot L \cdot V_{IN}} \quad (9)$$

Selection by output voltage ripple requirements

The output capacitor should be selected in order to minimize the output voltage ripple and provide a stable voltage at the output. Under steady state conditions, the voltage ripple observed at the output can be defined as:

$$V_{OUT\ ripple} = \Delta I_L \cdot ESR + \Delta I_L \cdot \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \quad (10)$$

Very low ESR capacitors, like ceramic and polymer electrolytic, are recommended. If a low ESR capacitor is selected, equation (10) can be simplified and a first condition for the minimum capacitance value can be derived:

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot V_{OUT\ ripple} \cdot f_{SW}} \quad (11)$$

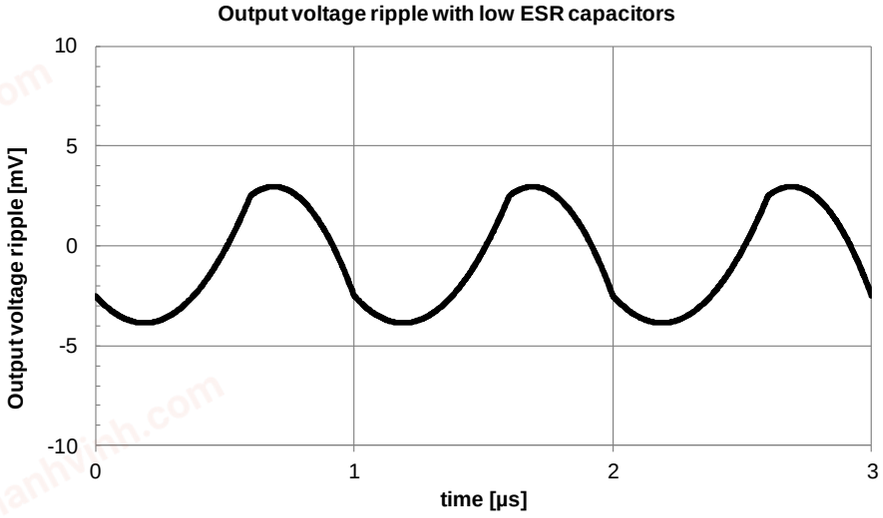
Beyond that, the additional capacitance will reduce the output voltage ripple as long as the ESR is low enough to permit it. Please consider the derating of the nominal capacitance value due to temperature, aging and applied DC voltage (e.g. MLCC X7R up to -50%).

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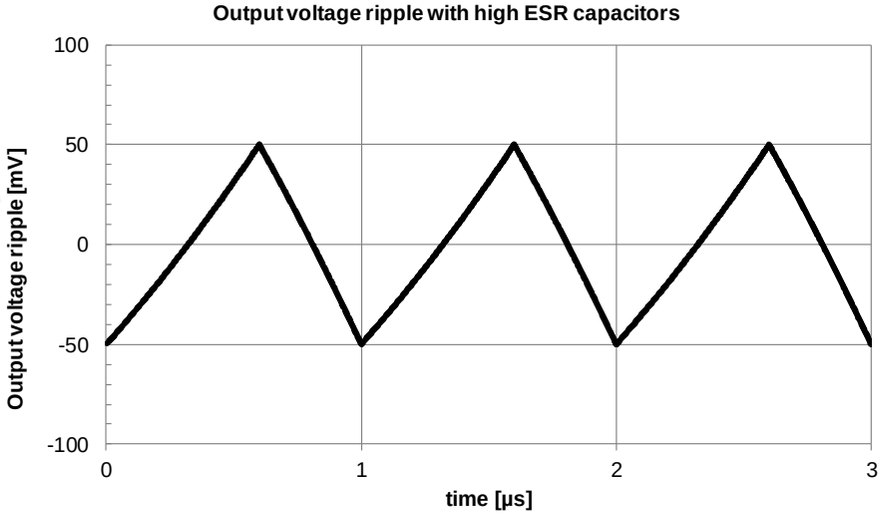
The use of very low ESR capacitors leads to an output voltage ripple as shown below (generic waveform):



When capacitors with slightly higher ESR are utilized, the dominant parameter that influences the output voltage ripple is just the ESR:

$$ESR \leq \frac{V_{OUT\ ripple}}{\Delta I_L} \quad (12)$$

Consequently, the shape of the output voltage ripple changes as shown below (generic waveform):



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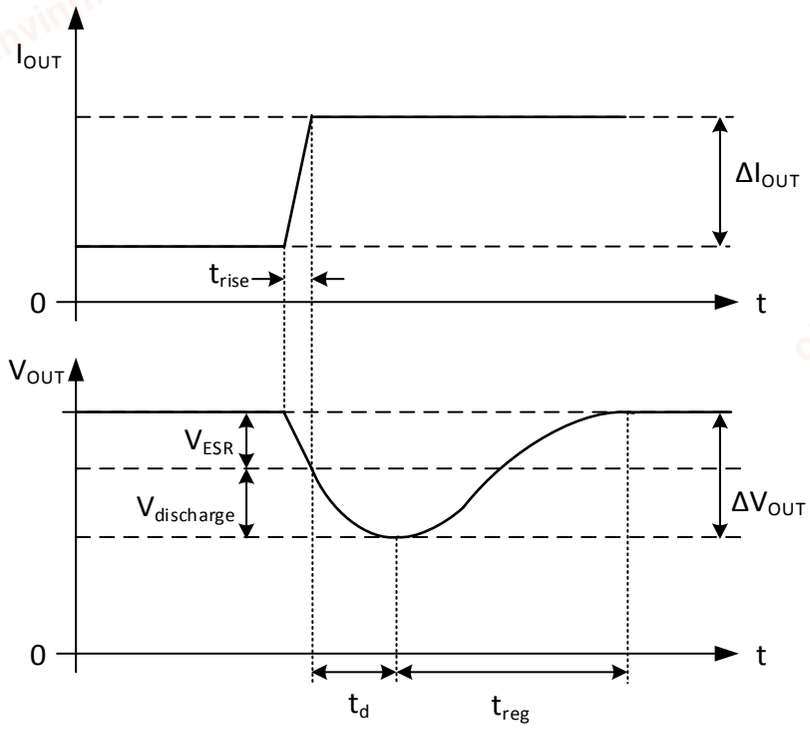
Selection by load step requirements

The output voltage is also affected by load transients (see picture below). The constant on-time control scheme generally provides faster response than the other control loops.

When the output current transitions from a low to a high value, the voltage at the output capacitor (V_{OUT}) drops due to two contributing factors. One is caused by the voltage drop across the ESR (V_{ESR}) and depends on the slope of the rising edge of the current step (t_{rise}). For low ESR values and small load currents, this is often negligible. It can be calculated as follows:

$$V_{ESR}=ESR\cdot\Delta I_{OUT} \quad (13)$$

where ΔI_{OUT} is the load step, as shown in the picture below (simplified: no voltage ripple is shown).



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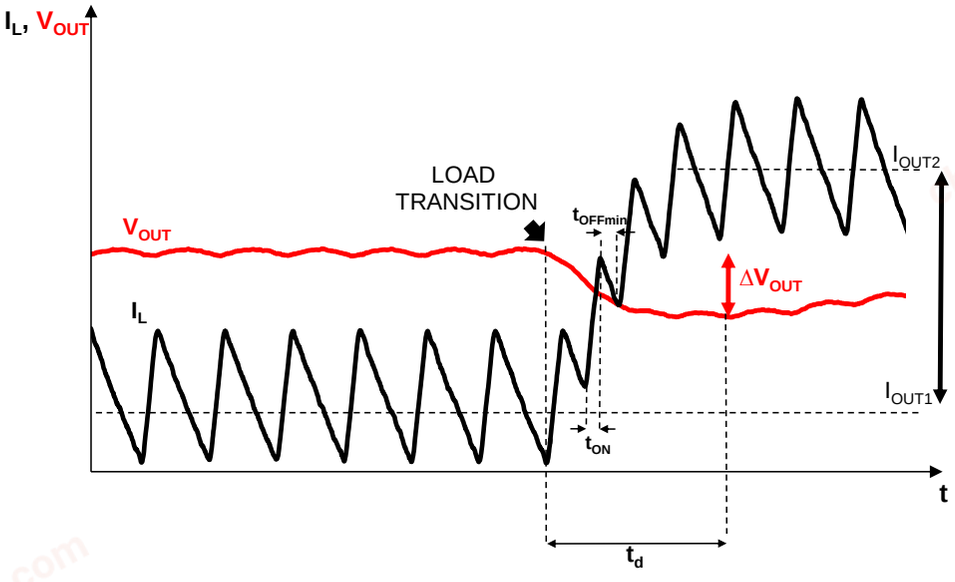
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The second contributing factor is the voltage drop due to the discharge of the output capacitor. In order to estimate this contribution, the behavior of the inductor current during the transient should be analyzed (see picture below, ESR contribution neglected).

At the transition, the device tries to reach the new steady state as fast as possible by increasing the inductor current. This can be achieved only by modulating the off-time t_{OFF} since the on-time is fixed and defined by R_{ON}. The device has a minimum t_{OFF} ($t_{OFF-MIN}$ = 260ns typ.). Therefore, as long as the new steady state is not achieved, the inductor current increases by performing consecutive cycles of t_{ON} and $t_{OFF-MIN}$. During the transition to the new output current, the load demand is supported by the energy stored in the output capacitor. For that reason, the output voltage drops until the average inductor current reaches the new output current. The time for reaching this condition (t_d) can be calculated as follows:

$$t_d = \frac{(\Delta I_{OUT} + \frac{\Delta I_L}{2}) \cdot L \cdot (t_{ON} + t_{OFF-MIN})}{V_{IN} \cdot t_{ON} - V_{OUT} \cdot (t_{ON} + t_{OFF-MIN})} \quad (14)$$

The t_d calculated above represents the worst case, i.e. it is supposed that the load transient occurs when the inductor current has its minimum value ($I_{OUT} - \frac{\Delta I_L}{2}$).



The selection of the C_{OUT} is related to the t_d as well as to the current step ΔI_{OUT} and the max allowed voltage drop ΔV_{OUT}, as shown by the following equation:

$$C_{OUT} \geq \frac{(\Delta I_{OUT} + \frac{\Delta I_L}{2}) \cdot t_d}{2 \cdot \Delta V_{OUT}} \quad (15)$$

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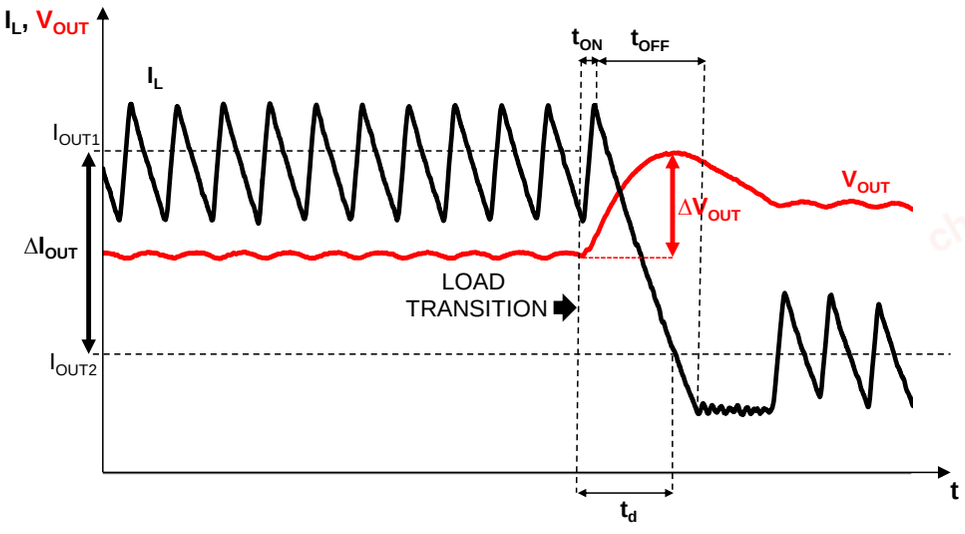
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The same equation can be used for calculating the minimum required capacitance for an output current transition from high to low (see picture below). Since the inductor current must reach the new steady state with a lower value than before, there is no need to trigger a new on-time cycle. Instead, the off-time is extended until the average inductor current reaches the new load current value. The excess of current during this time charges the output capacitor. This causes the output voltage to increase and an overshoot occurs. The time t_d for reaching the new steady state can be calculated for a negative load transient with the following equation:

$$t_d = \frac{L}{V_{OUT}} \cdot \left(\frac{\Delta I_L}{2} + \Delta I_{OUT}\right) + t_{ON} \qquad (16)$$

The equation (16) shows the worst case in terms of the current ($I_{OUT} + \frac{\Delta I_L}{2}$) as well as in terms of time. The inclusion of t_{ON} in the formula takes into account a new on-time triggered in case the load transient occurs at the end of the off-time. Under this condition a new on-time is generated because the device has not yet reacted to the transient and to the consequent deviation of V_{OUT} from its steady state value (see figure below).



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Example
The following application conditions are used as an example to show how to calculate a suitable C_{OUT} value:

- V_{IN} = 24V
- V_{OUT} = 5V
- R_{ON} = 75kΩ
- load transient from 0.5A to 1A and vice versa (ΔI_{OUT} = 0.5A)
- max allowed undershoot or overshoot ΔV_{OUT} = 100mV

The C_{OUT} can be calculated using the equation (15) on page 24. This equation provides two possible values depending on whether t_d is calculated for a positive load transient (generating a V_{OUT} drop) or for a negative load transient (resulting in a V_{OUT} overshoot).

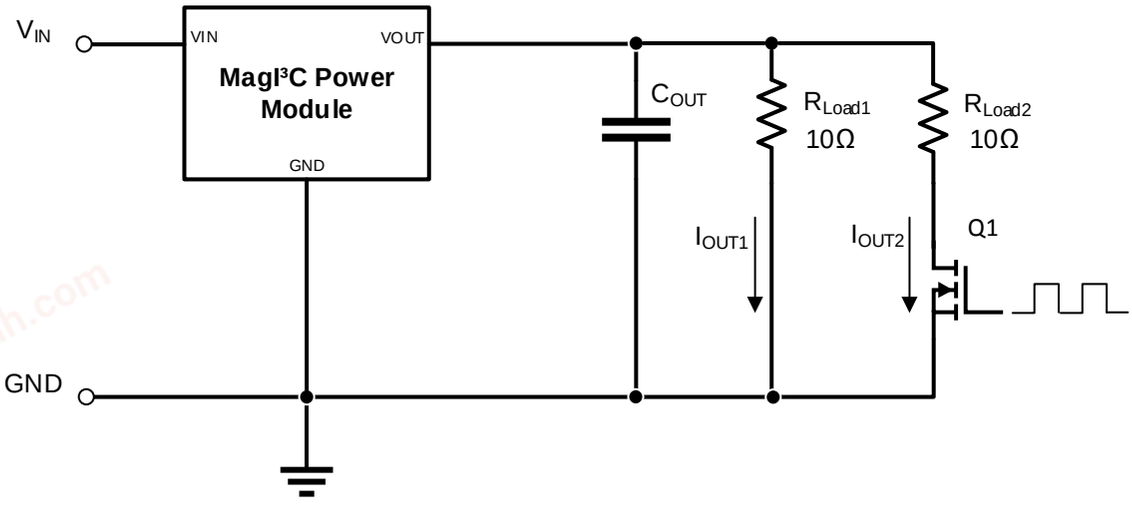
In case of positive load transient: t_d = 920ns and $C_{OUT} \geq$ 4.1µF
In case of negative load transient: t_d = 2.18µs and $C_{OUT} \geq$ 9.6µF

A combination of 10µF (Würth Elektronik, part number 885012109008) + 4.7µF (885012109008) MLCC are selected. Some margin from the calculated C_{OUT} value is recommended in order to take into account:

- Approximations within the equations to estimate td and C_{OUT} itself;
- Tolerances and variations of some components and parameters involved in those equations (e.g. R_{ON}, $t_{OFF-MIN}$, L, k, etc.)
- Derating of the capacitors with DC applied voltage and temperature

The use of two MLCCs in parallel contributes to the further reduction of the total ESR.

The load transients with the selected C_{OUT} can be tested using the setup depicted below:

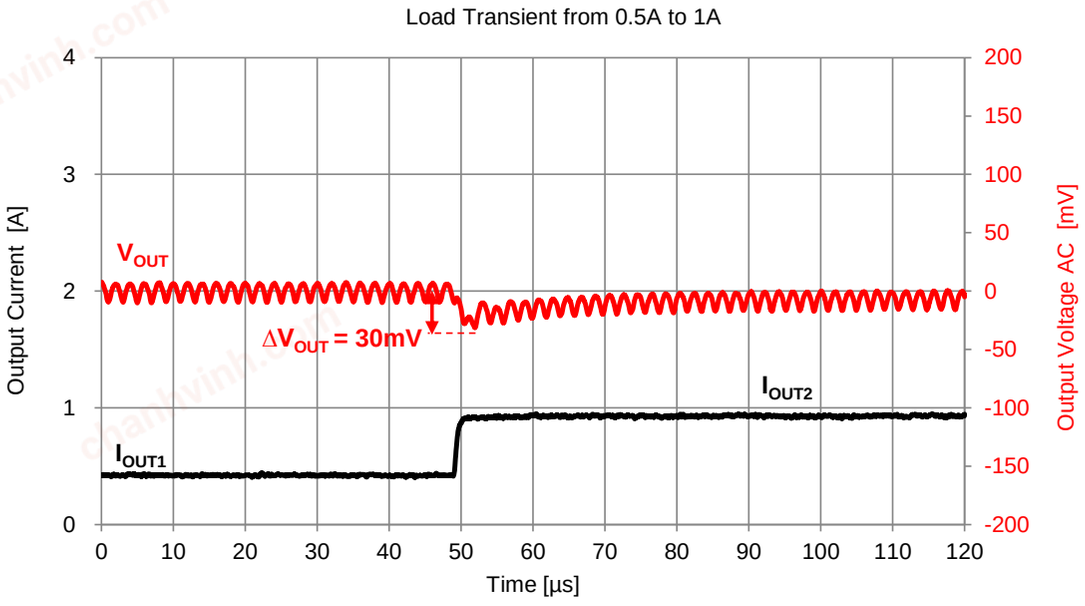


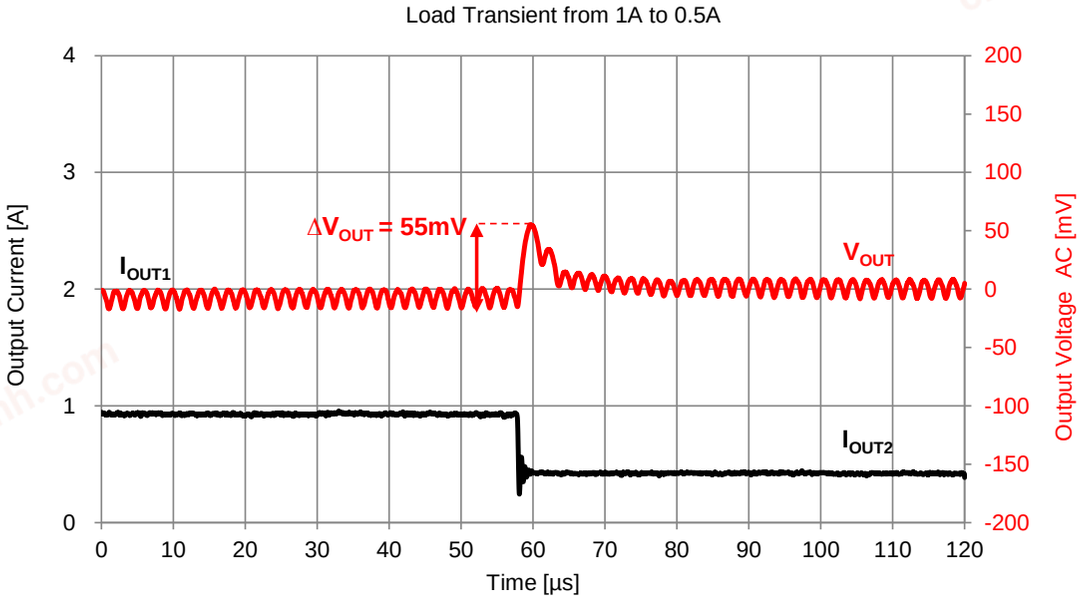
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The results of the load transient tests with the selected C_{OUT} are shown below:





In both the positive and the negative transition, the ΔV_{OUT} is significantly below the target (100mV). The explanation of the strong reduction of the ΔV_{OUT} lies in the use of a capacitance value higher than the one calculated.

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Step 5 Select the feed forward capacitor (C_{FF})

A feed-forward capacitor C_{FF} is placed in parallel with R_{FBT} that bypasses AC ripple directly to the feedback pin from the output to support the internal ripple generator. This capacitor also affects the load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM and adjusting for best transient response and minimum output ripple. A value of 22nF has been practically evaluated as the best choice. The feed forward capacitor C_{FF} should be located close to the FB pin.

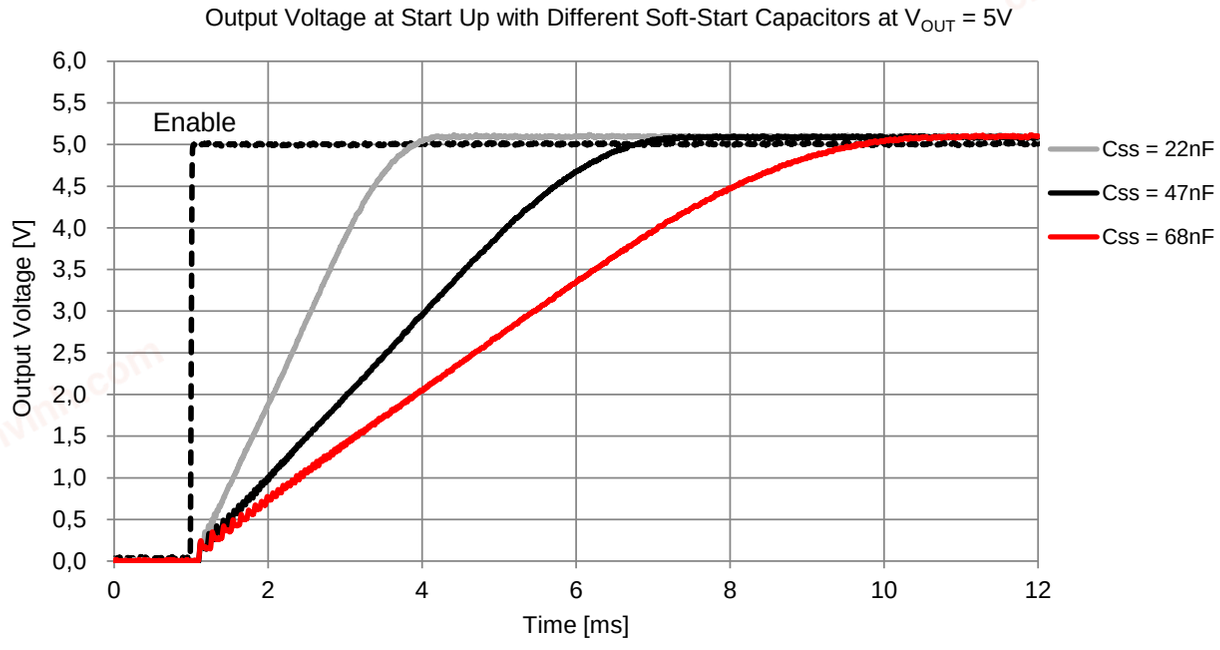
Step 6 Select soft-start capacitor (C_{SS})

A minimum soft-start capacitance of 22nF is required. Programmable soft-start permits the regulator to slowly ramp up to its steady state operating point after being enabled, thereby reducing the input current at start-up and slowing the output voltage rise-time to prevent overshoot. Upon turn-on, after all UVLO conditions have been passed, an internal 8µA current source begins charging the external soft-start capacitor. The soft-start capacitor can be calculated with:

$$C_{SS} = t_{SS} \cdot \frac{8\mu A}{0.8V} \quad (17)$$

Where t_{SS} in the desired soft-start time in milliseconds. The use of a 22nF capacitor results in 2.2ms soft-start duration.

As the soft-start input exceeds 0.8V the output of the power stage will be in regulation. The soft-start capacitor continues charging until it reaches approximately 3.8V on the SS pin. Voltage levels between 0.8V and 3.8V do not influence the regulation of the output voltage.
The picture below shows the output voltage under three different soft-start conditions:



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Note that high values of the C_{SS} capacitance will cause more output voltage droop when a load transient goes across the DCM-CCM boundary. Use equation (22) in the "LIGHT LOAD OPERATION" section (page 33) to find the DCM-CCM load current boundary for the specific operating conditions. If a fast load transient response is desired for steps between DCM and CCM mode the soft-start capacitor value should be less than 0.018µF. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200µA current sink:

1. The enable input being "pulled low"
2. Thermal shutdown condition
3. Overcurrent fault
4. Internal UVLO at input

Step 7 Optional: select enable divider, R_{ENT}, R_{ENB} (external UVLO)

The enable input provides a precise 1.18V reference threshold to allow a direct logic drive or connection to a voltage divider from a higher voltage such as V_{IN}. The enable input also incorporates 90mV (typ.) of hysteresis resulting in a falling threshold of 1.09V. The maximum recommended voltage into the EN pin is 6.5V. For applications where the midpoint of the enable divider exceeds 6.5V, a small zener diode can be added to limit this voltage.

The function of the R_{ENT} and R_{ENB} divider shown in the application block diagram is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable external under voltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turn-on of the supply as the main input voltage rail rises at power-up. Most systems will benefit by using the precision Enable threshold to establish a system under voltage lockout. Without an external enable divider the device would attempt to turn on around V_{IN} = 3.5V. In case of output voltages higher than this turn on threshold, the V_{OUT} follows the V_{IN} as long as $V_{IN}<V_{OUT}$ and it might not have a monotonic rise. However many systems need a smooth rise in the supply voltage. Therefore the recommended approach is to choose an input UVLO level that is higher than the target regulated output voltage. In case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the MagI³C power module output rail. The two resistors should be chosen based on the following ratio:

$$\frac{R_{ENT}}{R_{ENB}} = \frac{V_{UVLO\ (external)}}{1.18V} - 1 \qquad (18)$$

$V_{UVLO\ (external)}$ = User programmable voltage threshold to turn the module ON/OFF.

The EN pin is internally pulled up to V_{IN} and can be left floating for always-on operation. However, it is good practice to use the enable divider and turn on the regulator when V_{IN} is close to reaching its nominal value. This will guarantee smooth start up behavior and will prevent overloading the input supply.

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DETERMINE POWER LOSSES AND THERMAL REQUIREMENTS OF THE BOARD

This section provides an example of calculation of power losses and thermal design of the board.
As a starting point the following application conditions can be considered:

V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=1A, $T_{A(MAX)}$ =85°C and $T_{J(MAX)}$=125°C

where T_A is the maximum air temperature surrounding the module and $T_{J(MAX)}$ is the maximum value of the junction temperature according to the limits in the "OPERATING CONDITIONS" section on page 4.
The goal of the calculation is to determine the characteristics of the required heat sink. In the case of a surface mounted module this would be the PCB (number of layers, copper area and thickness). These characteristics are reflected in the value of the case to ambient thermal resistance (θ_{JA}).
The basic formula for calculating the operating junction temperature T_J of a semiconductor device is as follows:

$$T_J = P_{IC\text{-}LOSS} \cdot \theta_{JA} + T_A \quad (19)$$

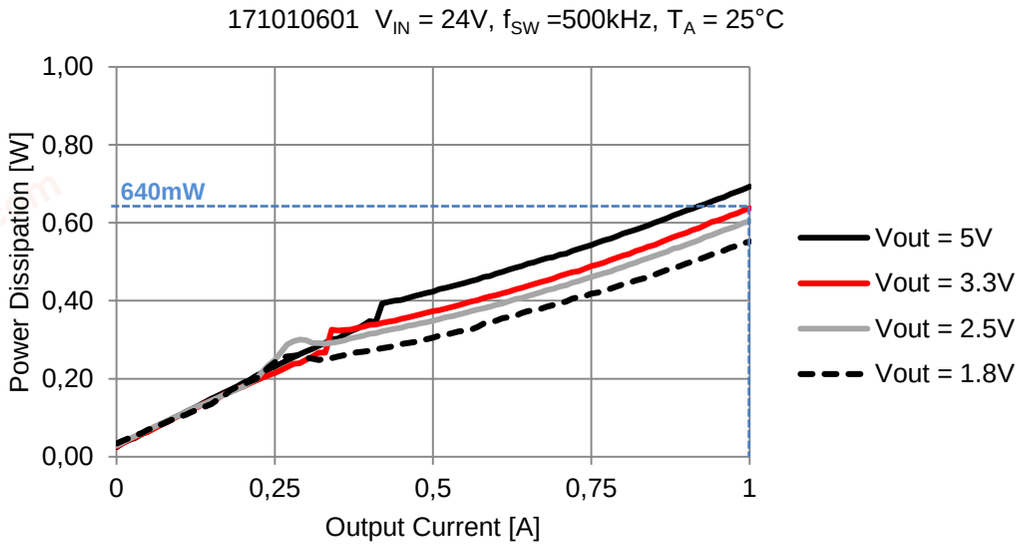
$P_{IC\text{-}LOSS}$ are the total power losses within the module´s IC and are related to the operating conditions.
Θ_{JA} is the junction to ambient thermal resistance and calculated as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (20)$$

Θ_{JC} is the junction to case thermal resistance.
Combining equations (19) and (20) results in the maximum case-to-ambient thermal resistance:

$$\theta_{CA(MAX)} < \frac{T_{J(MAX)} - T_{A(MAX)}}{P_{IC\text{-}LOSS}} - \theta_{JC} \quad (21)$$

From section "THERMAL SPECIFICATIONS" (page 4) the typical thermal resistance from junction to case (θ_{JC}) is defined as 1.9 °C/W. Use the 85°C power dissipation curves in the "TYPICAL PERFORMANCE CURVES" section (page 12) to estimate the $P_{IC\text{-}LOSS}$ for the application being designed.



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From the graph a power loss of 640mW is read. Entering the values in formula (21) results in:

$$\theta_{CA(MAX)} < \frac{125°C - 85°C}{0.64W} - 1.9°C/W = 60.6°C/W$$

$$\theta_{JA(MAX)} = \theta_{JC} + \theta_{CA(MAX)} = 1.9°C/W + 60.6°C/W = 62.5°C/W$$

In order to achieve a $\theta_{JA} < 62.5°C/W$ it would be sufficient to use the minimum area for placing the external components, in accordance with the indications in the "LAYOUT RECOMMENDATION" section on page 39.

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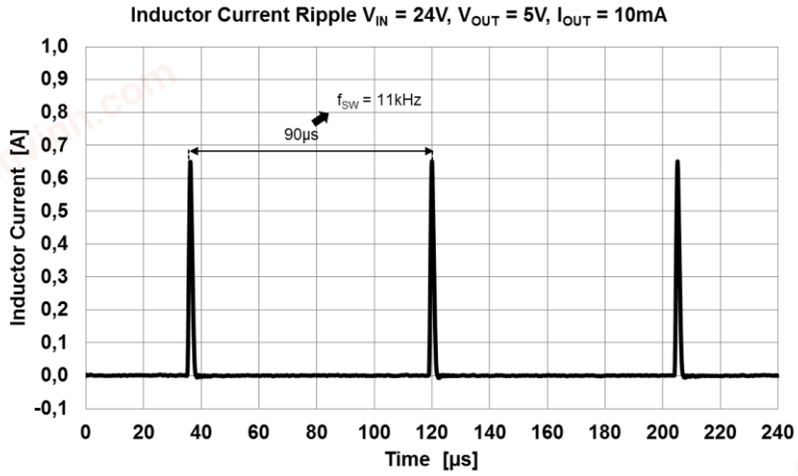
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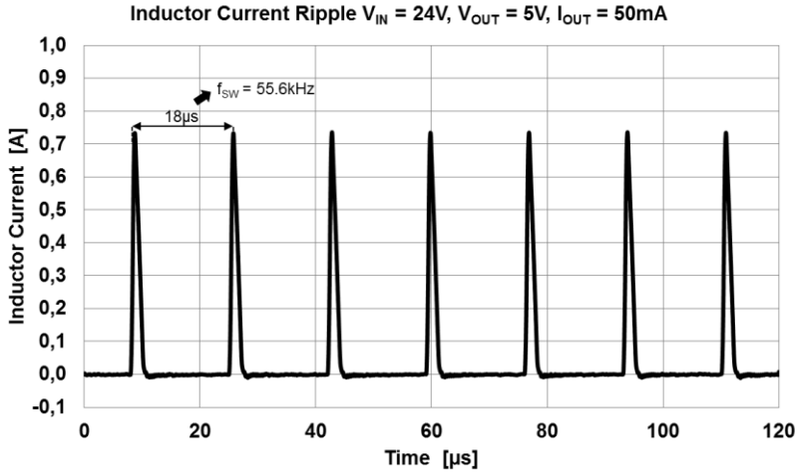
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LIGHT LOAD OPERATION

Under light load conditions, the device continuously decreases the switching frequency and thereby maintains a high efficiency.

At light load, the regulator will operate in Discontinuous Conduction Mode (DCM). When the load current is above the critical conduction point, it will operate in Continuous Conduction Mode (CCM). When operating in DCM the switching cycle begins at an inductor current of zero ampere, increases up to a peak value, and then recedes back to zero before the end of the off-time. Note that during the period of time when the inductor current is zero, all load current is supplied by the output capacitor. The next on-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. The pictures below depict how the current flows in the inductor during the DCM operation with two different load current (10mA and 50mA).





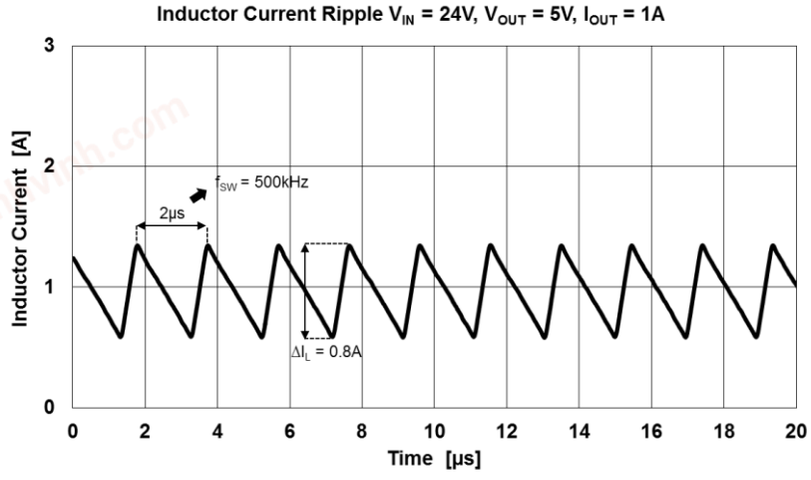
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In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using the equation below.



The load current where the transition between DCM and CCM takes place can be estimated using the following formula:

$$I_{OUT(DCM)} = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2 \cdot f_{SW} \cdot L} \quad (22)$$

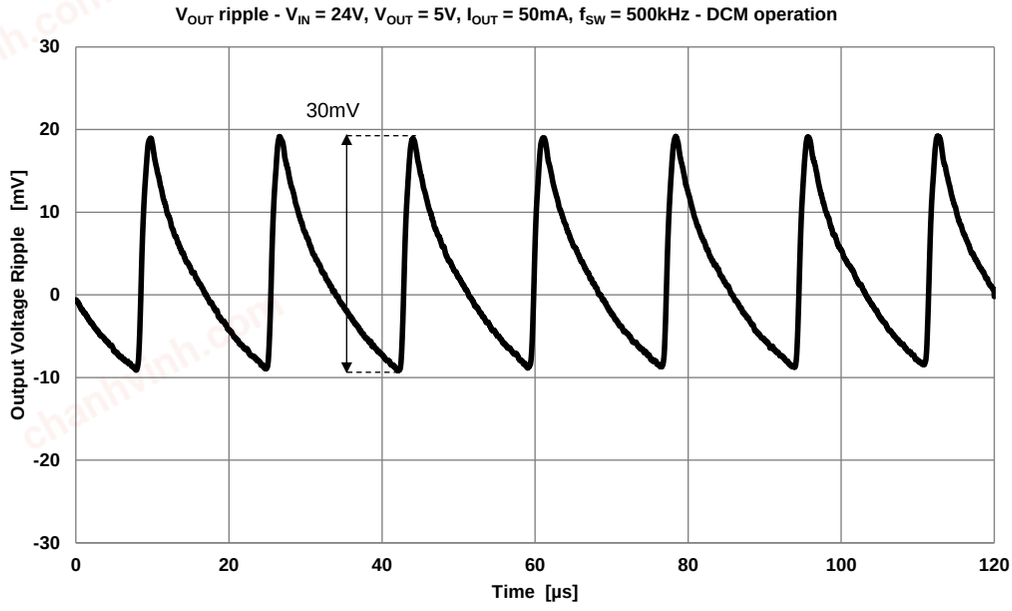
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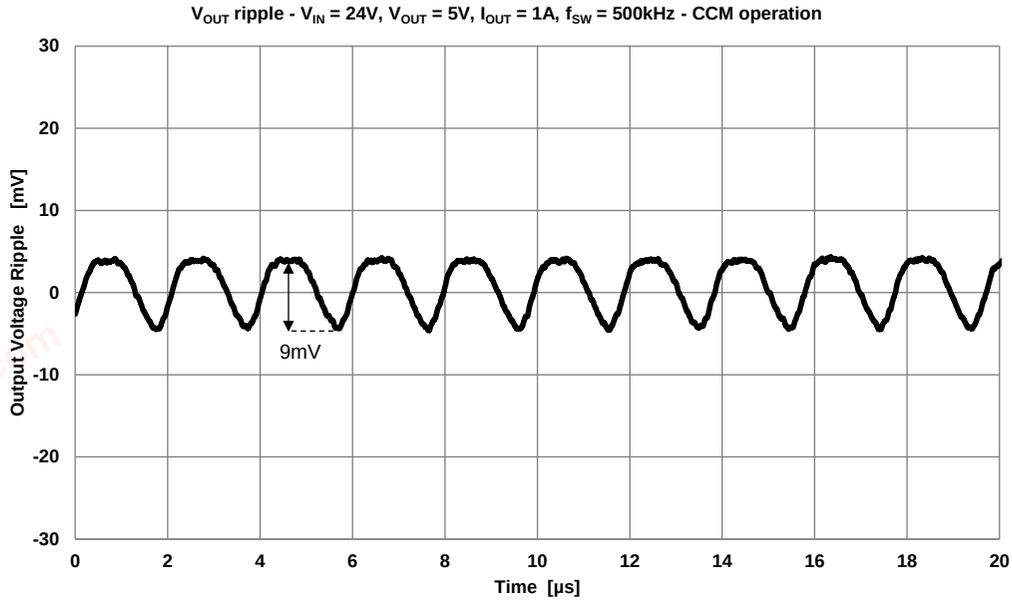
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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

OUTPUT VOLTAGE RIPPLE

The output voltage ripple of the V_{OUT} depends on several parameters, as already shown in DESIGN FLOW – Step4. The operating mode (CCM or DCM) further influences the output voltage ripple as shown in the two figures below:





The output voltage ripple during CCM operation is much lower (<10mV$_{pp}$) than the ripple during DCM operation (around 30mV$_{pp}$).

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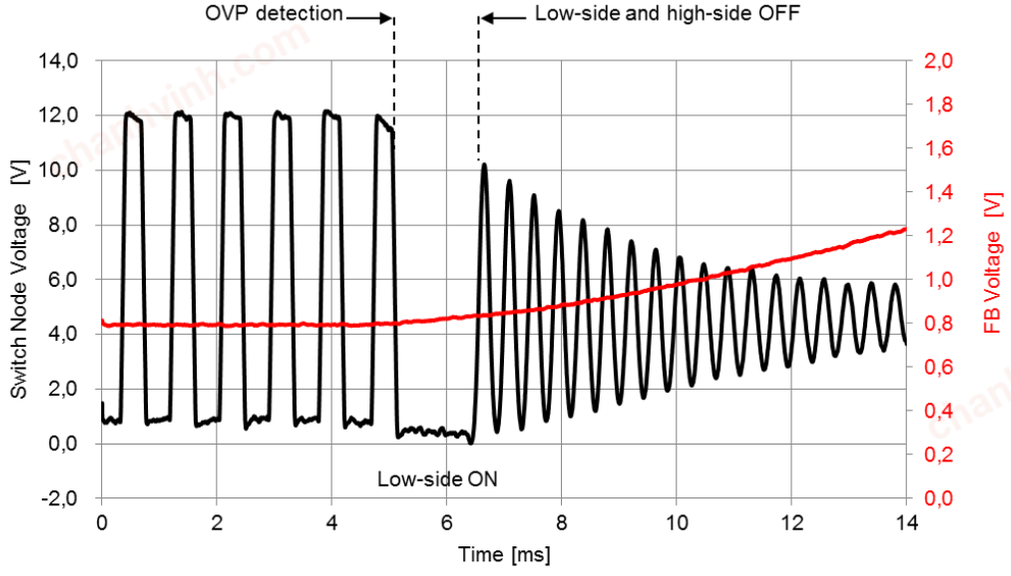
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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

PROTECTIVE FEATURES

Output Overvoltage Protection (OVP)

The voltage at the FB is compared to a 0.8V internal reference while the overvoltage protection (OVP) has a threshold of 0.92V. If FB rises above this limit, the on-time is immediately terminated. It can occur if the input voltage is increased with a very high $\frac{dV_{IN}}{dt}$ or if the output current is decreased with a very $\frac{dI_{OUT}}{dt}$. Once OVP is activated, the high-side MOSFET on-times will be inhibited until the condition clears. Additionally, the low-side MOSFET will remain on until the inductor current falls to zero. Then both high-side and low-side MOSFETs are turned off as long as the overvoltage condition is not removed (see figure below).



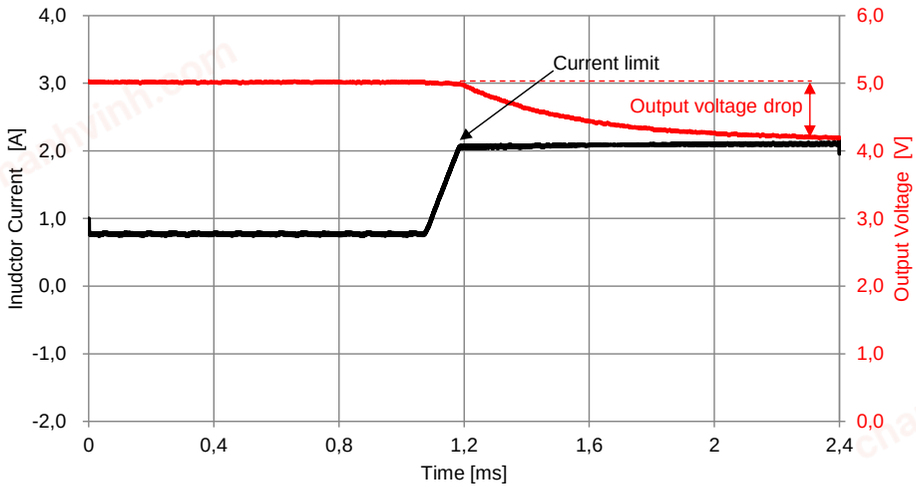
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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

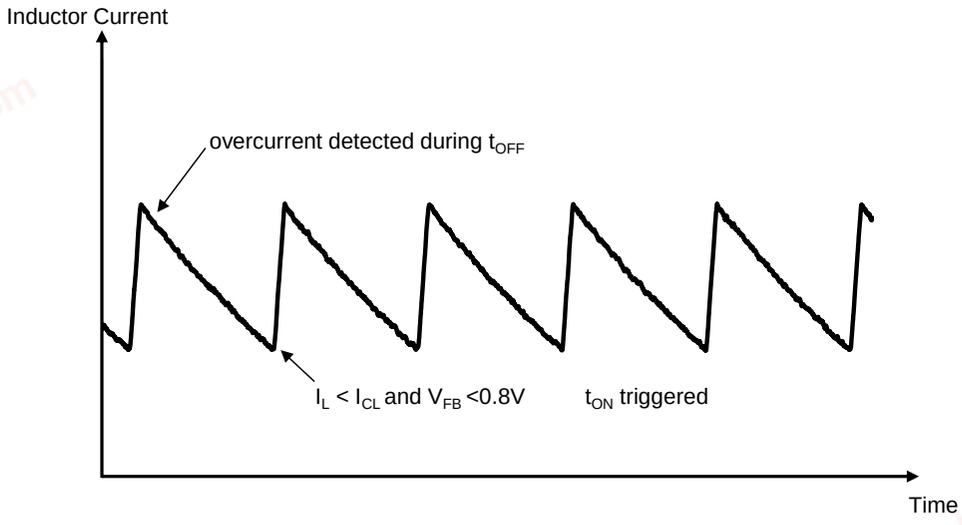
Overcurrent protection (OCP)

Current limit detection is carried out during the off-time by monitoring the current in the low-side MOSFET. Referring to the Functional Block Diagram, when the high-side MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal low-side MOSFET. If this current exceeds the I_{CL} value, the current limit comparator disables the start of the next on-time period. The inductor current is monitored during the off-time. As long as the inductor current exceeds I_{CL}, further on-time intervals will not occur. The next switching cycle will occur only if the FB input is less than 0.8V and the inductor current has decreased below I_{CL} (see figure below). The switching frequency is lower during current limited operation due to the longer off-time.
Due to the current limitation the output voltage drops (see figure below). It should also be noted that the DC current limit varies with the duty cycle, switching frequency, and temperature. At continuous overcurrent load the module junction temperature increase until the overtemperature protection (OTP) is triggered.



Short circuit protection

In case of short circuit, the device detects the condition during the off-time monitoring the current in the low-side MOSFET. As long as the current remains above I_{CL}, the start of the next on-time is prevented. A new on-time cycle occurs when the current falls below I_{CL} (under short condition V_{OUT} = 0 and V_{FB} = 0, therefore the condition V_{FB}<0.8V is always fulfilled). The device alternates very short on-time and extended off-time (see figure below).



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Overtemperature protection (OTP)

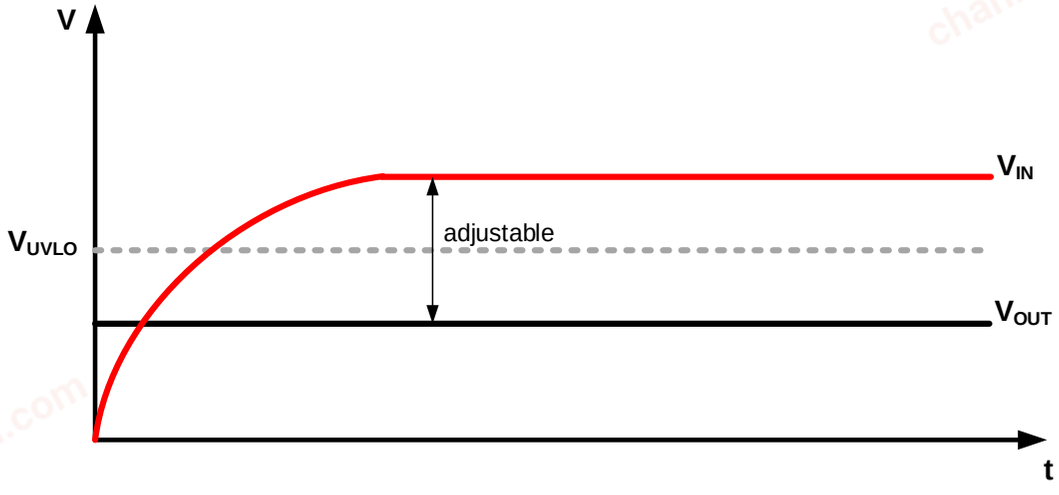
The junction temperature of the MagI³C power module should not be allowed to exceed its maximum rating. Thermal protection is implemented by an internal thermal shutdown circuit which activates at 165°C (typ.) causing the device to enter a low power standby state. In this state, the high-side MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps to prevent catastrophic failures in case of accidental device overheating. When the junction temperature falls back below 150°C (typical hysteresis = 15°C) the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes.

Zero coil current detection (ZCCT)

The current of the low-side MOSFET is monitored by a zero coil current detection circuit that inhibits the low-side MOSFET when its current reaches zero until the next on-time. This circuit prevents a negative inductor current and enables the DCM operating mode. In this way the efficiency at light loads is improved, also because the output capacitor is not discharged by the negative current.

Start up into pre-biased load

The MagI³C power module will properly start up into a pre-biased output. This start up situation is common in multiple rail logic applications where current paths may exist between different power rails during the start up sequence. The UVLO threshold must be set higher than the pre-bias level of the output voltage (see figure below). This will prevent the pre-biased output from enabling the regulator through the high-side MOSFET body diode.

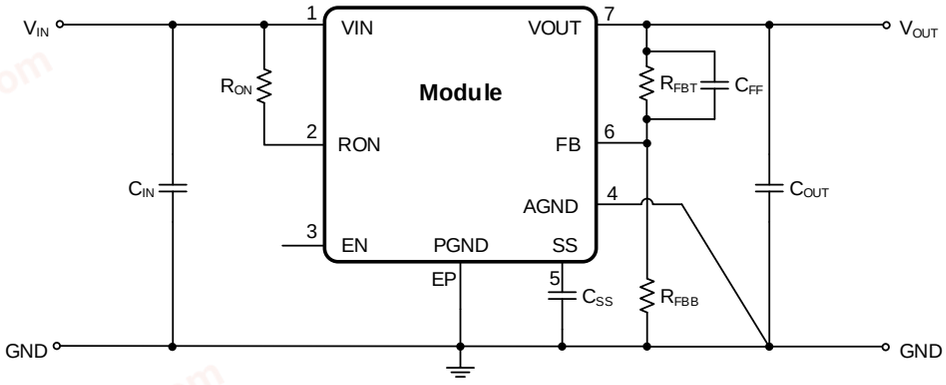


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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

TYPICAL SCHEMATIC



Quick setup guide

Conditions: T_A = 25°C, I_{OUT} = 1A

Recommended component values

V_{OUT}	5V	3.3V	2.5V	1.8V	1.5V	1.2V
R_{FBT}	5.62kΩ	3.32kΩ	2.26kΩ	1.87kΩ	1.00kΩ	4.22kΩ
R_{FBB}	1.07kΩ	1.07kΩ	1.07kΩ	1.5kΩ	1.13kΩ	8.45kΩ
R_{ON}	100kΩ	61.9kΩ	47.5kΩ	32.4kΩ	28.0kΩ	22.6kΩ
C_{IN}	10µF					
C_{OUT}	100µF					
C_{SS}	0.022µF					
C_{FF}	0.022µF					
V_{IN}	7.5-42V	6-42V	6-30V	6-25V	6-21V	6-19V

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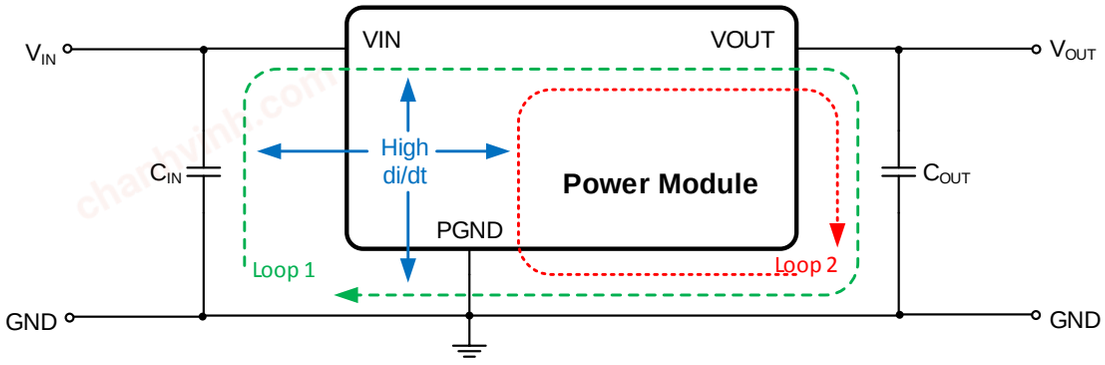
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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

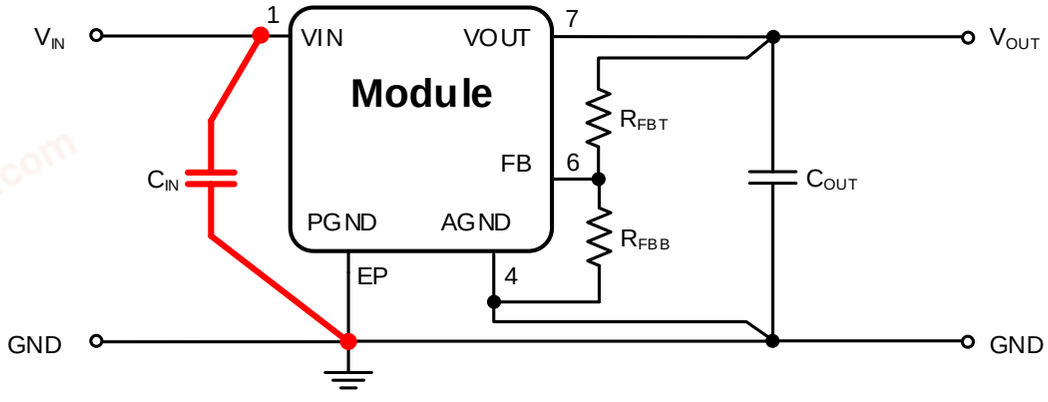
LAYOUT RECOMMENDATION

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. A good layout can be implemented by following simple design rules.

1: Minimize the area of switched current loops.



The target is to identify the paths in the system that have discontinuous current flow. They are the most critical ones because they act as an antenna and cause observable high frequency noise (EMI). The easiest approach to find the critical paths is to draw the high current loops during both switching cycles and identify the sections which do not overlap. They are the ones where no continuous current flows and high di/dt is observed. Loop1 is the current path during the ON-time of the high-side MOSFET. Loop2 is the current path during the OFF-time of the high-side MOSFET.



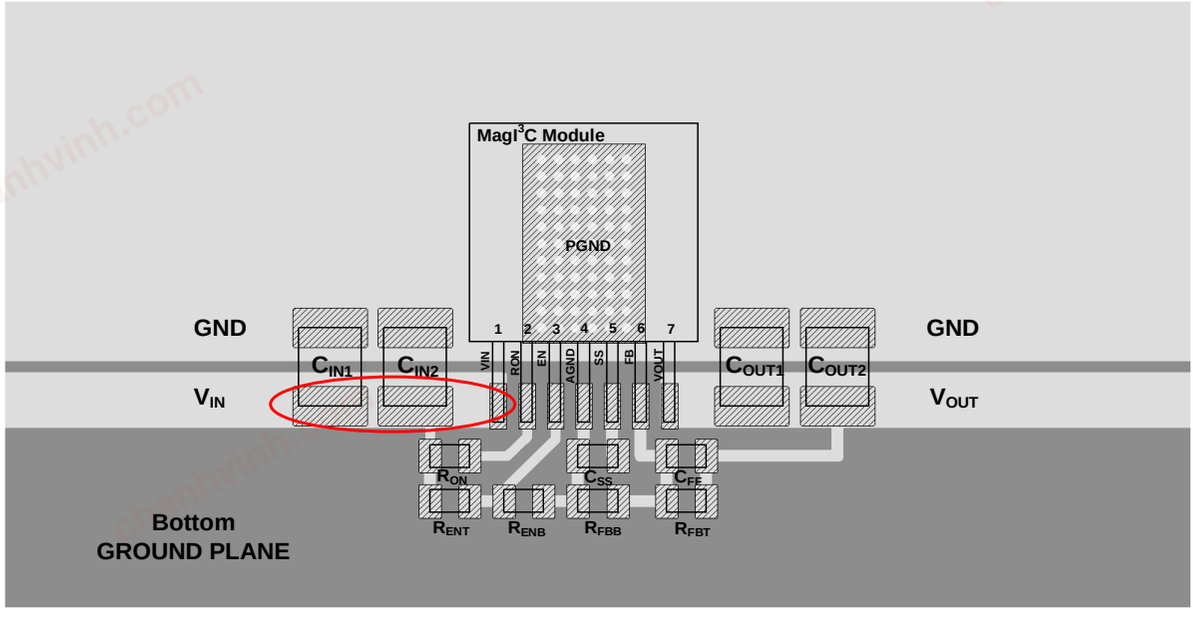
Based on those considerations, the path of the input capacitor C_{IN} is the most critical one to generate high frequency noise on V_{IN}. Therefore place C_{IN} as close as possible to the MagI³C power module V_{IN} and PGND exposed pad EP. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND exposed pad.

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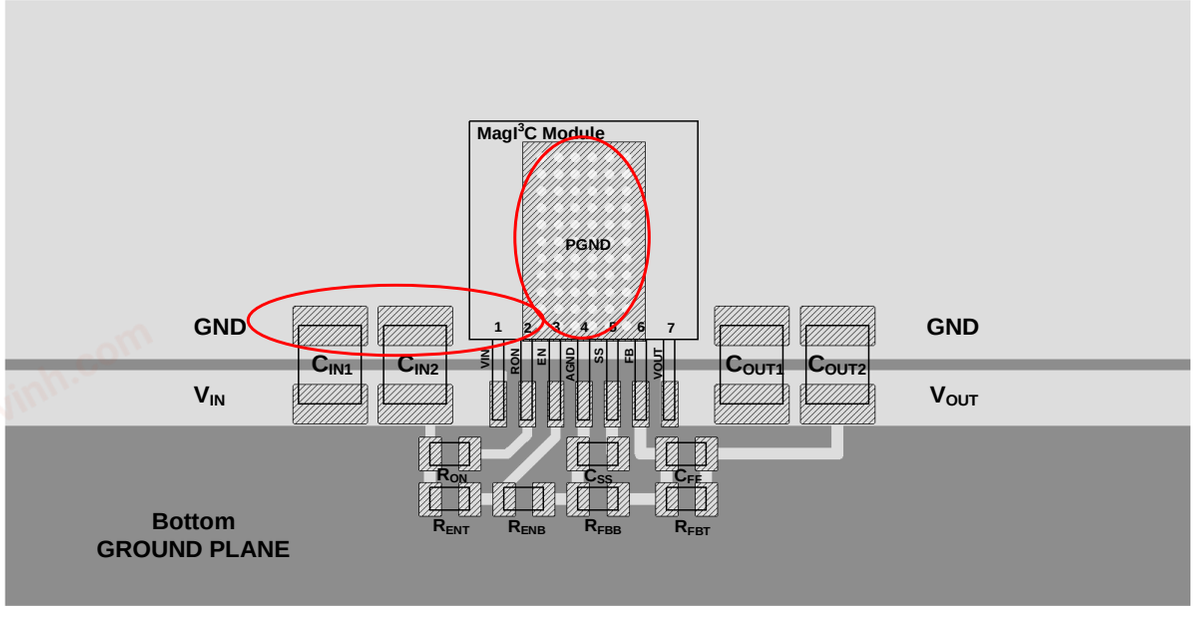
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

The placement of the input capacitors is highlighted in the following picture.



PCB color coding: Top layer Bottom layer

The positive terminal of C_{IN1} and C_{IN2} need to be very close to the VIN pin of the power module.



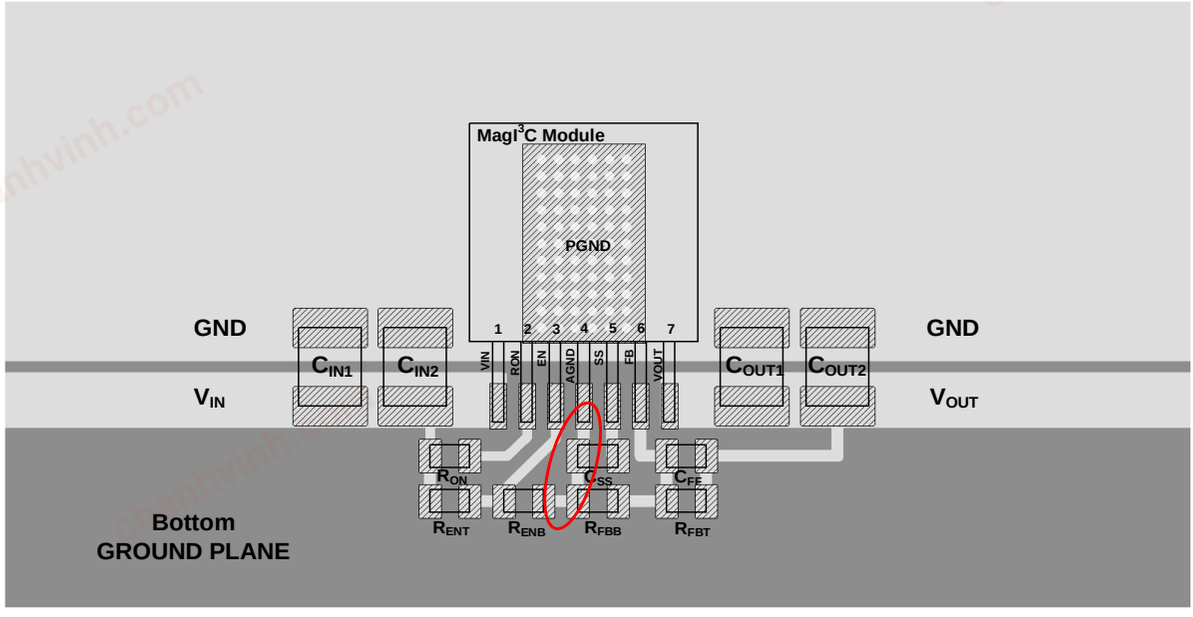
The negative terminal of C_{IN1} and C_{IN2} needs to be very close to the PGND pad of the power module.

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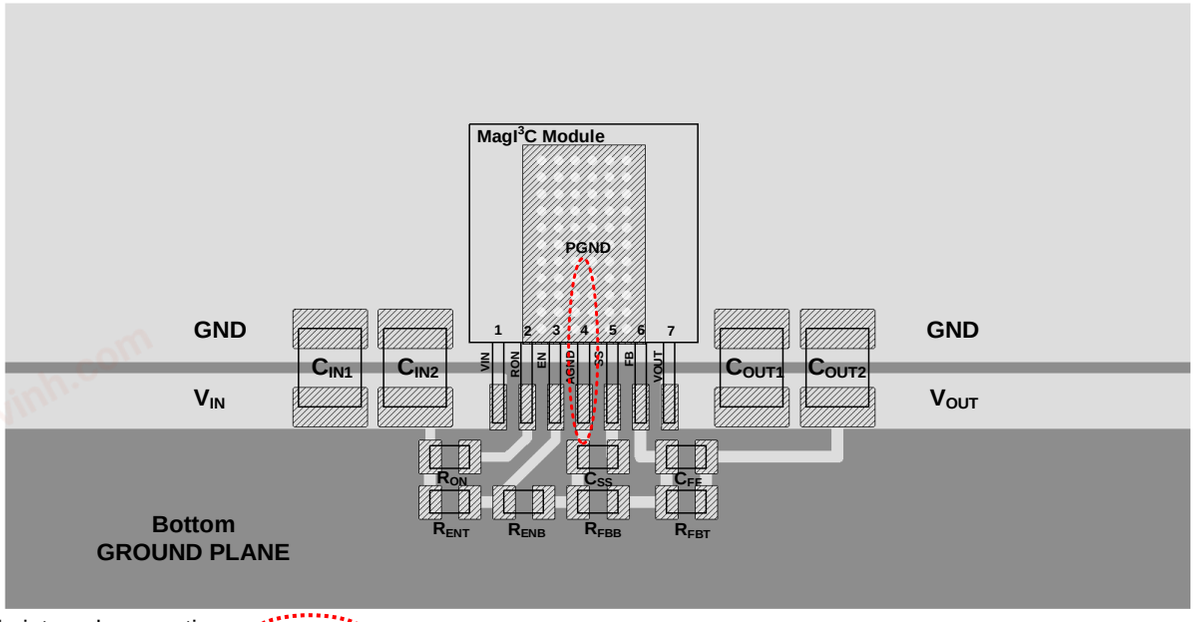
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

2: Analog Ground (AGND) connections



The ground connections for the soft-start capacitor (C_{SS}), the output voltage lower resistor divider (R_{FBB}) and enable components (when used) should be routed to the AGND pin of the device. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Place C_{SS}, R_{FBT} and R_{FBB} close to their respective pins.

3: Analog Ground (AGND) to Power Ground (PGND) connections



Module internal connection:

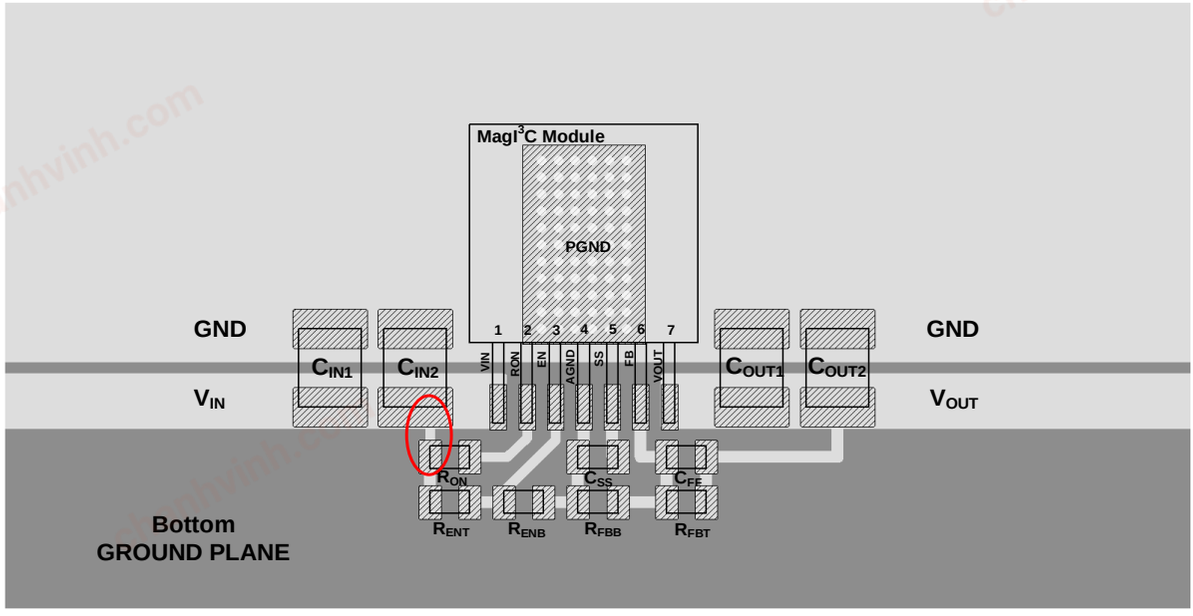
The AGND is **internally connected** to PGND at a low noise node. The output ground current is flowing from the PGND pad through the ground plane through the ground terminal of the first output capacitor. Due to its very low ripple it will not inject noise in the ground plane.

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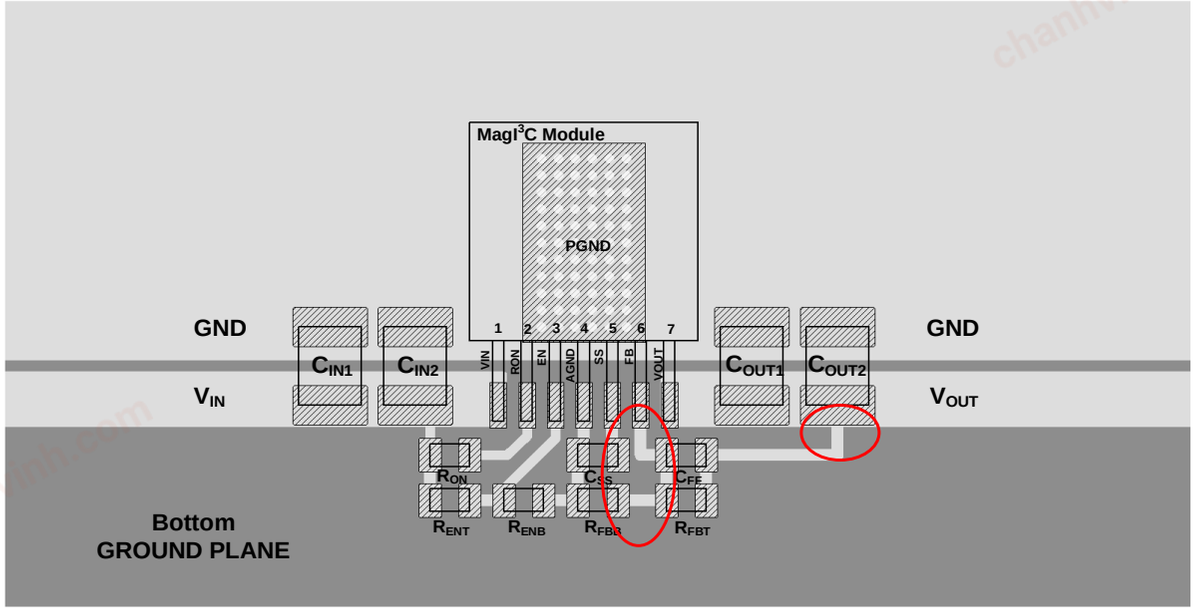
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

4: Connection to VIN



In order to avoid noise injection into RON pin, the resistor R_{ON} should be routed to one of the input capacitors.

5: Feedback layout



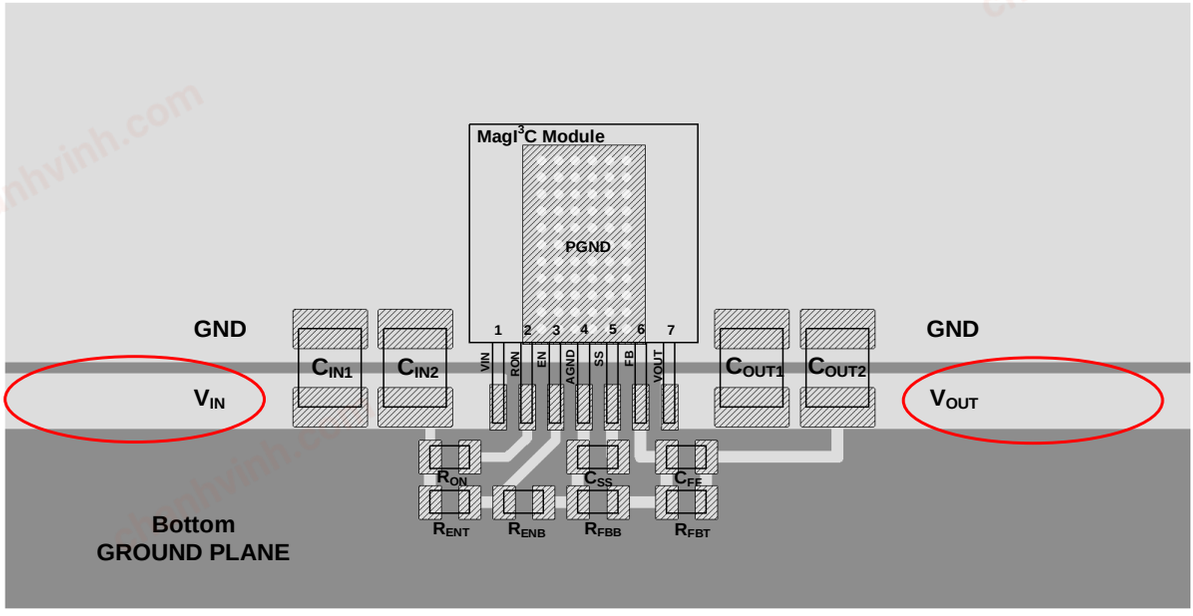
The resistor divider (R_{FBT} and R_{FBB}) should be located close to the FB pin. Since the FB node is high impedance, the trace thickness should be kept small. The traces from the FB pin to the middle point of the resistor divider should be as short as possible. The upper terminal of the output resistor divider (where the V_{OUT} is normally applied) should be connected to the positive terminal of the last output capacitor (C_{OUT2}), because this is the node with the lowest noise. The traces from R_{FBT}, R_{FBB} and C_{FF} should be routed away from the body of the MagI³C Power Module to minimize noise pickup.

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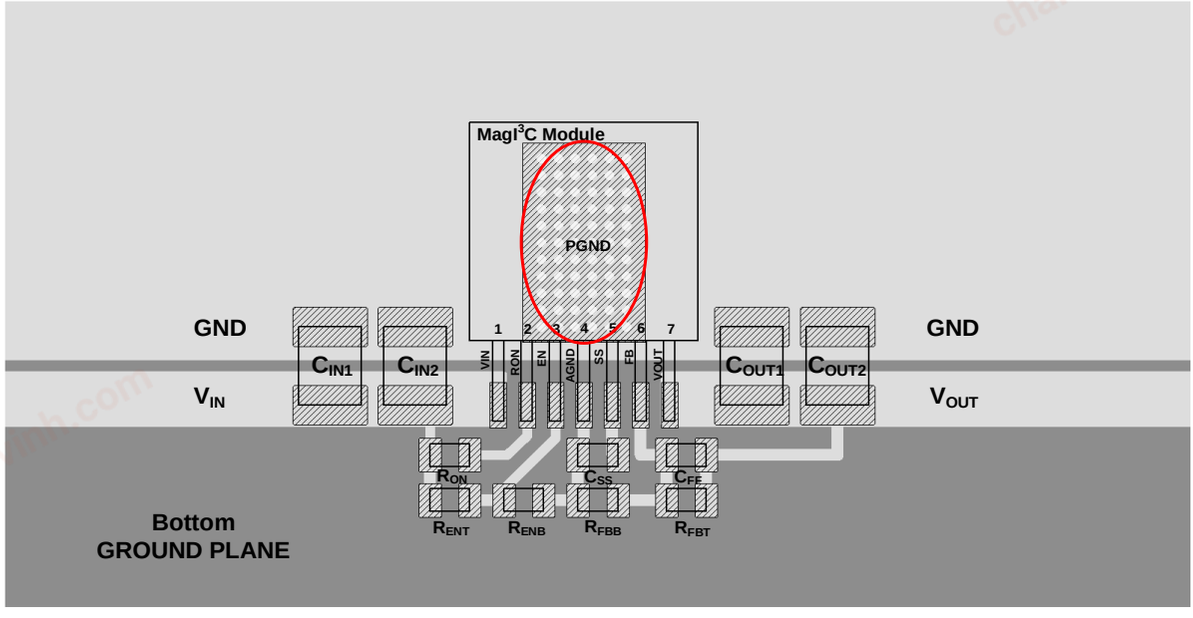
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

6: Make input and output bus connections as wide as possible



This reduces any voltage drops on the input or output of the converter and maximizes efficiency.

7: Provide adequate device heat-sinking

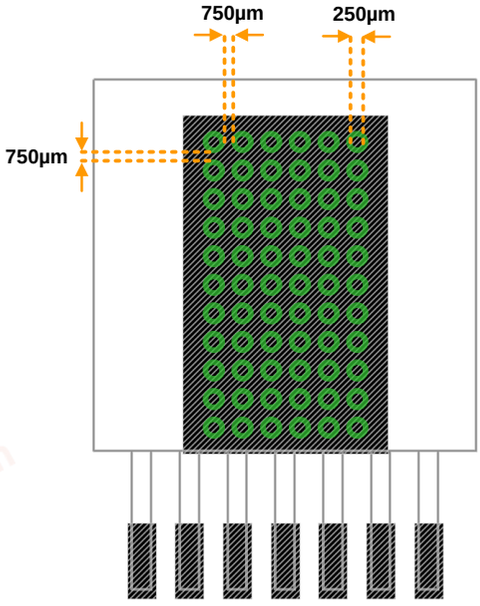


Place a dedicated PGND copper area beneath the MagI³C Power Module.
Use an array of heat-sinking vias to connect the PGND pad to the ground plane on the bottom PCB layer. If the PCB has multiple of copper layers, these thermal vias can also be used to make a connection to the heat-spreading ground planes located on inner layers.

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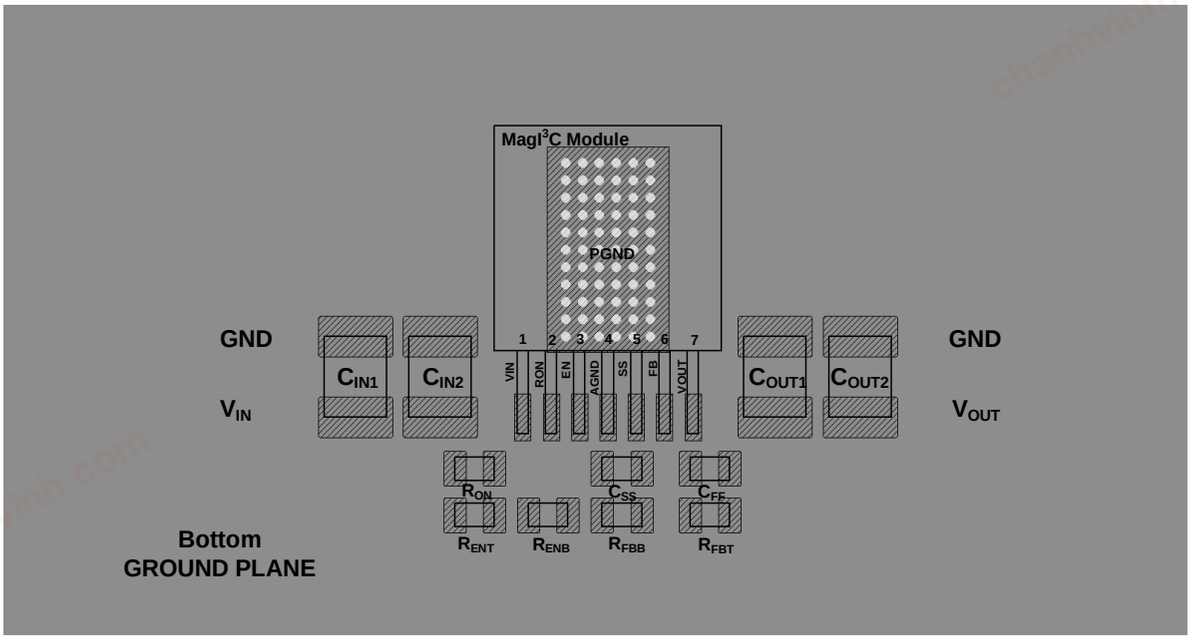
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MagI³C Power Module
VDRM – Variable Step Down Regulator Module



For best result, use a thermal via array as proposed in the picture above with drill of max 250µm, spaced 750µm apart. Ensure enough copper area is used for heat-sinking, to keep the junction temperature below 125°C.

8: Isolate high noise areas



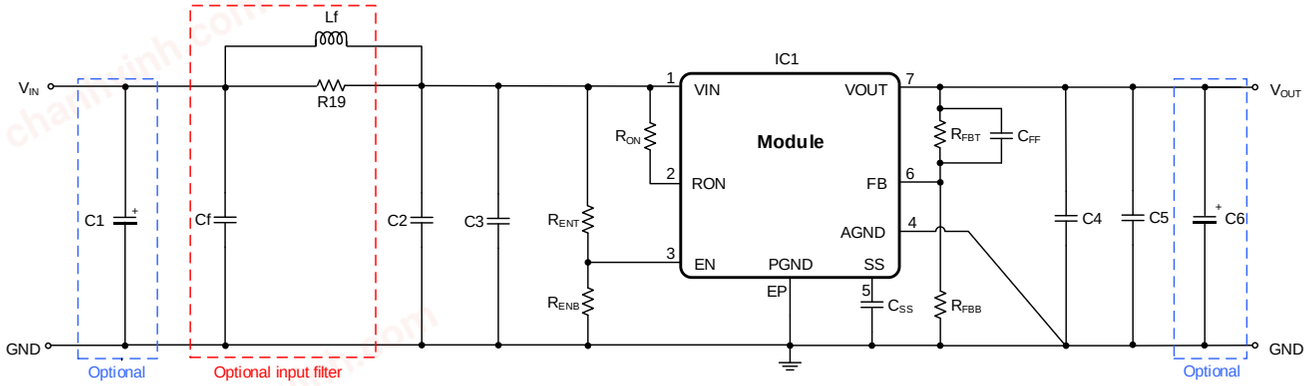
Place a dedicated solid GND copper area beneath the MagI³C Power Module.

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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

EVALUATION BOARD SCHEMATIC (178010601 v3.1)

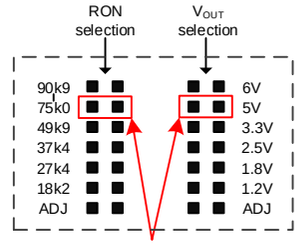
The evaluation board schematic has been developed to be suitable for all input and output voltage conditions, switching frequencies and load currents as well as to achieve optimum load transient response.



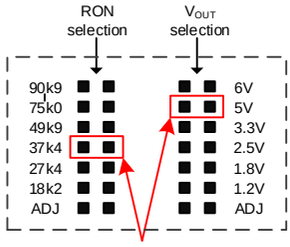
The two multi-layer ceramic capacitors (MLCCs) C2 and C3 at the input handle the switching current ripple and support fast load transients preventing the voltage at the VIN pin from dropping, potentially below the UVLO threshold. Two MLCCs in parallel helps to reduce the ESR. The additional aluminum electrolytic capacitor C1 is only for evaluation board protection purpose. It is mounted as termination of the supply line and provides a slight damping of possible oscillations of the series resonance circuit represented by the inductance of the supply line and the input capacitance.
The additional MLCC Cf is part of the input filter and is mounted on the board. The inductor Lf instead is not mounted and replaced by the zero ohm resistor R19. In case the input filter is placed, R19 must be removed and an appropriate Lf mounted.
The output capacitors should provide a low ESR, in order to reduce the output voltage ripple. The requirement of high capacitance for good transient response performance is fulfilled by mounting an additional aluminum polymer capacitor C6 in parallel to the MLCC output capacitors. The use of two MLCCs in parallel leads to a very low total ESR. Furthermore, the use of more MLCCs in parallel at the input and at the output increases the reliability of the system (in case one capacitor fails, there is still another one remaining).

Operational Requirements

At high duty cycles (V_{IN} very close to V_{OUT}) the input current will be very similar to the output current. Make sure that your supply for the module is capable of delivering high enough currents (check the current limit setting of your power supply). In case your module output voltage V_{OUT} is set to very low values (for example 0.8V) electronic loads might not be able to work correctly. Use discrete high power resistors instead as a load.Use thick and short leads to the input of the module and to the load. High currents result in additional voltage drops across the cables which decrease the voltage at the load. Measure the input and output voltage directly at the ceramic capacitors at the input and output (test points).
In order to have a constant switching frequency of 500kHz, put the jumper of R_{ON} on the same line of the jumper of the selected V_{OUT} (see below).



That corresponds to f_{SW} = 500kHz



That **DOES NOT** correspond to f_{SW} = 500kHz

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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

Bill of Material

Designator	Description		Quantity	Order Code	Manufacturer
IC1	MagI³C Power Module		1	171010601	Würth Elektronik
C1	Aluminum electrolytic capacitor 100µF/50V		1	860010674014	Würth Elektronik
C2,C3	Ceramic chip capacitor 10µF/50V X5R, 1210		2		
C4,C5	Ceramic chip capacitor 47µF/10V X5R, 1210		2		
C6	Aluminum polymer capacitor 220µF/10V		1	875105244013	Würth Elektronik
C_f	Ceramic chip capacitor 1µF/50V, X7R, 1210		1	885012209047	Würth Elektronik
C_{FF}	Ceramic chip capacitor 22nF/50V X7R, 0805		1	885012207094	Würth Elektronik
C_{SS}	Ceramic chip capacitor 4.7nF/50V, COG, 0805		1		
L_f	Not mounted, see recommended value in the "Filter suggestion for conducted EMI" section on the next page				
R_{ENT}, R_{ENB}	Not mounted				
R19	SMD bridge 0Ω resistance		1		
R_{FBT}	10kΩ		1		
R_{FBB}	Set by jumper	1.54 kΩ for V_{OUT} = 6V	1		
		1.87 kΩ for V_{OUT} = 5V	1		
		3.16 kΩ for V_{OUT} = 3.3V	1		
		4.64 kΩ for V_{OUT} = 2.5V	1		
		7.87 kΩ for V_{OUT} = 1.8V	1		
		20 kΩ for V_{OUT} = 1.2V	1		
		Not connected for adjustable V_{OUT}			
R_{ON}	Set by jumper	90.9 kΩ, f_{SW} = 500kHz if R_{FBB} = 1.54kΩ	1		
		75 kΩ, f_{SW} = 500kHz if R_{FBB} = 1.87kΩ	1		
		49.9 kΩ, f_{SW} = 500kHz if R_{FBB} = 3.16kΩ	1		
		37.4 kΩ, f_{SW} = 500kHz if R_{FBB} = 4.64kΩ	1		
		27.4 kΩ, f_{SW} = 500kHz if R_{FBB} = 7.87kΩ	1		
		18.2 kΩ, f_{SW} = 500kHz if R_{FBB} = 20kΩ	1		
		Not connected for adjustable t_{ON}			

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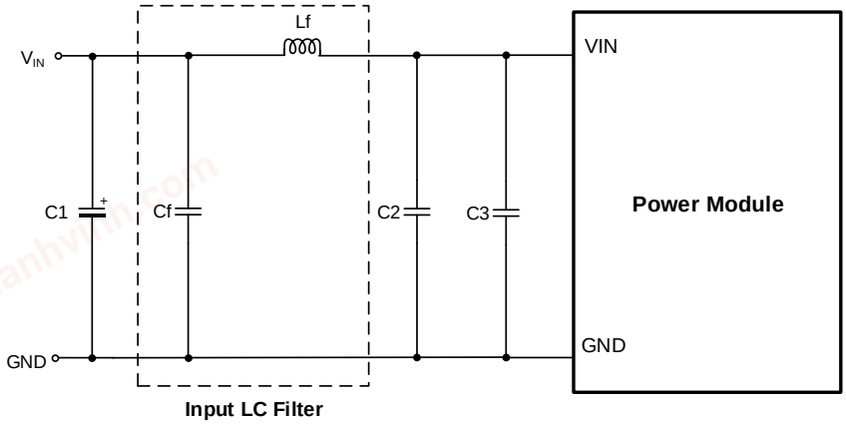
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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

Filter suggestion for conducted EMI

The input filter shown in the schematic below is recommended to achieve conducted compliance according to EN55022 Class B (see results on page 8).
For radiated EMI the input filter is not necessary. It is only used to comply with the setup recommended in the norms.



Input LC Filter

Bill of Material of the Input LC Filter

Designator	Description	Order Code	Manufacturer
C_f	Filter ceramic chip capacitor 1µF/50V, X7R, 1210	885012209047	Würth Elektronik
Lf	Filter inductor, 10µH, TI family	7447462100	Würth Elektronik
	Filter inductor, 10µH, PD2 family (pads located on the bottom layer of the Evaluation Board)	74477410	Würth Elektronik

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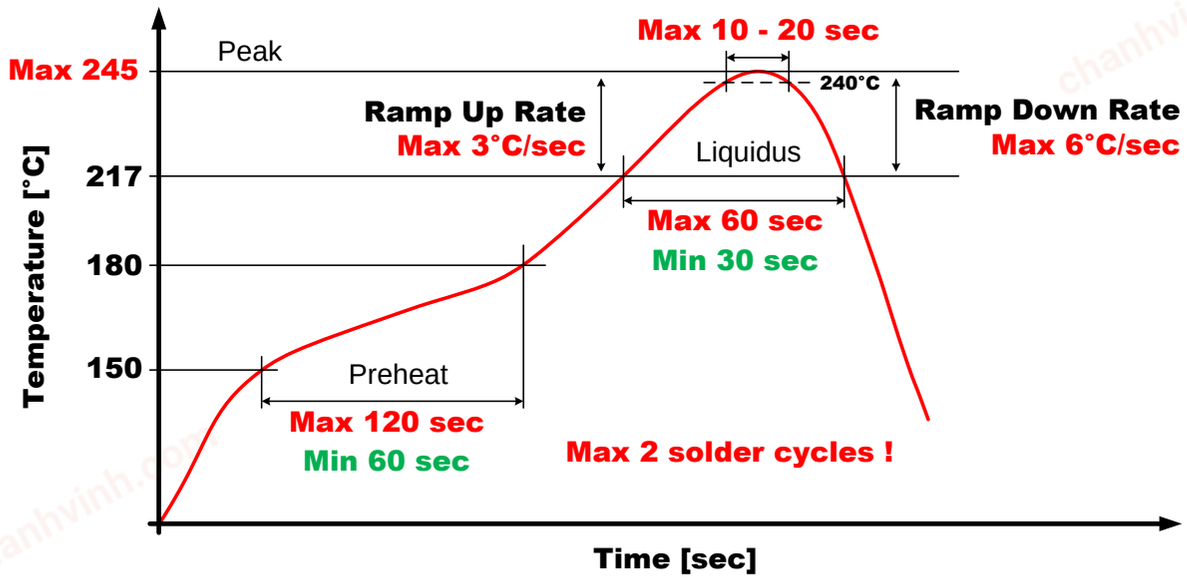
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

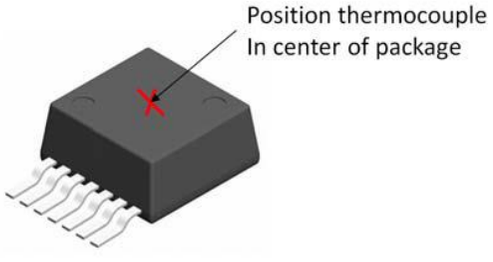
HANDLING RECOMMENDATIONS

1. The power module is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033).
2. The parts are delivered in a sealed bag (Moisture Barrier Bags = MBB) and should be processed within one year.
3. When opening the moisture barrier bag check the Humidity Indicator Card (HIC) for color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card .
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033 recommendation.

SOLDER PROFILE

1. Only Pb-Free assembly is recommended according to JEDEC J-STD020.
2. Measure the peak reflow temperature of the MagI³C power module in the middle of the top view.
3. Ensure that the peak reflow temperature does not exceed 240°C ±5°C as per JEDEC J-STD020.
4. The reflow time period during peak temperature of 240°C ±5°C must not exceed 20 seconds.
5. Reflow time above liquidus (217°C) must not exceed 60 seconds.
6. Maximum ramp up is rate 3°C per second
7. Maximum ramp down rate is 6°C per second
8. Reflow time from room (25°C) to peak must not exceed 8 minutes as per JEDEC J-STD020.
9. **Maximum numbers of reflow cycles is two**.
10. **For minimum risk, solder the module in the last reflow cycle of the PCB production.**
11. For soldering process please consider lead material copper (Cu) and lead finish tin (Sn).
12. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
13. Below profile is valid for convection reflow only
14. Other soldering methods (e.g.vapor phase) are not verified and have to be validated by the customer on his own risk





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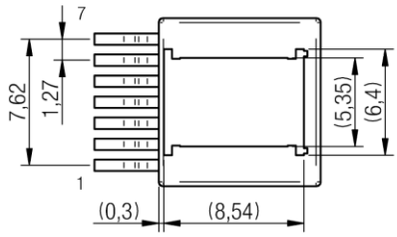
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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

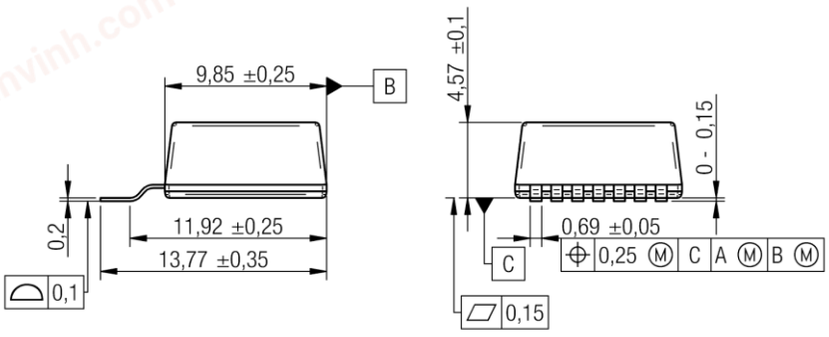
PHYSICAL DIMENSIONS

Package type: TO263-7

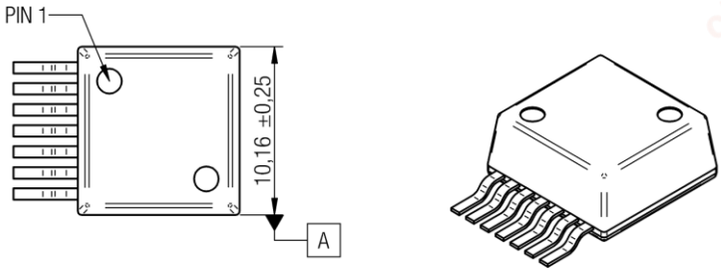
Bottom view

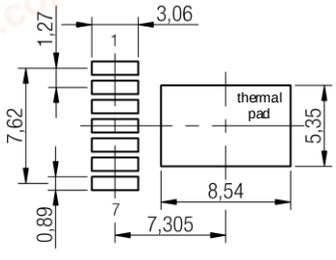


Side view

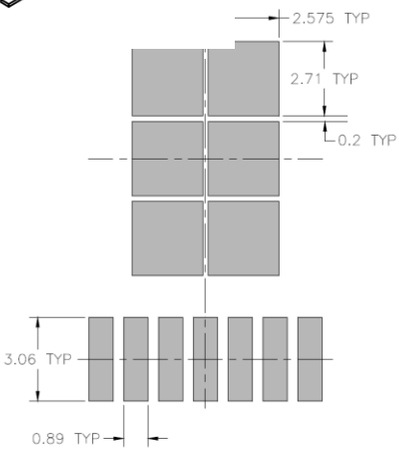


Top view





Recommended soldering pad



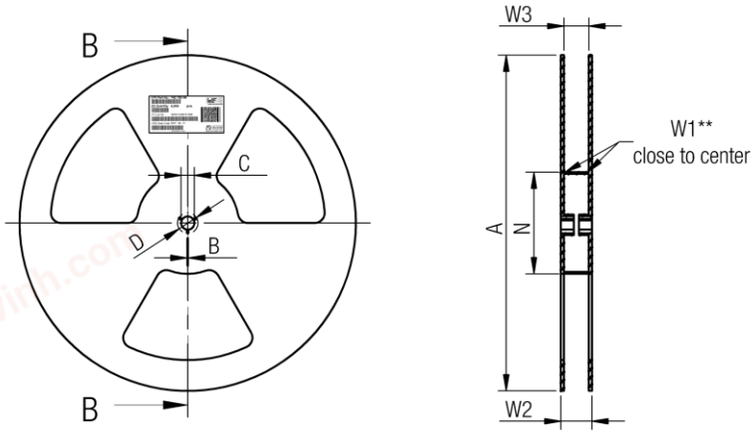
recommended stencil design

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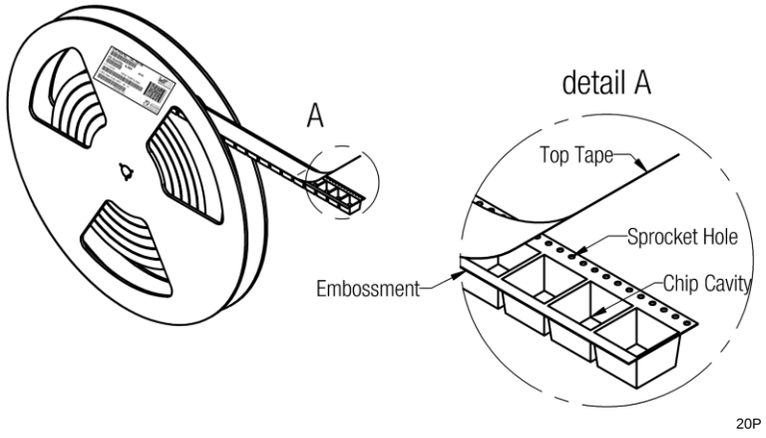
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VDRM – Variable Step Down Regulator Module

PACKAGING
Reel (mm)



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	± 2,0	+ 2	max.	min.	max.
Tape width	**24mm**	330,00	1,50	13,00	20,20	60,00	24,40	30,40	23,90	27,40

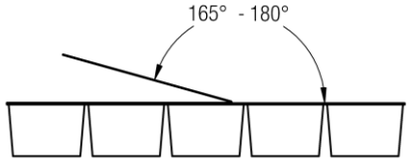


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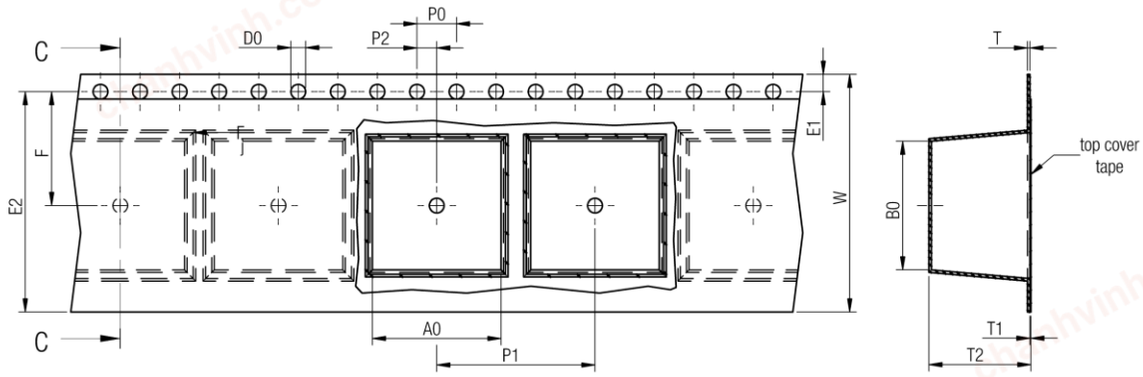
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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

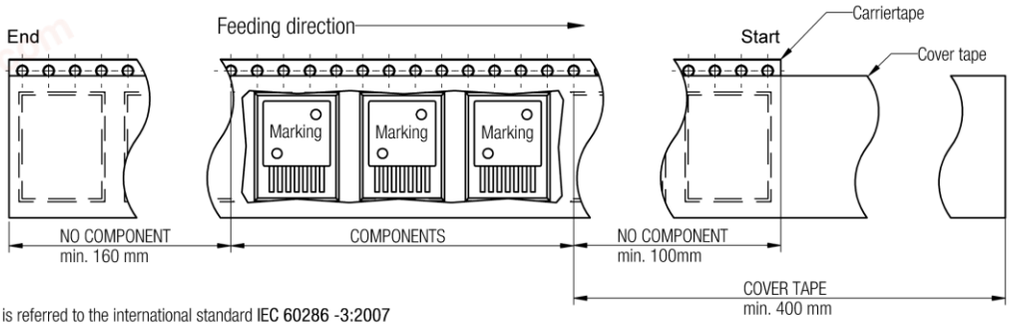
Tape (mm)



		Pull-of force
Tape width	**24 mm**	0,1 N - 1,3 N



		A0	B0	W	P1	T	T1	T2	D0	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		typ.	typ.	+0,3 -0,1	± 0,1	± 0,1	max.	typ.	+0,3 -0,1	± 0,1	min.	± 0,05	± 0,1	± 0,05		
size	TO263-7EP	10,60	14,22	24,00	16,00	0,50	0,10	5,00	1,50	1,75	22,25	11,50	4,00	2,00	Polystyrene	250



Packaging is referred to the international standard IEC 60286 -3:2007

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VDRM – Variable Step Down Regulator Module

DOCUMENT HISTORY

Revision	Date	Description	Comment
1.0	September 2017	Release of the final version	

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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the datasheet have to be complied with.

The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products.

Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product.
Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.

Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications.

Product specific:
Follow all instructions mentioned in the datasheet, especially:
- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

IMPORTANT NOTES

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

3. Best Care and Attention
Any product-specific notes, warnings and cautions must be strictly observed.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.

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