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CAB011M12FM3

1200 V, 11 mΩ All-Silicon Carbide Half-Bridge Module

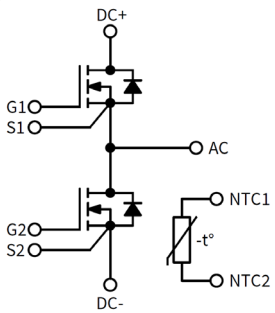
V_{DS}	1200 V
$R_{DS(on)}$	11 mΩ

Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation

Package





Applications

- EV Chargers
- Solar
- High-Efficiency Converters / Inverters
- Motor & Traction Drives
- Smart-Grid / Grid-Tied Distributed Generation

System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Maximum Parameters (Verified by Design)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{DS\ max}$	Drain-Source Voltage			1200	V		
$V_{GS\ max}$	Gate-Source Voltage, Maximum Value	-8		+19		Transient, <100 ns	Fig. 33
$V_{GS\ op}$	Gate-Source Voltage, Recommended Op. Value	-4		+15		Static	
I_D	DC Continuous Drain Current ($T_{VJ} \leq 150\ ^\circ C$)		105		A	$V_{GS} = 15$ V, $T_H = 50\ ^\circ C$, $T_{VJ} \leq 150\ ^\circ C$	Fig. 20
	DC Continuous Drain Current ($T_{VJ} \leq 175\ ^\circ C$)		109			$V_{GS} = 15$ V, $T_H = 50\ ^\circ C$, $T_{VJ} \leq 175\ ^\circ C$	
$I_{SD\ BD}$	DC Source-Drain Current (Body Diode)		55			$V_{GS} = -4$ V, $T_H = 50\ ^\circ C$, $T_{VJ} \leq 175\ ^\circ C$	
$I_{D\ (pulsed)}$	Maximum Pulsed Drain Current			218		t_{Pmax} limited by T_{jmax} $V_{GS} = 15$ V, $T_H = 50\ ^\circ C$	
$T_{VJ\ op}$	Maximum Virtual Junction Temperature under Switching Conditions	-40		150	°C	Operation	
		-40		175	°C	Intermittent with Reduced Life	

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6		V_{DS} = V_{GS}, I_D = 35 mA	
I_{DSS}	Zero Gate Voltage Drain Current		2	50	µA	V_{GS} = 0 V, V_{DS} = 1200 V	
I_{GSS}	Gate-Source Leakage Current		0.02	0.5		V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance (Devices Only)		10.5	14.0	mΩ	V_{GS} = 15 V, I_D = 100 A	Fig. 2 Fig. 3
			16.3			V_{GS} = 15 V, I_D = 100 A, T_{VJ} = 150 °C	
			19.0			V_{GS} = 15 V, I_D = 100 A, T_{VJ} = 175 °C	
g_{fs}	Transconductance		73		S	V_{DS}= 20 V, I_{DS}= 100 A	Fig. 4
			69			V_{DS}= 20 V, I_{DS}= 100 A, T_{VJ} = 150 °C	
E_{On}	Turn-On Switching Energy, T_J = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C		1.28 1.34 1.43		mJ	V_{DS} = 600 V, I_D = 100 A, V_{GS} = -4 V/15 V, $R_{G(OFF)}$ = 1.0 Ω, $R_{G(ON)}$ = 1.0 Ω L= 13.6 µH	Fig. 11 Fig. 13
E_{Off}	Turn-Off Switching Energy, T_J = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C		0.71 0.70 0.71				
$R_{G(int)}$	Internal Gate Resistance		3.2		Ω	T_{VJ} = 25 °C, f = 100 kHz, V_{AC} = 25 mV	
C_{iss}	Input Capacitance		10.3		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
C_{oss}	Output Capacitance		0.39				
C_{rss}	Reverse Transfer Capacitance		30		pF		
Q_{GS}	Gate to Source Charge		98		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 100 A Per IEC60747-8-4 pg 21	
Q_{GD}	Gate to Drain Charge		100				
Q_G	Total Gate Charge		324				
$R_{th\ JH}$	FET Thermal Resistance, Junction to Heatsink		0.553		°C/W		Fig. 17

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Diode Characteristics (Per Position) (T_{VJ} = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Body Diode Forward Voltage		5.1		V	V_{GS} = -4 V, I_{SD} = 100 A	Fig. 7
			4.7			V_{GS} = -4 V, I_{SD} = 100 A, T_{VJ} = 150 °C	
t_{rr}	Reverse Recovery Time		20.5		ns	V_{GS} = -4 V, I_{SD} = 100 A, V_R = 600 V di/dt = 13.5 A/ns, $R_{G(ON)}$ = 1.0 Ω, T_J = 150 °C	Fig. 32
Q_{RR}	Reverse Recovery Charge		1.85		µC		
I_{RRM}	Peak Reverse Recovery Current		144		A		
E_{RR}	Reverse Recovery Energy T_J = 25 °C T_J = 125 °C T_J = 150 °C		0.16 0.48 0.64		mJ	V_{DS} = 600 V, I_D = 100 A, V_{GS} = -4 V/15 V, $R_{G(ON)}$ = 1.0 Ω, L= 13.6 µH	Fig. 14

Module Physical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R_{HS}	Package Resistance, M1 (High-Side)		1.98		mΩ	T_C = 25 °C, I_D = 100 A, Note 1
			2.23			T_C = 125 °C, I_D = 100 A, Note 1
R_{LS}	Package Resistance, M2 (Low-Side)		1.85			T_C = 25 °C, I_D = 100 A, Note 1
			2.06			T_C = 125 °C, I_D = 100 A, Note 1
L_{Stray}	Stray Inductance		11.4		nH	Between Terminals DC+ and DC-
T_C	Case Temperature	-40		125	°C	
W	Weight		21		g	
M_S	Mounting Torque		2.0	2.3	N-m	M4 bolts
V_{isol}	Case Isolation Voltage		3		kV	AC, 50 Hz, 1 min
CTI	Comparative Tracking Index	200				
	Clearance Distance		5.0		mm	Terminal to Terminal
			10.0			Terminal to Heatsink
	Creepage Distance		6.3			Terminal to Terminal
			11.5			Terminal to Heatsink

Note 1. Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance.

NTC Thermistor Characterization

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
R_{NTC}	Rated Resistance		5.0		kΩ	T_{NTC} = 25 °C	Fig. 23
ΔR/R	Resistance Tolerance at 25°C	-5		5	%		
$\beta_{25/50}$	Beta Value (T_2 = 50°C)		3380		K		
$\beta_{25/80}$	Beta Value (T_2 = 80°C)		3468		K		
$\beta_{25/100}$	Beta Value (T_2 = 100°C)		3523		K		
P_{Max}	Power Dissipation			10	mW	T_{NTC} = 25 °C	

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Typical Performance

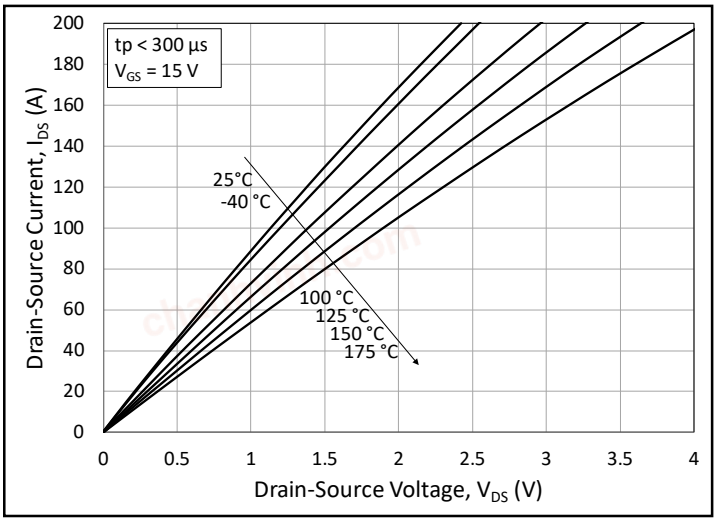


Figure 1. Output Characteristics for Various Junction Temperatures

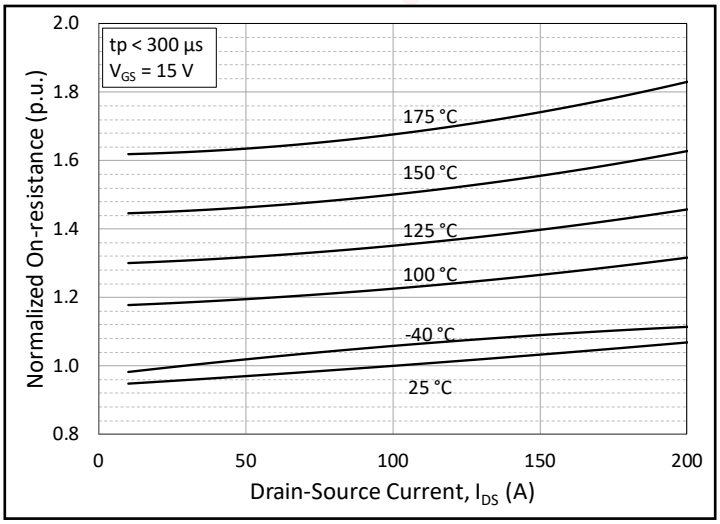


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

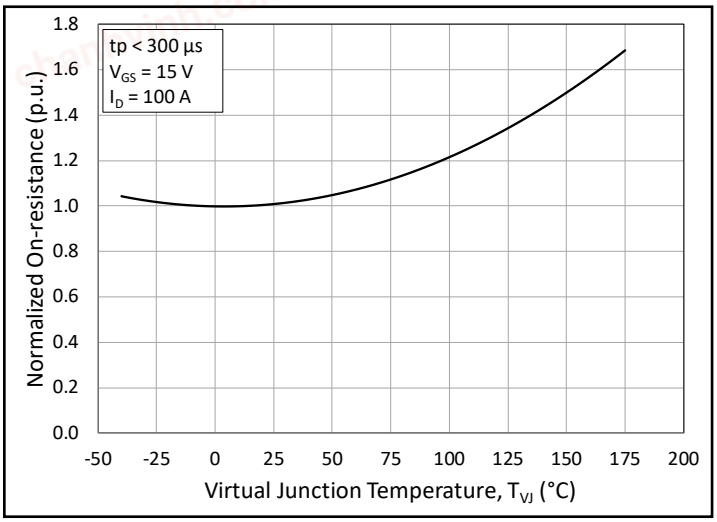


Figure 3. Normalized On-State Resistance vs. Junction Temperature

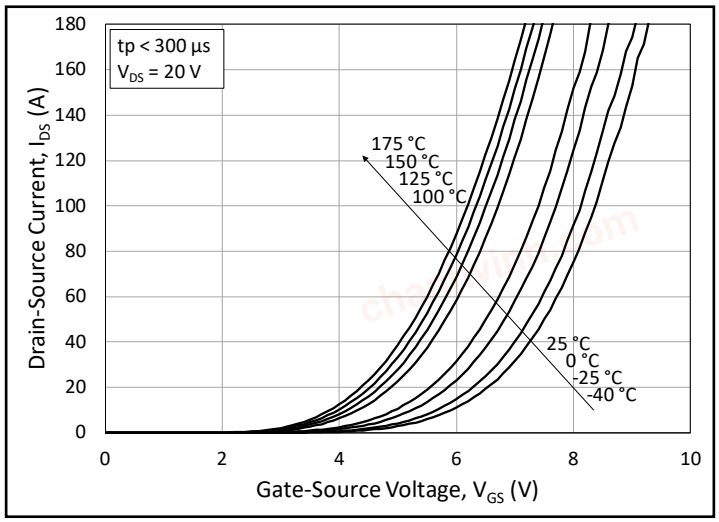


Figure 4. Transfer Characteristic for Various Junction Temperatures

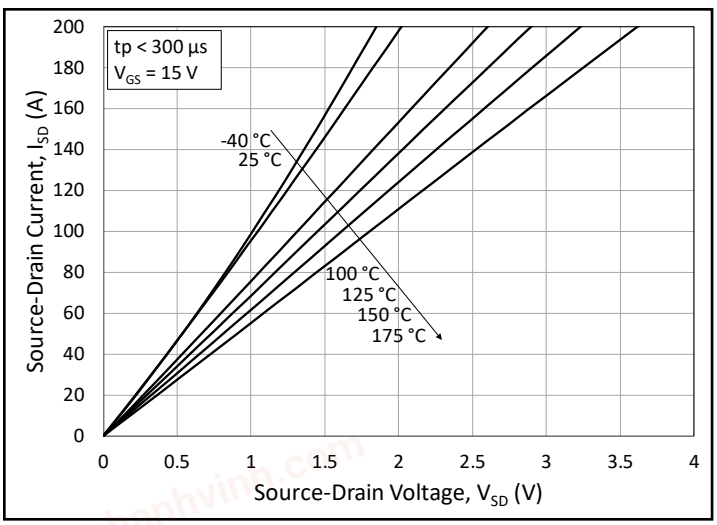


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

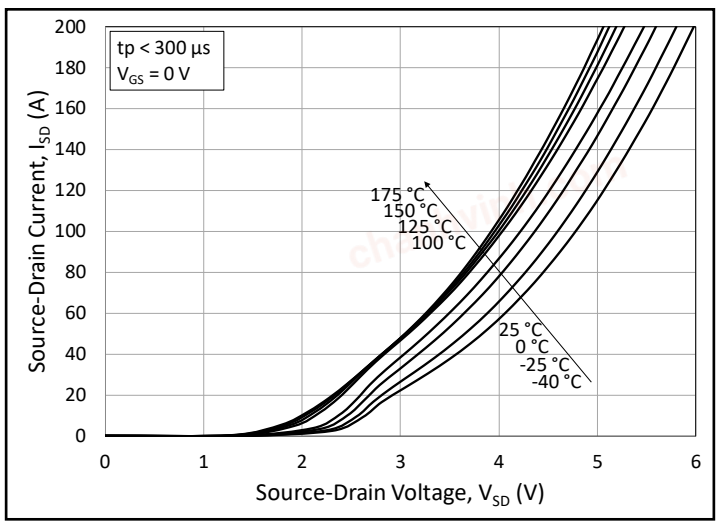


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

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Typical Performance

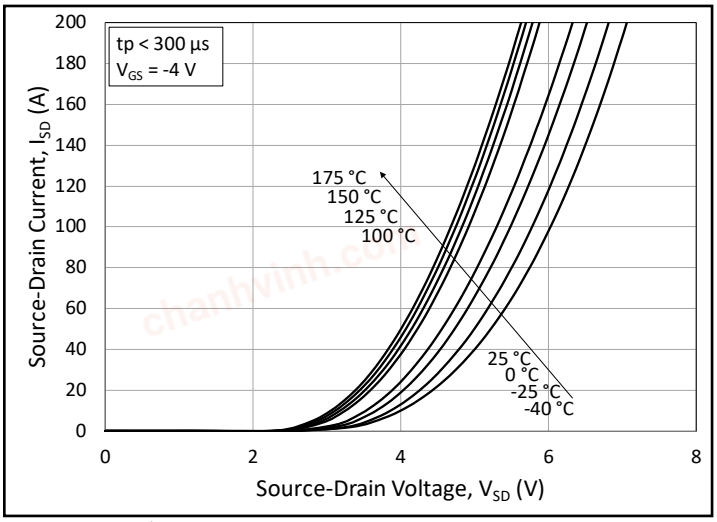


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Body Diode)

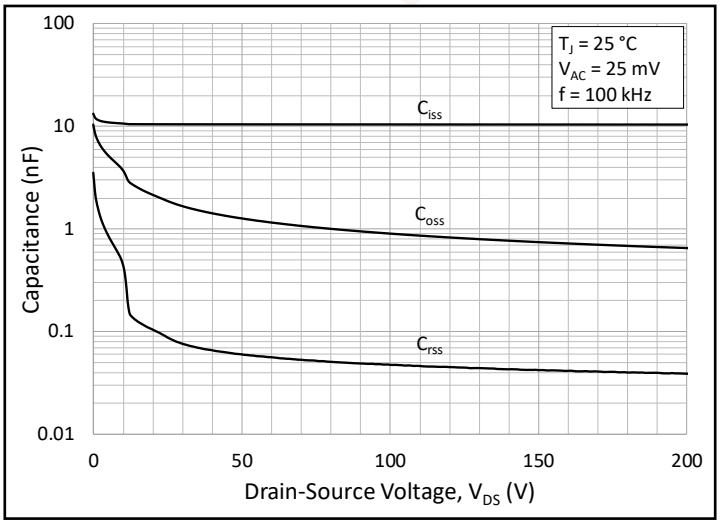


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

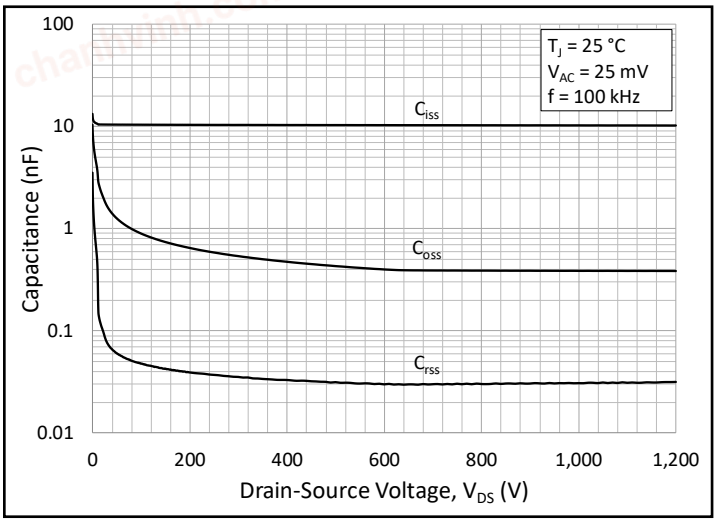


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

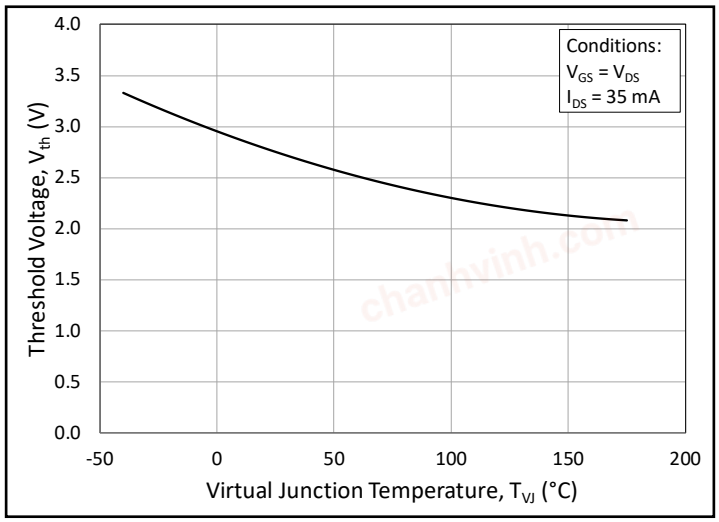


Figure 10. Threshold Voltage vs. Junction Temperature

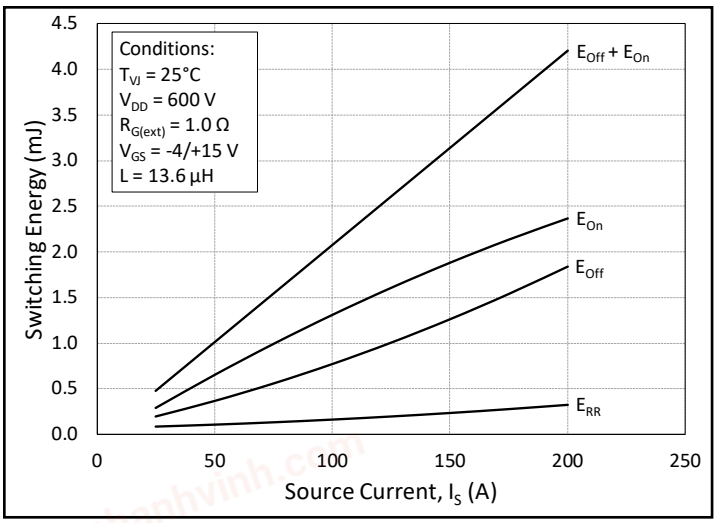


Figure 11. Switching Energy vs. Drain Current (V_{DS} = 600 V)

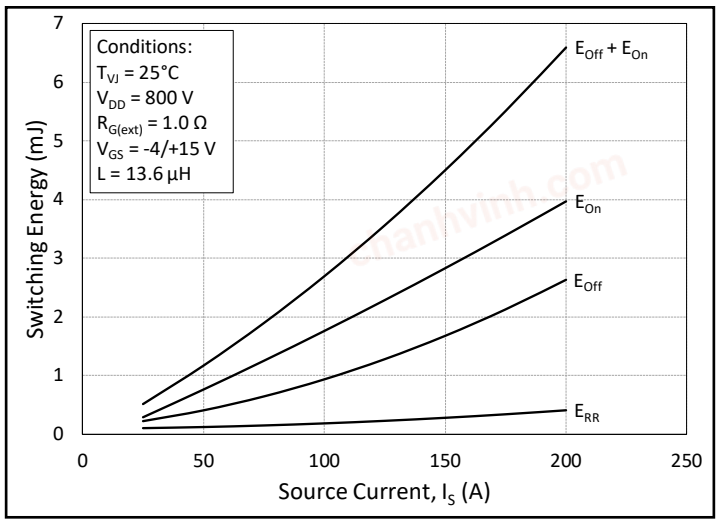


Figure 12. Switching Energy vs. Drain Current (V_{DS} = 800 V)

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Typical Performance

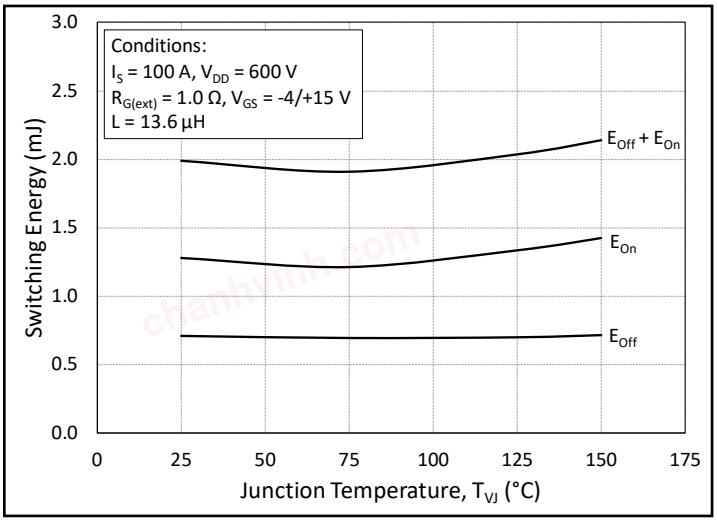


Figure 13. MOSFET Switching Energy vs. Junction Temperature

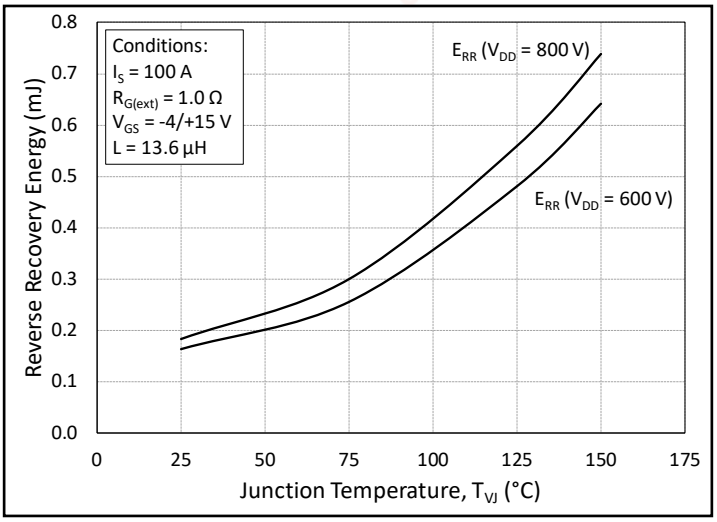


Figure 14. Reverse Recovery Energy vs. Junction Temperature

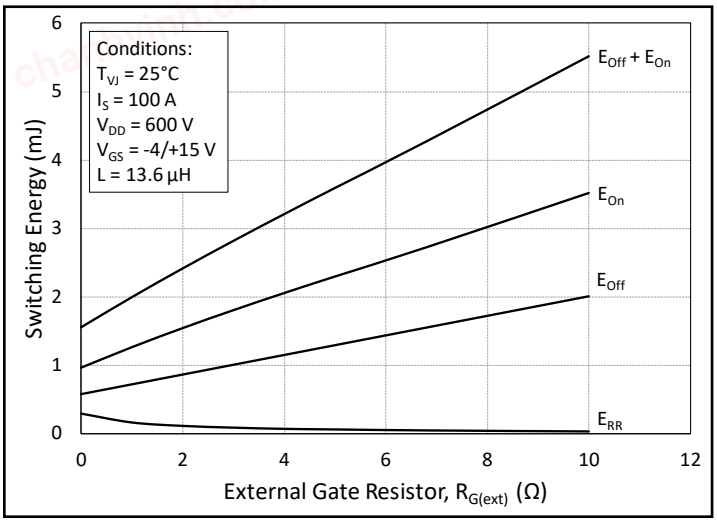


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

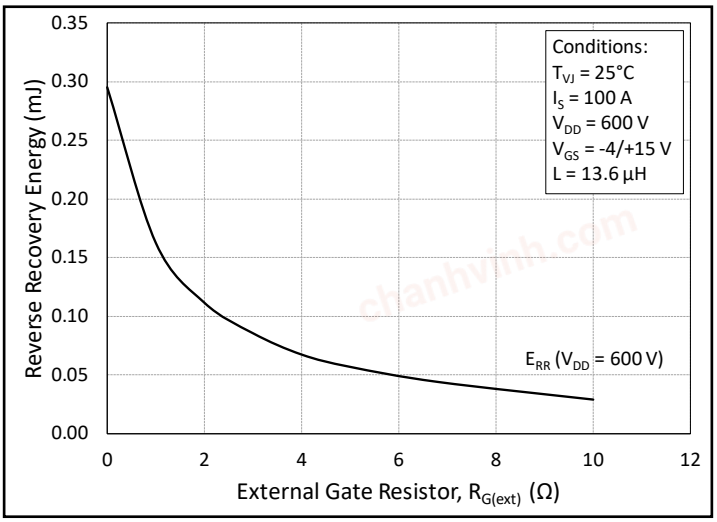


Figure 16. Reserve Recovery Energy vs. External Gate Resistance

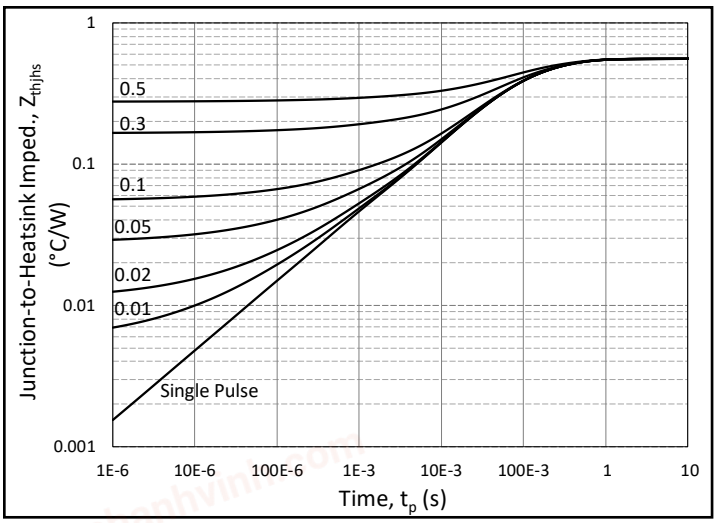


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\,JC}$ (°C/W)

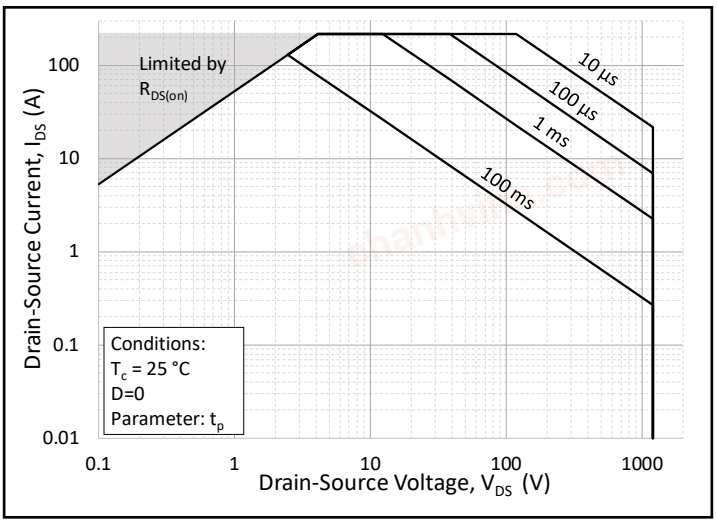


Figure 18. Forward Bias Safe Operating Area (FBSOA)

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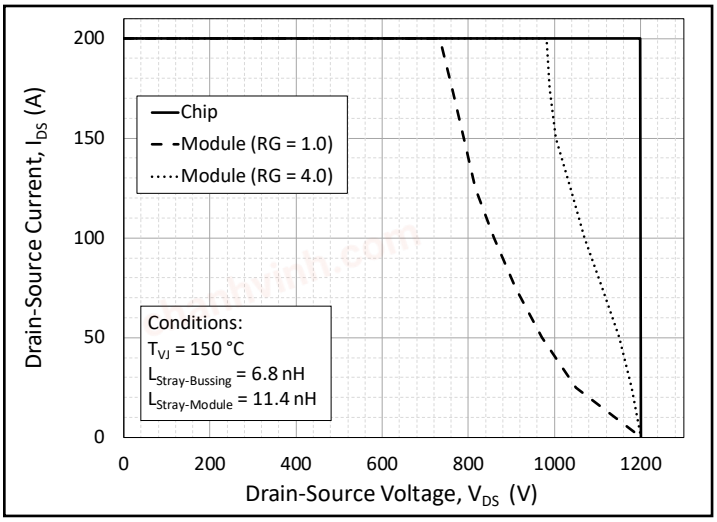


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

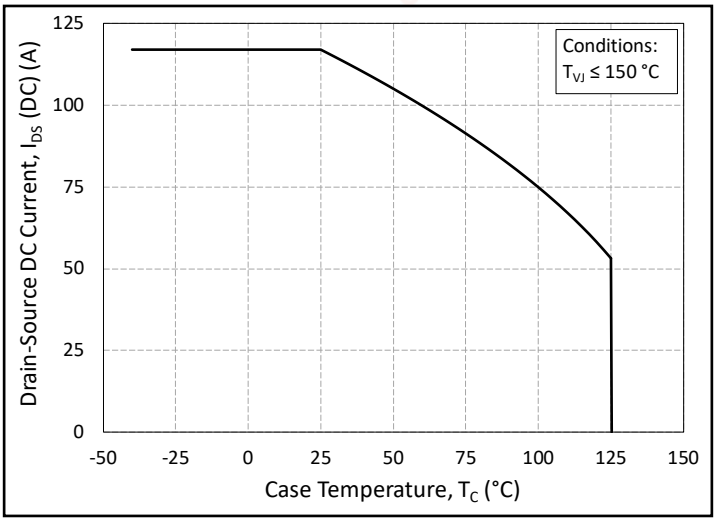


Figure 20. Continuous Drain Current Derating vs. Case Temperature

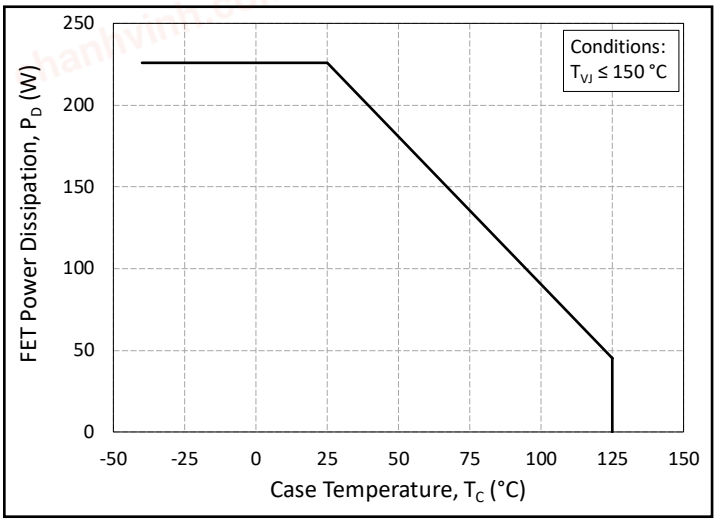


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

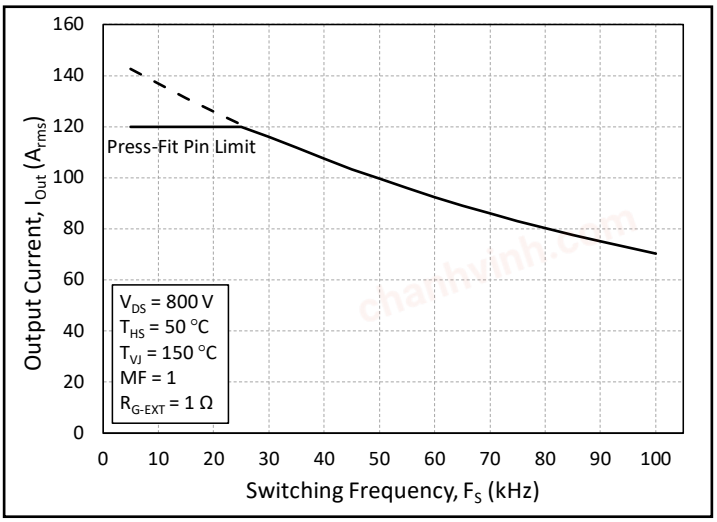


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

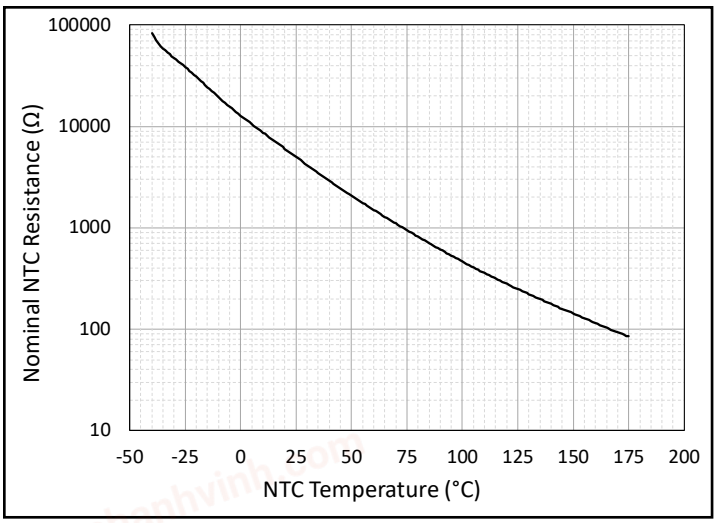


Figure 23. Nominal NTC Resistance vs. NTC Temperature

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Timing Characteristics

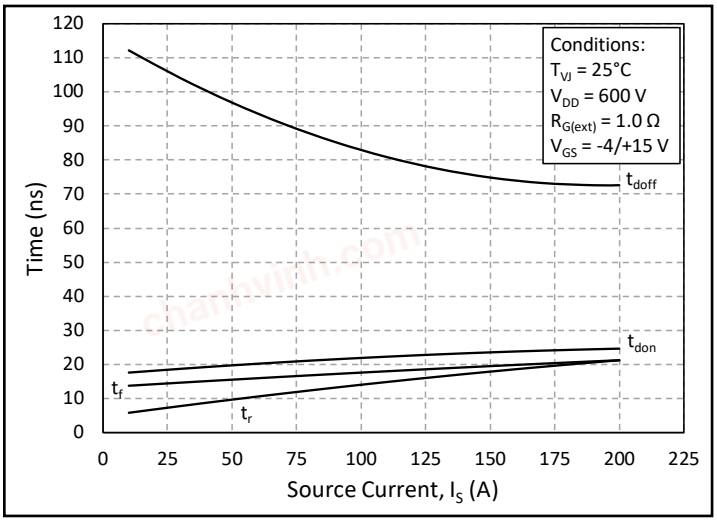


Figure 24. Timing vs. Source Current

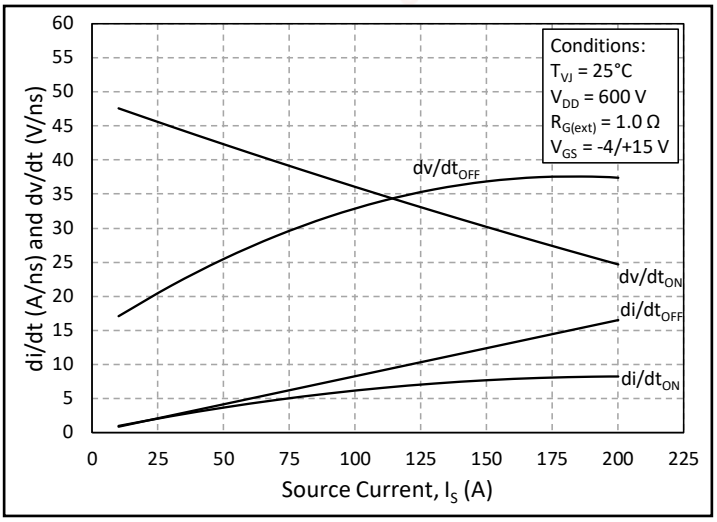


Figure 25. dv/dt and di/dt vs. Source Current

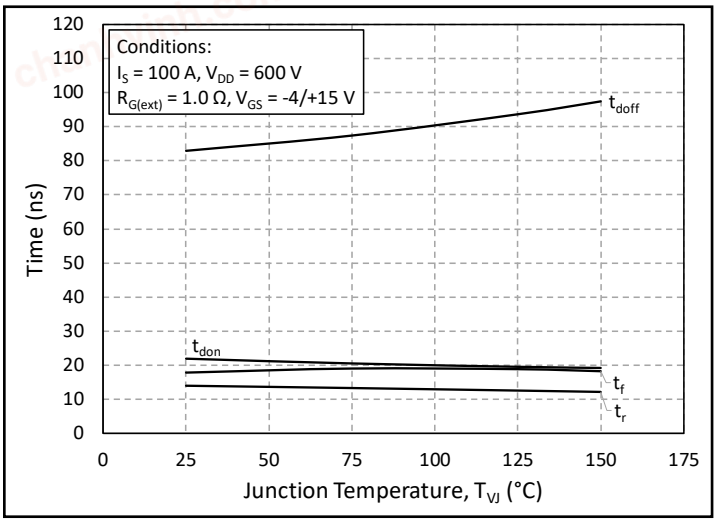


Figure 26. Timing vs. Junction Temperature

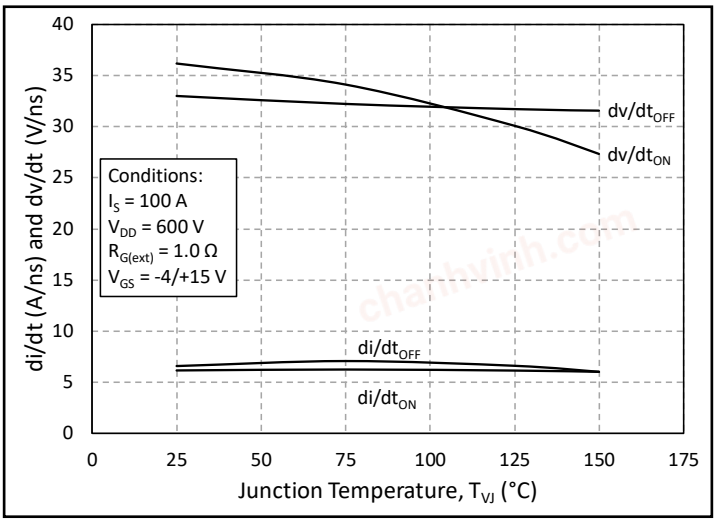


Figure 27. dv/dt and di/dt vs. Junction Temperature

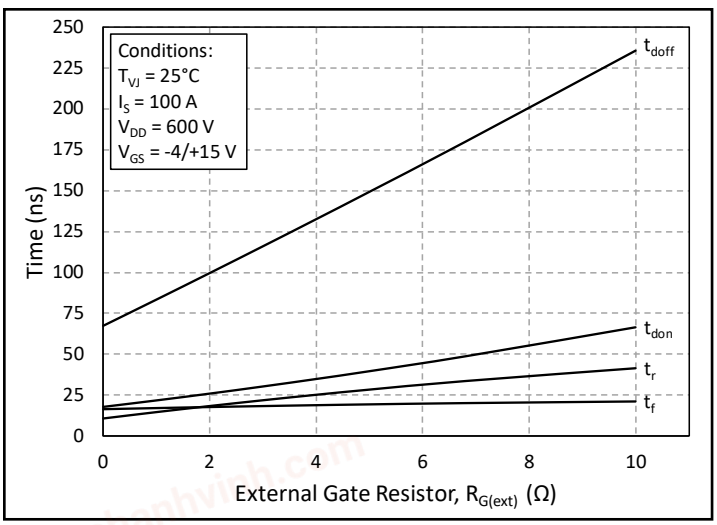


Figure 28. Timing vs. External Gate Resistance

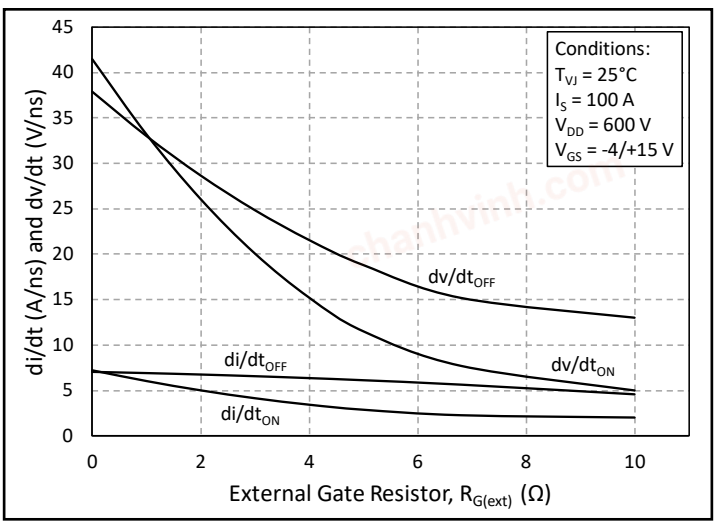


Figure 29. dv/dt and di/dt vs. External Gate Resistance

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Definitions

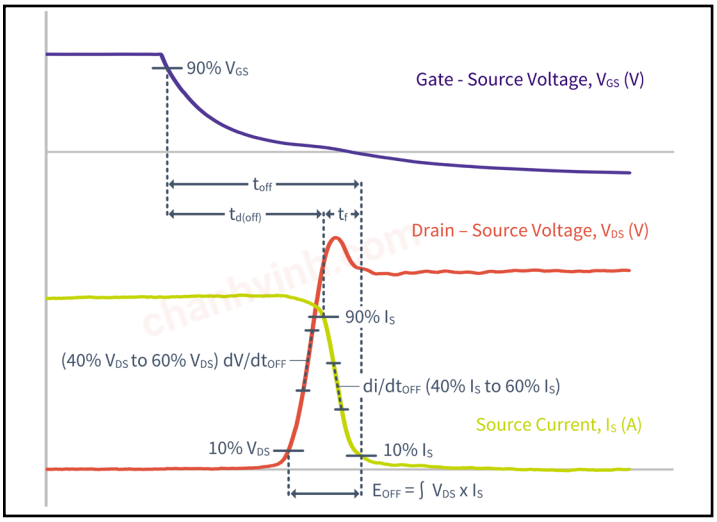


Figure 30. Turn-off Transient Definitions

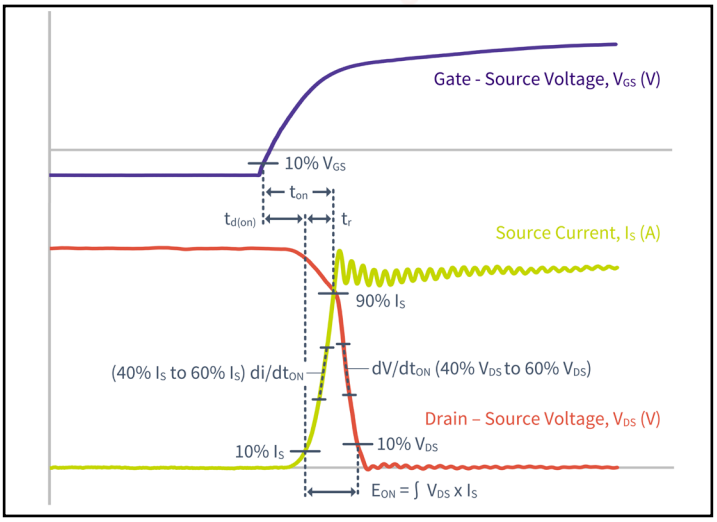


Figure 31. Turn-on Transient Definitions

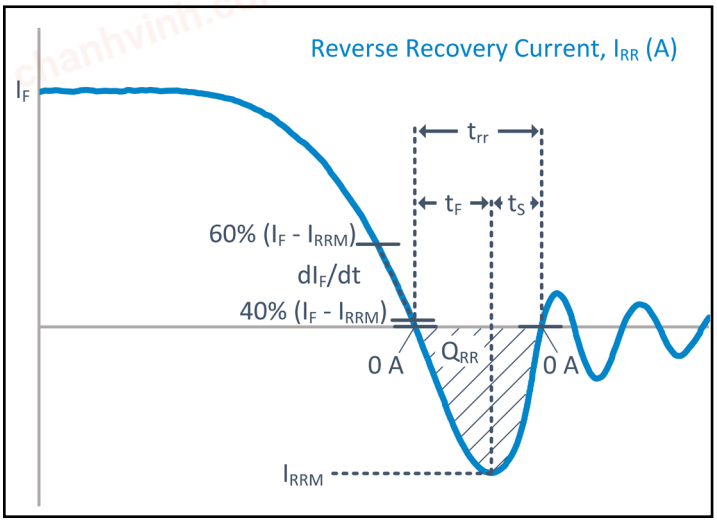


Figure 32. Reverse Recovery Definitions

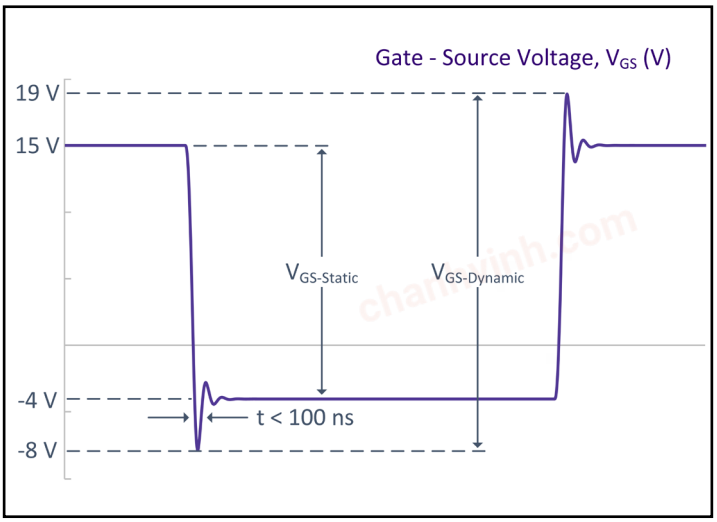
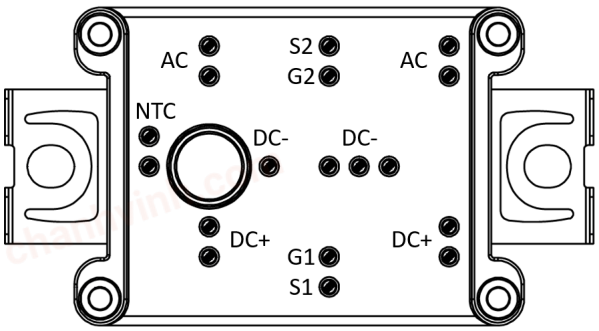


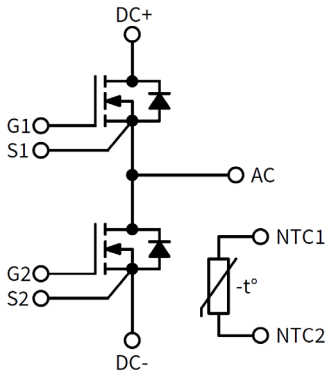
Figure 33. V_{GS} Transient Definitions

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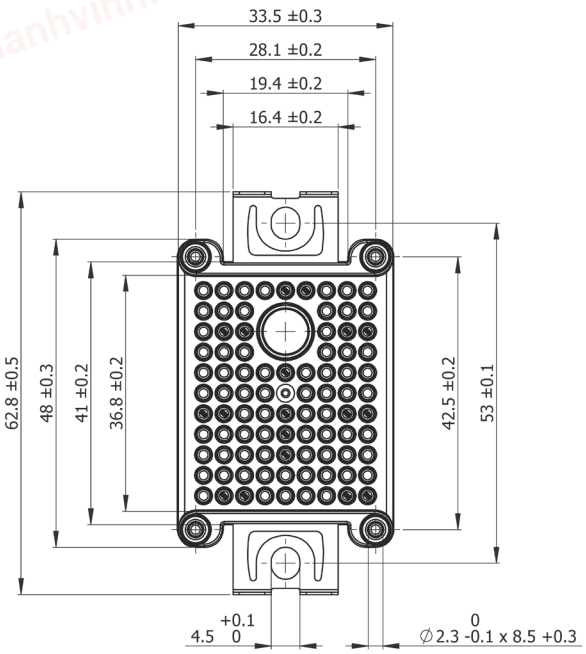
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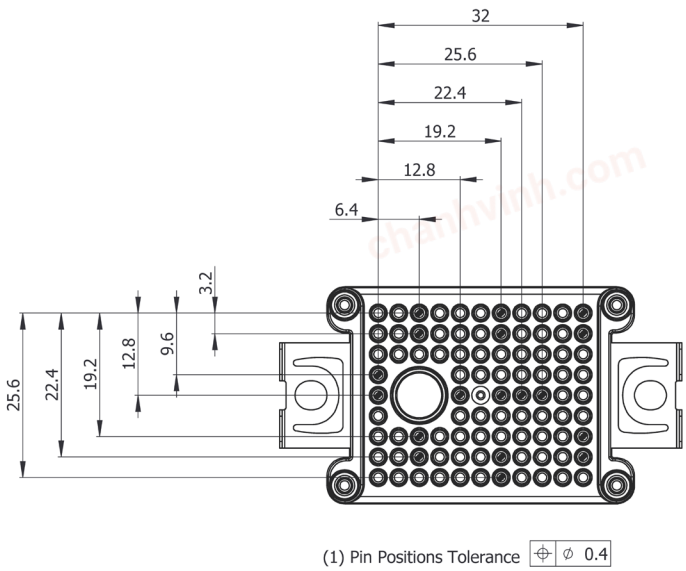
Schematic and Pin Out

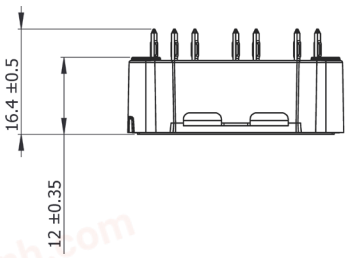


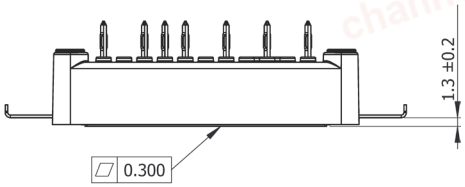


Package Dimension (mm)









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Supporting Documents & Tools

Evaluation Tools

- KIT-CRD-CIL12N-FMA: Dynamic Evaluation Board for Half-Bridge FM3 Modules
- KIT-CRD-CIL12N-FMC: Dynamic Evaluation Board for Six-Pack FM3 Modules
- CRD25AD12N-FMC: 25 kW SiC Active Front End (AFE)
- CAB011M12FM3 PLECS Model
- SpeedFit 2.0 Design Simulator™

Dual-Channel Companion Gate Driver Boards

- EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board
- Si823H-AxWA-KIT: Silicon Labs® Gate Driver Board
- CGD1700HB2M-UNA: Wolfspeed Gate Driver Board
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- CPWR-AN41: Mounting Instructions and PCB Requirements
- CPWR-AN42: Thermal Interface Material Application Note
- CPWR-AN45: Dynamic Performance Application Note

Notes

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

- The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.

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