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W971GG6NB

winbond

8M × 8 BANKS × 16 BIT DDR2 SDRAM

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1. GENERAL DESCRIPTION

The W971GG6NB is a 1G bits DDR2 SDRAM, organized as 8,388,608 words × 8 banks × 16 bits. This device achieves high speed transfer rates up to 1066 Mbps (DDR2-1066) for various applications. W971GG6NB is sorted into the following grade parts: -18, 18I, 18J, -25, 25I, 25J and -3.

The -18, 18I and 18J grade parts are compliant to the DDR2-1066 (6-6-6) specification (The 18I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 18J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The -25, 25I and 25J grade parts are compliant to the DDR2-800 (5-5-5) or DDR2-800 (6-6-6) specification (The 25I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 25J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The -3 grade parts is compliant to the DDR2-667 (5-5-5) specification.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CLK rising and $\overline{CLK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS- $\overline{DQS}$ pair in a source synchronous fashion.

2. FEATURES

- Power Supply: V_{DD}, V_{DDQ} = 1.8 V ± 0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3, 4, 5, 6 and 7
- Burst Length: 4 and 8
- Bi-directional, differential data strobes (DQS and $\overline{DQS}$) are transmitted / received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and $\overline{CLK}$)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Posted $\overline{CAS}$ programmable additive latency supported to make command and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-precharge operation for read and write bursts
- Auto Refresh and Self Refresh modes
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18
- Packaged in VFBGA 84 Ball (8x12.5 mm^2 with thickness of 1.0 mm) - (Window BGA Type), using Lead free materials with RoHS compliant

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3. ORDER INFORMATION

PART NUMBER	SPEED GRADE	OPERATING TEMPERATURE
W971GG6NB-18	DDR2-1066 (6-6-6)	0°C ≤ TCASE ≤ 85°C
W971GG6NB18I	DDR2-1066 (6-6-6)	-40°C ≤ TCASE ≤ 95°C
W971GG6NB18J	DDR2-1066 (6-6-6)	-40°C ≤ TCASE ≤ 105°C
W971GG6NB-25	DDR2-800 (5-5-5) or DDR2-800 (6-6-6)	0°C ≤ TCASE ≤ 85°C
W971GG6NB25I	DDR2-800 (5-5-5) or DDR2-800 (6-6-6)	-40°C ≤ TCASE ≤ 95°C
W971GG6NB25J	DDR2-800 (5-5-5) or DDR2-800 (6-6-6)	-40°C ≤ TCASE ≤ 105°C
W971GG6NB-3	DDR2-667 (5-5-5)	0°C ≤ TCASE ≤ 85°C

4. KEY PARAMETERS

SYM.	SPEED GRADE				DDR2-1066	DDR2-800	DDR2-667
	Bin(CL-tRCD-tRP)				6-6-6	5-5-5/6-6-6	5-5-5
	Part Number Extension				-18/18I/18J	-25/25I/25J	-3
tCK(avg)	Average clock period		@CL = 7	Min.	1.875 nS	–	–
				Max.	7.5 nS	–	–
			@CL = 6	Min.	1.875 nS	2.5 nS	–
				Max.	7.5 nS	8 nS	–
			@CL = 5	Min.	2.5 nS	2.5 nS	3 nS
				Max.	7.5 nS	8 nS	8 nS
			@CL = 4	Min.	3 nS	3.75 nS	3.75 nS
				Max.	7.5 nS	8 nS	8 nS
			@CL = 3	Min.	–	5 nS	5 nS
				Max.	–	8 nS	8 nS
tRCD	Active to Read/Write Command Delay Time			Min.	11.25 nS	12.5 nS	15 nS
tREFI	Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C		Max.	7.8 µS*2, 3	7.8 µS*2, 3	–*2
		0°C ≤ TCASE ≤ 85°C		Max.	7.8 µS*1	7.8 µS*1	7.8 µS*1
		85°C < TCASE ≤ 95°C		Max.	3.9 µS*4	3.9 µS*4	3.9 µS*4
		95°C < TCASE ≤ 105°C		Max.	3.9 µS*4	3.9 µS*4	3.9 µS*4
tRP	Precharge to Active Command Period			Min.	11.25 nS	12.5 nS	15 nS
tRC	Active to Ref/Active Command Period			Min.	51.25 nS	52.5 nS	55 nS
tRAS	Active to Precharge Command Period			Min.	40 nS	40 nS	40 nS
IDD0	Operating one bank active-precharge current			Max.	60 mA	55 mA	50 mA
IDD1	Operating one bank active-read-precharge current			Max.	70 mA	65 mA	60 mA
IDD4R	Operating burst read current			Max.	110 mA	105 mA	100 mA
IDD4W	Operating burst write current			Max.	120 mA	110 mA	100 mA
IDD5B	Burst refresh current			Max.	85 mA	80 mA	75 mA
IDD6	Self refresh current (TCASE ≤ 85°C)			Max.	8 mA	8 mA	8 mA
IDD7	Operating bank interleave read current			Max.	150 mA	140 mA	130 mA

Notes:

1. All speed grades support 0°C ≤ TCASE ≤ 85°C with full JEDEC AC and DC specifications.
2. For -18, -25 and -3 speed grades, -40°C ≤ TCASE < 0°C is not available.
3. 18I and 25I speed grades support -40°C ≤ TCASE ≤ 85°C with full JEDEC AC and DC specifications.
4. For -18, 18I, -25, 25I and -3 speed grades, TCASE is able to extend to 95°C. For 18J and 25J speed grades, TCASE is able to extend to 105°C. They are with doubling Auto Refresh commands in frequency to a 32 mS period (tREFI = 3.9 µS) and to enter to Self Refresh mode at this high temperature range via A7 “1” on EMR (2).

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5. BALL CONFIGURATION

1	2	3	4	5	6	7	8	9
VDD	NC	VSS		A		VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM		B		UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ		C		VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11		D		DQ10	VSSQ	DQ13
VDD	NC	VSS		E		VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM		F		LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ		G		VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3		H		DQ2	VSSQ	DQ5
VDDL	VREF	VSS		J		VSSDL	CLK	VDD
	CKE	$\overline{\text{WE}}$		K		$\overline{\text{RAS}}$	$\overline{\text{CLK}}$	ODT
BA2	BA0	BA1		L		$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1		M		A2	A0	VDD
VSS	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	VSS
VDD	A12	NC		R		NC	NC	

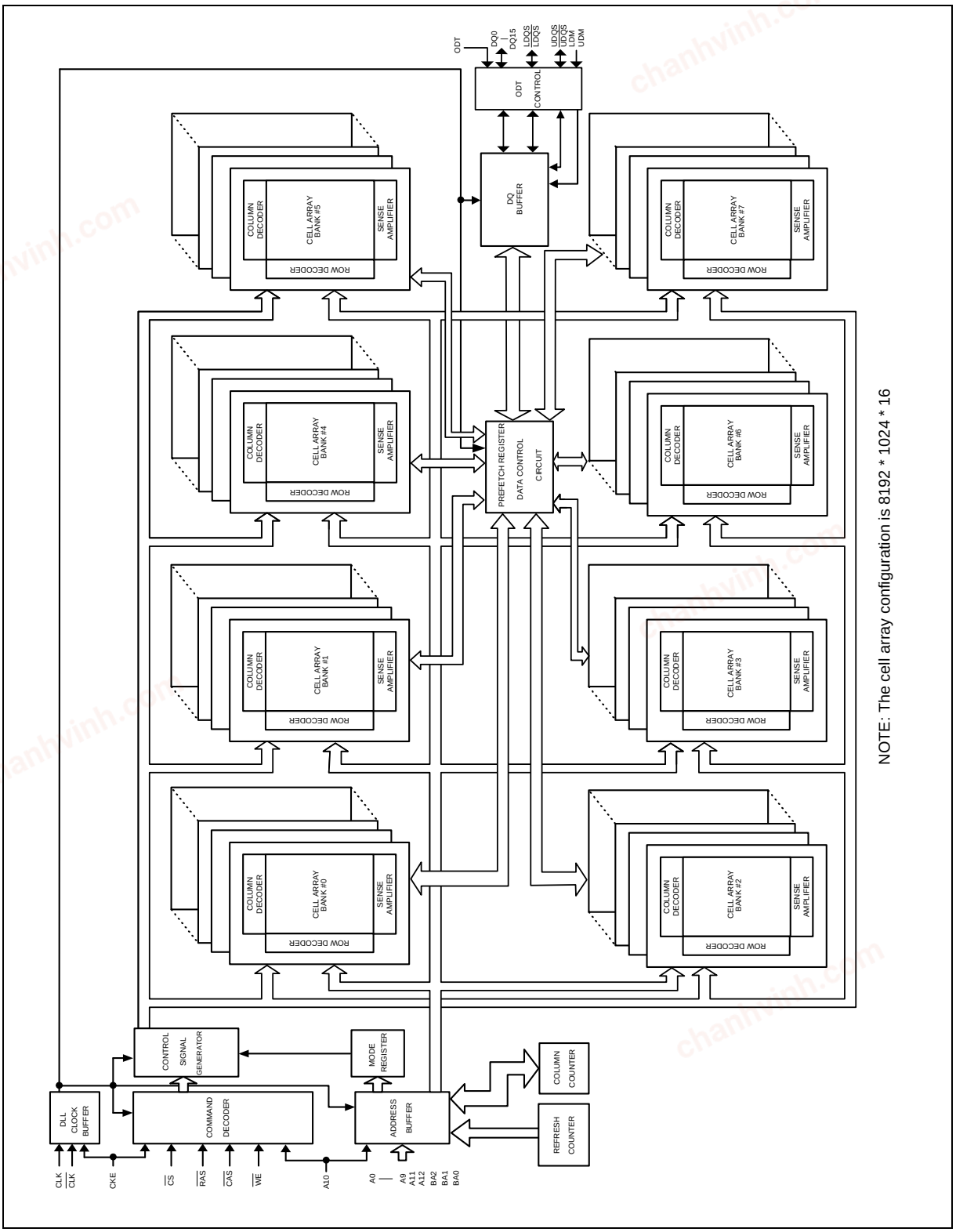
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6. BALL DESCRIPTION

BALL NUMBER	SYMBOL	FUNCTION	DESCRIPTION
M8,M3,M7,N2,N8,N3,N7,P2,P8,P3,M2,P7,R2	A0−A12	Address	Provide the row address for active commands, and the column address and Auto-precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. Row address: A0−A12. Column address: A0−A9. (A10 is used for Auto-precharge)
L2,L3,L1	BA0−BA2	Bank Select	BA0−BA2 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
G8,G2,H7,H3,H1,H9,F1,F9,C8,C2,D7,D3,D1,D9,B1,B9	DQ0−DQ15	Data Input / Output	Bi-directional data bus.
K9	ODT	On Die Termination Control	ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM.
F7,E8	LDQS, $\overline{\text{LDQS}}$	LOW Data Strobe	Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS corresponds to the data on DQ0−DQ7. $\overline{\text{LDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
B7,A8	UDQS, $\overline{\text{UDQS}}$	UP Data Strobe	Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS corresponds to the data on DQ8−DQ15. $\overline{\text{UDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
L8	$\overline{\text{CS}}$	Chip Select	All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external rank selection on systems with multiple ranks. $\overline{\text{CS}}$ is considered part of the command code.
K7,L7,K3	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Command Inputs	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
B3,F3	UDM, LDM	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
J8,K8	CLK, $\overline{\text{CLK}}$	Differential Clock Inputs	CLK and $\overline{\text{CLK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{\text{CLK}}$. Output (read) data is referenced to the crossings of CLK and $\overline{\text{CLK}}$ (both directions of crossing).
K2	CKE	Clock Enable	CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
J2	V_{REF}	Reference Voltage	V_{REF} is reference voltage for inputs.
A1,E1,J9,M9,R1	V_{DD}	Power Supply	Power Supply: 1.8V ± 0.1V.
A3,E3,J3,N1,P9	V_{SS}	Ground	Ground.
A9,C1,C3,C7,C9,E9,G1,G3,G7,G9	V_{DDQ}	DQ Power Supply	DQ Power Supply: 1.8V ± 0.1V.
A7,B2,B8,D2,D8,E7,F2,F8,H2,H8	V_{SSQ}	DQ Ground	DQ Ground. Isolated on the device for improved noise immunity.
A2,E2,R3,R7,R8	NC	No Connection	No connection.
J7	V_{SSDL}	DLL Ground	DLL Ground.
J1	V_{DDL}	DLL Power Supply	DLL Power Supply: 1.8V ± 0.1V.

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7. BLOCK DIAGRAM



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8. FUNCTIONAL DESCRIPTION

8.1 Power-up and Initialization Sequence

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following sequence is required for Power-up and Initialization.

1. Apply power and attempt to maintain CKE below 0.2 × V_{DDQ} and ODT[*1] at a LOW state (all other inputs may be undefined.) Either one of the following sequence is required for Power-up.
   A. The V_{DD} voltage ramp time must be no greater than 200 mS from when V_{DD} ramps from 300 mV to V_{DD} min; and during the V_{DD} voltage ramp, $|V_{DD} - V_{DDQ}| \leq 0.3$ volts.
      - V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output
      - V_{TT} is limited to 0.95V max
      - V_{REF}[*2] tracks $V_{DDQ}/2$
      - $V_{DDQ} \geq V_{REF}$ must be met at all times
   B. Voltage levels at I/Os and outputs must be less than V_{DDQ} during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, $V_{DD} \geq V_{DDL} \geq V_{DDQ}$ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete.
      - Apply V_{DD}/V_{DDL}[*3] before or at the same time as V_{DDQ}
      - Apply V_{DDQ}[*4] before or at the same time as V_{TT}
      - V_{REF}[*2] tracks $V_{DDQ}/2$
      - $V_{DDQ} \geq V_{REF}$ must be met at all times.
      - Apply V_{TT}
      - The V_{TT} voltage ramp time from when V_{DDQ} min is achieved on V_{DDQ} to when V_{TT} min is achieved on V_{TT} must be no greater than 500 mS
2. Start Clock and maintain stable condition for 200 µS (min.).
3. After stable power and clock (CLK, $\overline{CLK}$), apply NOP or Deselect and take CKE HIGH.
4. Wait minimum of 400 nS then issue precharge all command. NOP or Deselect applied during 400 nS period.
5. Issue an EMRS command to EMR (2). (To issue EMRS command to EMR (2), provide LOW to BA0, HIGH to BA1, LOW to BA2.)
6. Issue an EMRS command to EMR (3). (To issue EMRS command to EMR (3), provide HIGH to BA0 and BA1, LOW to BA2.)
7. Issue an EMRS command to EMR (1) to enable DLL. (To issue DLL Enable command, provide LOW to A0, HIGH to BA0 and LOW to BA1, LOW to BA2. And A9=A8=A7=LOW must be used when issuing this command.)
8. Issue a Mode Register Set command for DLL reset. (To issue DLL Reset command, provide HIGH to A8 and LOW to BA0 and BA1 and BA2.)
9. Issue a precharge all command.
10. Issue 2 or more Auto Refresh commands.
11. Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS to EMR (1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR (1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR (1).
13. The DDR2 SDRAM is now ready for normal operation.

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Notes:

1. To guarantee ODT off, VREF must be valid and a LOW level must be applied to the ODT pin.
2. VREF must be within ± 300 mV with respect to VDDQ/2 during supply ramp time.
3. VDD/VDDL voltage ramp time must be no greater than 200 mS from when VDD ramps from 300 mV to VDD min.
4. The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500 mS.

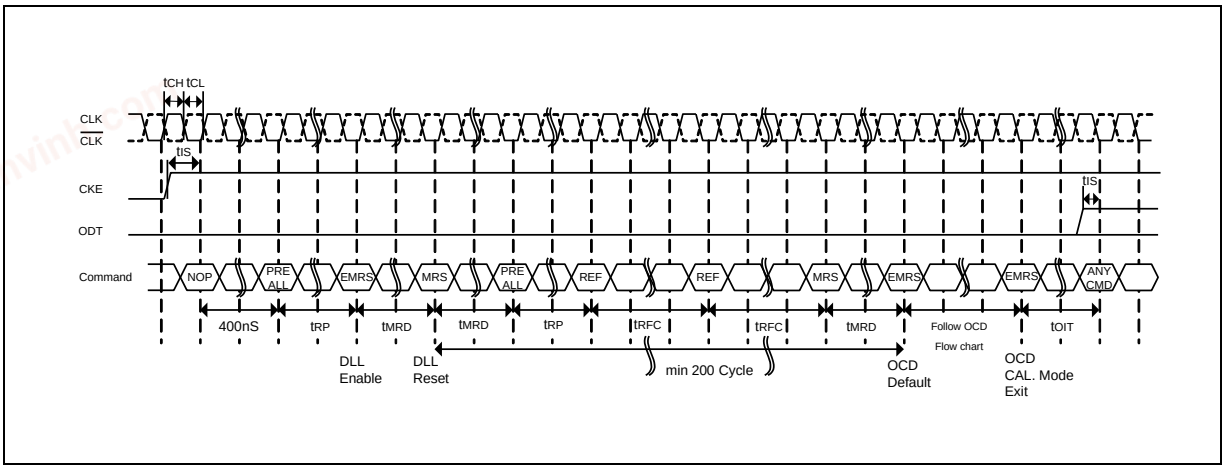


Figure 1 – Initialization sequence after power-up

8.2 Mode Register and Extended Mode Registers Operation

For application flexibility, burst length, burst type, CAS Latency, DLL reset function, write recovery time (WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS Latency, ODT (On Die Termination), single-ended strobe and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers EMR (1), EMR (2) and EMR (3) can be altered by re-executing the MRS or EMRS Commands. Even if the user chooses to modify only a subset of the MR or EMR (1), EMR (2) and EMR (3) variables, all variables within the addressed register must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which mean re-initialization including those can be executed at any time after power-up without affecting array contents.

8.2.1 Mode Register Set Command (MRS)

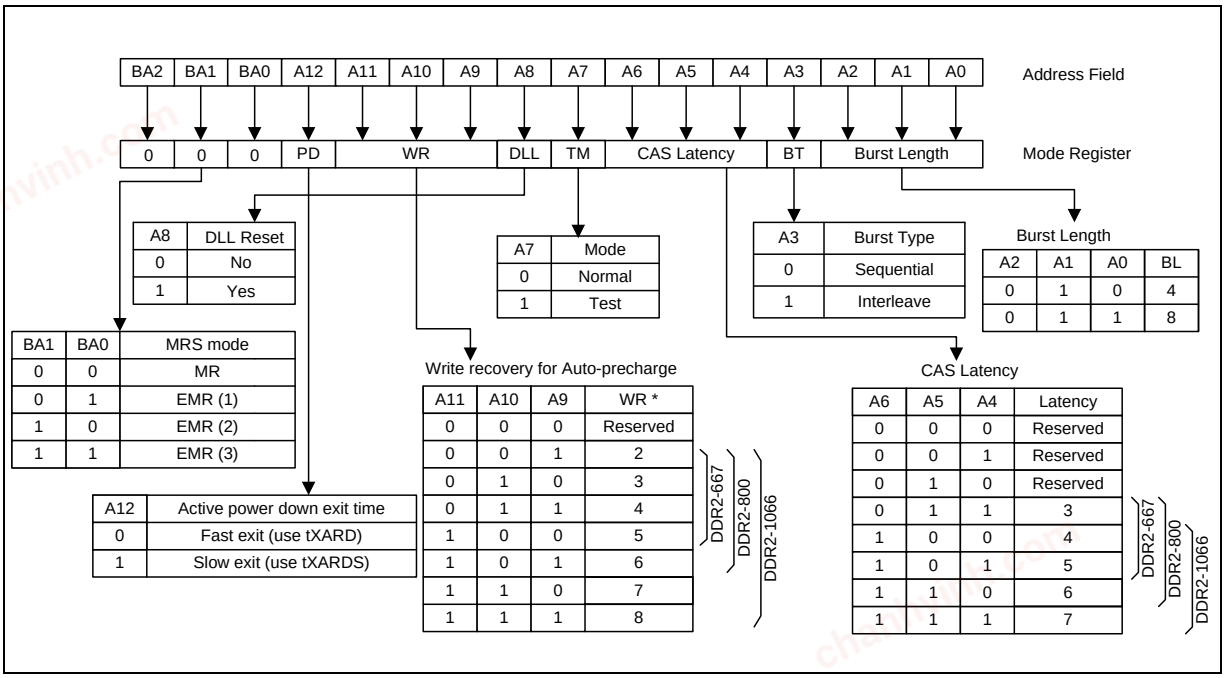
($\overline{CS}$ = "L", $\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "L", BA1 = "L", BA2 = "L", A0 to A12 = Register Data)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs CAS Latency, burst length, burst sequence, test mode, DLL reset, Write Recovery (WR) and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value in the Mode Register after power-up is not defined; therefore the Mode Register must be programmed during initialization for proper operation.

The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

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The mode register is divided into various fields depending on functionality. Burst length is defined by A[2:0] with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS Latency is defined by A[6:4]. The DDR2 does not support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to LOW for normal MRS operation. Write recovery time WR is defined by A[11:9]. Refer to the table for specific codes.



Note:

1. WR (write recovery for Auto-precharge) min is determined by tCK(avg) max and WR max is determined by tCK(avg) min. WR[cycles] = RU{ tWR[nS] / tCK(avg)[nS] }, where RU stands for round up. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Figure 2 – Mode Register Set (MRS)

8.2.2 Extend Mode Register Set Commands (EMRS)

8.2.2.1 Extend Mode Register Set Command (1), EMR (1)

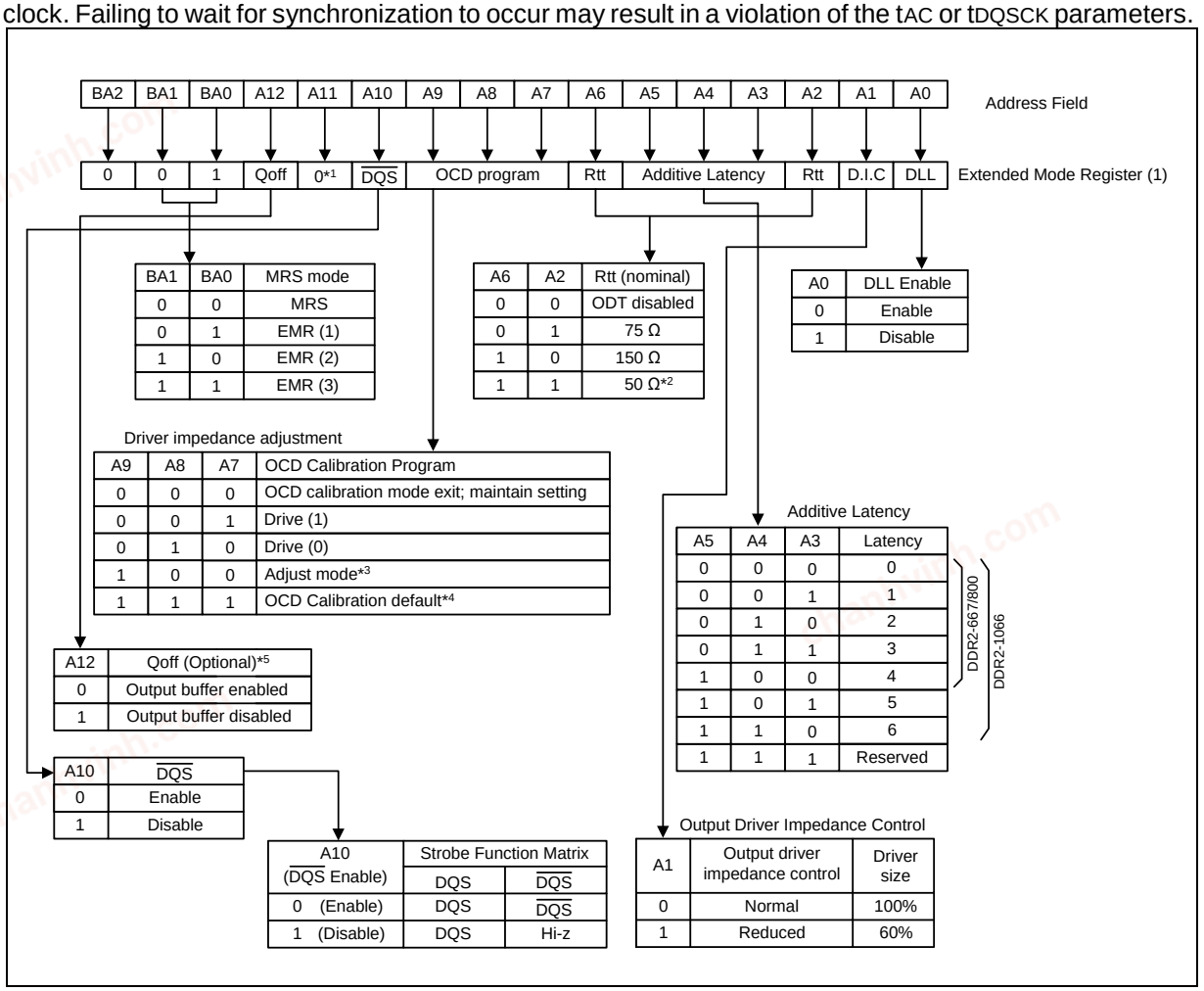
($\overline{CS}$ = "L", $\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "H", BA1 = "L, BA2 = "L" A0 to A12 = Register data)

The extended mode register (1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, $\overline{DQS}$ disable, OCD program. The default value of the extended mode register (1) is not defined; therefore the extended mode register (1) must be programmed during initialization for proper operation. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register (1). The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register (1). Extended mode register (1) contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a reduced strength output driver. A[5:3] determines the additive latency, A[9:7] are used for OCD control, A10 is used for $\overline{DQS}$ disable. A2 and A6 are used for ODT setting.

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8.2.2.2 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self Refresh operation and is automatically re-enabled and reset upon exit of Self Refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{AC} or t_{DQSCK} parameters.



Notes:

1. A11 default is “0” RDQS disabled.
2. Optional for DDR2-667, mandatory for DDR2-800 and DDR2-1066.
3. When Adjust mode is issued, AL from previously set value must be applied.
4. After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000. Refer to the section 8.2.3 for detailed information.
5. Output disabled - DQs, LDQS, $\overline{\text{LDQS}}$, UDQS, $\overline{\text{UDQS}}$. This feature is used in conjunction with DIMM I_{DD} measurements when I_{DDQ} is not desired to be included.

Figure 3 – EMR (1)

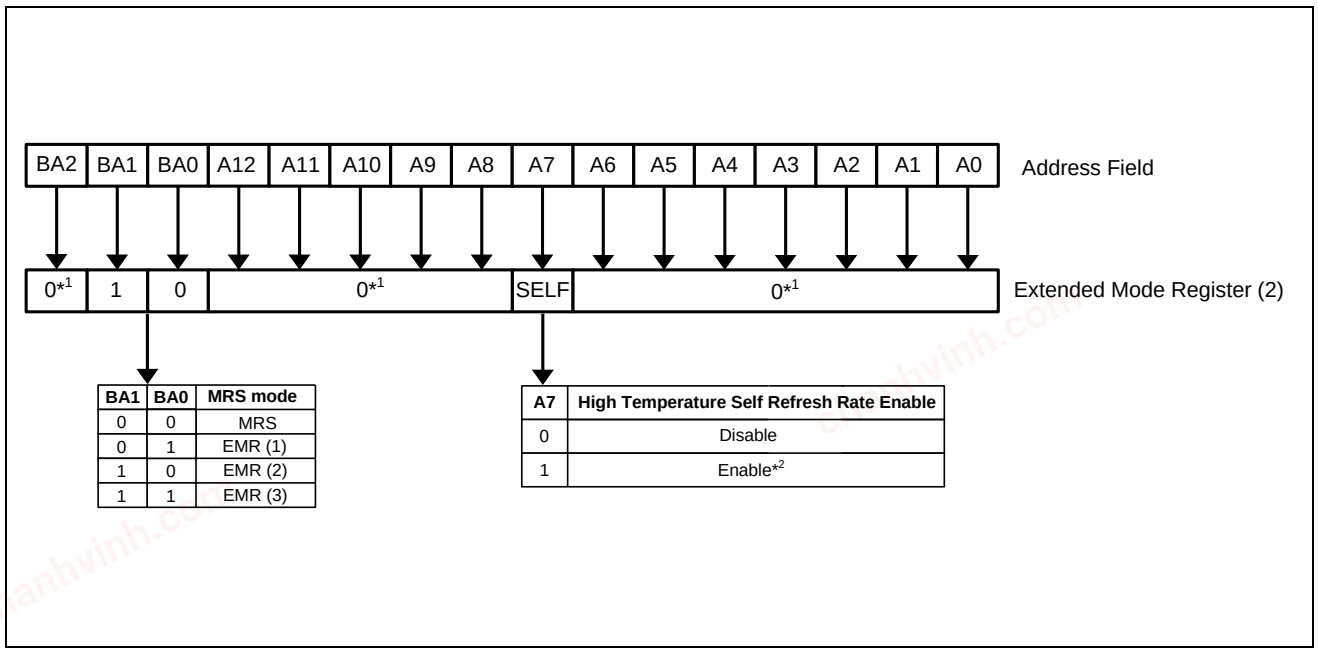
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8.2.2.3 Extend Mode Register Set Command (2), EMR (2)

($\overline{CS}$ = "L", $\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "L", BA1 = "H", BA2 = "L" A0 to A12 = Register data)

The extended mode register (2) controls refresh related features. The default value of the extended mode register (2) is not defined; therefore the extended mode register (2) must be programmed during initialization for proper operation.

The DDR2 SDRAM should be in all bank precharge state with CKE already high prior to writing into the extended mode register (2). The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.



Notes:

1. The rest bits in EMR (2) is reserved for future use and all bits in EMR (2) except A7, BA0, BA1 and BA2 must be programmed to “0” when setting the extended mode register (2) during initialization.
2. When DRAM is operated at 85°C < T_{CASE} ≤ 95°C or 105°C the extended Self Refresh rate must be enabled by setting bit A7 to “1” before the Self Refresh mode can be entered.

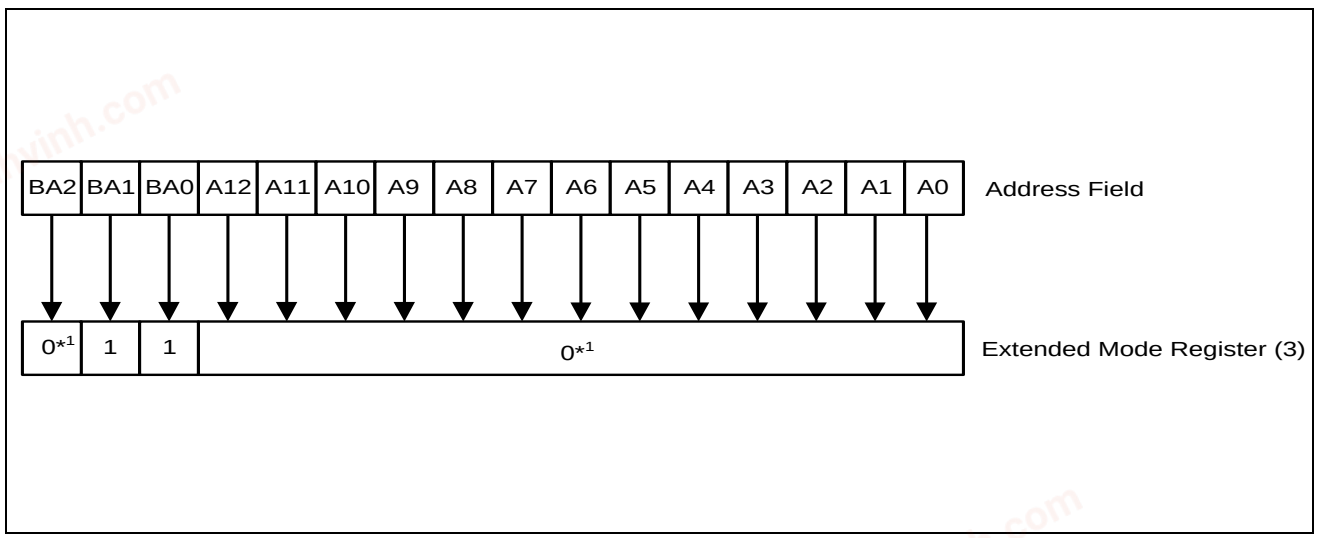
Figure 4 – EMR (2)

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8.2.2.4 Extend Mode Register Set Command (3), EMR (3)

($\overline{CS}$ = "L", $\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "H", BA1 = "H", BA2 = "L", A0 to A12 = Register data)

No function is defined in extended mode register (3). The default value of the EMR (3) is not defined; therefore the EMR (3) must be programmed during initialization for proper operation.



Note:

1. All bits in EMR (3) except BA0 and BA1 are reserved for future use and must be set to “0” when programming the EMR (3).

Figure 5 – EMR (3)

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8.2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart in Figure 6 is an example of the sequence. Every calibration mode command should be followed by “OCD calibration mode exit” before any other command being issued. MRS should be set before entering OCD impedance adjustment and On Die Termination (ODT) should be carefully controlled depending on system environment.

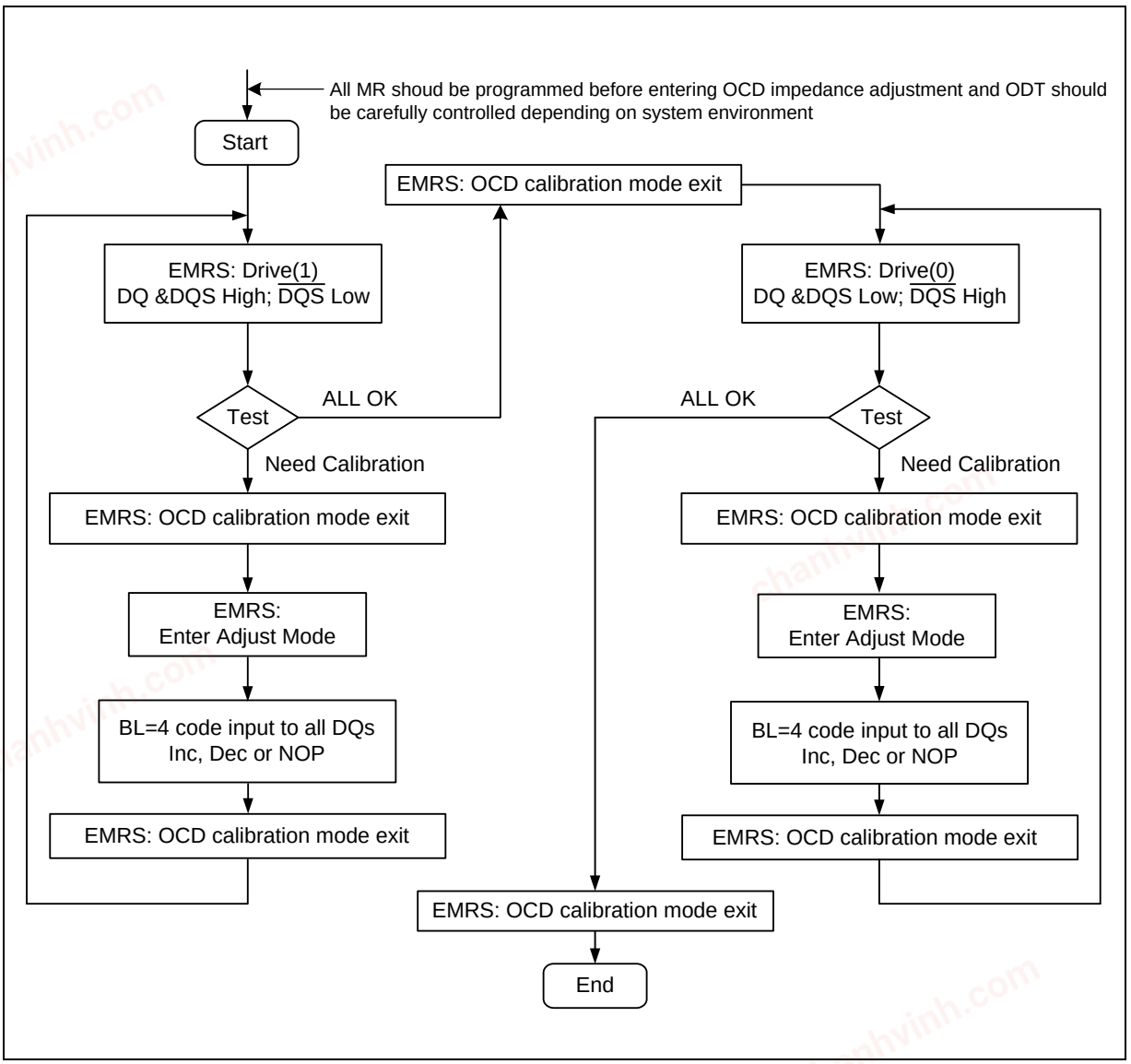


Figure 6 – OCD Impedance Adjustment Flow Chart

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8.2.3.1 Extended Mode Register for OCD Impedance Adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM. In Drive (1) mode, all DQ, DQS signals are driven HIGH and all $\overline{DQS}$ signals are driven LOW. In Drive (0) mode, all DQ, DQS signals are driven LOW and all $\overline{DQS}$ signals are driven HIGH. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and voltage conditions. OCD applies only to normal full strength output drive setting defined by EMR (1) and if reduced strength is set, OCD default driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A[9:7] as '000' in order to maintain the default or calibrated value.

Table 1 – OCD Drive Mode Program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive (1) DQ, DQS HIGH and $\overline{DQS}$ LOW
0	1	0	Drive (0) DQ, DQS LOW and $\overline{DQS}$ HIGH
1	0	0	Adjust mode
1	1	1	OCD calibration default

8.2.3.2 OCD Impedance Adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4 bit burst code to DDR2 SDRAM as in table 2. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT_0 in table 2 means all DQ bits at bit time 0, DT_1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs and DQS's of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

Table 2 – OCD Adjust Mode Program

4 bit burst code inputs to all DQs				Operation	
DT_0	DT_1	DT_2	DT_3	**Pull-up driver strength**	**Pull-down driver strength**
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

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For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and t_{DS}/t_{DH} should be met as shown in Figure 7. For input data pattern for adjustment, D_{T0} - D_{T3} is a fixed order and is not affected by burst type (i.e., sequential or interleave).

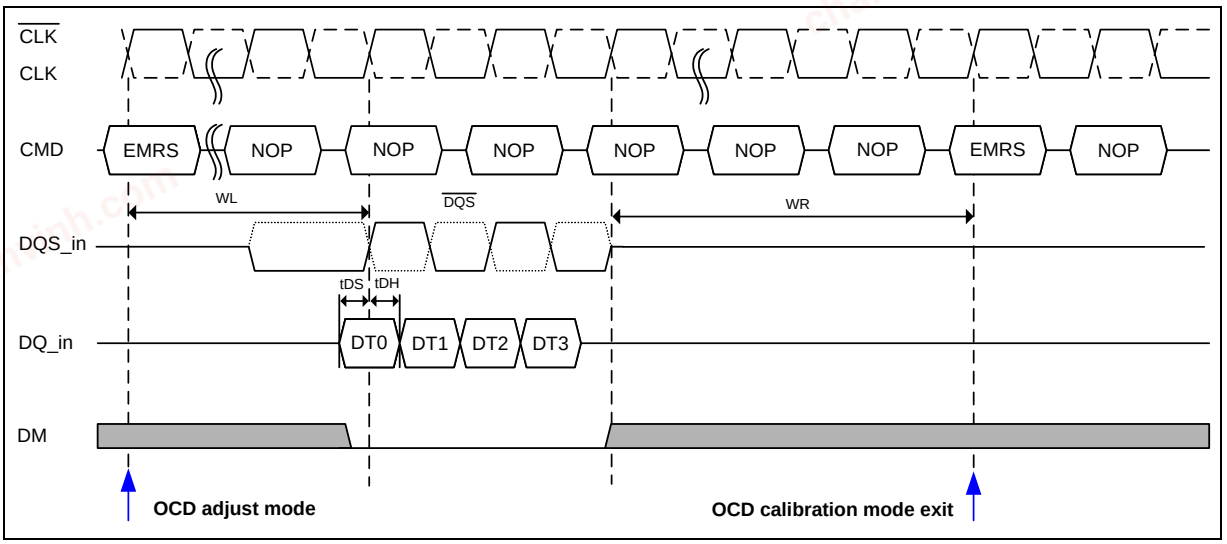


Figure 7 – OCD Adjust Mode

8.2.3.3 Drive Mode

Drive mode, both Drive (1) and Drive (0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out t_{OIT} after "enter drive mode" command and all output drivers are turned-off t_{OIT} after "OCD calibration mode exit" command as shown in Figure 8.

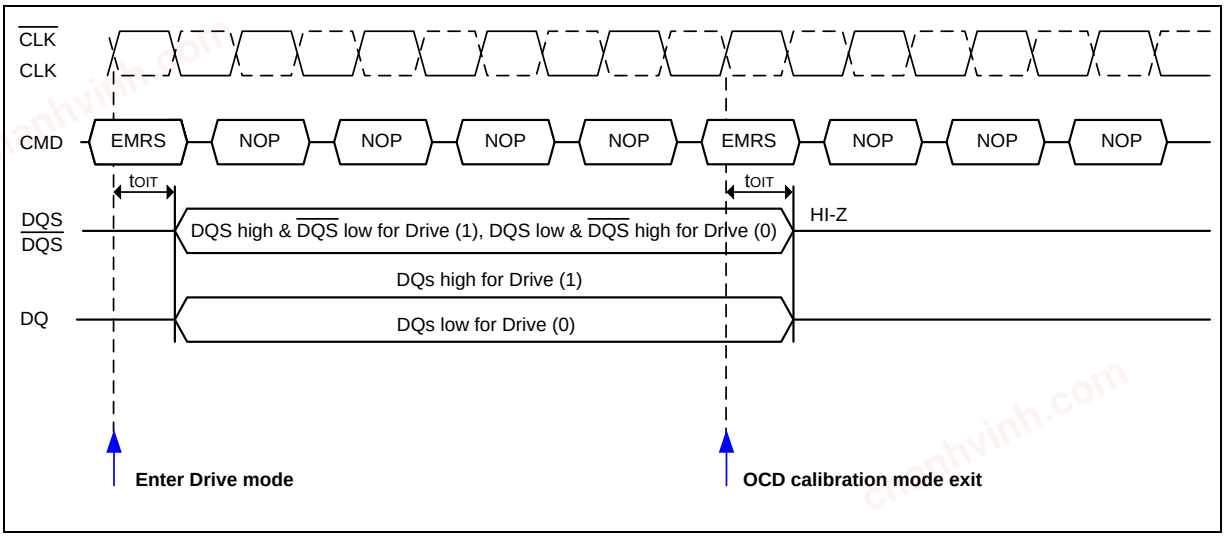


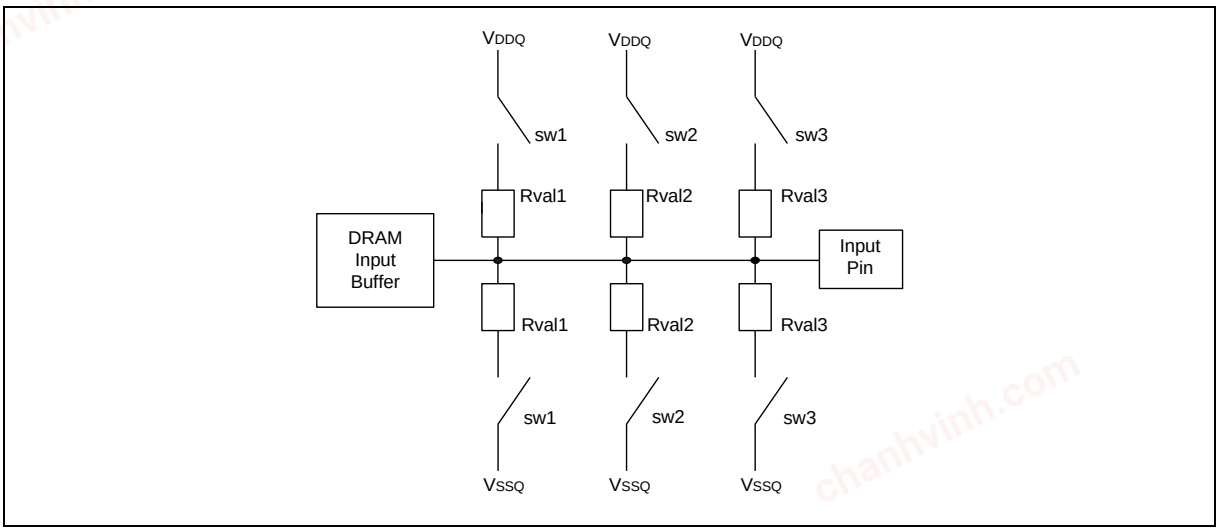
Figure 8 – OCD Drive Mode

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8.2.4 On-Die Termination (ODT)

On-Die Termination (ODT) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, UDQS/$\overline{\text{UDQS}}$, LDQS/$\overline{\text{LDQS}}$, UDM and LDM signal via the ODT control pin. $\overline{\text{UDQS}}$ and $\overline{\text{LDQS}}$ are terminated only when enabled in the EMR (1) by address bit A10 = 0. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self Refresh mode. *(Example timing waveforms refer to 11.2, 11.3 ODT Timing for Active/Standby/Power Down Mode and 11.4, 11.5 ODT timing mode switch at entering/exiting power down mode diagram in Chapter 11)*



Switch (sw1, sw2, sw3) is enabled by ODT pin.

Selection among sw1, sw2, and sw3 is determined by “Rtt (nominal)” in EMR (1).

Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$ pins.

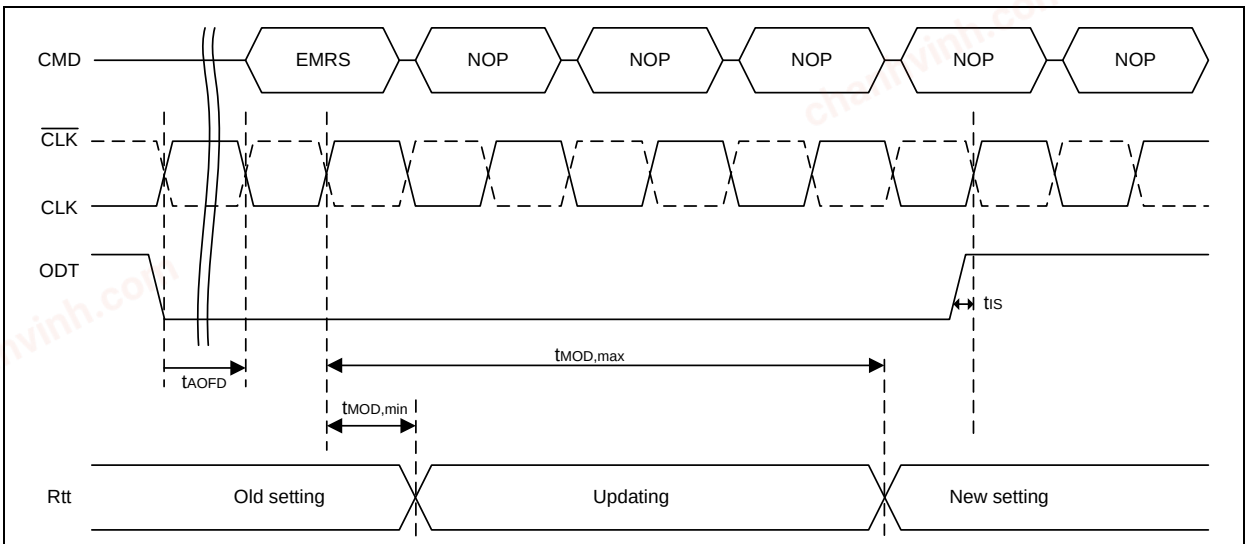
Figure 9 – Functional Representation of ODT

8.2.5 ODT related timings

8.2.5.1 MRS command to ODT update delay

During normal operation the value of the effective termination resistance can be changed with an EMRS command. The update of the Rtt setting is done between $t_{MOD,min}$ and $t_{MOD,max}$, and CKE must remain HIGH for the entire duration of t_{MOD} window for proper operation. The timings are shown in the following timing diagram.

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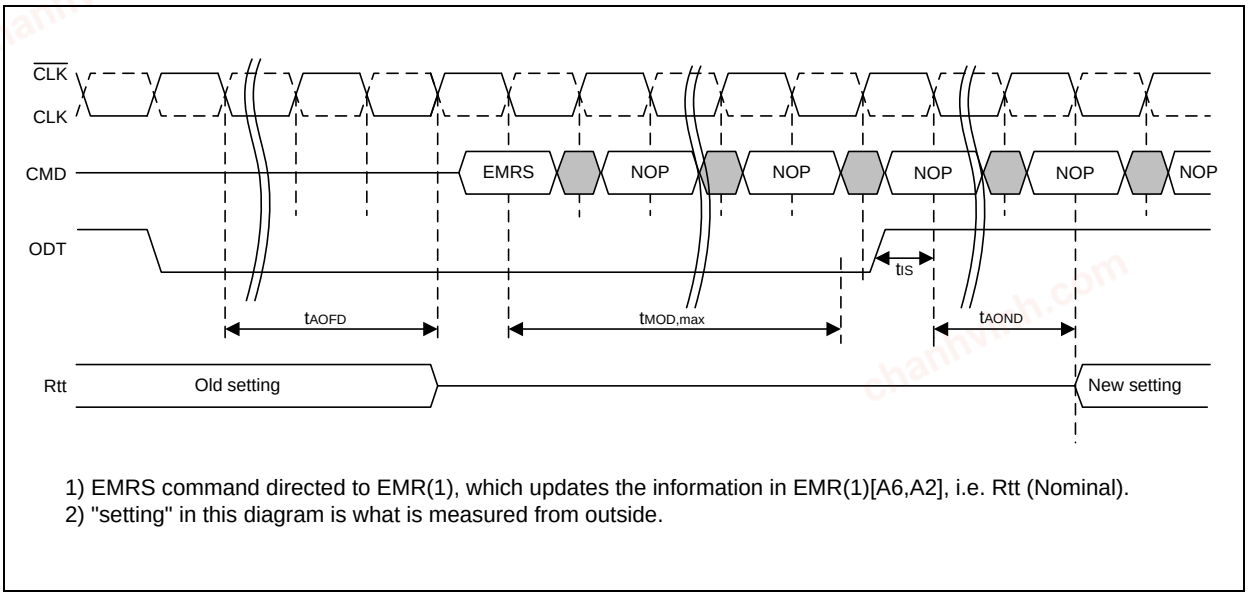
1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
2) "setting" in this diagram is the Register and I/O setting, not what is measured from outside.

Figure 10 – ODT update delay timing - tMOD

However, to prevent any impedance glitch on the channel, the following conditions must be met.

- tAOFD must be met before issuing the EMRS command.
- ODT must remain LOW for the entire duration of tMOD window, until tMOD,max is met.

Now the ODT is ready for normal operation with the new setting, and the ODT signal may be raised again to turned on the ODT. Following timing diagram shows the proper Rtt update procedure.



1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
2) "setting" in this diagram is what is measured from outside.

Figure 11 – ODT update delay timing - tMOD, as measured from outside

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8.3 Command Function

8.3.1 Bank Activate Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="L", $\overline{CAS}$ ="H", $\overline{WE}$ ="H", BA0, BA1, BA2=Bank, A0 to A12 be row address)

The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a Read/Write command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the Read/Write command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3, 4, 5 and 6 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between Bank Activate commands is tRRD.

In order to ensure that components with 8 internal memory banks do not exceed the instantaneous current supplying capability, certain restrictions on operation of the 8 banks must be observed. There are two rules. One for restricting the number of sequential ACT commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

- Sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW[nS] by tCK(avg)[ns], and rounding up to next integer value. As an example of the rolling window, if RU{ (tFAW / tCK(avg) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9.
- Precharge All Allowance: tRP for a Precharge All command is equal to tnRP + 1 x nCK, where tnRP = RU{ tRP / tCK(avg) } and tRP is the value for a single bank precharge.

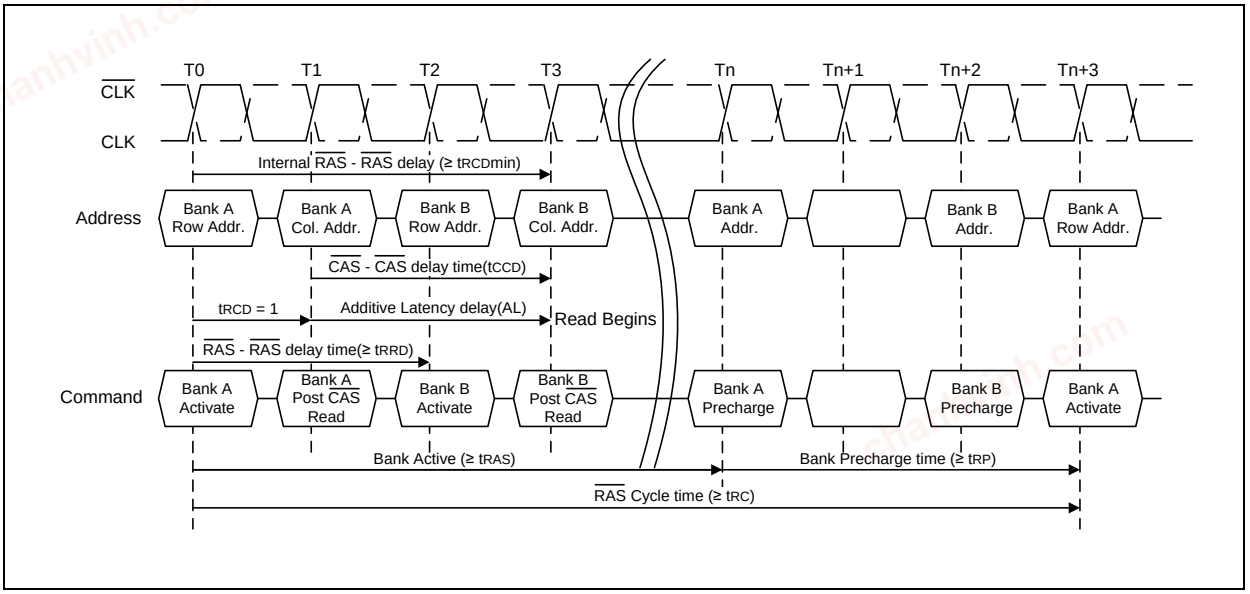


Figure 12 – Bank activate command cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2

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8.3.2 Read Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", BA0, BA1, BA2=Bank, A10="L", A0 to A9=Column Address)

The READ command is used to initiate a burst read access to an active row. The value on BA0, BA1, BA2 inputs selects the bank, and the A0 to A9 address inputs determine the starting column address. The address input A10 determines whether or not Auto-precharge is used. If Auto-precharge is selected, the row being accessed will be precharged at the end of the READ burst; if Auto-precharge is not selected, the row will remain open for subsequent accesses.

8.3.3 Write Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="L", BA0, BA1, BA2=Bank, A10="L", A0 to A9=Column Address)

The WRITE command is used to initiate a burst write access to an active row. The value on BA0, BA1, BA2 inputs selects the bank, and the A0 to A9 address inputs determine the starting column address. The address input A10 determines whether or not Auto-precharge is used. If Auto-precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if Auto-precharge is not selected, the row will remain open for subsequent accesses.

8.3.4 Burst Read with Auto-precharge Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", BA0, BA1, BA2=Bank, A10="H", A0 to A9=Column Address)

If A10 is HIGH when a Read Command is issued, the Read with Auto-precharge function is engaged. The DDR2 SDRAM starts an Auto-precharge operation on the rising edge which is (AL + BL/2) cycles later than the read with AP command if t_{RAS}(min) and t_{RTP}(min) are satisfied.

8.3.5 Burst Write with Auto-precharge Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="L", BA0, BA1, BA2=Bank, A10="H", A0 to A9=Column Address)

If A10 is HIGH when a Write Command is issued, the Write with Auto-precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (WR) programmed in the mode register.

8.3.6 Precharge All Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="L", $\overline{CAS}$ ="H", $\overline{WE}$ ="L", BA0, BA1, BA2=Don't Care, A10="H", A0 to A9 and A11 to A12=Don't Care)

The Precharge All command precharge all banks simultaneously. Then all banks are switched to the idle state.

8.3.7 Self Refresh Entry Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="L", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", CKE="L", BA0, BA1, BA2, A0 to A12=Don't Care)

The Self Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin LOW or using an EMRS command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the DDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are "Don't Care".

The clock is internally disabled during self refresh operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit self refresh operation.

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8.3.8 Self Refresh Exit Command

(CKE="H", $\overline{CS}$ ="H" or CKE="H", $\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="H", $\overline{WE}$ ="H", BA0, BA1, BA2, A0 to A12=Don't Care)

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least t_{XSNR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSRD} for proper operation except for self refresh re-entry.

Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after waiting at least t_{XSNR} period and issuing one refresh command (refresh period of t_{RFC}). NOP or Deselect commands must be registered on each positive clock edge during the Self Refresh exit interval t_{XSNR}. ODT should be turned off during t_{XSRD}.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.

8.3.9 Refresh Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="L", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", CKE="H", BA0, BA1, BA2, A0 to A12=Don't Care)

Refresh is used during normal operation of the DDR2 SDRAM. This command is non persistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto Refresh command. The DDR2 SDRAM requires Auto Refresh cycles at an average periodic interval of t_{REFI} (max.).

When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the auto refresh command (REF) and the next activate command or subsequent auto refresh command must be greater than or equal to the auto refresh cycle time (t_{RFC}).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 x t_{REFI}.

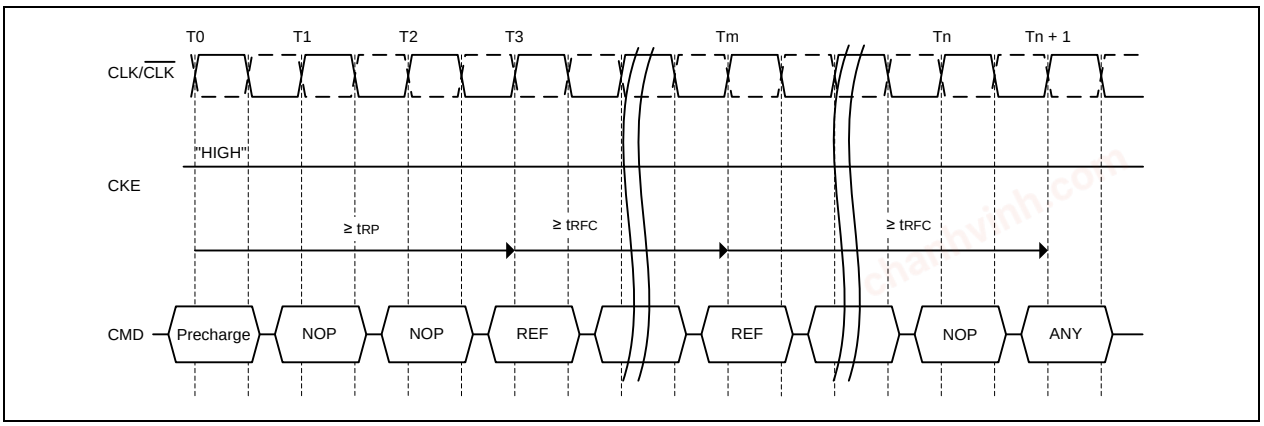


Figure 13 – Refresh command

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8.3.10 No-Operation Command

($\overline{CS}$ = "L", $\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "H", CKE, BA0, BA1, BA2, A0 to A12 = Don't Care)

The No-Operation command simply performs no operation (same command as Device Deselect).

8.3.11 Device Deselect Command

($\overline{CS}$ = "H", $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, BA0, BA1, BA2, A0 to A12 = Don't Care)

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

8.4 Read and Write access modes

The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length.

The 8 Mbit x 16 I/O x 8 Bank chip has a page length of 1024 bits (defined by CA0 to CA9)*. The page length of 1024 is divided into 256 or 128 uniquely addressable boundary segments depending on burst length, 256 for 4 bit burst, 128 for 8 bit burst respectively. A 4-bit or 8-bit burst operation will occur entirely within one of the 256 or 128 groups beginning with the column address supplied to the device during the Read or Write Command (CA0 to CA9). The second, third and fourth access will also occur within this group segment. However, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively. The minimum $\overline{CAS}$ to $\overline{CAS}$ delay is defined by t_{CCD}, and is a minimum of 2 clocks for read or write cycles.

Note: Page length is a function of I/O organization and column addressing
8M bits × 16 organization (CA0 to CA9); Page Length = 1024 bits

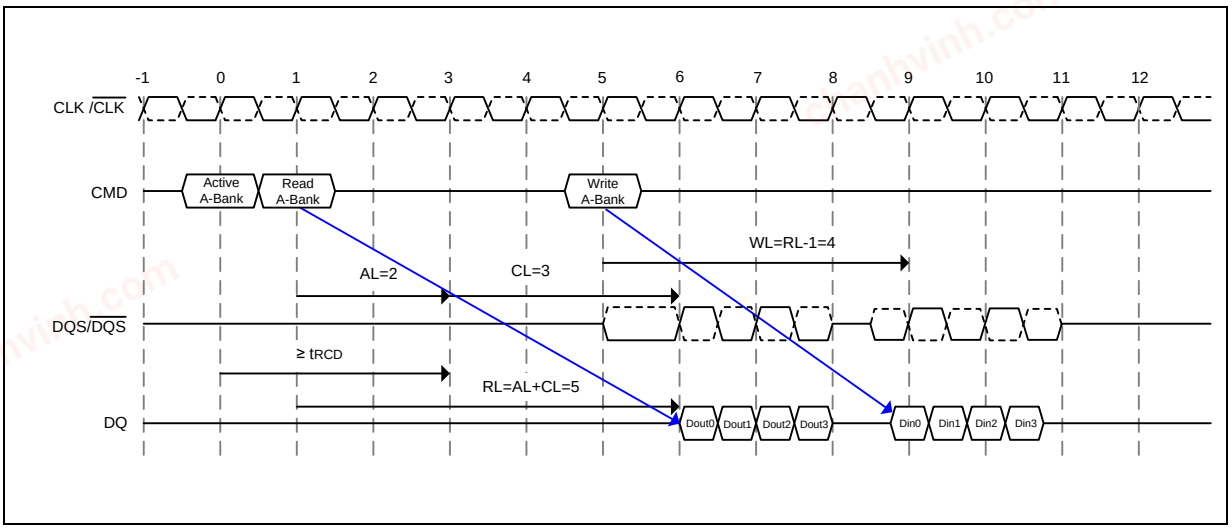
8.4.1 Posted $\overline{CAS}$

Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a $\overline{CAS}$ read or write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the $\overline{RAS}$ - $\overline{CAS}$ -delay time, t_{RCD}, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS Latency (CL). Therefore if a user chooses to issue a Read/Write command before the t_{RCDmin}, then AL (greater than 0) must be written into the EMR (1). The Write Latency (WL) is always defined as RL -1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus CAS Latency (RL = AL + CL). Read or Write operations using AL allow seamless bursts. *(Example timing waveforms refer to 11.10 and 11.11 seamless burst read/write operation diagram in Chapter 11)*

8.4.1.1 Examples of posted $\overline{CAS}$ operation

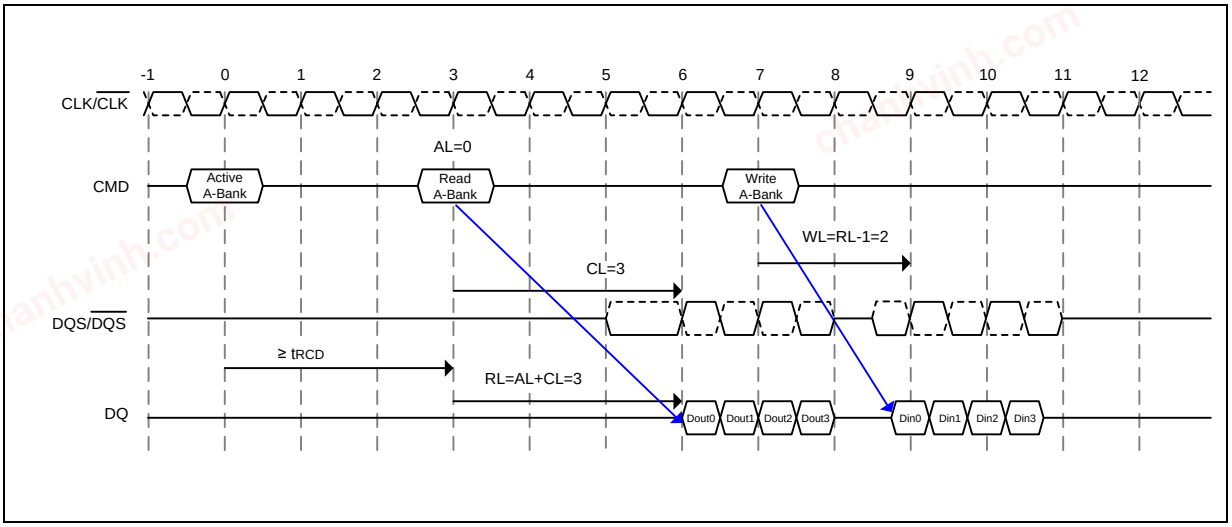
Examples of a read followed by a write to the same bank where AL = 2 and where AL = 0 are shown in Figures 14 and 15, respectively.

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[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

Figure 14 – Example 1: Read followed by a write to the same bank, where AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4



AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

Figure 15 – Example 2: Read followed by a write to the same bank, where AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4

8.4.2 Burst mode operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by MR A[2:0]. The burst type, either sequential or interleaved, is programmable and defined by MR [A3]. Seamless burst read or write operations are supported.

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Unlike DDR1 devices, interruption of a burst read or writes cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. *(Example timing waveforms refer to 11.12 and 11.13 Burst read and write interrupt timing diagram in Chapter 11)*

Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Table 3 – Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

8.4.3 Burst read mode operation

Burst Read is initiated with a READ command. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven LOW one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus CAS Latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register EMR (1). *(Example timing waveforms refer to 11.6 and 11.7 Data output (read) timing and Burst read operation diagram in Chapter 11)*

8.4.4 Burst write mode operation

Burst Write is initiated with a WRITE command. The address inputs determine the starting column address for the burst. Write Latency (WL) is defined by a Read Latency (RL) minus one and is equal to (AL + CL -1); and is the number of clocks of delay that are required from the time the write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven LOW (preamble) nominally half clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The t_{DQSS} specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR). *(Example timing waveforms refer to 11.8 and 11.9 Data input (write) timing and Burst write operation diagram in Chapter 11)*

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8.4.5 Write data mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAM, consistent with the implementation on DDR1 SDRAM. It has identical timings on write operations as the data bits, and though used in a unidirectional manner, is internally loaded identically to data bits to insure matched system timing. DM is not used during read cycles. *(Example timing waveform refer to 11.14 Write operation with Data Mask diagram in Chapter 11)*

8.5 Burst Interrupt

Read or Write burst interruption is prohibited for burst length of 4 and only allowed for burst length of 8 under the following conditions:

1. Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write or Precharge Command is prohibited.
2. Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read or Precharge Command is prohibited.
3. Read burst interrupt must occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.
4. Write burst interrupt must occur exactly two clocks after the previous Write command. Any other Write burst interrupt timings are prohibited.
5. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.
6. Read or Write burst with Auto-precharge enabled is not allowed to interrupt.
7. Read burst interruption is allowed by a Read with Auto-precharge command.
8. Write burst interruption is allowed by a Write with Auto-precharge command.
9. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example below:
   - Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).
   - Minimum Write to Precharge timing is WL + BL/ 2 + t_{WR}, where t_{WR} starts with the rising clock after the un-interrupted burst end and not from the end of the actual burst end.

(Example timing waveforms refer to 11.12 and 11.13 Burst read and write interrupt timing diagram in Chapter 11)

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8.6 Precharge operation

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 and BA2 are used to define which bank to precharge when the command is issued.

Table 4 – Bank selection for precharge by address bits

A10	BA2	BA1	BA0	Precharge Bank(s)
LOW	LOW	LOW	LOW	Bank 0 only
LOW	LOW	LOW	HIGH	Bank 1 only
LOW	LOW	HIGH	LOW	Bank 2 only
LOW	LOW	HIGH	HIGH	Bank 3 only
LOW	HIGH	LOW	LOW	Bank 4 only
LOW	HIGH	LOW	HIGH	Bank 5 only
LOW	HIGH	HIGH	LOW	Bank 6 only
LOW	HIGH	HIGH	HIGH	Bank 7 only
HIGH	Don't Care	Don't Care	Don't Care	All Banks

8.6.1 Burst read operation followed by precharge

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 + max(RTP, 2) - 2 clks

For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive Latency (AL) + BL/2 + max(RTP, 2) - 2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (tRP). A precharge command cannot be issued until tRAS is satisfied.

The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called tRTP (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command. *(Example timing waveforms refer to 11.15 to 11.19 Burst read operation followed by precharge diagram in Chapter 11)*

8.6.2 Burst write operation followed by precharge

Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clks + tWR

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay. *(Example timing waveforms refer to 11.20 to 11.21 Burst write operation followed by precharge diagram in Chapter 11)*

8.7 Auto-precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the Auto-precharge function. When a Read or a Write command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is LOW when the READ or WRITE command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is HIGH when the Read or Write command is issued, then the Auto-precharge function is engaged. During Auto-precharge, a Read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is CAS Latency (CL) clock cycles before the end of the read burst.

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Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto-precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS Latency) thus improving system performance for random data access. The $\overline{RAS}$ lockout circuit internally delays the Precharge operation until the array restore operation has been completed (t_{RAS} satisfied) so that the Auto-precharge command may be issued with any read or write command.

8.7.1 Burst read with Auto-precharge

If A10 is HIGH when a Read Command is issued, the Read with Auto-precharge function is engaged. The DDR2 SDRAM starts an Auto-precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if t_{RAS}(min) and t_{RTP}(min) are satisfied. *(Example timing waveform refer to 11.22 Burst read operation with Auto-precharge diagram in Chapter 11)*

If t_{RAS}(min) is not satisfied at the edge, the start point of Auto-precharge operation will be delayed until t_{RAS}(min) is satisfied.

If t_{RTP}(min) is not satisfied at the edge, the start point of Auto-precharge operation will be delayed until t_{RTP}(min) is satisfied.

In case the internal precharge is pushed out by t_{RTP}, t_{RP} starts at the point where t_{RTP} ends (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-precharge to the next Activate command becomes AL + RU{ (t_{RTP} + t_{RP}) / $t_{CK(avg)}$ } *(Example timing waveform refer to 11.23 Burst read operation with Auto-precharge diagram in Chapter 11.)*, for BL = 8 the time from Read with Auto-precharge to the next Activate command is AL + 2 + RU{ (t_{RTP} + t_{RP}) / $t_{CK(avg)}$ }, where RU stands for “rounded up to the next integer”. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously.

- The $\overline{RAS}$ precharge time (t_{RP}) has been satisfied from the clock at which the Auto-precharge begins.
- The $\overline{RAS}$ cycle time (t_{RC}) from the previous bank activation has been satisfied.

(Example timing waveforms refer to 11.24 to 11.25 Burst read with Auto-precharge followed by an activation to the same bank (t_{RC} Limit) and (t_{RP} Limit) diagram in Chapter 11)

8.7.2 Burst write with Auto-precharge

If A10 is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (WR) programmed in the mode register. The bank undergoing Auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

- The data-in to bank activate delay time (WR + t_{RP}) has been satisfied.
- The $\overline{RAS}$ cycle time (t_{RC}) from the previous bank activation has been satisfied.

(Example timing waveforms refer to 11.26 to 11.27 Burst write with Auto-precharge (t_{RC} Limit) and (WR + t_{RP} Limit) diagram in Chapter 11)

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Table 5 – Precharge & Auto-precharge clarifications

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	AL + BL/2 + max(RTP, 2) - 2	clks	1, 2
	Precharge All	AL + BL/2 + max(RTP, 2) - 2	clks	1, 2
Read w/AP	Precharge (to same Bank as Read w/AP)	AL + BL/2 + max(RTP, 2) - 2	clks	1, 2
	Precharge All	AL + BL/2 + max(RTP, 2) - 2	clks	1, 2
Write	Precharge (to same Bank as Write)	WL + BL/2 + tWR	clks	2
	Precharge All	WL + BL/2 + tWR	clks	2
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + WR	clks	2
	Precharge All	WL + BL/2 + WR	clks	2
Precharge	Precharge (to same Bank as Precharge)	1	clks	2
	Precharge All	1	clks	2
Precharge All	Precharge	1	clks	2
	Precharge All	1	clks	2

Notes:

1. RTP[cycles] = RU{ tRTP[nS] / tCK(avg)[nS] }, where RU stands for round up.
2. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRPall (= tRP + 1 x tCK) depending on the latest precharge command issued to that bank.

8.8 Refresh Operation

DDR2 SDRAM requires a refresh of all rows in any rolling 64 ms interval. The necessary refresh can be generated in one of two ways: by explicit Auto Refresh commands or by an internally timed Self Refresh mode. Dividing the number of device rows into the rolling 64 ms interval defines the average refresh interval, tREFI, which is a guideline to controllers for distributed refresh timing.

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held LOW and $\overline{WE}$ HIGH at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started. *(Example timing waveform refer to 11.28 Self Refresh diagram in Chapter 11)*

8.9 Power Down Mode

Power-down is synchronously entered when CKE is registered LOW, along with NOP or Deselect command. CKE is not allowed to go LOW while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go LOW while any other operation such as row activation, Precharge or Auto-precharge or Auto Refresh is in progress, but power down IDD specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

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8.9.1 Power Down Entry

Two types of Power Down Mode can be performed on the device: Precharge Power Down Mode and Active Power Down Mode.

If power down occurs when all banks are idle, this mode is referred to as Precharge Power Down; if power down occurs when there is a row active in any bank, this mode is referred to as Active Power Down. Entering power down deactivates the input and output buffers, excluding CLK, $\overline{CLK}$, ODT and CKE. Also the DLL is disabled upon entering Precharge Power Down or slow exit Active Power Down, but the DLL is kept enabled during fast exit Active Power Down.

In power down mode, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and ODT should be in a valid state but all other input signals are “Don’t Care”. CKE LOW must be maintained until t_{CKE} has been satisfied. Maximum power down duration is limited by the refresh requirements of the device, which allows a maximum of 9 x t_{REFI} if maximum posting of REF is utilized immediately before entering power down. *(Example timing waveforms refer to 11.29 Basic Power Down Entry and Exit diagram and 11.30 Precharged Power Down Entry and Exit diagram in Chapter 11)*

8.9.2 Power Down Exit

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or Deselect command). CKE high must be maintained until t_{CKE} has been satisfied. A valid, executable command can be applied with power-down exit latency, t_{XP}, t_{XARD}, or t_{XARDS}, after CKE goes HIGH. Power-down exit latency is defined at AC Characteristics table of this data sheet.

8.10 Input clock frequency change during precharge power down

DDR2 SDRAM input clock frequency can be changed under following condition:

DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels.

Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via MRS command after precharge power down exit. Depending on new clock frequency an additional MRS or EMRS command may need to be issued to appropriately set the WR, CL etc…

During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency. *(Example timing waveform refer to 11.31 Clock frequency change in precharge Power Down mode diagram in Chapter 11)*

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9. OPERATION MODE

9.1 Command Truth Table

COMMAND	CKE		BA2 BA1 BA0	A12 A11	A10	A9-A0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	NOTES
	Previous Cycle	Current Cycle									
Bank Activate	H	H	BA	Row Address			L	L	H	H	1,2
Single Bank Precharge	H	H	BA	X	L	X	L	L	H	L	1,2
Precharge All Banks	H	H	X	X	H	X	L	L	H	L	1
Write	H	H	BA	Column	L	Column	L	H	L	L	1,2,3
Write with Auto-precharge	H	H	BA	Column	H	Column	L	H	L	L	1,2,3
Read	H	H	BA	Column	L	Column	L	H	L	H	1,2,3
Read with Auto-precharge	H	H	BA	Column	H	Column	L	H	L	H	1,2,3
(Extended) Mode Register Set	H	H	BA	OP Code			L	L	L	L	1,2
No Operation	H	X	X	X	X	X	L	H	H	H	1
Device Deselect	H	X	X	X	X	X	H	X	X	X	1
Refresh	H	H	X	X	X	X	L	L	L	H	1
Self Refresh Entry	H	L	X	X	X	X	L	L	L	H	1,4
Self Refresh Exit	L	H	X	X	X	X	H	X	X	X	1,4,5
							L	H	H	H	
Power Down Mode Entry	H	L	X	X	X	X	H	X	X	X	1,6
							L	H	H	H	
Power Down Mode Exit	L	H	X	X	X	X	H	X	X	X	1,6
							L	H	H	H	

Notes:

1. All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
2. Bank addresses BA [2:0] determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL = 4 can not be terminated or interrupted. See **"Burst Interrupt"** in section 8.5 for details.
4. V_{REF} must be maintained during Self Refresh operation.
5. Self Refresh Exit is asynchronous.
6. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section 8.8.

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9.2 Clock Enable (CKE) Truth Table for Synchronous Transitions

CURRENT STATE[2]	CKE		COMMAND (N)[3]	ACTION (N)[3]	NOTES
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain Power Down	11, 13, 15
	L	H	DESELECT or NOP	Power Down Exit	4, 8, 11, 13
Self Refresh	L	L	X	Maintain Power Down	11, 15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5, 9, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4, 8, 10, 11, 13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	4, 8, 10, 11, 13
	H	L	REFRESH	Self Refresh Entry	6, 9, 11, 13
	H	H	Refer to the Command Truth Table		7

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELECT only.
10. Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See section 8.9 **"Power Down Mode"** and section 8.3.7/8.3.8 **"Self Refresh Entry Command/Self Refresh Exit Command"** for a detailed list of restrictions.
11. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 8.2.4.
13. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section 8.8.
14. CKE must be maintained HIGH while the SDRAM is in OCD calibration mode.
15. "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMR (1)).
16. V_{REF} must be maintained during Self Refresh operation.

9.3 Data Mask (DM) Truth Table

FUNCTION	DM	DQS	NOTE
Write enable	L	Valid	1
Write inhibit	H	X	1

Note:

1. Used to mask write data, provided coincident with the corresponding data.

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9.4 Function Truth Table

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	ACTION	NOTES
Idle	H	X	X	X	X	DSL	NOP or Power down	
	L	H	H	H	X	NOP	NOP or Power down	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PREA	Precharge/ Precharge all banks	
	L	L	L	H	X	REF/SELF	Auto Refresh or Self Refresh	2
	L	L	L	L	Op-Code	MRS/EMRS	Mode/Extended register accessing	2
Banks Active	H	X	X	X	X	DSL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	Precharge/ Precharge all banks	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Read	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	Burst interrupt	1,3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Burst interrupt	1,3
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

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Function Truth Table, continued

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	ACTION	NOTES
Read with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Precharge	H	X	X	X	X	DSL	NOP-> Idle after t_{RP}	
	L	H	H	H	X	NOP	NOP-> Idle after t_{RP}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	NOP-> Idle after t_{RP}	1
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Row Activating	H	X	X	X	X	DSL	NOP-> Row active after t_{RCD}	
	L	H	H	H	X	NOP	NOP-> Row active after t_{RCD}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

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Function Truth Table, continued

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	ACTION	NOTES
Write Recovering	H	X	X	X	X	DSL	NOP-> Bank active after t_{WR}	
	L	H	H	H	X	NOP	NOP-> Bank active after t_{WR}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write Recovering with Auto-precharge	H	X	X	X	X	DSL	NOP-> Precharge after t_{WR}	
	L	H	H	H	X	NOP	NOP-> Precharge after t_{WR}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Refreshing	H	X	X	X	X	DSL	NOP-> Idle after t_{RC}	
	L	H	H	H	X	NOP	NOP-> Idle after t_{RC}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	DSL	NOP-> Idle after t_{MRD}	
	L	H	H	H	X	NOP	NOP-> Idle after t_{MRD}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

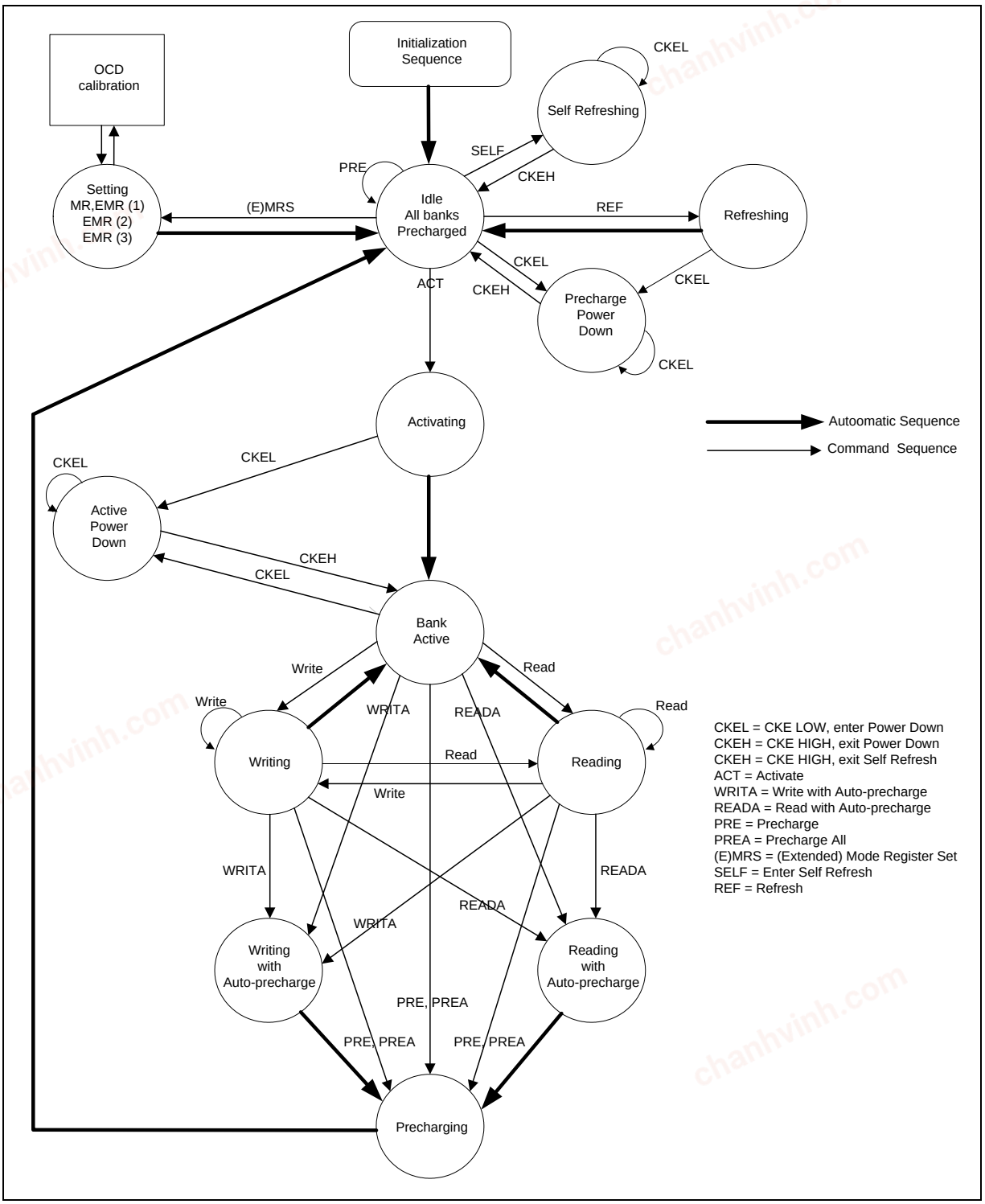
Notes:

1. This command may be issued for other banks, depending on the state of the banks.
2. All banks must be in “IDLE”.
3. Read or Write burst interruption is prohibited for burst length of 4 and only allowed for burst length of 8. Burst read/write can only be interrupted by another read/write with 4 bit burst boundary. Any other case of read/write interrupt is not allowed.

Remark: H = High level, L = Low level, X = High or Low level (Don’t Care), V = Valid data.

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9.5 Simplified Stated Diagram



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10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT	NOTES
Voltage on VDD pin relative to VSS	VDD	-1.0 ~ 2.3	V	1, 2
Voltage on VDDQ pin relative to VSS	VDDQ	-0.5 ~ 2.3	V	1, 2
Voltage on VDDL pin relative to VSS	VDDL	-0.5 ~ 2.3	V	1, 2
Voltage on any pin relative to VSS	VIN, VOUT	-0.5 ~ 2.3	V	1, 2
Storage Temperature	TSTG	-55 ~ 150	°C	1, 3

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. When VDD and VDDQ and VDDL are less than 500mV; VREF may be equal to or less than 300mV.
3. Storage temperature is the case surface temperature on the center/top side of the DRAM.

10.2 Operating Temperature Condition

PARAMETER	SYM.	MIN.	MAX.	UNIT	NOTES
Commercial Operating Temperature Range (for -18/-25/-3)	TCASE	0	85	°C	1, 2, 3
Industrial Operating Temperature Range (for 18I/25I)	TCASE	-40	95	°C	1, 2, 3, 4
Industrial Plus Operating Temperature Range (for 18J/25J)	TCASE	-40	105	°C	1, 2, 3, 4

Notes:

1. Operating case temperature is the case surface temperature on the center/top side of the DRAM.
2. Supporting 0°C ≤ TCASE ≤ 85°C with full JEDEC AC and DC specifications.
3. Supporting 0°C ≤ TCASE ≤ 85°C and being able to extend to 95°C or 105°C with doubling Auto Refresh commands in frequency to a 32 mS period (tREFI = 3.9 µS) and to enter to Self Refresh mode at this high temperature range via A7 “1” on EMR (2).
4. During operation, the DRAM case temperature must be maintained between -40°C ≤ TCASE ≤ 95°C for Industrial grade parts or -40°C ≤ TCASE ≤ 105°C for Industrial plus grade parts under all specification parameters.
5. All parts list in ordering information table (section 3) will not guarantee to meet functional and AC specification if the operation temperature range out of range mentioned in above table.

10.3 Recommended DC Operating Conditions

SYM.	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	2, 3
VTT	Termination Voltage (System)	VREF - 0.04	VREF	VREF + 0.04	V	4

Notes:

1. There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must than or equal to VDD.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak AC noise on VREF may not exceed ± 2 % VREF(dc).
4. VTT of transmitting device must track VREF of receiving device.
5. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together.
6. All parts list in ordering information table (section 3) will not guarantee to meet functional and AC specification if the DC operation conditions out of range mentioned in above table.

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10.4 ODT DC Electrical Characteristics

PARAMETER/CONDITION	SYM.	MIN.	NOM.	MAX.	UNIT	NOTES
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 Ω	Rtt2(eff)	120	150	180	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,1; 50 Ω	Rtt3(eff)	40	50	60	Ω	1, 2
Deviation of V_M with respect to $V_{DDQ}/2$	ΔV_M	-6		+6	%	1

Notes:

1. Test condition for Rtt measurements.
2. Optional for DDR2-667, mandatory for DDR2-800 and DDR2-1066.

Measurement Definition for Rtt(eff):

Apply $V_{IH\ (ac)}$ and $V_{IL\ (ac)}$ to test pin separately, then measure current $I(V_{IH\ (ac)})$ and $I(V_{IL\ (ac)})$ respectively. $V_{IH\ (ac)}$, $V_{IL\ (ac)}$, and V_{DDQ} values defined in SSTL_18.

$$Rtt(eff) = (V_{IH(ac)} – V_{IL(ac)}) /(I(V_{IHac}) – I(V_{ILac}))$$

Measurement Definition for ΔV_M:

Measure voltage (V_M) at test pin (midpoint) with no load.

$$\Delta V_M = ((2 \times V_m / V_{DDQ}) – 1) \times 100\%$$

10.5 Input DC Logic Level

PARAMETER	SYM.	MIN.	MAX.	UNIT
DC input logic HIGH	$V_{IH(dc)}$	V_{REF} + 0.125	V_{DDQ} + 0.3	V
DC input logic LOW	$V_{IL(dc)}$	-0.3	V_{REF} - 0.125	V

10.6 Input AC Logic Level

PARAMETER	SYM.	-18/18I/18J		-25/25I/25J/-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
AC input logic HIGH	$V_{IH\ (ac)}$	V_{REF} + 0.200	–	V_{REF} + 0.200	V_{DDQ} + V_{PEAK}[1]	V
AC input logic LOW	$V_{IL\ (ac)}$	–	V_{REF} - 0.200	V_{SSQ} - V_{PEAK}[1]	V_{REF} - 0.200	V

Note:

1. Refer to the page 67 sections 10.14.1 and 10.14.2 AC Overshoot/Undershoot specification table for V_{PEAK} value: maximum peak amplitude allowed for Overshoot/Undershoot.

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10.7 Capacitance

SYM.	PARAMETER	MIN.	MAX.	UNIT
C_{CK}	Input Capacitance , CLK and $\overline{CLK}$	1.0	1.5	pF
C_{DCK}	Input Capacitance delta , CLK and $\overline{CLK}$	–	0.25	pF
C_I	input Capacitance, all other input-only pins	1.0	1.75	pF
C_{DI}	Input Capacitance delta, all other input-only pins	–	0.25	pF
C_{IO}	Input/output Capacitance, DQ, LDM, UDM, LDQS, $\overline{LDQS}$, UDQS, $\overline{UDQS}$	2.5	3.5	pF
C_{DIO}	Input/output Capacitance delta, DQ, LDM, UDM, LDQS, $\overline{LDQS}$, UDQS, $\overline{UDQS}$	–	0.5	pF

10.8 Leakage and Output Buffer Characteristics

SYM.	PARAMETER	MIN.	MAX.	UNIT	NOTES
I_{IL}	Input Leakage Current ($0V \le V_{IN} \le V_{DD}$)	-2	2	µA	1
I_{OL}	Output Leakage Current (Output disabled, $0V \le V_{OUT} \le V_{DDQ}$)	-5	5	µA	2
V_{OTR}	Output Timing Measurement Reference Level	0.5 x VDDQ	–	V	3
$I_{OH(dc)}$	Output Minimum Source DC Current	-13.4	–	mA	4, 6
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	–	mA	5, 6

Notes:

1. All other pins not under test = 0 V.
2. DQ, LDQS, $\overline{LDQS}$, UDQS, $\overline{UDQS}$ are disabled and ODT is turned off.
3. The V_{DDQ} of the device under test is referenced.
4. V_{DDQ} = 1.7 V; V_{OUT} = 1.42 V. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 0.28V.
5. V_{DDQ} = 1.7 V; V_{OUT} = 0.28V. V_{OUT}/I_{OL} must be less than 21 Ω for values of V_{OUT} between 0 V and 0.28V.
6. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 4 and 5. They are used to test drive current capability to ensure V_{IH}min plus a noise margin and V_{IL}max minus a noise margin are delivered to an SSTL_18 receiver.

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10.9 DC Characteristics

SYM.	CONDITIONS		-18/18I/18J	-25/25I/25J	-3	UNIT	NOTES
			MAX.	MAX.	MAX.		
I_{DD0}	**Operating Current - One Bank Active-Precharge** $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address and control inputs are SWITCHING; Databus inputs are SWITCHING.		60	55	50	mA	1,2,3,4,5,6
I_{DD1}	**Operating Current - One Bank Active-Read-Precharge** I_{OUT} = 0 mA; BL = 4, CL = $CL_{(IDD)}$, AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address and control inputs are SWITCHING; Data bus inputs are SWITCHING.		70	65	60	mA	1,2,3,4,5,6
I_{DD2P}	**Precharge Power-Down Current** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address inputs are STABLE; Data Bus inputs are FLOATING. ($T_{CASE} \leq 85°C$)		8	8	8	mA	1,2,3,4,5,6, 7
I_{DD2N}	**Precharge Standby Current** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		40	35	32	mA	1,2,3,4,5,6
I_{DD2Q}	**Precharge Quiet Standby Current** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address inputs are STABLE; Data bus inputs are FLOATING.		35	33	30	mA	1,2,3,4,5,6
I_{DD3PF}	**Active Power-Down Current** All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address inputs are STABLE; Data bus inputs are FLOATING. ($T_{CASE} \leq 85°C$)	Fast PDN Exit MRS(12) = 0	30	30	30	mA	1,2,3,4,5,6
I_{DD3PS}		Slow PDN Exit MRS(12) = 1	17	17	17	mA	1,2,3,4,5,6, 7
I_{DD3N}	**Active Standby Current** All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		50	47	45	mA	1,2,3,4,5,6

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IDD4R	**Operating Burst Read Current** All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address inputs are SWITCHING; Data Bus inputs are SWITCHING.	110	105	100	mA	1,2,3,4,5,6
IDD4W	**Operating Burst Write Current** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address inputs are SWITCHING; Data Bus inputs are SWITCHING.	120	110	100	mA	1,2,3,4,5,6
IDD5B	**Burst Refresh Current** tCK = tCK(IDD); Refresh command every tRFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.	85	80	75	mA	1,2,3,4,5,6
IDD6	**Self Refresh Current** CKE ≤ 0.2 V, external clock off, CLK and $\overline{CLK}$ at 0 V; Other control and address inputs are FLOATING; Data bus inputs are FLOATING. (TCASE ≤ 85°C)	8	8	8	mA	1,2,3,4,5,6, 7
IDD7	**Operating Bank Interleave Read Current** All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = tRCD(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during deselects; Data Bus inputs are SWITCHING.	150	140	130	mA	1,2,3,4,5,6

Notes:

1. VDD = 1.8 V ± 0.1V; VDDQ = 1.8 V ± 0.1V.
2. IDD specifications are tested after the device is properly initialized.
3. Input slew rate is specified by AC Parametric Test Condition.
4. IDD parameters are specified with ODT disabled.
5. Data Bus consists of DQ, LDM, UDM, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
6. Definitions for IDD
   - LOW = Vin ≤ VIL (ac) (max)
   - HIGH = Vin ≥ VIH (ac) (min)
   - STABLE = inputs stable at a HIGH or LOW level
   - FLOATING = inputs at VREF = VDDQ/2
   - SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.
7. The following IDD values must be derated (IDD limits increase), when TCASE ≥ 85°C IDD2P must be derated by 20%; IDD3P(slow) must be derated by 30% and IDD6 must be derated by 80%. (IDD6 will increase by this amount if TCASE < 85°C and the 2X refresh option is still enabled)

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10.10 IDD Measurement Test Parameters

SPEED GRADE	DDR2-1066 (-18/18I/18J)	DDR2-800 (-25/25I/25J)	DDR2-667 (-3)	UNIT
Bin(CL-tRCD-tRP)	**6-6-6**	**5-5-5/6-6-6**	**5-5-5**	
CL(IDD)	6	5/6	5	tCK
tCK(IDD)	1.875	2.5	3	nS
tRCD(IDD)	11.25	12.5	15	nS
tRP(IDD)	11.25	12.5	15	nS
tRC(IDD)	51.25	52.5	55	nS
tRASmin(IDD)	40	40	40	nS
tRASmax(IDD)	70000	70000	70000	nS
tRRD(IDD)-2KB	10	10	10	nS
tFAW(IDD)-2KB	45	45	50	nS
tRFC(IDD)	127.5	127.5	127.5	nS

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10.11 AC Characteristics

10.11.1 AC Characteristics and Operating Condition for -18/18I/18J speed grade

Notes: 1-3 and 45-47 apply to the entire table

SYM.	SPEED GRADE		DDR2-1066 (-18/18I/18J)		UNIT[25]	NOTES
	Bin(CL-tRCD-tRP)		6-6-6			
	PARAMETER		MIN.	MAX.		
tRCD	Active to Read/Write Command Delay Time		11.25	–	nS	23
tRP	Precharge to Active Command Period		11.25	–	nS	23
tRC	Active to Ref/Active Command Period		51.25	–	nS	23
tRAS	Active to Precharge Command Period		40	70000	nS	4,23
tRFC	Auto Refresh to Active/Auto Refresh command period		127.5	–	nS	5
tREFI	Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C*	–	7.8	µS	5
		0°C ≤ TCASE ≤ 85°C	–	7.8	µS	5
		85°C < TCASE ≤ 95°C	–	3.9	µS	5,6
		95°C < TCASE ≤ 105°C*	–	3.9	µS	5,6
tCCD	$\overline{CAS}$ to $\overline{CAS}$ command delay		2	–	nCK	
tCK(avg)	Average clock period	tCK(avg) @ CL=4	3	7.5	nS	30,31
		tCK(avg) @ CL=5	2.5	7.5	nS	30,31
		tCK(avg) @ CL=6	1.875	7.5	nS	30,31
		tCK(avg) @ CL=7	1.875	7.5	nS	30,31
tCH(avg)	Average clock high pulse width		0.45	0.55	tCK(avg)	30,31
tCL(avg)	Average clock low pulse width		0.45	0.55	tCK(avg)	30,31
tAC	DQ output access time from CLK/ $\overline{CLK}$		-350	350	pS	35
tDQSCK	DQS output access time from CLK / $\overline{CLK}$		-325	325	pS	35
tDQSQ	DQS-DQ skew for DQS & associated DQ signals		–	175	pS	13
tCKE	CKE minimum high and low pulse width		3	–	nCK	7
tRRD	Active to active command period for 2KB page size		10	–	nS	8,23
tFAW	Four Activate Window for 2KB page size		45		nS	23
tWR	Write recovery time		15	–	nS	23
tDAL	Auto-precharge write recovery + precharge time		WR + tnRP	–	nCK	24
tWTR	Internal Write to Read command delay		7.5	–	nS	9,23
tRTP	Internal Read to Precharge command delay		7.5	–	nS	4,23
tIS (base)	Address and control input setup time		125	–	pS	10,26, 40,42,43
tIH (base)	Address and control input hold time		200	–	pS	11,26, 40,42,43
tIS (ref)	Address and control input setup time		325	–	pS	10,26, 40,42,43
tIH (ref)	Address and control input hold time		325	–	pS	11,26, 40,42,43
tIPW	Address and control input pulse width for each input		0.6	–	tCK(avg)	
tDQSS	DQS latching rising transitions to associated clock edges		-0.25	0.25	tCK(avg)	28
tDSS	DQS falling edge to CLK setup time		0.2	–	tCK(avg)	28
tDSH	DQS falling edge hold time from CLK		0.2	–	tCK(avg)	28
tDQSH	DQS input high pulse width		0.35	–	tCK(avg)	
tDQSL	DQS input low pulse width		0.35	–	tCK(avg)	

* -40°C ≤ TCASE ≤ 85°C is for 18I and 18J grade parts only. 95°C < TCASE ≤ 105°C is for 18J grade parts only.

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AC Characteristics and Operating Condition for -18/18I/18J speed grade, continued

Notes: 1-3 and 45-47 apply to the entire table

SYM.	SPEED GRADE	DDR2-1066 (-18/18I/18J)		UNITS[25]	NOTES
	Bin(CL-tRCD-tRP)	6-6-6			
	PARAMETER	MIN.	MAX.		
tWPRE	Write preamble	0.35	–	tCK(avg)	
tWPST	Write postamble	0.4	0.6	tCK(avg)	12
tRPRE	Read preamble	0.9	1.1	tCK(avg)	14,36
tRPST	Read postamble	0.4	0.6	tCK(avg)	14,37
tDS(base)	DQ and DM input setup time	0	–	pS	16,27,29, 41,42,44
tDH(base)	DQ and DM input hold time	75	–	pS	17,27,29, 41,42,44
tDS(ref)	DQ and DM input setup time	200	–	pS	16,27,29, 41,42,44
tDH(ref)	DQ and DM input hold time	200	–	pS	17,27,29, 41,42,44
tDIPW	DQ and DM input pulse width for each input	0.35	–	tCK(avg)	
tHZ	Data-out high-impedance time from CLK/ $\overline{CLK}$	–	tAC,max	pS	15,35
tLZ(DQS)	DQS/ $\overline{DQS}$ -low-impedance time from CLK/ $\overline{CLK}$	tAC,min	tAC,max	pS	15,35
tLZ(DQ)	DQ low-impedance time from CLK/ $\overline{CLK}$	2 x tAC,min	tAC,max	pS	15,35
tHP	Clock half pulse width	Min. (tCH(abs), tCL(abs))	–	pS	32
tQHS	Data hold skew factor	–	250	pS	33
tQH	DQ/DQS output hold time from DQS	tHP - tQHS	–	pS	34
tXSNR	Exit Self Refresh to a non-Read command	tRFC + 10	–	nS	23
tXSRD	Exit Self Refresh to a Read command	200	–	nCK	
tXP	Exit precharge power down to any command	3	–	nCK	
tXARD	Exit active power down to Read command	3	–	nCK	18
tXARDS	Exit active power down to Read command (slow exit, lower power)	10 - AL	–	nCK	18,19
tAOND	ODT turn-on delay	2	2	nCK	20
tAON	ODT turn-on	tAC,min	tAC,max + 2.575	nS	20,35
tAONPD	ODT turn-on (Power Down mode)	tAC,min + 2	3 x tCK(avg) + tAC,max+1	nS	
tAOFD	ODT turn-off delay	2.5	2.5	nCK	21,39
tAOF	ODT turn-off	tAC,min	tAC,max + 0.6	nS	21,38,39
tAOFPD	ODT turn-off (Power Down mode)	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	nS	
tANPD	ODT to power down Entry Latency	4	–	nCK	
tAXPD	ODT Power Down Exit Latency	11		nCK	
tMRD	Mode Register Set command cycle time	2	–	nCK	
tMOD	MRS command to ODT update delay	0	12	nS	23
tOIT	OCD Drive mode output delay	0	12	nS	23
tDELAY	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS+tCK(avg)+tIH	–	nS	22

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10.11.2 AC Characteristics and Operating Condition for -25/25I/25J/-3 speed grades

Notes: 1-3 and 45-47 apply to the entire table

SYM.	SPEED GRADE		DDR2-800 (-25/25I/25J)		DDR2-667 (-3)		UNITS[25]	NOTES
	Bin(CL-tRCD-tRP)		5-5-5/6-6-6		5-5-5			
	PARAMETER		MIN.	MAX.	MIN.	MAX.		
tRCD	Active to Read/Write Command Delay Time		12.5	–	15	–	nS	23
tRP	Precharge to Active Command Period		12.5	–	15	–	nS	23
tRC	Active to Ref/Active Command Period		52.5	–	55	–	nS	23
tRAS	Active to Precharge Command Period		40	70000	40	70000	nS	4,23
tRFC	Auto Refresh to Active/Auto Refresh command period		127.5	–	127.5	–	nS	5
tREFI	Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C*	–	7.8	–	–	µS	5
		0°C ≤ TCASE ≤ 85°C	–	7.8	–	7.8	µS	5
		85°C < TCASE ≤ 95°C	–	3.9	–	3.9	µS	5,6
		95°C < TCASE ≤ 105°C*	–	3.9	–	–	µS	5,6
tCCD	$\overline{CAS}$ to $\overline{CAS}$ command delay		2	–	2	–	nCK	
tCK(avg)	Average clock period	tCK(avg) @ CL=3	5	8	5	8	nS	30,31
		tCK(avg) @ CL=4	3.75	8	3.75	8	nS	30,31
		tCK(avg) @ CL=5	2.5	8	3	8	nS	30,31
		tCK(avg) @ CL=6	2.5	8	–	–	nS	30,31
tCH(avg)	Average clock high pulse width		0.45	0.55	0.45	0.55	tCK(avg)	30,31
tCL(avg)	Average clock low pulse width		0.45	0.55	0.45	0.55	tCK(avg)	30,31
tAC	DQ output access time from CLK/ $\overline{CLK}$		-400	400	-450	450	pS	35
tDQSCK	DQS output access time from CLK / $\overline{CLK}$		-350	350	-400	400	pS	35
tDQSQ	DQS-DQ skew for DQS & associated DQ signals		–	200	–	240	pS	13
tCKE	CKE minimum high and low pulse width		3	–	3	–	nCK	7
tRRD	Active to active command period for 2KB page size		10	–	10	–	nS	8,23
tFAW	Four Activate Window for 2KB page size		45	–	50	–	nS	23
tWR	Write recovery time		15	–	15	–	nS	23
tDAL	Auto-precharge write recovery + precharge time		WR + tnRP	–	WR + tnRP	–	nCK	24
tWTR	Internal Write to Read command delay		7.5	–	7.5	–	nS	9,23
tRTP	Internal Read to Precharge command delay		7.5	–	7.5	–	nS	4,23
tIS (base)	Address and control input setup time		175	–	200	–	pS	10,26, 40,42,43
tIH (base)	Address and control input hold time		250	–	275	–	pS	11,26, 40,42,43
tIS (ref)	Address and control input setup time		375	–	400	–	pS	10,26, 40,42,43
tIH (ref)	Address and control input hold time		375	–	400	–	pS	11,26, 40,42,43
tIPW	Address and control input pulse width for each input		0.6	–	0.6	–	tCK(avg)	
tDQSS	DQS latching rising transitions to associated clock edges		-0.25	0.25	-0.25	0.25	tCK(avg)	28
tDSS	DQS falling edge to CLK setup time		0.2	–	0.2	–	tCK(avg)	28
tDSH	DQS falling edge hold time from CLK		0.2	–	0.2	–	tCK(avg)	28
tDQSH	DQS input high pulse width		0.35	–	0.35	–	tCK(avg)	
tDQSL	DQS input low pulse width		0.35	–	0.35	–	tCK(avg)	

* -40°C ≤ TCASE ≤ 85°C is for 25I and 25J grade parts only. 95°C < TCASE ≤ 105°C is for 25J grade parts only.

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AC Characteristics and Operating Condition for -25/25I/25J/-3 speed grades, continued

Notes: 1-3 and 45-47 apply to the entire table

SYM.	SPEED GRADE	DDR2-800 (-25/25I/25J)		DDR2-667 (-3)		UNITS[25]	NOTES
	Bin(CL-tRCD-tRP)	5-5-5/6-6-6		5-5-5			
	PARAMETER	MIN.	MAX.	MIN.	MAX.		
tWPRE	Write preamble	0.35	–	0.35	–	tCK(avg)	
tWPST	Write postamble	0.4	0.6	0.4	0.6	tCK(avg)	12
tRPRE	Read preamble	0.9	1.1	0.9	1.1	tCK(avg)	14,36
tRPST	Read postamble	0.4	0.6	0.4	0.6	tCK(avg)	14,37
tDS(base)	DQ and DM input setup time	50	–	100	–	pS	16,27,29, 41,42,44
tDH(base)	DQ and DM input hold time	125	–	175	–	pS	17,27,29, 41,42,44
tDS(ref)	DQ and DM input setup time	250	–	300	–	pS	16,27,29, 41,42,44
tDH(ref)	DQ and DM input hold time	250	–	300	–	pS	17,27,29, 41,42,44
tDIPW	DQ and DM input pulse width for each input	0.35	–	0.35	–	tCK(avg)	
tHZ	Data-out high-impedance time from CLK/ $\overline{\text{CLK}}$	–	tAC,max	–	tAC,max	pS	15,35
tLZ(DQS)	DQS/ $\overline{\text{DQS}}$ -low-impedance time from CLK/ $\overline{\text{CLK}}$	tAC,min	tAC,max	tAC,min	tAC,max	pS	15,35
tLZ(DQ)	DQ low-impedance time from CLK/ $\overline{\text{CLK}}$	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	pS	15,35
tHP	Clock half pulse width	Min. (tCH(abs), tCL(abs))		Min. (tCH(abs), tCL(abs))		pS	32
tQHS	Data hold skew factor	–	300	–	340	pS	33
tQH	DQ/DQS output hold time from DQS	tHP - tQHS	–	tHP - tQHS	–	pS	34
tXSNR	Exit Self Refresh to a non-Read command	tRFC + 10	–	tRFC + 10	–	nS	23
tXSRD	Exit Self Refresh to a Read command	200	–	200	–	nCK	
tXP	Exit precharge power down to any command	2	–	2	–	nCK	
tXARD	Exit active power down to Read command	2	–	2	–	nCK	18
tXARDS	Exit active power down to Read command (slow exit, lower power)	8 - AL	–	7 - AL	–	nCK	18,19
tAOND	ODT turn-on delay	2	2	2	2	nCK	20
tAON	ODT turn-on	tAC,min	tAC,max + 0.7	tAC,min	tAC,max + 0.7	nS	20,35
tAONPD	ODT turn-on (Power Down mode)	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	nS	
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	nCK	21,39
tAOF	ODT turn-off	tAC,min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	nS	21,38,39
tAOFPD	ODT turn-off (Power Down mode)	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	nS	
tANPD	ODT to power down Entry Latency	3	–	3	–	nCK	
tAXPD	ODT Power Down Exit Latency	8		8		nCK	
tMRD	Mode Register Set command cycle time	2	–	2	–	nCK	
tMOD	MRS command to ODT update delay	0	12	0	12	nS	23
tOIT	OCD Drive mode output delay	0	12	0	12	nS	23
tDELAY	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS+tCK(avg)+ tIH	–	tIS+tCK(avg)+ tIH	–	nS	22

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Notes:

1. All voltages are referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.
3. AC timing reference load:

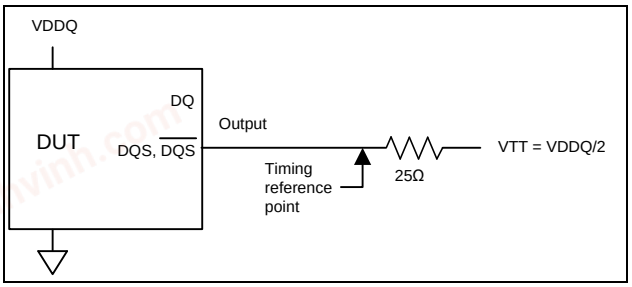


Figure 16 – AC timing reference load

4. This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min) have been satisfied.
5. If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
6. This is an optional feature. For detailed information, please refer to **"Operating Temperature Condition"** section 10.2 in this data sheet.
7. tCKE min of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.
8. A minimum of two clocks (2 * nCK) is required irrespective of operating frequency.
9. tWTR is at least two clocks (2 * nCK) independent of operation frequency.
10. There are two sets of values listed for Command/Address input setup time: tIS(base) and tIS(ref). The tIS(ref) value (for reference only) is equivalent to the baseline value of tIS(base) at VREF when the slew rate is 1.0 V/nS. The baseline value tIS(base) is the JEDEC defined value, referenced from the input signal crossing at the VIH(ac) level for a rising signal and VIL(ac) for a falling signal applied to the device under test. See Figure 17. If the Command/Address slew rate is not equal to 1.0 V/nS, then the baseline values must be derated by adding the values from table of tIS/tIH derating values for DDR2-667, DDR2-800 and DDR2-1066 (page 55).

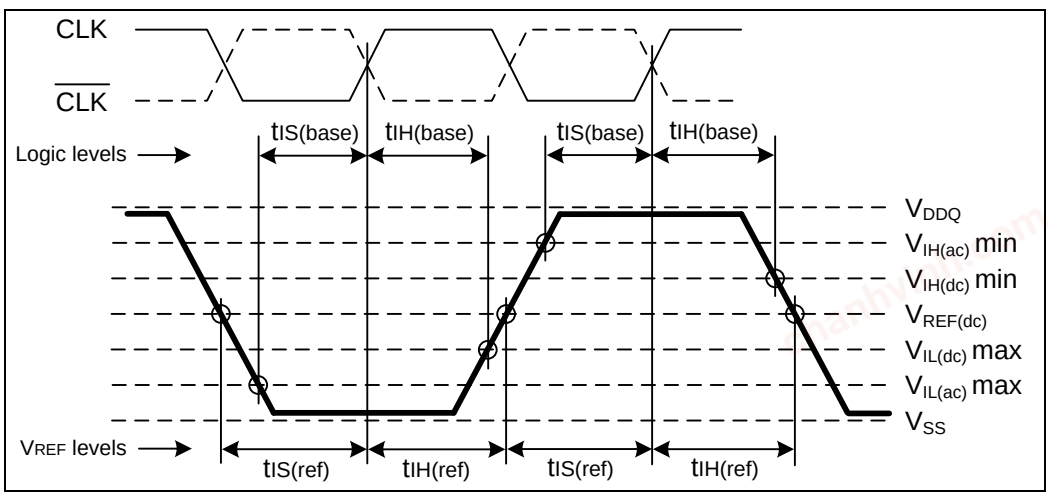


Figure 17 – Differential input waveform timing – tIS and tIH

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11. There are two sets of values listed for Command/Address input hold time: tIH(base) and tIH(ref). The tIH(ref) value (for reference only) is equivalent to the baseline value of tIH(base) at VREF when the slew rate is 1.0 V/nS. The baseline value tIH(base) is the JEDEC defined value, referenced from the input signal crossing at the VIL(dc) level for a rising signal and VIH(dc) for a falling signal applied to the device under test. See Figure 17. If the Command/Address slew rate is not equal to 1.0 V/nS, then the baseline values must be derated by adding the values from table tIS/tIH derating values for DDR2-667, DDR2-800 and DDR2-1066 (page 55).

12. The maximum limit for the tWPST parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrades accordingly.

13. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mismatch between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.

14. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Figure 18 shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

15. tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ). Figure 18 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQ's and tLZ(DQS) refers to tLZ of the (UDQS, LDQS, $\overline{\text{UDQS}}$ and $\overline{\text{LDQS}}$) each treated as single-ended signal.

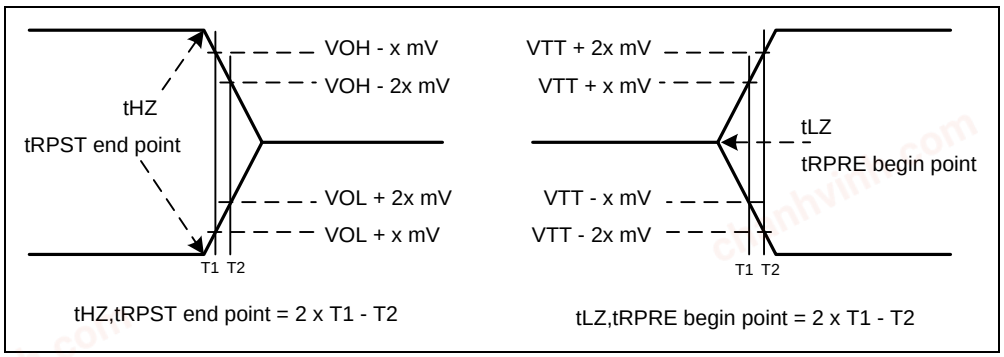


Figure 18 – Method for calculating transitions and endpoints

16. Input waveform timing tDS with differential data strobe enabled MR[bit10]=0. There are two sets of values listed for DQ and DM input setup time: tDS(base) and tDS(ref). The tDS(ref) value (for reference only) is equivalent to the baseline value tDS(base) at VREF when the slew rate is 2.0 V/nS, differentially. The baseline value tDS(base) is the JEDEC defined value, referenced from the input signal crossing at the VIH(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the VIL(ac) level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, $\overline{\text{DQS}}$ signals must be monotonic between VIL(dc)max and VIH(dc)min. See Figure 19. If the differential DQS slew rate is not equal to 2.0 V/nS, then the baseline values must be derated by adding the values from table of DDR2-667, DDR2-800 and DDR2-1066 tDS/tDH derating with differential data strobe (page 60).

17. Input waveform timing tDH with differential data strobe enabled MR[bit10]=0. There are two sets of values listed for DQ and DM input hold time: tDH(base) and tDH(ref). The tDH(ref) value (for reference only) is equivalent to the baseline value tDH(base) at VREF when the slew rate is 2.0 V/nS, differentially. The baseline value tDH(base) is the JEDEC defined value, referenced from the differential data strobe crosspoint to the input signal crossing at the VIH(dc) level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the VIL(dc) level for a rising signal applied to the device under test. DQS, $\overline{\text{DQS}}$ signals must be monotonic between VIL(dc)max and VIH(dc)min. See Figure 19. If the differential DQS slew rate is not equal to 2.0 V/nS, then the baseline values must be derated by adding the values from table of DDR2-667, DDR2-800 and DDR2-1066 tDS/tDH derating with differential data strobe (page 60).

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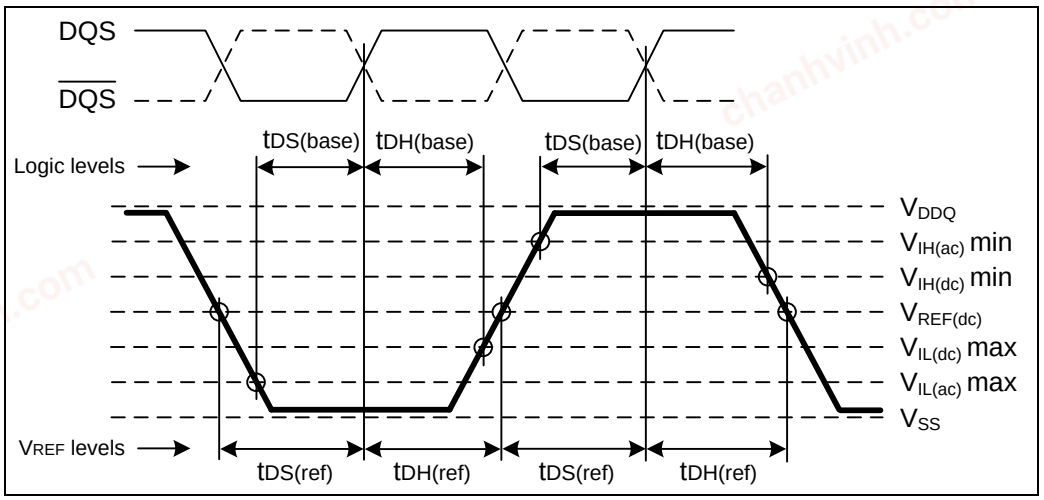


Figure 19 – Differential input waveform timing – tDS and tDH

18. User can choose which active power down exit timing to use via MRS (bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing.

19. AL = Additive Latency.

20. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from tAOND, which is interpreted differently per speed bin. For DDR2-667/800/1066, tAOND is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

21. ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD, which is interpreted as 0.5 x tCK(avg) [nS] after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

    For DDR2-667/800: If tCK(avg) = 3 nS is assumed, tAOFD is 1.5 nS (= 0.5 x 3 nS) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

    For DDR2-1066: tAOFD is 0.9375 [nS] (= 0.5 x 1.875 [nS]) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

22. The clock frequency is allowed to change during Self Refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in section 8.10.

23. For these parameters, the DDR2 SDRAM device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.

    Examples:

    The device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means:

    For DDR2-667 5-5-5, of which tRP = 15nS, the device will support tnRP = RU{tRP / tCK(avg)} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm+5 is valid even if (Tm+5 - Tm) is less than 15nS due to input clock jitter.

    For DDR2-1066 6-6-6, of which tRP = 11.25 nS, the device will support tnRP = RU{tRP / tCK(avg)} = 6, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 11.25 nS due to input clock jitter.

24. tDAL [nCK] = WR [nCK] + tnRP [nCK] = WR + RU {tRP [pS] / tCK(avg) [pS] }, where WR is the value programmed in the mode register set and RU stands for round up.

    Example:

    For DDR2-1066 6-6-6 at tCK(avg) = 1.875 nS with WR programmed to 8 nCK, tDAL = 8 + RU{11.25 nS / 1.875 nS} [nCK] = 8 + 6 [nCK] = 14 [nCK].

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25. New units, 'tCK(avg)' and 'nCK', are introduced in DDR2-667, DDR2-800 and DDR2-1066.

    Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation.

    Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

    Examples:

    For DDR2-667/800: tXP = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+2, even if (Tm+2 - Tm) is 2 x tCK(avg) + tERR(2per),min.

    For DDR2-1066: tXP = 3 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+3, even if (Tm+3 - Tm) is 3 x tCK(avg) + tERR(3per),min.

26. These parameters are measured from a command/address signal (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CLK/ $\overline{CLK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

27. If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

28. These parameters are measured from a data strobe signal ((L/U)DQS/ $\overline{DQS}$) crossing to its respective clock signal (CLK/ $\overline{CLK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

29. These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U)DQS/ $\overline{DQS}$) crossing.

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30. Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters'. The jitter specified is a random jitter meeting a Gaussian distribution.

Input clock-Jitter specifications parameters for DDR2-667, DDR2-800 and DDR2-1066

PARAMETER	SYMBOL	DDR2-667		DDR2-800		DDR2-1066		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Clock period jitter	tJIT(per)	-125	125	-100	100	-90	90	pS
Clock period jitter during DLL locking period	tJIT(per,lck)	-100	100	-80	80	-80	80	pS
Cycle to cycle clock period	tJIT(cc)	-250	250	-200	200	-180	180	pS
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-200	200	-160	160	-160	160	pS
Cumulative error across 2 cycles	tERR(2per)	-175	175	-150	150	-132	132	pS
Cumulative error across 3 cycles	tERR(3per)	-225	225	-175	175	-157	157	pS
Cumulative error across 4 cycles	tERR(4per)	-250	250	-200	200	-175	175	pS
Cumulative error across 5 cycles	tERR(5per)	-250	250	-200	200	-188	188	pS
Cumulative error across n cycles, n = 6 ... 10, inclusive	tERR(6-10per)	-350	350	-300	300	-250	250	pS
Cumulative error across n cycles, n = 11 ... 50, inclusive	tERR(11-50per)	-450	450	-450	450	-425	425	pS
Duty cycle jitter	tJIT(duty)	-125	125	-100	100	-75	75	pS

Definitions:

- tCK(avg)

  tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window.

$$tCK(avg) = \left[\sum_{j=1}^{N} tCK_j\right] / N$$

$$where \qquad N = 200$$

- tCH(avg) and tCL(avg)

  tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.

$$tCH(avg) = \left[\sum_{j=1}^{N} tCH_j\right] / (N \times tCK(avg))$$

$$where \qquad N = 200$$

  tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

$$tCL(avg) = \left[\sum_{j=1}^{N} tCL_j\right] / (N \times tCK(avg))$$

$$where \qquad N = 200$$

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- tJIT(duty)

  tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).

  tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)}

  where,

  tJIT(CH) = {tCHi- tCH(avg) where i=1 to 200}

  tJIT(CL) = {tCLi- tCL(avg) where i=1 to 200}

- tJIT(per), tJIT(per,lck)

  tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).

  tJIT(per) = Min/max of {tCKi- tCK(avg) where i=1 to 200}

  tJIT(per) defines the single period jitter when the DLL is already locked.

  tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

  tJIT(per) and tJIT(per,lck) are not guaranteed through final production testing.

- tJIT(cc), tJIT(cc,lck)

  tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles:

  tJIT(cc) = Max of |tCKi+1 – tCKi|

  tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

  tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

  tJIT(cc) and tJIT(cc,lck) are not guaranteed through final production testing.

- tERR(2per), tERR (3per), tERR (4per), tERR (5per), tERR (6-10per) and tERR (11-50per)

  tERR is defined as the cumulative error across multiple consecutive cycles from tCK(avg).

$$tERR(nper) = \left[\sum_{j=1}^{i+n-1} tCK_j \right] - n \times tCK(avg)$$

$$Where \begin{cases} n = 2 & for \quad tERR(2per) \\ n = 3 & for \quad tERR(3per) \\ n = 4 & for \quad tERR(4per) \\ n = 5 & for \quad tERR(5per) \\ 6 \le n \le 10 & for \quad tERR(6-10per) \\ 11 \le n \le 50 & for \quad tERR(11-50per) \end{cases}$$

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31. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in the table below.)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Absolute clock period	tCK(abs)	tCK(avg),min + tJIT(per),min	tCK(avg),max + tJIT(per),max	pS
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min x tCK(avg),min + tJIT(duty),min	tCH(avg),max x tCK(avg),max + tJIT(duty),max	pS
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min x tCK(avg),min + tJIT(duty),min	tCL(avg),max x tCK(avg),max + tJIT(duty),max	pS

Examples: 1) For DDR2-667, tCH(abs),min = (0.45 x 3000 pS) - 125 pS = 1225 pS

2) For DDR2-1066, tCH(abs),min = (0.45 x 1875 pS) - 75 pS = 768.75 pS

32. tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH. The value to be used for tQH calculation is determined by the following equation;

    tHP = Min (tCH(abs), tCL(abs)),

    where,

    tCH(abs) is the minimum of the actual instantaneous clock HIGH time;

    tCL(abs) is the minimum of the actual instantaneous clock LOW time;

33. tQHS accounts for:

    1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and

    2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers

34. tQH = tHP – tQHS, where:

    tHP is the minimum of the absolute half period of the actual input clock; and

    tQHS is the specification value under the max column.

    {The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}

    Examples:

    1) If the system provides tHP of 1315 pS into a DDR2-667 SDRAM, the DRAM provides tQH of 975 pS minimum.

    2) If the system provides tHP of 1420 pS into a DDR2-667 SDRAM, the DRAM provides tQH of 1080 pS minimum.

    3) If the system provides tHP of 825 pS into a DDR2-1066 SDRAM, the DRAM provides tQH of 575 pS minimum.

    4) If the system provides tHP of 900 pS into a DDR2-1066 SDRAM, the DRAM provides tQH of 650 pS minimum.

35. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)

    Examples:

    1) If the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 pS and tERR(6-10per),max = + 293 pS, then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 400 pS - 293 pS = - 693 pS and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 400 pS + 272 pS = + 672 pS.

    Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ),min(derated) = - 900 pS - 293 pS = - 1193 pS and tLZ(DQ),max(derated) = 450 pS + 272 pS = + 722 pS. (Caution on the min/max usage!)

    2) If the measured jitter into a DDR2-1066 SDRAM has tERR(6-10per),min = - 202 pS and tERR(6-10per),max = + 223 pS, then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 300 pS - 223 pS = - 523 pS and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 300 pS + 202 pS = + 502 pS.

    Similarly, tLZ(DQ) for DDR2-1066 derates to tLZ(DQ),min(derated) = - 700 pS - 223 pS = - 923 pS and tLZ(DQ),max(derated) = 350 pS + 202 pS = + 552 pS. (Caution on the min/max usage!)

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36. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)

    Examples:

    1) If the measured jitter into a DDR2-667 SDRAM has tJIT(per),min = - 72 pS and tJIT(per),max = + 93 pS, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 pS = + 2178 pS and tRPRE,max(derated) = tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 93 pS = + 2843 pS. (Caution on the min/max usage!)

    2) If the measured jitter into a DDR2-1066 SDRAM has tJIT(per),min = - 72 pS and tJIT(per),max = + 63 pS, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 pS = + 1615.5 pS and tRPRE,max(derated) = tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 63 pS = + 2125.5 pS. (Caution on the min/max usage!)

37. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)

    Examples:

    1) If the measured jitter into a DDR2-800 SDRAM has tJIT(duty),min = - 72 pS and tJIT(duty),max = + 93 pS, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 pS = + 928 pS and tRPST,max(derated) = tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 93 pS = + 1593 pS. (Caution on the min/max usage!)

    2) If the measured jitter into a DDR2-1066 SDRAM has tJIT(duty),min = - 72 pS and tJIT(duty),max = + 63 pS, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 pS = + 678 pS and tRPST,max(derated) = tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 63 pS = + 1188 pS. (Caution on the min/max usage!)

38. When the device is operated with input clock jitter, this parameter needs to be derated by { -tJIT(duty),max - tERR(6-10per),max } and { - tJIT(duty),min - tERR(6-10per),min } of the actual input clock. (output deratings are relative to the SDRAM input clock.)

    Examples:

    1) If the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 pS, tERR(6-10per),max = + 293 pS, tJIT(duty),min = - 106 pS and tJIT(duty),max = + 94 pS, then tAOF,min(derated) = tAOF,min + { - tJIT(duty),max - tERR(6-10per),max } = - 450 pS + { - 94 pS - 293 pS} = - 837 pS and tAOF,max(derated) = tAOF,max + { - tJIT(duty),min - tERR(6-10per),min } = 1050 pS + { 106 pS + 272 pS } = + 1428 pS. (Caution on the min/max usage!)

    2) If the measured jitter into a DDR2-1066 SDRAM has tERR(6-10per),min = - 202 pS, tERR(6-10per),max = + 223 pS, tJIT(duty),min = - 66 pS and tJIT(duty),max = + 74 pS, then tAOF,min(derated) = tAOF,min + { - tJIT(duty),max - tERR(6-10per),max } = - 350 pS + { - 74 pS - 223 pS} = - 647 pS and tAOF,max(derated) = tAOF,max + { - tJIT(duty),min - tERR(6-10per),min } = 950 pS + { 66 pS + 202 pS } = + 1218 pS. (Caution on the min/max usage!)

39. For tAOFD of DDR2-667/800/1066, the 1/2 clock of nCK in the 2.5 x nCK assumes a tCH(avg), average input clock HIGH pulse width of 0.5 relative to tCK(avg). tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5.

    Example:

    If an input clock has a worst case tCH(avg) of 0.45, the tAOF,min should be derated by subtracting 0.02 x tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.55, the tAOF,max should be derated by adding 0.02 x tCK(avg) to it. Therefore, we have;

    tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH(avg),min)] x tCK(avg)

    tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH(avg),max) - 0.5] x tCK(avg)

    or

    tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH(avg),min] x tCK(avg))

    tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH(avg),max - 0.5] x tCK(avg))

    where tCH(avg),min and tCH(avg),max are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls.

Note that these deratings are in addition to the tAOF derating per input clock jitter, i.e. tJIT(duty) and tERR(6-10per). However tAC values used in the equations shown above are from the timing parameter table and are not derated.

Thus the final derated values for tAOF are;

tAOF,min(derated_final) = tAOF,min(derated) + { - tJIT(duty),max - tERR(6-10per),max }

tAOF,max(derated_final) = tAOF,max(derated) + { - tJIT(duty),min - tERR(6-10per),min }

40. Timings are specified with command/address input slew rate of 1.0 V/nS.

41. Timings are specified with DQs and DM input slew rate of 1.0V/nS.

42. Timings are specified with CLK/ $\overline{\text{CLK}}$ differential slew rate of 2.0 V/nS. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/nS in differential strobe mode.

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43. tIS and tIH (input setup and hold) derating.

tIS/tIH derating values for DDR2-667, DDR2-800 and DDR2-1066

Command/Address Slew Rate (V/nS)	ΔtIS and ΔtIH Derating Values for DDR2-667, DDR2-800 and DDR2-1066						
	CLK/ $\overline{\text{CLK}}$ Differential Slew Rate						
	2.0 V/nS		1.5 V/nS		1.0 V/nS		Unit
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
4.0	+150	+94	+180	+124	+210	+154	pS
3.5	+143	+89	+173	+119	+203	+149	pS
3.0	+133	+83	+163	+113	+193	+143	pS
2.5	+120	+75	+150	+105	+180	+135	pS
2.0	+100	+45	+130	+75	+160	+105	pS
1.5	+67	+21	+97	+51	+127	+81	pS
1.0	0	0	+30	+30	+60	+60	pS
0.9	-5	-14	+25	+16	+55	+46	pS
0.8	-13	-31	+17	-1	+47	+29	pS
0.7	-22	-54	+8	-24	+38	+6	pS
0.6	-34	-83	-4	-53	+26	-23	pS
0.5	-60	-125	-30	-95	0	-65	pS
0.4	-100	-188	-70	-158	-40	-128	pS
0.3	-168	-292	-138	-262	-108	-232	pS
0.25	-200	-375	-170	-345	-140	-315	pS
0.2	-325	-500	-295	-470	-265	-440	pS
0.15	-517	-708	-487	-678	-457	-648	pS
0.1	-1000	-1125	-970	-1095	-940	-1065	pS

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to AC region', use nominal slew rate for derating value. See Figure 20 Illustration of nominal slew rate for tIS.

If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value. See Figure 21 Illustration of tangent line for tIS.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'DC to VREF(dc) region', use nominal slew rate for derating value. See Figure 22 Illustration of nominal slew rate for tIH.

If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF(dc) region', the slew rate of a tangent line to the actual signal from the DC level to VREF(dc) level is used for derating value. See Figure 23 Illustration of tangent line for tIH.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in above tIS/tIH derating values for DDR2-667, DDR2-800 and DDR2-1066 table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

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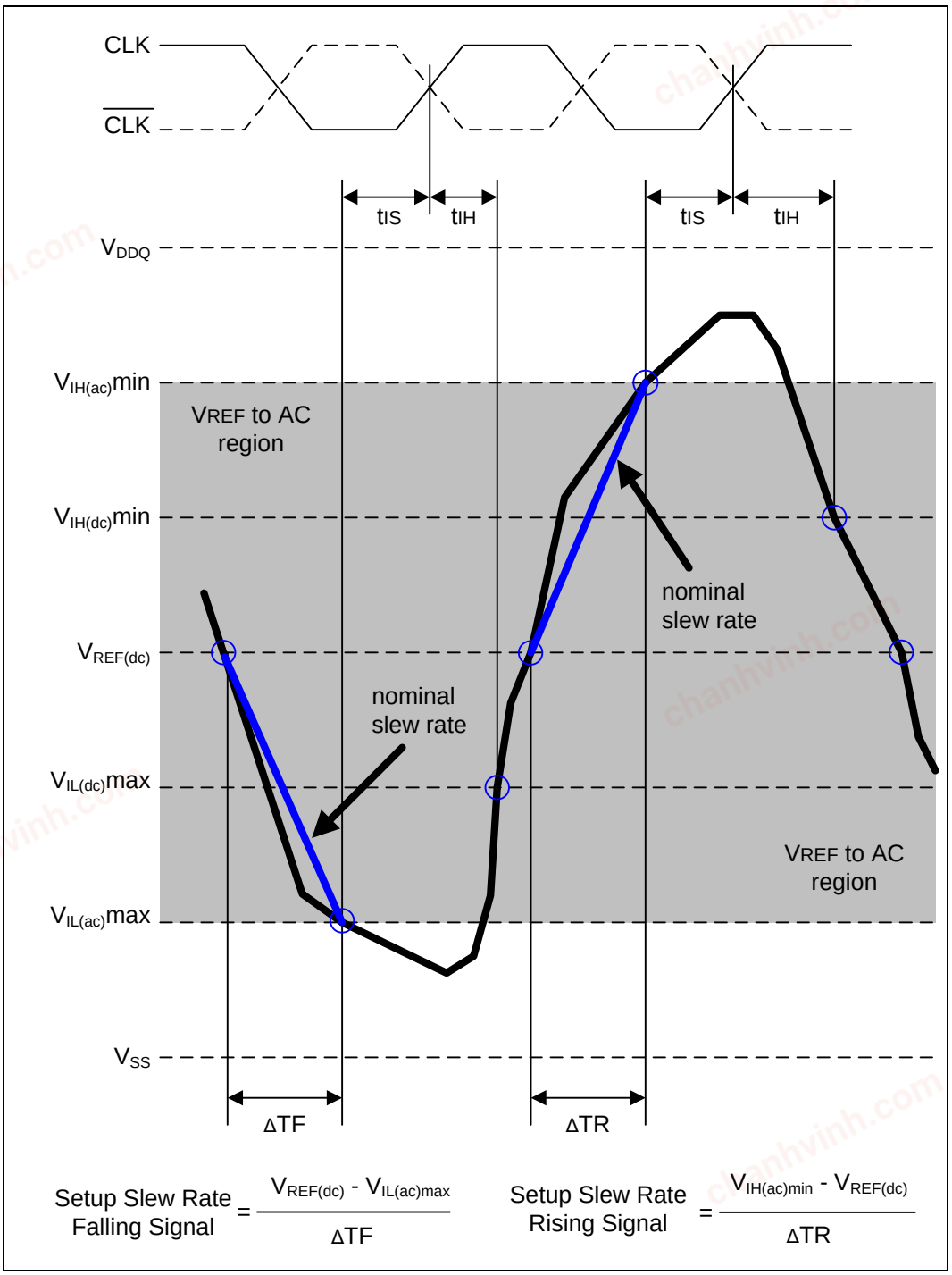


Figure 20 – Illustration of nominal slew rate for tIS

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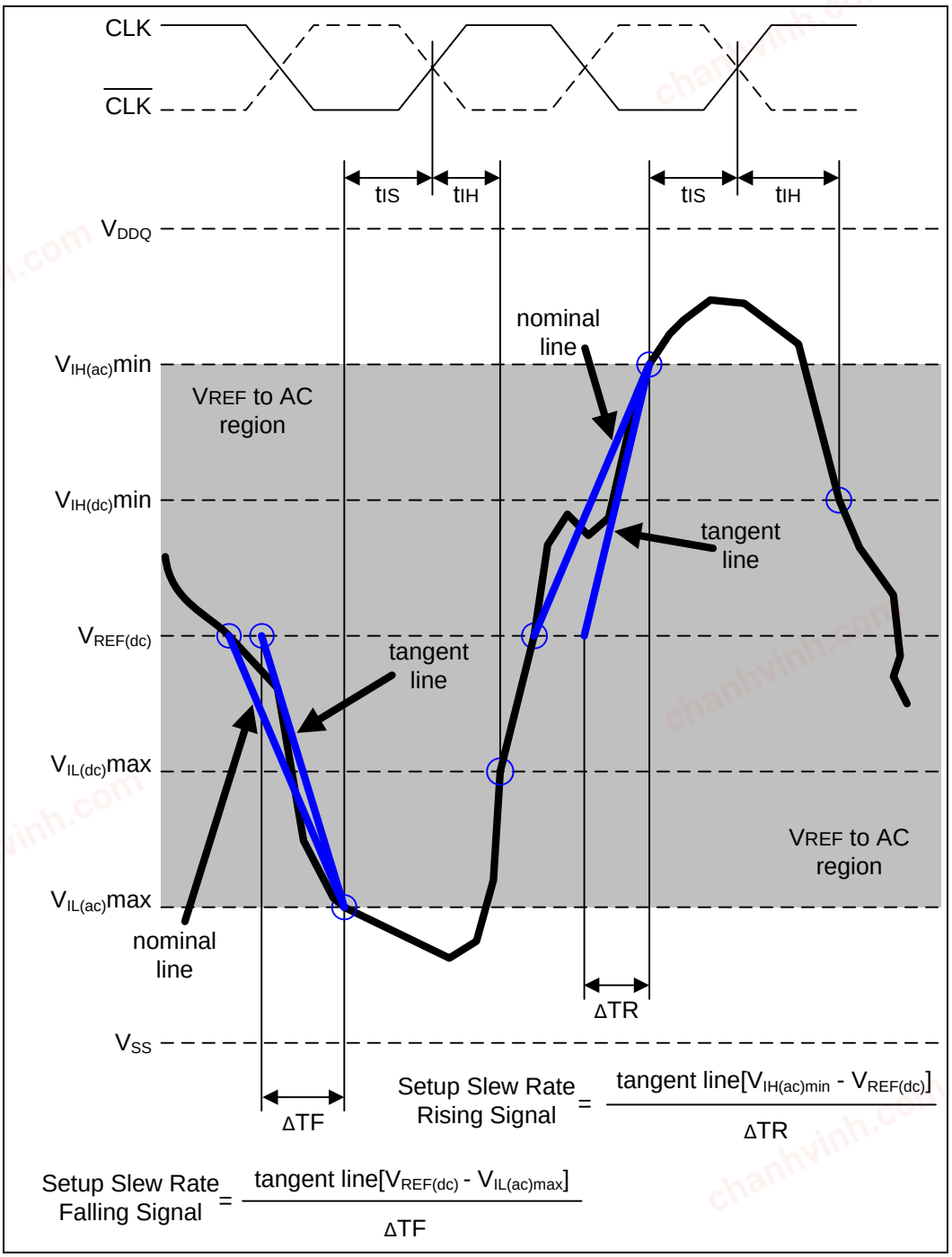


Figure 21 – Illustration of tangent line for tIS

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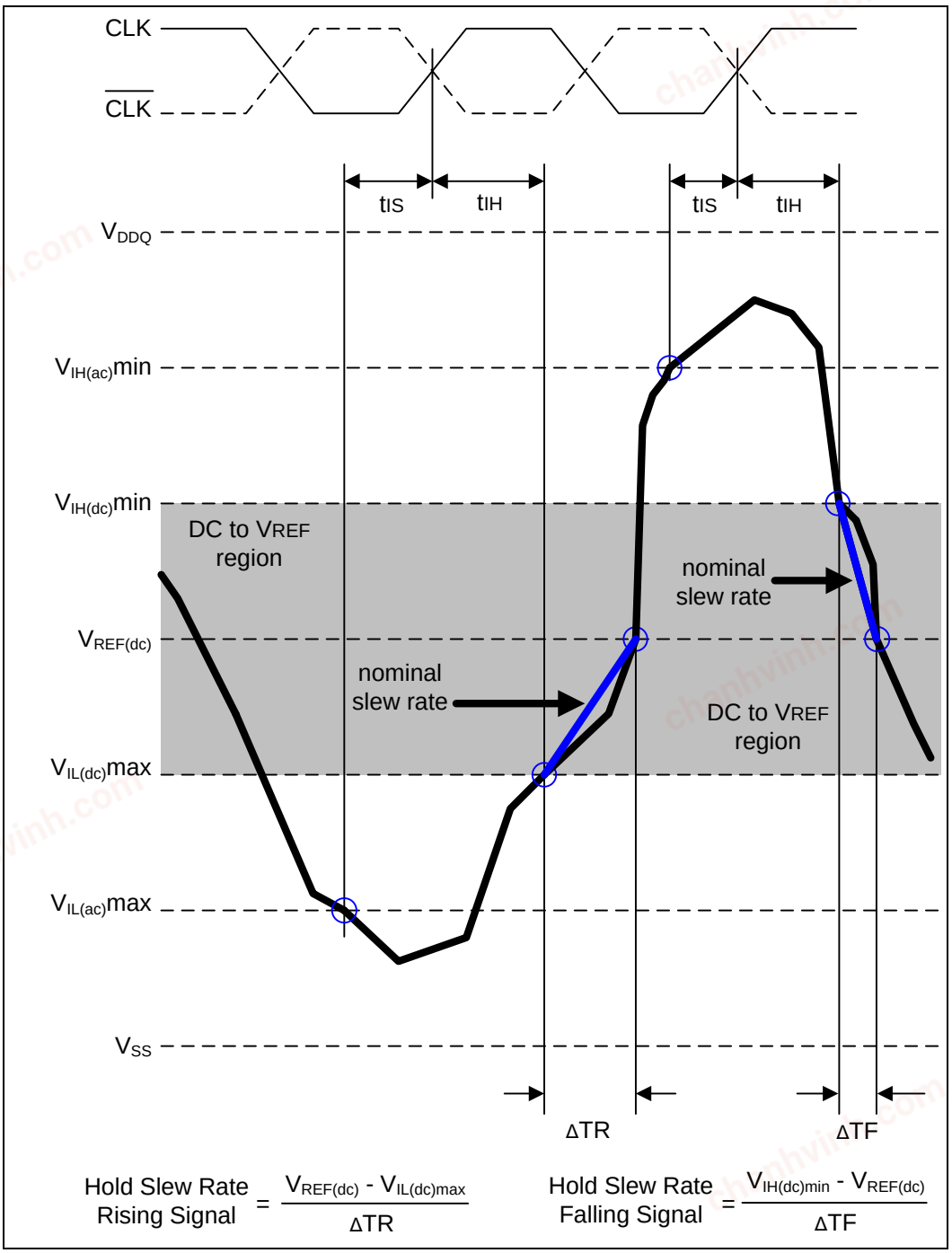


Figure 22 – Illustration of nominal slew rate for tIH

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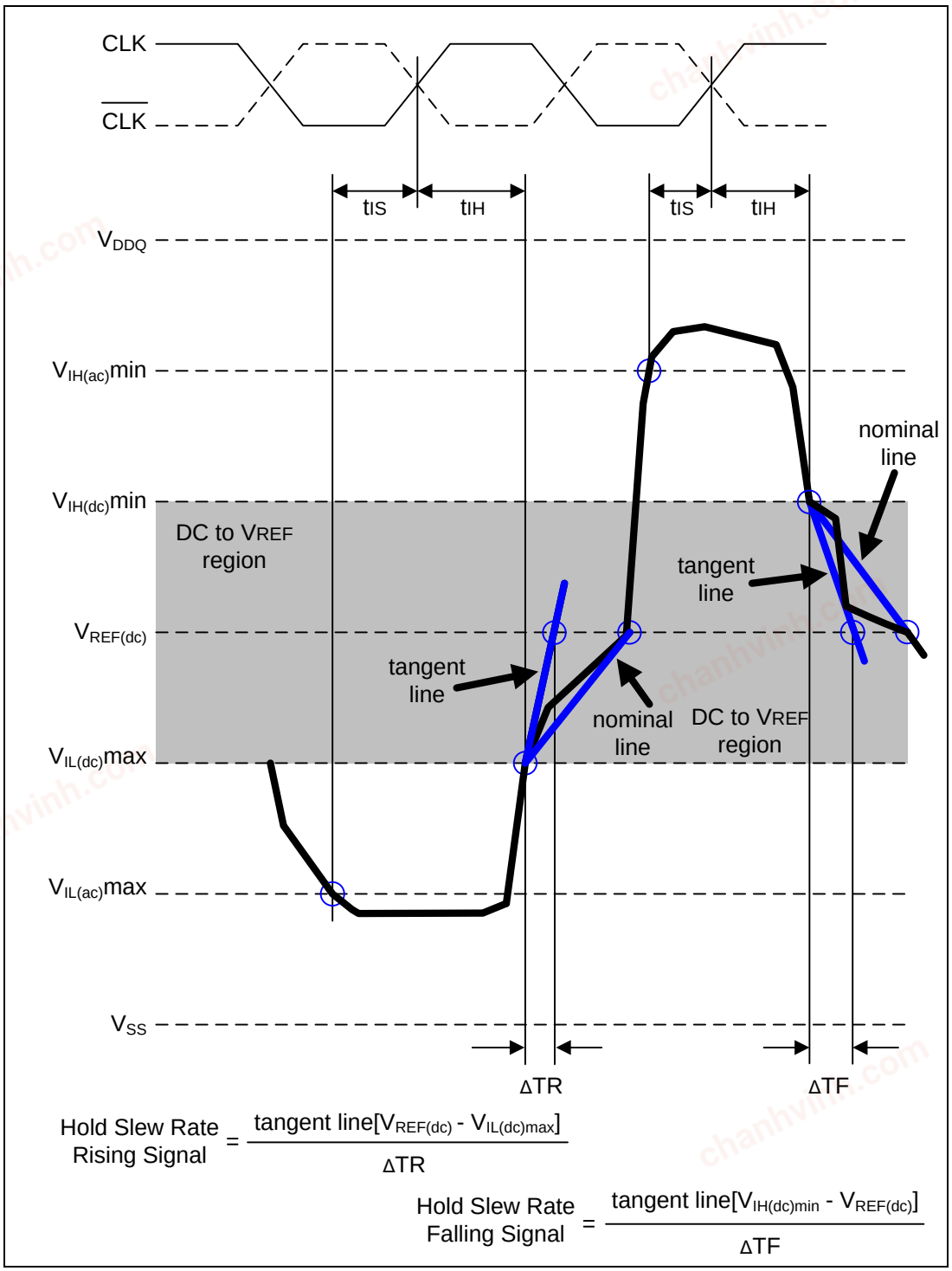


Figure 23 – Illustration of tangent line for tIH

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44. Data setup and hold time derating.

DDR2-667, DDR2-800 and DDR2-1066 tDS/tDH derating with differential data strobe

DQ Slew Rate (V/nS)	ΔtDS, ΔtDH Derating Values for DDR2-667, DDR2-800 and DDR2-1066 (All units in 'pS'; the note applies to the entire table)																	
	DQS/ $\overline{\text{DQS}}$ Differential Slew Rate																	
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS		0.8 V/nS	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to AC region', use nominal slew rate for derating value. See Figure 24 Illustration of nominal slew rate for tDS (differential DQS, $\overline{\text{DQS}}$).

If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value. See Figure 25 Illustration of tangent line for tDS (differential DQS, $\overline{\text{DQS}}$).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'DC level to VREF(dc) region', use nominal slew rate for derating value. See Figure 26 Illustration of nominal slew rate for tDH (differential DQS, $\overline{\text{DQS}}$).

If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF(dc) region', the slew rate of a tangent line to the actual signal from the DC level to VREF(dc) level is used for derating value. See Figure 27 Illustration of tangent line for tDH (differential DQS, $\overline{\text{DQS}}$).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in above DDR2-667, DDR2-800 and DDR2-1066 tDS/tDH derating with differential data strobe table, the derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

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45. Slew Rate Measurement Levels:

a) Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals.

For differential signals (e.g. DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = - 500 mV and DQS - $\overline{DQS}$ = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

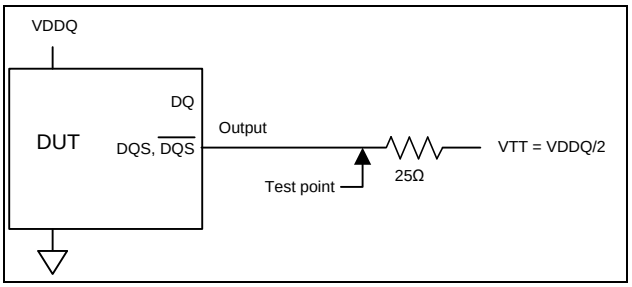
b) Input slew rate for single ended signals is measured from VREF(dc) to VIH(ac),min for rising edges and from VREF(dc) to VIL(ac),max for falling edges.

For differential signals (e.g. CLK - $\overline{CLK}$) slew rate for rising edges is measured from CLK - $\overline{CLK}$ = - 250 mV to CLK - $\overline{CLK}$ = + 500 mV (+ 250 mV to - 500 mV for falling edges).

c) V_{ID} is the magnitude of the difference between the input voltage on CLK and the input voltage on $\overline{CLK}$, or between DQS and $\overline{DQS}$ for differential strobe.

46. DDR2 SDRAM output slew rate test load:

Output slew rate is characterized under the test conditions as shown in below figure.



Output slew rate test load

47. Differential data strobe:

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the cross point of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization.

Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10 kΩ resistor to insure proper operation.

48. All parts list in ordering information table (section 3) will not guarantee to meet functional and AC specification if the t_{CK} out of range mentioned in 10.11 AC Characteristics table.

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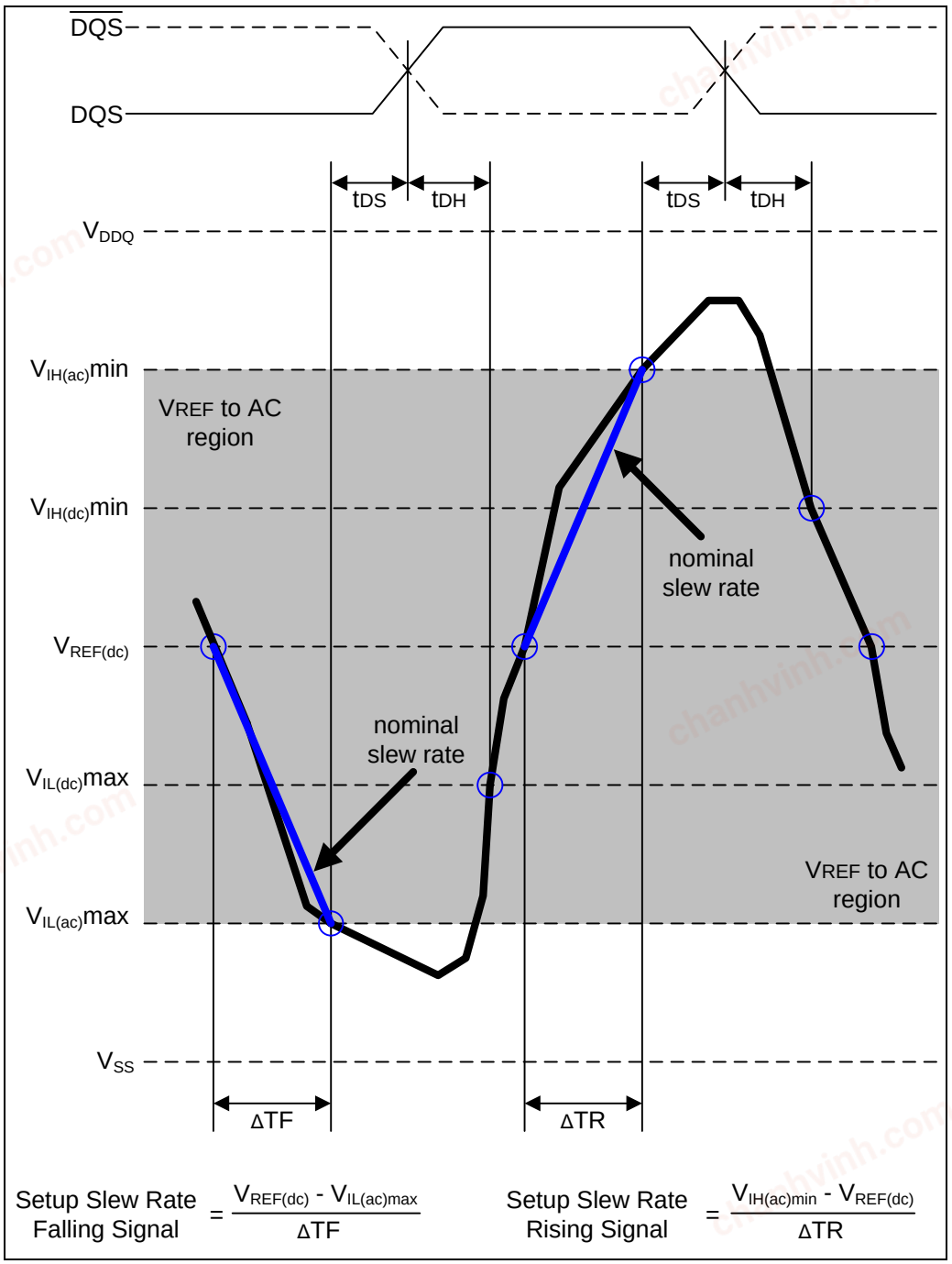


Figure 24 – Illustration of nominal slew rate for tDS (differential DQS, $\overline{DQS}$)

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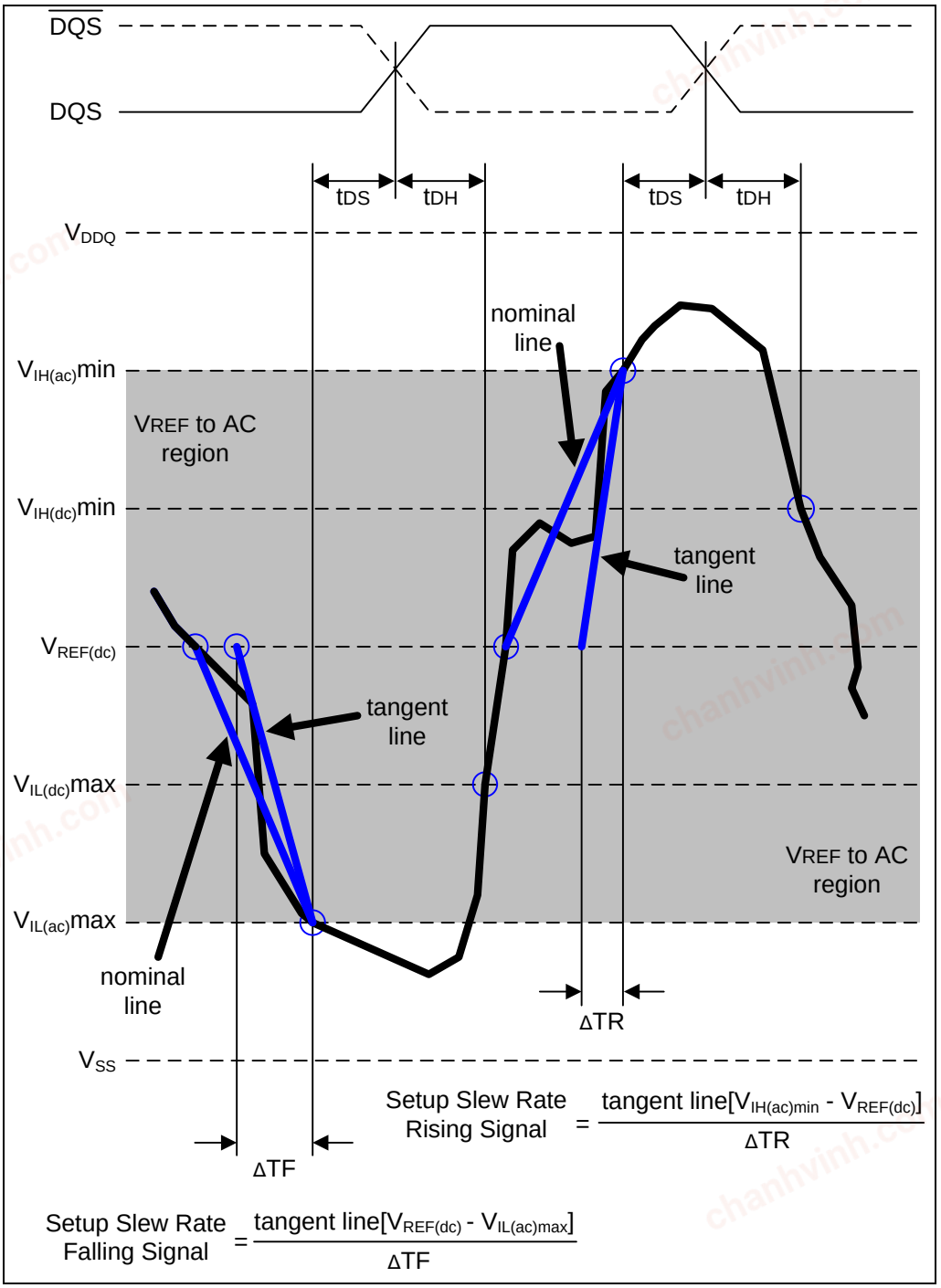


Figure 25 – Illustration of tangent line for tDS (differential DQS, $\overline{DQS}$)

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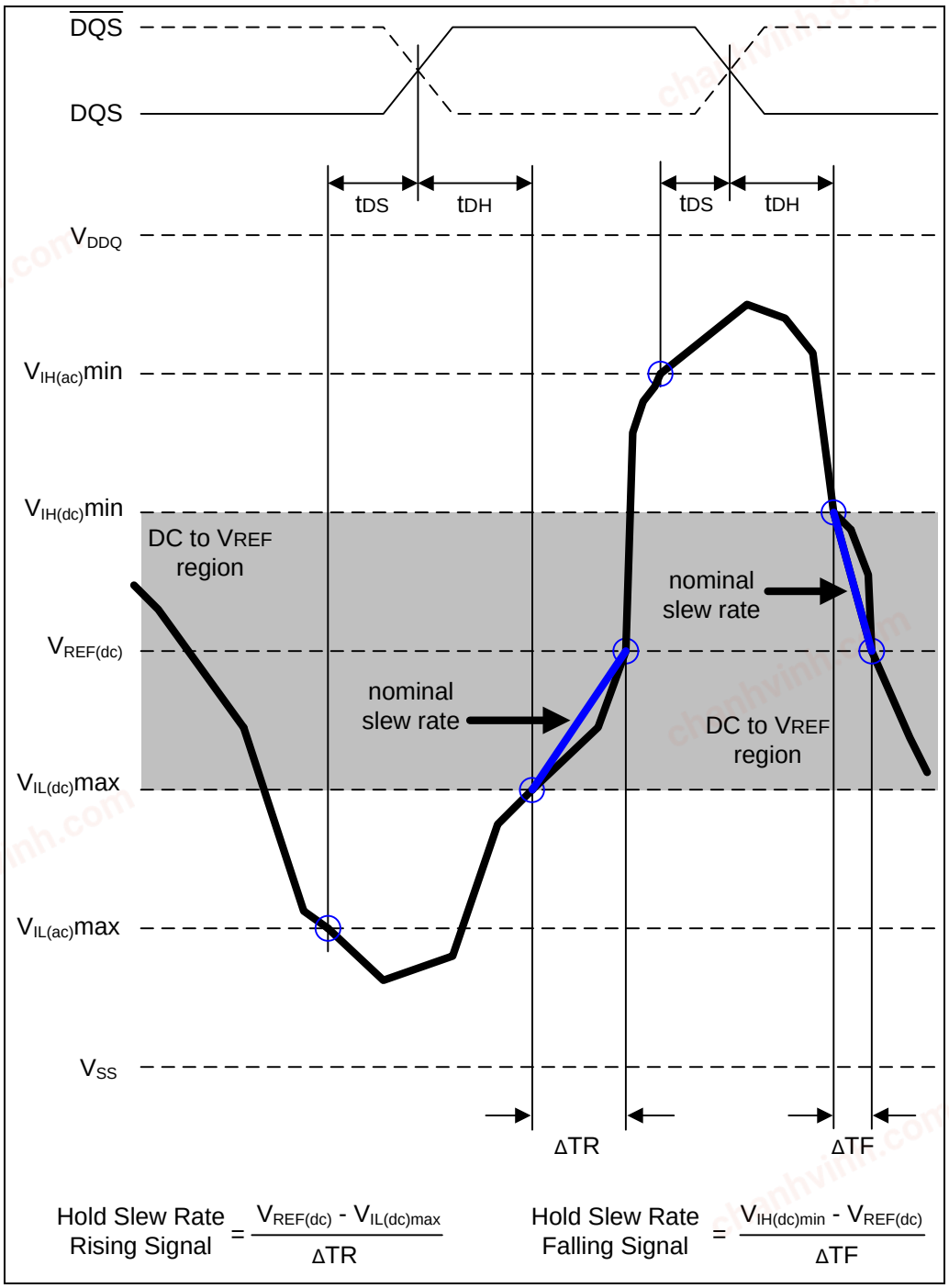


Figure 26 – Illustration of nominal slew rate for tDH (differential DQS, $\overline{DQS}$)

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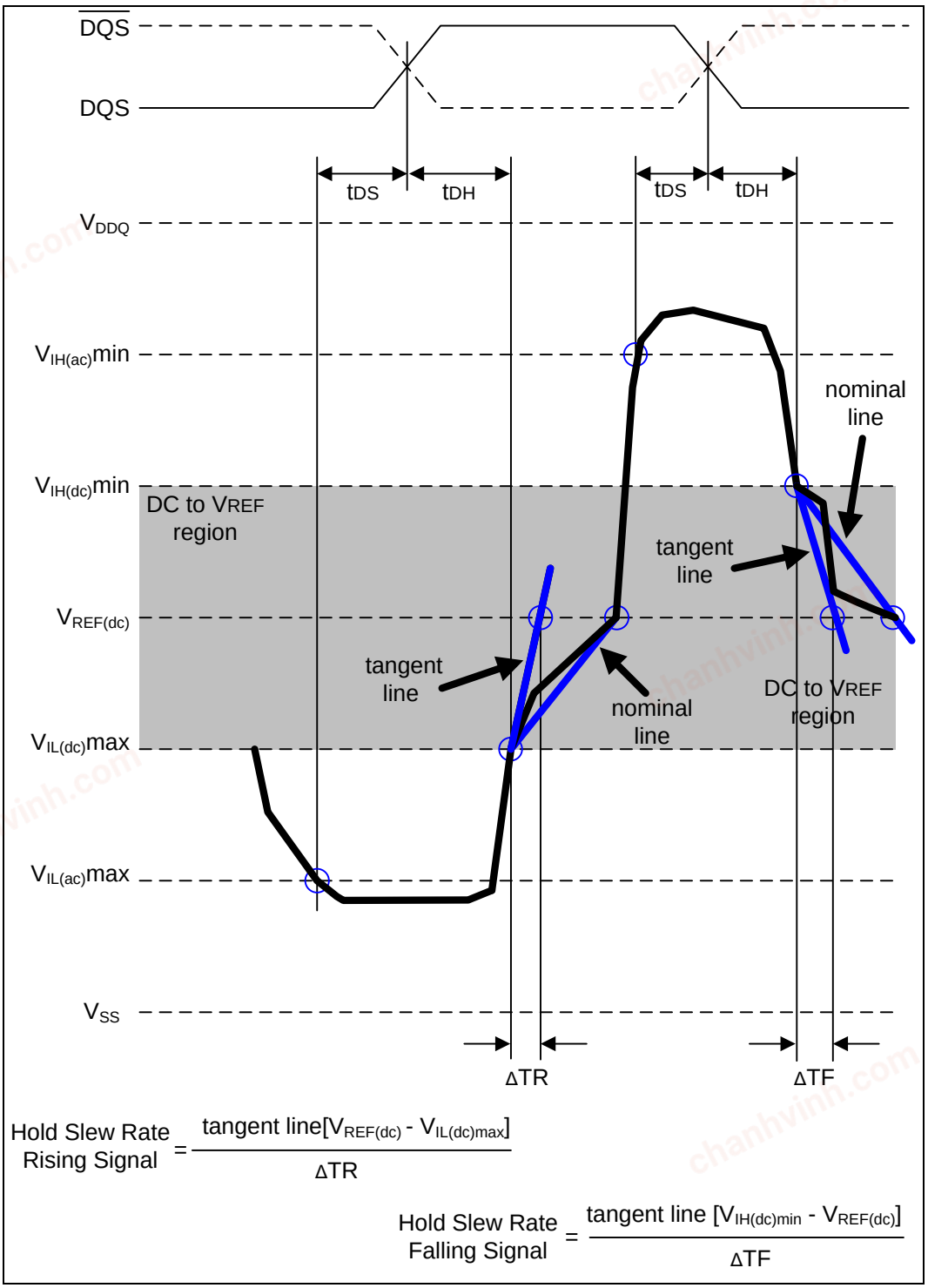


Figure 27 – Illustration tangent line for tDH (differential DQS, $\overline{DQS}$)

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10.12 AC Input Test Conditions

CONDITION	SYMBOL	VALUE	UNIT	NOTES
Input reference voltage	VREF	0.5 x VDDQ	V	1
Input signal maximum peak to peak swing	VSWING(MAX)	1.0	V	1
Input signal minimum slew rate	SLEW	1.0	V/nS	2, 3

Notes:

1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(ac) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(ac) min for rising edges and the range from VREF to VIL(ac) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

10.13 Differential Input/Output AC Logic Levels

PARAMETER	SYM.	MIN.	MAX.	UNIT	NOTES
AC differential input voltage	VID (ac)	0.5	VDDQ + 0.6	V	1
AC differential cross point input voltage	VIX (ac)	0.5 x VDDQ - 0.175	0.5 x VDDQ + 0.175	V	2
AC differential cross point output voltage	VOX (ac)	0.5 x VDDQ - 0.125	0.5 x VDDQ + 0.125	V	3

Notes:

1. VID (ac) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CLK, LDQS or UDQS) and VCP is the complementary input signal (such as $\overline{CLK}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to VIH (ac) - VIL (ac).
2. The typical value of VIX (ac) is expected to be about 0.5 x VDDQ of the transmitting device and VIX (ac) is expected to track variations in VDDQ. VIX (ac) indicates the voltage at which differential input signals must cross.
3. The typical value of VOX (ac) is expected to be about 0.5 x VDDQ of the transmitting device and VOX (ac) is expected to track variations in VDDQ. VOX (ac) indicates the voltage at which differential output signals must cross.

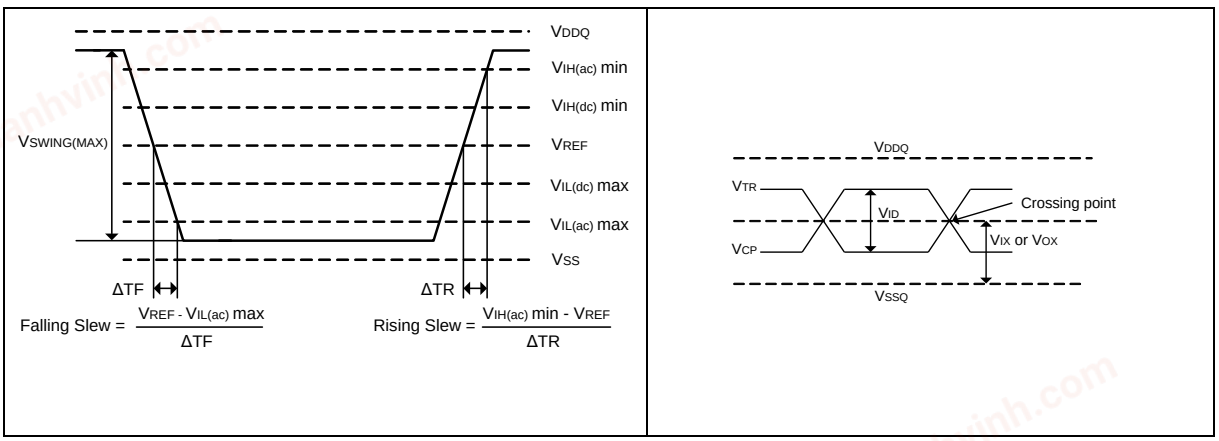


Figure 28 – AC input test signal and Differential signal levels waveform

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10.14 AC Overshoot / Undershoot Specification

10.14.1 AC Overshoot / Undershoot Specification for Address and Control Pins:

Applies to A0-A12, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

PARAMETER	DDR2-1066	DDR2-800	DDR2-667	UNIT
Maximum peak amplitude allowed for overshoot area	0.5	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	0.5	V
Maximum overshoot area above VDD	0.5	0.66	0.8	V-nS
Maximum undershoot area below VSS	0.5	0.66	0.8	V-nS

10.14.2 AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins:

Applies to DQ, LDQS, $\overline{LDQS}$, UDQS, $\overline{UDQS}$, LDM, UDM, CLK, $\overline{CLK}$

PARAMETER	DDR2-1066	DDR2-800	DDR2-667	UNIT
Maximum peak amplitude allowed for overshoot area	0.5	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	0.5	V
Maximum overshoot area above VDDQ	0.19	0.23	0.23	V-nS
Maximum undershoot area below VSSQ	0.19	0.23	0.23	V-nS

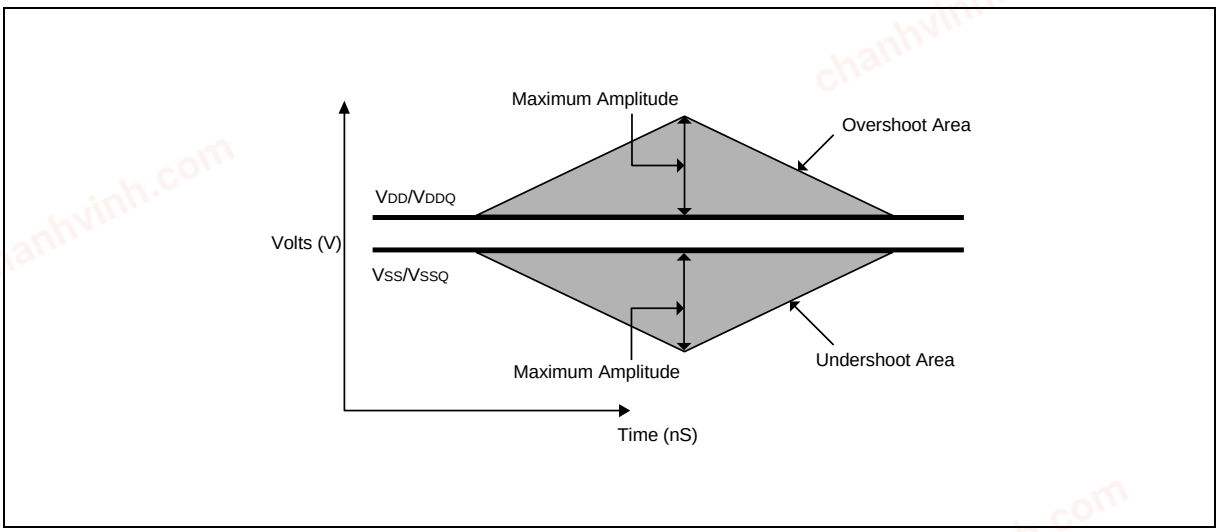
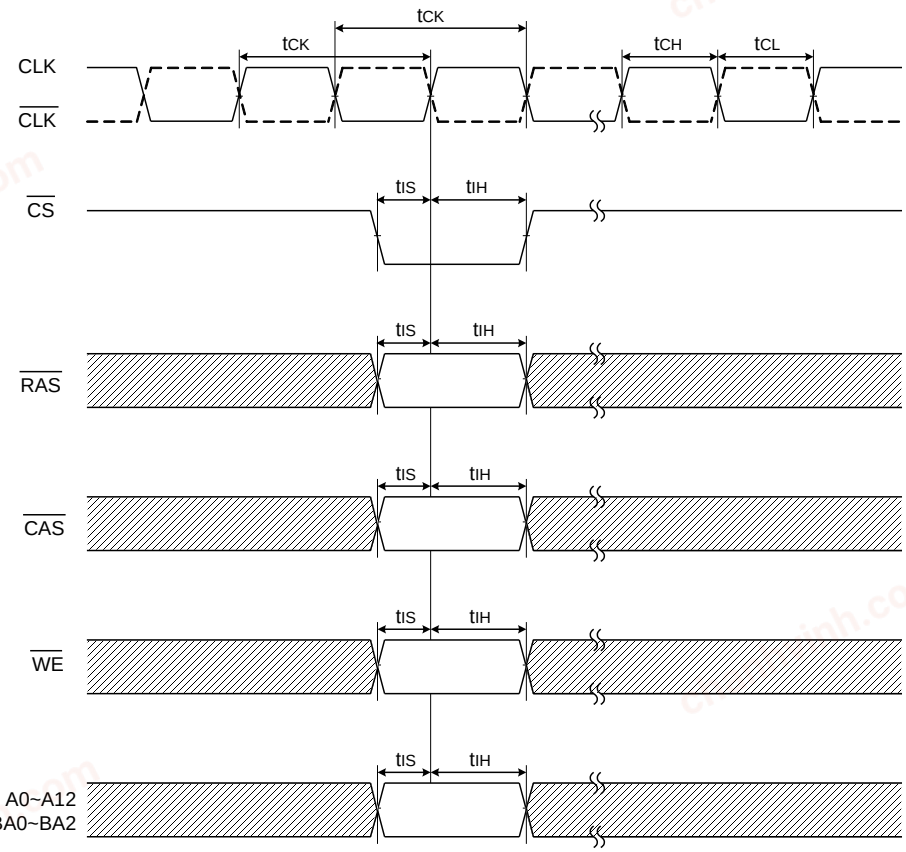


Figure 29 – AC overshoot and undershoot definition

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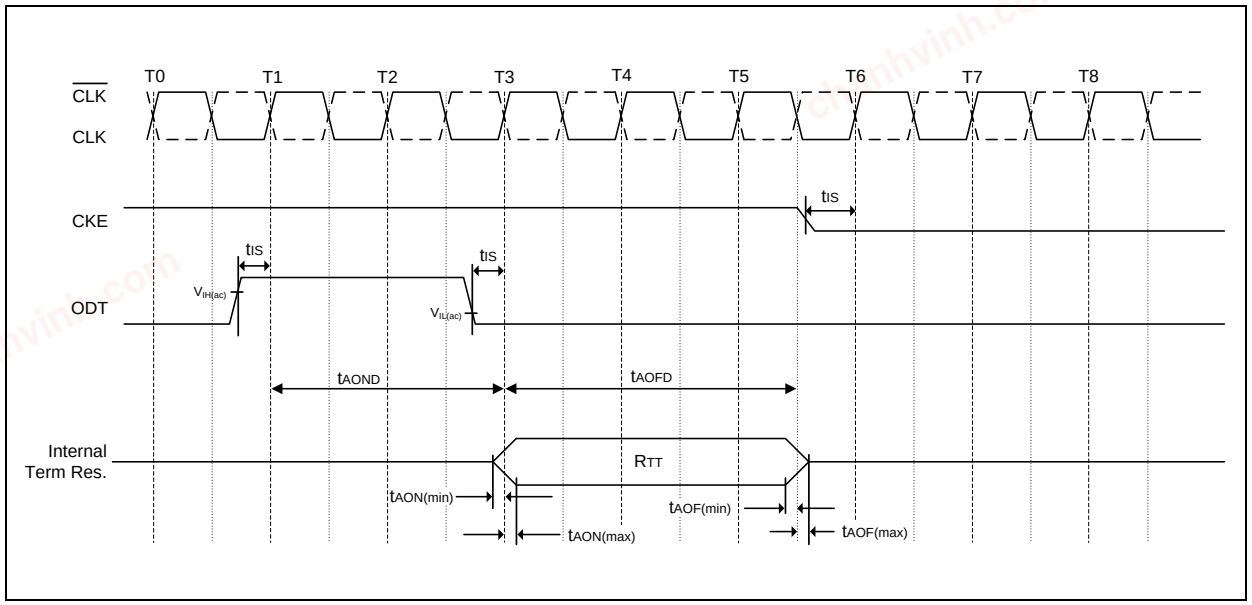
11. TIMING WAVEFORMS

11.1 Command Input Timing

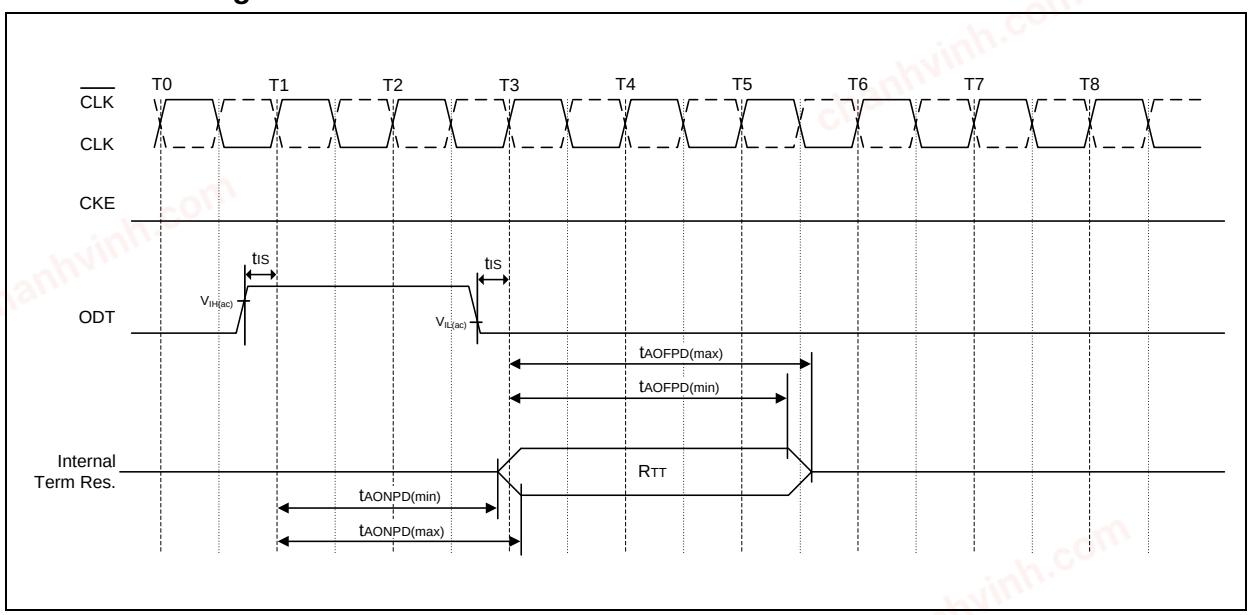


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11.2 ODT Timing for Active/Standby Mode

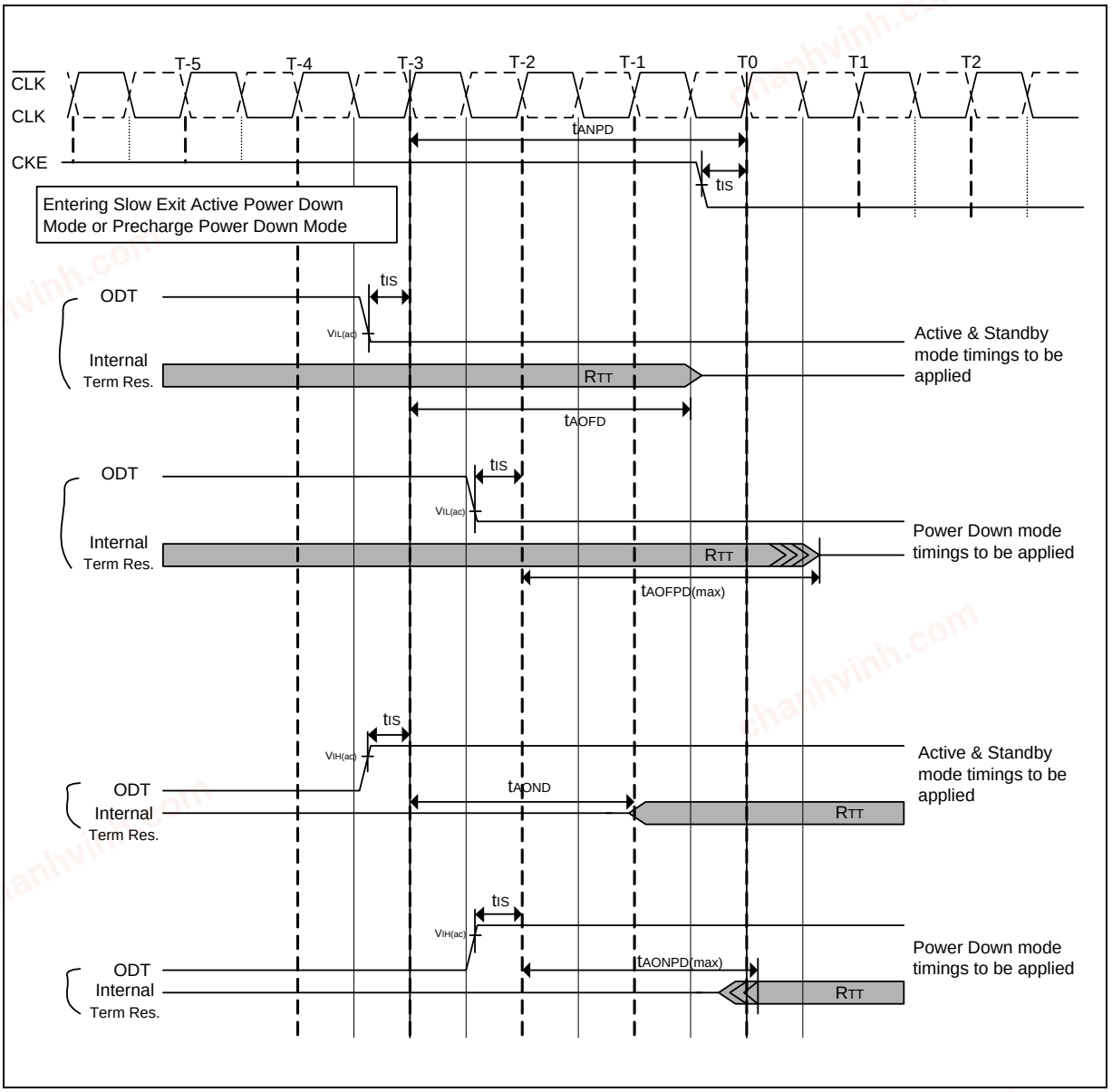


11.3 ODT Timing for Power Down Mode



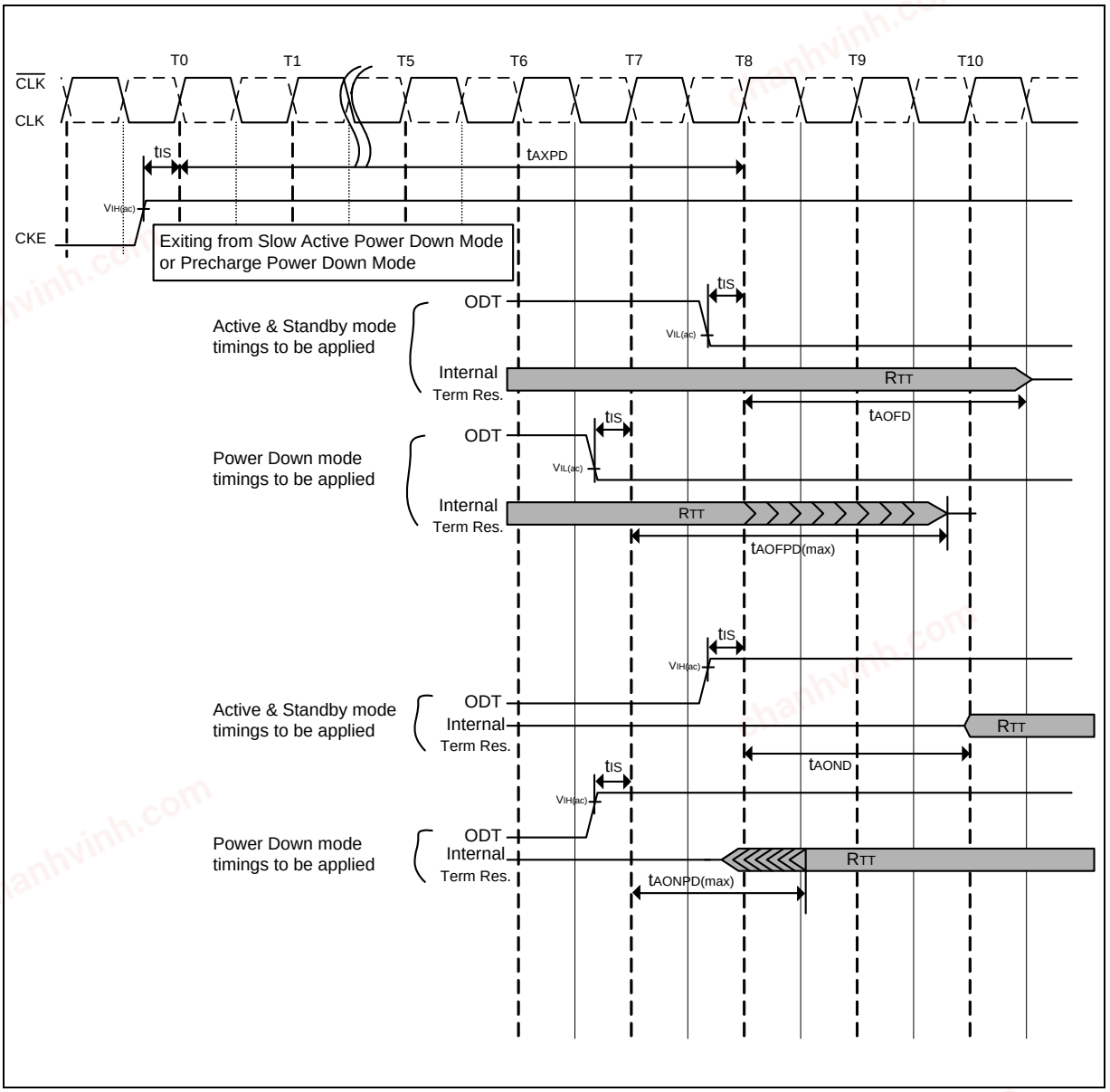
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11.4 ODT Timing mode switch at entering power down mode



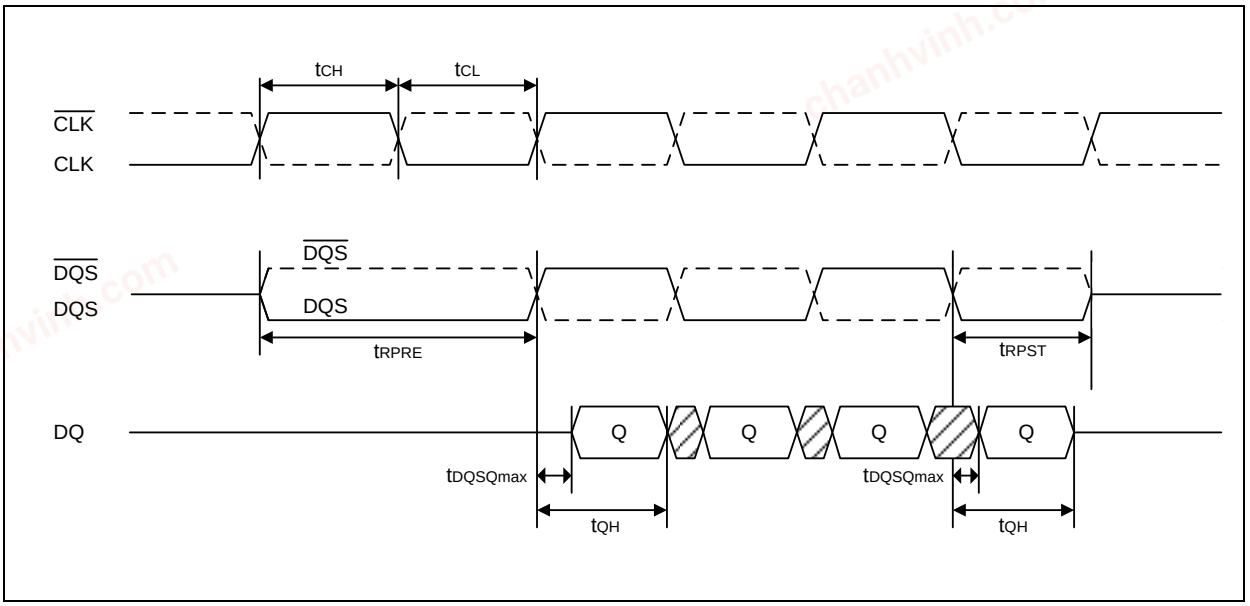
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11.5 ODT Timing mode switch at exiting power down mode

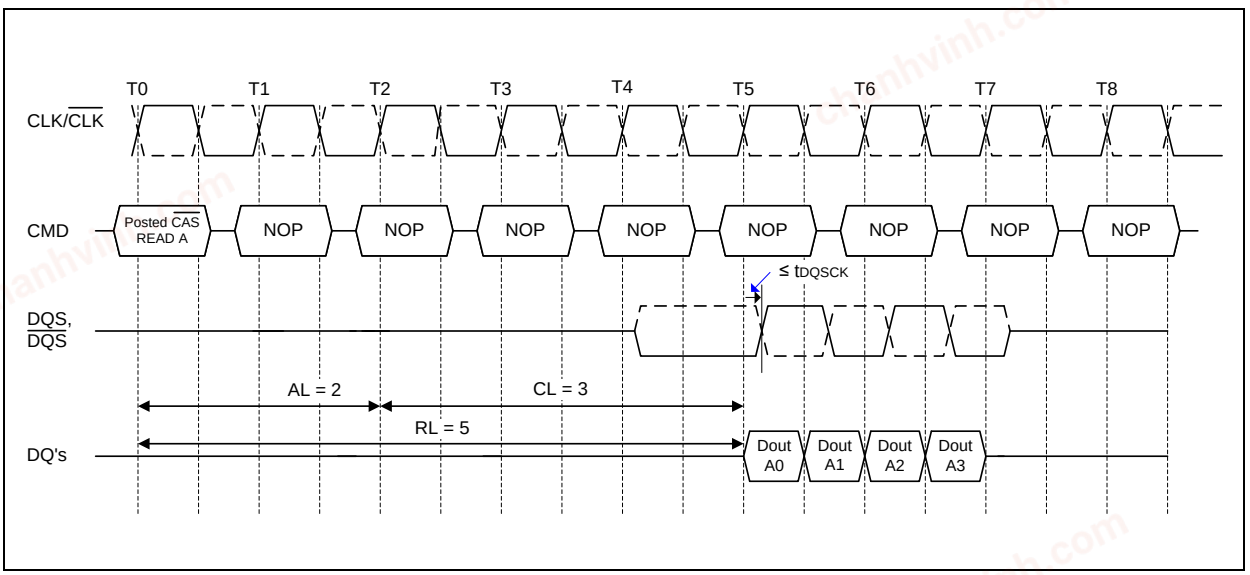


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11.6 Data output (read) timing

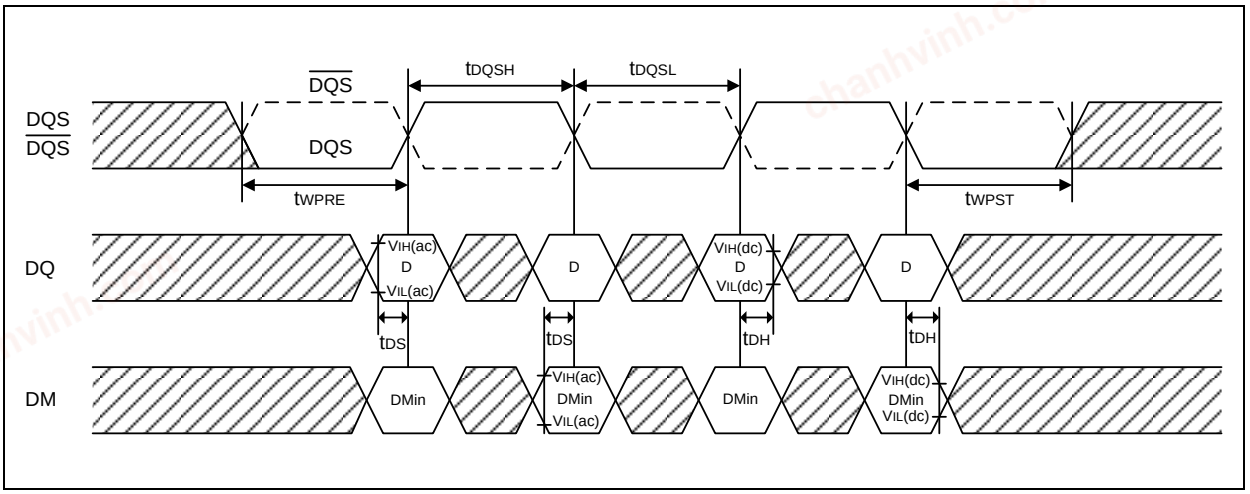


11.7 Burst read operation: RL=5 (AL=2, CL=3, BL=4)

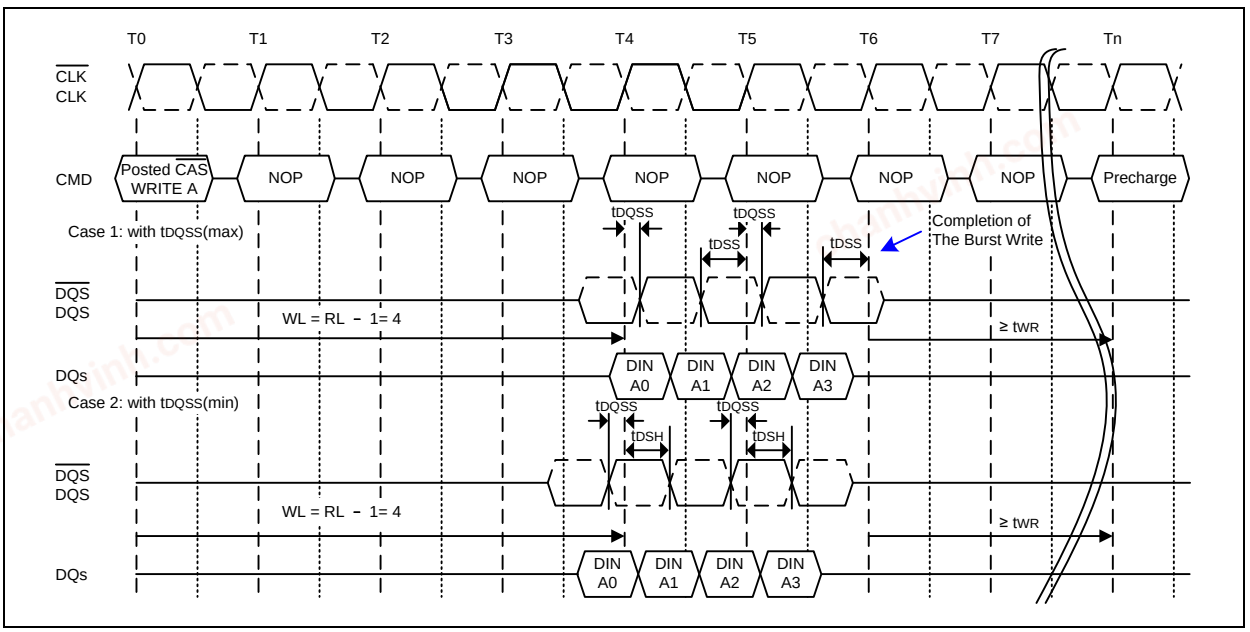


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11.8 Data input (write) timing

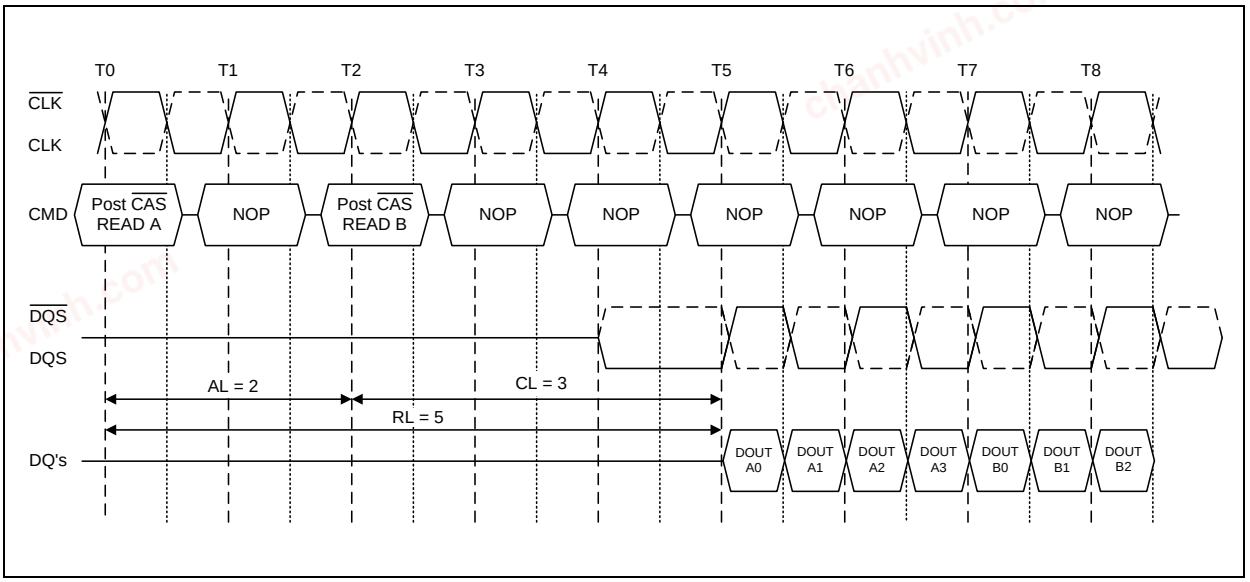


11.9 Burst write operation: RL=5 (AL=2, CL=3, WL=4, BL=4)



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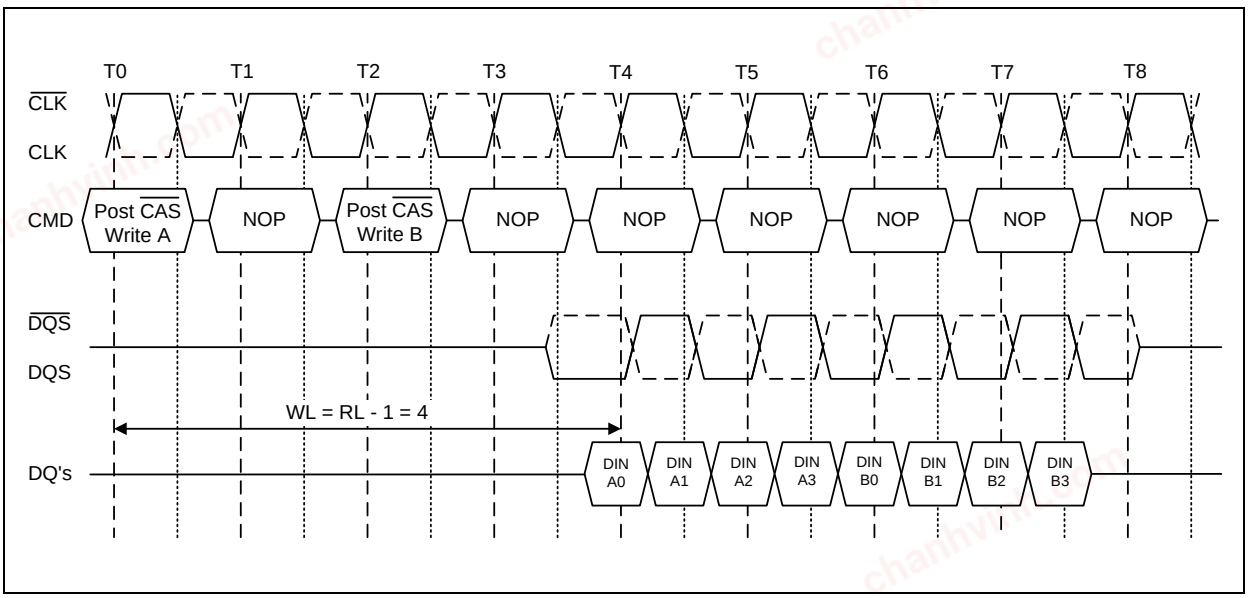
11.10 Seamless burst read operation: RL = 5 (AL = 2, and CL = 3, BL = 4)



Note:

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

11.11 Seamless burst write operation: RL = 5 (WL = 4, BL = 4)

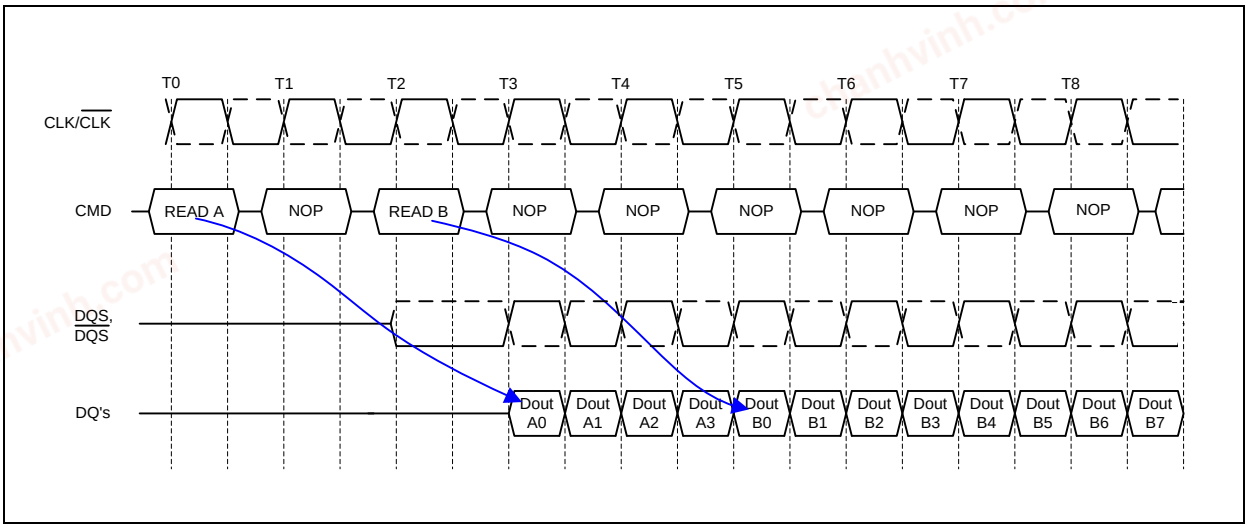


Note:

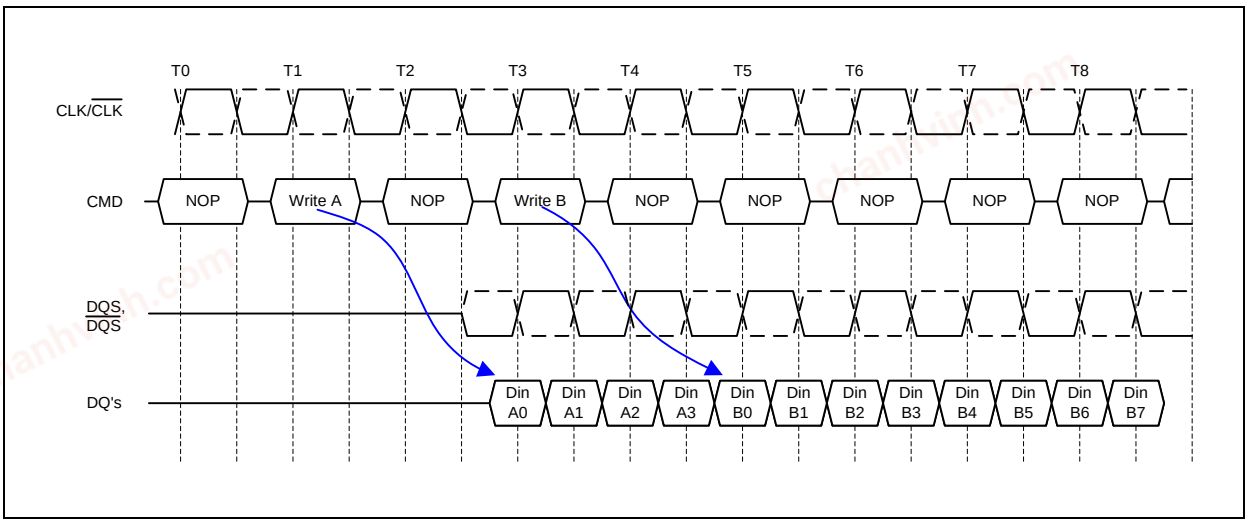
The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

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11.12 Burst read interrupt timing: RL =3 (CL=3, AL=0, BL=8)

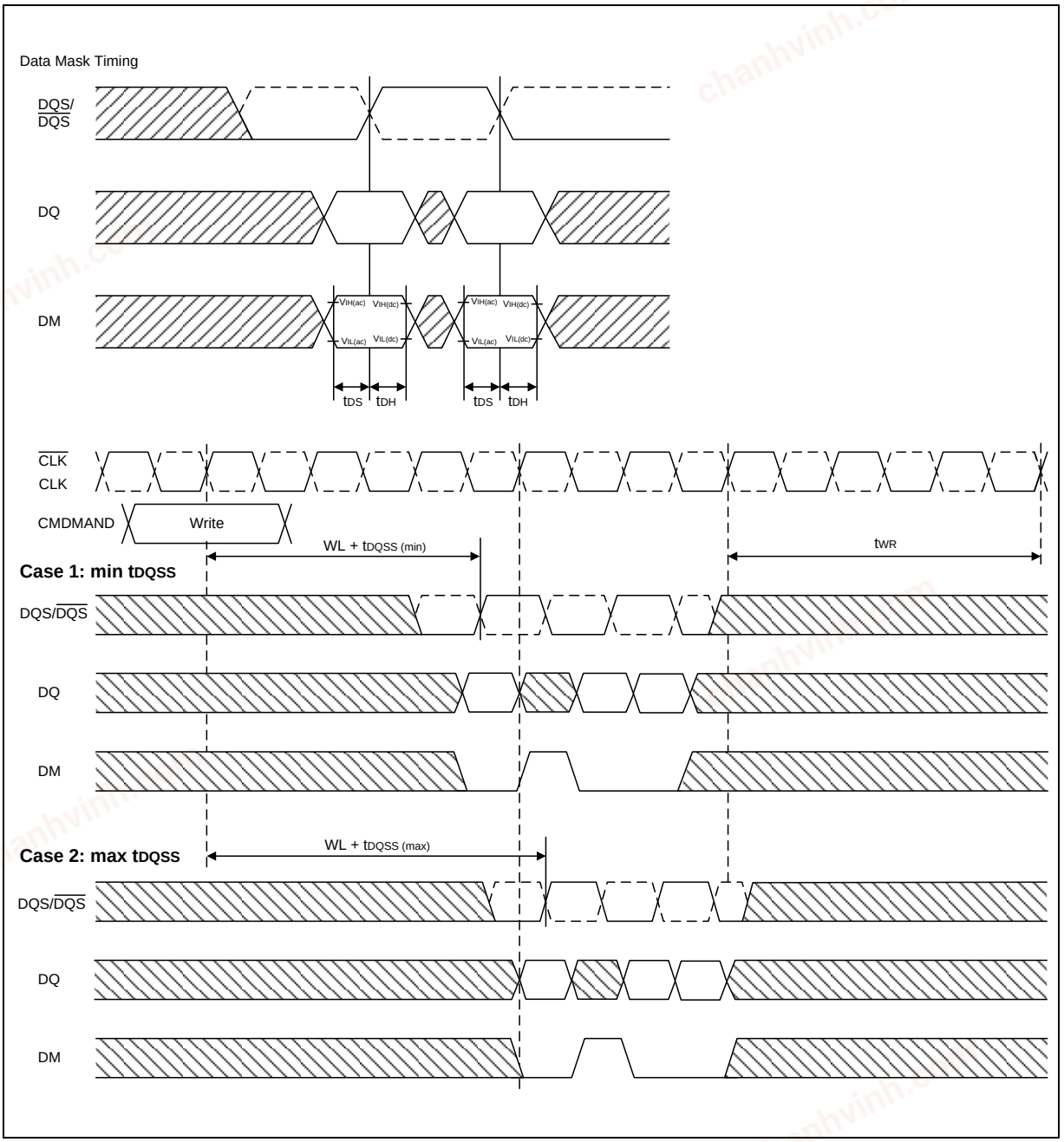


11.13 Burst write interrupt timing: RL=3 (CL=3, AL=0, WL=2, BL=8)



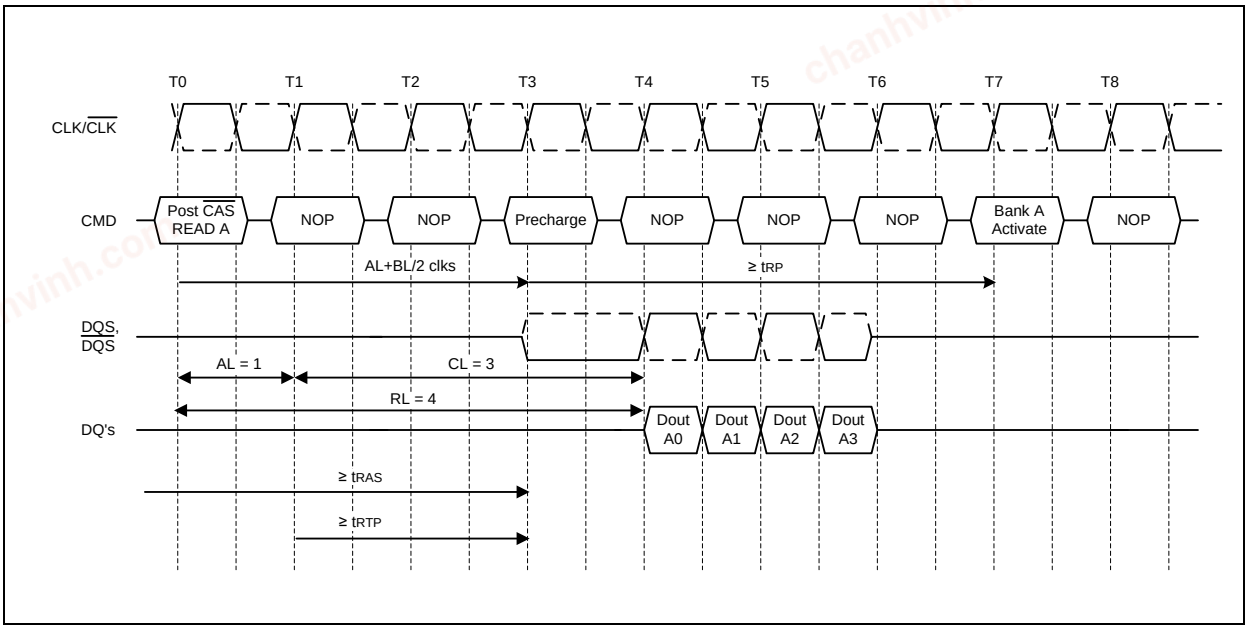
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11.14 Write operation with Data Mask: WL=3, AL=0, BL=4)

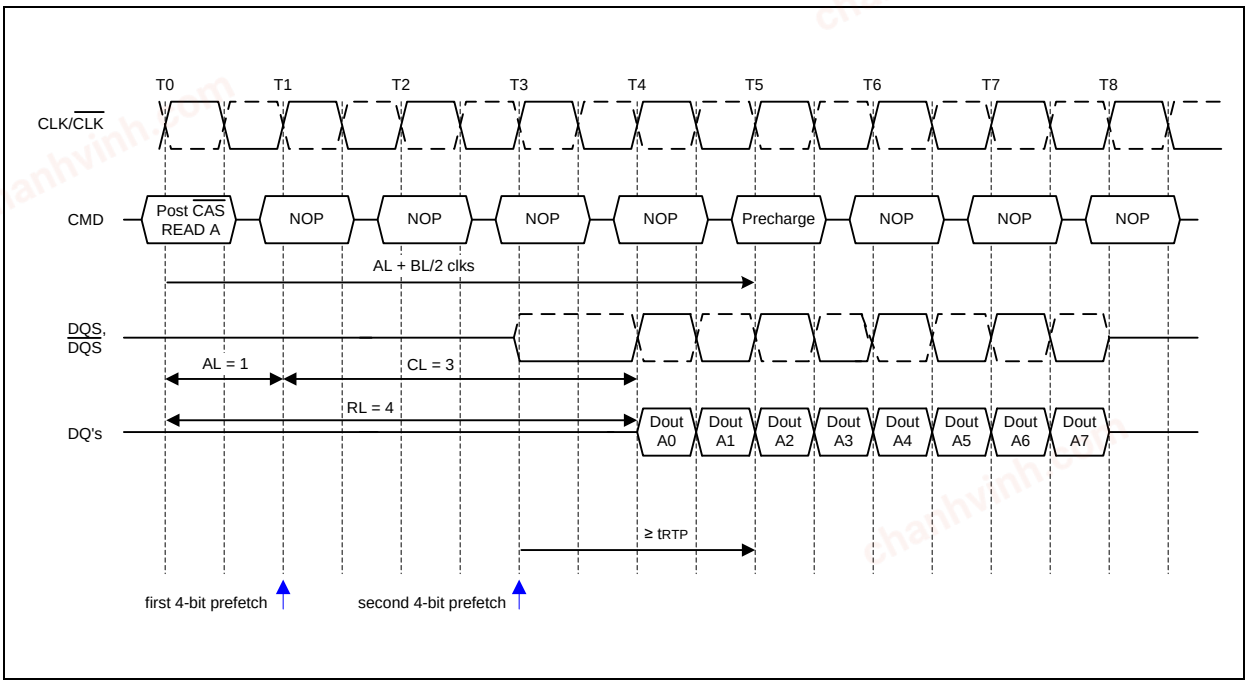


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11.15 Burst read operation followed by precharge: RL=4 (AL=1, CL=3, BL=4, tRTP ≤ 2clks)

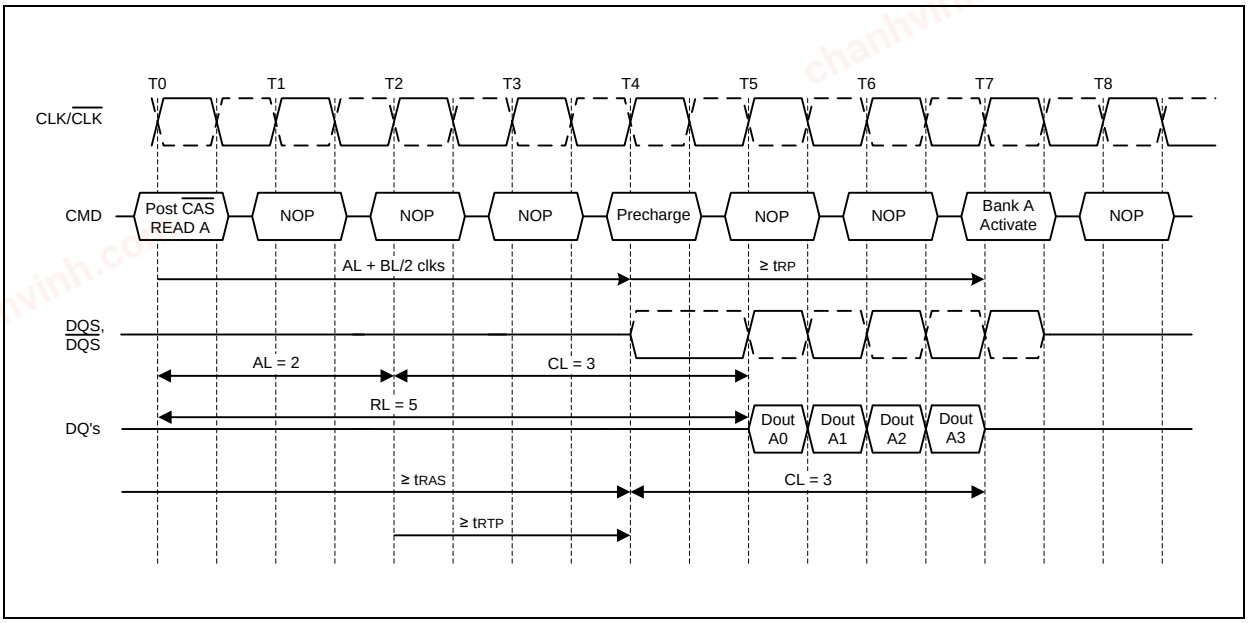


11.16 Burst read operation followed by precharge: RL=4 (AL=1, CL=3, BL=8, tRTP ≤ 2clks)

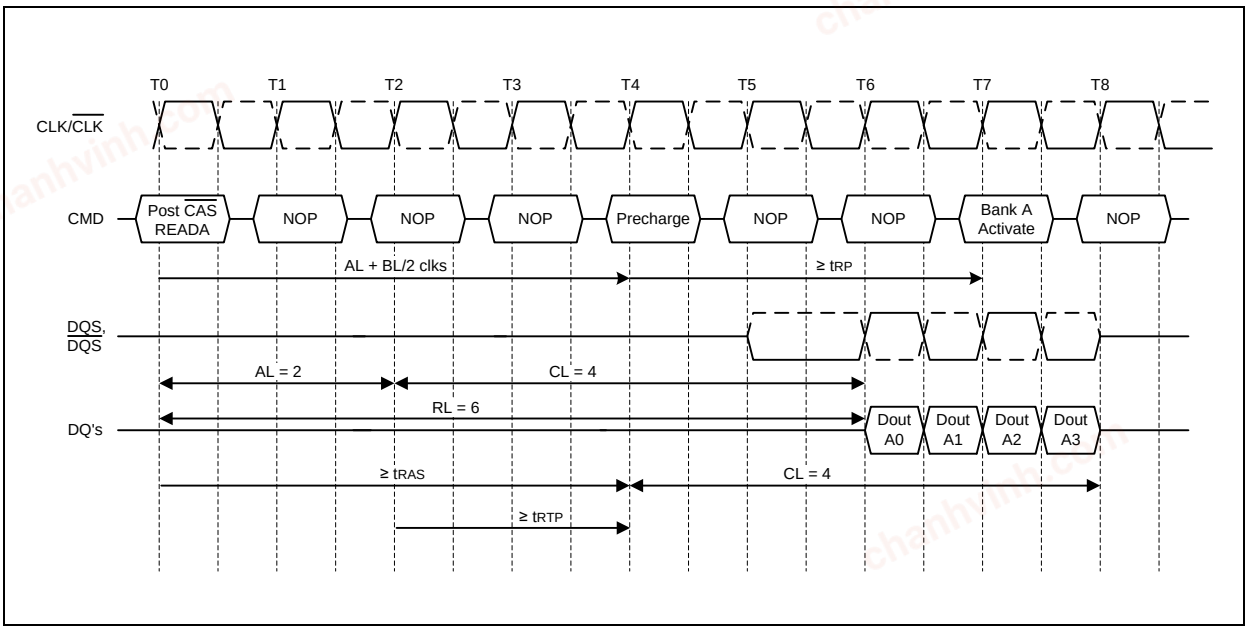


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11.17 Burst read operation followed by precharge: RL=5 (AL=2, CL=3, BL=4, tRTP ≤ 2clks)

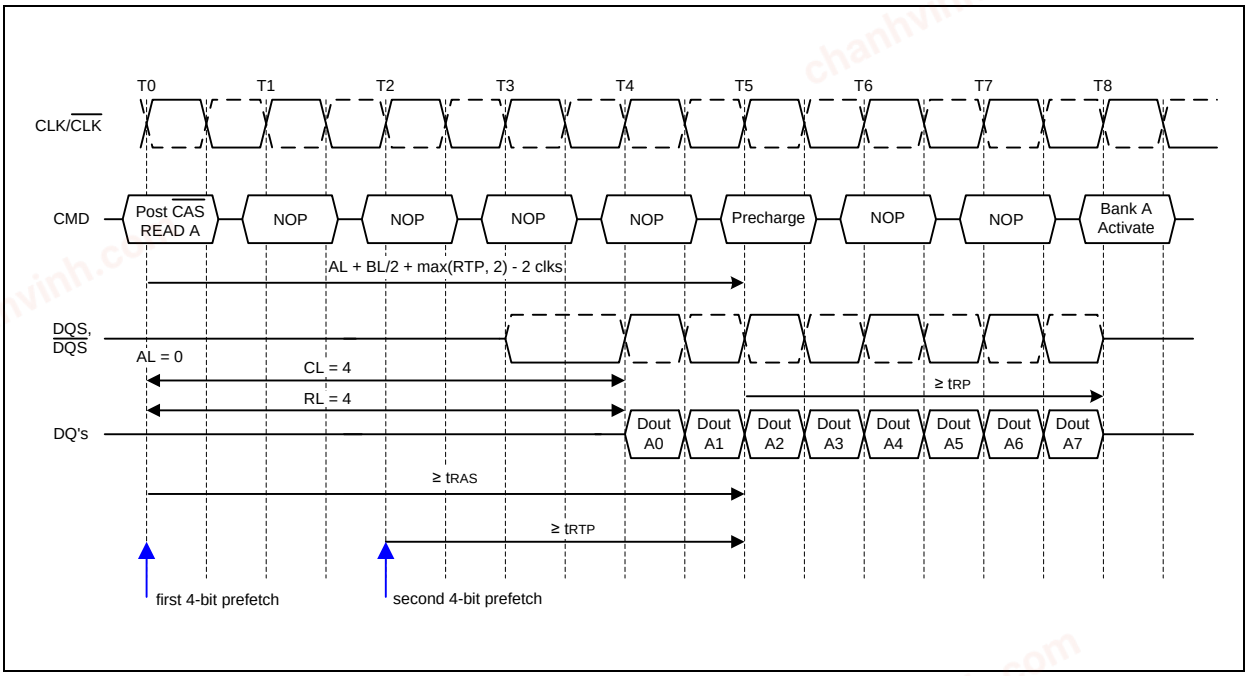


11.18 Burst read operation followed by precharge: RL=6 (AL=2, CL=4, BL=4, tRTP ≤ 2clks)

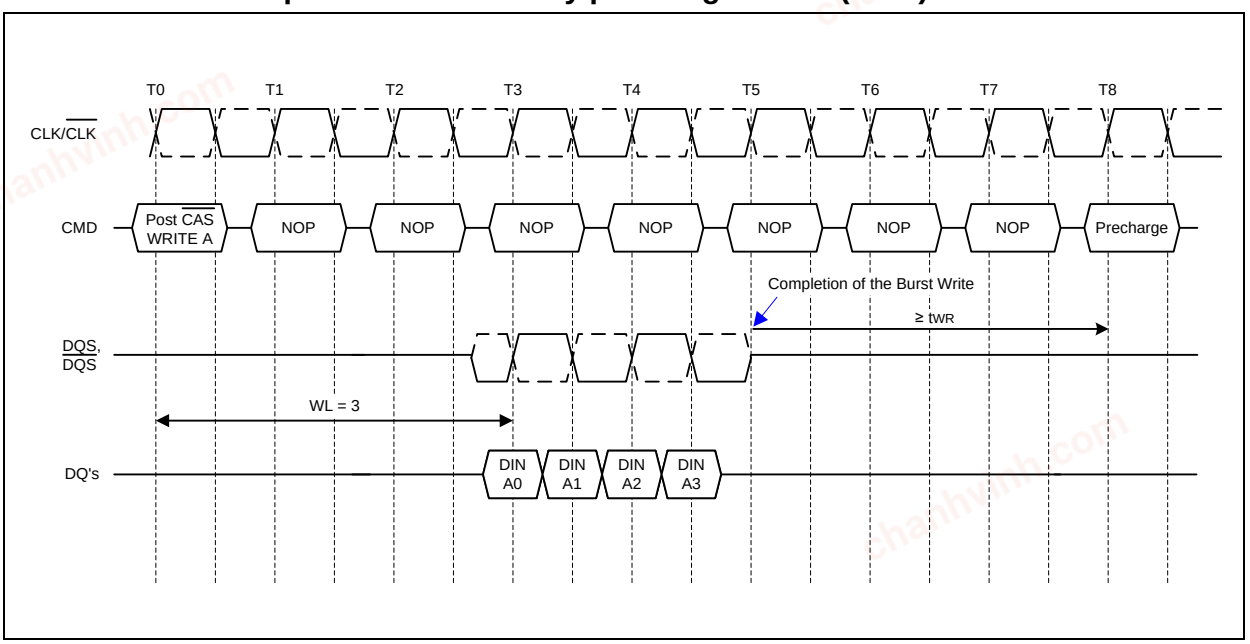


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11.19 Burst read operation followed by precharge: RL=4 (AL=0, CL=4, BL=8, tRTP > 2clks)

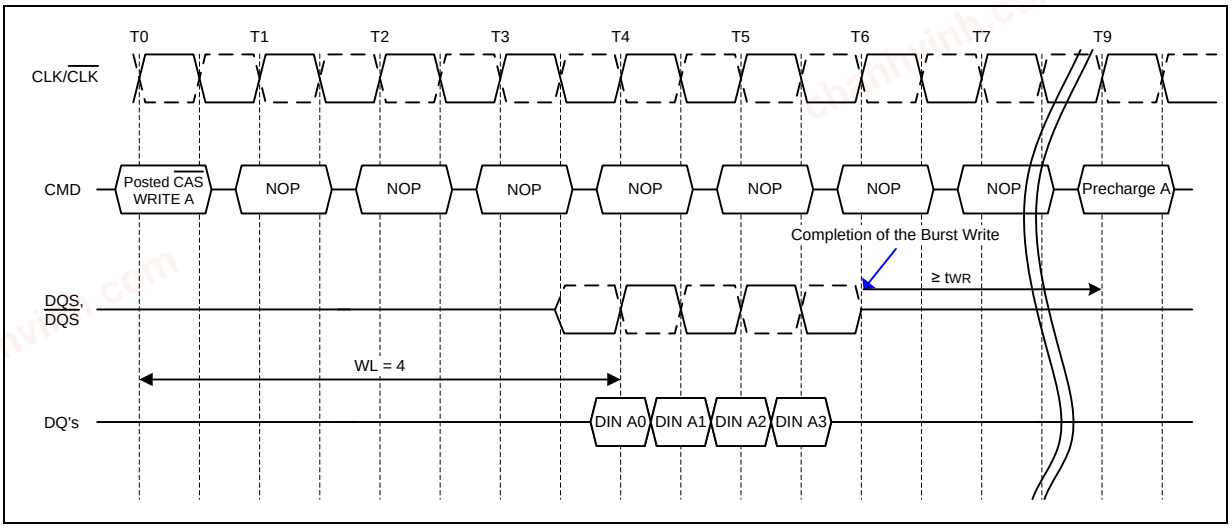


11.20 Burst write operation followed by precharge: WL = (RL-1) = 3

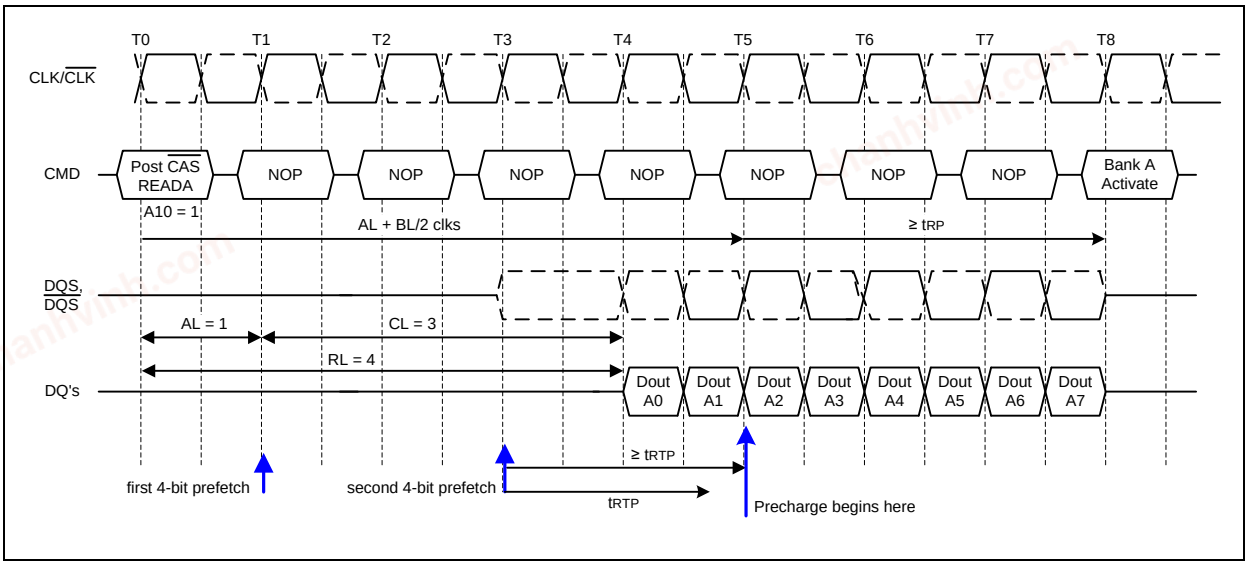


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11.21 Burst write operation followed by precharge: WL = (RL-1) = 4

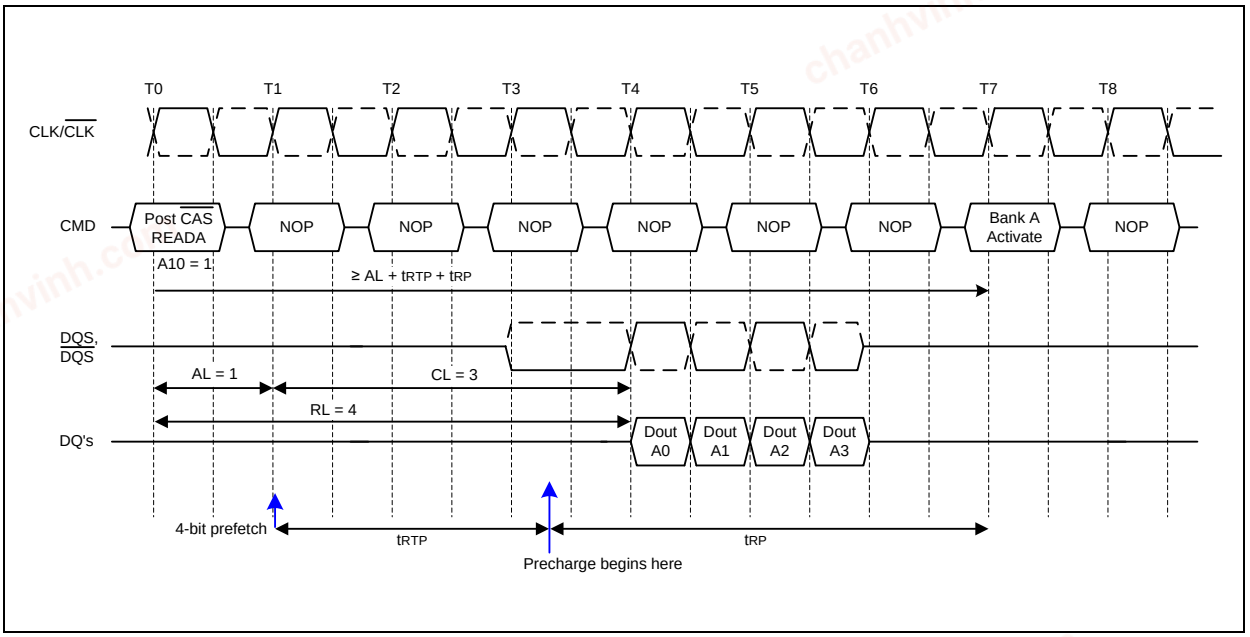


11.22 Burst read operation with Auto-precharge: RL=4 (AL=1, CL=3, BL=8, tRTP ≤ 2clks)

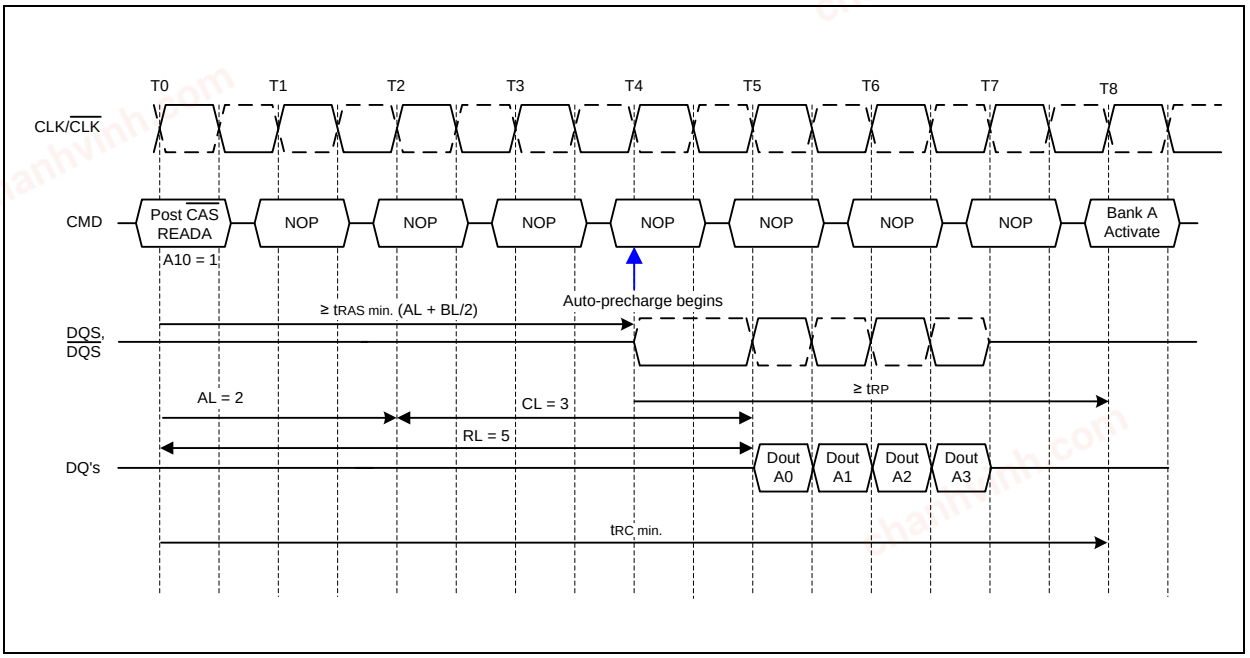


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11.23 Burst read operation with Auto-precharge: RL=4 (AL=1, CL=3, BL=4, tRTP > 2clks)

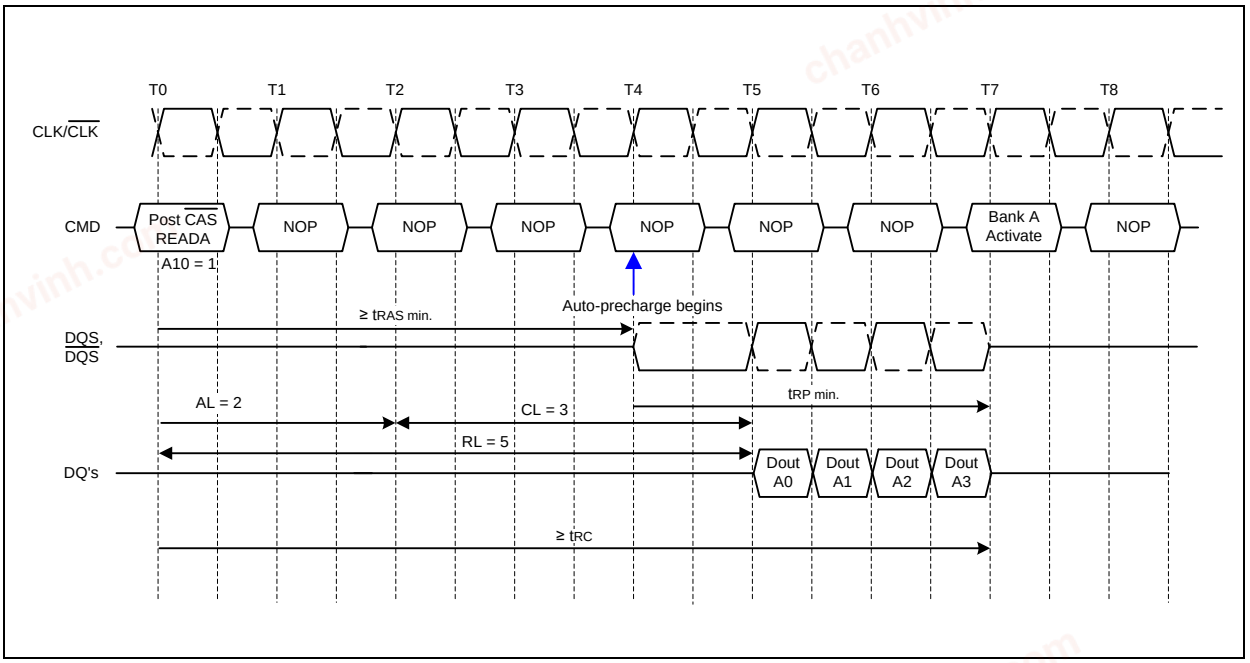


11.24 Burst read with Auto-precharge followed by an activation to the same bank (tRC Limit): RL=5 (AL=2, CL=3, internal tRCD=3, BL=4, tRTP ≤ 2clks)

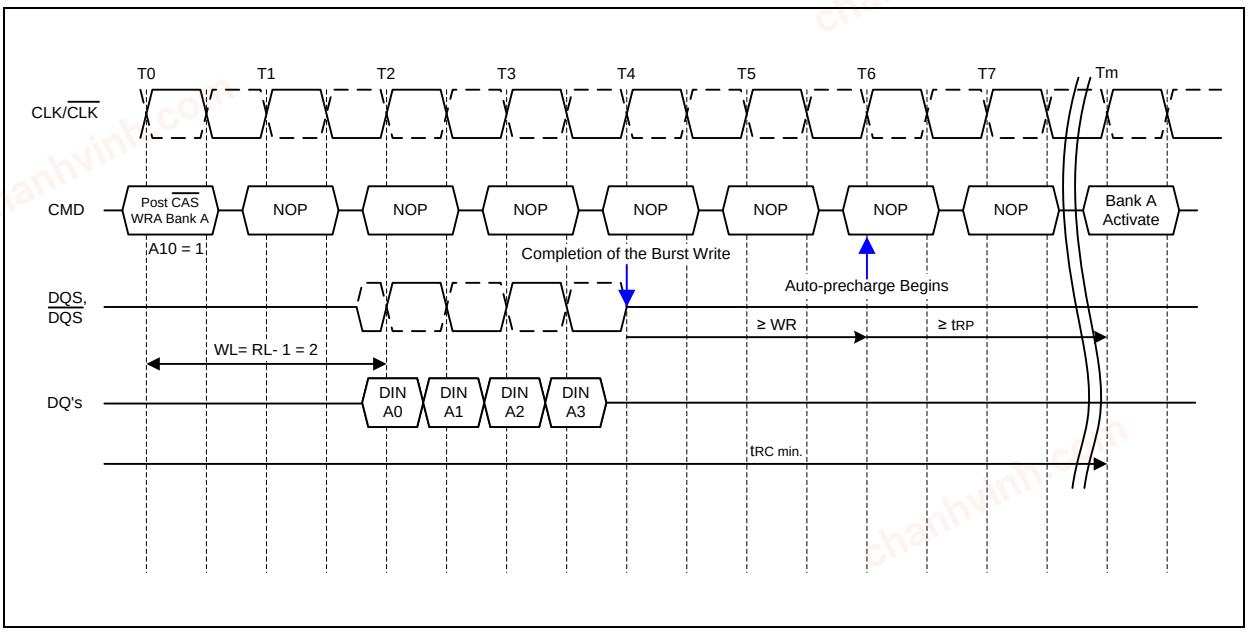


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11.25 Burst read with Auto-precharge followed by an activation to the same bank (tRP Limit): RL=5 (AL=2, CL=3, internal tRCD=3, BL=4, tRTP ≤ 2clks)

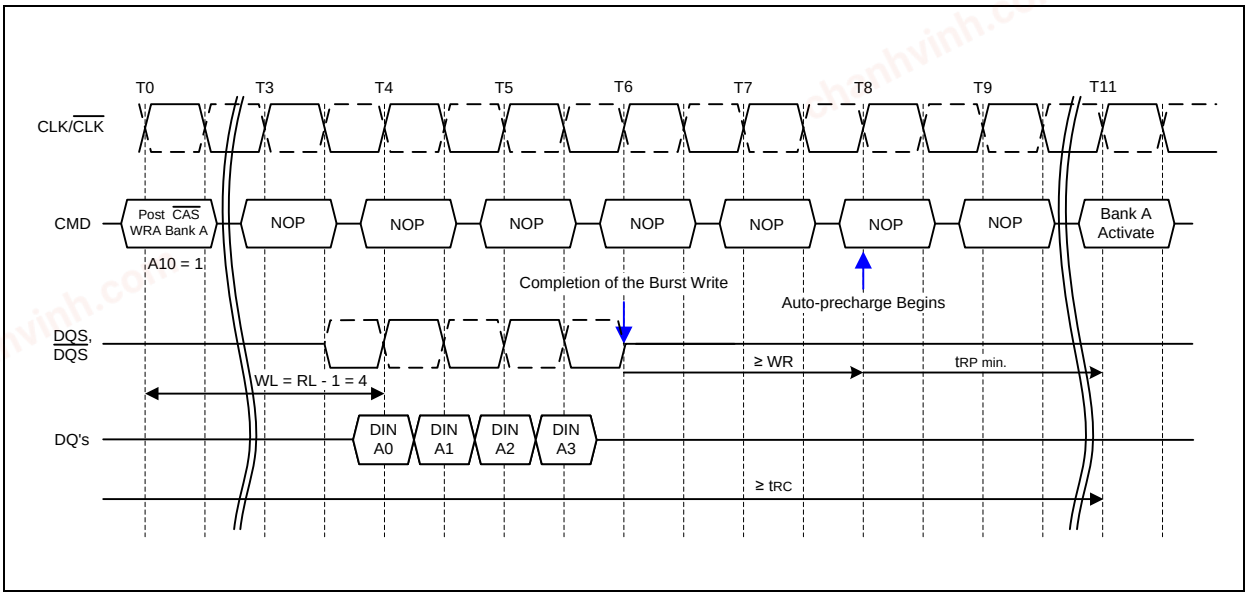


11.26 Burst write with Auto-precharge (tRC Limit): WL=2, WR=2, BL=4, tRP=3

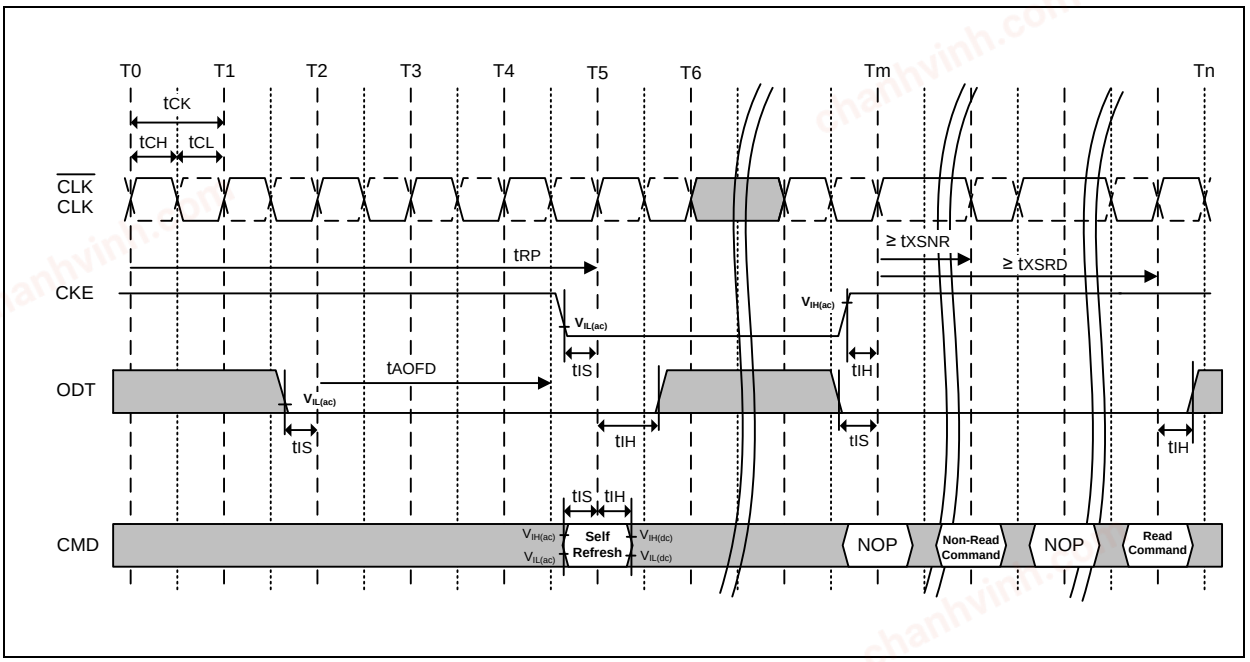


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11.27 Burst write with Auto-precharge (WR + tRP Limit): WL=4, WR=2, BL=4, tRP=3



11.28 Self Refresh Timing

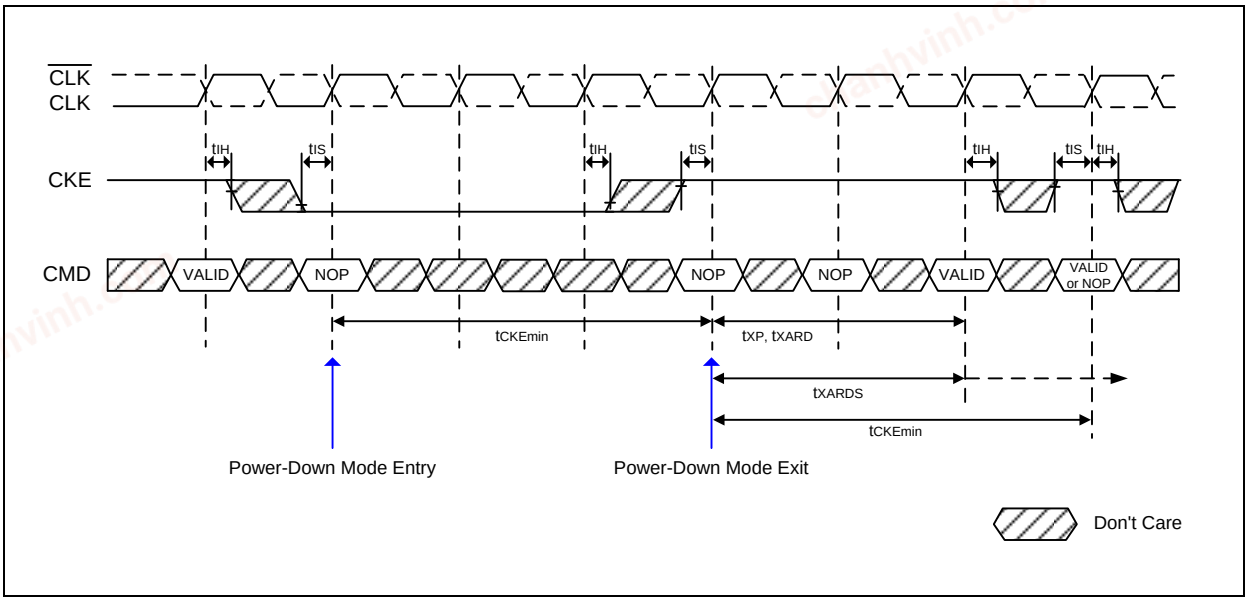


Notes:

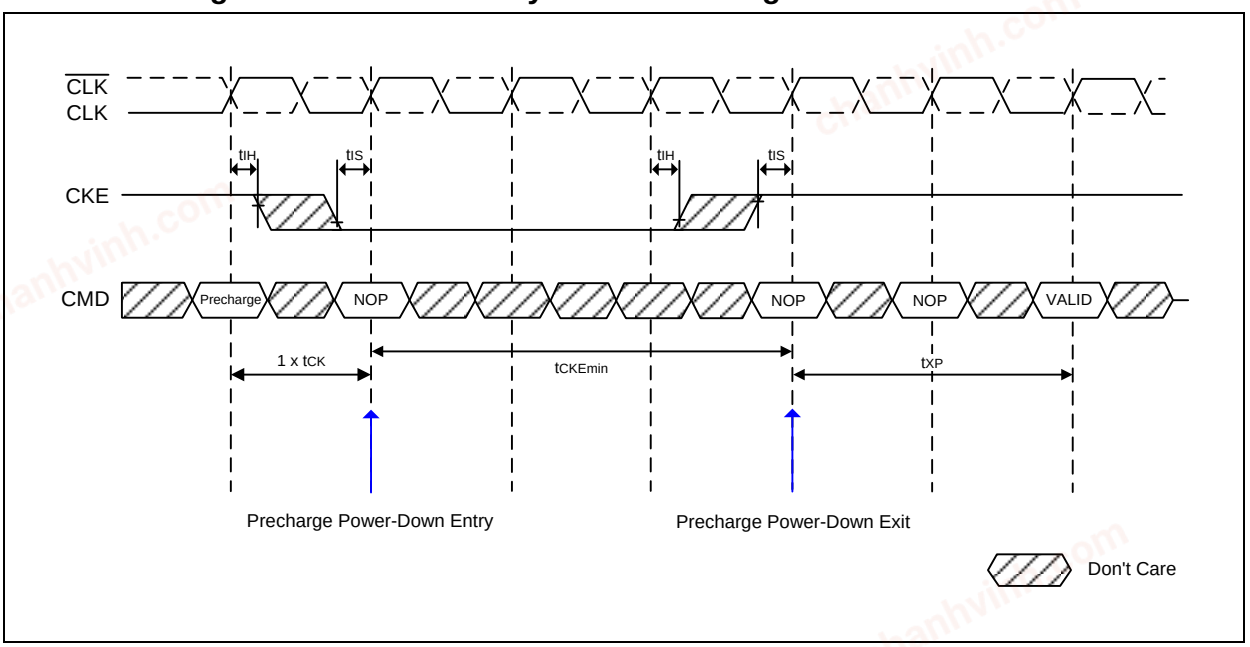
1. Device must be in the “All banks idle” state prior to entering Self Refresh mode.
2. ODT must be turned off tAOFD before entering Self Refresh mode, and can be turned on again when tXSRD timing is satisfied.
3. tXSRD is applied for a Read or a Read with Auto-precharge command. tXSNR is applied for any command except a Read or a Read with Auto-precharge command.

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11.29 Basic Power Down Entry and Exit Timing

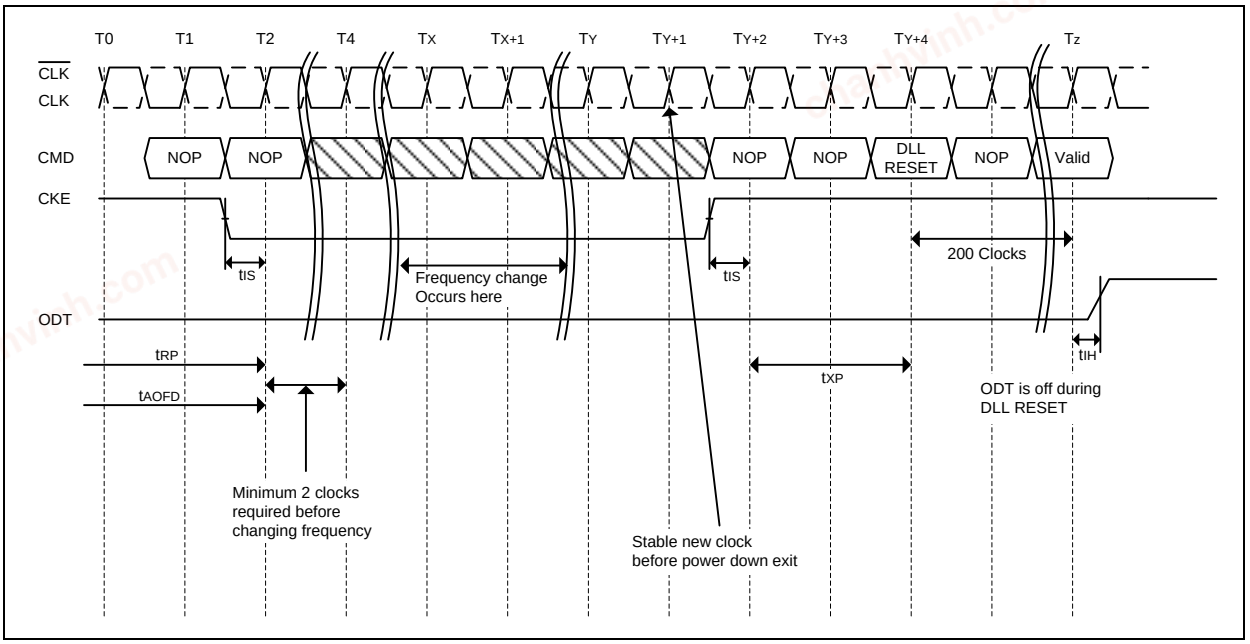


11.30 Precharged Power Down Entry and Exit Timing



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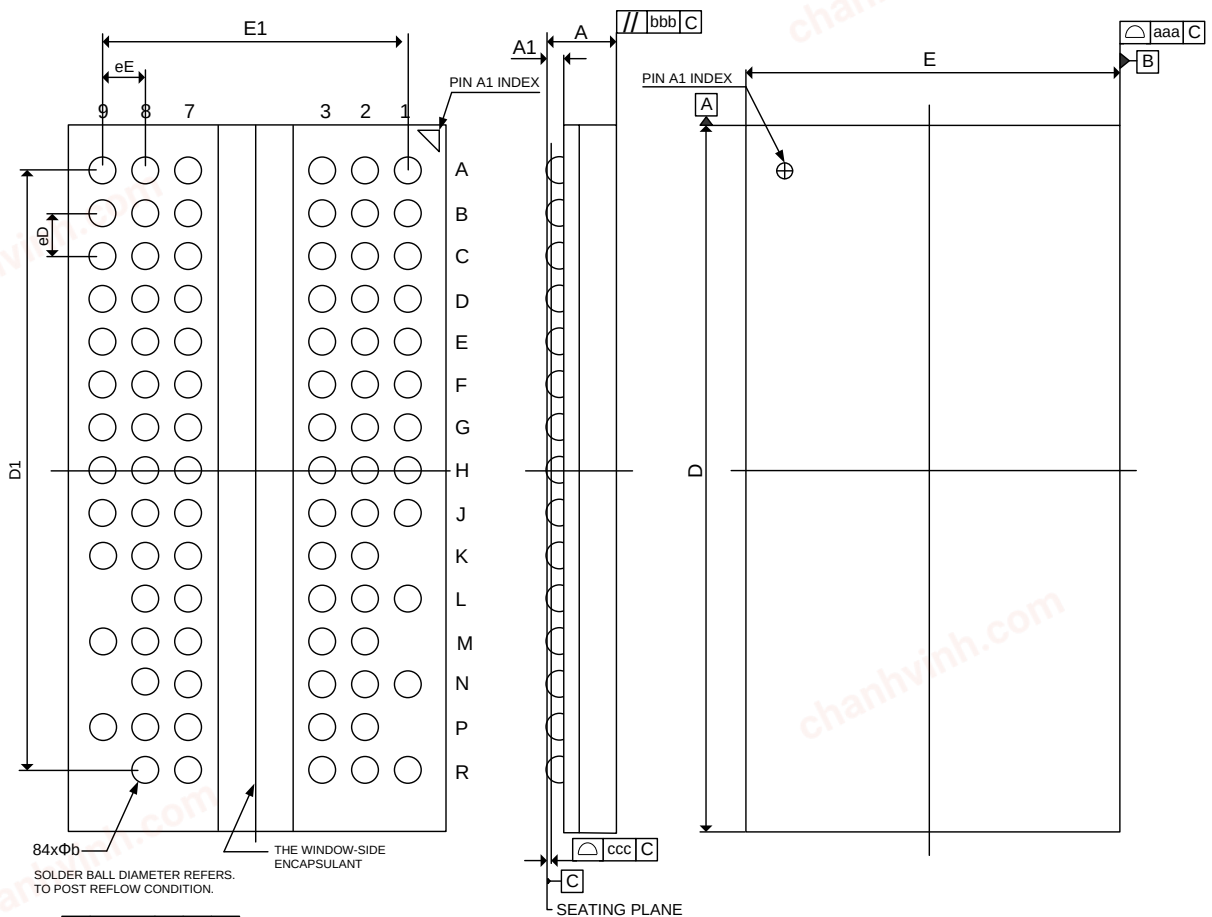
11.31 Clock frequency change in precharge Power Down mode



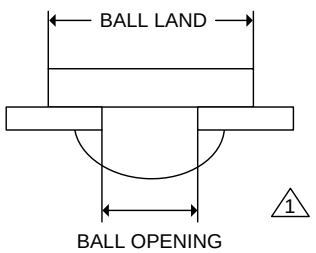
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12. PACKAGE SPECIFICATION

Package Outline VFBGA84 Ball (8x12.5 mm², Ball pitch: 0.8mm) - (Window BGA Type)



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.86	0.93	1.00
A1	0.25	---	0.40
b	0.40	---	0.50
D	12.40	12.50	12.60
E	7.90	8.00	8.10
D1	11.20 BSC.		
E1	6.40 BSC.		
eE	0.80 BSC.		
eD	0.80 BSC.		
aaa	---	---	0.15
bbb	---	---	0.20
ccc	---	---	0.10
ddd	---	---	0.15
eee	---	---	0.08



Note:
1. Ball land: 0.5mm, Ball opening: 0.4mm, PCB Ball land suggested ≤ 0.4mm

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13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	Aug. 11, 2020	All	Initial formal datasheet
A02	Dec. 02, 2020	5, 42, 43, 45	Revise t_{RAS} min. value from 45nS to 40nS
		43, 45	Revise $t_{CH(avg)}$ & $t_{CL(avg)}$ min./max. value from 0.48 $t_{CK(avg)}$/0.52 $t_{CK(avg)}$ to 0.45 $t_{CK(avg)}$/0.55 $t_{CK(avg)}$

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