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SMD PTC Thermistors, Inrush Current Limiter



LINKS TO ADDITIONAL RESOURCES

3D Models | Design Tools | SPICE Models

QUICK REFERENCE DATA		
PARAMETER (1)	VALUE	UNIT
Resistance at 25 °C (R_{25}) (2)	60 to 1000	Ω
Switching temperature	135, 165	°C
Maximum inrush current	10 to 40	A
Maximum AC voltage (2)	350 to 700	V_{RMS}
Maximum DC voltage (2)	500 to 1200	V_{DC}
Maximum peak voltage (3)	4000	V_P
Minimum dielectric withstanding voltage between terminals and housing	3000	V_{AC}
Maximum energy at 25 °C (typical)	240, 300	J
Operating temperature range	-40 to 105	°C
Storage temperature range	-40 to 175	°C
Dissipation factor (typical)	16	mW/K
Thermal time constant (τ_{th}) (typical by still air cooling)	260	s
Weight	8.5	g

Notes

(1) Definitions, measurements, and tests are made in accordance with standard IEC 60738-1 “Thermistors - Directly heated positive temperature coefficient” and AEC-Q200 stress test qualification for passive components

(2) Other resistance values and maximum operating voltages available on request.
Matched resistance values available on request

(3) Maximum peak voltages are based on 8/20 µs pulses that can be applied with limited none-switching energy

FEATURES

- Standard 240 J and high energy 300 J available
- High number of inrush-power cycles: > 100 000 cycles
- Suitable for reflow soldering
- Can handle high direct voltage up to 1200 V
- Highly resistant against shock and vibration
- Insulated housing up to 3 kV_{AC}
- Self protecting in case of overload with no risk of over-heating
- AEC-Q200 qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb e3 RoHS COMPLIANT HALOGEN FREE

APPLICATIONS

Inrush current limiting and energy-dump resistor in:

- AC/DC and DC/DC converters
- Energy dump and DC-Link circuits
- Emergency discharge circuits
- OBC, battery charging equipment
- Motor drives

PTCES thermistors have resistance values that can change instantly based on the applied voltage levels and varying body temperatures.

DESCRIPTION

These directly heated ceramic-based doped barium titanate thermistors have a positive temperature coefficient and are primarily intended for inrush current limiting and overload protection. They consist of a solder connected homogeneous ceramic PTC encapsulated in a UL 94 V-0 approved PPS-GF housing. The part is laser marked with the Vishay logo, R25 value, date code YYWW, and ES for PTCES17, or HES for PTCES67.

MOUNTING

Important mounting and handling instructions, see:

www.vishay.com/doc?29260

By reflow soldering in any position.

Not intended for potting or sealing.

Maximum surface temperature in case of overload can reach 180 °C.

PACKAGING

PTCES thermistors are available in tape on reel 350 pieces.

For technical questions, contact: nlr@vishay.com

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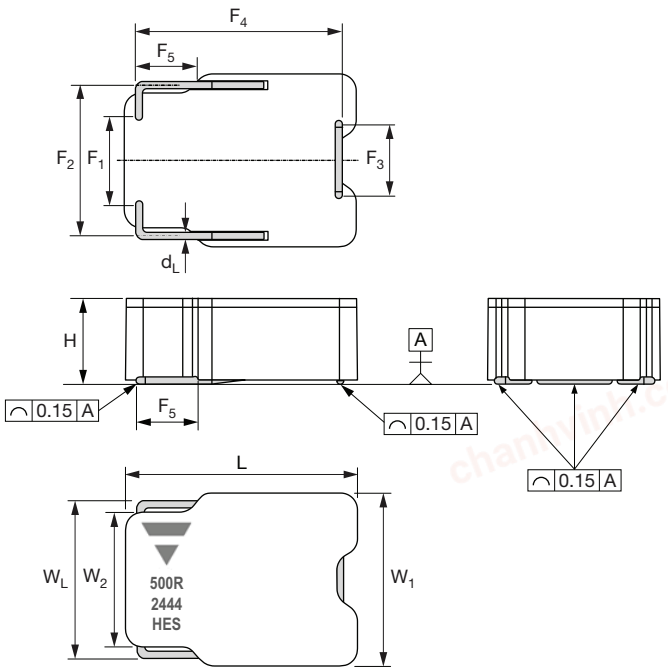
ELECTRICAL DATA AND ORDERING INFORMATION

PART NUMBER	R_{25} (Ω)	R_{25} TOL. (%)	$V_{MAX.}$ (V_{RMS})	$V_{LINK\ MAX.}$ (V_{DC})	$R_{MIN.}$ < 1.5 V_{DC} (Ω)	I_{HOLD} AT 25 °C (mA) (1)	C_{th} (J/K) (1)	ENERGY 1 CYCLE AT 25 °C (J) (1)	τ_{th} (s) (1)	WEIGHT (g)
PTCES17R600MTE	60	30	440	625	32	125	2.4	240	260	8.2
PTCES17R121NTE	120	30	460	650	64	90	2.4	240	260	8.2
PTCES17R251STE	250	30	600	850	130	63	2.4	240	260	8.2
PTCES17R501TTE	500	30	700	1000	260	45	2.4	230	260	8.2
PTCES17R102UTE	1000	30	700	1200	500	32	2.4	230	260	8.2
PTCES67R151NTE	150	30	460	650	65	92	2.6	300	260	8.2
PTCES67R251STE	250	30	600	850	105	71	2.6	300	260	8.2
PTCES67R501TTE	500	30	700	1000	200	50	2.6	300	260	8.2

Note

(1) Typical values for information, are temperature or mounting dependent

OUTLINE AND DIMENSIONS

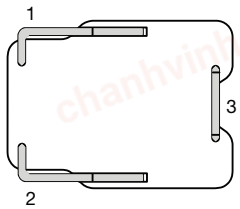


COMPONENT DIMENSIONS in millimeters	
SYMBOL	PTCES
L	26.2 ± 0.3
W_1	19.5 ± 0.3
W_2	15.1 ± 0.3
W_L	17.8 ± 0.35
H	9.6 ± 0.3
d_L	0.8 ± 0.05 (Ø)
F_1	10.0 ± 0.2
F_2	17.0 ± 0.3
F_3	8.0 ± 0.2
F_4	23.3 ± 0.4
F_5	7.0 ± 0.3

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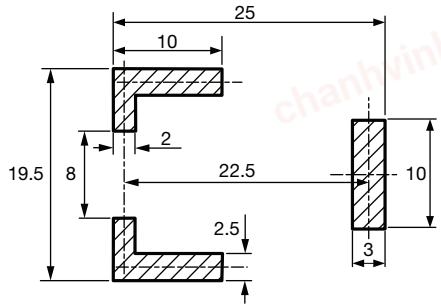
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PINOUT INFORMATION



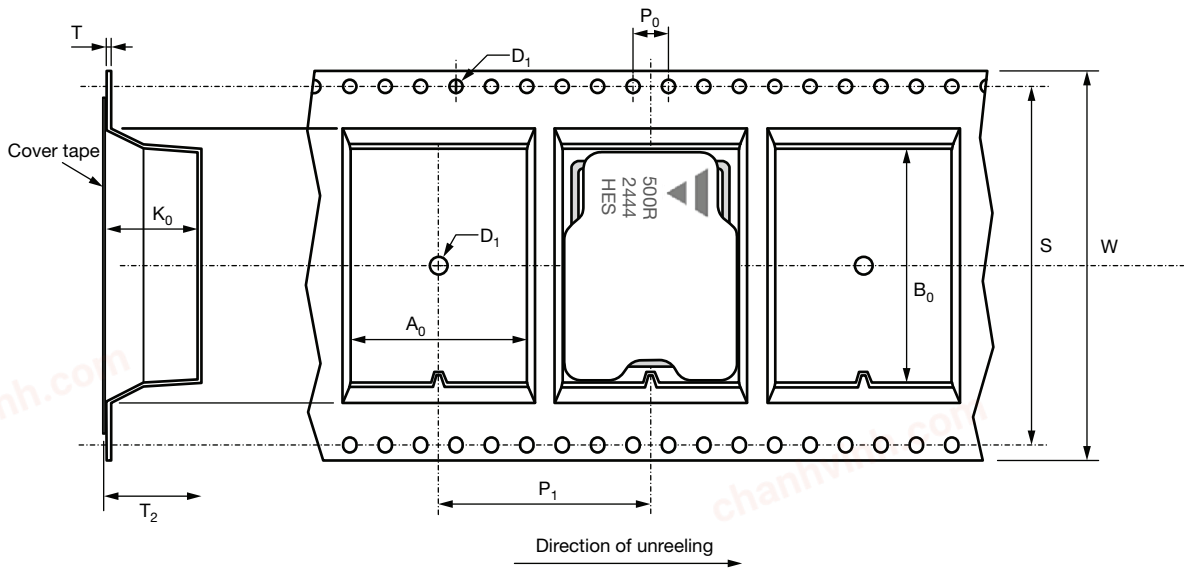
PIN 1 - Electrical connection
PIN 2 - Electrical connection
PIN 3 - Mechanical connection only. No electrical connection

SOLDER LAND PATTERN AND DIMENSIONS



TAPE AND REEL DIMENSIONS

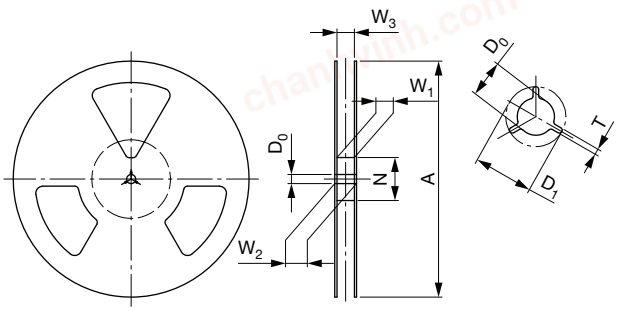
Taping on reel according to IEC 60286-3 on 44.0 mm tape width.



TAPE DIMENSIONS in millimeters		
SYMBOL	**PARAMETER**	**VALUE**
A_0	Pocket width	19.9 ± 0.1
B_0	Pocket length	26.4 ± 0.1
K_0	Pocket depth	10.4 ± 0.1
W	Tape width	44.0 ± 0.3
T	Tape thickness	0.5 ± 0.1
T_2	Total thickness	10.8 ± 0.3
P_1	Component pitch	24.0 ± 0.1
P_0	Sprocket hole pitch	4.0 ± 0.1

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Dimension according to IEC EN 60286-3

REEL DIMENSIONS in millimeters		
SYMBOL	**PARAMETER**	**VALUE**
D_0	Reel hole inner diameter	12.8 min.
D_1	Reel hole outer diameter	21.1 min.
T	Notch width	2.0 min.
N	Hub diameter	100
A	Reel diameter	380
W_1	Reel inner width (at hub)	44.4 min.
W_2	Reel outer width (at hub)	50.4 max.
W_3	Reel inner width (at flange)	50.4 max.

REQUIRED NUMBER OF PTC THERMISTORS TO LIMIT CURRENT AND ABSORB ENERGY

By using several PTC's in a series / parallel network, the maximum current limitation and absorbed energy levels can be further optimized. For homogeneous current and energy distribution it is recommended to combine only PTCES of the same nominal resistance value. Energy absorption per PTC in a network depends on current distribution in the network and as such on the individual PTC resistance value. PTCES thermistors might be used in a series connection to further lower the inrush current, but not to increase the maximum allowed voltage levels. PTCES thermistors placed in series can have a reduced energy handling depending on their resistance values. Following formula may be used to calculate the minimum number of PTCES thermistors of the same resistance value that are required in a DC link or other capacitor bank application to properly charge or discharge a given amount of non-repetitive energy without follow current. The formula is valid for one charge or discharge operation within cool down period of at least 5 times the thermal time constant and for which the T_{PTC} equals the T_{amb} before a consecutive operation. To make a better evaluation of which PTCES type and how many parts would be needed for a specific circuit and operating mode, it is advisable to use the available SPICE models and simulate the circuit application.

$$N \geq \frac{K \times C \times V^2}{2 \times C_{th} \times (T_{sw} - T_{amb})}$$

Notes

- N is the number of PTCEL required in the network
- C is the total capacitor value to charge or discharge in [F]
- V is the maximum DC voltage on the capacitor C
- C_{th} is the typical thermal capacity of one PTC in [J/K] (see table)
- T_{sw} is the minimum switching temperature of the PTCES type (130 °C for PTCES17, 155 °C for PTCES67)
- T_{amb} is the maximum ambient temperature at which the PTC needs to operate
- K is the factor that determines the charging operation mode
  K = 1 for DC ICL charging or discharging
  K = 0.94 for 3-phase ICL charging
  K = 0.84 for 2 out of 3-phase ICL charging
  K = 0.76 for single phase ICL charging

The different charging operating modes are expressed in the circuit drawings on page 5.

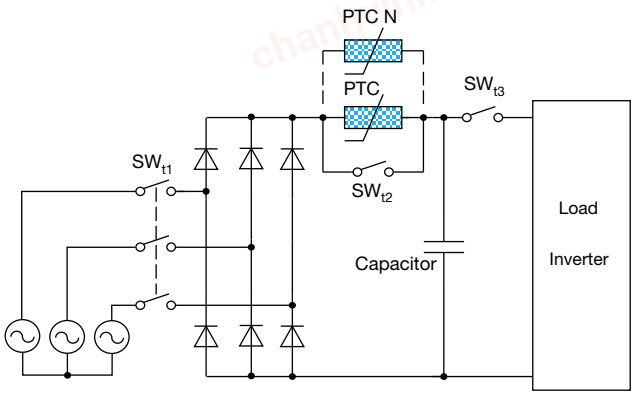
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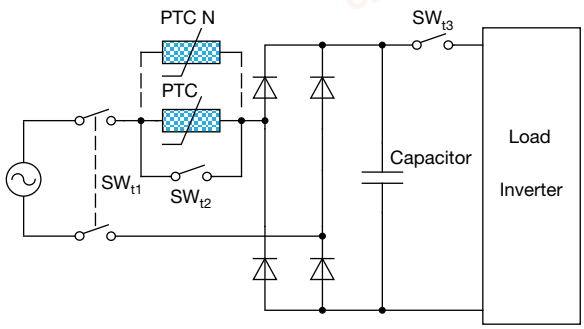
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DIFFERENT ICL CIRCUITS USING PTCES(L) AT DIFFERENT POSSIBLE POSITIONS

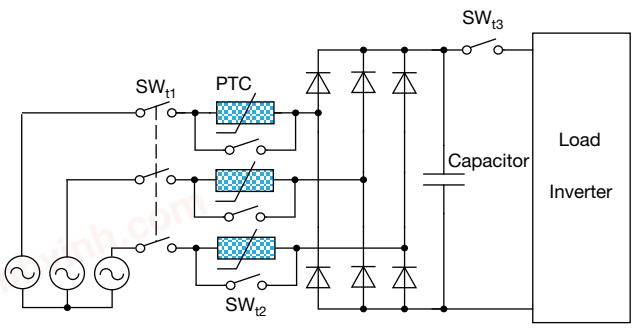
3 Phase - PTC(s) After Bridge (K = 0.94)



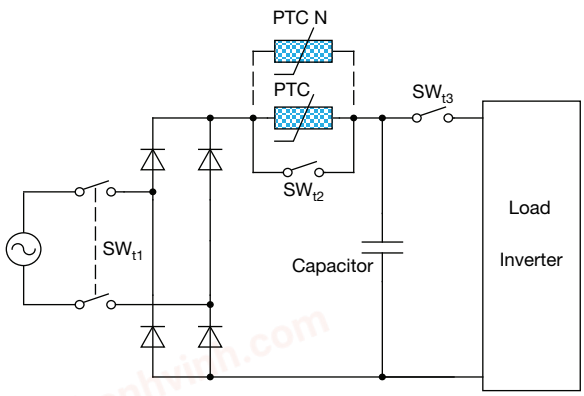
1 Phase - PTC(s) Before Bridge (K = 0.76)



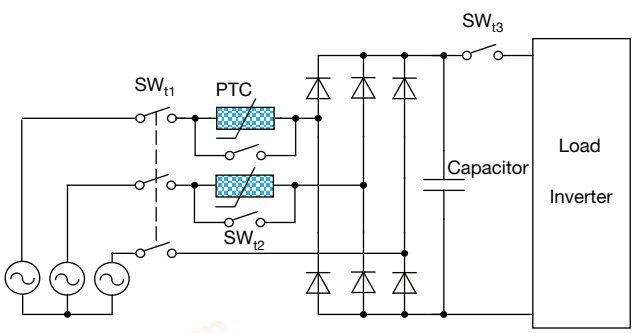
3 Phase - PTC(s) Before Bridge 3 Phases (K = 0.94)



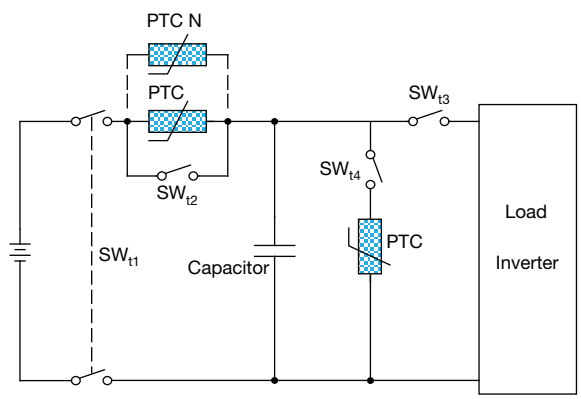
1 Phase - PTC(s) After Bridge (K = 0.76)



3 Phase - PTC(s) Before Bridge 2 Phases (K = 0.84)



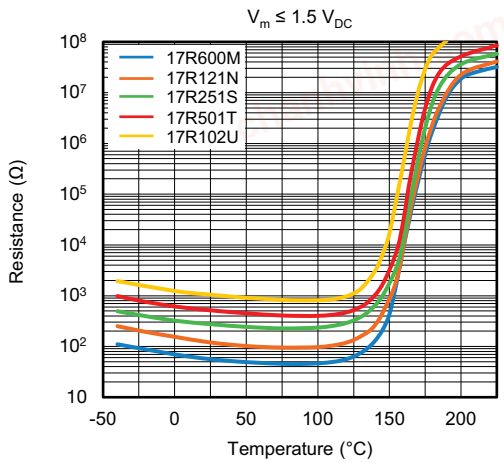
DC - PTC Charge And / Or Discharge (K = 1.00)

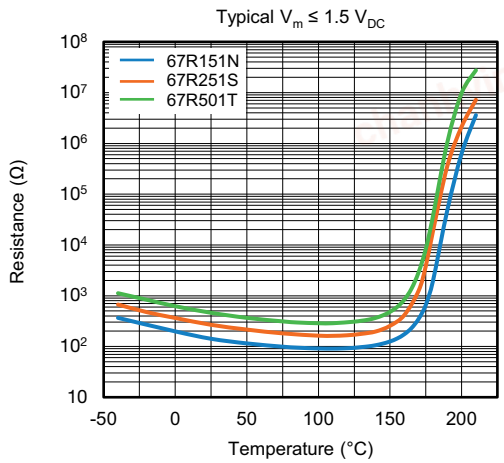


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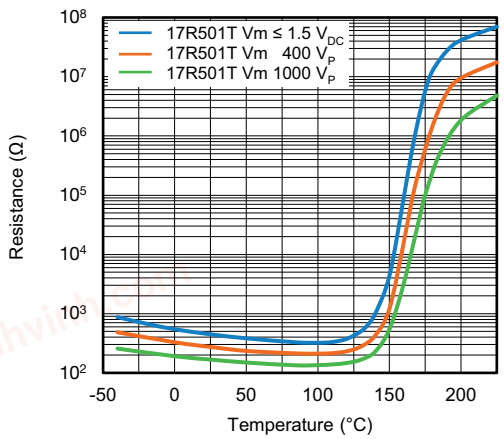
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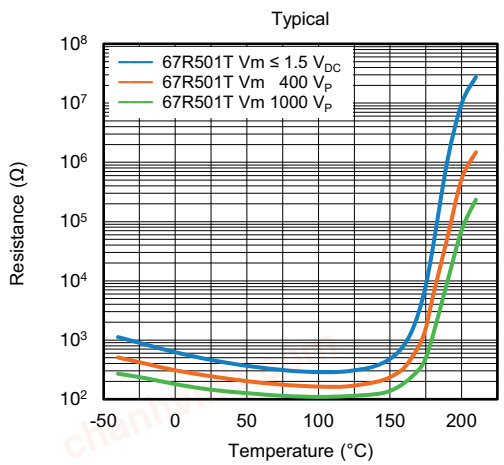
RESISTANCE VS. TEMPERATURE





RESISTANCE VS. TEMPERATURE PULSED





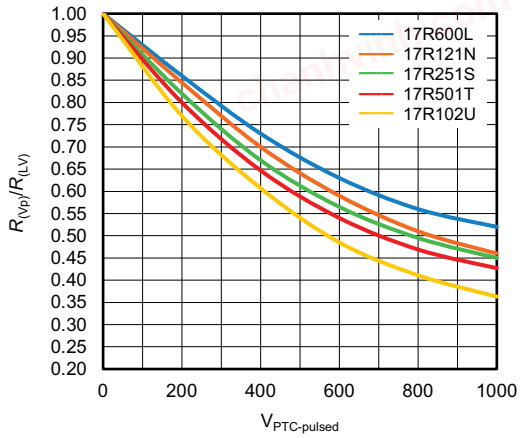
Notes

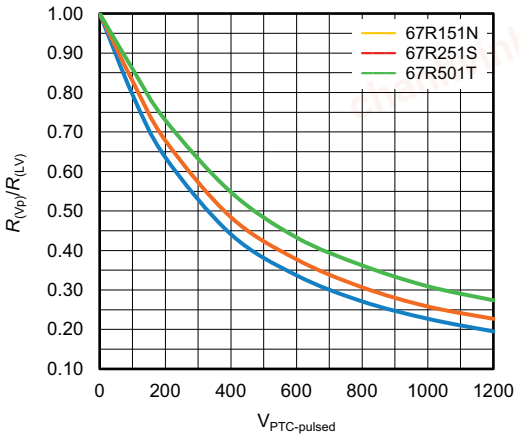
- The minimum PTC resistance values under (pulsed) voltage are depending on actual minimum resistance value in the temperature range of 80 °C to 120 °C. The actual voltage dependency effect or $R_{(VP)}/R_{(LV)}$ ratio (see page 6) of ceramic PTC is depending on its resistance values at low voltage ($R_{(LV)}$) and the applied pulsed voltage. The different curves (on top of page 6) represent the influence of (pulsed) voltage related to some typical PTC resistance values at any temperature below 150 °C. A PTC resistance value $R_{(LV)}$ can be taken from the Resistance vs Temperature graphs and multiplied by a corresponding ratio to estimate the (minimum) resistance value and determine a maximum peak current at a defined voltage. Actual peak currents that could be reached at certain voltage levels can be more precisely evaluated by using the available SPICE models
- The graphs “Resistance vs. temperature pulsed” on a PTCES17R501T and a PTCES67R501T above, are examples of pulsed voltage RT curves, where the voltage is applied in short pulses with low energy (< 1 J) to prevent self heating of the PTC ceramic pellet

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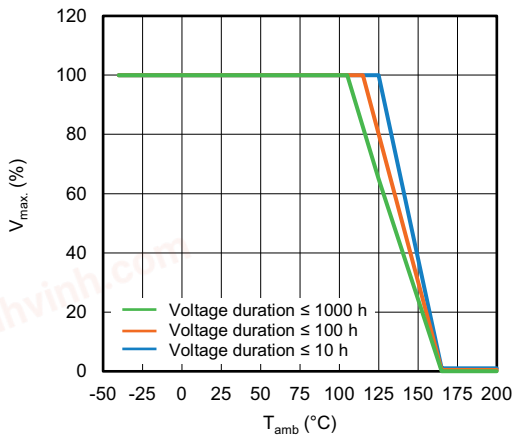
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PTC RESISTANCE UNDER PULSED VOLTAGE

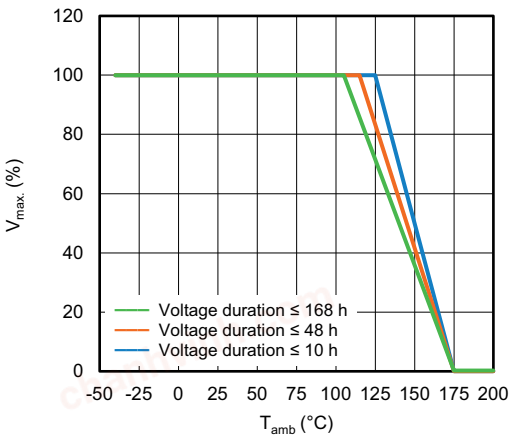




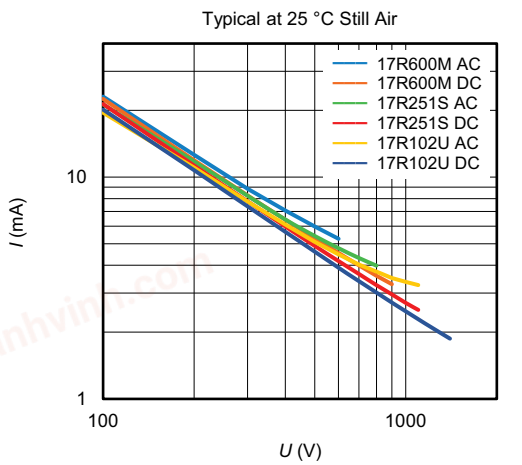
$V_{max.}$ DERATING VS. T_{amb} FOR PTCES17



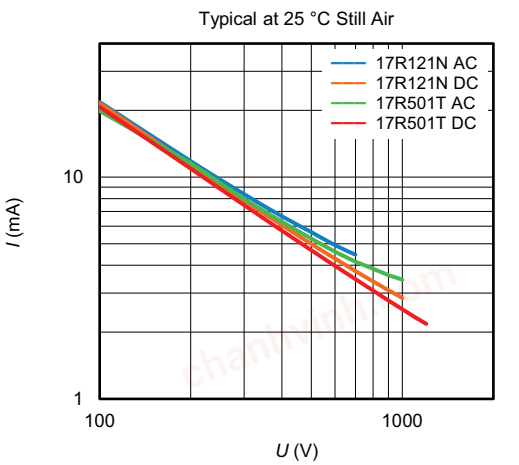
$V_{max.}$ DERATING VS. T_{amb} FOR PTCES67



RESIDUAL CURRENT VS. VOLTAGE FOR PTCES17 V_{AC} / V_{DC}



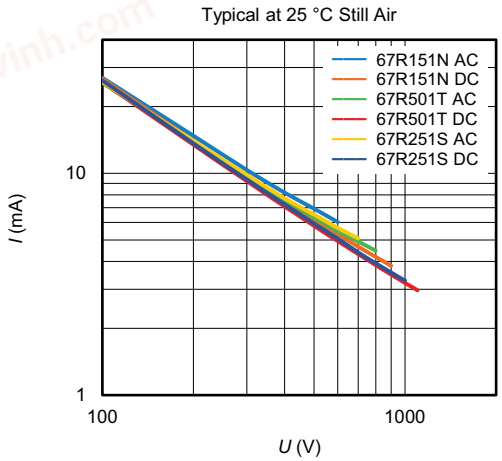
RESIDUAL CURRENT VS. VOLTAGE FOR PTCES17 V_{AC} / V_{DC}



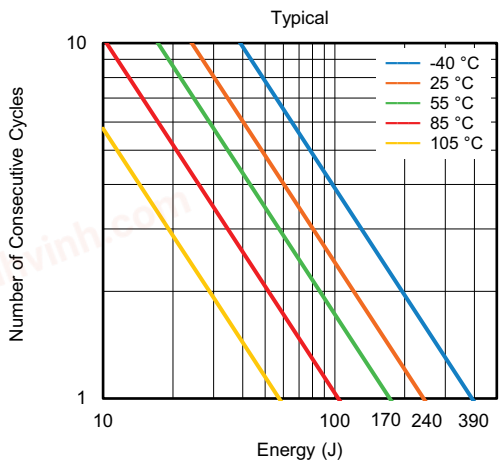
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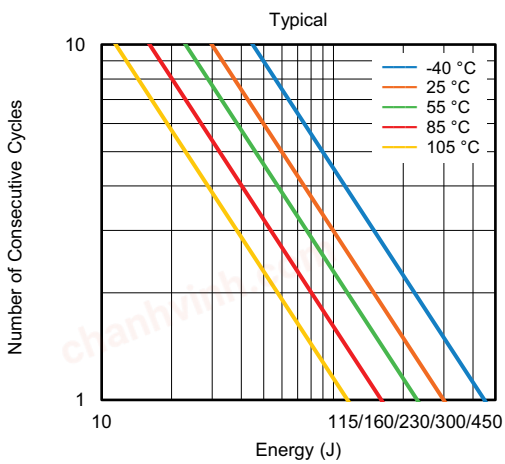
RESIDUAL CURRENT VS. VOLTAGE FOR PTCES67 V_{AC} / V_{DC}



CONSECUTIVE ENERGY CYCLES AT DIFFERENT T_{amb} FOR PTCES17



CONSECUTIVE ENERGY CYCLES AT DIFFERENT T_{amb} FOR PTCES67



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