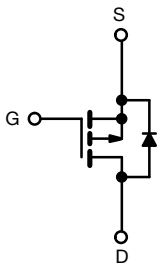
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Power MOSFET

TO-220 FULLPAK





P-Channel MOSFET

FEATURES

- Isolated package
- High voltage isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to lead creepage distance = 4.8 mm
- P-channel
- 175 °C operating temperature
- Dynamic dV/dt rating
- Low thermal resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

PRODUCT SUMMARY		
V_{DS} (V)	-100	
$R_{DS(on)}$ (Ω)	V_{GS} = -10 V	0.30
Q_g max. (nC)	38	
Q_{gs} (nC)	6.8	
Q_{gd} (nC)	21	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI9530GPbF

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	-100	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	-7.7	A
		T_C = 100 °C		-5.4	
Pulsed drain current [a]			I_{DM}	-31	
Linear derating factor				0.28	W/°C
Single pulse avalanche energy [b]			E_{AS}	380	mJ
Repetitive avalanche current [a]			I_{AR}	-7.7	A
Repetitive avalanche energy [a]			E_{AR}	4.2	mJ
Maximum power dissipation	T_C = 25 °C		P_D	42	W
Peak diode recovery dV/dt [c]			dV/dt	-5.5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d]	For 10 s			300	
Mounting torque	M3 screw			0.6	Nm

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = -25 V, starting T_J = 25 °C, L = 9.6 mH, R_G = 25 Ω, I_{AS} = -7.7 A (see fig. 12)
c. I_{SD} ≤ -7.7 A, dI/dt ≤ 140 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C
d. 1.6 mm from case

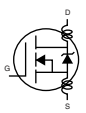
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THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	65	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	3.6	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-ssource breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	-100	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	-0.10	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	-2.0	-	-4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = -100 V, V_{GS} = 0 V	-	-	-100	µA
		V_{DS} = -80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	-500	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = -10 V; I_D = -4.6 A [b]	-	-	0.30	Ω
Forward transconductance	g_{fs}	V_{DS} = -50 V, I_D = -4.6 A [b]	3.4	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz, see fig. 5	-	860	-	pF
Output capacitance	C_{oss}		-	340	-	
Reverse transfer capacitance	C_{rss}		-	93	-	
Drain to sink capacitance	C	f = 1.0 MHz	-	12	-	
Total gate charge	Q_g	V_{GS} = -10 V; I_D = -12 A, V_{DS} = -80 V, see fig. 6 and 13 [b]	-	-	38	nC
Gate-source charge	Q_{gs}		-	-	6.8	
Gate-drain charge	Q_{gd}		-	-	21	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -50 V, I_D = -12 A, R_G = 12 Ω, R_D = 3.9 Ω, see fig. 10 [b]	-	12	-	ns
Rise time	t_r		-	52	-	
Turn-off delay time	$t_{d(off)}$		-	31	-	
Fall time	t_f		-	39	-	
Gate input resistance	R_g	f = 1 MHz, open drain	0.4	-	3.3	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	-7.7	A
Pulsed diode forward current [a]	I_{SM}		-	-	-31	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = -7.7 A, V_{GS} = 0 V [b]	-	-	-6.3	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = -12 A, dI/dt = 100 A/µs [b]	-	120	240	ns
Body diode reverse recovery charge	Q_{rr}		-	0.46	0.92	µC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

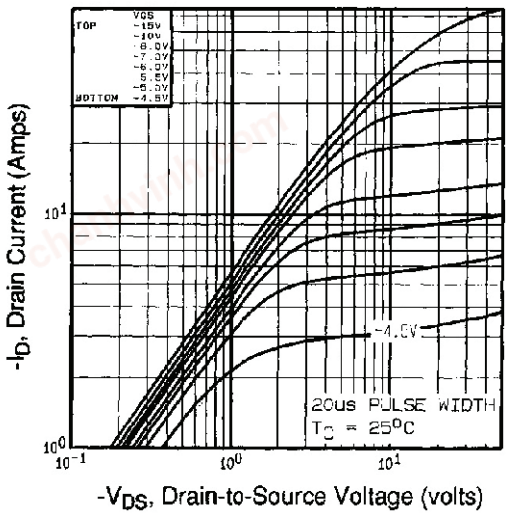


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

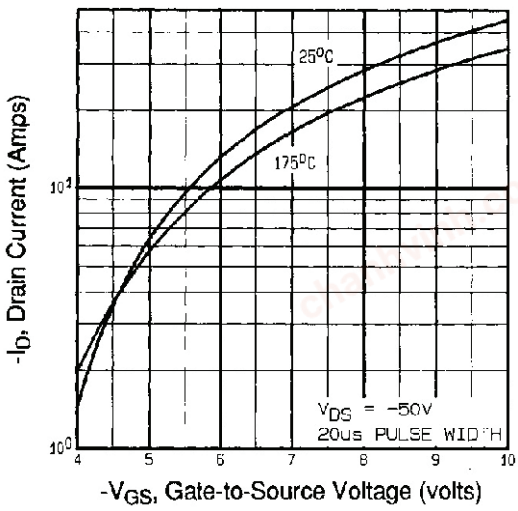


Fig. 3 - Typical Transfer Characteristics

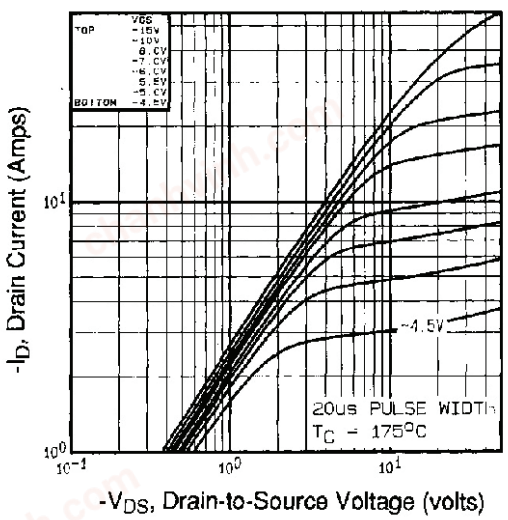


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

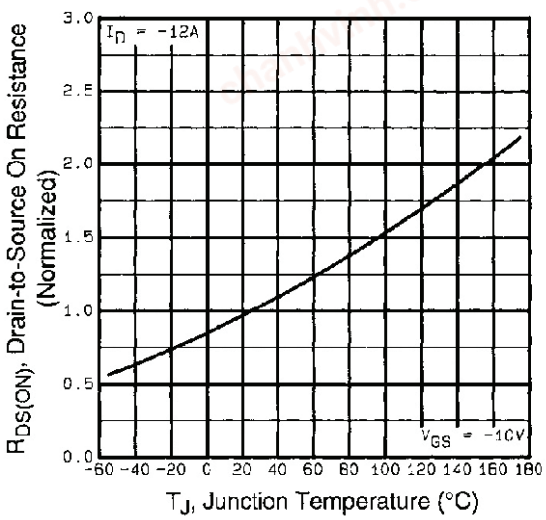


Fig. 4 - Normalized On-Resistance vs. Temperature

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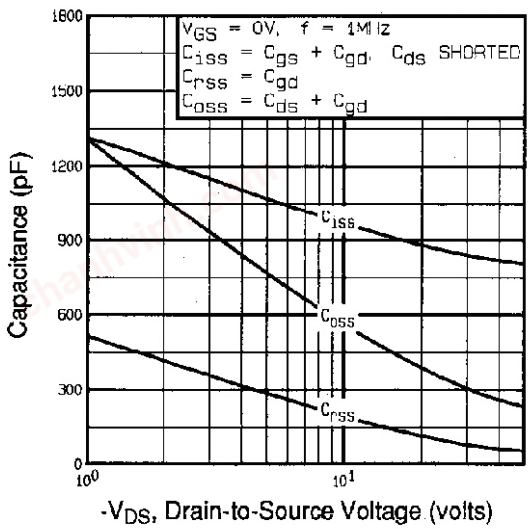


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

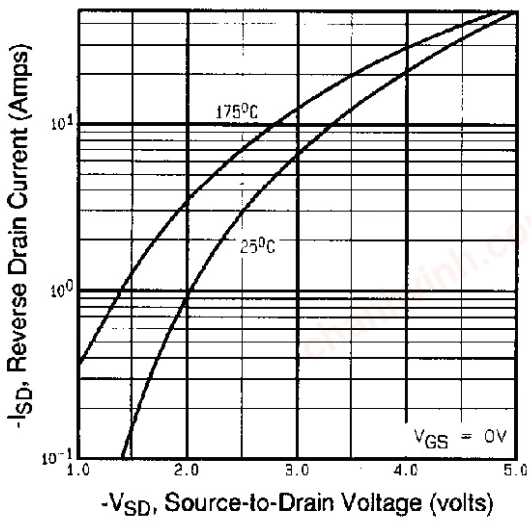


Fig. 7 - Typical Source-Drain Diode Forward Voltage

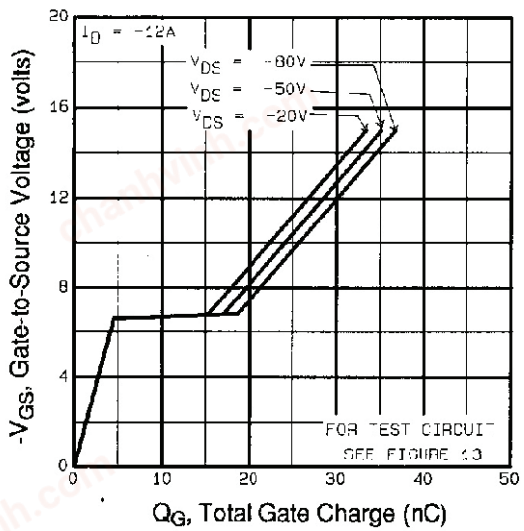


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

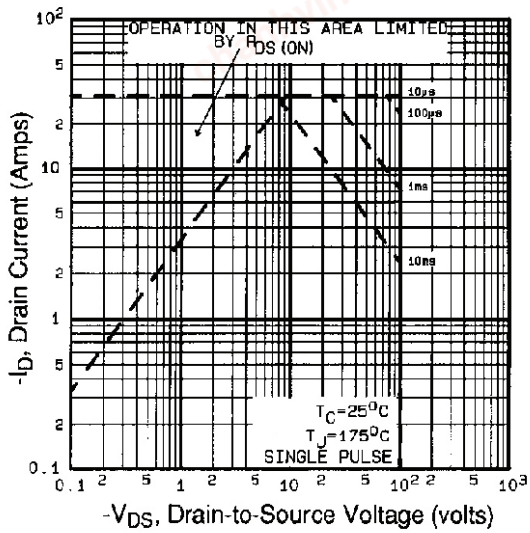


Fig. 8 - Maximum Safe Operating Area

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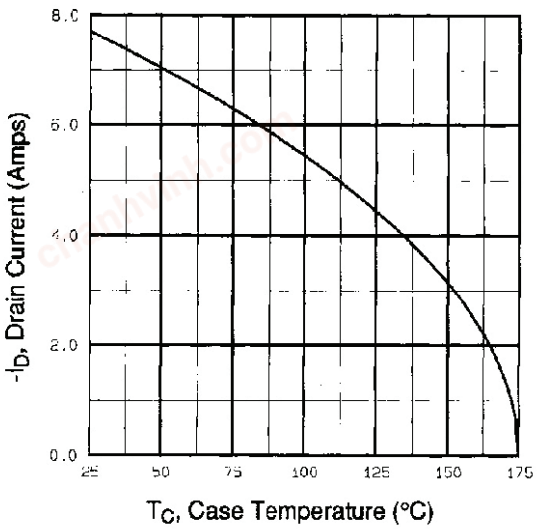


Fig. 9 - Maximum Drain Current vs. Case Temperature

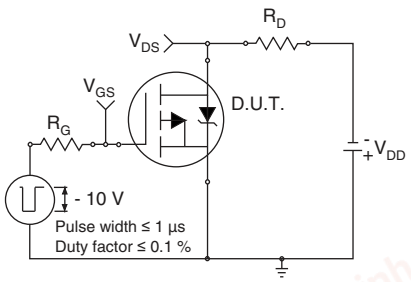


Fig. 10a - Switching Time Test Circuit

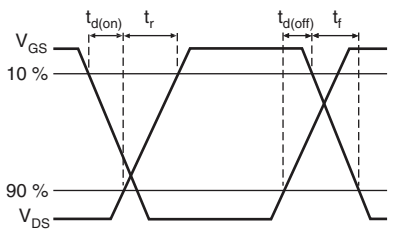


Fig. 10b - Switching Time Waveforms

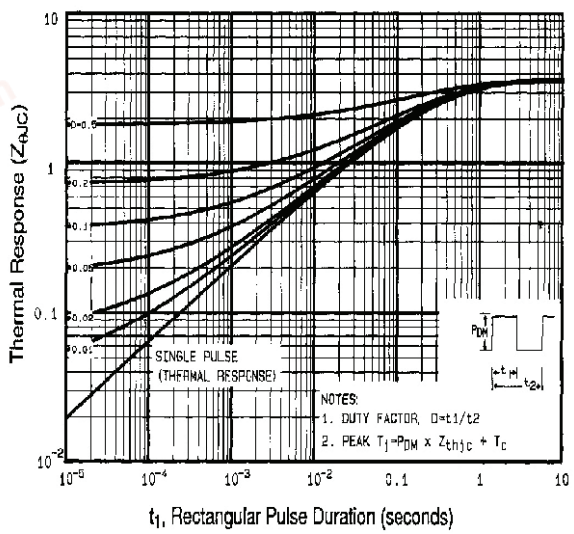


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

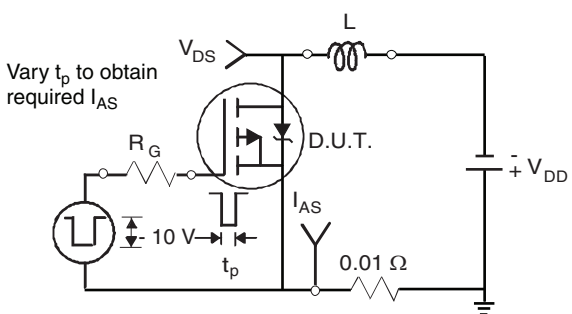


Fig. 12a - Unclamped Inductive Test Circuit

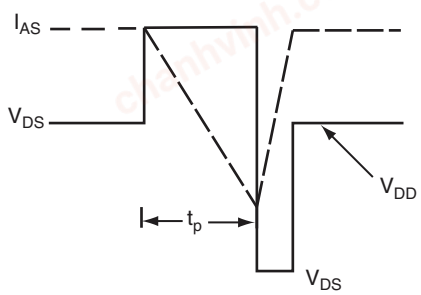


Fig. 12b - Unclamped Inductive Waveforms

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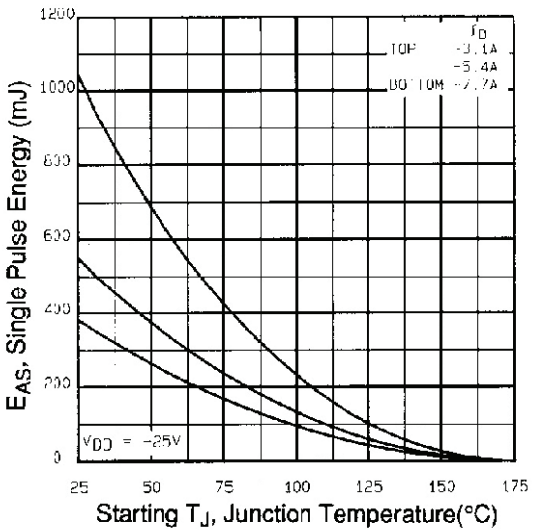


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

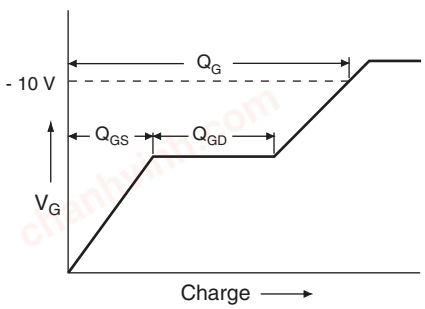


Fig. 13a - Basic Gate Charge Waveform

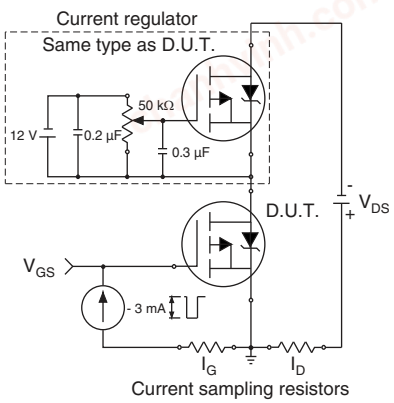


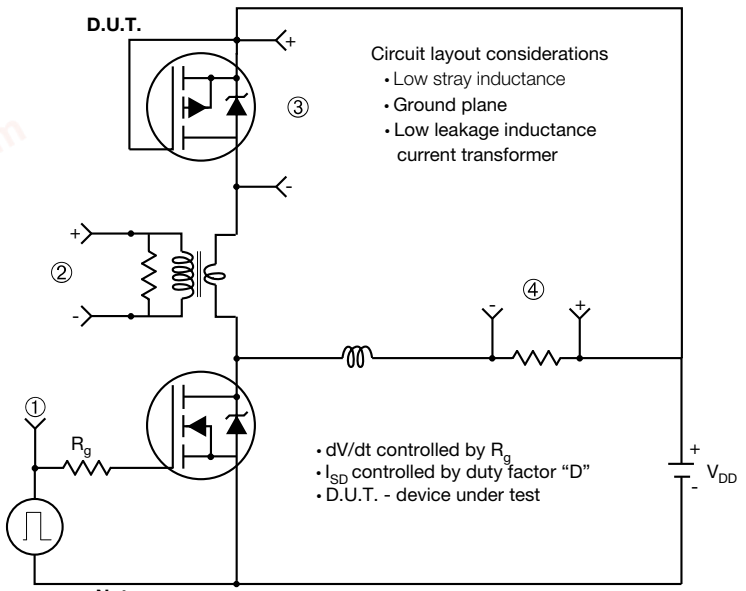
Fig. 13b - Gate Charge Test Circuit

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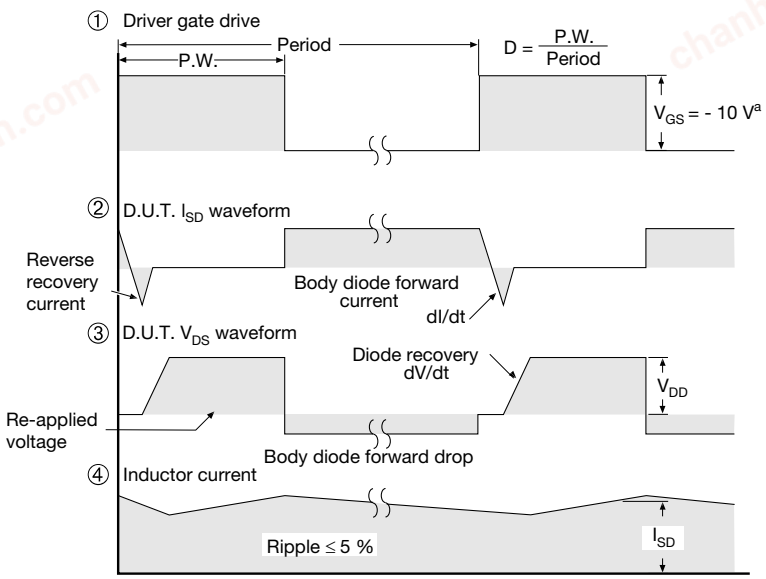
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Peak Diode Recovery dV/dt Test Circuit



Note
• Compliment N-Channel of D.U.T. for driver



Note
a. V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig.14 - For P-Channel

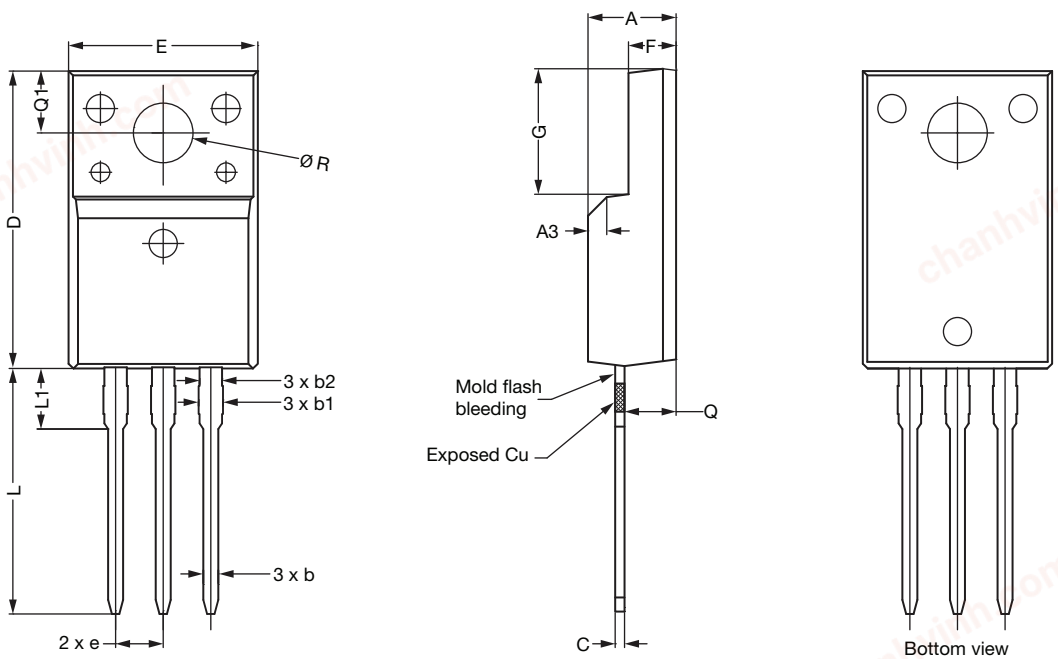
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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



	MILLIMETERS		
DIM.	**MIN.**	**NOM.**	**MAX.**
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e		2.54 BSC	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

Notes

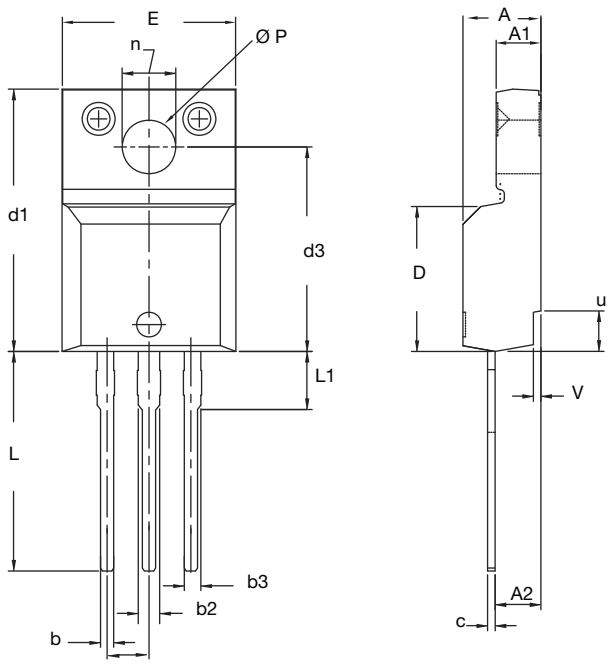
1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

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OPTION 2: FACILITY CODE = Y



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020
ECN: E19-0180-Rev. D, 08-Apr-2019 DWG: 5972				

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

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