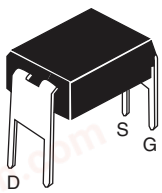
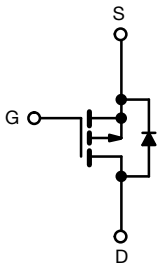
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Power MOSFET

HVMDIP





P-Channel MOSFET

FEATURES

- Dynamic dv/dt rating
- Repetitive avalanche rated
- For automatic Insertion
- End stackable
- P-channel
- 175 °C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

PRODUCT SUMMARY		
V_{DS} (V)	-100	
$R_{DS(on)}$ (Ω)	V_{GS} = -10 V	0.60
Q_g max. (nC)	18	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	9.0	
Configuration	Single	

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRFD9120PbF

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	-100	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at -10 V	T_A = 25 °C	I_D	-1.0	A
		T_A = 100 °C		-0.70	
Pulsed drain current [a]			I_{DM}	-8.0	
Linear derating factor				0.0083	W/°C
Single pulse avalanche energy [b]			E_{AS}	140	mJ
Repetitive avalanche current [a]			I_{AR}	-1.0	A
Repetitive avalanche energy [a]			E_{AR}	0.13	mJ
Maximum power dissipation	T_A = 25 °C		P_D	1.3	W
Peak diode recovery dv/dt [c]			dv/dt	-5.5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +175	°C
Soldering rRecommendations (peak temperature) [d]	For 10 s			300	

Notes

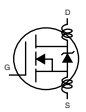
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = -25 V, starting T_J = 25 °C, L = 52 mH, R_g = 25 Ω, I_{AS} = -2.0 A (see fig. 12)
c. I_{SD} ≤ -6.8 A, di/dt ≤ 110 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C
d. 1.6 mm from case

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THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-100	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = -1 mA	-	-0.10	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-2.0	-	-4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = -100 V, V_{GS} = 0 V	-	-	-100	µA
		V_{DS} = -80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	-500	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -0.6 A [b]	-	-	0.60	Ω
Forward transconductance	g_{fs}	V_{DS} = -50 V, I_D = -0.60 A [b]	0.71	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz, see fig. 5	-	390	-	pF
Output capacitance	C_{oss}		-	170	-	
Reverse transfer capacitance	C_{rss}		-	45	-	
Total gate charge	Q_g	V_{GS} = -10 V, I_D = -6.8 A, V_{DS} = -80 V see fig. 6 and 13 [b]	-	-	18	nC
Gate-source charge	Q_{gs}		-	-	3.0	
Turn-on delay time	Q_{gd}		-	-	9.0	
Rise time	$t_{d(on)}$	V_{DD} = -50 V, I_D = -6.8 A, R_g = 18 Ω, R_D = 7.1 Ω, see fig. 10 [b]	-	9.6	-	ns
Turn-off delay time	t_r		-	29	-	
Fall time	$t_{d(off)}$		-	21	-	
Turn-on delay time	t_f		-	25	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.0	-	nH
Internal source inductance	L_S		-	6.0	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	-1.0	A
Pulsed diode forward current [a]	I_{SM}		-	-	-8.0	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = -1.0 A, V_{GS} = 0 V [b]	-	-	-6.3	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = -6.8 A, di/dt = 100 A/µs [b]	-	98	200	ns
Body diode reverse recovery charge	Q_{rr}		-	0.33	0.66	µC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

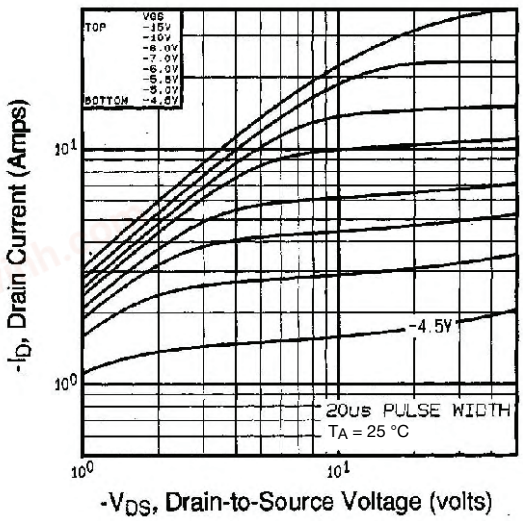


Fig. 1 - Typical Output Characteristics, T_A = 25 °C

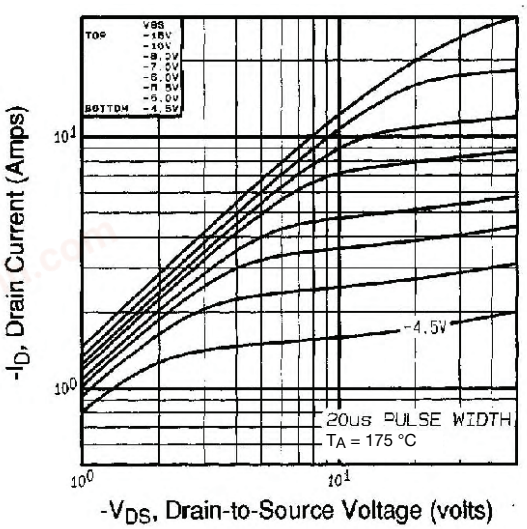


Fig. 2 - Typical Output Characteristics, T_A = 175 °C

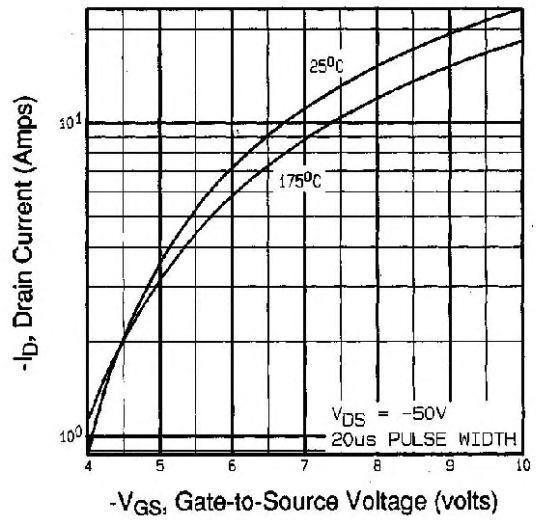


Fig. 3 - Typical Transfer Characteristics

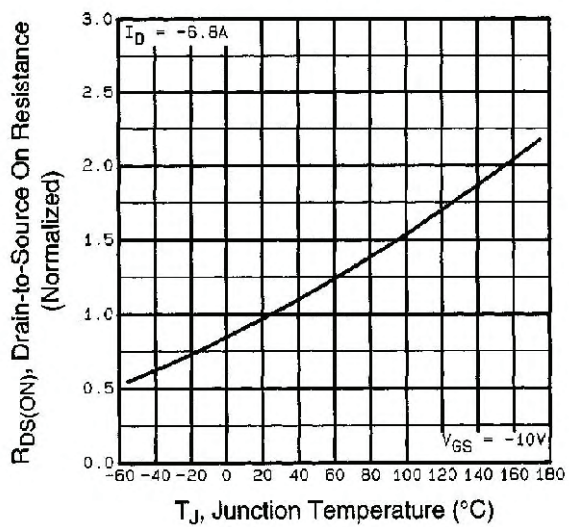


Fig. 4 - Normalized On-Resistance vs. Temperature

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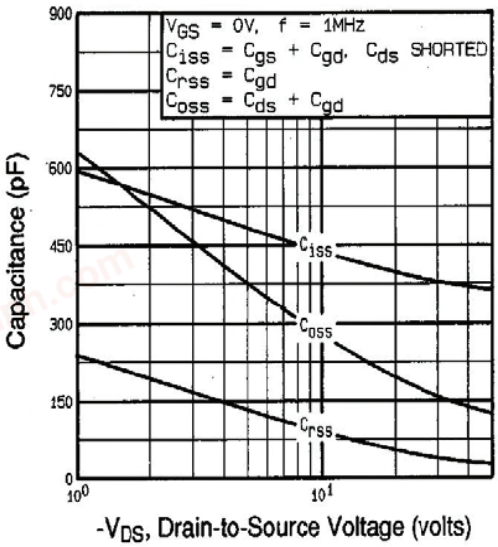


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

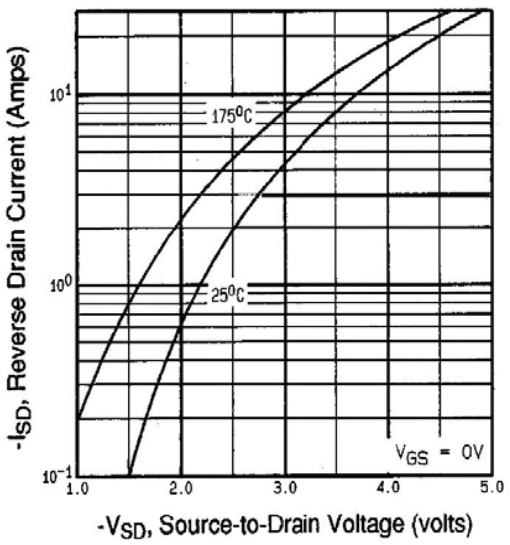


Fig. 7 - Typical Source-Drain Diode Forward Voltage

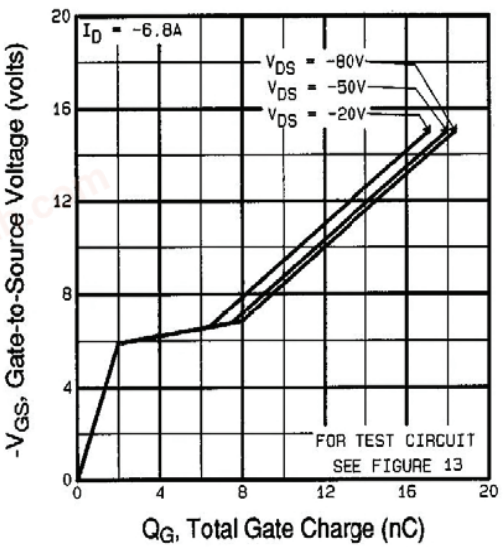


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

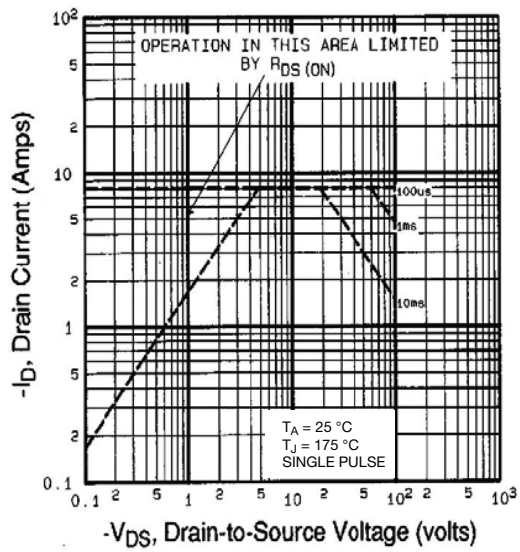


Fig. 8 - Maximum Safe Operating Area

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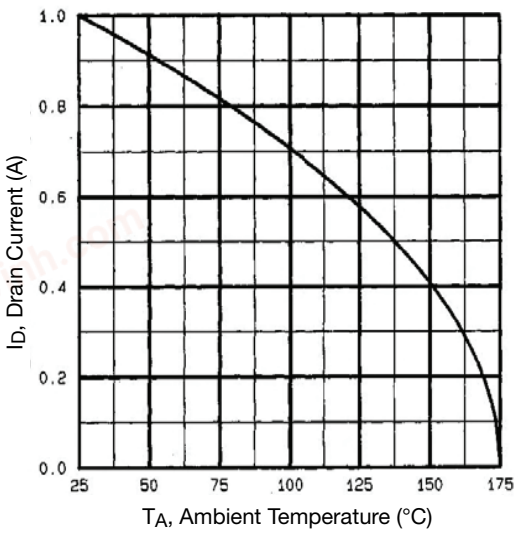


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

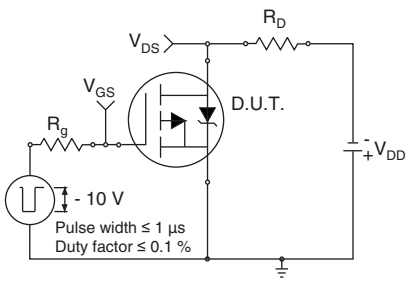


Fig. 10a - Switching Time Test Circuit

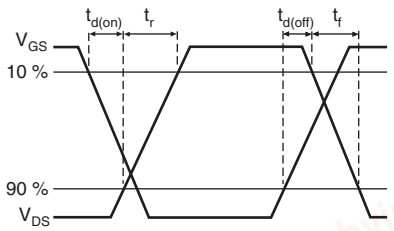


Fig. 10b - Switching Time Waveforms

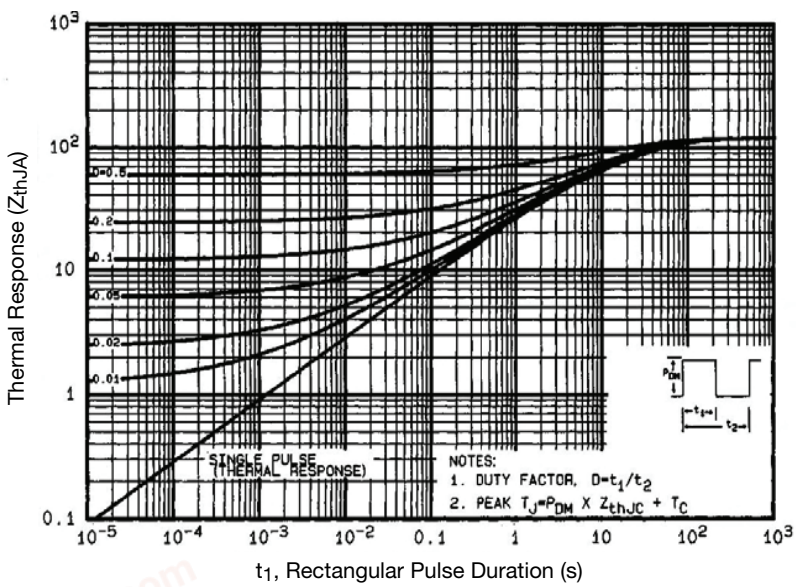


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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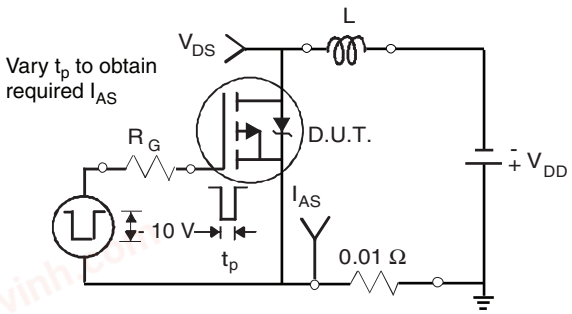


Fig. 12a - Unclamped Inductive Test Circuit

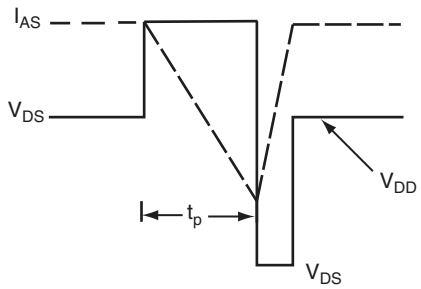


Fig. 12b - Unclamped Inductive Waveforms

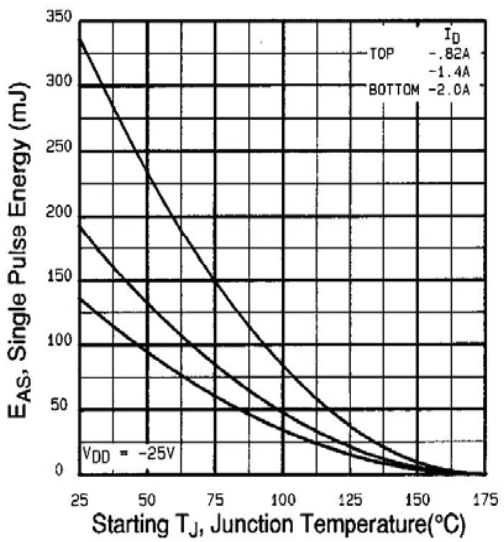


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

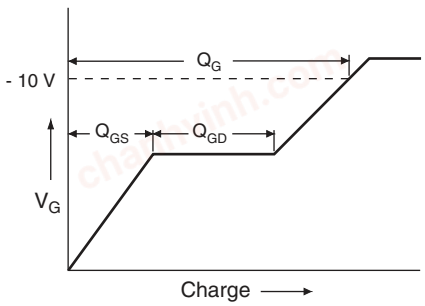


Fig. 13a - Basic Gate Charge Waveform

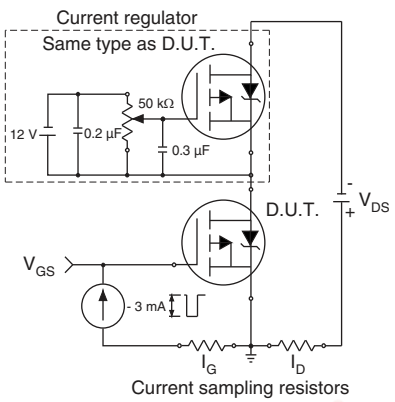
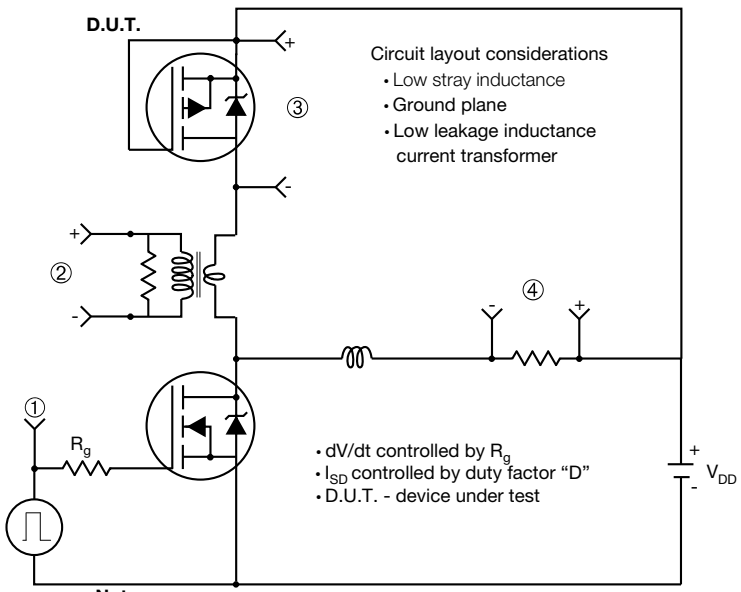


Fig. 13b - Gate Charge Test Circuit

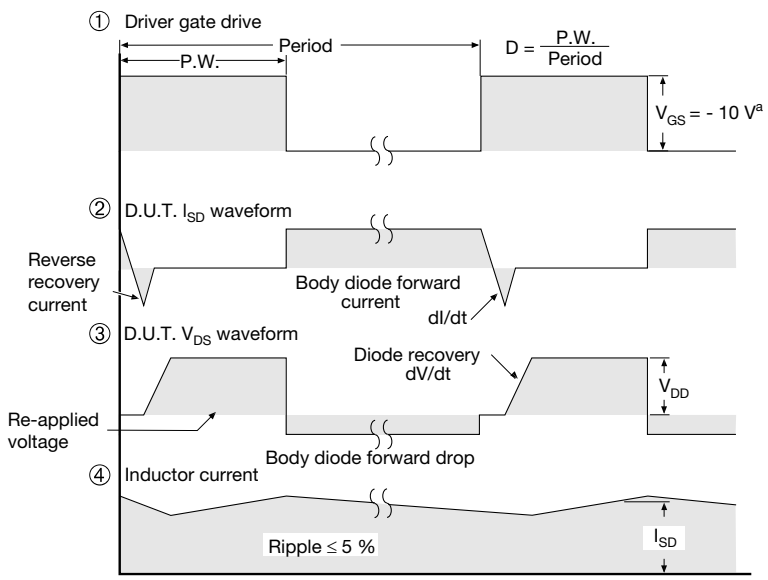
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Peak Diode Recovery dV/dt Test Circuit



Note
• Compliment N-Channel of D.U.T. for driver



Note
a. V_{GS} = - 5 V for logic level and - 3 V drive devices

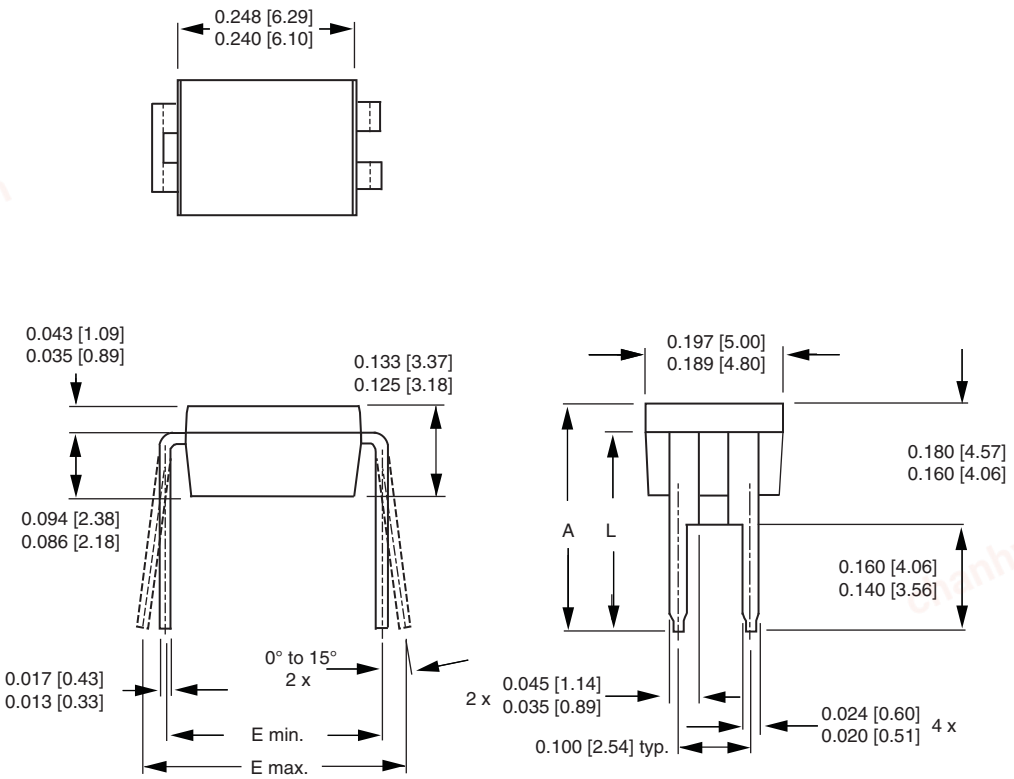
Fig. 14 - For P-Channel

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HVM DIP (High voltage)



	INCHES		MILLIMETERS	
DIM.	**MIN.**	**MAX.**	**MIN.**	**MAX.**
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36
ECN: X10-0386-Rev. B, 06-Sep-10 DWG: 5974				

Note

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

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