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High Power Thin Film Wraparound Chip Resistor AEC-Q200 Qualified



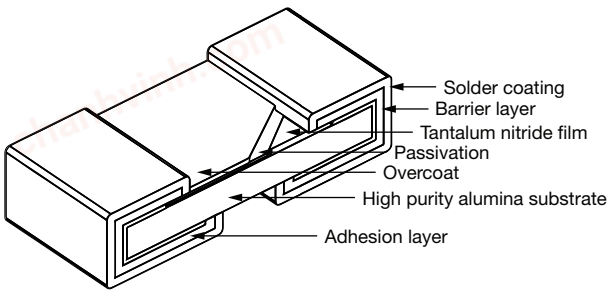
LINKS TO ADDITIONAL RESOURCES

3D Models

PHPA series chip resistors incorporate the self passivated enhanced tantalum nitride film to give superior moisture resistance, ESD, voltage coefficient, and resistance stability performance. They are designed with enlarged backside terminations to reduce the thermal resistance between the topside resistor layer and the solder joint on the end user's circuit board.

Actual power handling capability is limited by the end user mounting process. As with any high power chip resistor the ability to remove the generated heat is critical to the overall performance of the device.

CONSTRUCTION



FEATURES

- AEC-Q200 qualified
- ESD rating 5A (HBM)
- Moisture resistant
- High purity ceramic substrate
- Power rating to 2.5 W
- Resistance range 10 Ω to 30.1 kΩ
- Resistor tolerance to ± 0.1 %
- TCR to ± 25 ppm/°C
- Flame resistant UL 94 V-0
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Power supplies
- Power switching
- Braking system
- Test and measurement equipment
- Motor deflection circuits

TYPICAL PERFORMANCE

	ABSOLUTE
TCR	25
TOL.	0.1

STANDARD ELECTRICAL SPECIFICATIONS		
TEST	**SPECIFICATIONS**	**CONDITIONS**
Material	Tantalum nitride	-
Resistance Range	10 Ω to 30.1 kΩ	-
TCR: Absolute	25 ppm/°C, 50 ppm/°C, and 100 ppm/°C	-55 °C to +155 °C
Tolerance: Absolute	± 0.1 % to ± 5 %	+25 °C
Power Rating: Resistor	1 W to 2.5 W (1)	Maximum at +70 °C
Stability: Absolute	Δ*R* 0.50 %	4000 h at +70 °C
Stability: Ratio	Not applicable	-
Voltage Coefficient	< 0.1 ppm/V	-
Working Voltage	200 V	-
Operating Temperature Range	-55 °C to +155 °C	-
Storage Temperature Range	-55 °C to +155 °C	-
Noise	< -30 dB	-
Shelf Life Stability: Absolute	± 0.01 %	1 year at +25 °C

Note

(1) Dependent on component mounting by user

For technical questions, contact: thinfilm@vishay.com

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COMPONENT RATINGS

CASE SIZE	POWER RATING (mW)	WORKING VOLTAGE (V)	RESISTANCE RANGE (Ω)
1206	1000 (1)	200	12 to 30.1K
2512	2500 (1)	200	10 to 30.1K

Note

(1) Dependent on component mounting by user

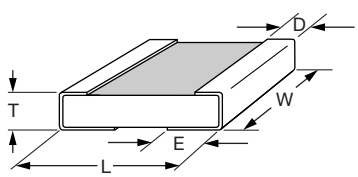
ENVIRONMENTAL TESTS (Vishay Performance vs. AEC-Q200 Requirements)

ENVIRONMENTAL TEST		CONDITIONS	TEST LIMITS	TYPICAL VISHAY PERFORMANCE
Resistance Temperature Characteristic		-55 °C to +155 °C	± 25 ppm/°C	+11.5 ppm/°C
Maximum Ambient Temperature at Rated Wattage		See Derating Curve		
Maximum Ambient Temperature at Power Derating				
High Temperature Exposure	ΔR	MIL-STD-202, method 108, 1000 h at 155 °C	± 0.2 %	+0.013 %
Temperature Cycling	ΔR	JESD22, JA-104, 1000 cycles, -55 °C to 155 °C	± 0.25 %	+0.006 %
Biased Humidity	ΔR	MIL-STD-202, 103, 1000 h at 85 °C, 85 % RH, 10 % power	± 1.0 %	+0.025 %
Life	ΔR	MIL-STD-202, 108, 2000 h at 70 °C, 100 % power	± 0.5 %	+0.060 %
Mechanical Shock	ΔR	MIL-STD-202, 213, condition C	± 0.25 %	0.000 %
Vibration	ΔR	MIL-STD-202, 204, 10 Hz to 2 kHz	± 0.25 %	0.000 %
Resistance to Soldering Heat	ΔR	MIL-STD-202, 210, condition D	± 0.25 %	+0.006 %
Electrostatic Discharge	ΔR	AEC-Q200-002 > 8 kV	± 1.0 %	-0.098 %
Solderability	Visual	J-STD-002, method B and B1	95 %	Acceptable
Terminal Strength	ΔR	AEC-Q200-006 at 1 kg for 60 s	± 1.0 %	0.000
Flame Retardance	Visual	AEC-Q200-001, para 4.0		Acceptable

Note

- Typical Vishay performance based on the data median

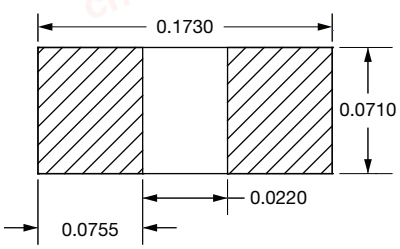
DIMENSIONS in inches



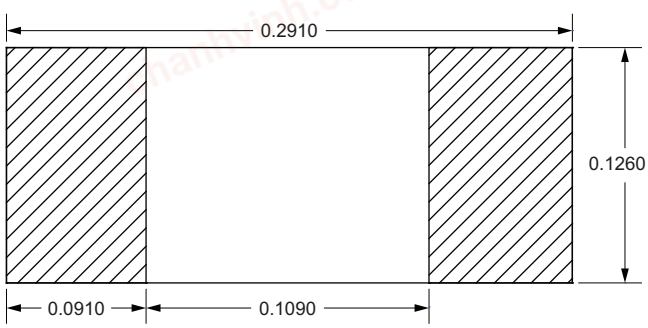
CASE SIZE	LENGTH	WIDTH W (± 0.005)	THICKNESS MIN. / MAX.	TOP PAD D (± 0.005)	BOTTOM PAD E (± 0.005)
1206	0.126 ± 0.008	0.063	0.015 / 0.020	0.020	0.040
2512	0.259 + 0.009/- 0.015	0.124	0.015 / 0.020	0.020	0.050

LAND PATTERN DIMENSIONS in inches

1206 Land Pattern



2512 Land Pattern

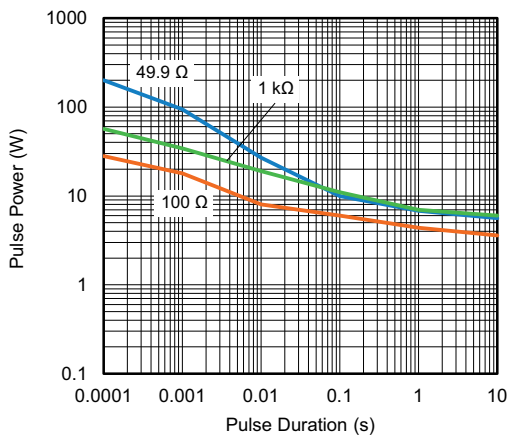


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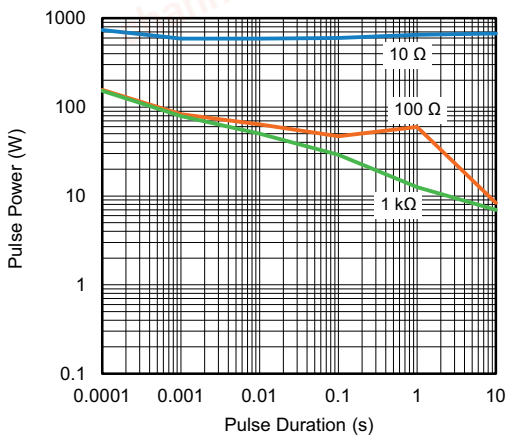
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STANDARD MATERIAL SPECIFICATIONS	
Resistive Element	Tantalum nitride
Substrate Material	Alumina (Al_2O_3)
Terminations (Lead (Pb)-Free)	Tin solder plate over nickel barrier

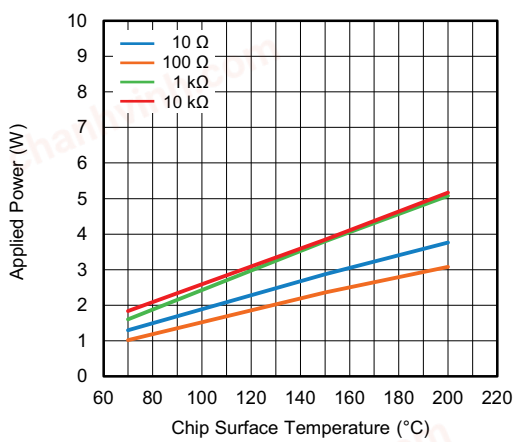
PHPA1206 SINGLE PULSE CURVE



PHPA2512 SINGLE PULSE CURVE



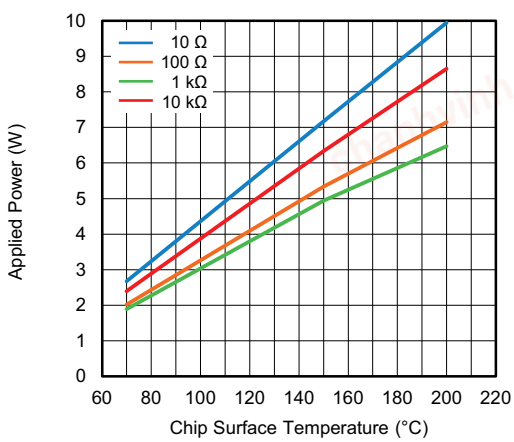
PHPA1206 CHIP TEMP. VS. APPLIED POWER



Notes

- Chip surface temperature measured using FLIR A40 thermal imaging system with an approximate test card surface temperature of 25 °C
- Thermal imaging was conducted under ambient conditions resulting in a steady state test card surface temperature of 85 °C over the full range of power levels
- Thermal imaging and load life testing was conducted mounting one device to 2" x 3" test cards with 2.5 mil copper plating on both surfaces. Thermal vias on 120 mil centers were utilized for heat transfer between surfaces of the test card

PHPA2512 CHIP TEMP. VS. APPLIED POWER



Notes

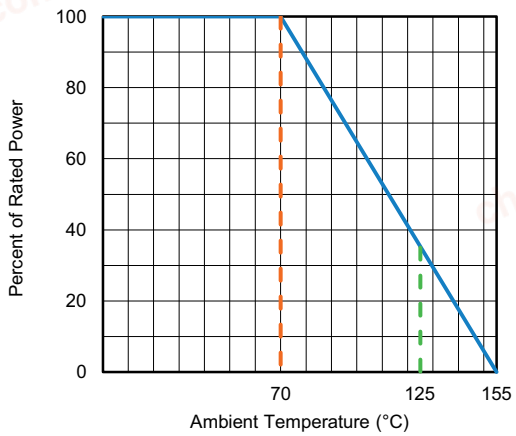
- Chip surface temperature measured using FLIR A40 thermal imaging system with an approximate test card surface temperature of 25 °C

Case Size	2512	2512	2512
Resistance Value	Up to 10 Ω	Up to 100 Ω	Up to 1 kΩ
Temperature	**Power (W)**		
70	2.67	2.02	1.89
150	7.17	5.34	4.94
200	9.94	7.15	6.48

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DERATING CURVE



GLOBAL PART NUMBER INFORMATION

P	H	P	A	1	2	0	6	E	1	0	0	2	B	S	T	1

GLOBAL MODEL	CASE SIZE	TCR (1)	RESISTANCE	TOLERANCE	TERMINATION	PACKAGING
PHPA	**1206** **2512**	**E** = ± 25 ppm/°C **H** = ± 50 ppm/°C **K** = ± 100 ppm/°C	The first 3 digits are significant figures and the last digit specifies the number of zeros to follow. "R" designates the decimal point. Example: 10R0 = 10 Ω 1000 = 100 Ω 1001 = 1 kΩ	**B** = ± 0.1 % **D** = ± 0.5 % **F** = ± 1.0 % **G** = ± 2.0 % **J** = ± 5.0 %	**S** = wraparound 100 % electroplated pure matte tin RoHS-compliant - e3	BULK **BS** = 100 min., 1 mult. WAFFLE **WS** = 100 min., 1 mult. **W0** = 100 min.,100 mult. **WI** = 100 min., 1 mult. (2) **WP** = 100 min.,1 mult. (3) TAPE AND REEL **T0** = 100 min., 100 mult. **T1** = 1000 min., 1000 mult. (4) **T3** = 300 min., 300 mult. **T5** = 500 min., 500 mult. **TF** = full reel **TS** = 100 min., 1 mult. **TI** = 100 min., 1 mult. (2) **TP** = 100 min., 1 mult. (3)

Notes

(1) < 50 Ω "E" TCR characteristic is not available
(2) Item single lot date code
(3) Package unit single lot date code
(4) Preferred packaging code

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