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Low On-Resistance Wideband/Video Switches

DESCRIPTION

The DG641, DG642, DG643 are high performance monolithic video switches designed for switching wide bandwidth analog and digital signals. DG641 is a quad SPST, DG642 is a single SPDT, and DG643 is a dual SPDT function. These devices have exceptionally low on-resistances (5 Ω typ-DG642), low capacitance and high current handling capability.

To achieve TTL compatibility, low channel capacitances and fast switching times, the DG641, DG642, DG643 are built on the Vishay Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when on, and blocks up to 14 V_{p-p} when off. An epitaxial layer prevents latchup.

FEATURES

- Wide bandwidth: 500 MHz
- Low crosstalk at 5 MHz: - 85 dB
- Low $R_{DS(on)}$: 5 Ω, DG642
- TTL logic compatible
- Fast switching: t_{ON} 50 ns
- Single supply compatibility
- High current: 100 mA, DG642

BENEFITS

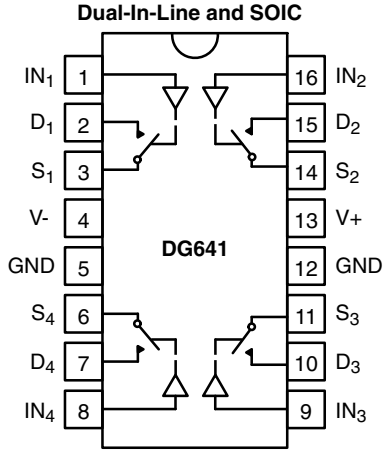
- High precision
- Improved frequency response
- Low insertion loss
- Improved system performance
- Reduced board space
- Low power consumption

APPLICATIONS

- RF and video switching
- RGB switching
- Video routing
- Cellular communications
- ATE
- Radar/FLIR systems
- Satellite receivers
- Programmable filters

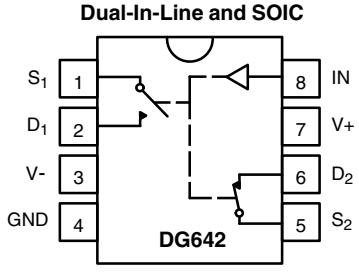
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line and SOIC



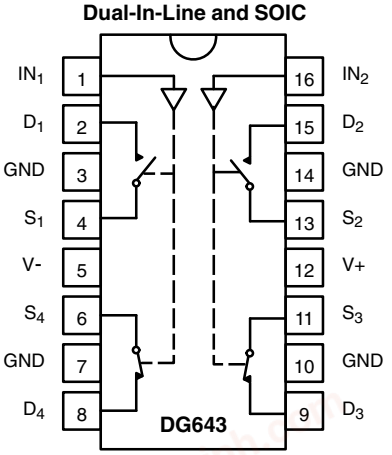
Top View

Dual-In-Line and SOIC



Top View

Dual-In-Line and SOIC



Top View

TRUTH TABLE (DG641)	
Logic	**Switch**
0	OFF
1	ON

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

TRUTH TABLE (DG642)		
Logic	**SW_1**	**SW_2**
0	OFF	ON
1	ON	OFF

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

TRUTH TABLE (DG643)		
Logic	**SW_1, SW_2**	**SW_3, SW_4**
0	OFF	ON
1	ON	OFF

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

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ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
DG641		
- 40 °C to 85 °C	16-Pin Plastic DIP	DG641DJ
	16-Pin Narrow SOIC	DG641DY
DG642		
- 40 °C to 85 °C	8-Pin Plastic DIP	DG642DJ
	8-Pin Narrow SOIC	DG642DY
DG643		
- 40 °C to 85 °C	16-Pin Plastic DIP	DG643DJ
	16-Pin Narrow SOIC	DG643DY

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
V+ to V-			- 0.3 to 21	V
V+ to GND			- 0.3 to 21	
V- to GND			- 19 to + 0.3	
Digital Inputs			(V-) - 0.3 V to (V+) + 0.3 V or 20 mA, whichever occurs first	
V_S, V_D			(V-) - 0.3 V to (V+) + 14 V or 20 mA, whichever occurs first	
Continuous Current (Any terminal except S or D)			20	mA
Continuous Current S or D	DG641, DG643		75	
	DG642		100	
Current, S or D (Pulsed at 1 ms, 10 % duty cycle max)	DG641, DG643		200	
	DG642		300	
Storage Temperature			- 65 to 125	°C
Power Dissipation (Package)[b]	8-Pin Plastic DIP and Narrow SOIC[c]		300	mW
	16-Pin Plastic DIP[d]		470	
	16-Pin Narrow SOIC[e]		600	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 7.6 mW/°C above 75 °C.
d. Derate 6 mW/°C above 75 °C.
e. Derate 80 mW/°C above 75 °C.

SCHEMATIC DIAGRAM (Typical Channel)

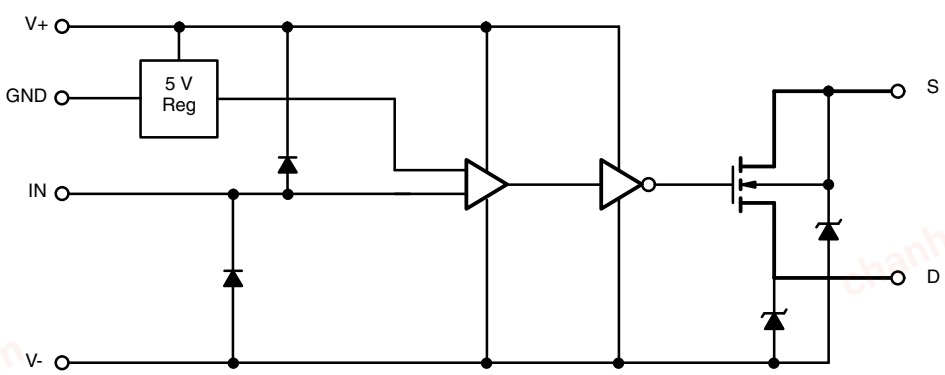


Figure 1.

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SPECIFICATIONS (for DG641 and DG643)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 15 V, V- = - 3 V V_{INH} = 2.4 V, V_{INL} = 0.8 V[e]	**Temp.[a]**	**Limits** - 40 °C to 85 °C **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}	V- = - 5 V, V+ = 12 V	Full	- 5		8	V
		V- = GND V, V+ = 12 V	Full	0		8	
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = - 10 mA, V_D = 0 V	Room Full		8	15 20	Ω
$R_{DS(on)}$ Match	$\Delta R_{DS(on)}$		Room		1	2	
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, V_D = 10 V	Room Full	- 10 - 100	- 0.02	10 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0 V	Room Full	- 10 - 100	- 0.02	10 100	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V	Room Full	- 10 - 100	- 0.1	10 100	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	
Input Current	I_{IN}	V_{IN} = GND or V+	Room Full	- 1 - 20	0.05	1 20	µA
Dynamic Characteristics							
On State Input Capacitance[d]	$C_{S(on)}$	V_S = V_D = 0 V	Room		10	20	pF
Off State Output Capacitance[d]	$C_{S(off)}$	V_S = 0 V	Room		4	12	
Off State Input Capacitance[d]	$C_{D(off)}$	V_D = 0 V	Room		4	12	
Bandwidth	BW	R_L = 50 Ω, see figure 6	Room		500		MHz
Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF see figure 2	Room Full		50	70 140	ns
Turn Off Time	t_{OFF}		Room Full		28	50 85	
Charge Injection	Q	C_L = 1000 pF, V_D = 0 V see figure 3	Room		- 19		pC
Off Isolation	OIRR	R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz, see figure 4	Room		- 60		dB
All Hostie Crosstalk	X_{TALK}	R_{IN} = 10 Ω, R_L = 75 Ω f = 5 MHz, see figure 5	Room		- 87		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or V_{IN} = 5 V	Room Full		3.5	6 9	mA
Negative Supply Current	I-		Room Full	- 6 - 9	- 3		

Notes:
a. Room = 25 °C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

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SPECIFICATIONS (for DG642)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 15 V, V- = - 3 V V_{INH} = 2.4 V, V_{INL} = 0.8 V[e]	**Temp.[a]**	**Limits** - 40 °C to 85 °C **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}	V- = - 5 V, V+ = 12 V	Full	- 5		8	V
		V- = GND V, V+ = 12 V	Full	0		8	
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = - 10 mA, V_D = 0 V	Room Full		5	8 9	Ω
$R_{DS(on)}$ Match	$\Delta R_{DS(on)}$		Room		0.5	1	
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, V_D = 10 V	Room Full	- 10 - 200	- 0.04	10 200	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0 V	Room Full	- 10 - 200	- 0.04	10 200	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V	Room Full	- 10 - 200	- 0.2	10 200	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	
Input Current	I_{IN}	V_{IN} = GND or V+	Room Full	- 1 - 20	0.05	1 20	µA
Dynamic Characteristics							
On State Input Capacitance[d]	$C_{S(on)}$	V_S = V_D = 0 V	Room		19	40	pF
Off State Input Capacitance[d]	$C_{S(off)}$	V_D = 0 V	Room		8	20	
Off State Output Capacitance[d]	$C_{D(off)}$	V_S = 0 V	Room		8	20	
Bandwidth	BW	R_L = 50 Ω, see figure 6	Room		500		MHz
Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF see figure 2	Room Full		60	100 160	ns
Turn Off Time	t_{OFF}		Room Full		40	60 100	
Charge Injection	Q	C_L = 1000 pF, V_D = 0 V see figure 3	Room		- 40		pC
Off Isolation		R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz, see figure 4	Room		- 63		dB
All Hostie Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 75 Ω f = 5 MHz, see figure 5	Room		- 85		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or V_{IN} = 5 V	Room Full		3.5	6 9	mA
Negative Supply Current	I-		Room Full	- 6 - 9	- 3		

Notes:

a. Room = 25 °C, Full = as determined by the operating temperature suffix.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

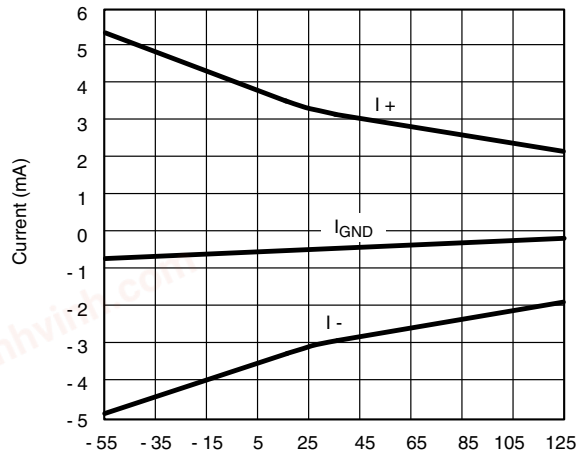
d. Guaranteed by design, not subject to production test.

e. V_{IN} = input voltage to perform proper function.

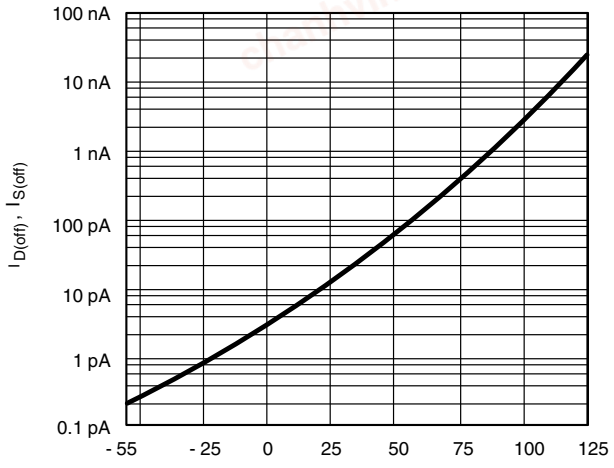
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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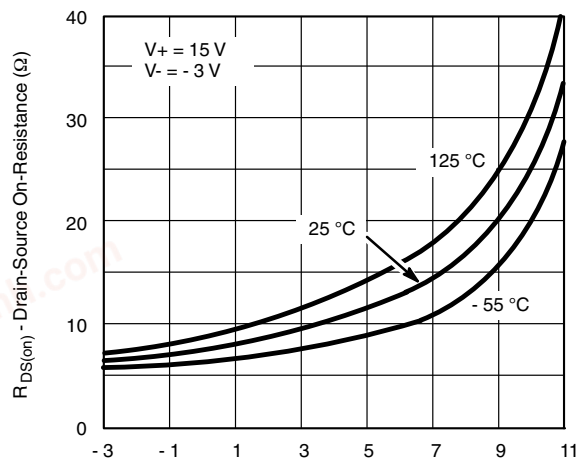
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



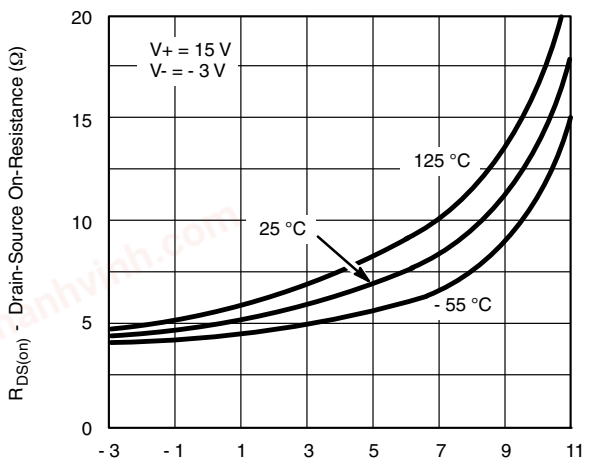
Supply Current vs. Temperature



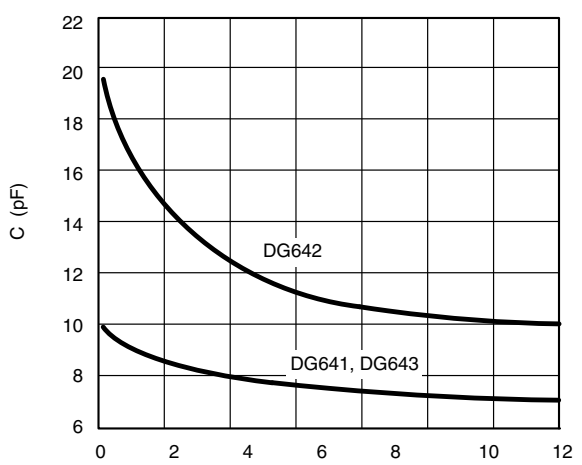
Leakages vs. Temperature



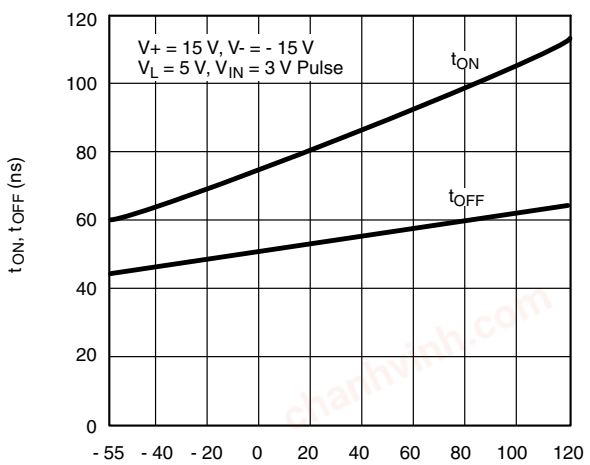
DG641, DG643
$R_{DS(on)}$ vs. Drain Voltage



DG642
$R_{DS(on)}$ vs. Drain Voltage



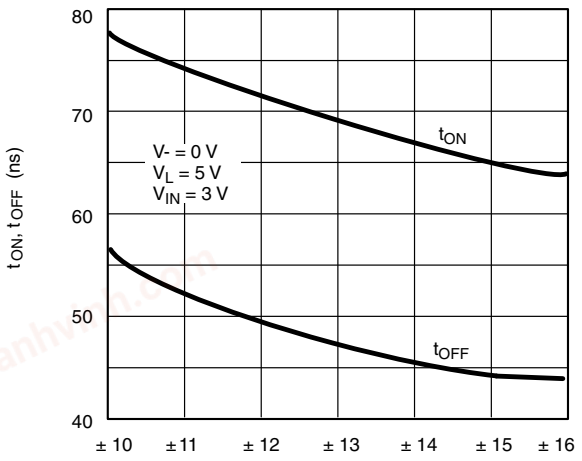
On Capacitance



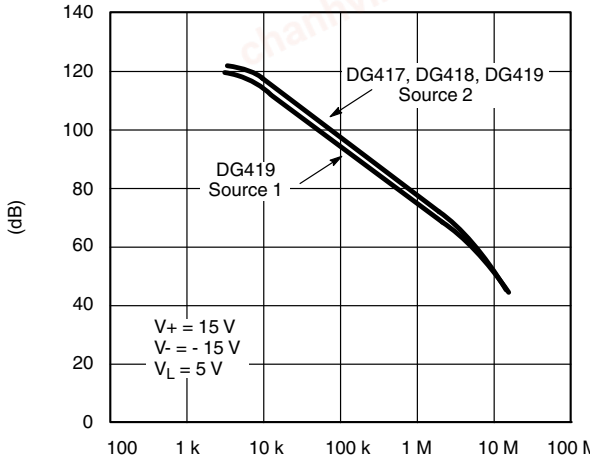
Off Isolation

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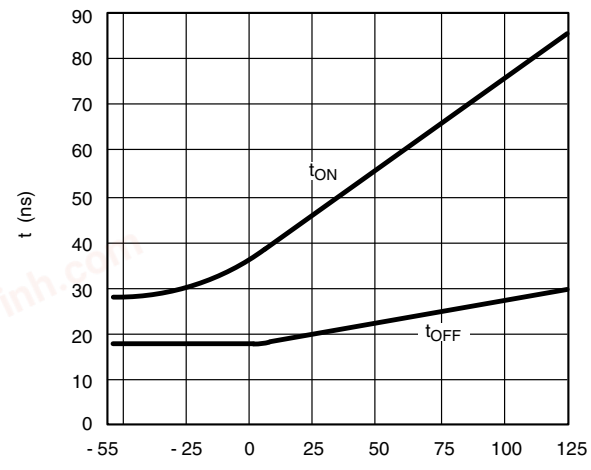
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



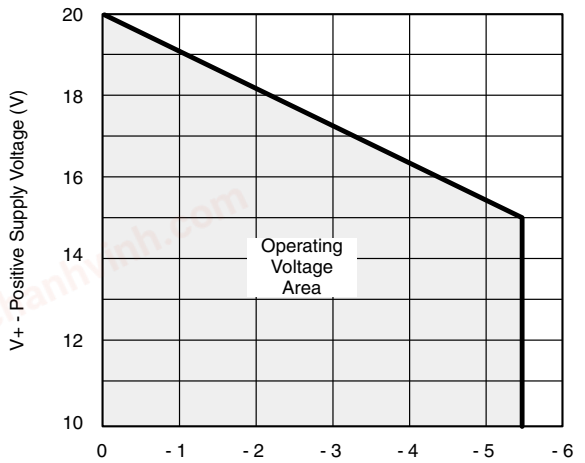
All Hostile Crosstalk



Charge Injection vs. V_D

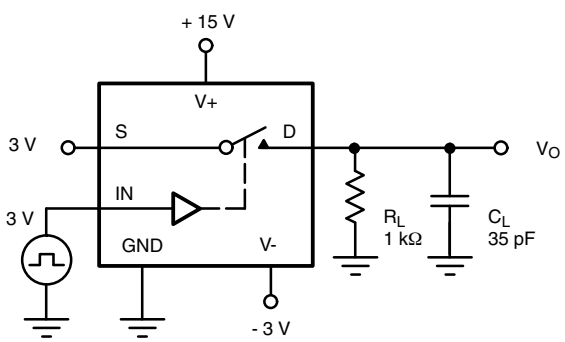


Switching Times vs. Temperature



Operating Supply Voltage Range

TEST CIRCUITS



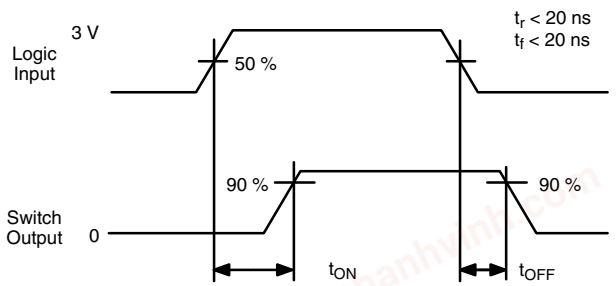


Figure 2. Switching Time

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TEST CIRCUITS

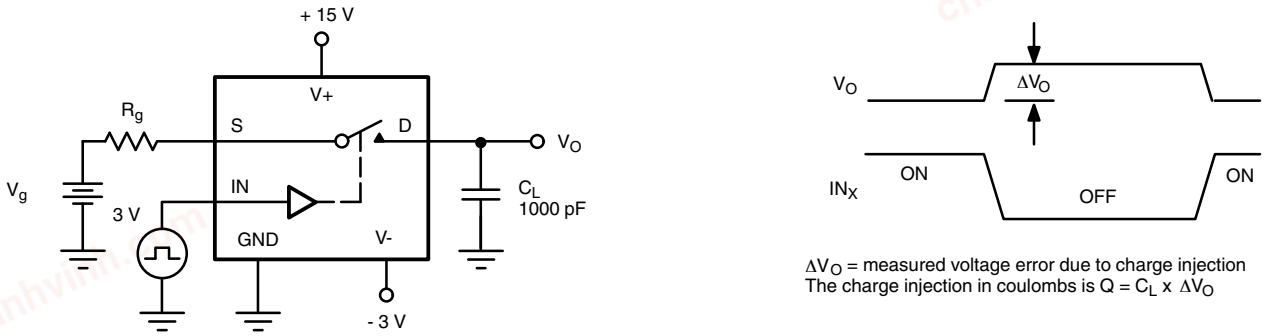


Figure 3. Charge Injection

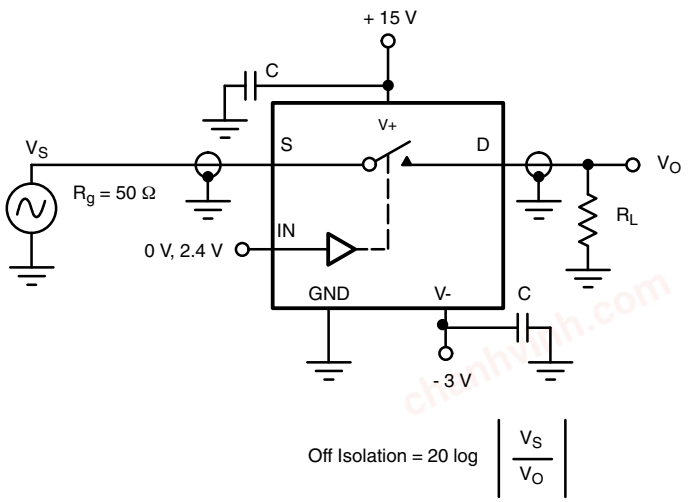


Figure 4. Off Isolation

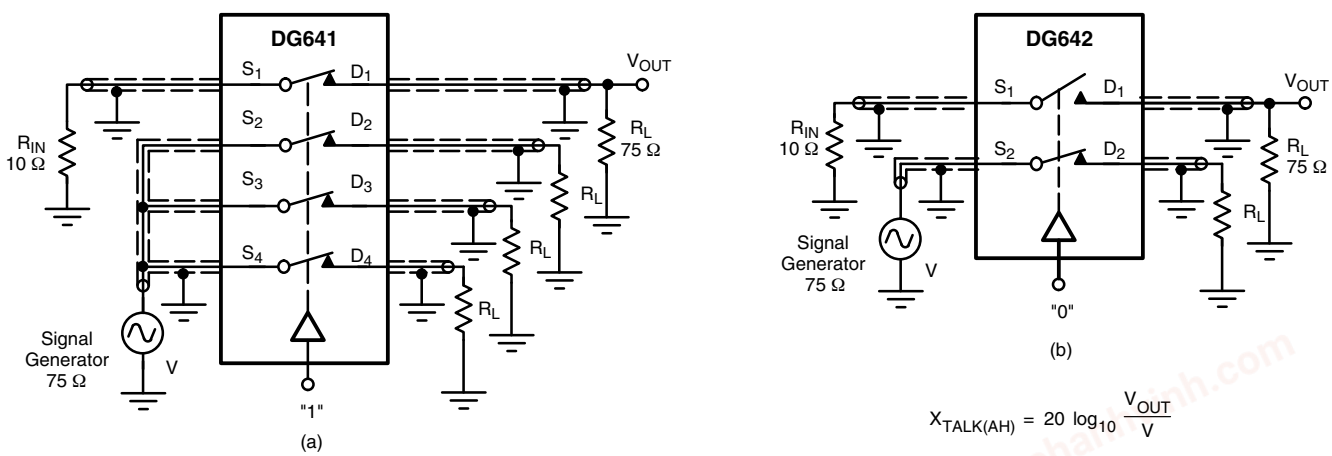


Figure 5. All Hostile Crosstalk - $X_{TALK(AH)}$

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TEST CIRCUITS

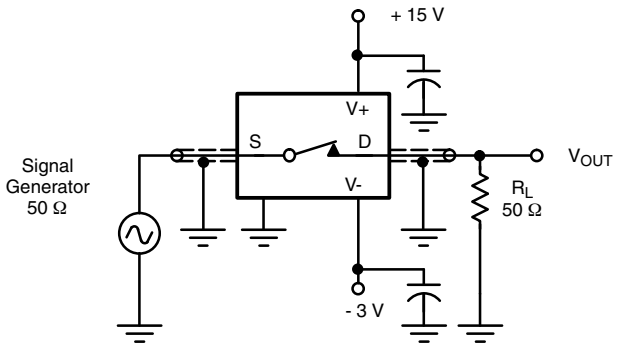


Figure 6. Bandwidth

APPLICATIONS

Device Description

The DG641, DG642, DG643 switches offer true bidirectional switching of high frequency analog or digital signals with minimum signal crosstalk, low insertion loss, and negligible non-linearity distortion and group delay.

Built on the Siliconix D/CMOS process, these switches provide excellent off-isolation with a bandwidth of around 500 MHz. The silicon-gate D/CMOS processing also yields fast switching speeds.

An on-chip regulator circuit maintains TTL input compatibility over the whole operating supply voltage range shown, easing control logic interfacing.

Circuit layout is facilitated by the interchangeability of source and drain terminals.

Frequency Response

A single switch on-channel exhibits both resistance [$R_{DS(on)}$] and capacitance [$C_{S(on)}$]. This RC combination has an attenuation effect on the analog signal - which is frequency dependent (like an RC low-pass filter). The - 3 dB bandwidth of the DG641, DG642, DG643 is typically 500 MHz (into 50 Ω).

Power Supplies

Power supply flexibility is a useful feature of the DG641, DG642, DG643 series. It can be operated from a single positive supply (V+) if required (V- connected to ground).
Note that the analog signal must not exceed V- by more than - 0.3 V to prevent forward biasing the substrate p-n junction. The use of a V- supply has a number of advantages:

1. It allows flexibility in analog signal handling, i.e., with V- = - 5 V and V+ = 12 V; up to ± 5 V ac signals can be controlled.
2. The value of on capacitance [$C_{S(on)}$] may be reduced. A property known as 'the body-effect' on the DMOS switch devices causes various parametric effects to occur. One of these effects is the reduction in $C_{S(on)}$ for an increasing V body-source. Note however that to increase V- normally requires V+ to be reduced (since V+ to V- = 21 V max.). A reduction in V+ causes an increase in $r_{DS(on)}$, hence a compromise has to be achieved. It is also useful to note that tests indicate that optimum video linearity performance (e.g., differential phase and gain) occurs when V- is around - 3 V.
3. V- eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

Decoupling

It is an established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG641, DG642, DG643 series is adversely affected by poor decoupling of power supply pins. Also, of even more significance, since the substrate of the device is connected to the negative supply, adequate decoupling of this pin is essential. Suitable decoupling capacitors are 1- to 10 µF tantalum bead, plus 10- to 100-nF ceramic or polyester.

Rules:

1. Decoupling capacitors should be incorporated on all power supply pins (V+, V-). (see figure 7).
2. They should be mounted as close as possible to the device pins.
3. Capacitors should be of a suitable type with good high frequency characteristics - tantalum bead and/or ceramic disc types are adequate.

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APPLICATIONS

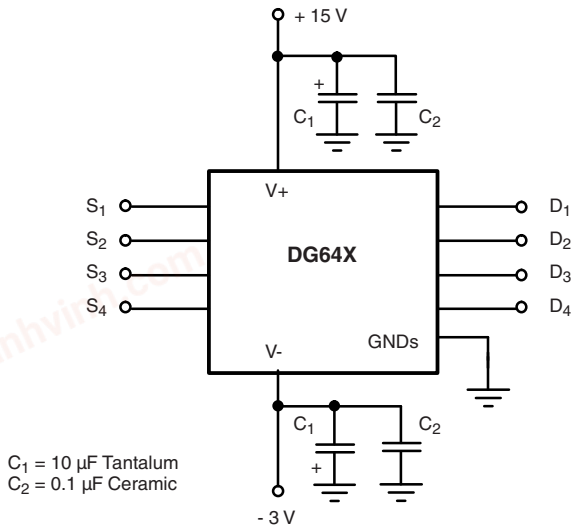


Figure 7. Supply Decoupling

Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by these analog switches. Some tips for minimizing stray effects are:

1. Use extensive ground planes on double sided PCB, separating adjacent signal paths. Multilayer PCB is even better.
2. Keep signal paths as short as practically possible, with all channel paths of near equal length.
3. Careful arrangement of ground connections is also very important. Star connected system grounds eliminate signal current, flowing through ground path parasitic resistance, from coupling between channels.

Figure 8 shows a 4-channel video multiplexer using a DG641.

In Figure 9, two coax cables terminated on 75 Ω bring two video signals to the DG642 switch. The two drains tied together lower the on-state capacitance. An Si582 video amplifier drives a double terminated 75 Ω cable. The double terminated coax cable eliminates line reflections.

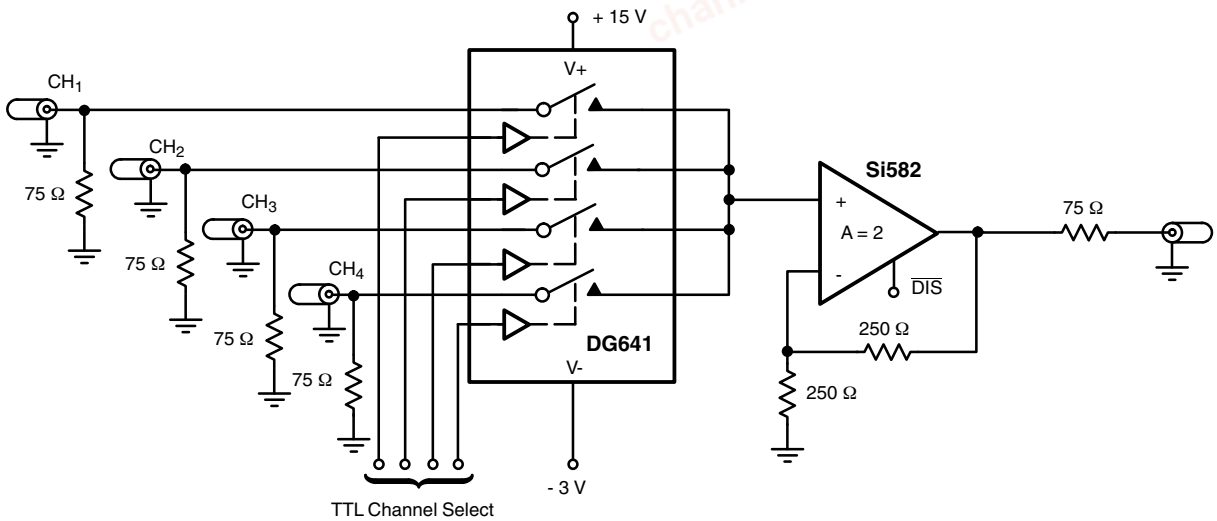


Figure 8. 4 by 1 Video Multiplexing Using the DG641

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APPLICATIONS

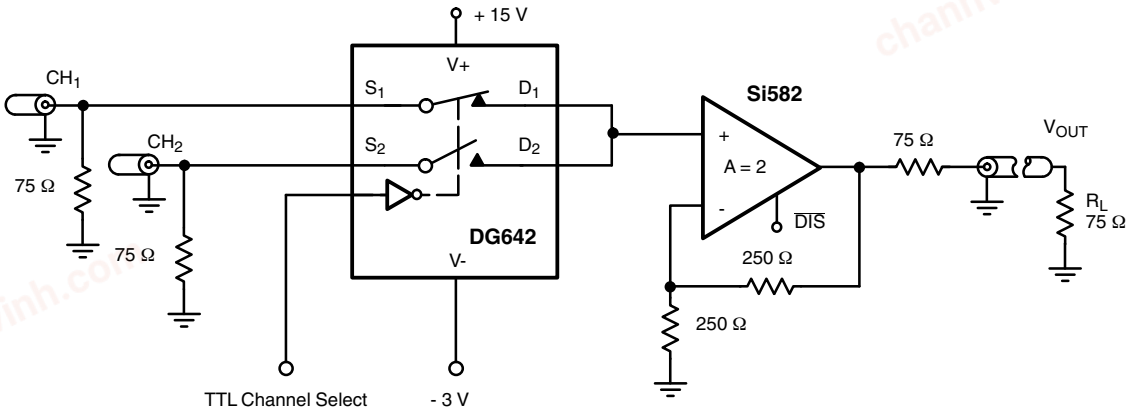


Figure 9. 2-Channel Video Selector Using the DG642

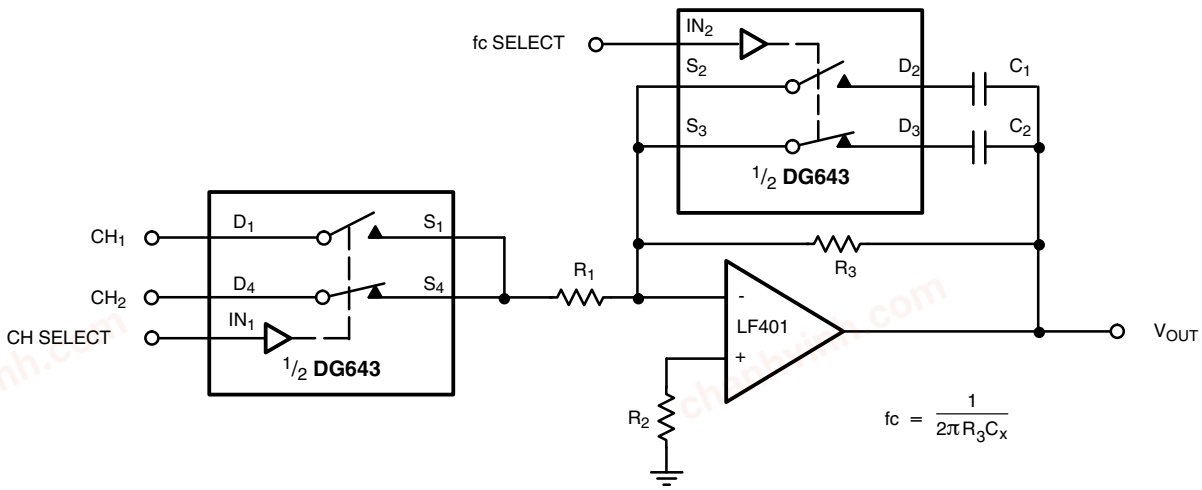


Figure 10. Active Low Pass Filter with Selectable Inputs and Break Frequencies

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70058.

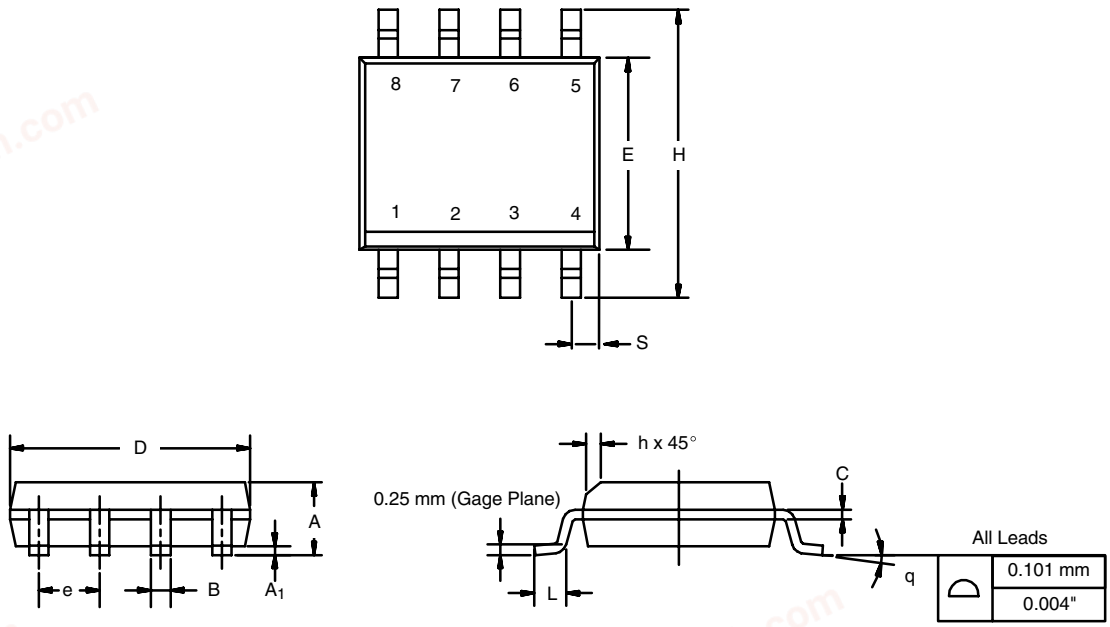
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Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

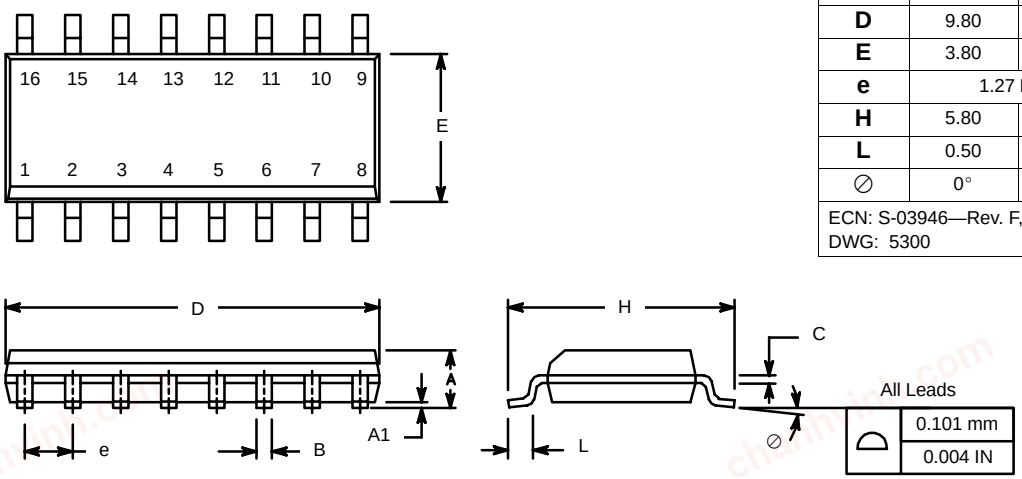
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Package Information
Vishay Siliconix

SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

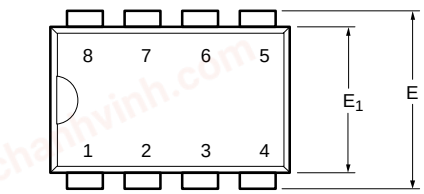
ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

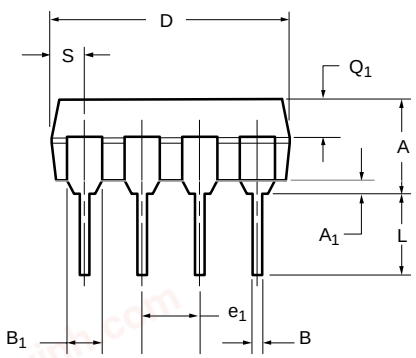


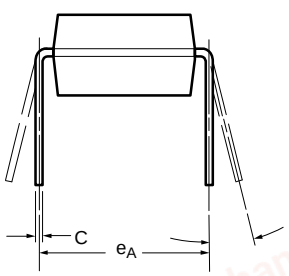
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Package Information
Vishay Siliconix

PDIP: 8-LEAD







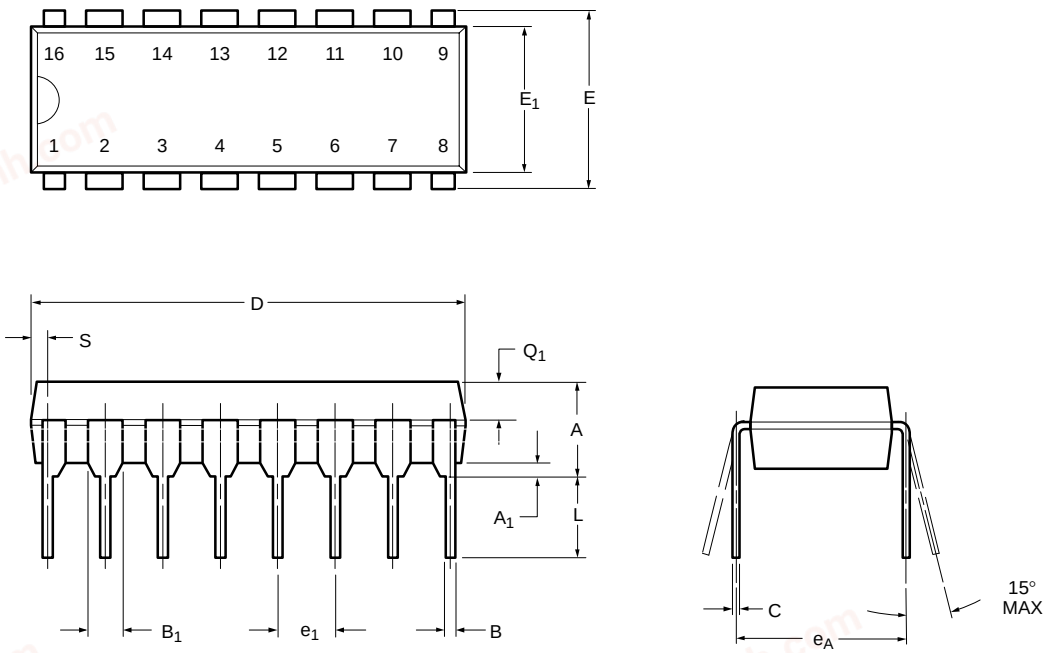
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	9.02	10.92	0.355	0.430
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.76	1.65	0.030	0.065

ECN: S-03946—Rev. E, 09-Jul-01
DWG: 5478

NOTE: End leads may be half leads.

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PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482

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VISHAY SILICONIX

Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

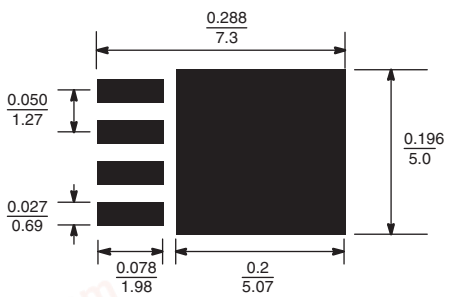


Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

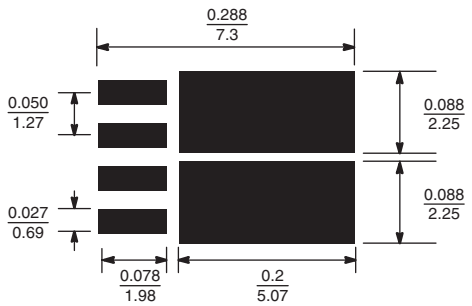


Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

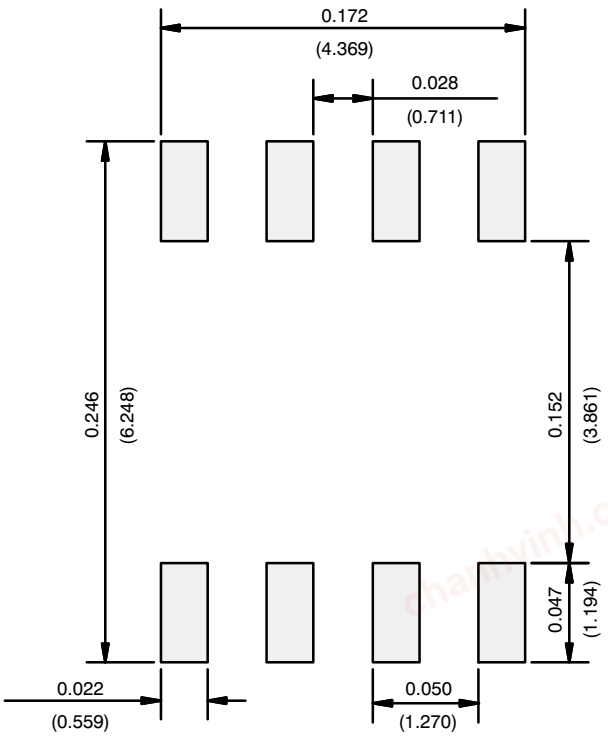
The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

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RECOMMENDED MINIMUM PADS FOR SO-8



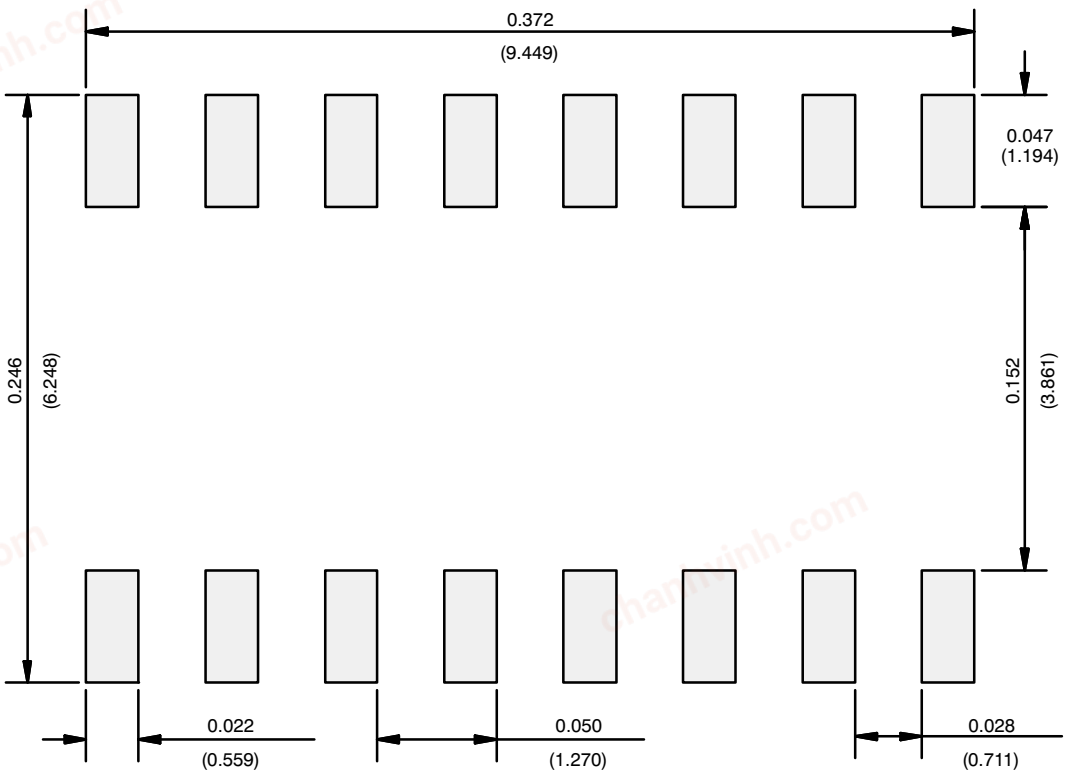
Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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