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Improved Quad CMOS Analog Switches

DESCRIPTION

The DG211B/212B analog switches are highly improved versions of the industry-standard DG211/212. These devices are fabricated in Vishay Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG211B and DG212B can handle up to ± 22 V, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

The DG211B is a normally closed switch and the DG212B is a normally open switch. (See Truth Table.)

FEATURES

- ± 22 V supply voltage rating
- TTL and CMOS compatible logic
- Low on-resistance - $r_{DS(on)}$: 50 Ω
- Low leakage - $I_{D(on)}$: 20 pA
- Single supply operation possible
- Extended temperature range
- Fast switching - t_{ON}: 120 ns
- Low charge injection - Q: 1 pC

Pb-free Available

RoHS* COMPLIANT

BENEFITS

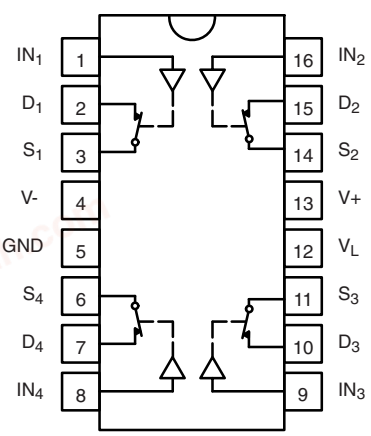
- Wide analog signal range
- Simple logic interface
- Higher accuracy
- Minimum transients
- Reduced power consumption
- Superior to DG211/212
- Space savings (TSSOP)

APPLICATIONS

- Industrial instrumentation
- Test equipment
- Communications systems
- Disk drives
- Computer peripherals
- Portable instruments
- Sample-and-hold circuits

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG211B
Dual-In-Line, SOIC and TSSOP



Top View

TRUTH TABLE

Logic	DG211B	DG212B
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply.

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ORDERING INFORMATION

Temp. Range	Package	Standard Part Number	Lead (Pb)-free Part Number
- 40 °C to 85 °C	16-Pin Plastic DIP	DG211BDJ	DG211BDJ-E3
		DG212BDJ	DG212BDJ-E3
	16-Pin Narrow SOIC	DG211BDY DG211BDY-T1	DG211BDY-E3 DG211BDY-T1-E3
		DG212BDY DG212BDY-T1	DG212BDY-E3 DG212BDY-T1-E3
	16-Pin TSSOP	DG211BDQ DG211BDQ-T1	DG211BDQ-E3 DG211BDQ-T1-E3
		DG212BDQ DG212BDQ-T1	DG212BDQ-E3 DG212BDQ-T1-E3

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Limit	Unit
Voltages Referenced, V+ to V-		44	V
GND		25	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current, Any Terminal		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature		- 65 to 125	°C
Power Dissipation (Package)[b]	16-Pin Plastic DIP[c]	470	mW
	16-Pin Narrow SOIC and TSSOP[d]	640	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.5 mW/°C above 75 °C.
d. Derate 7.6 mW/°C above 75 °C.

SCHEMATIC DIAGRAM Typical Channel

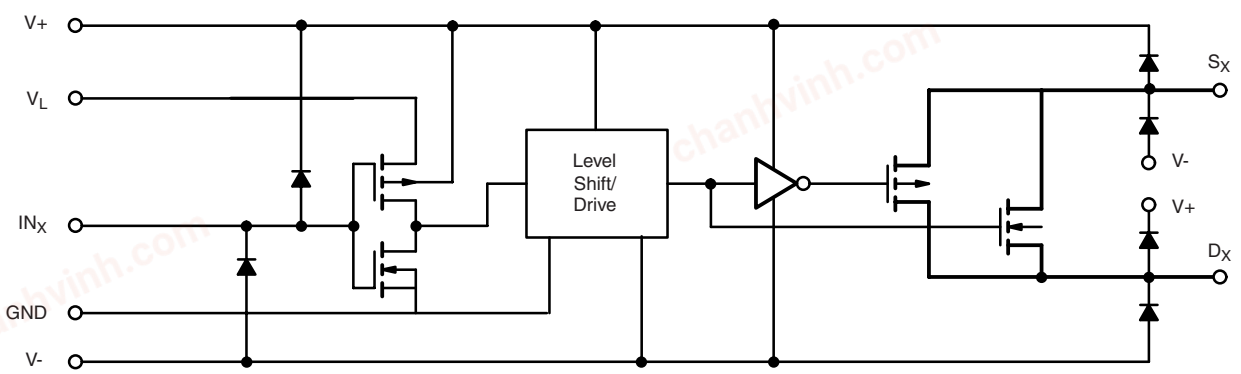


Figure 1.

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SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp.[a]	D Suffix - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	- 15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ± 10 V, I_S = 1 mA	Room Full		45	85 100	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room		2		
Source Off Leakage Current	$I_{S(off)}$	V_S = ± 14 V, V_D = ± 14 V	Room Full	- 0.5 - 5	± 0.01	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ± 14 V, V_S = ± 14 V	Room Full	- 0.5 - 5	± 0.01	0.5 5	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 14 V	Room Full	- 0.5 - 10	± 0.02	0.5 10	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	
Input Current	I_{INH} or I_{INL}	V_{INH} or V_{INL}	Full	- 1		1	µA
Input Capacitance	C_{IN}		Room		5		pF
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = 10 V See Figure 2	Room			300	ns
Turn-Off Time	t_{OFF}		Room			200	
Charge Injection	Q	C_L = 1000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		1		pC
Source-Off Capacitance	$C_{S(off)}$	V_S = 0 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		5		
Channel-On Capacitance	$C_{D(on)}$	V_D = V_S = 0 V, f = 1 MHz	Room		16		
Off Isolation	OIRR	C_L = 15 pF, R_L = 50 Ω, V_S = 1 V_{RMS}, f = 100 kHz	Room		90		dB
Channel-to-Channel Crosstalk	X_{TALK}		Room		95		
Power Supply							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			10 50	µA
Negative Supply Current	I-		Room Full	- 10 - 50			
Logic Supply Current	I_L		Room Full			10 50	
Power Supply Range for Continuous Operation	V_{OP}		Full	± 4.5		± 22	V

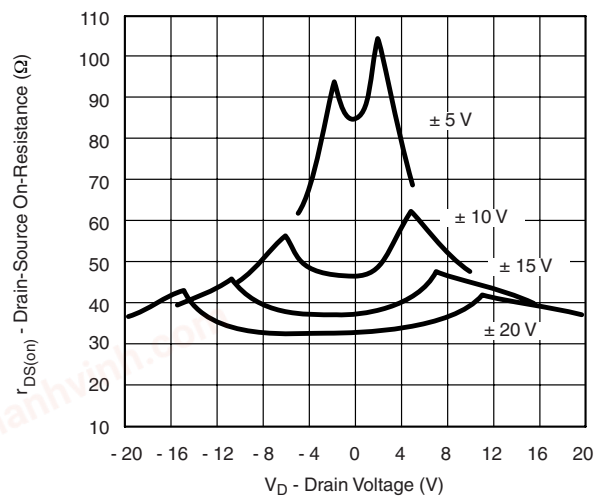
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SPECIFICATIONS for Single Supply							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	**Temp.[a]**	**D Suffix - 40 °C to 85 °C** **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = 3 V, 8 V, I_S = 1 mA	Room Full		90	160 200	Ω
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = 8 V See Figure 1	Room			300	ns
Turn-Off Time	t_{OFF}		Room			200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room		4		pC
Power Supply							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			10 50	µA
Negative Supply Current	I-		Room Full	- 10 - 50			
Logic Supply Current	I_L		Room Full			10 50	
Power Supply Range for Continuous Operation	V_{OP}		Full	+ 4.5		+ 25	V

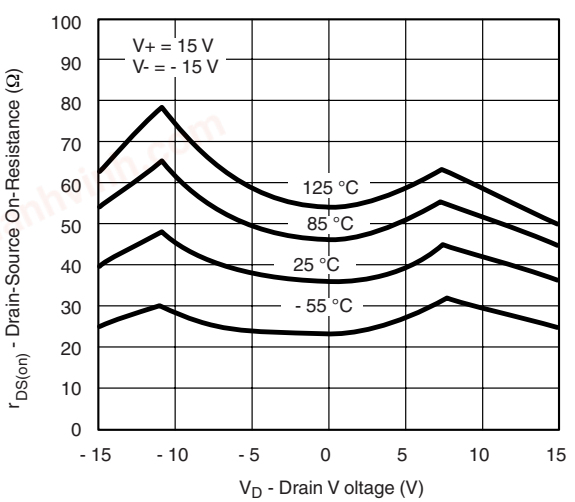
Notes:
a. Room = 25 °C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



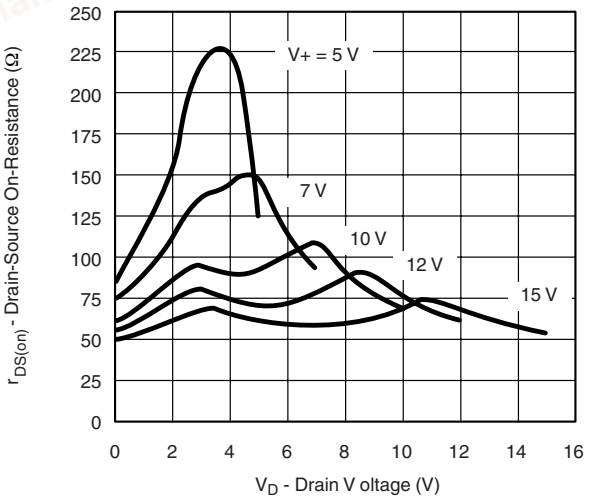
$r_{DS(on)}$ vs. V_D and Power Supply Voltages



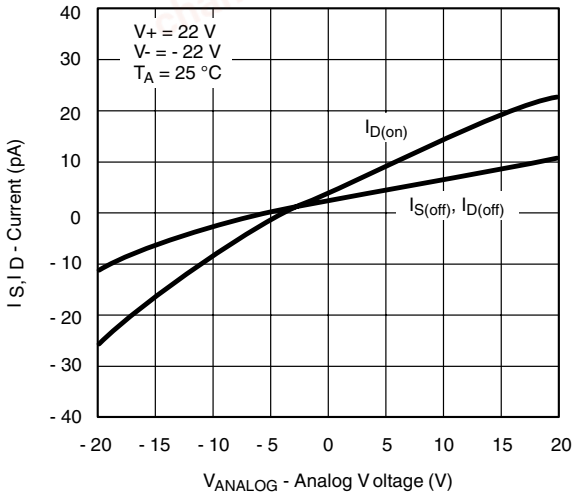
$r_{DS(on)}$ vs. V_D and Temperature

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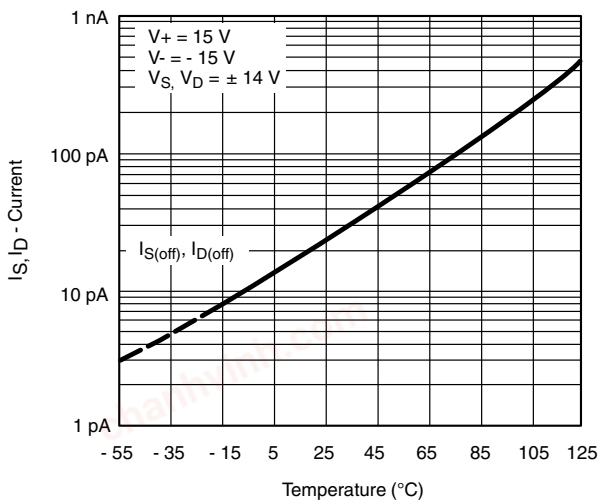
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



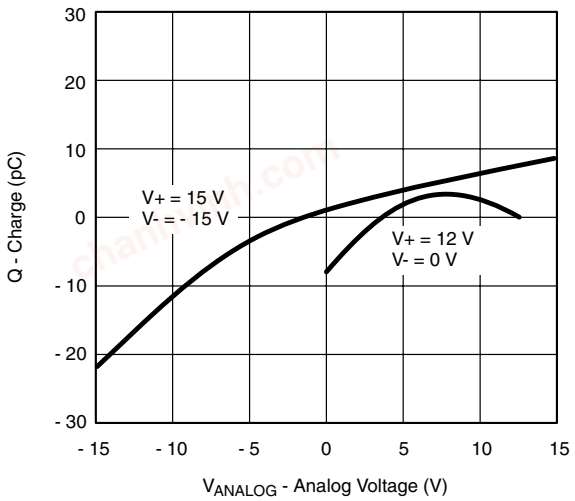
$r_{DS(on)}$ vs. V_D and Single Power Supply Voltages



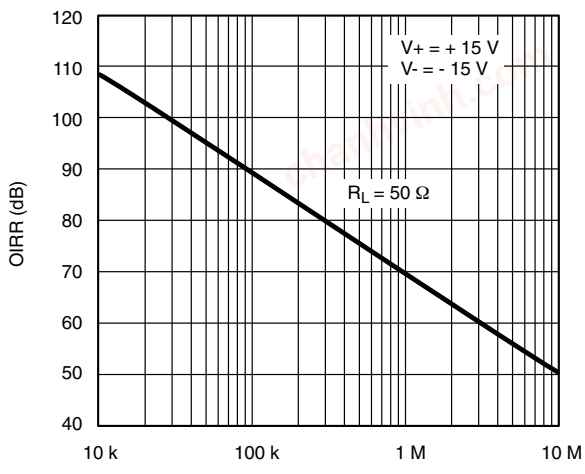
Leakage Currents vs. Analog Voltage



Leakage Current vs. Temperature



Q_S, Q_D - Charge Injection vs. Analog Voltage



Off Isolation vs. Frequency

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TEST CIRCUITS

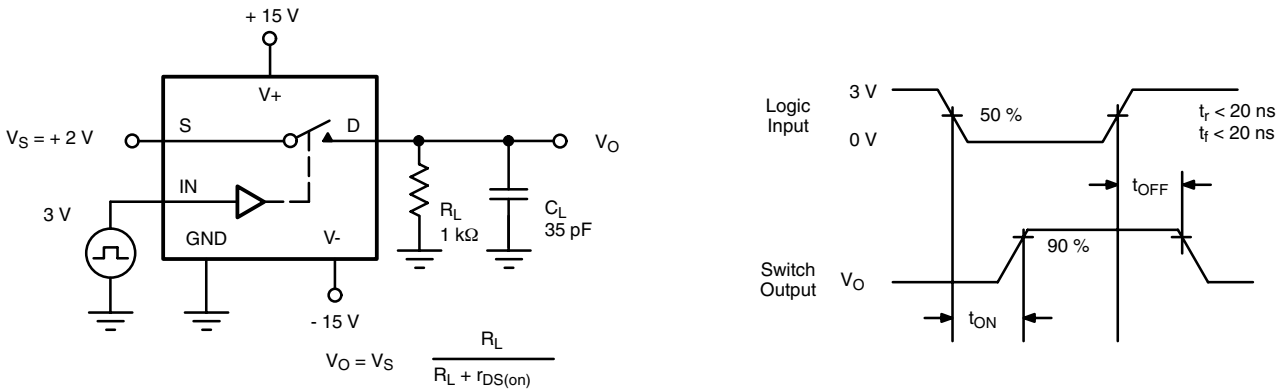


Figure 2. Switching Time

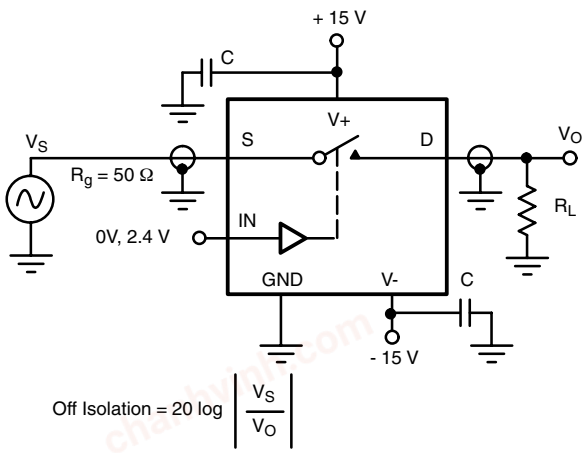


Figure 3. Off Isolation

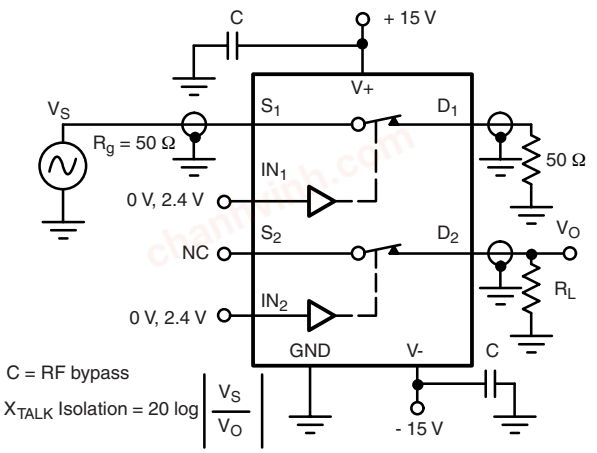
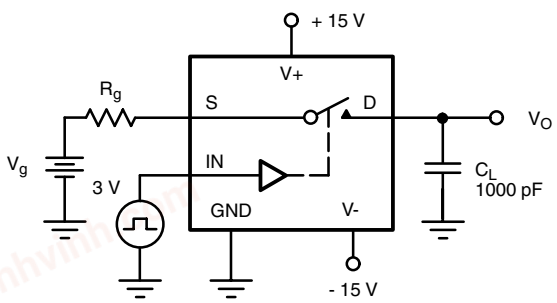
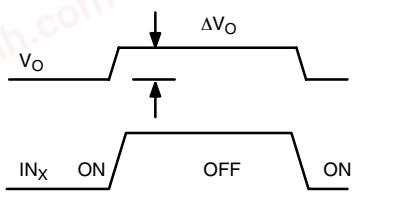


Figure 4. Channel-to-Channel Crosstalk



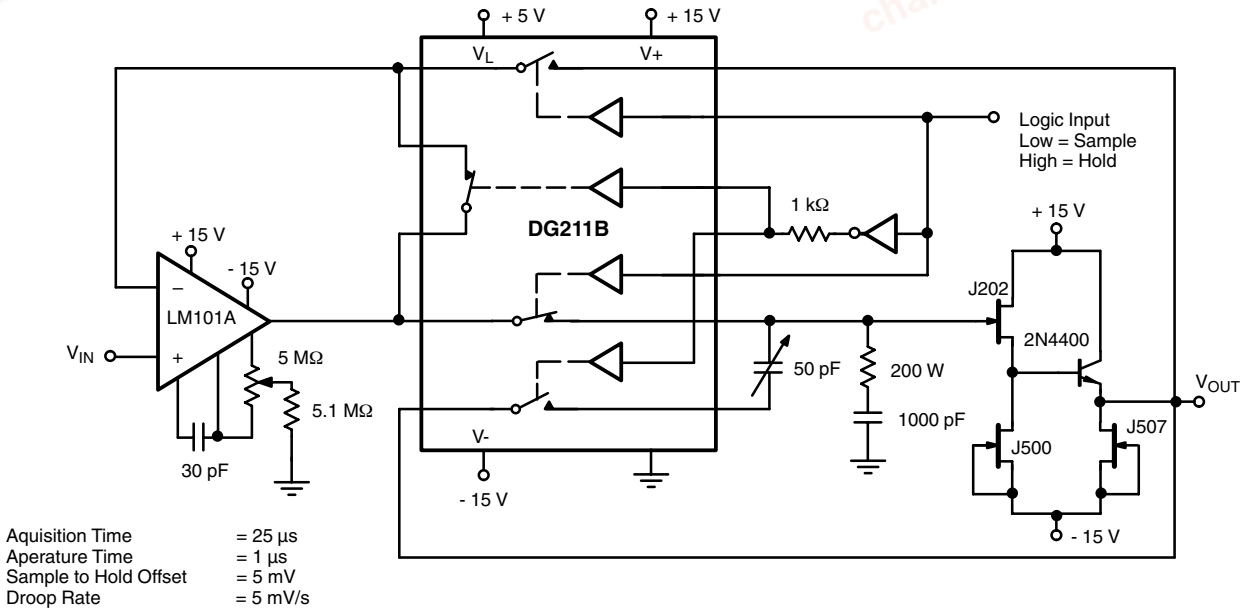


ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is Q = C_L x ΔV_O

Figure 5. Charge Injection

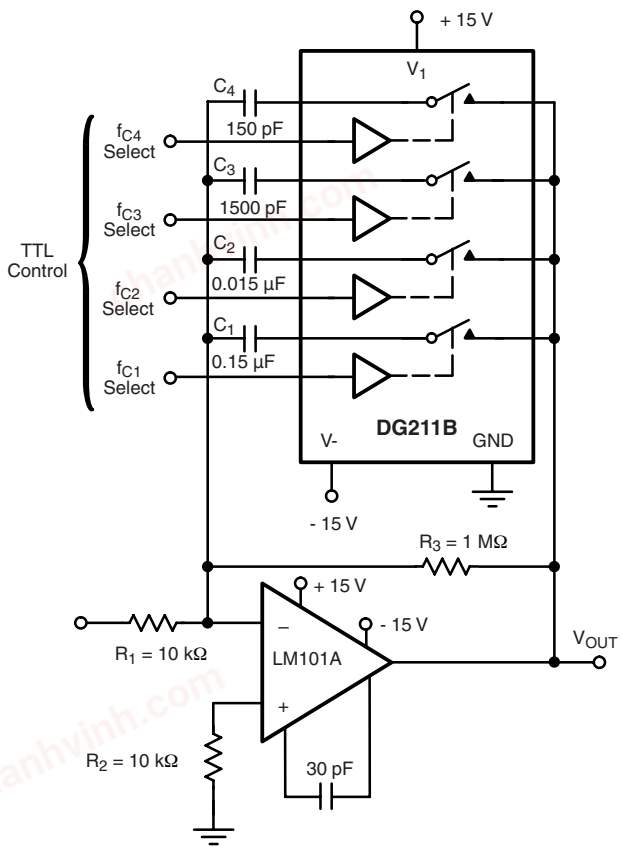
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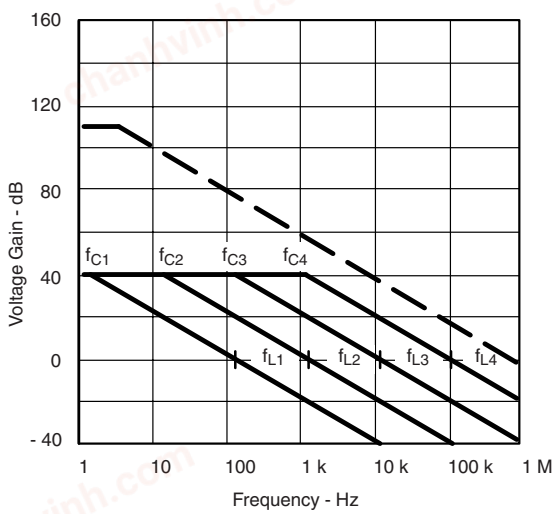
APPLICATIONS



Aquisition Time = 25 µs
Aperature Time = 1 µs
Sample to Hold Offset = 5 mV
Droop Rate = 5 mV/s

Figure 6. Sample-and-Hold





$$A_L \text{ (Voltage Gain Below Break Frequency)} = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (Break Frequency)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (Unity Gain Frequency)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{Max Attenuation} = \frac{r_{DS(on)}}{10\ k\Omega} \approx -47 \text{ dB}$$

Figure 7. Active Low Pass Filter with Digitally Selected Break Frequency

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APPLICATIONS

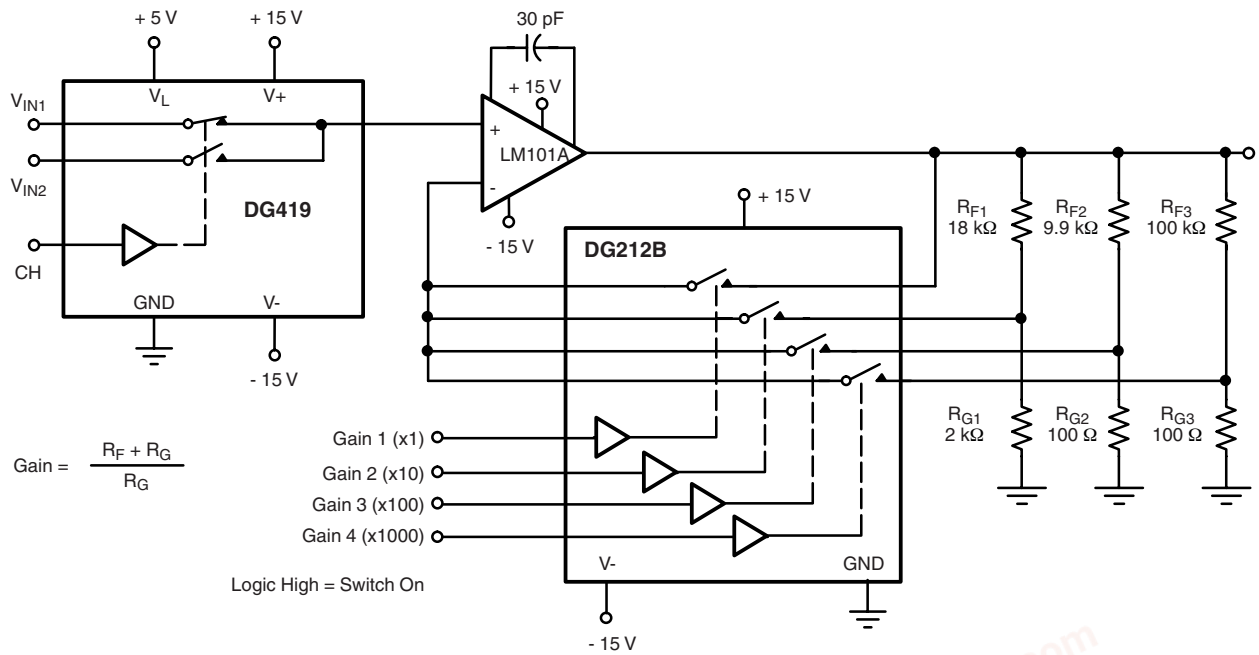


Figure 8. A Precision Amplifier with Digitally Programable Input and Gains

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70040.

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Package Information

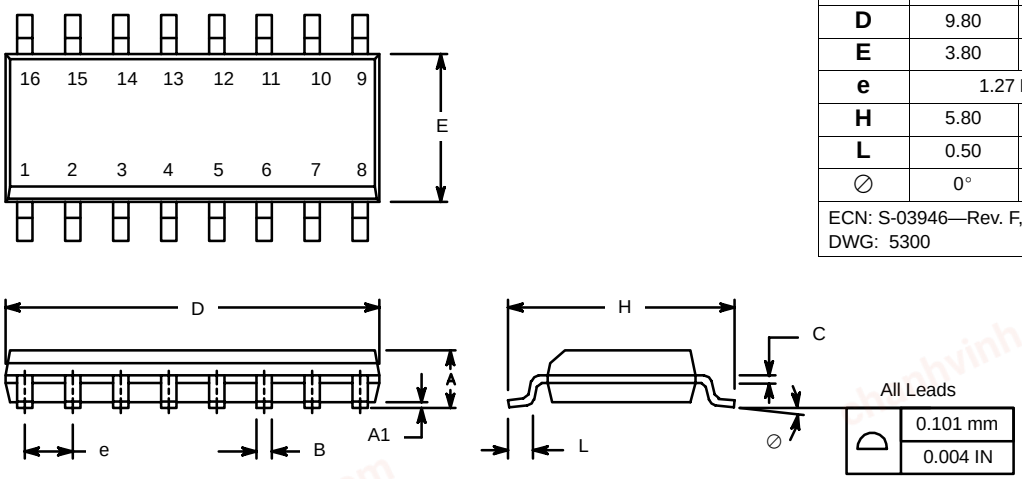
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SOIC (NARROW): 16-LEAD

JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

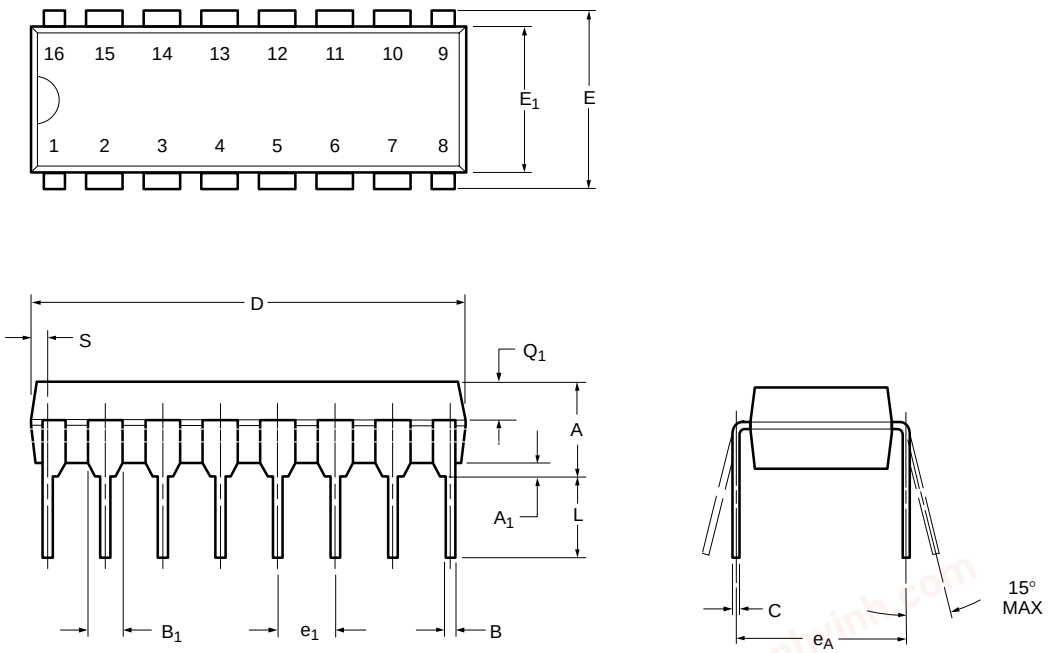


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Package Information

Vishay Siliconix

PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060

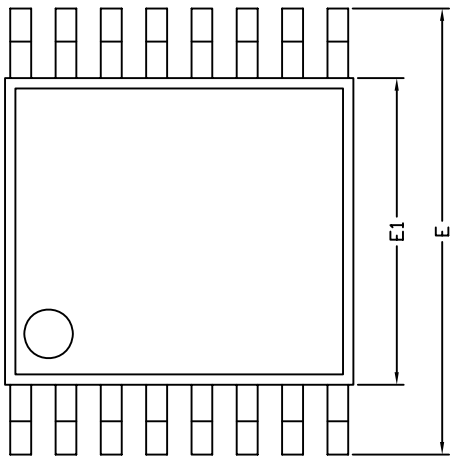
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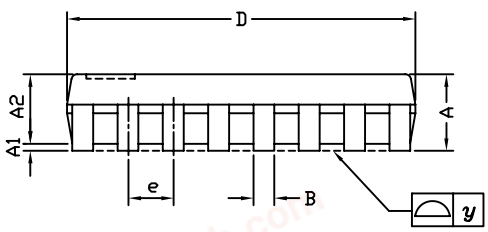
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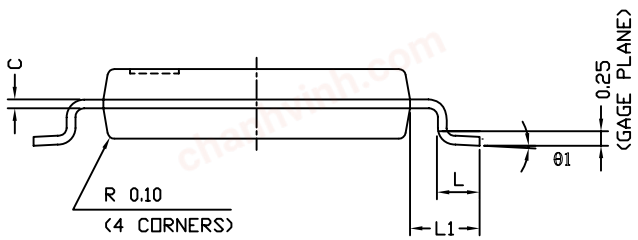
Package Information

Vishay Siliconix

TSSOP: 16-LEAD



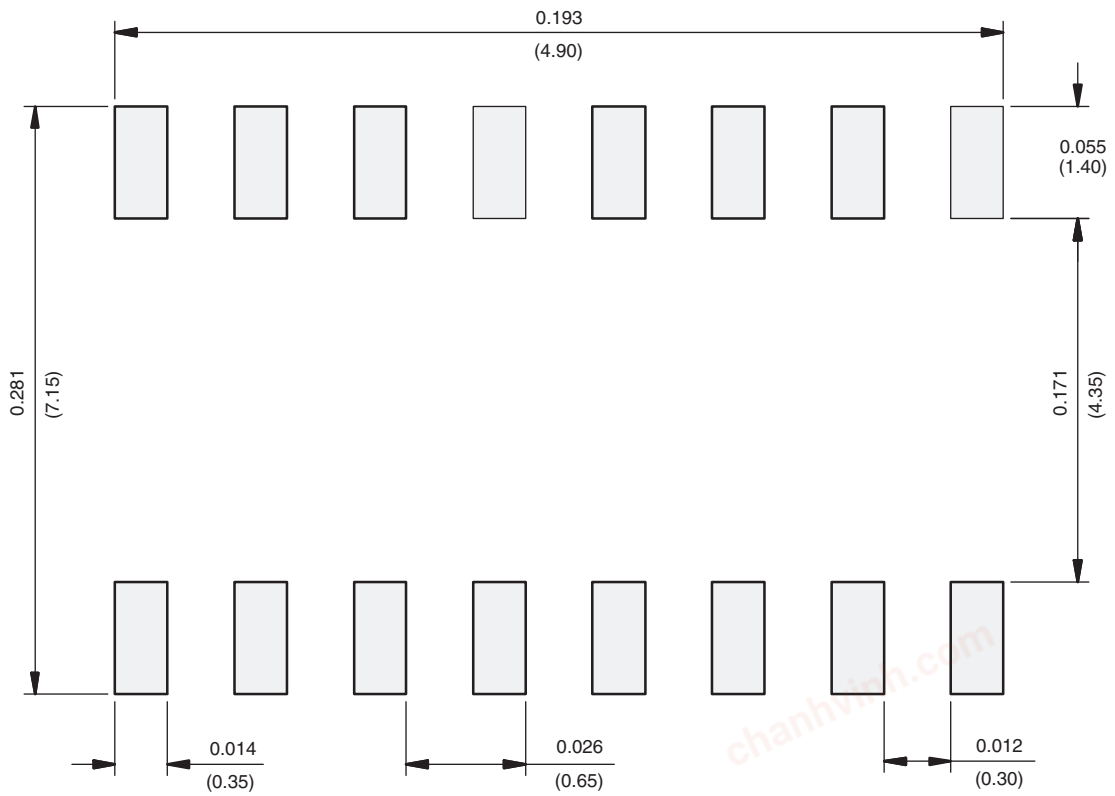




Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

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RECOMMENDED MINIMUM PAD FOR TSSOP-16

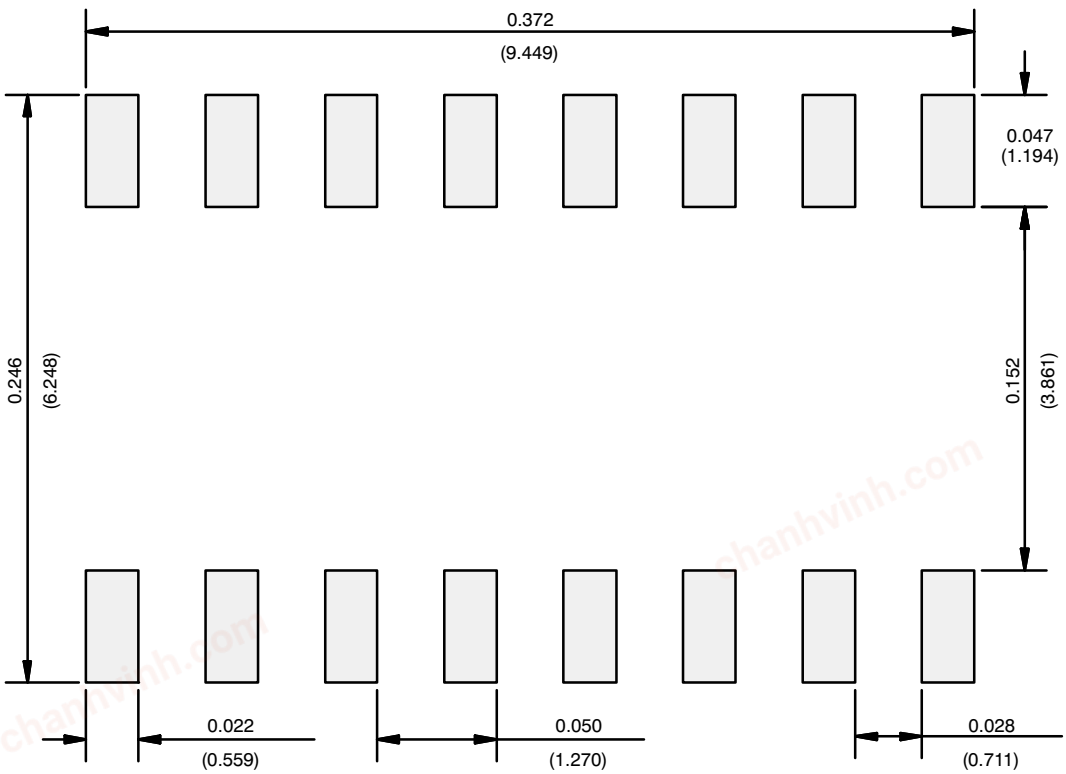


Recommended Minimum Pads
Dimensions in inches (mm)

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RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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