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TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC164P,TC74AC164F,TC74AC164FN,TC74AC164FT

8-Bit Shift Register (S-IN, P-OUT)

The TC74AC164 is an advanced high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of a serial-in, parallel-out 8-bit shift register with a CLOCK input and an overriding $\overline{\text{CLEAR}}$ input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

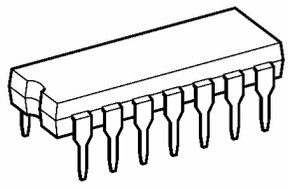
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: f_{max} = 170 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 8 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Symmetrical output impedance:
  $|I_{OH}| = I_{OL}$ = 24 mA (min)
  Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 V to 5.5 V
- Pin and function compatible with 74F164

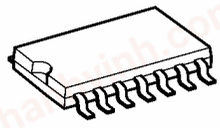
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74AC164P



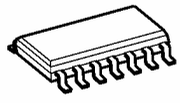
DIP14-P-300-2.54

TC74AC164F



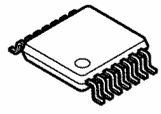
SOP14-P-300-1.27A

TC74AC164FN



SOL14-P-150-1.27

TC74AC164FT



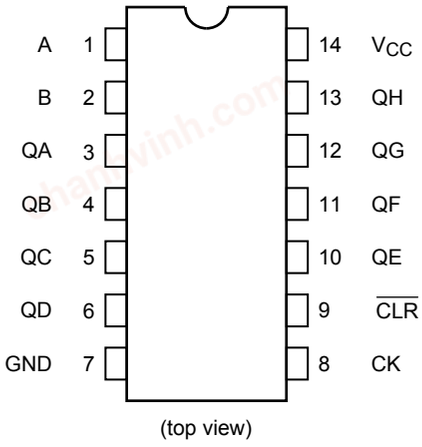
TSSOP14-P-0044-0.65A

Weight

DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)

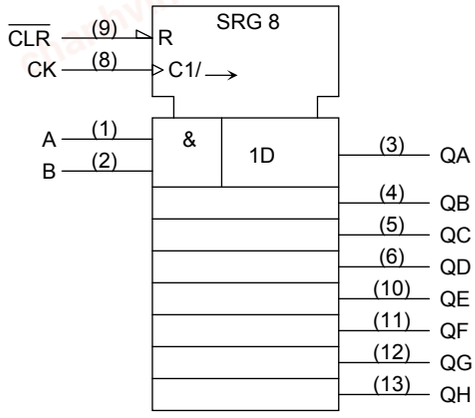
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Pin Assignment



(top view)

IEC Logic Symbol



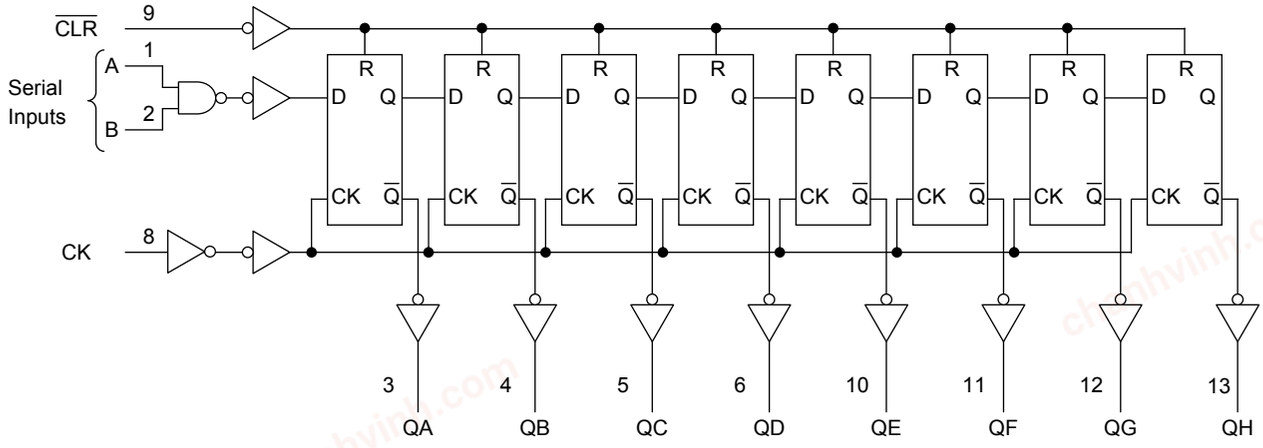
Truth Table

Inputs				Outputs			
$\overline{CLR}$	CK	Serial In		QA	QB	⋯	QH
		A	B				
L	X	X	X	L	L	⋯	L
H	↓	X	X	No Change			
H	↑	L	X	L	QA_n	⋯	QG_n
H	↑	X	L	L	QA_n	⋯	QG_n
H	↑	H	H	H	QA_n	⋯	QG_n

X: Don't care

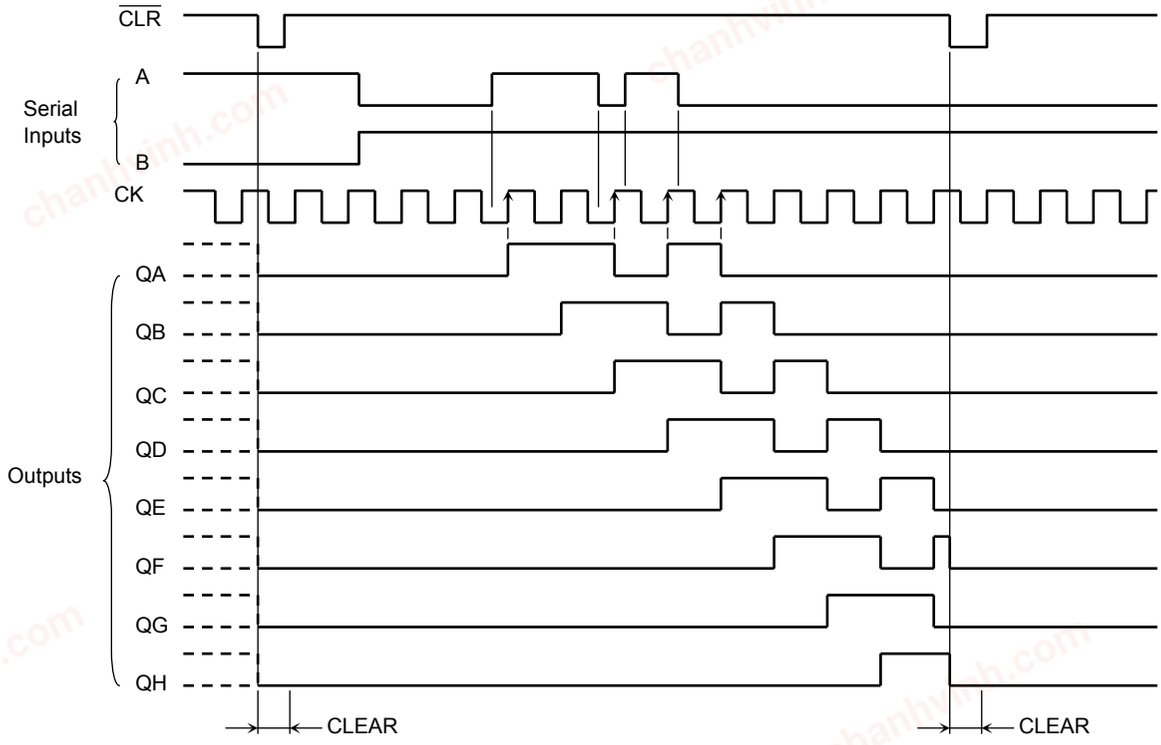
QA_n to QG_n: The level of QA to QG, respectively, before the most recent positive edge of the clock.

System Diagram



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Timing Chart



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±50	mA
DC output current	I_{OUT}	±50	mA
DC V_{CC}/ground current	I_{CC}	±200	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40°C to 65°C. From Ta = 65°C to 85°C a derating factor of −10 mW/°C should be applied up to 300 mW.

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Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 (V_{CC} = 3.3 ± 0.3 V) 0 to 20 (V_{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −24 mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = −75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 12 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 24 mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75 mA (Note)	5.5	—	—	—	—	1.65	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	μA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

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Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = −40 to 85°C	Unit
			V_{CC} (V)	Limit	Limit	
Minimum pulse width (CK)	$t_{w(L)}$ $t_{w(H)}$	—	3.3 ± 0.3 5.0 ± 0.5	9.0 5.0	10.0 6.0	ns
Minimum pulse width ($\overline{CLR}$)	$t_{w(L)}$	—	3.3 ± 0.3 5.0 ± 0.5	9.0 5.0	10.0 6.0	ns
Minimum set-up time	t_s	—	3.3 ± 0.3 5.0 ± 0.5	7.0 4.0	7.0 4.0	ns
Minimum hold time	t_h	—	3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	ns
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	3.3 ± 0.3 5.0 ± 0.5	8.5 5.0	8.5 5.0	ns

AC Characteristics ($C_L = 50$ pF, $R_L = 500\ \Omega$, input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	3.3 ± 0.3 5.0 ± 0.5	— —	9.6 6.6	16.3 9.8	1.0 1.0	18.6 11.2	ns
Propagation delay time ($\overline{CLR}$-Q)	t_{pHL}	—	3.3 ± 0.3 5.0 ± 0.5	— —	8.0 6.0	15.4 11.0	1.0 1.0	17.5 12.5	ns
Maximum clock frequency	f_{max}	—	3.3 ± 0.3 5.0 ± 0.5	45 85	100 150	— —	45 80	— —	MHz
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note)		—	110	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

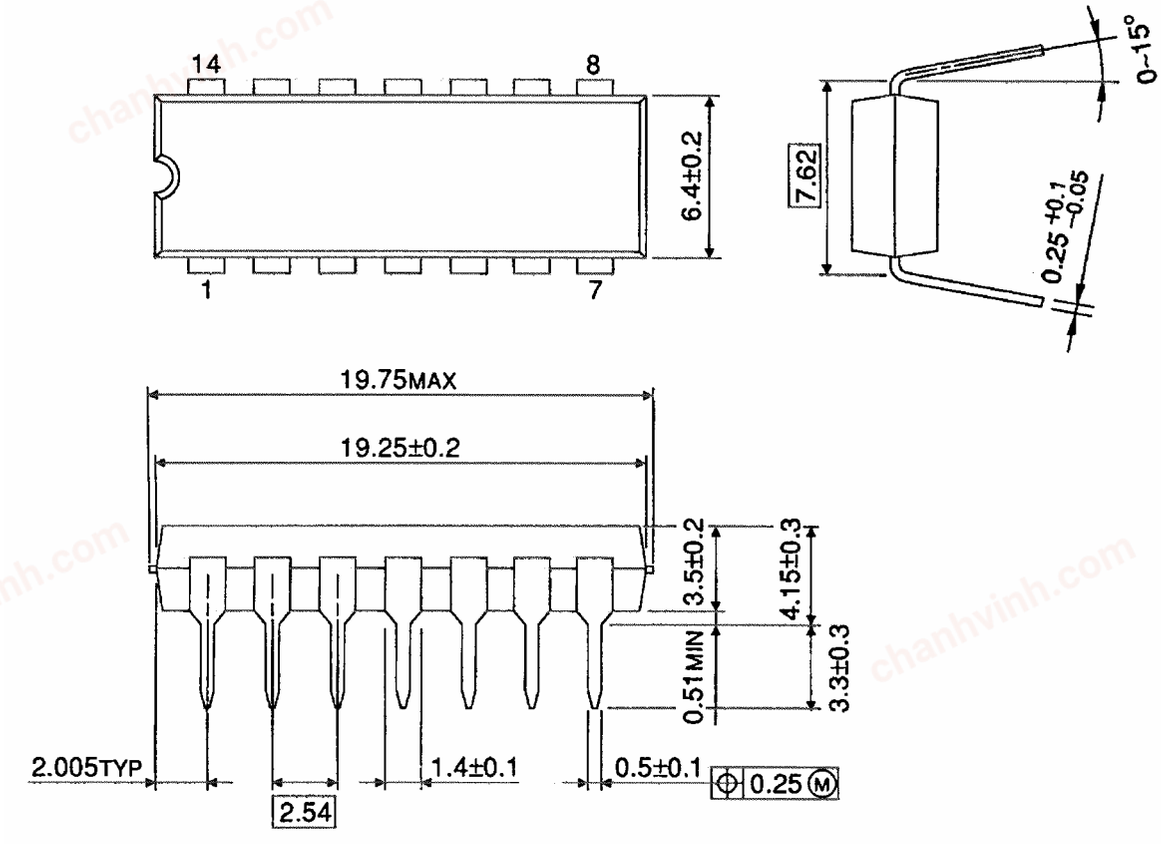
Average operating current can be obtained by the equation:

$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

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Package Dimensions

DIP14-P-300-2.54 Unit : mm

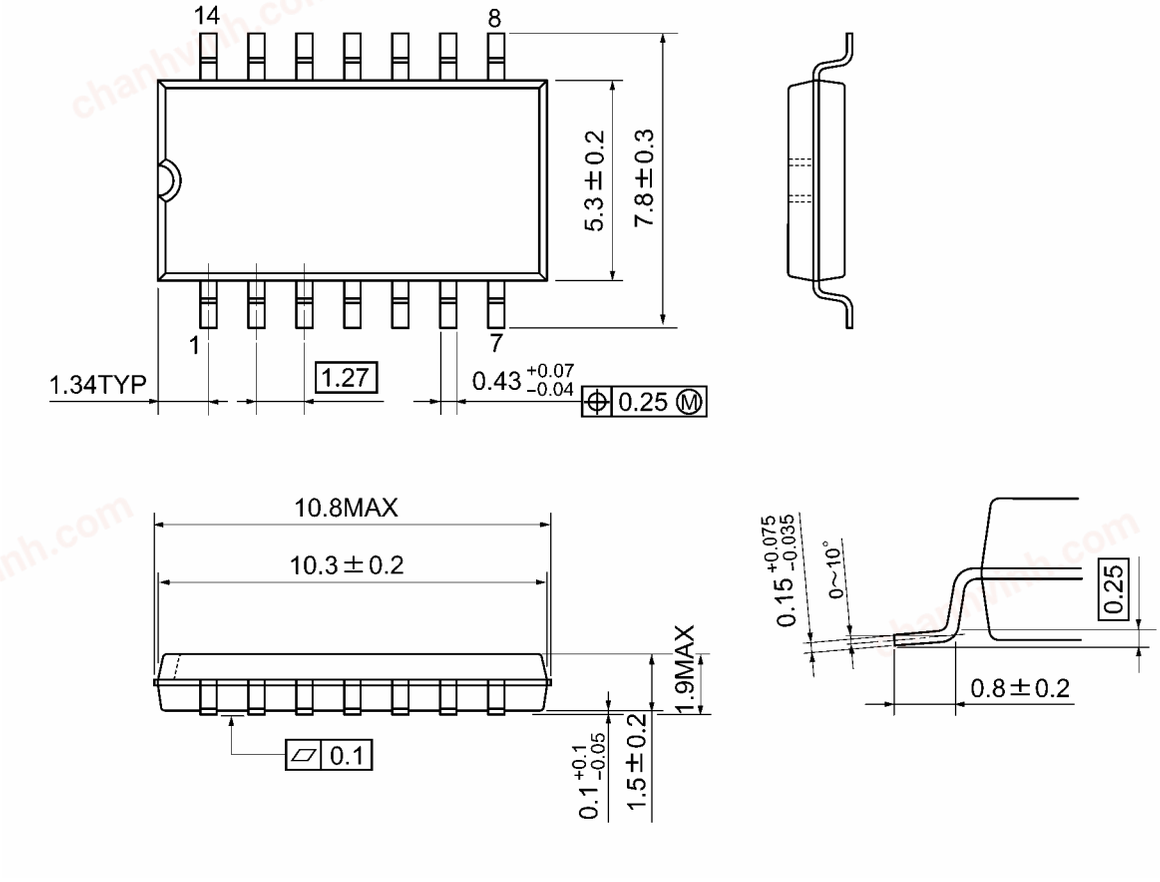


Weight: 0.96 g (typ.)

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Package Dimensions

SOP14-P-300-1.27A Unit: mm

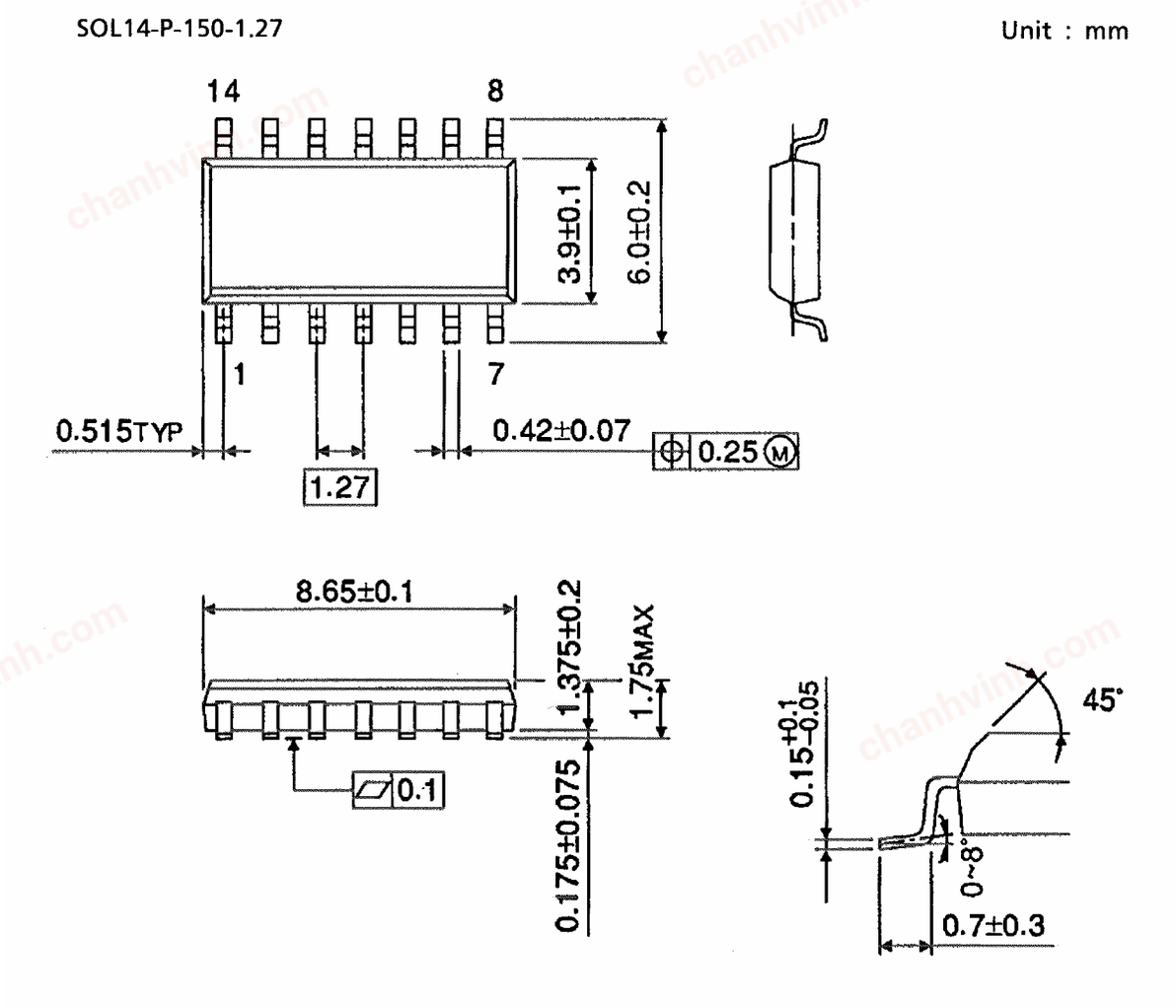


Weight: 0.18 g (typ.)

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Package Dimensions (Note)

SOL14-P-150-1.27 Unit : mm



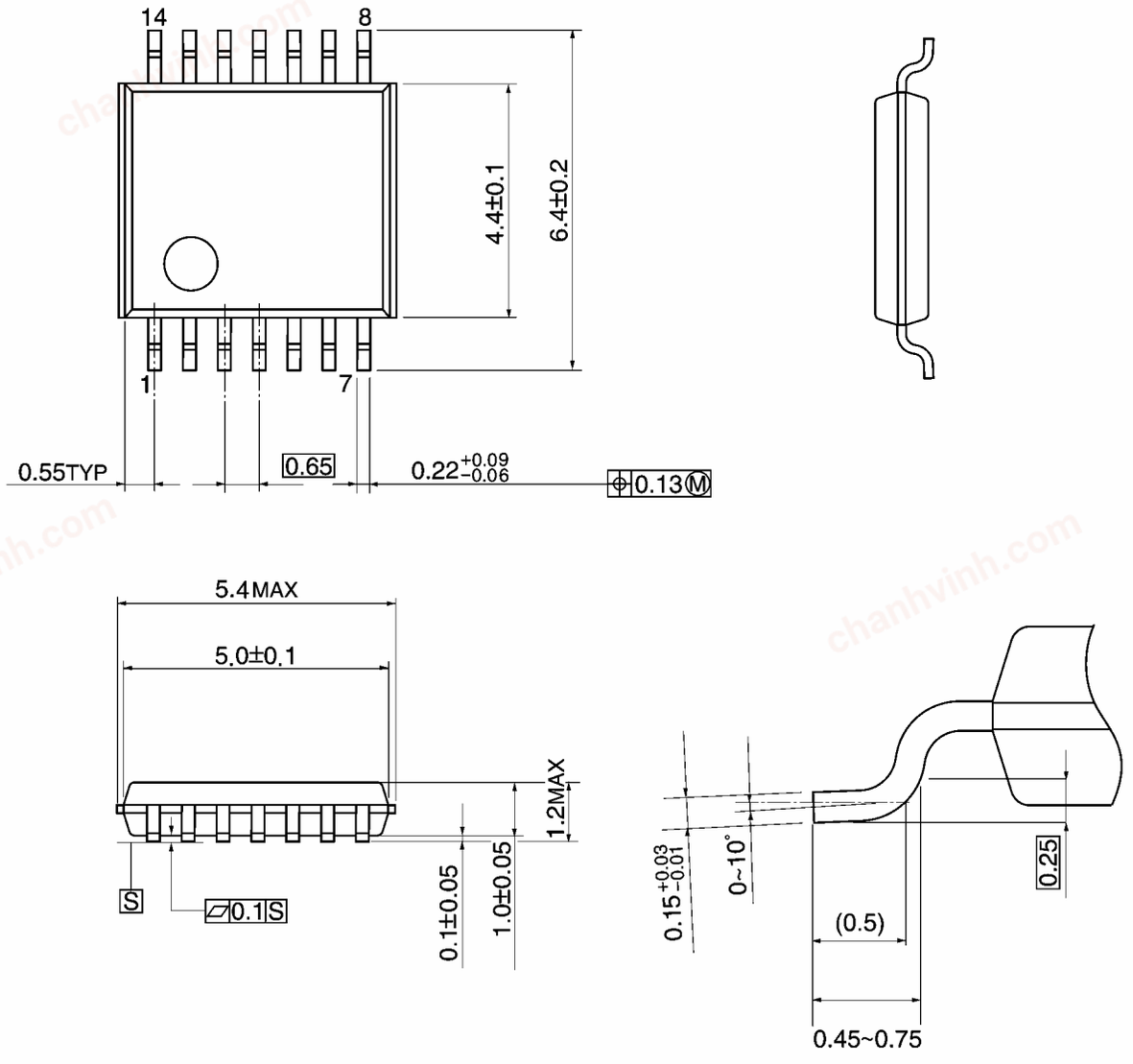
Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

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Package Dimensions

TSSOP14-P-0044-0.65A Unit: mm



Weight: 0.06 g (typ.)

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20070701-EN GENERAL

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