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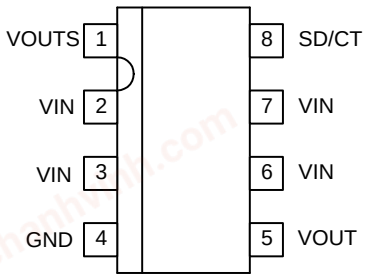
# UCC284–5, UCC284–12, UCC284–ADJ, UCC384–5, UCC384–12, UCC384–ADJ
# LOW-DROPOUT 0.5-A NEGATIVE LINEAR REGULATOR

SLUS234D – JANUARY 2000 – REVISED FEBRUARY 2002

- **Precision Negative Series Pass Voltage Regulation**
- **0.2 V Dropout at 0.5 A**
- **Wide Input Voltage Range –3.2 V to –15 V**
- **Low Quiescent Current Irrespective of Load**
- **Simple Logic Shutdown Interfacing**
- **–5 V, –12 V, and Adjustable Output**
- **2.5% Duty Cycle Short Circuit Protection**

**DP PACKAGE**
**(FRONT VIEW)**




## description

The UCC384-x family of negative linear-series pass regulators is tailored for low-dropout applications where low-quiescent power is important. Fabricated with a BCDMOS technology ideally suited for low input-to-output differential applications, the UCC384-x passes 0.5 A while requiring only 0.2 V of input-voltage headroom. Dropout voltage decreases linearly with output current, so that dropout at 50 mA is less than 20 mV.

Quiescent current consumption for the device under normal (non-dropout) conditions is typically 200 µA. An integrated charge pump is internally enabled only when the device is operating near dropout with low VIN. This ensured that the device meets the dropout specifications even for maximum load current and a VIN of –3.2 V with only a modest increase in quiescent current. Quiescent current is always less than 350 µA, with the charge pump enabled. The quiescent current of the UCC384 does not increase with load current.

Short-circuit current is internally limited. The device responds to a sustained overcurrent condition by turning off after a $t_{ON}$ delay. The device then stays off for a period, $t_{OFF}$, that is 40 times the $t_{ON}$ delay. The device then begins pulsing on and off at the $t_{ON}/t_{OFF}$ duty cycle of 2.5%. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accommodate normal operation. An external capacitor sets the on time. The off time is always 40 times $t_{ON}$.

The UCCx84-x can be shutdown to 45 µA (maximum) by pulling the SD/CT pin more positive than –0.7 V. To allow for simpler interfacing, the SD/CT pin may be pulled up to 6 V above the ground pin without turning on clamping diodes.

Internal power dissipation is further controlled with thermal-overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 140°C. The chip remains off until the temperature has dropped 20°C ($T_J$ = 120°C).

**AVAILABLE OPTIONS**

| $T_A$ | OUTPUT VOLTAGE (V) | PACKAGE DEVICES |
|---|---|---|
| | TYP | (SOIC) DP |
| –40°C to 85°C | –5 | UCC284DP–5 |
| | –12 | UCC284DP–12 |
| | ADJ | UCC284DP–ADJ |
| 0°C to 70°C | –5 | UCC384DP–5 |
| | –12 | UCC384DP–12 |
| | ADJ | UCC384DP–ADJ |

† All package types are available taped and reeled. Add TR suffix to device type (e.g. UCC284DP–5TR) to order quantities of 3000 devices per reel.

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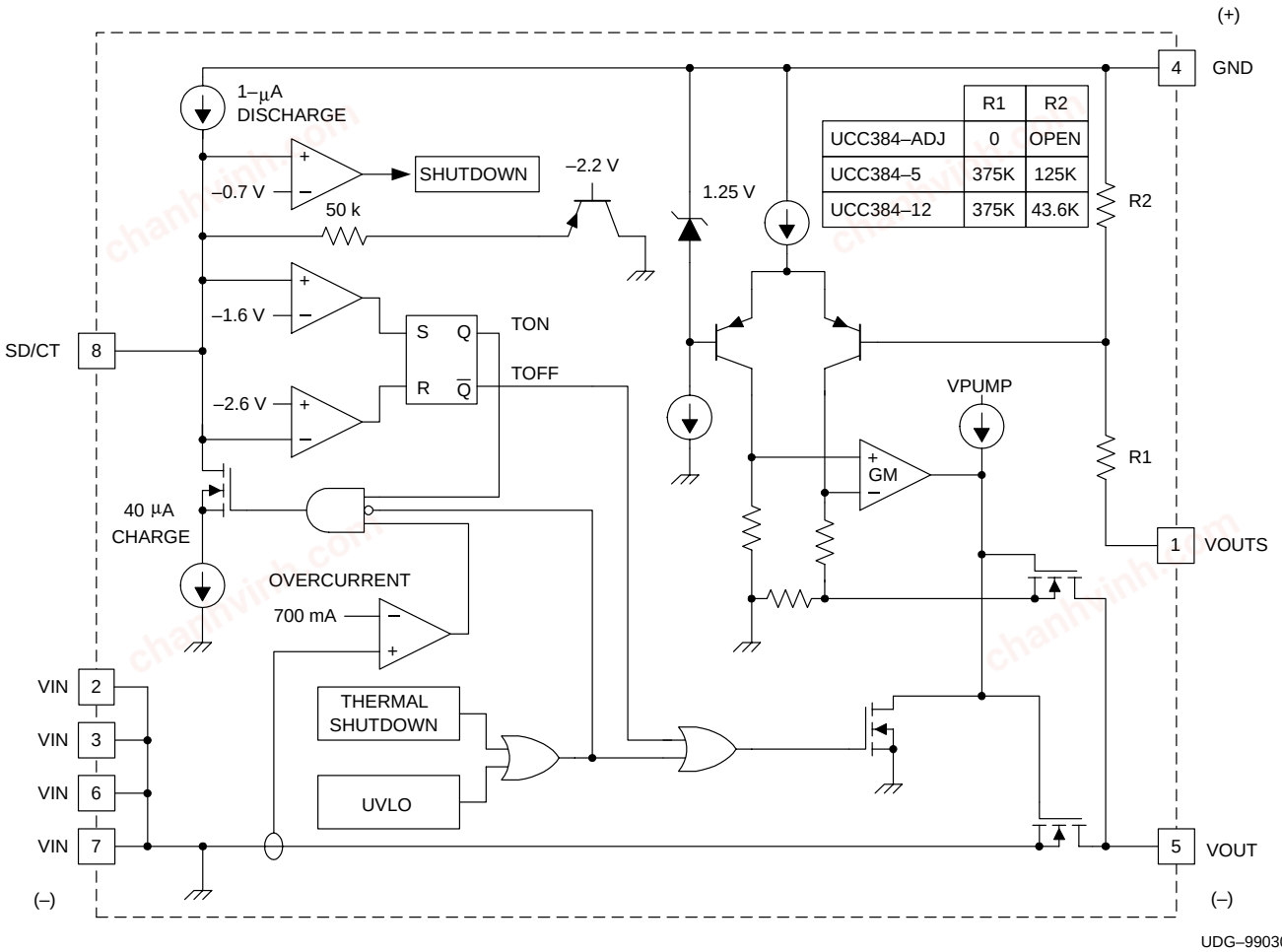
## functional block diagram




## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

| | |
|---|---|
| Input voltage range‡, $V_{IN}$ | –16 V |
| Shutdown voltage range, SD/CT | –5 V to 6 V |
| Operating virtual junction temperature range, $T_J$ | –55°C to 150°C |
| Storage temperature range $T_{stg}$ | –65°C to 150°C |
| Lead temperature (Soldering, 10 seconds) | 300°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to ground. Currents are positive into and negative out of the specified terminals.

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**electrical characteristics $T_A$ = 0°C to 70°C for the UCC384 and –40°C to 85°C for the UCC284, VIN = VOUT – 1.5 V, $I_{OUT}$ = 0 mA, $C_{OUT}$ = 4.7 µF, and CT = 0.015 µF. For UCC384–ADJ, VOUT is set to –3.3V (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **UCC384–5 Fixed –5-V 0.5-A Regulation Section** | | | | | |
| Output voltage | $T_A$ = 25°C | –5.075 | –5 | –4.925 | V |
| | Over all conditions | –5.100 | | –4.850 | V |
| Line regulation | VIN = –5.2 V to –15 V | | 1.5 | 10 | mV |
| Load regulation | $I_{OUT}$ = 0 mA to 0.5 A | | 0.1 | 0.25 | % |
| Output noise voltage | $T_A$ = 25°C, BW = 10 Hz to 10 kHz | | 200 | | µVRMS |
| Dropout voltage, VOUT – VIN | $I_{OUT}$ 0.5 A, VOUT = –4.8 V | | 0.20 | 0.50 | V |
| | $I_{OUT}$ 50 mA, VOUT = –4.8 V | | 20 | 50 | mV |
| **UCC384–5 Fixed –5-V 0.5-A Power Supply Section** | | | | | |
| Input voltage range | | –15 | | –5.2 | V |
| Quiescent current charge pump on | VIN = –4.85 V, See Note 1 | | 280 | 350 | µA |
| Quiescent current | VIN = –15 V | | 200 | 250 | µA |
| Quiescent current in shutdown | VIN = –13 V, SD/CT = 0 V, $T_A$ = 0°C to 85°C, See Note 2 | | 15 | 45 | µA |
| | VIN = –13 V, SD/CT = 0 V, $T_A$ = –40°C to 0°C, See Note 2 | | | 100 | µA |
| Shutdown threshold | At shutdown pin (SD/CT) | –1.0 | –0.7 | –0.4 | V |
| Shutdown input current | SD/CT = 0 V | 5 | 10 | 25 | µA |
| Output leakage in shutdown | VIN = –15 V, VOUT = 0 V, See Note 3 | | 1 | 50 | µA |
| Overtemperature shutdown | | | 140 | | °C |
| Overtemperature hysteresis | | | 20 | | °C |
| **UCC384–5 Fixed –5-V 0.5-A Current Limit Section** | | | | | |
| Peak current limit | VOUT = 0 V | 0.7 | 1.1 | 1.5 | A |
| Overcurrent threshold | | 0.55 | 0.7 | 0.9 | A |
| Current limit duty cycle | VOUT = 0 V | | 2.5 | 4 | % |
| Overcurrent time out, $t_{ON}$ | VOUT = 0 V | 300 | 500 | 700 | µs |
| **UCC384–12 Fixed 12-V 0.5-A Regulation Section** | | | | | |
| Output voltage | $T_A$ = 25°C | –12.18 | –12 | –11.82 | V |
| | Over all conditions | –12.24 | | –11.64 | V |
| Line regulation | VIN = –12.5 V to –15 V | | 5 | 15 | mV |
| Load regulation | $I_{OUT}$= 0 mA to 0.5 A | | 0.1 | 0.3 | % |
| Output noise voltage | $T_A$ = 25°C BW = 10 Hz to 10 kHz | | 200 | | µVRMS |
| Dropout voltage, VOUT – VIN | $I_{OUT}$ 0.5 A, VOUT = –11.6 V | | 0.15 | 0.5 | V |
| | $I_{OUT}$ 50 mA, VOUT = –11.6 V | | 15 | 50 | mV |
| **UCC384–12 Fixed –12 V-0.5-A Power Supply Section** | | | | | |
| Input voltage range | | –15 | | –12.5 | V |
| Quiescent current | VIN = –15 V | | 220 | 350 | µA |
| Quiescent current in shutdown | VIN = –13 V, SD/CT = 0 V, $T_A$ = 0°C to 85°C, See Note 2 | | 15 | 45 | µA |
| | VIN = –13 V, SD/CT = 0 V, $T_A$ = –40°C to 0°C, See Note 2 | | | 100 | µA |

NOTES: 1. The internal charge pump is enabled only for dropout condition with low VIN. Only in this condition is the charge pump required to provide additional output FET fate drive to maintain dropout specifications. For conditions where the charge pump is not required, it is disabled, which lowers overall device power consumption.
2. Ensured by design. Not production tested.
3. In the application during shutdown mode, output leakage current adds to quiescent current.

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## electrical characteristics $T_A$ = 0°C to 70°C for the UCC384 and –40°C to 85°C for the UCC284, VIN = VOUT – 1.5 V, $I_{OUT}$ = 0 mA, $C_{OUT}$ = 4.7 µF, and CT = 0.015 µF. For UCC384–ADJ, VOUT is set to –3.3V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **UCC384–12 Fixed –12 V-0.5-A Power Supply Section (continued)** | | | | | |
| Shutdown threshold | At shutdown pin (SD/CT) | –1.0 | –0.7 | –0.4 | V |
| Shutdown input current | SD/CT = 0 V | 5 | 10 | 25 | µA |
| Output leakage in shutdown | VIN = –15 V, VOUT = 0 V, See Note 3 | | 1 | 50 | µA |
| Overtemperature shutdown | | | 140 | | °C |
| Overtemperature hysteresis | | | 20 | | °C |
| **UCC384–12 Fixed –12-V 0.5-A Current Limit Section** | | | | | |
| Peak current limit | VOUT = 0 V | 0.7 | 1.1 | 1.5 | A |
| Overcurrent threshold | | 0.55 | 0.7 | 0.9 | A |
| Current limit duty cycle | VOUT = 0 V | | 2.5 | 4 | % |
| Overcurrent time out, $t_{ON}$ | VOUT = 0 V | 300 | 500 | 700 | µs |
| **UCC384–ADJ Adjustable 0.5-A Regulation Section** | | | | | |
| Reference voltage | $T_A$ = 25°C | –1.27 | –1.25 | –1.23 | V |
| | Over temperature | –1.275 | | –1.215 | V |
| Line regulation | VIN = –3.5 V to –15 V, VOUT = VOUTS | | 0.5 | 3 | mV |
| Load regulation | $I_{OUT}$ = 0 mA to 0.5 A | | 0.1 | 0.18 | % |
| Output noise voltage | BW = 10 Hz to 10 kHz, $T_A$ = 25°C | | 200 | | µVRMS |
| Dropout voltage, VOUT – VIN | $I_{OUT}$ 0.5 A, VOUT = –3.15 V | | 0.25 | 0.5 | V |
| | $I_{OUT}$ 50 mA, VOUT = –3.15 V | | 25 | 50 | mV |
| Sense pin input current | | | 100 | 250 | nA |
| **UCC384–ADJ Adjustable 0.5-A Power Supply Section** | | | | | |
| Input voltage range | | –15 | | –3.5 | V |
| Undervoltage lockout | | –3.2 | –2.95 | –2.7 | V |
| Quiescent current charge pump on | VIN = –3.15 V, See Note 1 | | 200 | 350 | µA |
| Quiescent current | VIN = –15 V | | 200 | 250 | µA |
| Quiescent current in shutdown | VIN = –13 V, SD/CT = 0 V, $T_A$ = 0°C to 85°C, See Note 2 | | 15 | 45 | µA |
| | VIN = –13 V, SD/CT = 0 V, $T_A$ = –40°C to 0°C, See Note 2 | | | 100 | µA |
| Shutdown threshold | At shutdown pin (SD/CT) | –1.0 | –0.7 | –0.4 | V |
| Shutdown input current | SD/CT = 0V | 5 | 10 | 25 | µA |
| Output leakage in shutdown | VIN = –15V, VOUT = 0 V, See Note 3 | | 1 | 50 | µA |
| Overtemperature shutdown | | | 140 | | °C |
| Overtemperature hysteresis | | | 20 | | °C |
| **UCC384–ADJ Adjustable 0.5-A Current Limit Section** | | | | | |
| Peak current limit | VOUT = 0 V | 0.7 | 1.1 | 1.5 | A |
| Overcurrent threshold | | 0.55 | 0.7 | 0.9 | A |
| Current limit duty cycle | VOUT = 0 V | | 2.5 | 4 | % |
| Overcurrent time out, $t_{ON}$ | VOUT = 0 V | 300 | 500 | 700 | µs |

NOTES: 1. The internal charge pump is enabled only for dropout condition with low VIN. Only in this condition is the charge pump required to provide additional output FET fate drive to maintain dropout specifications. For conditions where the charge pump is not required, it is disabled, which lowers overall device power consumption.
2. Ensured by design. Not production tested.
3. In the application during shutdown mode, output leakage current adds to quiescent current.

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### pin descriptions

**GND:** This is the low noise ground reference input. All voltages are measured with respect to the GND pin.

**SD/CT:** This is the shutdown pin and also the short-circuit timing pin. Pulling this pin more positive than –0.7 V puts the circuit in a low-current shutdown mode. Placing a timing capacitor between this pin and GND sets the short-circuit charging time, $t_{ON}$ during an overcurrent condition. During an overcurrent condition, the output pulses at approximately a 2.5% duty cycle.

> **NOTE:** The CT capacitor must be connected between this pin and GND, not VIN, to assure that the SD/CT pin is not pulled significantly negative during power-up. This pin should not be externally driven more negative than –5 V or the device will be damaged.

**VIN:** This is the negative input supply. Bypass this pin to GND with at least 1 µF of low ESR or ESL capacitance.

**VOUT:** Regulated negative-output voltage. A single 4.7-µF capacitor should be connected between this pin and GND. Smaller value capacitors can be used for light loads, but this degrades the load-step performance of the regulator.

**VOUTS:** This is the feedback pin for sensing the output of the regulator. For the UCC384-5 and UCC384-12 versions, VOUTS can be connected directly to VOUT. If the load is placed at a considerable distance from the regulator, the VOUTS lead can be used as a Kelvin connection to minimize errors due to lead resistance. Connecting VOUTS at the load moves the resistance of the VOUT wire into the control loop of the regulator, thereby effectively canceling the IR drop associated with the load path.

## APPLICATION INFORMATION

### overview

The UCCx84-x family of **negative** low-dropout linear (LDO) regulators provides a regulated-output voltage for applications with up to 0.5 A of load current. The regulators feature a low-dropout voltage and short-circuit protection, making their use ideal for demanding applications requiring fault protection.

### programming the output voltage on the UCC384

The UCC384-5 and UCC384-12 have output voltages that are fixed at –5 V and –12 V respectively. Connecting VOUTS to VOUT gives the proper output voltage with respect to ground.

The UCC384-ADJ can be programmed for any output voltage between –1.25 V and –15 V. This is easily accomplished with the addition of an external resistor divider connected between GND and VOUT with VOUTS connected to the center tap of the divider. For an output of –1.25 V, no resistors are needed and VOUTS is connected directly to VOUT. The regulator-input voltage cannot be more positive than the UVLO threshold, or approximately –3 V. Thus, low dropout cannot be achieved when programming the output voltage more positive than approximately –3.3 V. A typical application circuit is shown in Figure 1.

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## APPLICATION INFORMATION

### programming the output voltage on the UCC384 (continued)

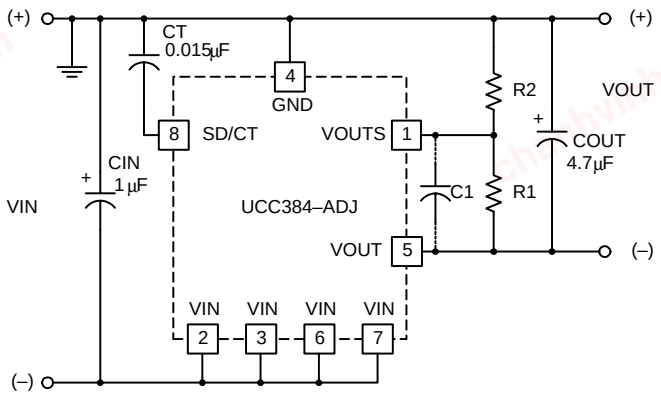


**Figure 1. Typical Application Circuit**

For the UCC384–ADJ, the output voltage is programmed by the following equation:

$$VOUT = -1.25 \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

When R1 or R2 are selected to be greater than about 100 kΩ, a small ceramic capacitor should be placed across R1 to cancel the input pole created by R1 and the parasitic capacitance appearing on VOUTS. Values of approximately 20 pF should be adequate.

### dropout performance

The UCC384 is tailored for low-dropout applications where low-quiescent power is important. Fabricated with a BCDMOS technology ideally suited for low input-to-output differential applications, the UCC384 passes 0.5 A while requiring only 0.2 V of headroom. The dropout voltage is dependent on operating conditions such as load current, input and load voltages, and temperature. The UCC384 achieves a low $R_{DS}(on)$ through the use of an internal charge-pump that drives the MOSFET gate.

Figure 2 shows typical dropout voltages versus output voltage for the UCC384-5 V and -12 V versions as well as the UCC384–ADJ version programmed between –3.3 V and –15 V. Since the dropout voltage is also affected by output current, Figure 3 shows typical dropout voltages versus load current for different values of VOUT.

Operating temperatures also affect the $R_{DS}(on)$ and the dropout voltage of the UCC384. Figure 4 shows typical dropout voltages for the UCC384 over temperature under a full load of 0.5 A.

### short-circuit protection

The UCC384 provides unique short-circuit protection circuitry that reduces power dissipation during a fault. When an overcurrent condition is detected, the device enters a pulsed mode of operation, limiting the output to a 2.5% duty cycle. This reduces the heat sink requirements during a fault. The operation of the UCC384 during an overcurrent condition is shown in Figure 5.

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## APPLICATION INFORMATION

### short-circuit protection (continued)

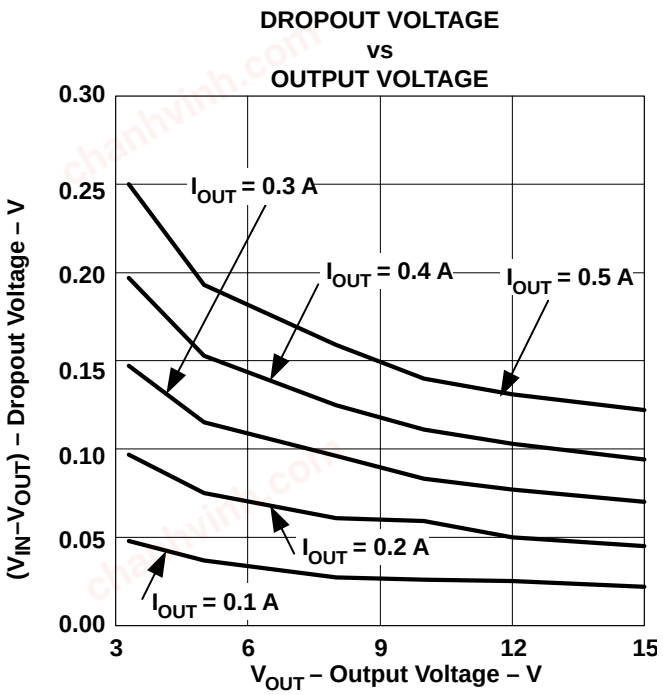


Figure 2

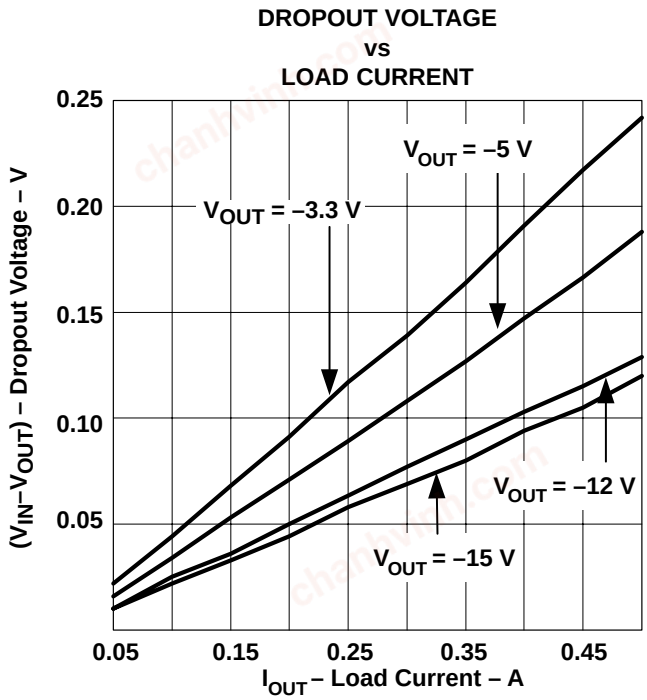


Figure 3

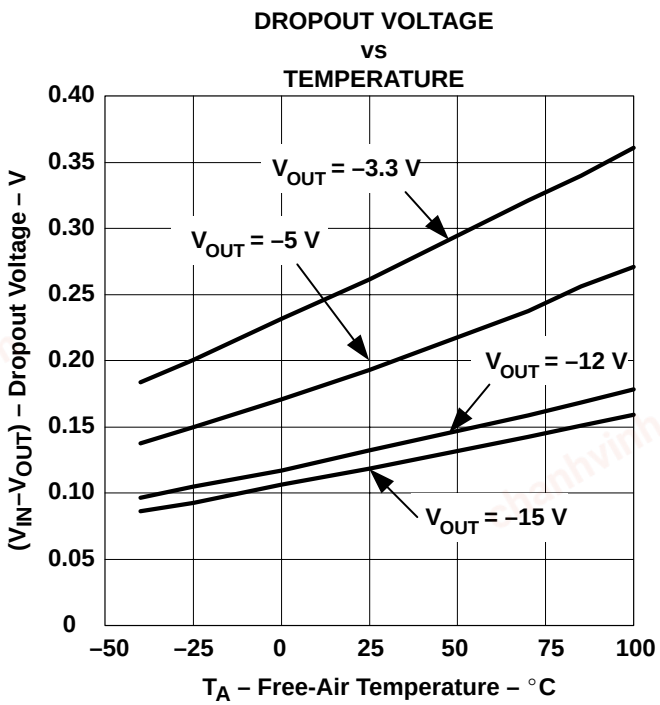


Figure 4

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## APPLICATION INFORMATION

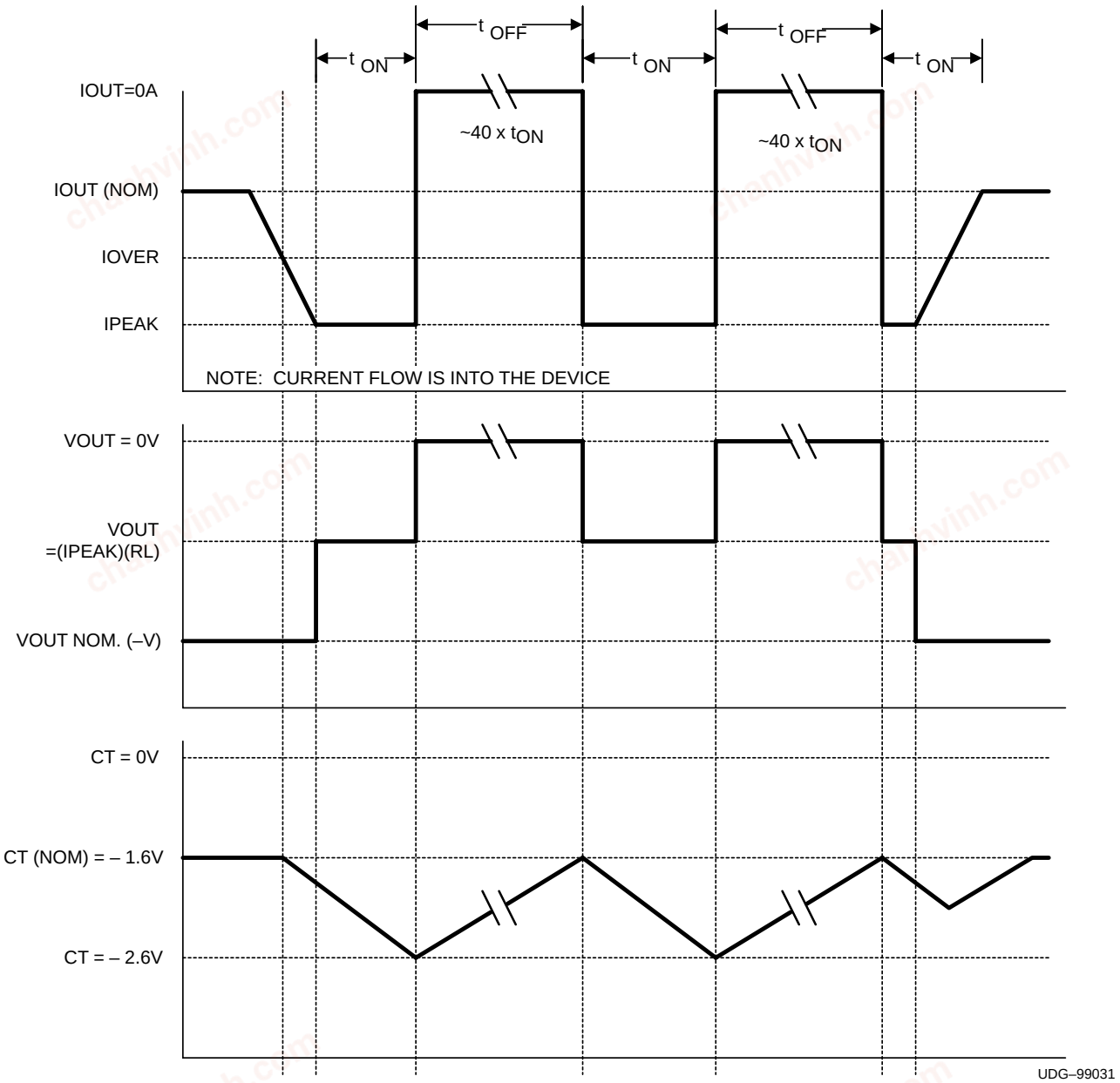


**Figure 5. Short Circuit Timing**

### UCC384 short circuit timing

During normal operation the output voltage is in regulation and the SD/CT pin is held to –1.5 V via a 50-kΩ internal-source impedance. If the output-current rises above the overcurrent threshold, the CT capacitor is charged by a 40-μA current sink. The voltage on the SD/CT pin moves in a negative direction with respect to GND.

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## APPLICATION INFORMATION

### UCC384 short-circuit timing (continued)

During an overcurrent condition, the regulator actively limits the maximum output current to the peak-current limit. This limits the output voltage of the regulator to:

$$V_{OUT} = I_{PEAK} \times R_L \quad (1)$$

If the output current stays above the overcurrent threshold, the voltage on the SD/CT pin reaches –2.6 V with respect to GND and the output turns off. The CT capacitor is then discharged by a 1-μA current source. When the voltage on the SD/CT pin reaches –1.6 V with respect to GND, the output turns back on. This process repeats until the output current falls below the overcurrent threshold.

$t_{ON}$, the time the output is on during an overcurrent condition is determined by the following equation:

$$t_{ON} = CT\ (\mu F) \times \frac{1\ V}{40\ \mu A} \text{seconds} \quad (2)$$

$t_{OFF}$, the time the output is off during an overcurrent condition is determined by the following equation:

$$t_{OFF} = CT\ (\mu F) \times \frac{1\ V}{1\ \mu A}\ \text{seconds} \quad (3)$$

### capacitive loads

A capacitive load on the regulator's output appears as a short-circuit during start-up. If the capacitance is too large, the output voltage does not begin to regulate during the initial $t_{ON}$ period and the UCC384 enters a pulsed mode operation. For a constant current load the maximum allowed output capacitance is calculated as follows:

$$C_{OUT(max)} = \left[I_{PEAK}(A) - I_{LOAD}(A)\right] \times \frac{t_{ON}(sec)}{V_{OUT}(V)}\ \text{Farads} \quad (4)$$

For worst case calculations, the minimum value for $t_{ON}$ should be used, which is based on the value of CT capacitor selected. For a resistive load the maximum output capacitor can be estimated as follows:

$$C_{OUT(max)} = \frac{t_{ON}(sec)}{R_{LOAD}\ (\Omega) \times \ell n \left( \frac{1}{1 - \left( \frac{V_{OUT}\ (V)}{I_{MAX}(A) \times R_{LOAD}(\Omega)} \right)} \right)}\ \text{Farads} \quad (5)$$

Figure 6 and Figure 7 are oscilloscope photos of the UCC384–ADJ operating during an overcurrent condition. Figure 6 shows operation of the circuit as the output current initially rises above the overcurrent threshold. This is shown on a 1ms/div. scale. Figure 7 shows operation of the same circuit on a 25 ms/div. scale showing one complete cycle of operation during an overcurrent condition.

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## APPLICATION INFORMATION

**UCC384–ADJ**
**OVERCURRENT CONDITION OPERATION**
**1 ms/div**

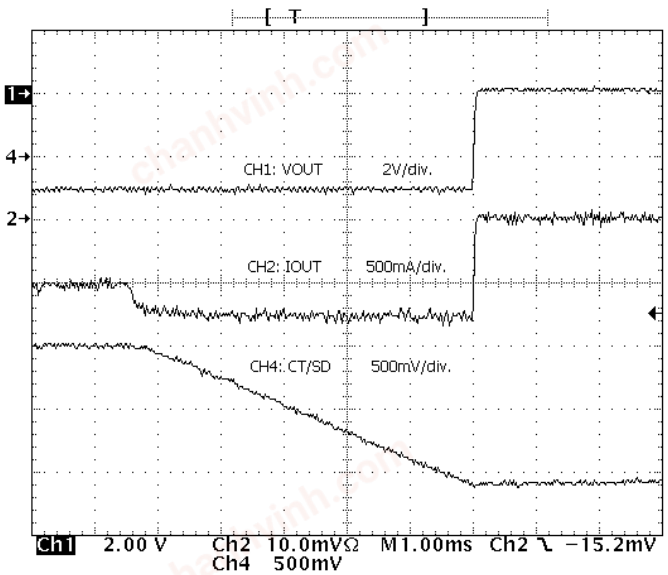


Figure 6

**UCC384–ADJ**
**OVERCURRENT CONDITION OPERATION**
**25 ms/div**

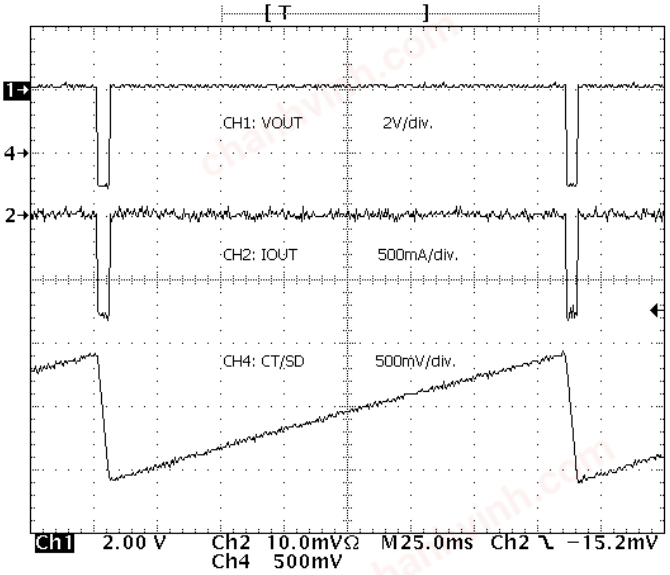


Figure 7

### shutdown feature of the UCC384

The shutdown feature of the UCC384 allows the device to be placed in a low quiescent current mode. The UCC384 is shut down by pulling the SD/CT pin more positive than –0.7 V with respect to GND. Figure 8 shows how a shutdown circuit can be configured for the UCC384 using a standard transistor-transistor logic signal to control it.

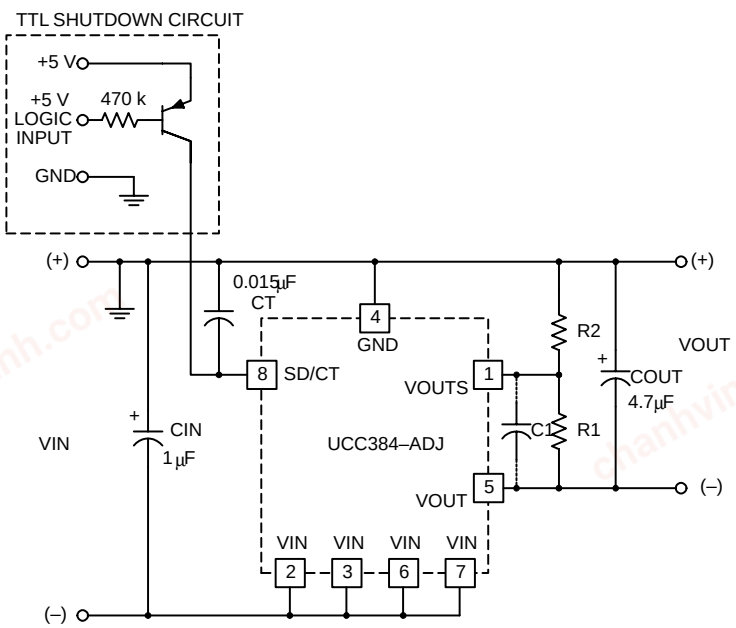


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**Figure 8. TTL Controlled Shutdown Circuit for the UCC384**

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## APPLICATION INFORMATION

### controlling the SD/CT pin

Forcing the SD/CT pin to any fixed voltage affects the operation of the circuit. As mentioned before, pulling the SD/CT pin more positive than –0.7 V puts the circuit in a shutdown mode, limiting the quiescent current to less than 45 μA. Pulling this pin more positive than 6 V with respect to GND damages the device.

Forcing the SD/CT pin to any fixed voltage between –0.7 V and –1.6 V with respect to GND enables the output. However, in an overcurrent condition, the output does not pulse at a 2.5% duty cycle, but the output current is still limited to the peak current limit. This circuit may be used where a fixed current limit is needed, where a 2.5% duty cycle is undesirable. The UCC384 supplies a maximum current in this configuration as long as the temperature of the device does not exceed the overtemperature shutdown. This is determined by the peak current being supplied, the input and output voltages, and the type of heat sink being used. *Thermal design* is discussed later on in this data sheet.

Forcing the SD/CT pin to a voltage level between approximately –1.6 V and –2.6 V with respect to GND is not recommended as the output may or may not be enabled.

Forcing the SD/CT pin to a voltage level between approximately –2.6 V and –5 V with respect to GND turns the output off completely. The output remains off as long as the voltage is applied. Pulling this pin more negative than –5 V with respect to GND damages the device (see Table 1).

**Table 1 SD/CT Voltage Levels**

| SD/CT | STATE |
|---|---|
| 6 V to –0.7 V | Output disabled and device in low quiescent shutdown mode. |
| –0.7 V to –1.6 V | Output enabled |
| –1.6 V to –2.6 V | Output enabled or disabled depending on the previous state. |
| –2.6 V to –5 V | Output disabled |

**VIN TO VOUT DELAY TIME
DURING POWER-UP WITH CT = 0.22 μF**

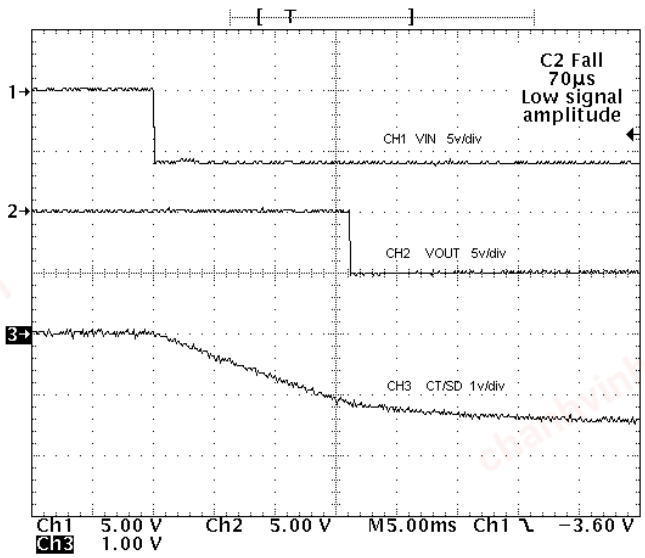


**Figure 9**

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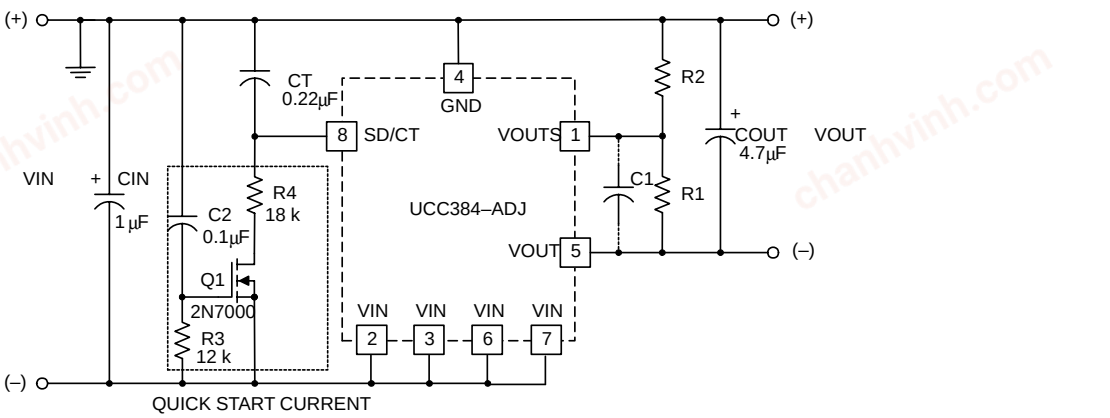
## APPLICATION INFORMATION

### VIN to VOUT Delay

During power-up there is a delay between VIN and VOUT. The majority of this delay time is due to the charging time of the CT capacitor. When VIN moves more negative than the UVLO of the device with respect to GND, the CT capacitor begins to charge. A 17-µA current sink is used only during power up to charge the CT capacitor. When the voltage on the SD/CT pin reaches approximately –1.6 V with respect to GND, the output turns on and regulates. The larger the value of the CT capacitor, the greater the delay time between VIN and VOUT. Figure 9 shows the VIN to VOUT start-up delay, approximately 16 ms for a circuit with CT = 0.22 µF.

Shorter delay times can be achieved with a smaller CT capacitor. The problem with a smaller CT capacitor is that with a very large load, the circuit may stay in overcurrent mode and never turn on. A circuit with a large capacitive load needs a large CT capacitor to operate properly.

One way to shorten the delay from VIN to VOUT during powerup, is with the use of the quick start-up circuit shown in Figure 10.




UDG–99033

**Figure 10. Quick Start-Up Circuit for UCC384**

With the quick start-up circuit, the delay time between VIN and VOUT during start-up can be reduced dramatically. Figure 11 shows that with the quick start-up circuit, the VIN to VOUT delay time has been reduced to approximately 1 ms.

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## APPLICATION INFORMATION

### VIN to VOUT Delay

**VIN TO VOUT DELAY TIME
WITH QUICK START-UP CIRCUIT**

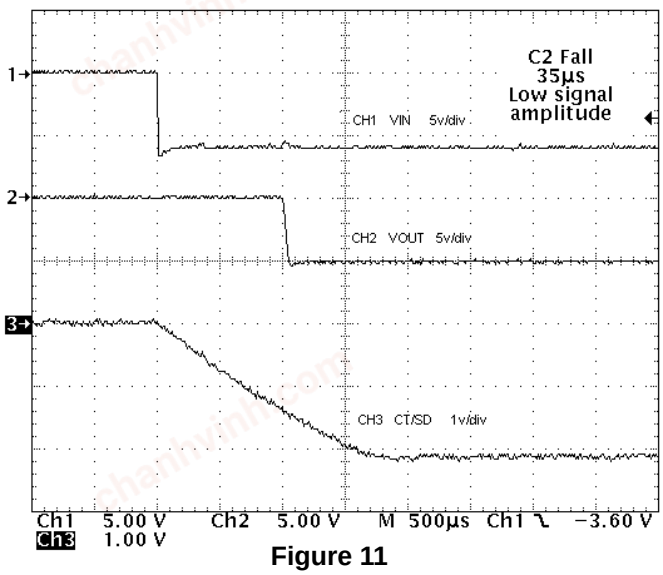


**Figure 11**

**VIN TO VOUT DELAY TIME
WITH CT CAPACITOR REMOVED**

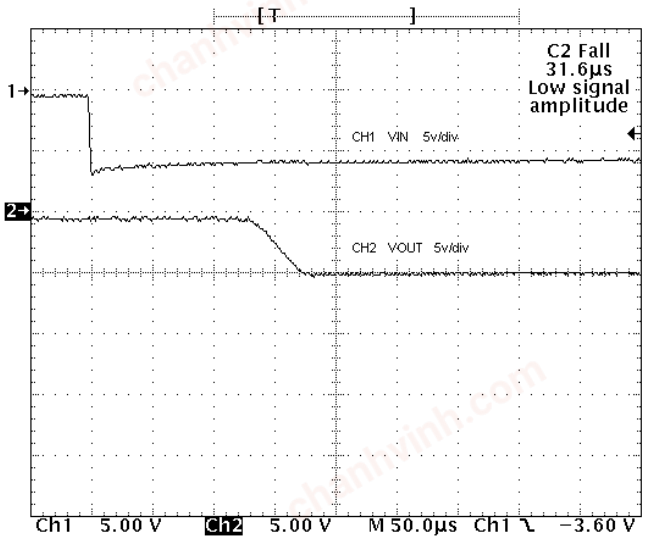


**Figure 12**

### operation of the quick start-up circuit

During normal start-up, the UCC384 does not turn on until the voltage on the SD/CT pin reaches approximately –1.6 V with respect to ground. It takes a certain amount of time for the CT capacitor to charge to this point. For a circuit that has a very large load, the CT capacitor needs to be large in order for the overcurrent timing to work properly. A large value of capacitance on the SD/CT pin increases the VIN to VOUT delay time.

The quick start-up circuit uses Q1 to quickly pull the SD/CT pin in a negative direction during start-up, thus decreasing the VIN-to-VOUT delay time. When VIN is applied to the circuit, Q1 turns on and starts to charge the CT capacitor. The current pulled through R4 determines the rate at which CT is charged. R4 can be calculated as follows:

$$R4 = \frac{V_{IN}(V) \times T_D \text{ seconds}}{1.6 \times CT\ (F)} \text{ ohms} \quad (6)$$

$t_D$ is the approximate VIN-to-VOUT delay time desired.

Q1 needs to be turned off after a fixed time to prevent the SD/CT pin from going too far negative with respect to GND. If the SD/CT pin is allowed to go too far negative with respect to GND, the output turns off again or possibly even damages the SD/CT pin. The maximum amount of time that Q1 should be allowed to be on is referred to as $t_M$ and can be calculated as follows:

$$t_M = \frac{2.6}{1.6} \times t_D \text{ seconds} \quad (7)$$

R3 along with C2 set the time that Q1 is allowed to be on. Since $t_M$ is the maximum amount of time that Q1 should be allowed to stay on, an added safety margin may be to use $0.9 \times t_M$ instead. This ensures that Q1 is turned off in the proper amount of time. With a chosen value for C2, R3 can be calculated as follows:

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## APPLICATION INFORMATION

### operation of the quick start-up circuit (continued)

$$R3 = \frac{0.9 \times t_M \text{ seconds}}{C2(F) \times \ell n\left(1 - \frac{V_{IN}(V) - 1.6}{V_{IN}(V)}\right)} \text{ Ohms} \quad (8)$$

After the CT capacitor has charged up for a time equal to $0.9 \times t_M$ , Q1 turns off and allows the SD/CT pin to be pulled back to –1.5 V with respect to GND through a 50-kΩ resistor. At this point , the SD/CT pin can be used by the UCC384 overcurrent timing control.

### minimum $V_{IN}$ to $V_{OUT}$ delay time

Although it may desirable to have as short a delay time as possible, a small portion of this delay time is fixed by the UCC384 and cannot be shortened. This is shown in Figure 12, where the CT capacitor has been removed from the circuit completely, giving a fixed VIN to VOUT delay of approximately 150 μs for a circuit with VIN = –6 V and VOUT = –5 V.

### thermal design

The *Packaging Information* section of the *Power Supply Control Products Data Book* (TI Literature No. SLUD003) contains reference material for the thermal ratings of various packages. The section also includes an excellent article entitled *Thermal Characteristics of Surface Mount Packages*, which is the basis for the following discussion.

Thermal design for the UCC384 includes two modes of operation, normal and pulsed. In normal mode, the linear regulator and heat sink must dissipate power equal to the maximum forward voltage drop multiplied by the maximum load current. Assuming a constant current load, the expected heat rise at the regulator's junction can be calculated as follows:

$$t_{RISE} = P_{DISS} \times (\theta jc + \theta ca) \quad (9)$$

Theta (θ) is the thermal resistance and $P_{DISS}$ is the power dissipated. The junction-to-case thermal resistance (θjc) of the SOIC–8 DP package is 22°C/W. In order to prevent the regulator from going into thermal shutdown, the case-to-ambient thermal resistance (θca) must keep the junction temperature below 150°C. If the UCC384 is mounted on a 5 square inch pad of 1-ounce copper, for example, the thermal resistance (θja) becomes 40–70°C/W. If a lower thermal resistance is required for the application, the device heat sinking needs to be improved.

When the UCC384 is in a pulsed mode, due to an overcurrent condition, the maximum average power dissipation is calculated as follows:

$$P_{avg} = \left[V_{IN}(V) - V_{OUT}(V)\right] \times I_{PEAK}(A) \times \left(\frac{t_{ON}(\text{seconds})}{40 \times t_{ON}(\text{seconds})}\right) \text{ Watts} \quad (10)$$

As seen in equation (10), the average power during a fault is reduced dramatically by the duty cycle, allowing the heat sink to be sized for normal operation. Although the peak power in the regulator during the $t_{ON}$ period can be significant, the thermal mass of the package normally keeps the junction temperature from rising unless the $t_{ON}$ period is increased to several milliseconds.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UCC284DP-12 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-12, UCC284) DP-12 |
| UCC284DP-12.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-12, UCC284) DP-12 |
| UCC284DP-5 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | - | (284-5, UCC284) DP-5 |
| UCC284DP-5.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-5, UCC284) DP-5 |
| UCC284DP-5G4 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-5, UCC284) DP-5 |
| UCC284DP-ADJ | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | - | (284-ADJ, UCC284D) P-ADJ |
| UCC284DP-ADJ.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-ADJ, UCC284D) P-ADJ |
| UCC284DP-ADJG4 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-ADJ, UCC284D) P-ADJ |
| UCC284DPTR-5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-5, UCC284) DP-5 |
| UCC284DPTR-5.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-5, UCC284) DP-5 |
| UCC284DPTR-ADJ | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | - | (284-ADJ, UCC284D) P-ADJ |
| UCC284DPTR-ADJ.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-ADJ, UCC284D) P-ADJ |
| UCC284DPTR-ADJG4 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | (284-ADJ, UCC284D) P-ADJ |
| UCC384DP-12 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | - | (384-12, UCC384) DP-12 |

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| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UCC384DP-12.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | (384-12, UCC384) DP-12 |
| UCC384DP-5 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | - | (384-5, UCC384) DP-5 |
| UCC384DP-5.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | (384-5, UCC384) DP-5 |
| UCC384DP-ADJ | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | - | (384-ADJ, UCC384D) P-ADJ |
| UCC384DP-ADJ.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | (384-ADJ, UCC384D) P-ADJ |
| UCC384DP-ADJG4 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | (384-ADJ, UCC384D) P-ADJ |
| UCC384DPTR-12 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | (384-12, UCC384) DP-12 |
| UCC384DPTR-12.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | (384-12, UCC384) DP-12 |
| UCC384DPTR-5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | - | (384-5, UCC384) DP-5 |
| UCC384DPTR-5.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | (384-5, UCC384) DP-5 |
| UCC384DPTR-ADJ | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | - | (384-ADJ, UCC384D) P-ADJ |
| UCC384DPTR-ADJ.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | (384-ADJ, UCC384D) P-ADJ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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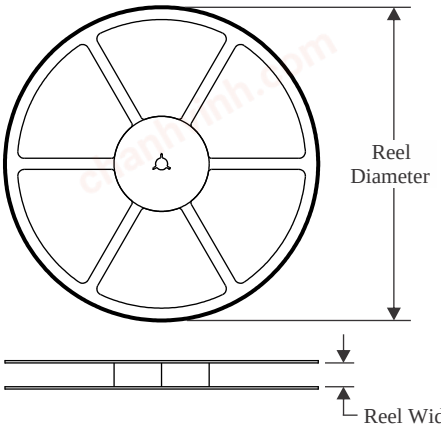
# PACKAGE MATERIALS INFORMATION

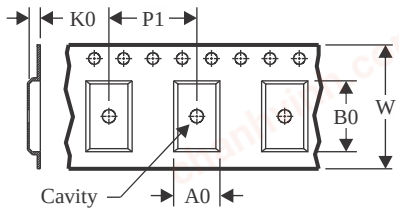


## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

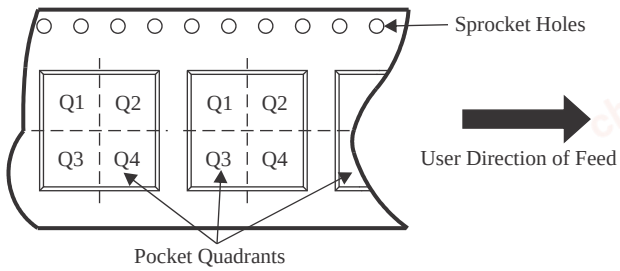



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC284DPTR-5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| UCC284DPTR-ADJ | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| UCC384DPTR-12 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| UCC384DPTR-5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| UCC384DPTR-ADJ | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

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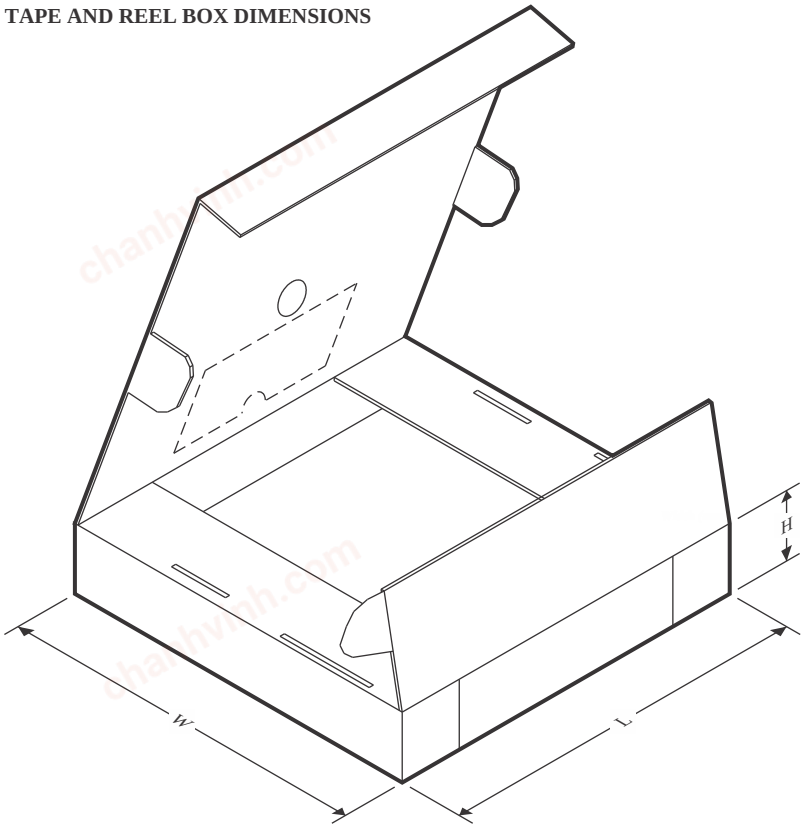
# PACKAGE MATERIALS INFORMATION



TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCC284DPTR-5 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| UCC284DPTR-ADJ | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| UCC384DPTR-12 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| UCC384DPTR-5 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| UCC384DPTR-ADJ | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

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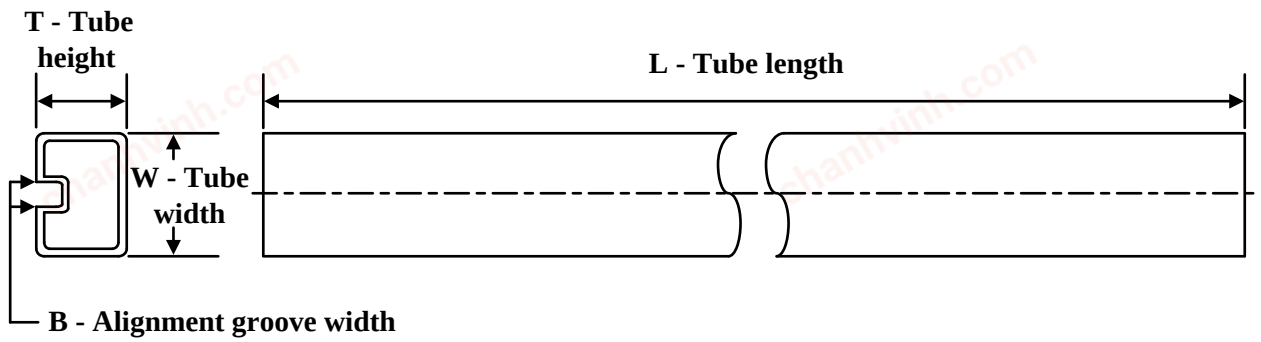
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| UCC284DP-12 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC284DP-12.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC284DP-5 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC284DP-5.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC284DP-5G4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC284DP-ADJ | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC284DP-ADJ.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC284DP-ADJG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC384DP-12 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC384DP-12.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC384DP-5 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC384DP-5.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC384DP-ADJ | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC384DP-ADJ.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC384DP-ADJG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |

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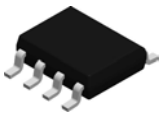
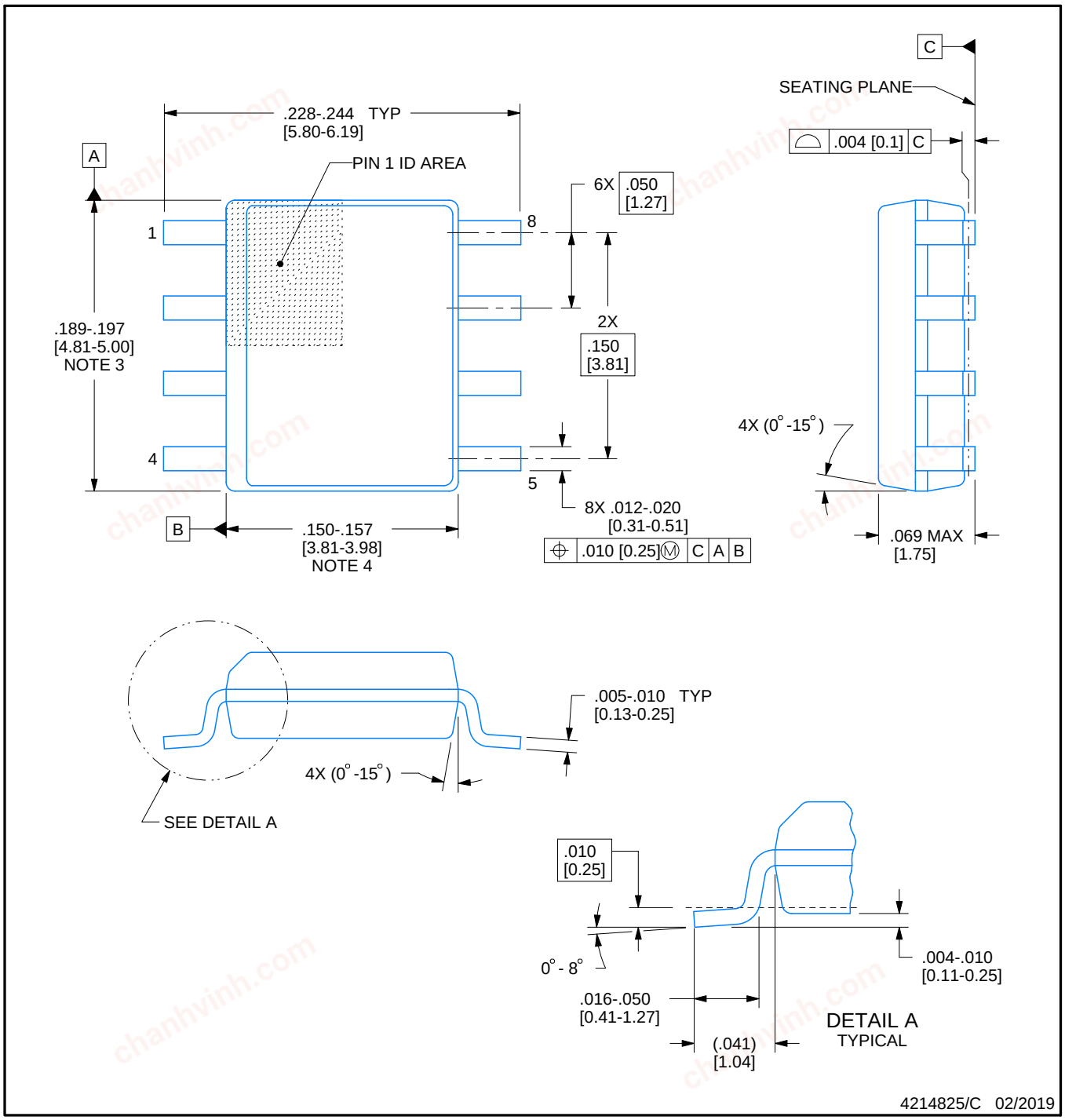


# PACKAGE OUTLINE

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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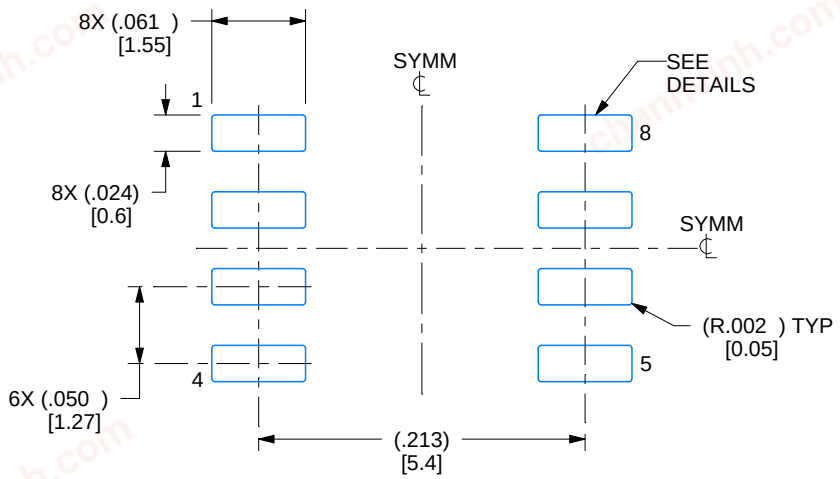
# EXAMPLE BOARD LAYOUT

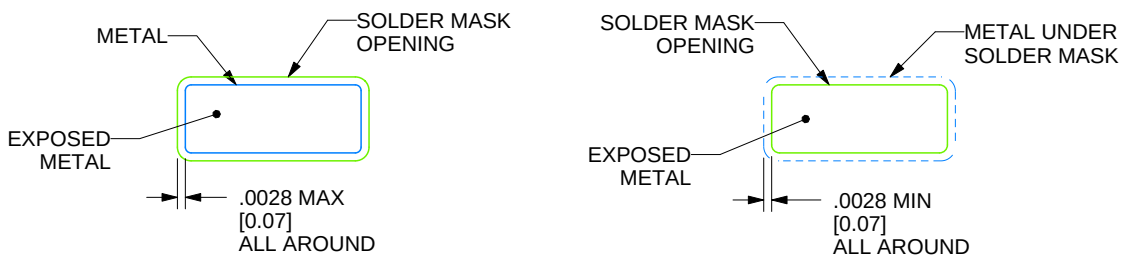
## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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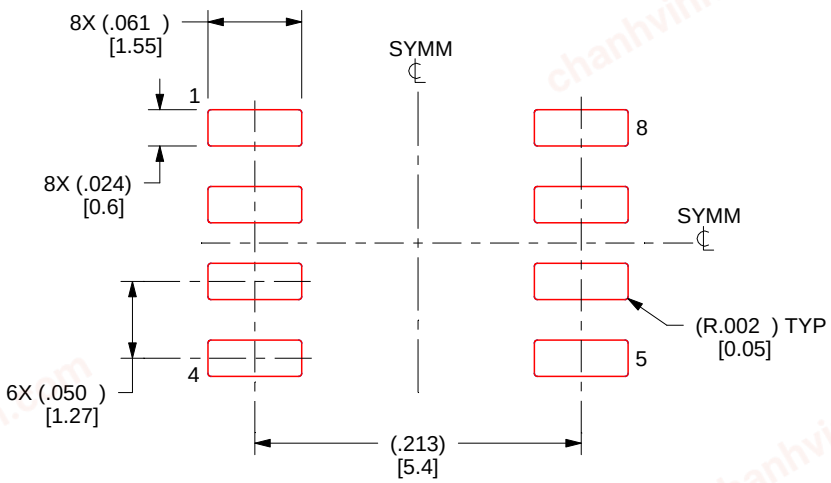
# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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