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250mA, Low Quiescent Current, Ultra-Low Noise, High PSRR Low-Dropout Linear Regulator

FEATURES

- **250mA Low Dropout Regulator with EN**
- **Low I_Q: 44μA**
- **Multiple Output Voltage Versions Available:**
  - **Fixed Outputs of 1.0V to 4.3V Using Innovative Factory EEPROM Programming**
  - **Adjustable Outputs from 1.25V to 6.2V**
- **High PSRR: 60dB at 1kHz**
- **Ultra-low Noise: 28μV_{RMS}**
- **Fast Start-Up Time: 45μs**
- **Stable with a Low-ESR, 2.0μF Typical Output Capacitance**
- **Excellent Load/Line Transient Response**
- **2% Overall Accuracy (Load/Line/Temp)**
- **Very Low Dropout: 125mV at 250mA**
- **ThinSOT-23, 2mm × 2mm SON-6, and 3mm x 3mm SON-8 Packages**

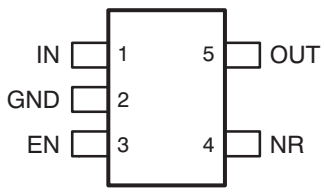
APPLICATIONS

- **WiFi, WiMax**
- **Printers**
- **Cellular Phones, SmartPhones**
- **Handheld Organizers, PDAs**

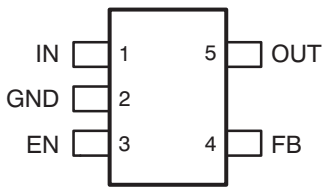
DESCRIPTION

The TPS734xx family of low-dropout (LDO), low-power linear regulators offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 44μA (typical) ground current. The TPS734xx is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a typical dropout voltage of 125mV at 250mA output. The TPS734xx uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from T_J = –40°C to +125°C and is offered in low-profile ThinSOT-23, 2mm × 2mm SON, and 3mm x 3mm SON packages that are ideal for wireless handsets, printers, and WLAN cards.

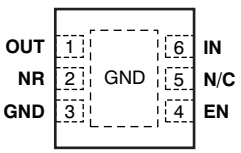
TPS734xxDDC
TSOT23-5
(TOP VIEW)



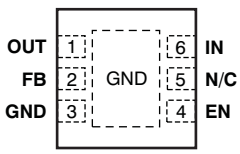
TPS73401DDC
TSOT23-5
(TOP VIEW)



TPS734xxDRV
2mm x 2mm SON-6
(TOP VIEW)



TPS73401DRV
2mm x 2mm SON-6
(TOP VIEW)



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS734**xxyyyz**	**XX** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 1.0V to 3.6V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

PARAMETER	TPS734xx	UNIT
V_{IN} range	–0.3 to +7.0	V
V_{EN} range	–0.3 to V_{IN} +0.3	V
V_{OUT} range	–0.3 to V_{IN} +0.3	V
V_{FB} range	–0.3 to V_{FB} (TYP) +0.3	V
Peak output current	Internally limited	
Continuous total power dissipation	See Dissipation Ratings Table	
Junction temperature range, T_J	–55 to +150	°C
Storage junction temperature range, T_{STG}	–55 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
Low-K(1)	DDC	90°C/W	280°C/W	3.6mW/°C	360mW	200mW	145mW
High-K(2)	DDC	90°C/W	200°C/W	5.0mW/°C	500mW	275mW	200mW
Low-K(1)	DRV	20°C/W	140°C/W	7.1mW/°C	715mW	395mW	285mW
High-K(2)	DRV	20°C/W	65°C/W	15.4mW/°C	1.54W	845mW	615mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3in × 3in (7,62cm × 7,62cm), two-layer board with 2-ounce (56,699g) copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in (7,62cm × 7,62cm), multilayer board with 1-ounce (28,35g) internal power and ground planes and 2-ounce (56,699g) copper traces on top and bottom of the board

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ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, C_{NR} = 0.01µF, unless otherwise noted. For TPS73401, V_{OUT} = 3.0V. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.7		6.5	V
V_{FB}	Internal reference (TPS73401)			1.184	1.208	1.232	V
V_{OUT}	Output voltage range (TPS73401)			V_{FB}		6.3	V
V_{OUT}	Output accuracy	Nominal	T_J = +25°C	–1.0		+1.0	%
V_{OUT}	Output accuracy(1)	Over V_{IN}, I_{OUT}, Temp	V_{OUT} + 0.3V ≤ V_{IN} ≤ 6.5V 1mA ≤ I_{OUT} ≤ 250mA	–2.0	±1.0	+2.0	%
ΔV_{OUT}%/ ΔV_{IN}	Line regulation(1)		$V_{OUT(NOM)}$ + 0.3V ≤ V_{IN} ≤ 6.5V		0.02		%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation		500µA ≤ I_{OUT} ≤ 250mA		0.005		%/mA
V_{DO}	Dropout voltage(2) (V_{IN} = $V_{OUT(NOM)}$ – 0.1V)		I_{OUT} = 250mA		125	219	mV
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(NOM)}$	300	580	900	mA
I_{GND}	Ground pin current		500µA ≤ I_{OUT} ≤ 250mA		45	65	µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V		0.15	1.0	µA
I_{FB}	Feedback pin current (TPS73401)			–0.5		0.5	µA
PSRR	Power-supply rejection ratio V_{IN} = 3.85V, V_{OUT} = 2.85V, C_{NR} = 0.01µF, I_{OUT} = 100mA		f = 100Hz		60		dB
			f = 1kHz		56		dB
			f = 10kHz		41		dB
			f = 100kHz		28		dB
V_N	Output noise voltage BW = 10Hz to 100kHz, V_{OUT} = 2.8V		C_{NR} = 0.01µF		11 x V_{OUT}		μV_{RMS}
			C_{NR} = none		95 x V_{OUT}		μV_{RMS}
T_{STR}	Startup time, V_{OUT} = 0 ~ 90%, V_{OUT} = 2.85V, R_L = 14Ω, C_{OUT} = 2.2µF		C_{NR} = none		45		µs
			C_{NR} = 0.001µF		45		µs
			C_{NR} = 0.01µF		50		µs
			C_{NR} = 0.047µF		50		µs
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled		V_{EN} = V_{IN} = 6.5V		0.03	1.0	µA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		165		°C
			Reset, temperature decreasing		145		°C
T_J	Operating junction temperature			–40		+125	°C
UVLO	Undervoltage lock-out		V_{IN} rising	1.90	2.20	2.65	V
	Hysteresis		V_{IN} falling		70		mV

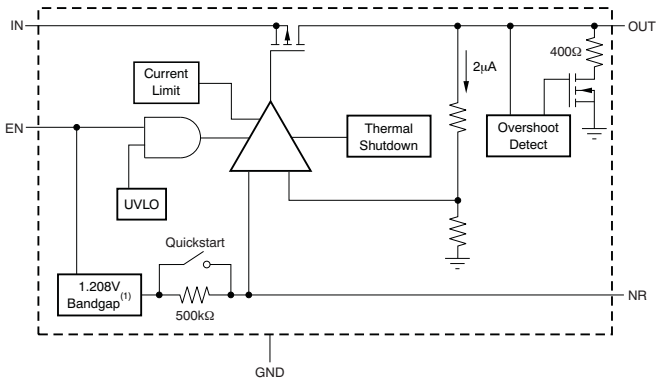
(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7V, whichever is greater.
(2) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.8V because minimum V_{IN} = 2.7V.

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DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAMS



NOTE (1): Fixed voltage versions between 1.0V to 1.2V have a 1.0V bandgap circuit instead of a 1.208V bandgap circuit.

Figure 1. Fixed Voltage Versions

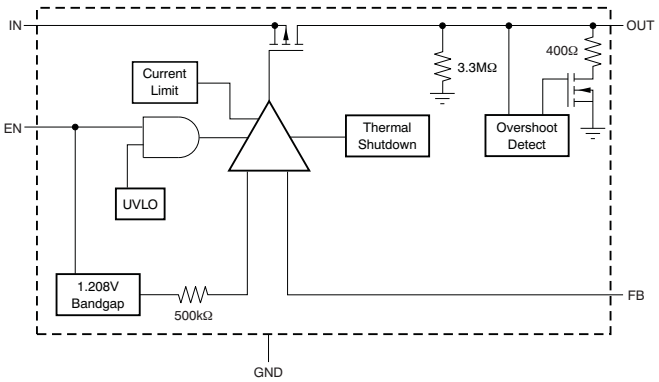
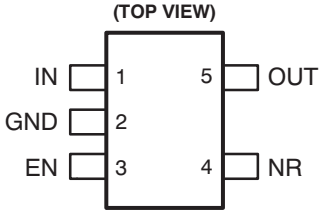


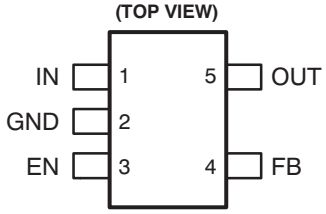
Figure 2. Adjustable Voltage Versions

PIN CONFIGURATIONS

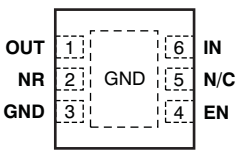
TPS734xxDDC
TSOT23-5
(TOP VIEW)



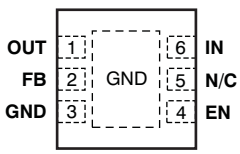
TPS73401DDC
TSOT23-5
(TOP VIEW)



TPS734xxDRV
2mm x 2mm SON-6
(TOP VIEW)



TPS73401DRV
2mm x 2mm SON-6
(TOP VIEW)



PIN DESCRIPTIONS

TPS734xx				
NAME	**DDC**	**DRV**	**DRB**	**DESCRIPTION**
IN	1	6	8	Input supply.
GND	2	3, Pad	4	Ground. The pad must be tied to GND.
EN	3	4	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	4	2	3	Fixed voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This allows output noise to be reduced to very low levels.
FB	4	2	3	Adjustable version only; this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	1	1	Output of the regulator. A small capacitor (total typical capacitance ≥ 2.0µF ceramic) is needed from this pin to ground to assure stability.
N/C	—	5	2, 6, 7	Not internally connected. This pin must either be left open, or tied to GND.

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TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C); V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT} = 1mA, V_{EN} = V_{IN},C_{OUT} = 2.2µF, C_{NR} = 0.01µF, unless otherwise noted. For TPS73401, V_{OUT} = 3.0V. Typical values are at T_J = +25°C.

TPS73401 LINE REGULATION

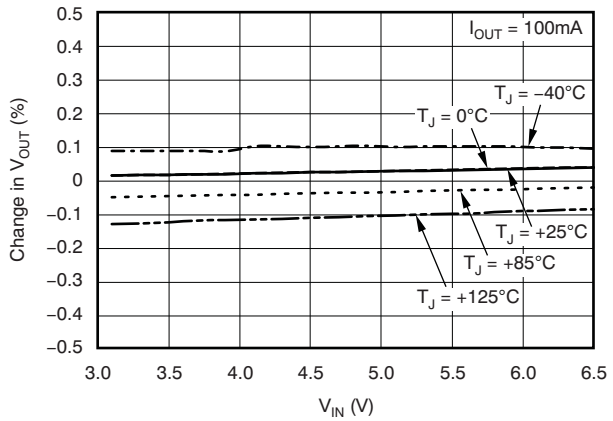


Figure 3.

TPS73425 LINE REGULATION

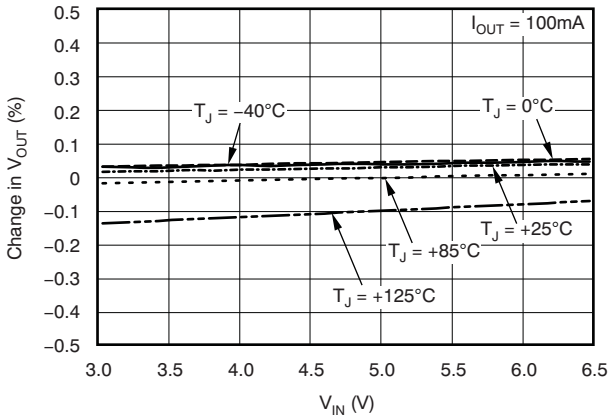


Figure 4.

TPS73401 LOAD REGULATION

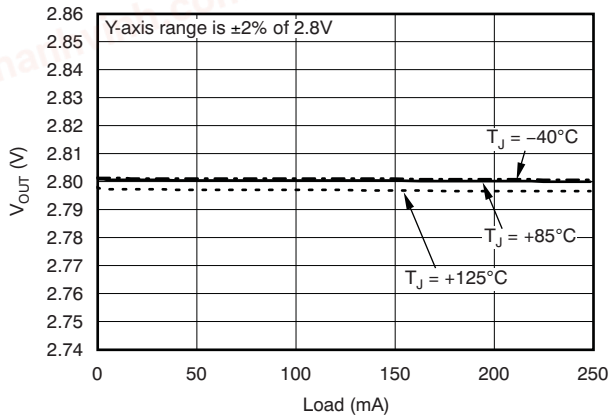


Figure 5.

TPS73425 LOAD REGULATION

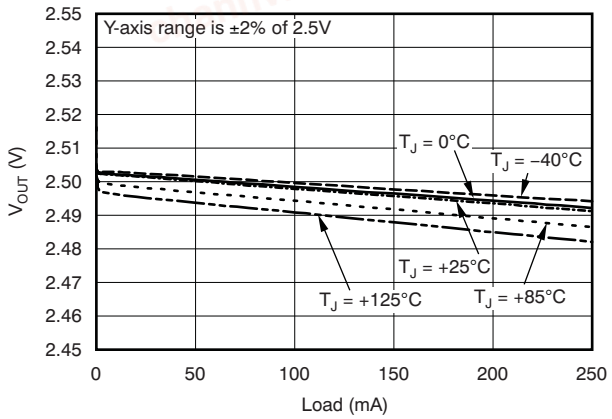


Figure 6.

TPS73425 GROUND PIN CURRENT vs OUTPUT CURRENT

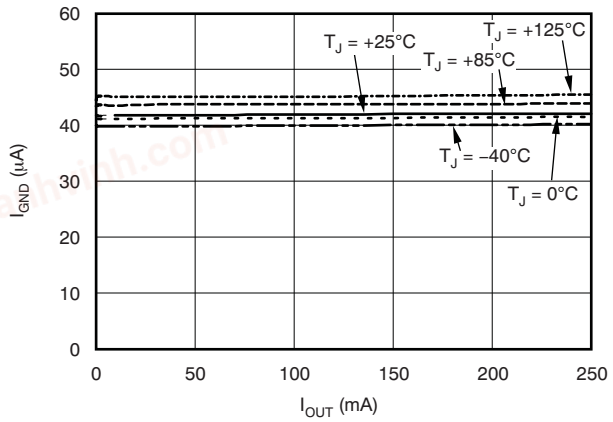


Figure 7.

TPS73425 GROUND PIN CURRENT (DISABLE) vs TEMPERATURE

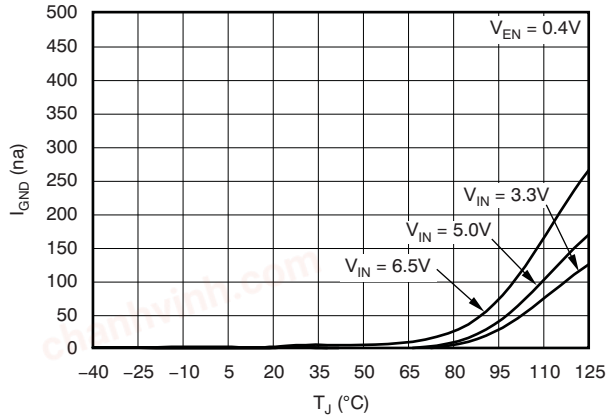


Figure 8.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C); V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, C_{NR} = 0.01µF, unless otherwise noted. For TPS73401, V_{OUT} = 3.0V. Typical values are at T_J = +25°C.

TPS73401 DROPOUT VOLTAGE vs OUTPUT CURRENT

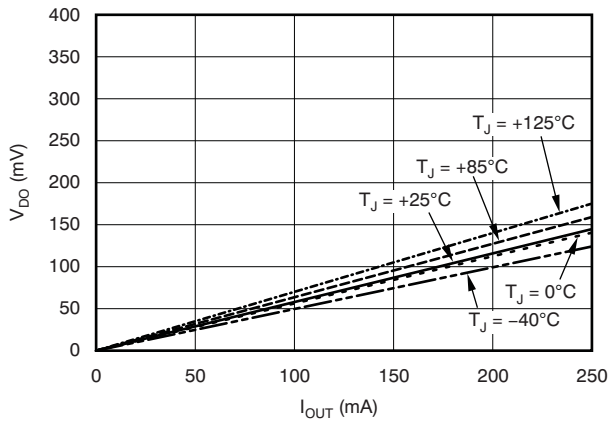


Figure 9.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1.0V)

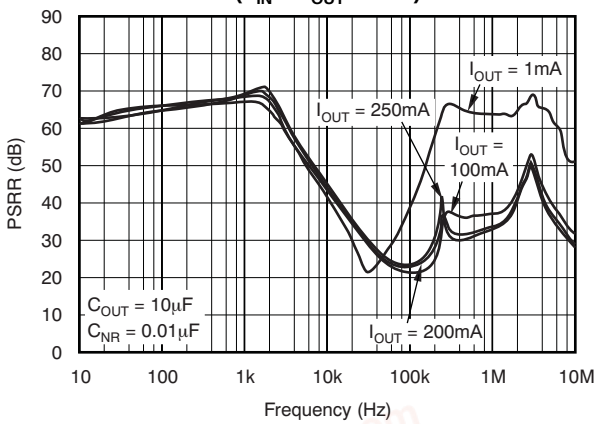


Figure 10.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.5V)

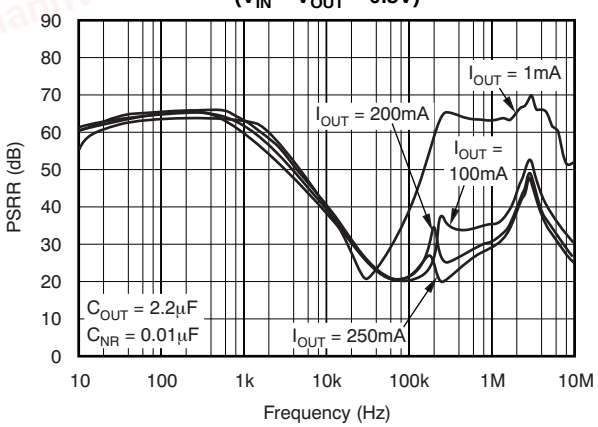


Figure 11.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.3V)

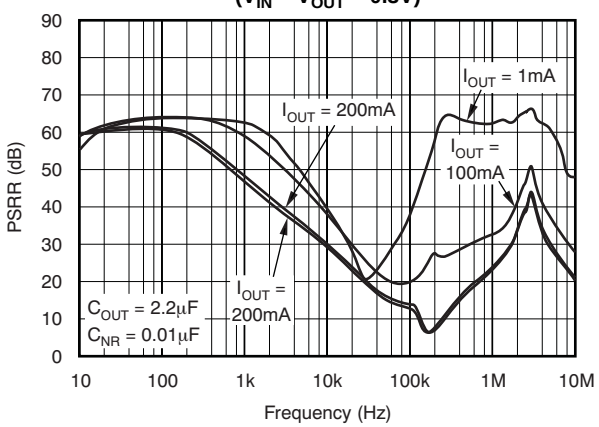


Figure 12.

TPS73425 TOTAL NOISE vs C_{NR}

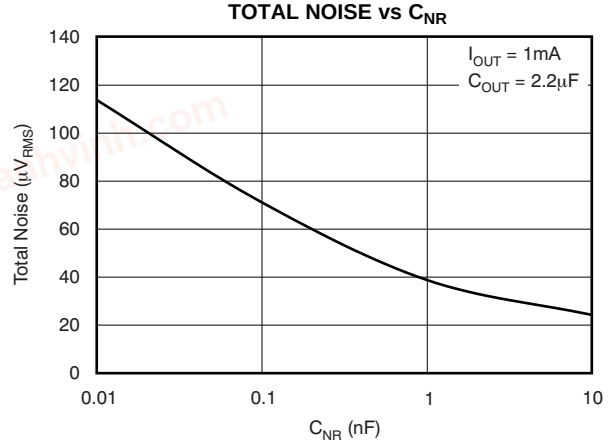


Figure 13.

TPS73425 TOTAL NOISE vs C_{OUT}

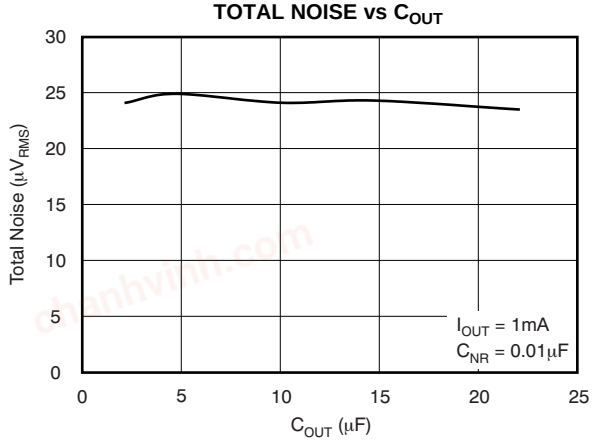


Figure 14.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C); V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2µF, C_{NR} = 0.01µF, unless otherwise noted. For TPS73401, V_{OUT} = 3.0V. Typical values are at T_J = +25°C.

TPS73425
TURN-ON RESPONSE
(V_{IN} = V_{EN})

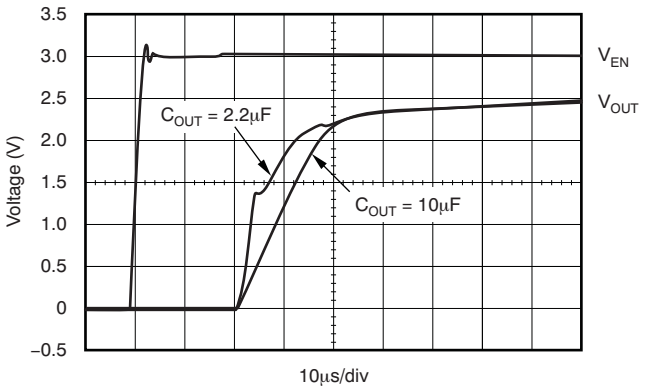


Figure 15.

TPS73425
ENABLE RESPONSE OVER STABLE V_{IN}

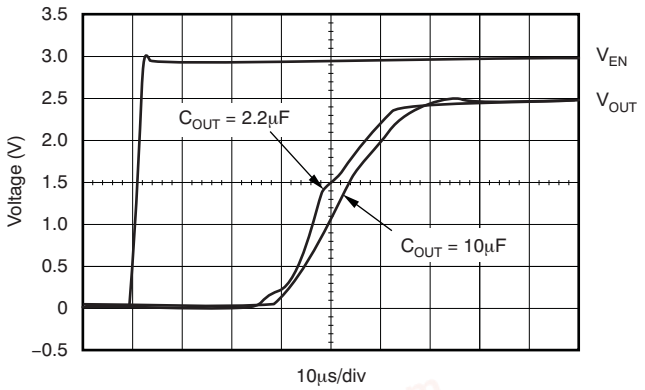


Figure 16.

TPS73410
POWER-UP/POWER-DOWN

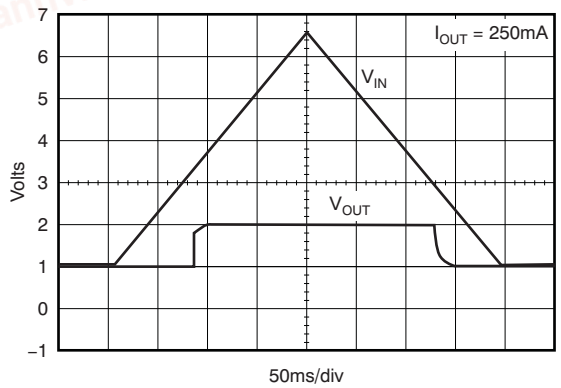


Figure 17.

TPS73410
LOAD TRANSIENT RESPONSE

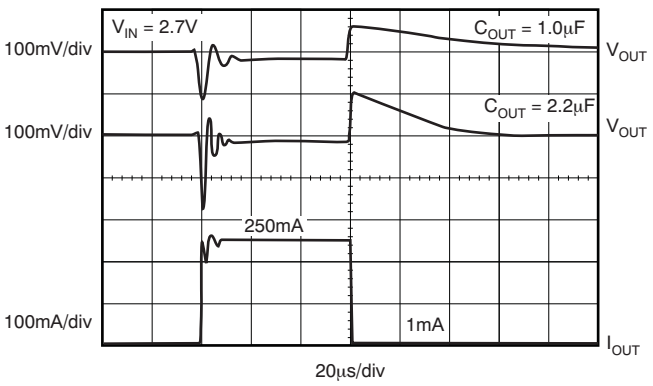


Figure 18.

TPS73410
LINE TRANSIENT RESPONSE

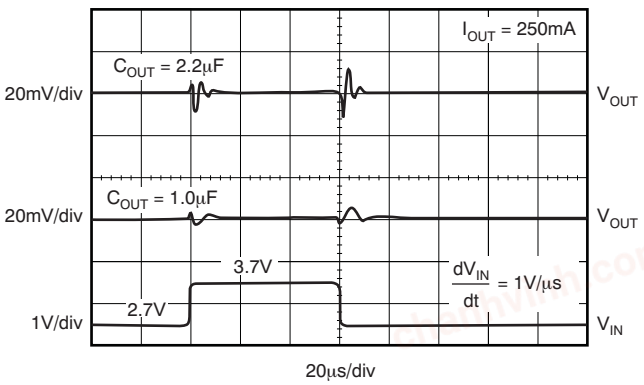


Figure 19.

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APPLICATION INFORMATION

The TPS734xx family of LDO regulators combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS734xx an excellent choice for portable applications. All versions have thermal and over-current protection and are fully specified from –40°C to +125°C.

Figure 20 shows the basic circuit connections for fixed voltage models. Figure 21 gives the connections for the adjustable output version (TPS73401). R_1 and R_2 can be calculated for any output voltage using the formula in Figure 21.

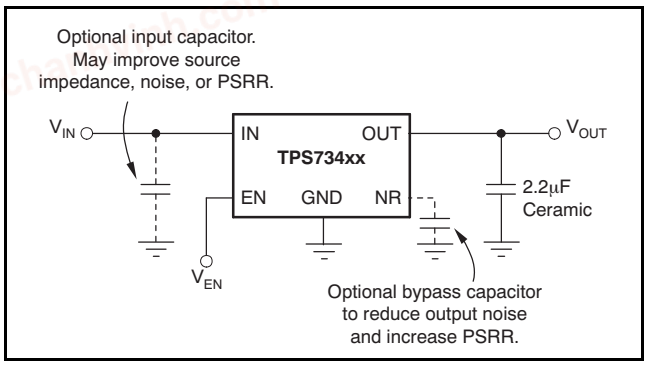


Figure 20. Typical Application Circuit for Fixed Voltage Versions

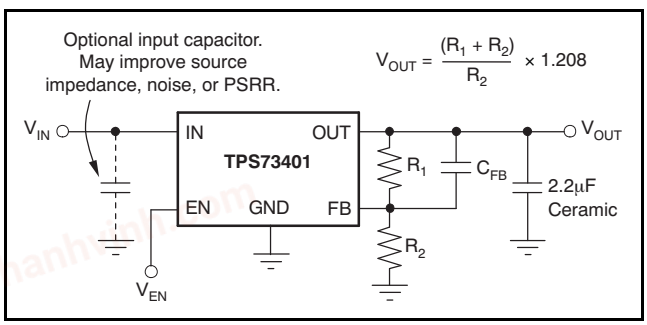


Figure 21. Typical Application Circuit for Adjustable Voltage Versions

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. The ground of this capacitor should be connected as close as the ground of output capacitor; a capacitor value of 0.1µF is enough in this condition. When it is difficult to place these two ground points close together, a 1µF capacitor is recommended. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS734xx is designed to be stable with standard ceramic output capacitors of values 2.2µF or larger. X5R and X7R type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor should be < 1.0Ω, so output capacitor type should be either ceramic or conductive polymer electrolytic.

Feedback Capacitor Requirements (TPS73401 only)

The feedback capacitor, C_{FB}, shown in Figure 21 is required for stability. For a parallel combination of R_1 and R_2 equal to 250kΩ, any value from 3pF to 1nF can be used. Fixed voltage versions have an internal 30pF feedback capacitor that is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5pF should be used to ensure fast startup; values above 47pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS73401 is stable in unity-gain configuration (OUT tied to FB) without C_{FB}.

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS734xx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01µF noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2µA of divider current has the same noise performance as a fixed voltage version. To further

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optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point (FB pin) such that with C_{NR} = 0.01µF, total noise is given approximately by Equation 1:

$$V_N = \frac{11\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

The TPS73401 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the above recommendations.

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS734xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS734xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Dropout Voltage

The TPS734xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS, ON}$ of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with output current.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in the Typical Characteristics section.

Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS734xx use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see the Functional Block Diagrams). This architecture allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, V_{IN} should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. Refer to the Typical Characteristics section. The quick-start switch is closed for approximately 135µs. To ensure that C_{NR} is fully charged during the quick-start time, a 0.01µF or smaller capacitor should be used.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. In the adjustable version, adding C_{FB} between OUT and FB improves stability and transient response. The transient response of the TPS734xx is enhanced by an active pull-down that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 400Ω resistor to ground.

Undervoltage Lock-Out (UVLO)

The TPS734xx utilizes an undervoltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 50µs duration.

Minimum Load

The TPS734xx is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of 1mA is required. Below 1mA at junction temperatures near +125°C, the output can drift up enough to cause the output pull-down to turn on. The output pull-down limits voltage drift to 5% typically but ground current could increase by approximately 50µA. In typical applications, the junction cannot reach high temperatures at light loads because there is no appreciable dissipated power. The specified ground current would then be valid at no load conditions in most applications.

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Thermal Information

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS734xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS734xx into thermal shutdown degrades device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current time the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

Package Mounting

Solder pad footprint recommendations for the TPS734xx are available from the Texas Instruments web site at www.ti.com.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73401DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCW	Samples
TPS73401DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCW	Samples
TPS73401DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CBG	Samples
TPS73401DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CBG	Samples
TPS73418DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CBI	Samples
TPS73418DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CBI	Samples
TPS73430DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVW	Samples
TPS73430DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVW	Samples
TPS73433DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OEV	Samples
TPS73433DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OEV	Samples
TPS73433DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVX	Samples
TPS73433DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CVX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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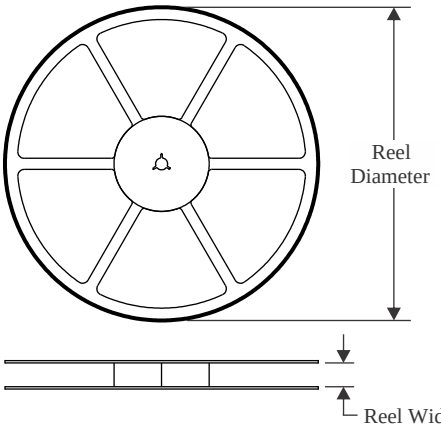
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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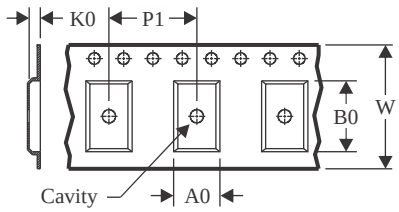
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

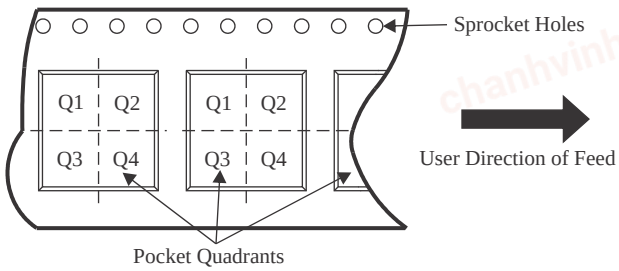


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73401DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73401DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73401DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73401DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73418DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73418DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73430DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73430DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73430DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73430DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73433DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73433DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73433DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

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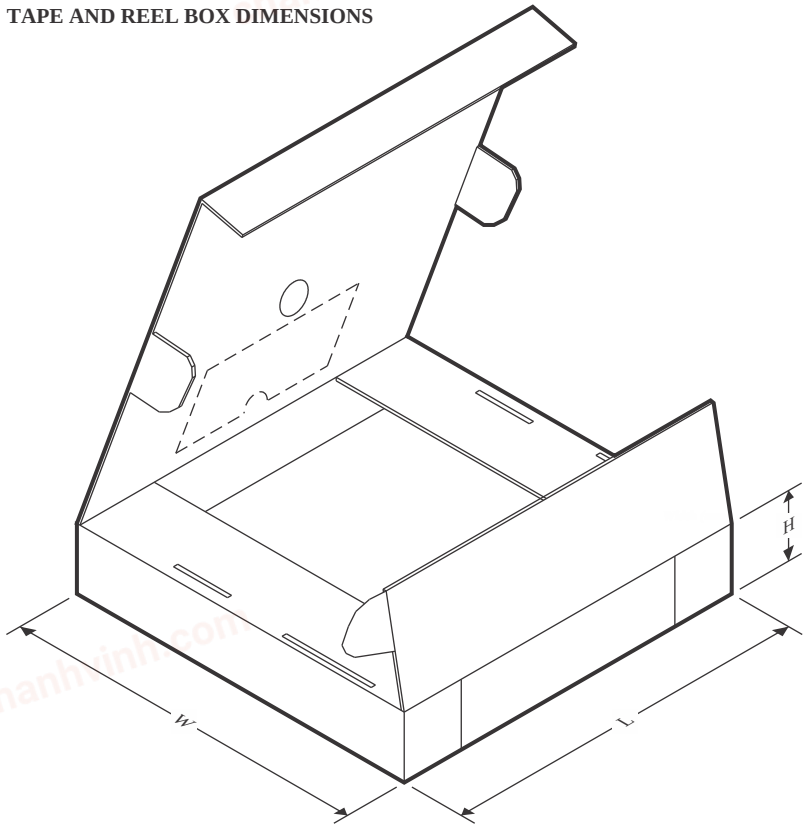
PACKAGE MATERIALS INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73433DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

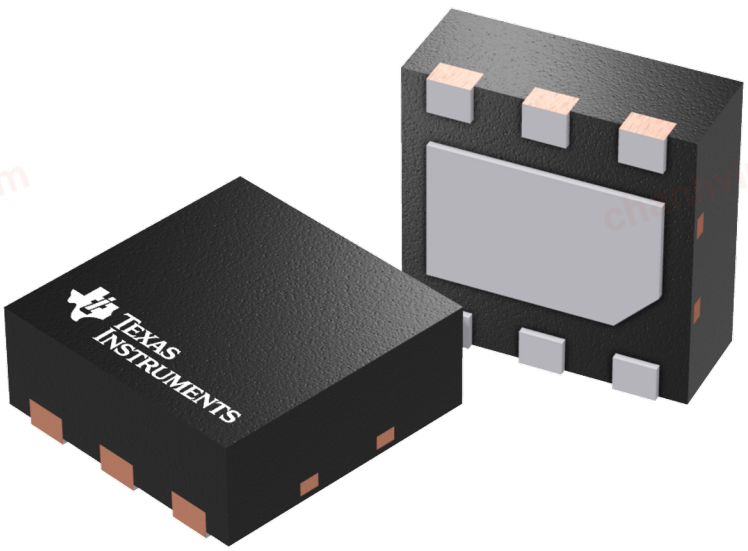
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TPS73401DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS73401DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS73401DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS73418DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS73418DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS73430DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS73430DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS73430DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS73430DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS73433DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS73433DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS73433DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS73433DRVT	WSON	DRV	6	250	200.0	183.0	25.0

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GENERIC PACKAGE VIEW

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

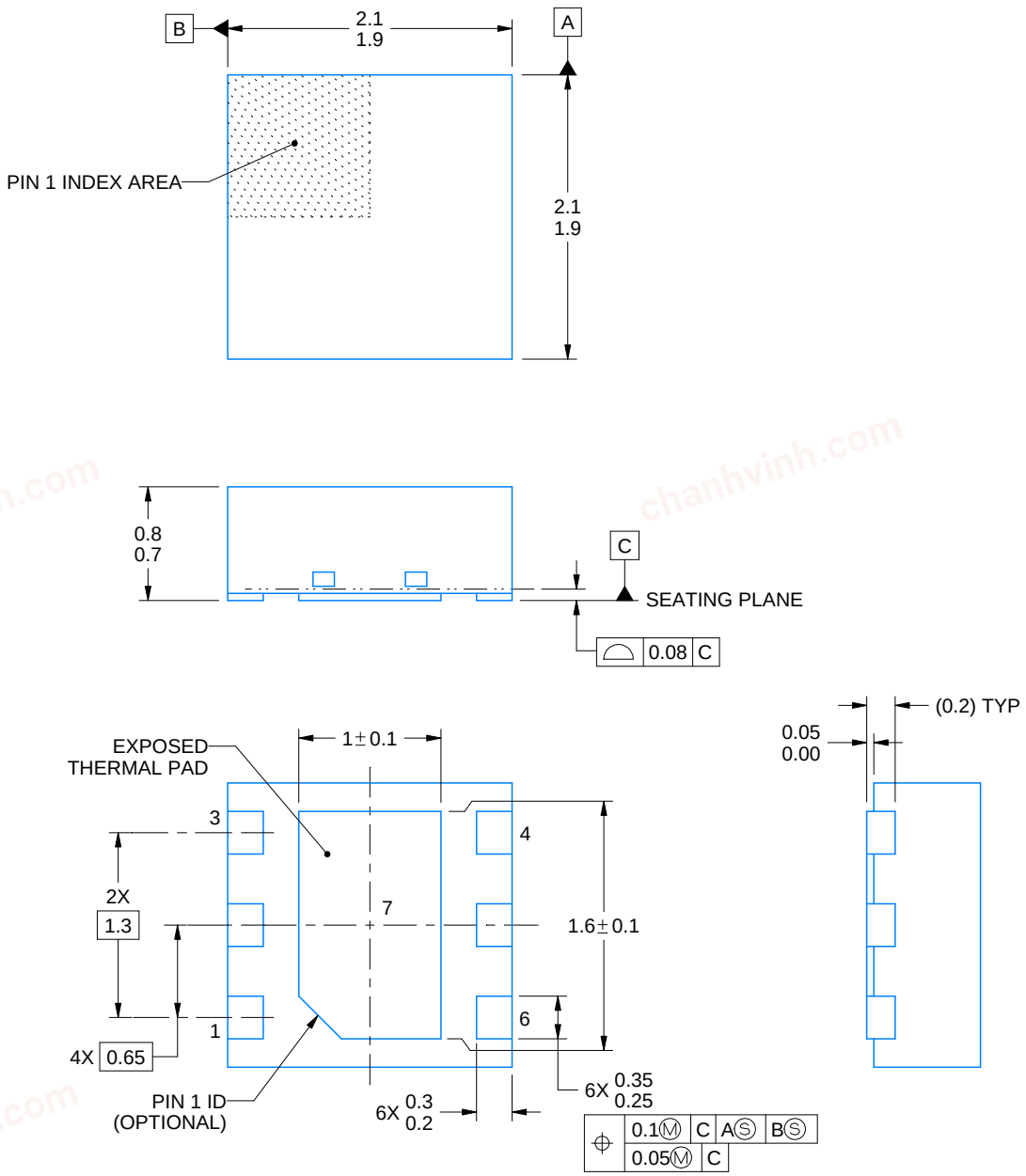
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PACKAGE OUTLINE

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

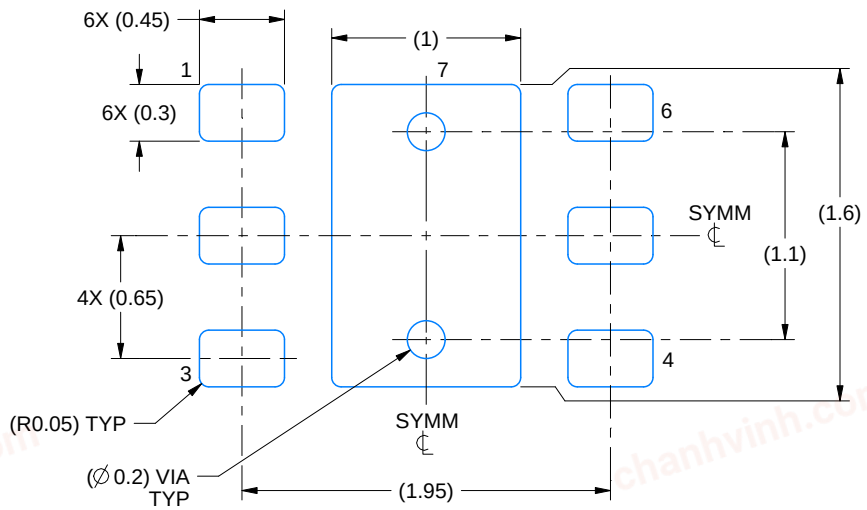
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EXAMPLE BOARD LAYOUT

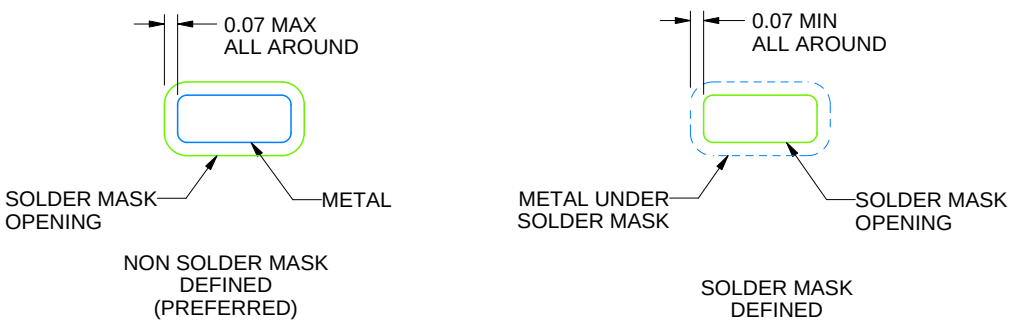
DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

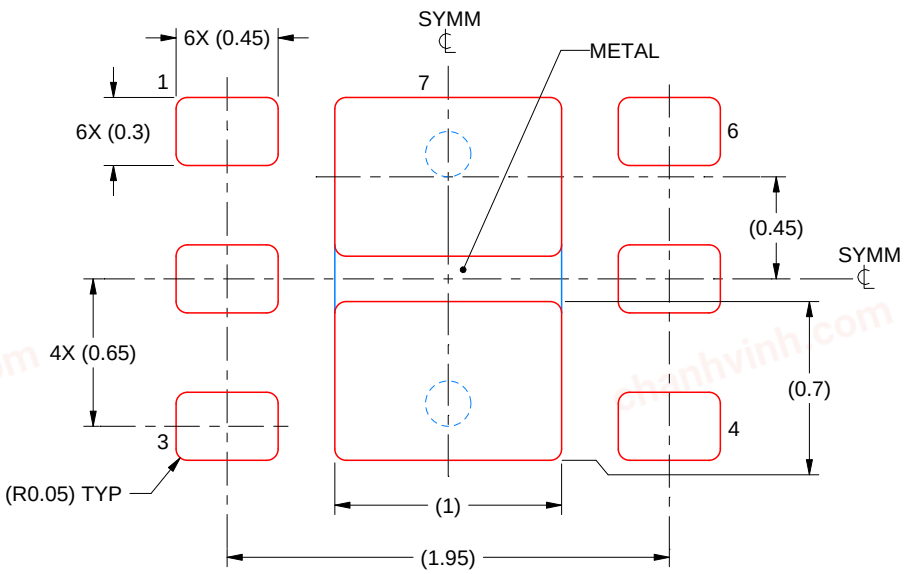
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EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

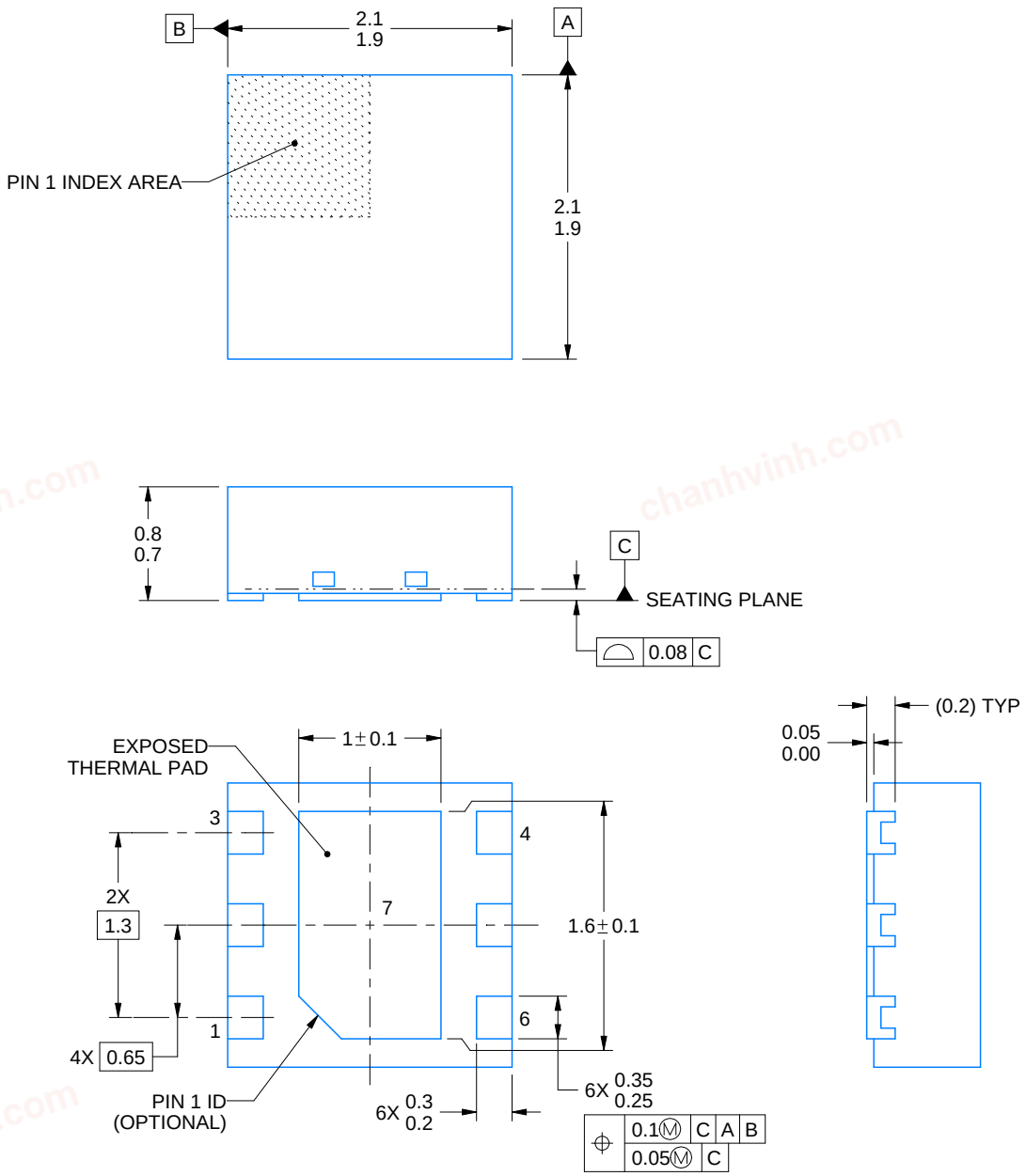
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PACKAGE OUTLINE

DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

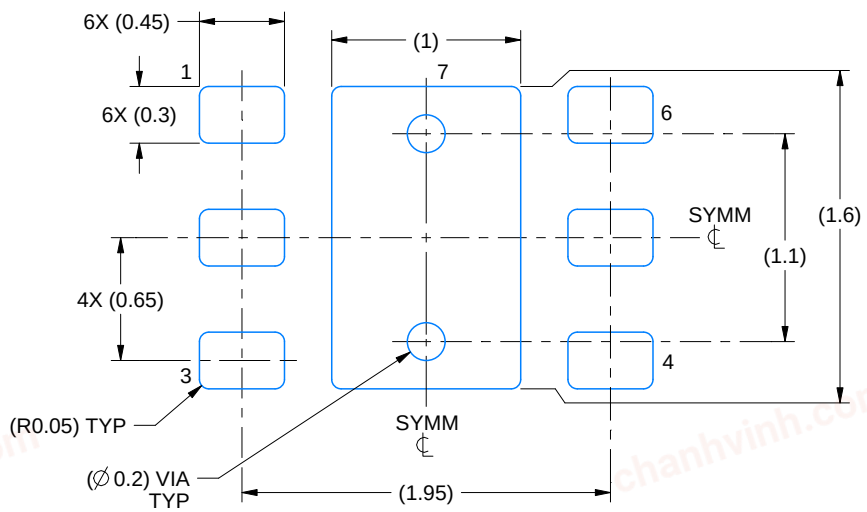
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EXAMPLE BOARD LAYOUT

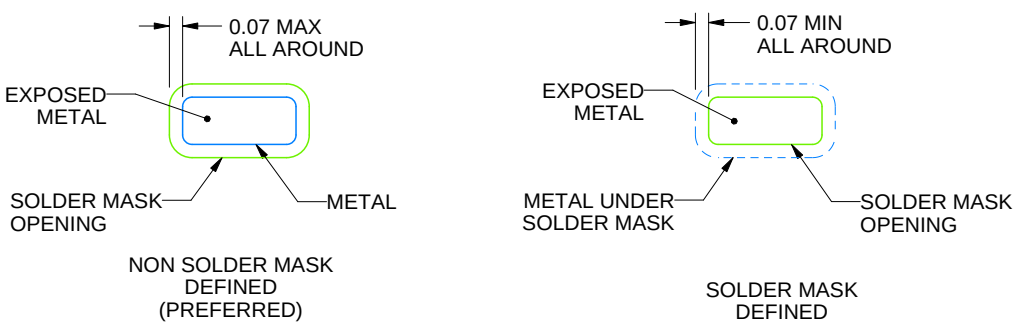
DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

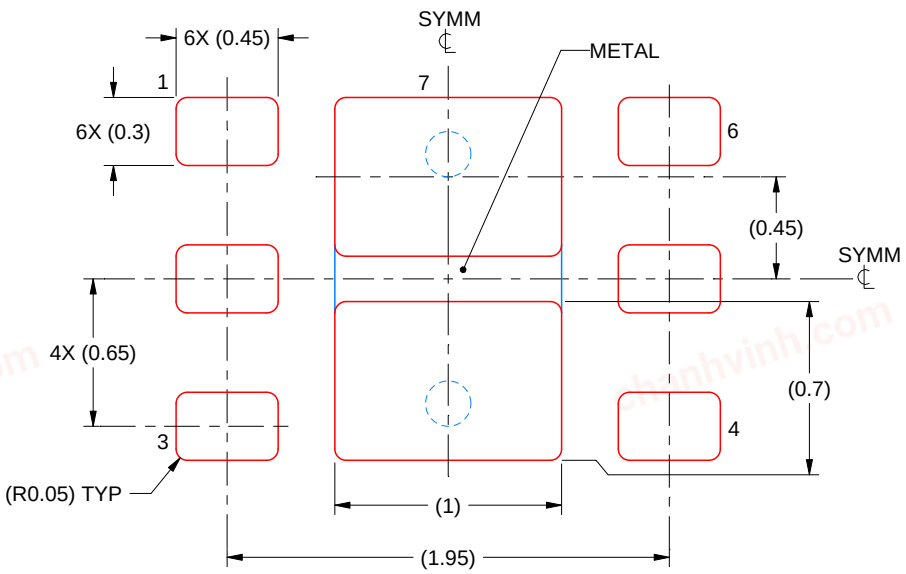
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EXAMPLE STENCIL DESIGN

DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

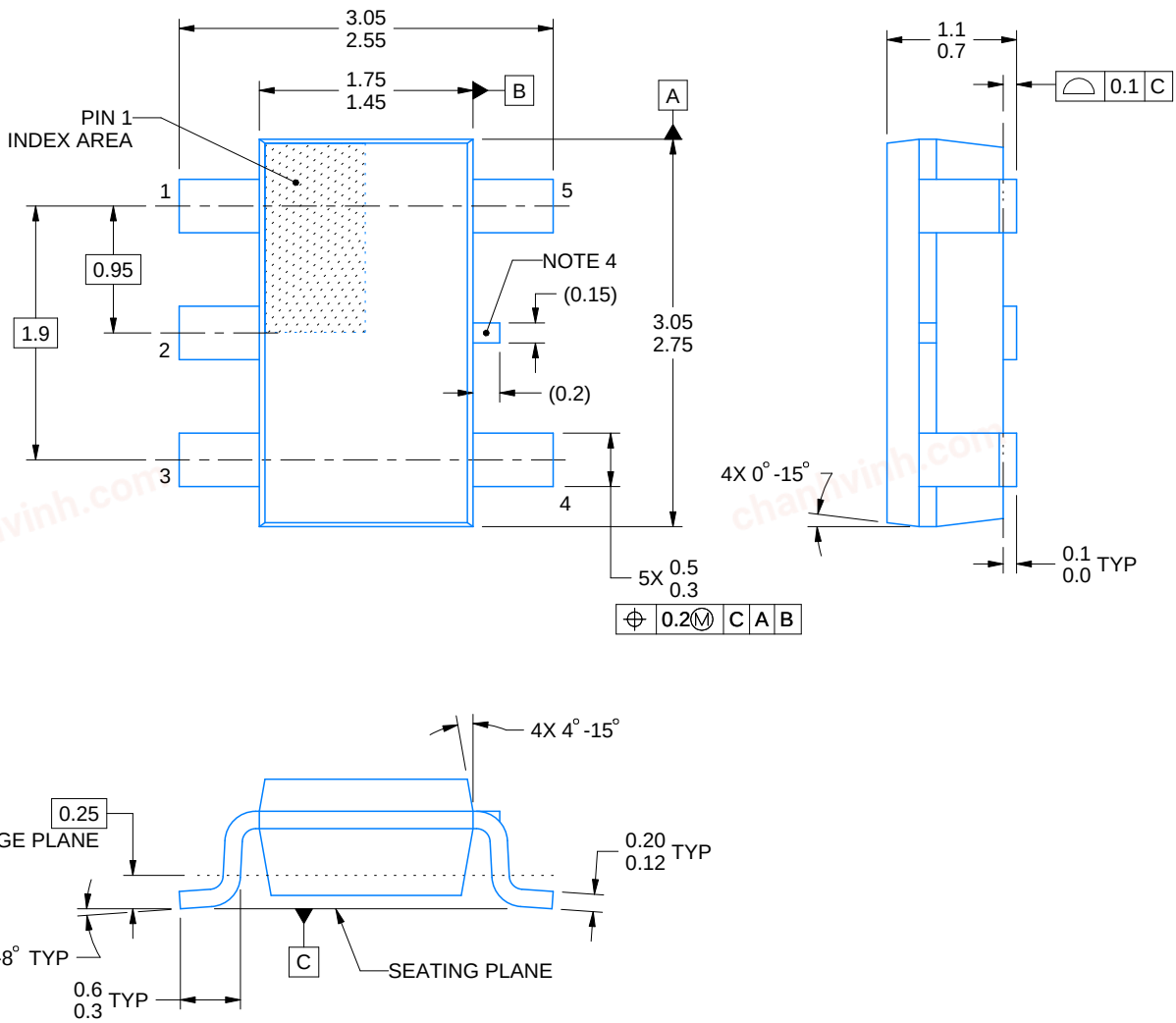
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PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.

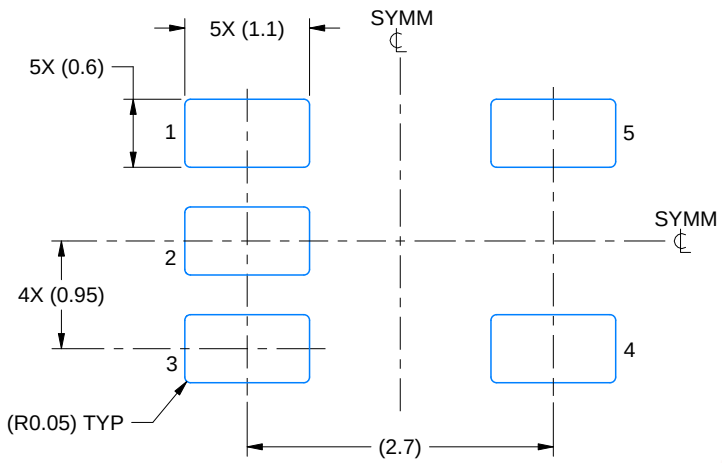
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EXAMPLE BOARD LAYOUT

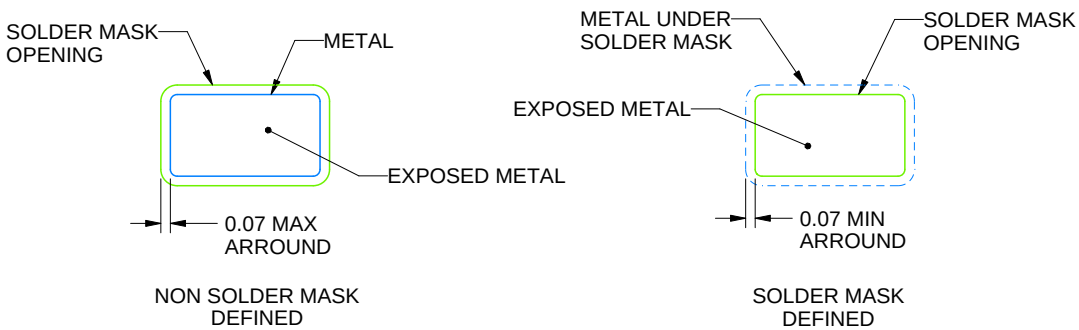
DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

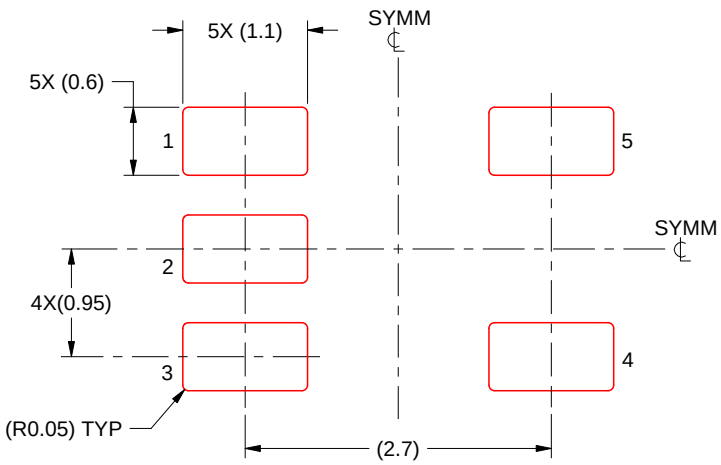
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EXAMPLE STENCIL DESIGN

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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