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TPS6303x High Efficiency Single Inductor Buck-Boost Converter With 1-A Switches

1 Features

- Input voltage range: 1.8 V to 5.5 V
- Fixed and adjustable output voltage options from 1.2 V to 5.5 V
- Up to 96% efficiency
- 800-mA Output current at 3.3 V in step-down mode (V_{IN} = 3.6 V to 5.5 V)
- Up to 500-mA output current at 3.3 V in boost mode (V_{IN} > 2.4 V)
- Automatic transition between step-down and boost mode
- Device quiescent current less than 50 μA
- Power-save mode for improved efficiency at low-output power
- Forced fixed frequency operation and synchronization possible
- Load disconnect during shutdown
- Overtemperature protection
- Available in a small 2.5-mm × 2.5-mm 10-pin VSON package (QFN)

2 Applications

- All two-cell and three-cell alkaline, NiCd or NiMH, or single-cell Li battery powered products
  - Smartphone
  - Portable media player
  - IP network camera
  - Blood glucose monitor
  - Portable data terminal

3 Description

The TPS6303x devices provide a power supply solution for products powered by either a two-cell or three-cell alkaline, NiCd or NiMH battery, or a one-cell Li-ion or Li-polymer battery. Output currents can go as high as 600 mA while using a single-cell Li-ion or Li-polymer battery, and discharge it down to 2.5 V or lower. The buck-boost converter is based on a fixed-frequency, pulse width modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low-load currents, the converter enters power-save mode to maintain high efficiency over a wide load current range. The power-save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average current in the switches is limited to a typical value of 1000 mA. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery.

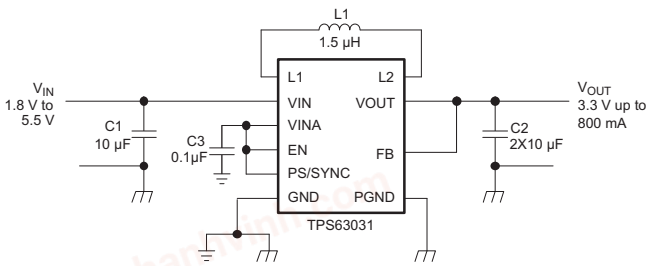
The TPS6303x devices operate over a free air temperature range of –40°C to 85°C. The devices are packaged in a 10-pin VSON package measuring 2.5-mm × 2.5-mm (DSK).

Device Information(1)

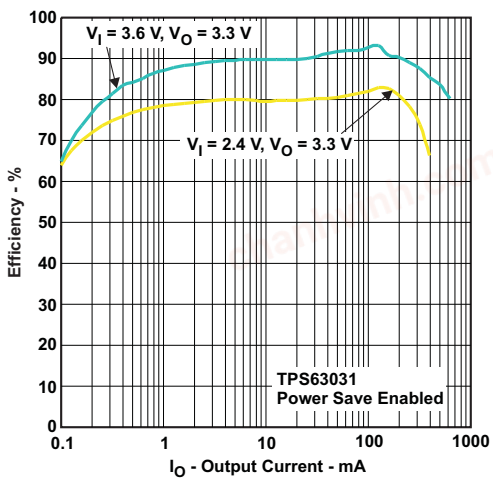
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS63030 TPS63031	VSON (10)	2.50 mm x 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency versus Output Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2014) to Revision D — **Page**

- Changed the max average switch current limit to 1300 mA ... 5
- Updated the *Soft Start and Short Circuit Protection* section ... 9
- Corrected typos ... 10
- Added Table 4 ... 13
- Corrected to TPS63030 ... 14
- Corrected to TPS63030 ... 14

Changes from Revision B (March 2012) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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5 Output Voltage Options(1)

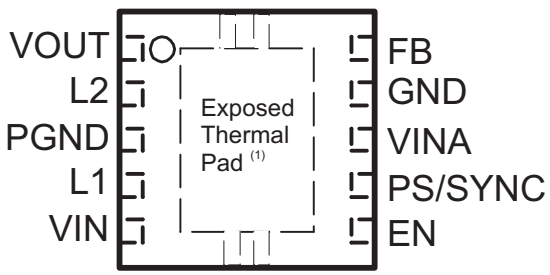
Table 1. Output Voltage Options

OUTPUT VOLTAGE DC/DC	PACKAGE MARKING	PACKAGE	PART NUMBER(1)
Adjustable	CEF	10-pin VSON	TPS63030DSK
3.3 V	CEF		TPS63031DSK

(1) Contact the factory to check availability of other fixed output voltage versions.
(1) The DSK package is available taped and reeled. Add R suffix to device type (for example, TPS63030DSKR) to order quantities of 3000 devices per reel. Add T suffix to device type (for example, TPS63030DSKT) to order quantities of 250 devices per reel.

6 Pin Configuration and Functions

DSK Package
10-Pin VSON
Top View



(1) The exposed thermal pad is connected to PGND.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	6	IN	Enable input (1 enabled, 0 disabled)
FB	10	IN	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
GND	9	—	Control / logic ground
L1	4	IN	Connection for inductor
L2	2	IN	Connection for inductor
PGND	3	—	Power ground
PS/SYNC	7	IN	Enable / disable power save mode (1 disabled, 0 enabled, clock signal for synchronization)
VIN	5	IN	Supply voltage for power stage
VINA	8	IN	Supply voltage for control stage
VOUT	1	OUT	Buck-boost converter output
Exposed Thermal Pad	—	—	The exposed thermal pad is connected to PGND.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage on VIN, VINA, L1, L2, VOUT, ILIM, EN, FB, SS	–0.3	7	V
Operating virtual junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage at VIN, VINA	1.8	5.5	V
Operating free air temperature, T_A	–40	85	°C
Operating virtual junction temperature, T_J	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6303x DSK (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_{IN}	Input voltage range			1.8		5.5	V
V_{IN}	Minimum input voltage for start-up		0°C ≤ T_A ≤ 85°C	1.6	1.8	1.9	V
V_{IN}	Minimum input voltage for start-up			1.6	1.8	2.0	V
V_{OUT}	TPS63030 output voltage range			1.2		5.5	V
	Minimum duty cycle in step-down conversion				30%	40%	
V_{FB}	TPS63030 feedback voltage		PS/SYNC = V_{IN}	495	500	505	mV
	TPS63031 output voltage			3.267	3.3	3.333	V
V_{FB}	TPS63030 feedback voltage		PS/SYNC = GND Referenced to 500 mV	-3%		+6%	
	TPS63031 output voltage		PS/SYNC = GND Referenced to 3.3 V	-3%		+6%	
f	Oscillator frequency			2200	2400	2600	kHz
	Frequency range for synchronization			2200	2400	2600	kHz
I_{SW}	Average switch current limit		V_{IN} = V_{INA} = 3.6 V, T_A = 25°C	900	1000	1300	mA
	High-side switch ON-resistance		V_{IN} = V_{INA} = 3.6 V		200		mΩ
	Low-side switch ON-resistance		V_{IN} = V_{INA} = 3.6 V		200		mΩ
	Maximum line regulation				0.5%		
	Maximum load regulation				0.5%		
I_q	Quiescent current	VIN and VINA	I_{OUT} = 0 mA, V_{EN} = V_{IN} = V_{INA} = 3.6 V, V_{OUT} = 3.3 V		25	35	µA
		VOUT			4	6	µA
	TPS63031 FB input impedance		V_{EN} = HIGH		1		MΩ
I_S	Shutdown current		V_{EN} = 0 V, V_{IN} = V_{INA} = 3.6 V		0.1	0.9	µA
CONTROL STAGE							
V_{UVLO}	Under voltage lockout threshold		V_{INA} voltage decreasing	1.4	1.5	1.6	V
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current		Clamped on GND or VINA		0.01	0.1	µA
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

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7.6 Typical Characteristics

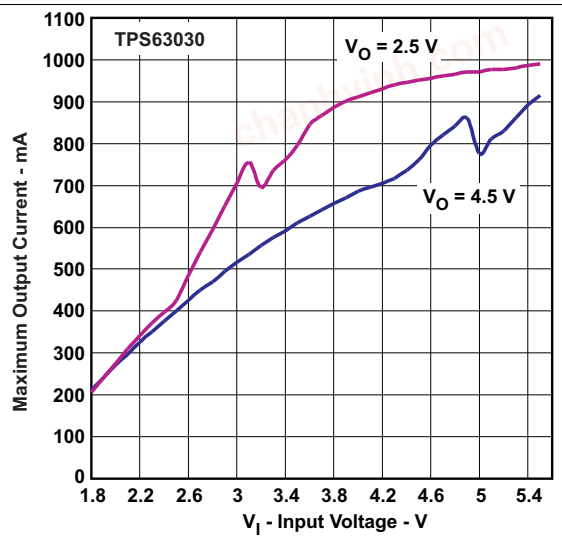

Figure 1. Maximum Output Current versus Input Voltage, TPS63030

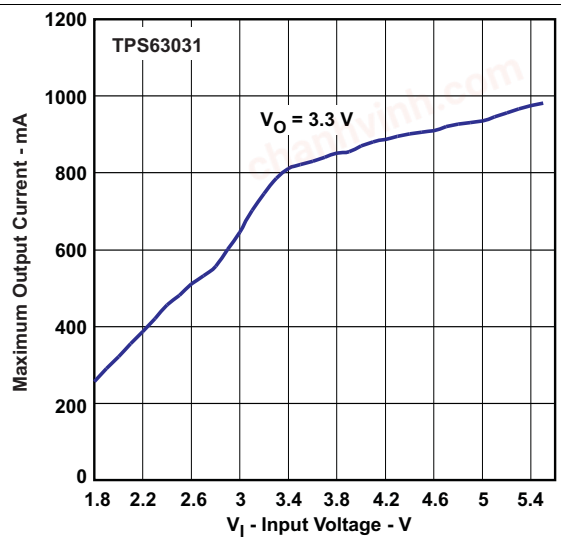

Figure 2. Maximum Output Current versus Input Voltage, TPS63031

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8 Detailed Description

8.1 Overview

The controlling circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. The controller also uses input and output voltage feed forward. Changes of input and output voltage are monitored and can immediately change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. At adjustable output voltages, a resistive voltage divider must be connected to that pin. At fixed output voltages, FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage is compared with the internal reference voltage to generate a stable and accurate output voltage.

The controller circuit also senses the average input current as well as the peak input current. With this, maximum input power can be controlled as well as the maximum peak current to achieve a safe and stable operation under all possible conditions. To finally protect the device from overheating, an internal temperature sensor is implemented.

The device uses four internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range.

To avoid ground shift problems due to the high currents in the switches, two separate ground pins, GND and PGND, are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point ideally close to the GND pin. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter.

8.2 Functional Block Diagrams

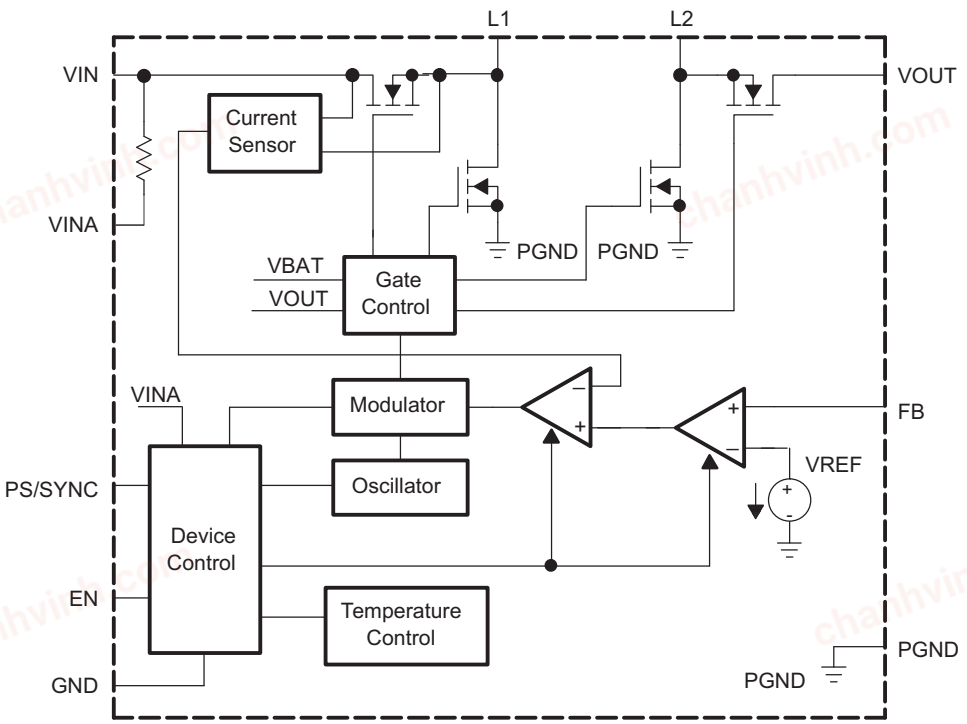

Figure 3. Functional Block Diagram (TPS63030)

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Functional Block Diagrams (continued)

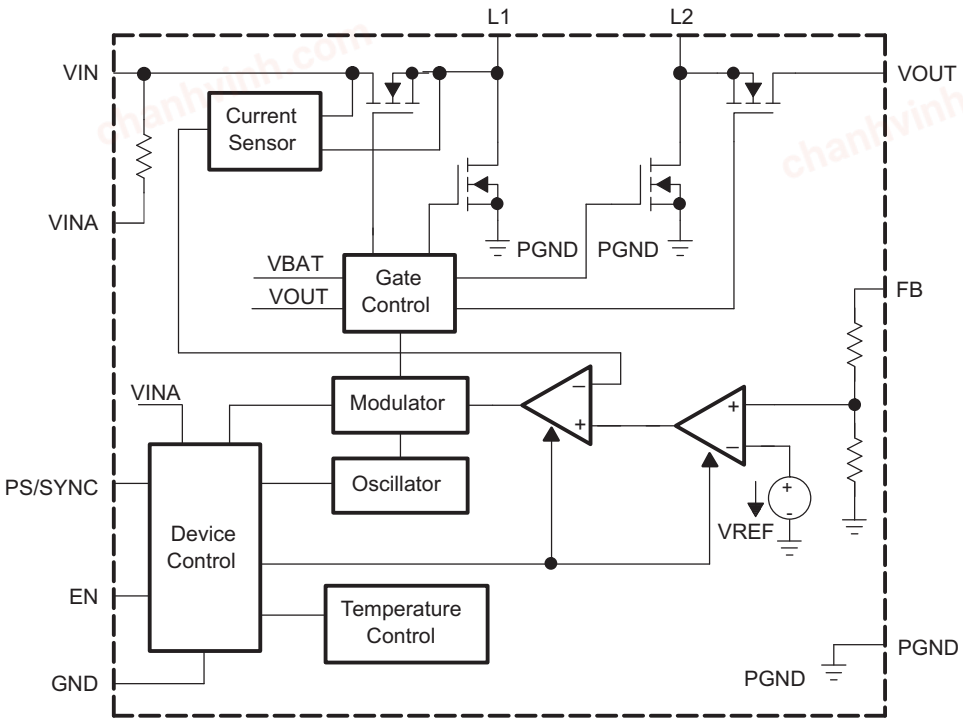

Figure 4. Functional Block Diagram (TPS63031)

8.3 Feature Description

8.3.1 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown. During the start-up of the converter, the duty cycle and the peak current are limited to avoid high peak currents flowing from the input.

8.3.2 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage at VINA is lower than approximately its threshold (see the *Electrical Characteristics*). When in operation, the device automatically enters the shutdown mode if the voltage at VINA drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

8.3.3 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see the *Electrical Characteristics*), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

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8.4 Device Functional Modes

8.4.1 Soft Start and Short Circuit Protection

After being enabled, the device starts operating. The average current limit ramps up from zero to the nominal current limit value. Thus, the output voltage overshoot at start-up, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner, even if a very large capacitor is connected at the output.

At an overload or short circuit condition at the output, the average current limit protects the device itself and the application. Higher change rates of output current or input voltage can trigger an additional built-in short circuit protection mode, which reduces the current limit to less than 50% of the nominal current limit. In this mode, the switching frequency can be reduced as well.

8.4.2 Buck-Boost Operation

To regulate the output voltage properly at all possible input voltage conditions, the device automatically switches from step-down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step-down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation where all four switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum to minimize switching and conduction losses. Switching losses are also kept low by using only one active and one passive switch. For the remaining two switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

8.4.3 Power-Save Mode and Synchronization

The PS/SYNC pin can be used to select different operation modes. To enable power-save, PS/SYNC must be set low. Power-save mode is used to improve efficiency at light load. If power-save mode is enabled, the converter stops operating if the average inductor current gets lower than about 100 mA and the output voltage is at or above its nominal value. If the output voltage decreases below its nominal value, the device ramps up the output voltage again by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last for one or several pulses. The converter again stops operating once the conditions for stopping operation are met again.

The power save mode can be disabled by programming high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency. Synchronization is done by a phase-locked loop (PLL), so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS63030 and TPS63031 are buck-boost converters suitable for applications that need a regulated output voltage from an input supply that is higher or lower than the desired output voltage.

9.2 Typical Application

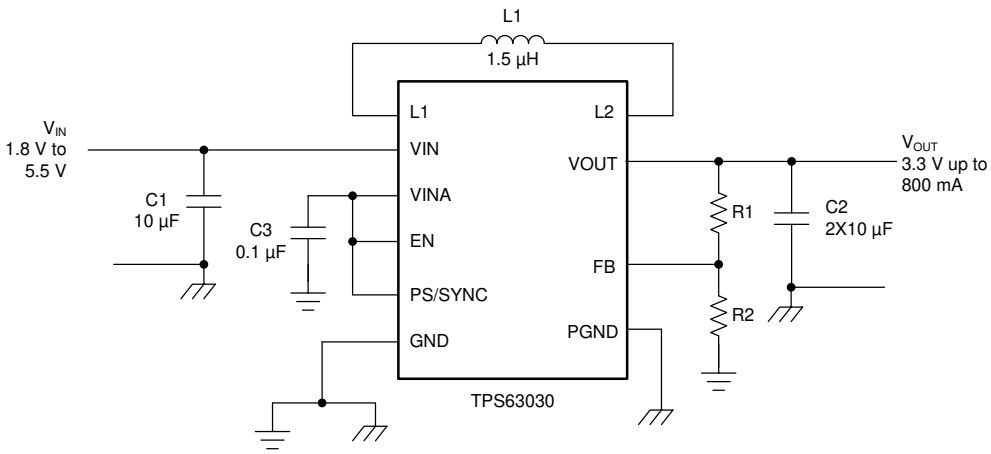

Figure 5. Typical Application Circuit for Adjustable Output Voltage

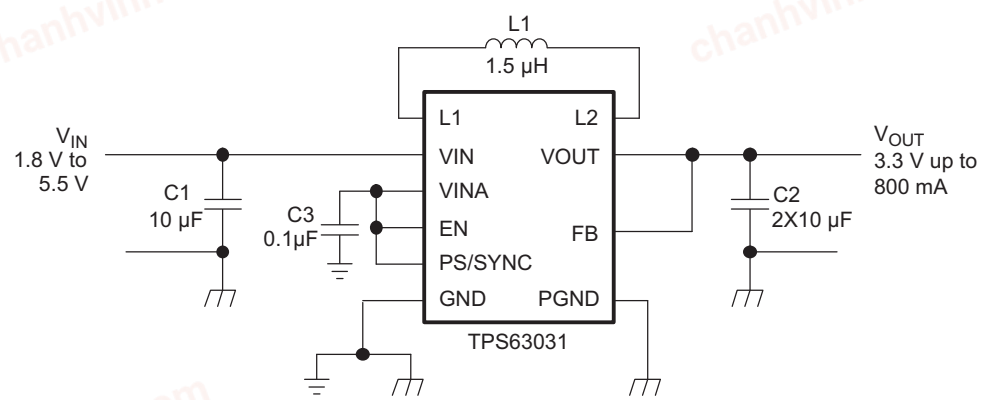

Figure 6. Typical Application Circuit for 3.3-V Fixed Output Voltage Option

9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the *Recommended Operating Conditions*.

Table 2 shows ths list of components for the application curves.

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Typical Application (continued)

Table 2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS6303 0 / 1	Texas Instruments
L1	1.5 µH, 3 mm x 3 mm x 1.5 mm	LPS3015-1R5, Coilcraft
C1	10 µF 6.3V, 0603, X7R ceramic	GRM188R60J106KME84D, Murata
C2	2 × 10 µF 6.3V, 0603, X7R ceramic	GRM188R60J106KME84D, Murata
C3	0.1 µF, X7R ceramic	
R1, R2	Depending on the output voltage at TPS63030, not used at TPS63031	

9.2.2 Detailed Design Procedure

9.2.2.1 Programming the Output Voltage

Within the TPS6303x family, there are fixed and adjustable output voltage versions available. To properly configure the fixed output voltage devices, the FB pin is used to sense the output voltage. This means that it must be connected directly to VOUT. At the adjustable output voltage versions, an external resistor divider is used to adjust the output voltage. The resistor divider must be connected between VOUT, FB, and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The current through the resistive divider must be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across the resistor between FB and GND, R_2, is typically 500 mV. Based on those two values, the recommended value for R_2 must be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. TI recommends to keep the value for this resistor in the range of 200 kΩ. From that, the value of the resistor connected between VOUT and FB, R_1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 1.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (1)$$

9.2.2.2 Inductor Selection

The inductor selection is affected by several parameter like inductor ripple current, output voltage ripple, transition point into power-save mode, and efficiency. See Table 3 for typical inductors.

Table 3. List of Recommended Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	LPS3015
	EPL3010
Murata	LQH3NP
Tajo Yuden	NR3015

For high efficiencies, the inductor must have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 3. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \quad (2)$$

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where

- D = duty cycle in boost mode
- f = converter switching frequency (typical 2.5 MHz)
- L = inductor value
- η = estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption) (3)

NOTE

The calculation must be done for the minimum input voltage which is possible to have in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. TI recommends to choose an inductor with a saturation current 20% higher than the value calculated using Equation 3. Possible inductors are listed in *Table 3*.

9.2.2.3 Capacitor Selection

9.2.2.3.1 *Input Capacitor*

At least a 4.7-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

9.2.2.3.2 *Bypass Capacitor*

To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor can be connected between VINA and GND. Using a ceramic capacitor with a value of 0.1 µF is recommended. The value of this capacitor should not be higher than 0.22 µF.

9.2.2.3.3 *Output Capacitor*

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. The recommended nominal output capacitance value is 10 µF.

There is also no upper limit for the output capacitance value. Larger capacitors causes lower output voltage ripple as well as lower output voltage drop during load transients.

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9.2.3 Application Curves

Table 4. Application Curves

PARAMETER	CONDITION	FIGURE
Efficiency versus Output Current, TPS63030, Power-Save Enabled		Figure 7
Efficiency versus Output Current, TPS63030, Power-Save Disabled		Figure 8
Efficiency versus Output Current, TPS63031, Power-Save Enabled		Figure 9
Efficiency versus Output Current, TPS63031, Power-Save Disabled		Figure 10
Efficiency versus Input Voltage, TPS63030, Power-Save Enabled	V_{OUT} = 2.5 V	Figure 11
Efficiency versus Input Voltage, TPS63030, Power-Save Enabled	V_{OUT} = 4.5 V	Figure 13
Efficiency versus Input Voltage, TPS63030, Power-Save Disabled	V_{OUT} = 2.5 V	Figure 13
Efficiency versus Input Voltage, TPS63030, Power-Save Disabled	V_{OUT} = 3.3 V	Figure 14
Efficiency versus Input Voltage, TPS63031, Power-Save Enabled	V_{OUT} = 3.3 V	Figure 15
Efficiency versus Input Voltage, TPS63031, Power-Save Disabled	V_{OUT} = 3.3 V	Figure 16
Output Voltage versus Output Current, TPS63031, Power-Save Disabled	V_{IN} = 3.6 V / V_{OUT} = 2.5 V	Figure 17
Output Voltage versus Output Current, TPS63031, Power Save Disabled	V_{IN} = 3.6 V / V_{OUT} = 3.3 V	Figure 19
Load Transient Response, TPS63031	V_{IN} = 2.4 V / V_{OUT} = 3.3 V	Figure 20
Load Transient Response, TPS63031	V_{IN} = 4.2 V / V_{OUT} = 3.3 V	Figure 21
Line Transient Response, TPS63031	V_{IN} = 3.0 V / V_{OUT} = 3.3 V	Figure 22
Start-up After Enable, TPS63031	V_{IN} = 2.4 V / V_{OUT} = 3.3 V	Figure 23
Start-up After Enable, TPS63031	V_{IN} = 4.2 V / V_{OUT} = 3.3 V	Figure 24

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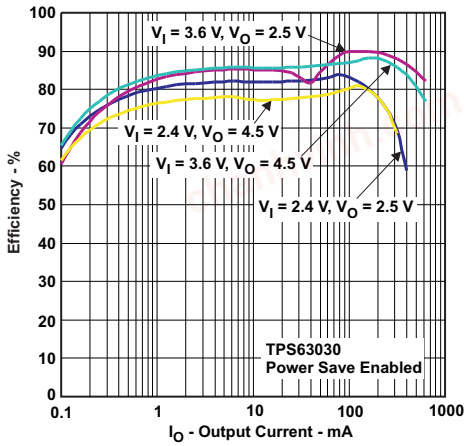

Figure 7. Efficiency versus Output Current, TPS63030, Power-Save Enabled

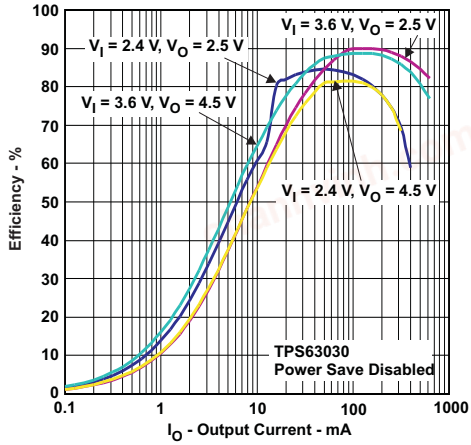

Figure 8. Efficiency versus Output Current, TPS63030, Power-Save Disabled

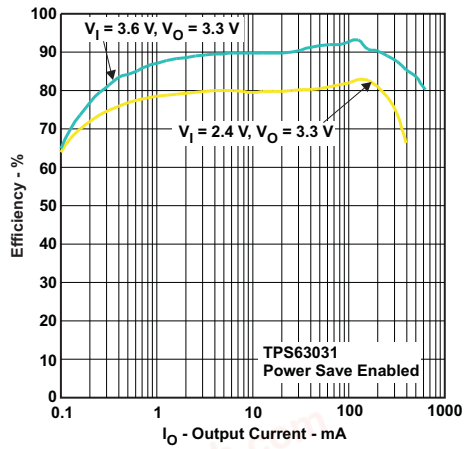

Figure 9. Efficiency versus Output Current, TPS63031, Power-Save Enabled

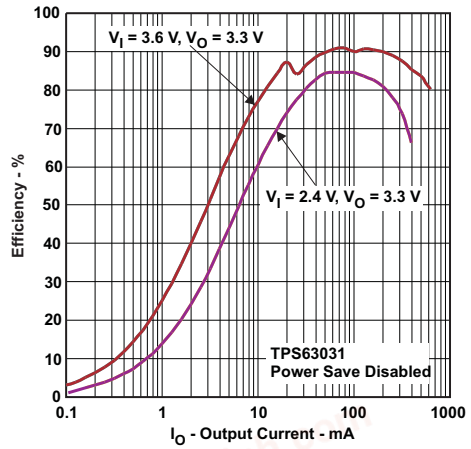

Figure 10. Efficiency versus Output Current, TPS63031, Power-Save Disabled

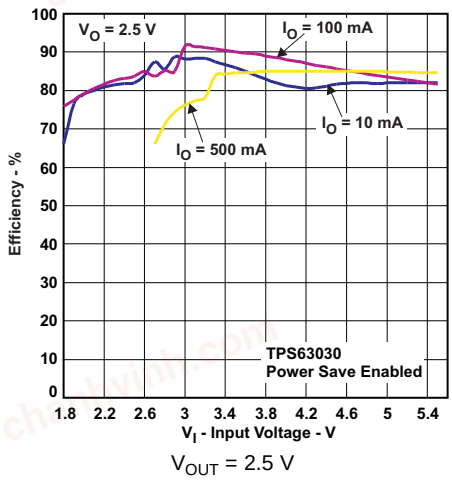

Figure 11. Efficiency versus Input Voltage, TPS63030, Power-Save Enabled

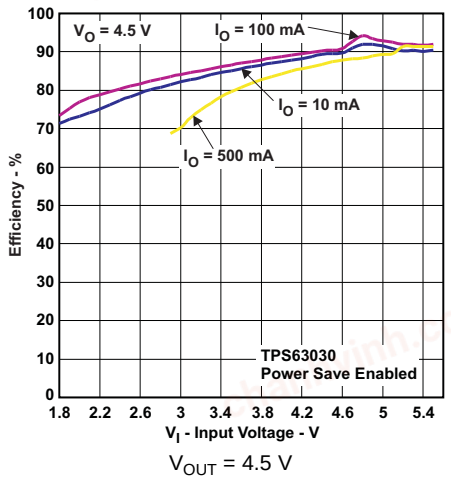

Figure 12. Efficiency versus Input Voltage, TPS63030, Power-Save Enabled

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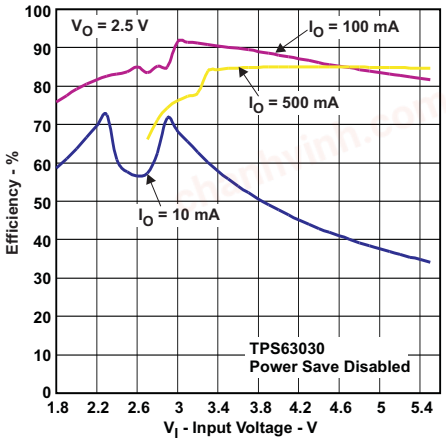
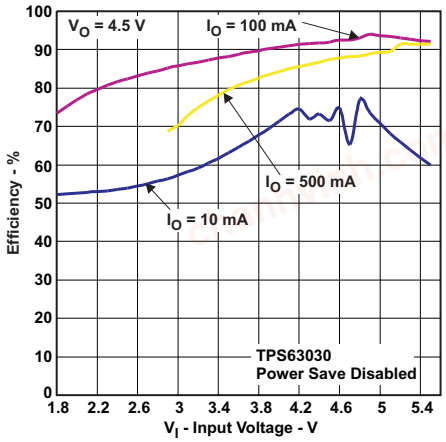


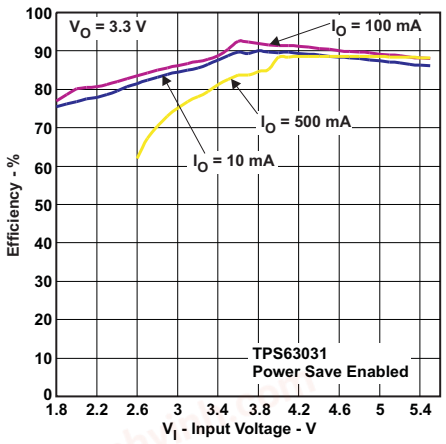
V_{OUT} = 2.5 V

Figure 13. Efficiency versus Input Voltage, TPS63030, Power-Save Disabled



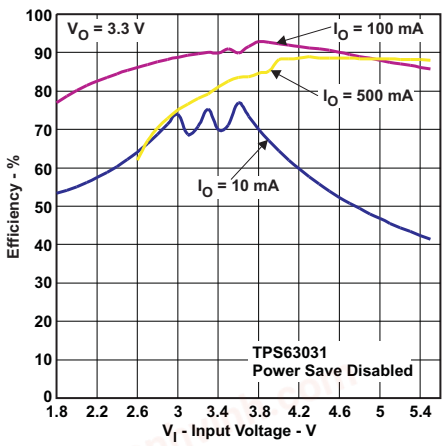
V_{OUT} = 4.5 V

Figure 14. Efficiency versus Input Voltage, TPS63030, Power-Save Disabled



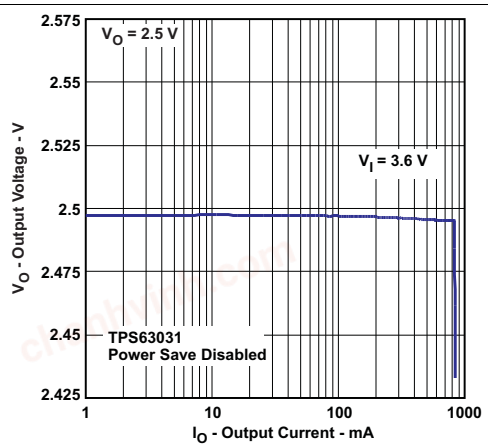
V_{OUT} = 3.3 V

Figure 15. Efficiency versus Input Voltage, TPS63031, Power-Save Enabled



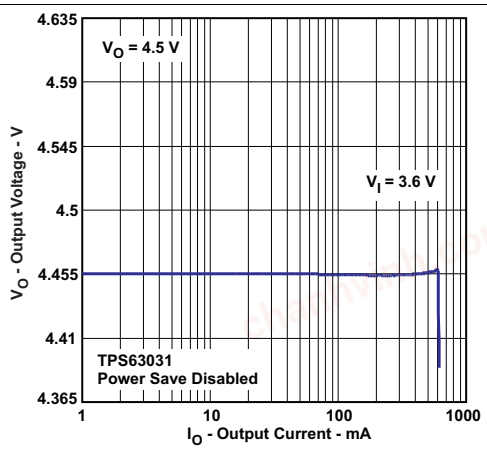
V_{OUT} = 3.3 V

Figure 16. Efficiency versus Input Voltage, TPS63031, Power-Save Disabled



V_{IN} = 3.6 V / V_{OUT} = 2.5 V

Figure 17. Output Voltage versus Output Current, TPS63030, Power-Save Disabled



V_{IN} = 3.6 V / V_{OUT} = 4.5 V

Figure 18. Output Voltage versus Output Current, TPS63030, Power Save Disabled

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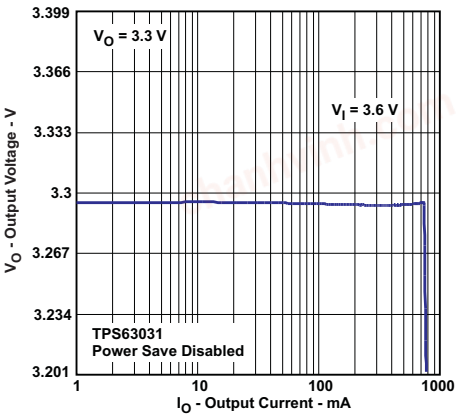


V_{IN} = 3.6 V / V_{OUT} = 3.3 V

Figure 19. Output Voltage versus Output Current, TPS63031, Power Save Disabled

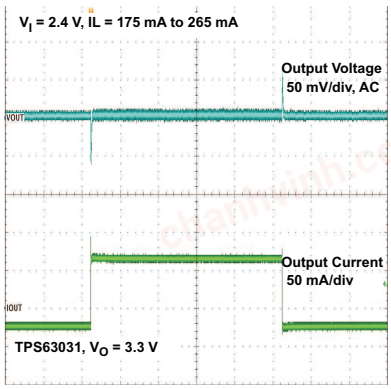
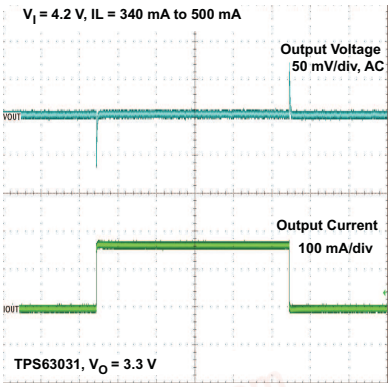
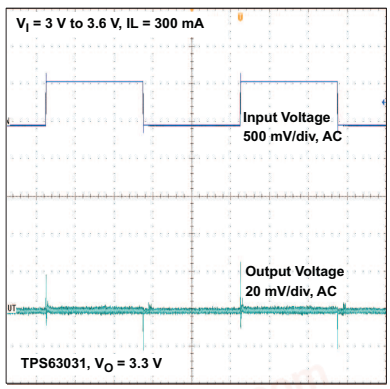


Figure 20. Load Transient Response, TPS63031



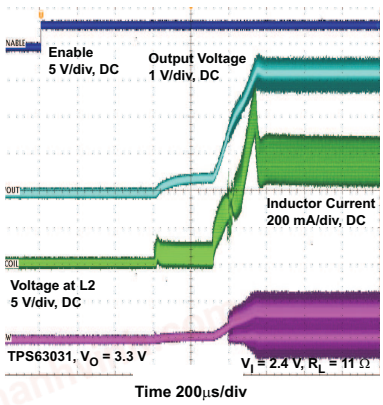
V_{IN} = 4.2 V / V_{OUT} = 3.3 V

Figure 21. Load Transient Response, TPS63031



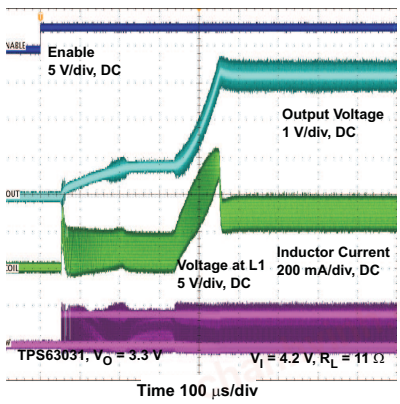
V_{IN} = 3.0 V / V_{OUT} = 3.3 V

Figure 22. Line Transient Response, TPS63031



V_{IN} = 2.4 V / V_{OUT} = 3.3 V

Figure 23. Start-up After Enable, TPS63031



V_{IN} = 4.2 V / V_{OUT} = 3.3 V

Figure 24. Start-up After Enable, TPS63031

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10 Power Supply Recommendations

The TPS6303x devices have no special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPS6303x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor must be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider must be placed as close as possible to the control ground pin of the IC. To lay out the control ground, TI recommends to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

11.2 Layout Example

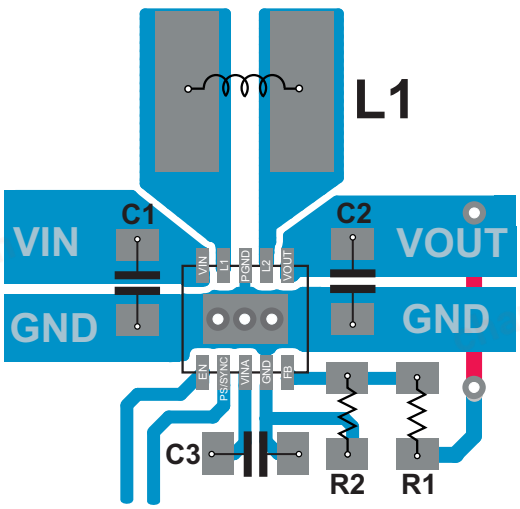

Figure 25. Layout Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

The follow are three basic approaches for enhancing thermal performance:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table, check the *Thermal Characteristics Application Note* and the *Semiconductor and IC Package Thermal Metrics Application Note*.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Thermal Characteristics Application Note*

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS63030	Click here	Click here	Click here	Click here	Click here
TPS63031	Click here	Click here	Click here	Click here	Click here

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

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12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS63030DSKR	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	CEE
TPS63030DSKR.A	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEE
TPS63030DSKRG4	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEE
TPS63030DSKRG4.A	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEE
TPS63030DSKT	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	CEE
TPS63030DSKT.A	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEE
TPS63031DSKR	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	CEF
TPS63031DSKR.A	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEF
TPS63031DSKRG4	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEF
TPS63031DSKRG4.A	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEF
TPS63031DSKT	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	CEF
TPS63031DSKT.A	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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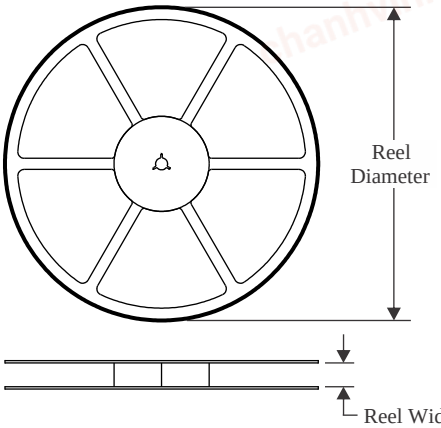
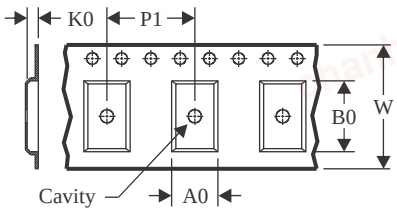
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

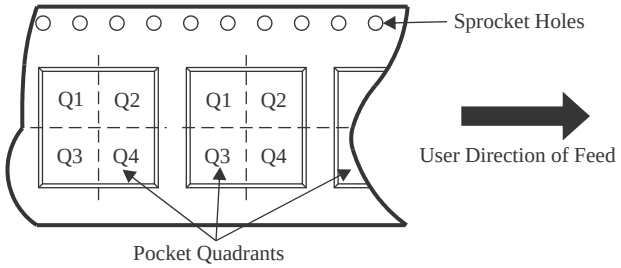


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63030DSKR	SON	DSK	10	3000	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2
TPS63030DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS63030DSKRG4	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS63030DSKT	SON	DSK	10	250	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS63031DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS63031DSKR	SON	DSK	10	3000	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2
TPS63031DSKRG4	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS63031DSKT	SON	DSK	10	250	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

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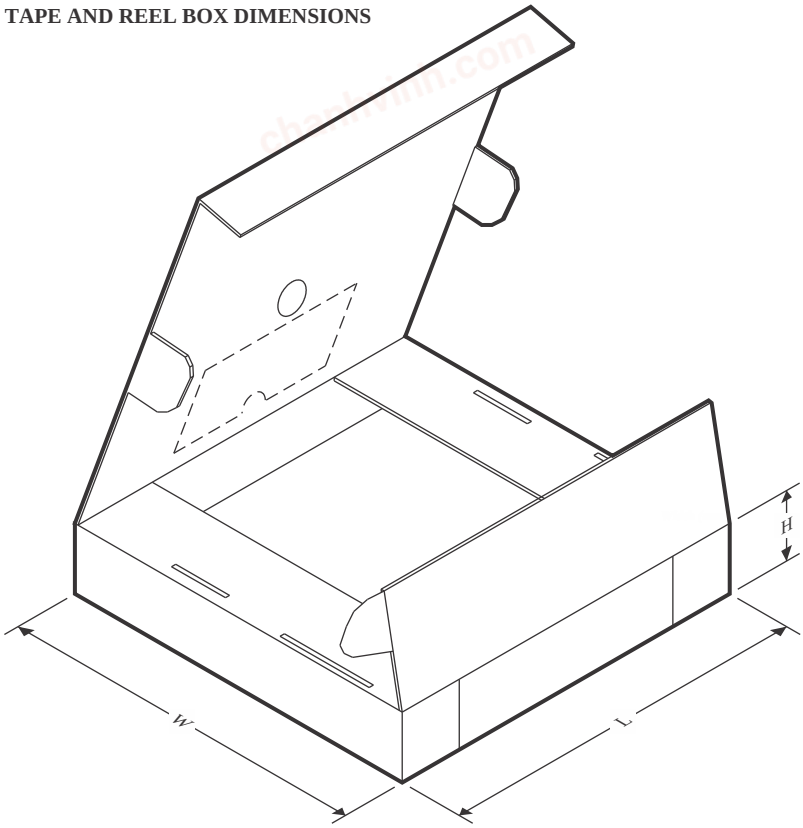
PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63030DSKR	SON	DSK	10	3000	205.0	200.0	33.0
TPS63030DSKR	SON	DSK	10	3000	182.0	182.0	20.0
TPS63030DSKRG4	SON	DSK	10	3000	182.0	182.0	20.0
TPS63030DSKT	SON	DSK	10	250	182.0	182.0	20.0
TPS63031DSKR	SON	DSK	10	3000	182.0	182.0	20.0
TPS63031DSKR	SON	DSK	10	3000	205.0	200.0	33.0
TPS63031DSKRG4	SON	DSK	10	3000	182.0	182.0	20.0
TPS63031DSKT	SON	DSK	10	250	182.0	182.0	20.0

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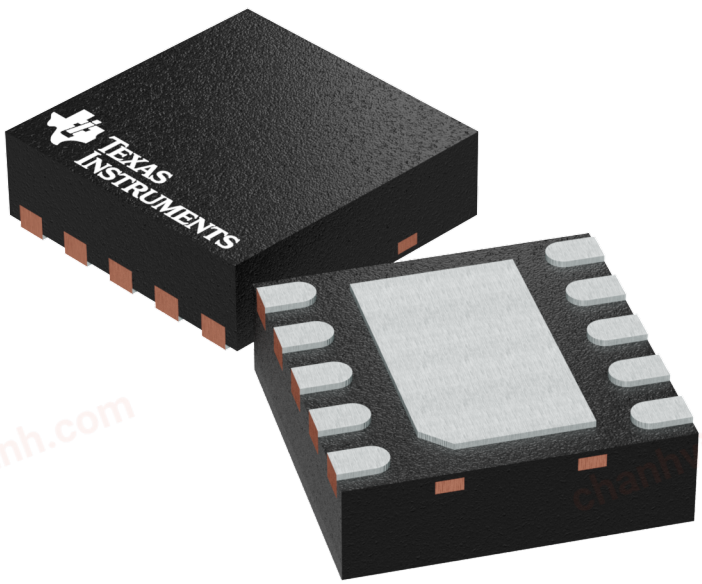
GENERIC PACKAGE VIEW

DSK 10 WSON - 0.8 mm max height

2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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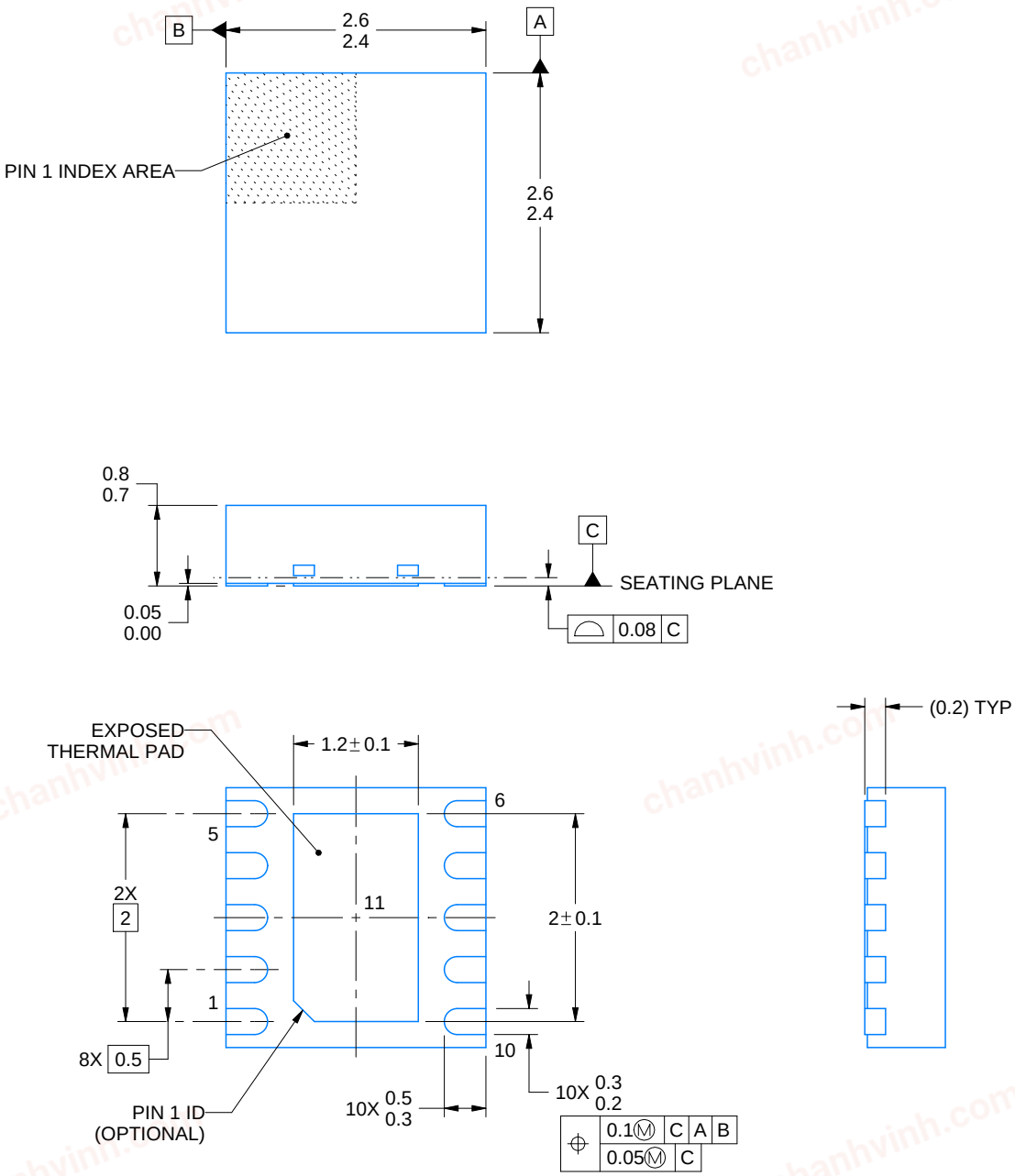
PACKAGE OUTLINE

DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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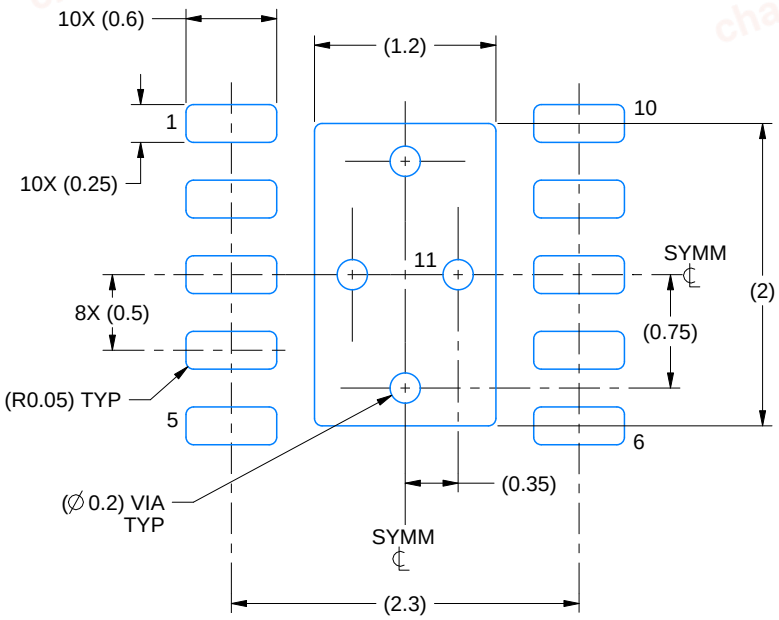
EXAMPLE BOARD LAYOUT

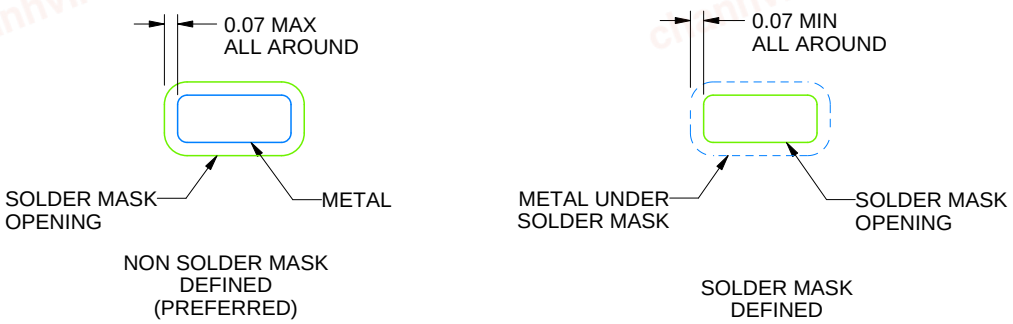
DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

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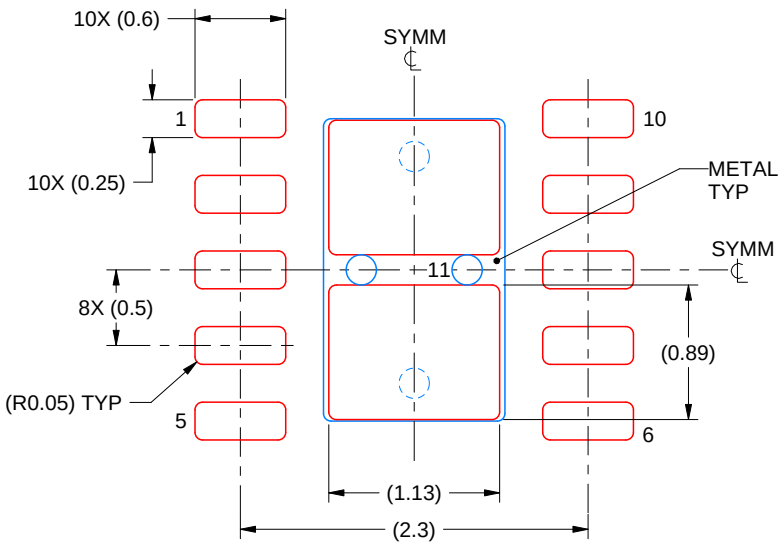
EXAMPLE STENCIL DESIGN

DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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