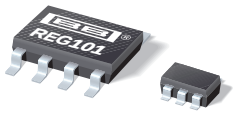
chanhvinh.com

Burr-Brown Products from Texas Instruments

REG101



SBVS026D – JULY 2001 – REVISED SEPTEMBER 2005

DMOS 100mA Low-Dropout Regulator

FEATURES

- NEW DMOS TOPOLOGY:
  Ultra Low Dropout Voltage:
  60mV typ at 100mA
  Output capacitor NOT required for stability
- FAST TRANSIENT RESPONSE
- VERY LOW NOISE: 23μVrms
- HIGH ACCURACY: ±1.5% max
- HIGH EFFICIENCY:
  I_{GND} = 500μA at I_{OUT} = 100mA
  Not Enabled: I_{GND} = 10nA
- 2.5V, 2.8V, 2.85V, 3.0V, 3.3V, 5.0V, AND ADJUSTABLE OUTPUT VERSIONS
- OTHER OUTPUT VOLTAGES AVAILABLE UPON REQUEST
- FOLDBACK CURRENT LIMIT
- THERMAL PROTECTION
- SMALL SURFACE-MOUNT PACKAGES:
  SOT23-5 and SO-8

APPLICATIONS

- PORTABLE COMMUNICATION DEVICES
- BATTERY-POWERED EQUIPMENT
- PERSONAL DIGITAL ASSISTANTS
- MODEMS
- BAR-CODE SCANNERS
- BACKUP POWER SUPPLIES

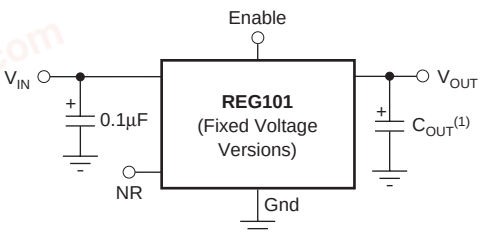
DESCRIPTION

The REG101 is a family of low-noise, low-dropout linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low dropout voltage (only 60mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1μF.

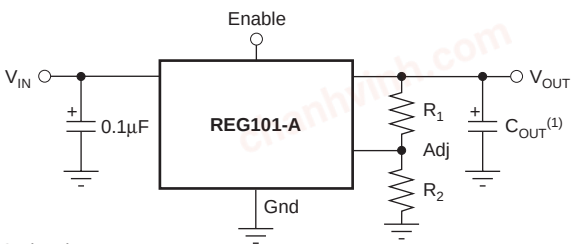
Typical ground pin current is only 500μA (at I_{OUT} = 100mA) and drops to 10nA when not in enabled mode. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variation and under dropout conditions.

The REG101 has very low output noise (typically 23μVrms for V_{OUT} = 3.3V with C_{NR} = 0.01μF), making it ideal for use in portable communications equipment. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (–40°C to +85°C).

The REG101 is well protected—internal circuitry provides a current limit that protects the load from damage. Thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG101 is available in the SOT23-5 and the SO-8 packages.



NR = Noise Reduction



NOTE: (1) Optional.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2000-2005, Texas Instruments Incorporated

chanhvinh.com

ABSOLUTE MAXIMUM RATINGS(1)

Supply Input Voltage, V_{IN}	–0.3V to 12V
Enable Input Voltage, V_{EN}	–0.3V to V_{IN}
Feedback Voltage, V_{FB}	–0.3V to 6.0V
NR Pin Voltage, V_{NR}	–0.3V to 6.0V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range (T_J)	–55°C to +125°C
Storage Temperature Range (T_A)	–65°C to +150°C
Lead Temperature (soldering, 3s, SOT23-5, and SO-8)	+240°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
REG101**xx-yyyy/zzz**	**XX** is package designator. **YYYY** is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable). **ZZZ** is package quantity.

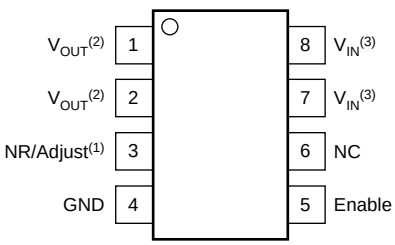
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Output voltages from 2.5V to 5.1V in 50mV increments are available; minimum order quantities apply. Contact factory for details and availability.

PIN CONFIGURATIONS

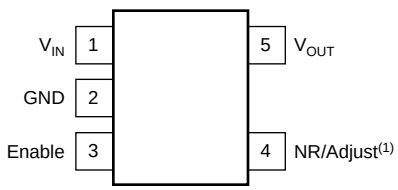
Top View

SO-8



(U Package)

SOT23-5



(N Package)

NOTE: (1) For REG101A-A: voltage setting resistor pin. All other models: noise reduction capacitor pin.
(2) Both pin 1 and pin 2 must be connected.
(3) Both pin 7 and pin 8 must be connected.

chanhvinh.com

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_J = –40°C to +85°C.**

At T_J = +25°C, V_{IN} = V_{OUT} + 1V (V_{OUT} = 2.5V for REG101-A), V_{ENABLE} = 1.8V, I_{OUT} = 2mA, C_{NR} = 0.01µF, and C_{OUT} = 0.1µF[1], unless otherwise noted.

PARAMETER		CONDITION	REG101NA REG101UA MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
Output Voltage	V_{OUT}					
REG101-2.5				2.5		V
REG101-2.8				2.8		V
REG101-2.85				2.85		V
REG101-3.0				3.0		V
REG101-3.3				3.3		V
REG101-5				5		V
REG101-A			2.5		5.5	V
Reference Voltage	V_{REF}			1.267		V
Adjust Pin Current	I_{ADJ}			0.2	1	µA
Accuracy				±0.5	±1.5	%
Over Temperature					**±2.2**	%
vs Temperature	**dV_{OUT}/dT**			**50**		ppm/°C
Includes Line and Load		I_{OUT} = 2mA to 100mA, V_{IN} = (V_{OUT} + 0.4V) to 10V		±0.8	±2.0	%
Over Temperature		**V_{IN} = (V_{OUT} + 0.6V) to 10V**			**±2.7**	**%**
DC DROPOUT VOLTAGE[2]	V_{DROP}	I_{OUT} = 2mA		4	10	mV
For all models		I_{OUT} = 100mA		60	100	mV
Over Temperature		**I_{OUT} = 100mA**			**130**	mV
VOLTAGE NOISE	V_n	f = 10Hz to 100kHz				
Without C_{NR}		C_{NR} = 0, C_{OUT} = 0		23µVrms/V • V_{OUT}		µVrms
With C_{NR} (all fixed voltage models)		C_{NR} = 0.01µF, C_{OUT} = 10µF		7µVrms/V • V_{OUT}		µVrms
OUTPUT CURRENT						
Current Limit[3]	I_{CL}		130	170	220	mA
Over Temperature			**110**		**240**	mA
Short-Circuit Current	I_{SC}			60		mA
RIPPLE REJECTION						
f = 120Hz		I_{OUT} = 100mA		65		dB
ENABLE CONTROL						
V_{ENABLE} High (output enabled)	V_{ENABLE}		1.8		V_{IN}	V
V_{ENABLE} Low (output disabled)			–0.2		0.5	V
I_{ENABLE} High (output enabled)	I_{ENABLE}	V_{ENABLE} = 1.8V to V_{IN}, V_{IN} = 1.8V to 6.5[4]		1	100	nA
I_{ENABLE} Low (output disabled)		V_{ENABLE} = 0V to 0.5V		2	100	nA
Output Disable Time		C_{OUT} = 1.0µF, R_{LOAD} = 33Ω		200		µs
Output Enable Time		C_{OUT} = 1.0µF, R_{LOAD} = 33Ω		1.5		ms
THERMAL SHUTDOWN						
Junction Temperature						
Shutdown				160		°C
Reset from Shutdown				140		°C
GROUND PIN CURRENT						
Ground Pin Current	I_{GND}	I_{OUT} = 2mA		400	500	µA
		I_{OUT} = 100mA		500	650	µA
Enable Pin Low		V_{ENABLE} ≤ 0.5V		0.01	0.2	µA
INPUT VOLTAGE	V_{IN}					
Operating Input Voltage Range[5]			1.8		10	V
Specified Input Voltage Range		V_{IN} > 1.8V	V_{OUT} + 0.4		10	V
Over Temperature		**V_{IN} > 1.8V**	**V_{OUT} + 0.6**		**10**	V
TEMPERATURE RANGE						
Specified Range	T_J		–40		+85	°C
Operating Range	T_J		–55		+125	°C
Storage Range	T_A		–65		+150	°C
Thermal Resistance						
SOT23-5 Surface Mount	θ_{JA}	Junction-to-Ambient		200		°C/W
SO-8 Surface Mount	θ_{JA}	Junction-to-Ambient		150		°C/W

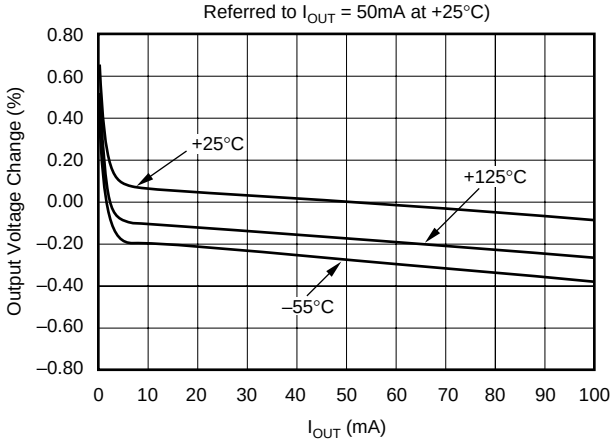
NOTES: (1) The REG101 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection.
(2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at V_{IN} = V_{OUT} + 1V at fixed load.
(3) Current limit is the output current that produces a 10% change in output voltage from V_{IN} = V_{OUT} + 1V and I_{OUT} = 2mA.
(4) For V_{ENABLE} > 6.5V, see typical characteristic "I_{ENABLE} vs V_{ENABLE}".
(5) The REG101 no longer regulates when V_{IN} < V_{OUT} + $V_{DROP\ (MAX)}$. In drop-out, the impedance from V_{IN} to V_{OUT} is typically less than 1Ω at T_J = +25°C.

chanhvinh.com

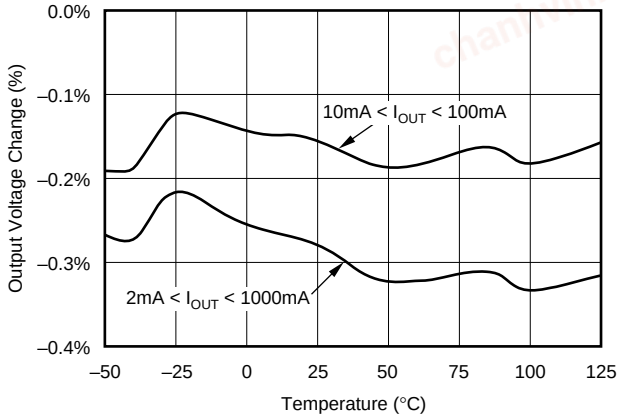
TYPICAL CHARACTERISTICS

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

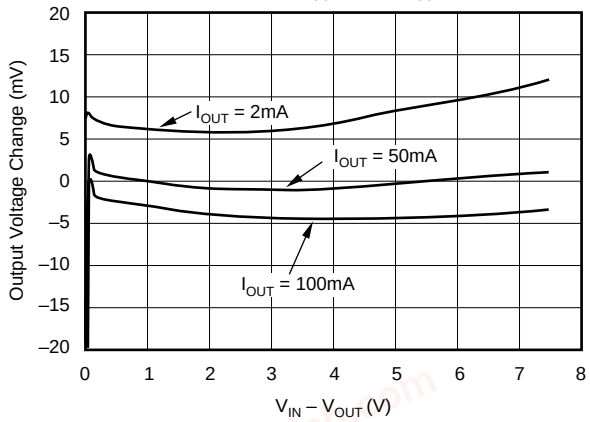
OUTPUT VOLTAGE CHANGE vs I_{OUT}
(V_{IN} = V_{OUT} + 1V, Output Voltage % Change
Referred to I_{OUT} = 50mA at +25°C)



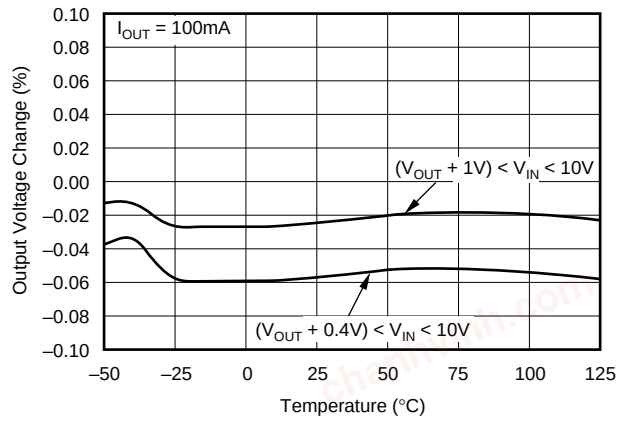
LOAD REGULATION vs TEMPERATURE
(V_{IN} = V_{OUT} + 1V)



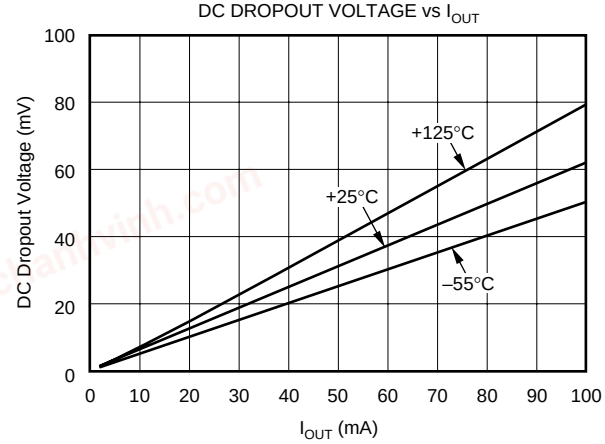
LINE REGULATION
(Referred to V_{IN} = V_{OUT} + 1V at I_{OUT} = 50mA)



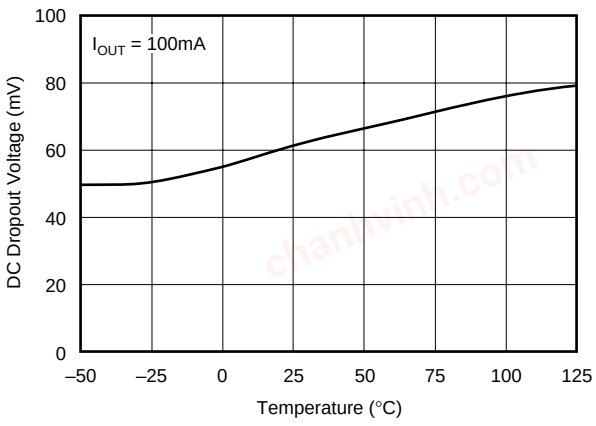
LINE REGULATION vs TEMPERATURE



DC DROPOUT VOLTAGE vs I_{OUT}



DC DROPOUT VOLTAGE vs TEMPERATURE

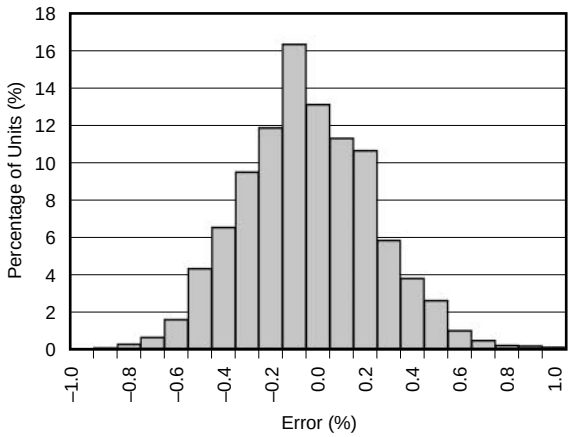


chanhvinh.com

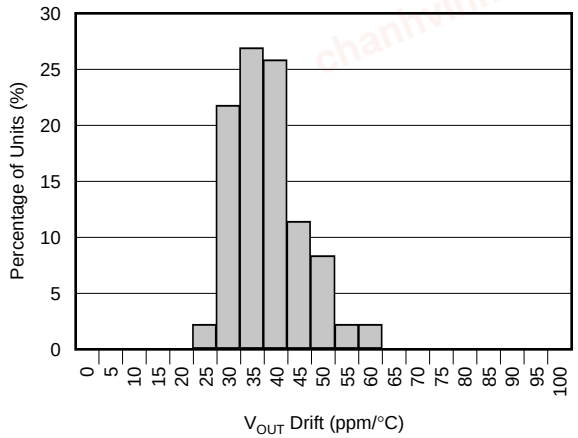
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

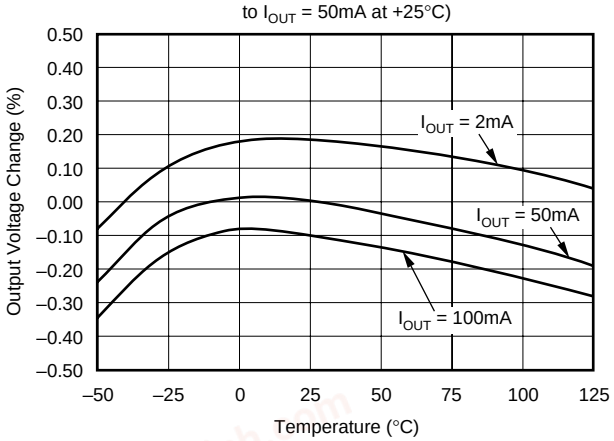
OUTPUT VOLTAGE ACCURACY HISTOGRAM



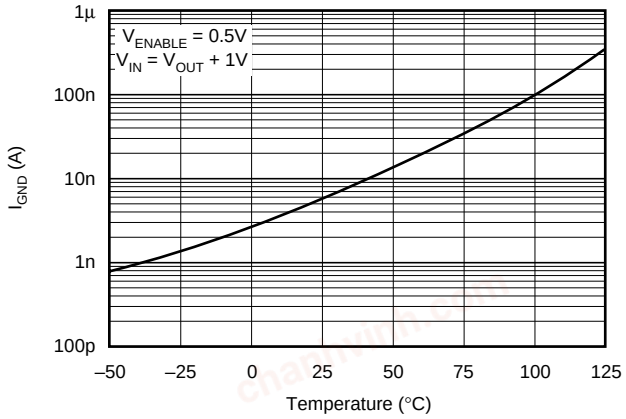
OUTPUT VOLTAGE DRIFT HISTOGRAM



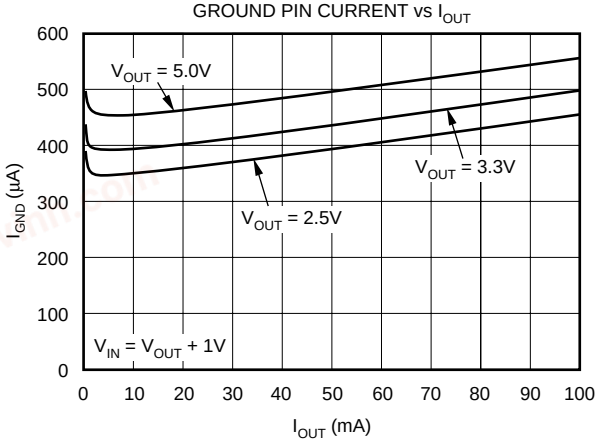
OUTPUT VOLTAGE vs TEMPERATURE
(Output Voltage % Change Referred to I_{OUT} = 50mA at +25°C)



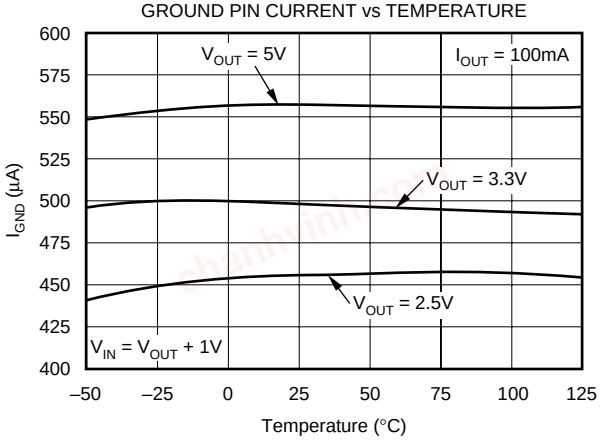
GROUND PIN CURRENT, NOT ENABLED vs TEMPERATURE



GROUND PIN CURRENT vs I_{OUT}



GROUND PIN CURRENT vs TEMPERATURE

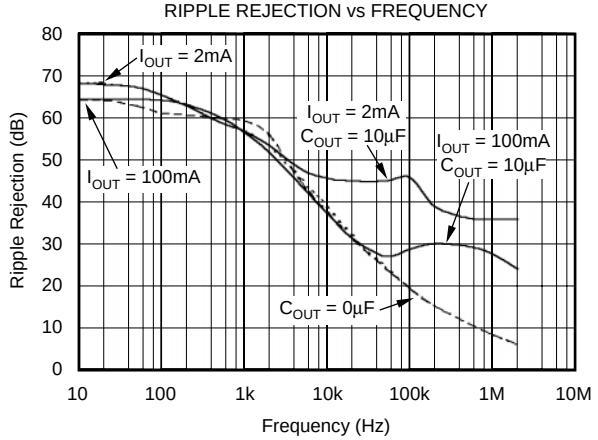


chanhvinh.com

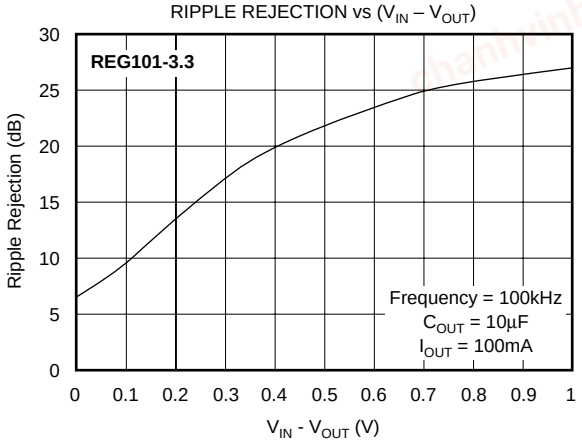
TTYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

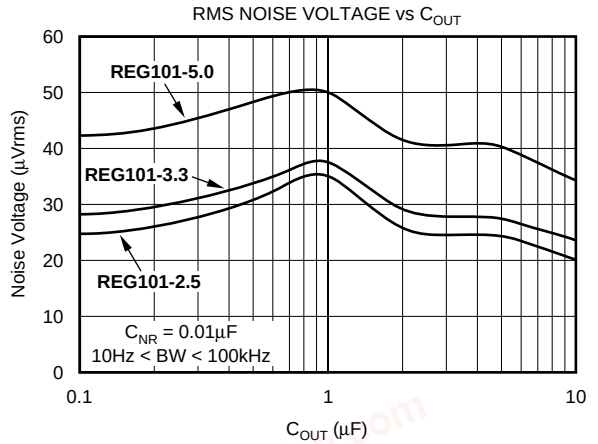
RIPPLE REJECTION vs FREQUENCY



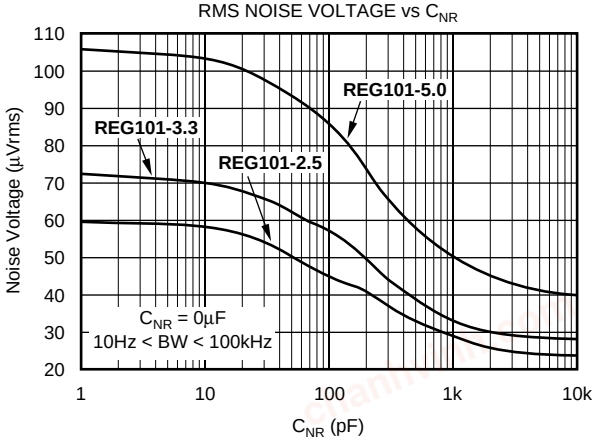
RIPPLE REJECTION vs (V_{IN} – V_{OUT})



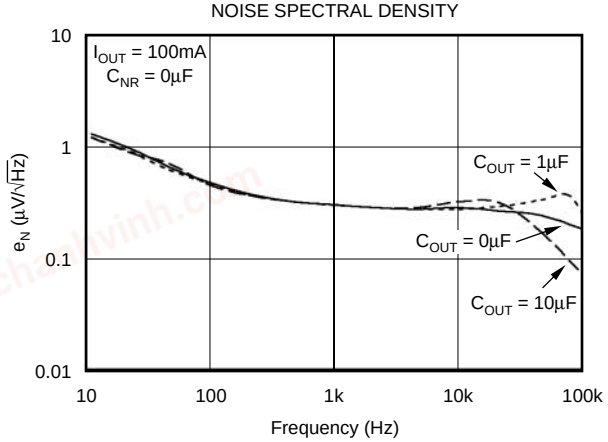
RMS NOISE VOLTAGE vs C_{OUT}



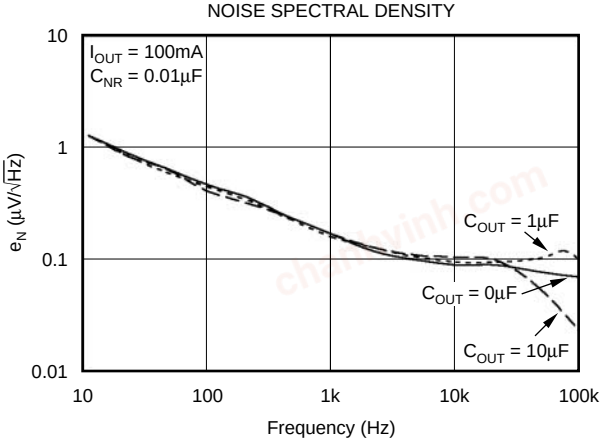
RMS NOISE VOLTAGE vs C_{NR}



NOISE SPECTRAL DENSITY



NOISE SPECTRAL DENSITY

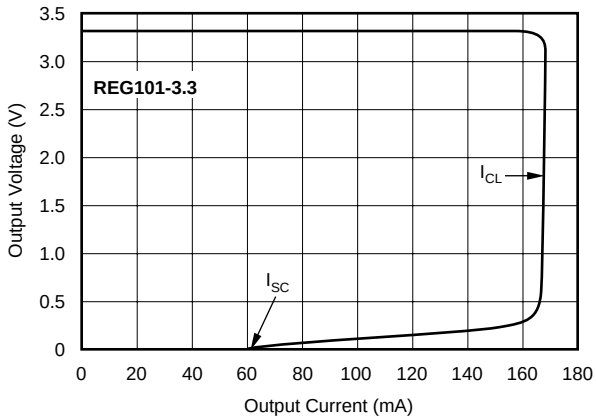


chanhvinh.com

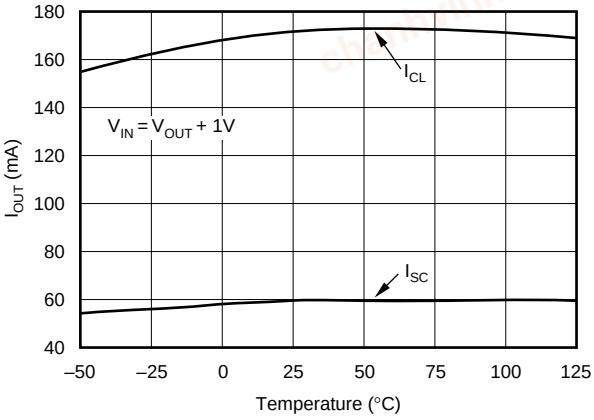
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

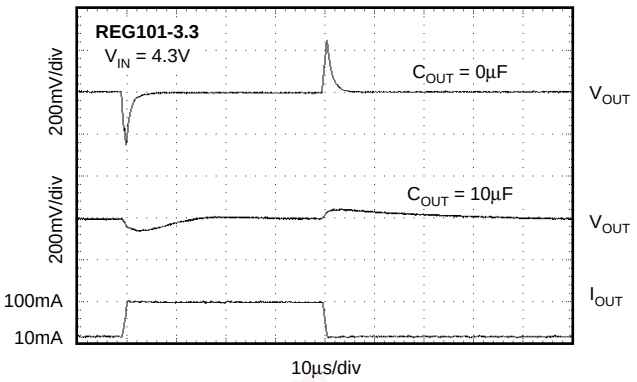
FOLDBACK CURRENT LIMIT



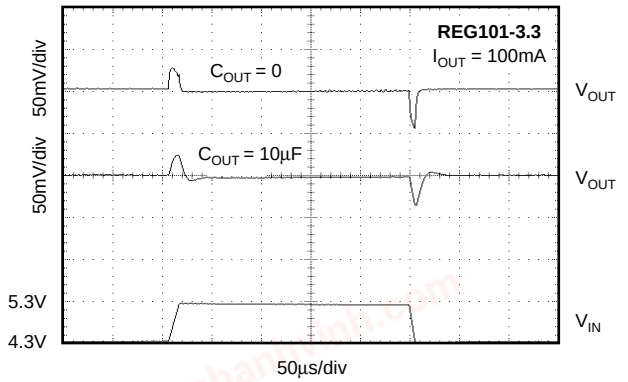
CURRENT LIMIT vs TEMPERATURE



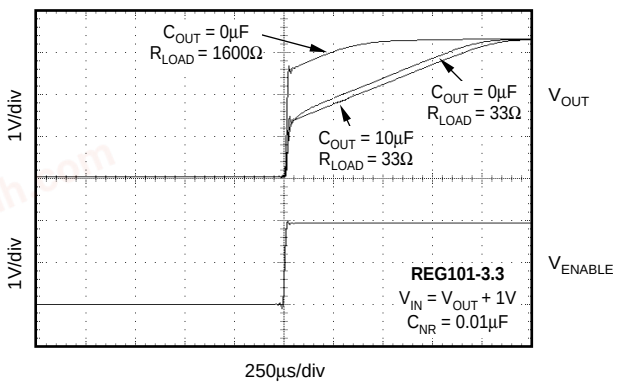
LOAD TRANSIENT RESPONSE



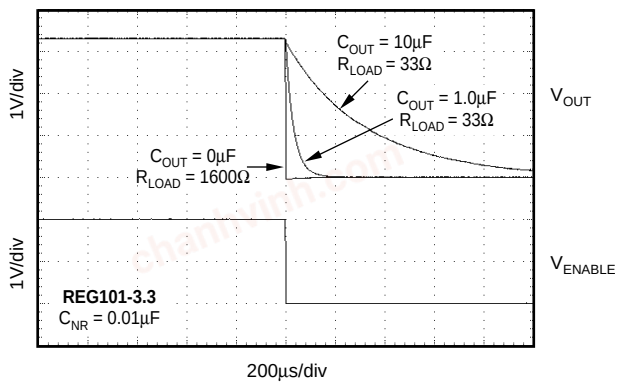
LINE TRANSIENT RESPONSE



TURN-ON



TURN-OFF

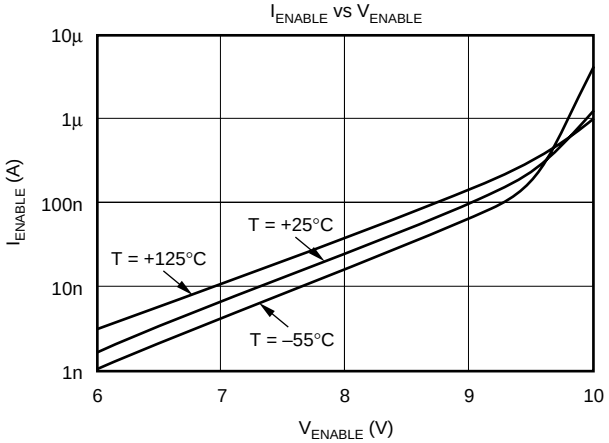


chanhvinh.com

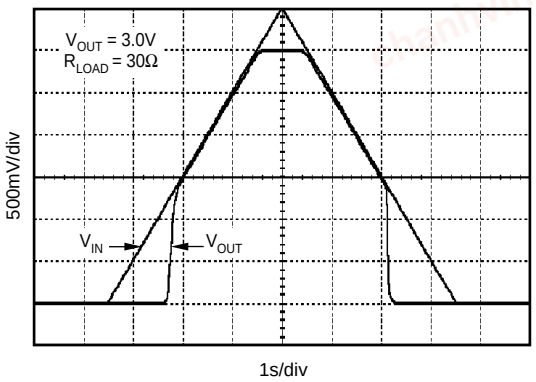
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

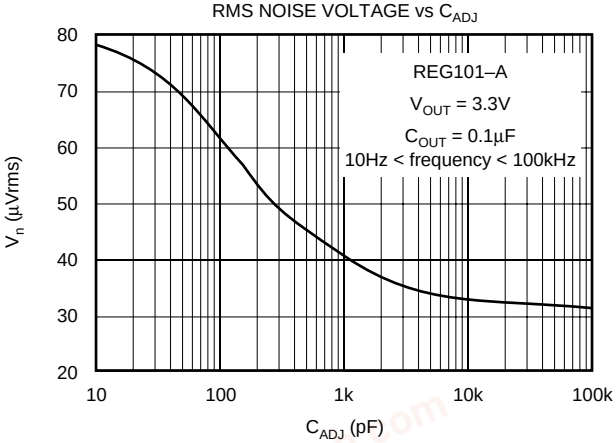
I_{ENABLE} vs V_{ENABLE}



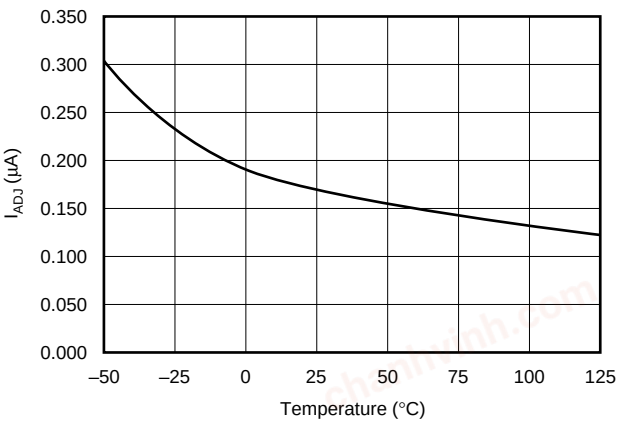
POWER UP/POWER DOWN



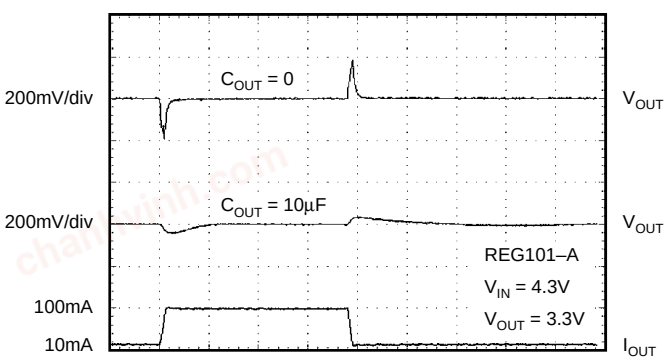
RMS NOISE VOLTAGE vs C_{ADJ}



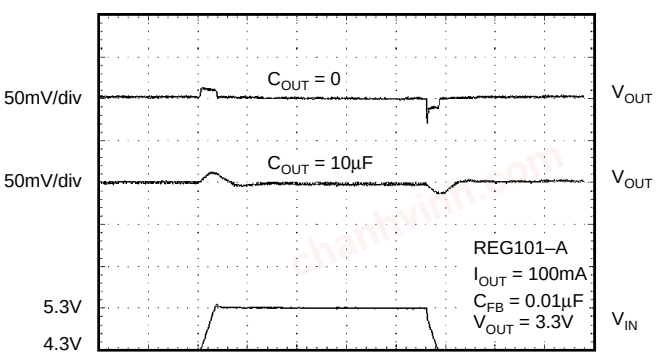
ADJUST PIN CURRENT vs TEMPERATURE



LOAD TRANSIENT-ADJUSTABLE VERSION



LINE TRANSIENT-ADJUSTABLE VERSION



chanhvinh.com

BASIC OPERATION

The REG101 series of LDO (Low Drop-Out) linear regulators offers a wide selection of fixed output voltage versions and an adjustable output version. The REG101 belongs to a family of new generation LDO regulators that utilize a DMOS pass transistor to achieve ultra-low dropout performance and freedom from output capacitor constraints. Ground pin current remains under 650µA over all line, load, and temperature conditions. All versions have thermal and overcurrent protection, including foldback current limit.

The REG101 does not require an output capacitor for regulator stability and is stable over most output currents and with almost any value and type of output capacitor up to 10µF or more. For applications where the regulator output current drops below several milliamps, stability can be enhanced by: adding a 1kΩ to 2kΩ load resistor; using capacitance values less than 10µF; or keeping the effective series resistance greater than 0.05Ω including the capacitor's ESR and parasitic resistance in printed circuit board traces, solder joints, and sockets.

Although an input capacitor is not required, it is good analog design practice to connect a 0.1µF low ESR capacitor across the input supply voltage. This is recommended to improve ripple rejection by reducing input voltage ripple.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG101A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2.

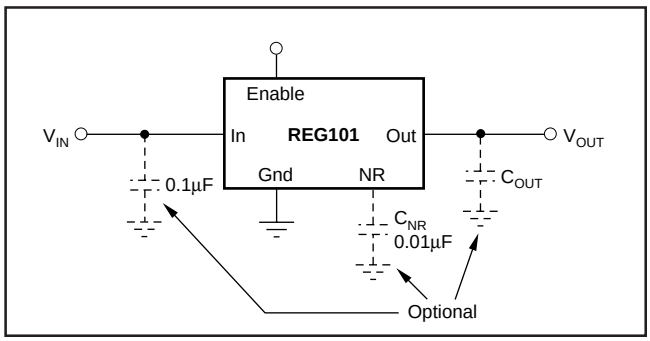


FIGURE 1. Fixed Voltage Nominal Circuit for REG101.

INTERNAL CURRENT LIMIT

The REG101 internal current limit has a typical value of 170mA. A foldback feature limits the short-circuit current to a typical short-circuit value of 60mA. This helps to protect the regulator from damage under all load conditions. A characteristic of V_{OUT} versus I_{OUT} is given in Figure 3 and in the Typical Characteristics section.

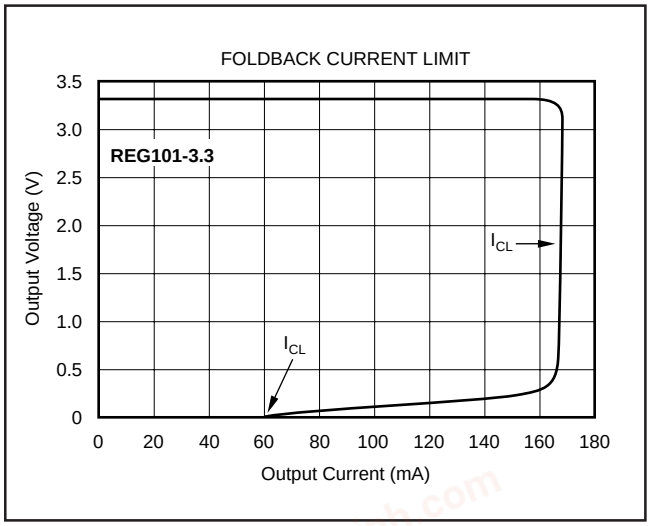
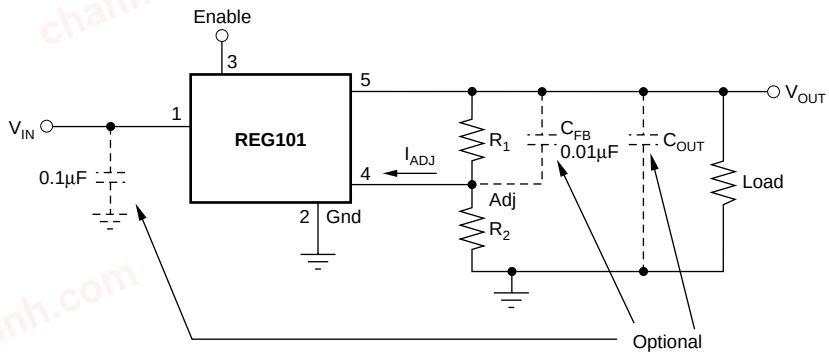


FIGURE 3. Foldback Current Limit of the REG101-3.3 at 25°C.



Pin numbers for SOT23 package.

$V_{OUT} = (1 + R_1/R_2) \cdot 1.267V$

To reduce current through divider, increase resistor values (see table at right).

As the impedance of the resistor divider increases, I_{ADJ} (~200nA) may introduce an error.

C_{FB} improves noise and transient response.

EXAMPLE RESISTOR VALUES

V_{OUT} (V)	R_1 (W)(1)	R_2 (Ω)(1)
2.5	11.3k 1.13k	11.5k 1.15k
3.0	15.8k 1.58k	11.5k 1.15k
3.3	18.7k 1.87k	11.5k 1.15k
5.0	34.0k 3.40k	11.5k 1.15k

NOTE: (1) Resistors are standard 1% values.

FIGURE 2. Adjustable Voltage Circuit for REG101A.

chanhvinh.com

ENABLE

The Enable pin is active HIGH and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 10nA. When a pull-up resistor is used, and operation down to V_{IN} = 1.8V is required, use values < 50kΩ.

OUTPUT NOISE

A precision band-gap reference is used for the internal reference voltage, V_{REF}. This reference is the dominant noise source within the REG101 and it generates approximately 29µVrms in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 29\mu Vrms \frac{R_1 + R_2}{R2} = 29\mu Vrms \bullet \frac{V_{OUT}}{V_{REF}}$$

Since the value of V_{REF} is 1.267V, this relationship reduces to:

$$V_N = 23 \frac{\mu Vrms}{V} \bullet V_{OUT}$$

Connecting a capacitor, C_{NR}, from the Noise Reduction (NR) pin to ground, as shown in Figure 4, forms a low-pass filter for the voltage reference. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 2.8 for V_O = 3.3V. This noise reduction effect is shown in Figure 5 and as "RMS Noise Voltage vs CNR" in the Typical Characteristics section.

Noise can be further reduced by carefully choosing an output capacitor, C_{OUT}. Best overall noise performance is achieved with very low (< 0.22µF) or very high (> 2.2µF) values of C_{OUT}. See "RMS Noise Voltage vs C_{OUT}" in the Typical Characteristics section.

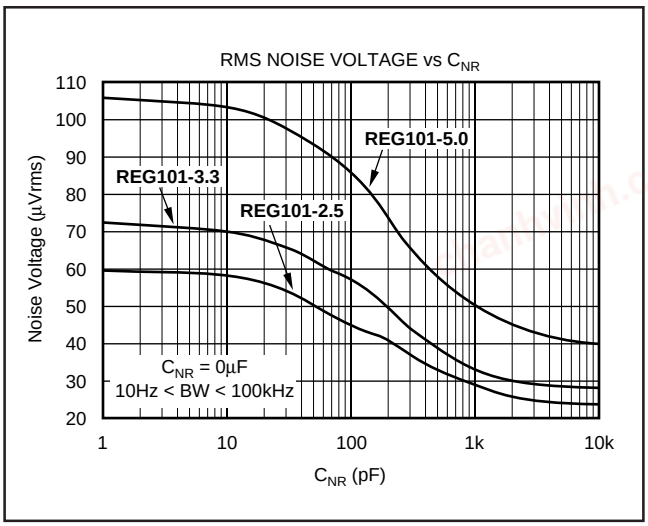


FIGURE 5. Output Noise versus Noise Reduction Capacitor.

The REG101 utilizes an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above V_{IN}. The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator over most values of C_{OUT} and I_{OUT}.

The REG101 adjustable version does not have the noise-reduction pin available, however, the adjust pin is the summing junction of the error amplifier. A capacitor, C_{FB}, connected from the output to the adjust pin will reduce both the output noise and the peak error from a load transient. See the typical characteristics for output noise performance.

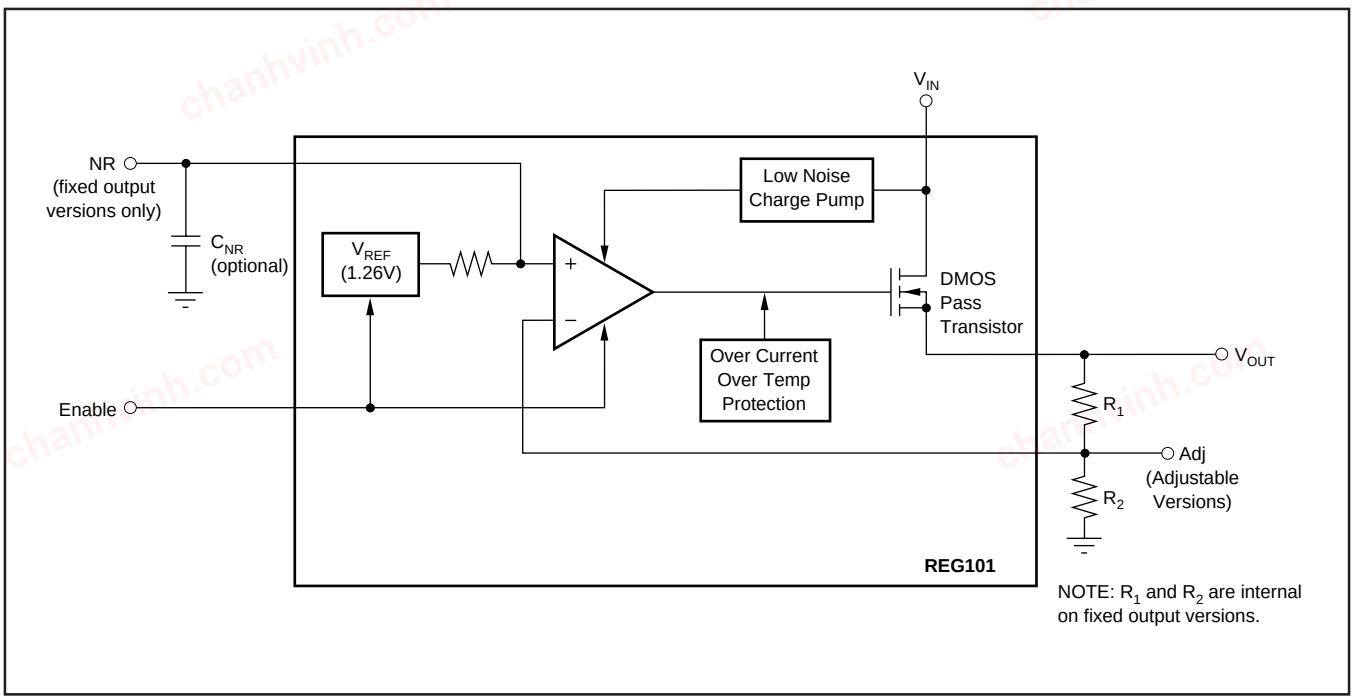


FIGURE 4. Block Diagram.

chanhvinh.com

DROP-OUT VOLTAGE

The REG101 uses an N-channel DMOS as the "pass" element. When the input voltage is within a few tens of millivolts of the output voltage, the DMOS device behaves like a resistor. Therefore, for low values of V_{IN} to V_{OUT}, the regulator's input-to-output resistance is the Rds_{ON} of the DMOS pass element (typically 600mΩ). For static (DC) loads, the REG101 will typically maintain regulation down to V_{IN} to V_{OUT} voltage drop of 60mV at full rated output current. In Figure 6, the bottom line (DC dropout) shows the minimum V_{IN} to V_{OUT} voltage drop required to prevent drop-out under DC load conditions.

For large step changes in load current, the REG101 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this "transient drop-out" region is shown as the top line in Figure 6. Values of V_{IN} to V_{OUT} voltage drop above this line insure normal transient response.

In the transient dropout region between "DC" and "Transient", transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available "headroom" V_{IN} to V_{OUT} voltage drop. Under worst-case conditions (full-scale load change with V_{IN} to V_{OUT} voltage drop close to DC dropout levels), the REG101 can take several hundred microseconds to re-enter the specified window of regulation.

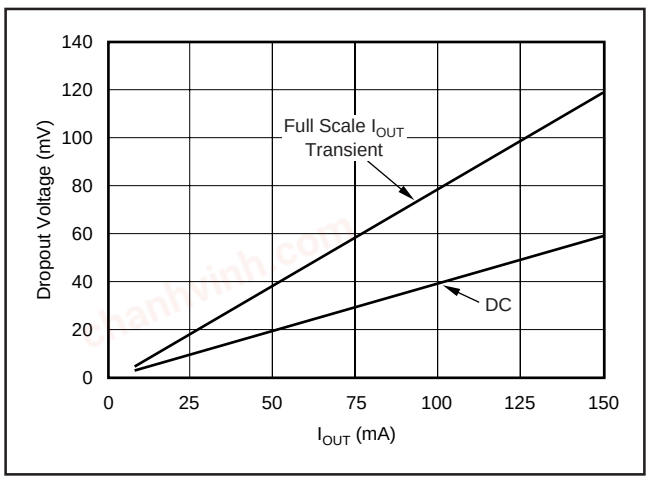


FIGURE 6. Transient and DC Dropout.

TRANSIENT RESPONSE

The REG101 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 0.47µF) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor, C_{FB} (nominal value 10nF), from the output to the adjust pin will also improve the transient response.

THERMAL PROTECTION

The REG101 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG101 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the REG101 into thermal shutdown will degrade reliability.

chanhvinh.com

POWER DISSIPATION

The REG101 is available in two different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. While it is difficult to impossible to quantify all of the variables in a thermal design of this type, performance data for several configurations are shown in Figure 7.

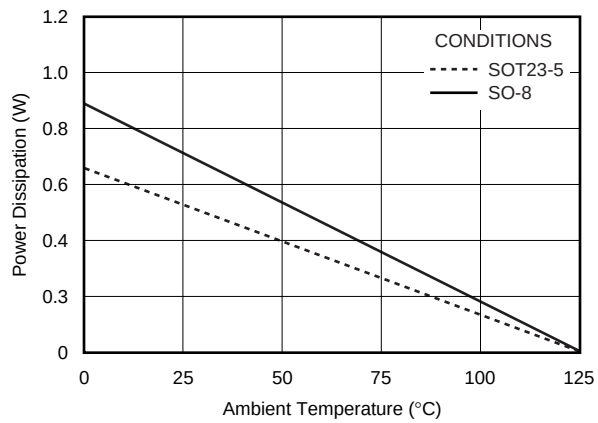
Power dissipation depends on input voltage, load condition, and duty cycle. Power dissipation is equal to the product of the average output current times the voltage across the output element, V_{IN} to V_{OUT} voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \bullet I_{OUT(AVG)}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

REGULATOR MOUNTING

Solder pad footprint recommendations for the various REG101 devices are presented in the Application Bulletin AB-132, “Solder Pad Recommendations for Surface-Mount Devices” (SBFA015), available from the Texas Instruments web site (www.ti.com).



PACKAGE	θ_{JA}
SOT23-5	200°C/W
SO-8	150°C/W

FIGURE 7. Maximum Power Dissipation versus Ambient Temperature for the Various Packages.

chanhvinh.com

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REG101NA-2.5/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1G
REG101NA-2.5/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1G
REG101NA-2.5/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1G
REG101NA-2.5/3K.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1G
REG101NA-2.8/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1E
REG101NA-2.8/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1E
REG101NA-2.85/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1N
REG101NA-2.85/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1N
REG101NA-2.85/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1N
REG101NA-2.85/3K.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1N
REG101NA-3.3/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C
REG101NA-3.3/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C
REG101NA-3.3/250G4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C
REG101NA-3.3/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C
REG101NA-3.3/3K.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C
REG101NA-3.3/3KG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C
REG101NA-3/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R01D
REG101NA-3/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R01D
REG101NA-3/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R01D
REG101NA-3/3K.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R01D
REG101NA-5/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1B
REG101NA-5/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1B
REG101NA-5/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1B
REG101NA-5/3K.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1B
REG101NA-A/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A
REG101NA-A/250.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A
REG101NA-A/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A
REG101NA-A/3K	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A
REG101NA-A/3K.A	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A

chanhvinh.com

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REG101NA-A/3K.B	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A
REG101NA-A/3KG4	NRND	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A
REG101UA-2.5	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U25
REG101UA-2.5.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U25
REG101UA-3	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U30
REG101UA-3.3	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U33
REG101UA-3.3.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U33
REG101UA-3.3/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U33
REG101UA-3.3/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U33
REG101UA-3.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U30
REG101UA-5	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U50
REG101UA-5.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U50
REG101UA-5/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U50
REG101UA-5/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U50
REG101UA-A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101UA
REG101UA-A.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101UA
REG101UA-A.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101UA

(1) **Status:** For more details on status, see our product life cycle.

chanhvinh.com

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

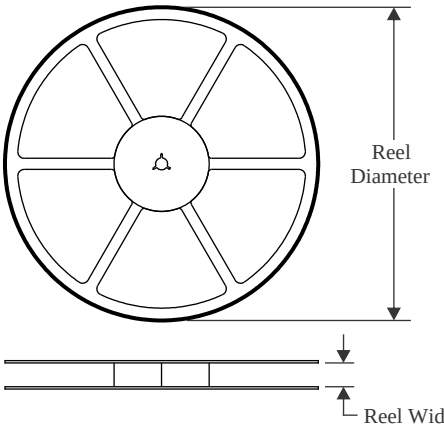
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

chanhvinh.com

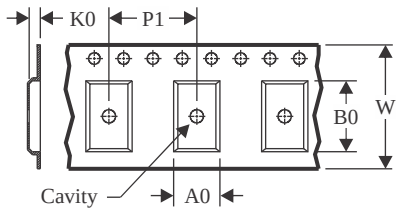
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

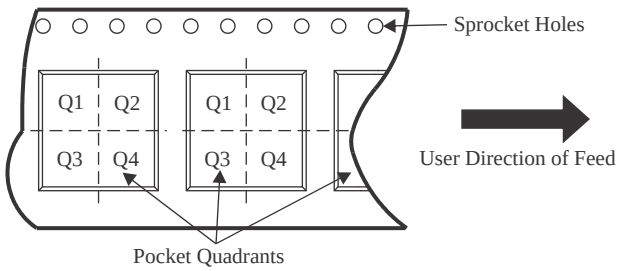


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



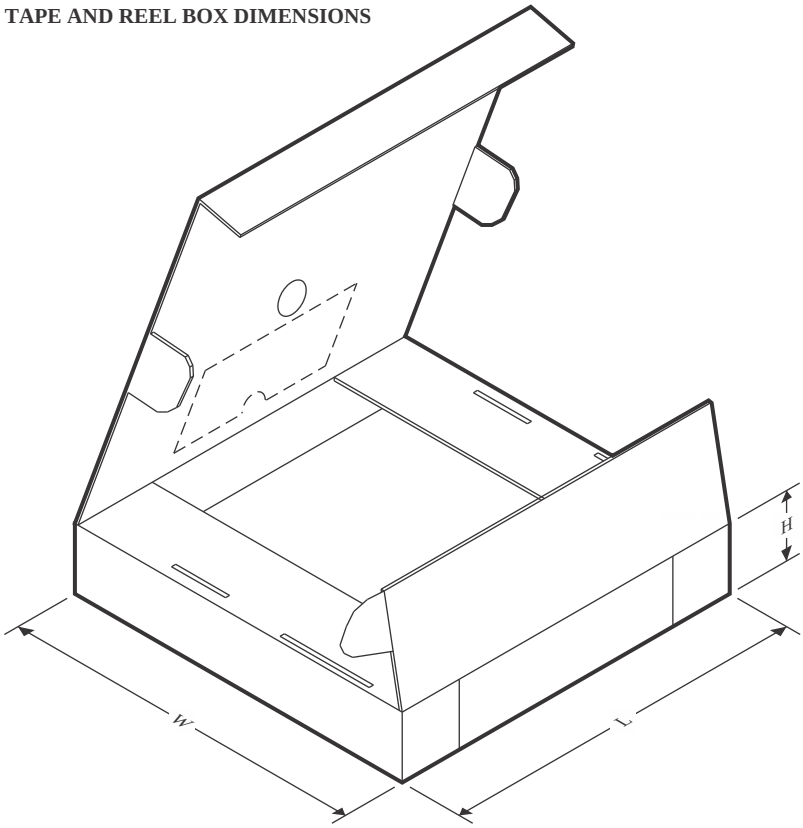
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG101NA-2.5/250	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG101NA-2.5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-2.5/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-2.8/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-2.85/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-2.85/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-3.3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-3.3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-5/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-A/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-A/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101UA-3.3/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REG101UA-5/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

chanhvinh.com

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

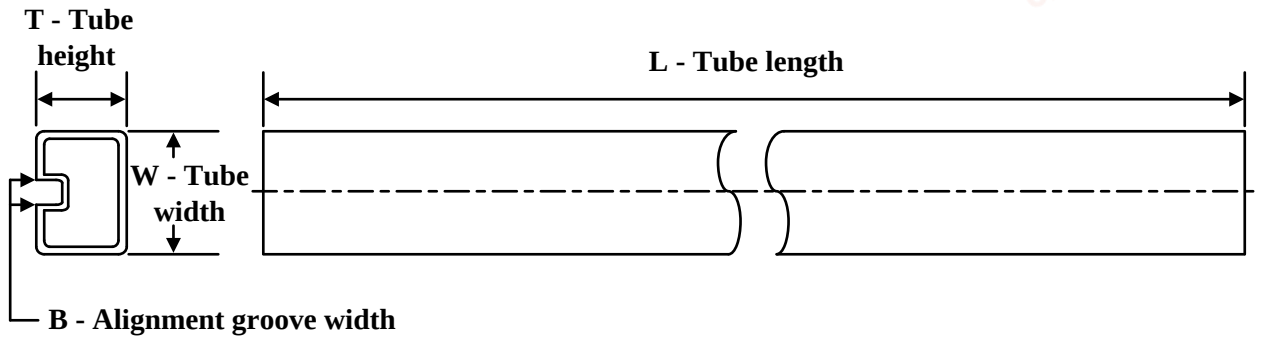


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG101NA-2.5/250	SOT-23	DBV	5	250	180.0	180.0	18.0
REG101NA-2.5/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG101NA-2.5/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG101NA-2.8/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG101NA-2.85/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG101NA-2.85/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG101NA-3.3/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG101NA-3.3/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG101NA-3/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG101NA-3/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG101NA-5/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG101NA-5/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG101NA-A/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG101NA-A/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG101UA-3.3/2K5	SOIC	D	8	2500	353.0	353.0	32.0
REG101UA-5/2K5	SOIC	D	8	2500	353.0	353.0	32.0

chanhvinh.com

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
REG101UA-2.5	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-2.5.B	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-3	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-3.3	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-3.3.B	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-3.B	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-5	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-5.B	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-A	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-A.A	D	SOIC	8	75	506.6	8	3940	4.32
REG101UA-A.B	D	SOIC	8	75	506.6	8	3940	4.32

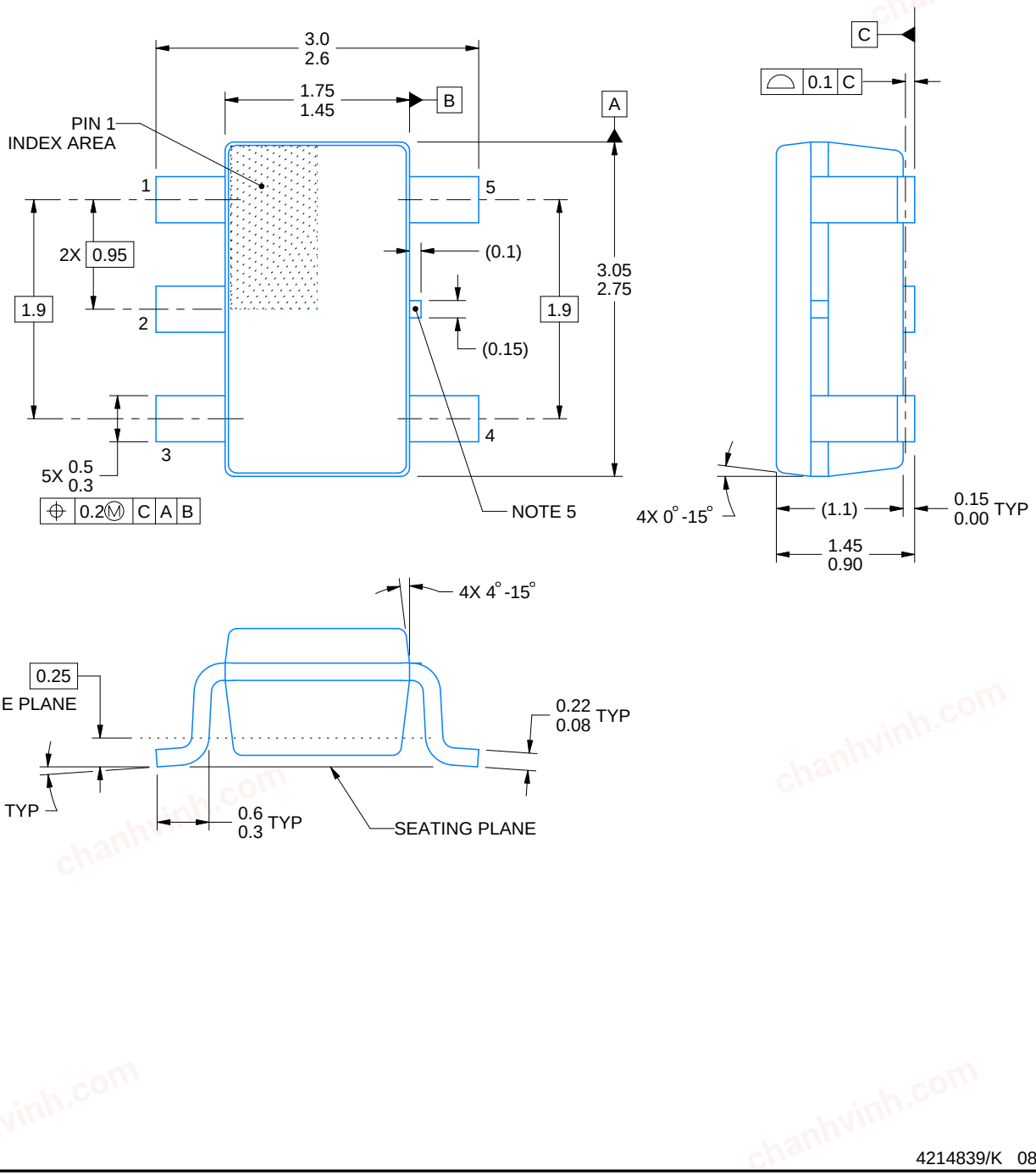
chanhvinh.com

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

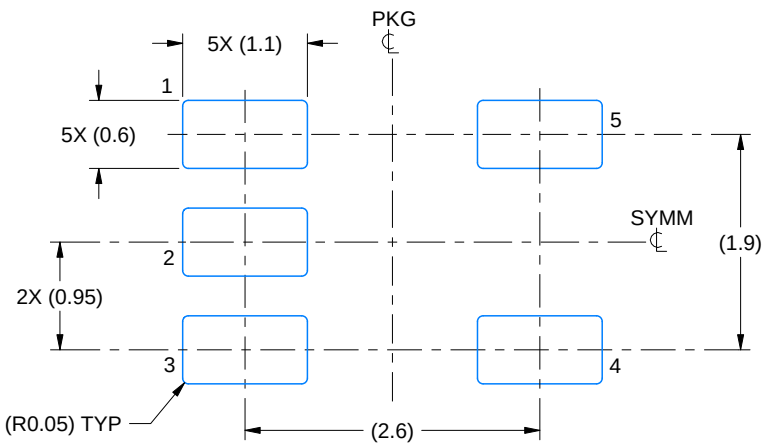
chanhvinh.com

EXAMPLE BOARD LAYOUT

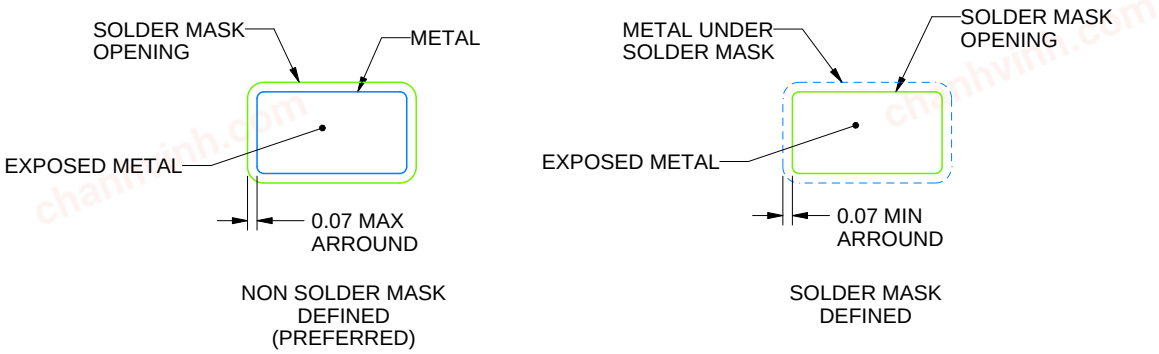
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

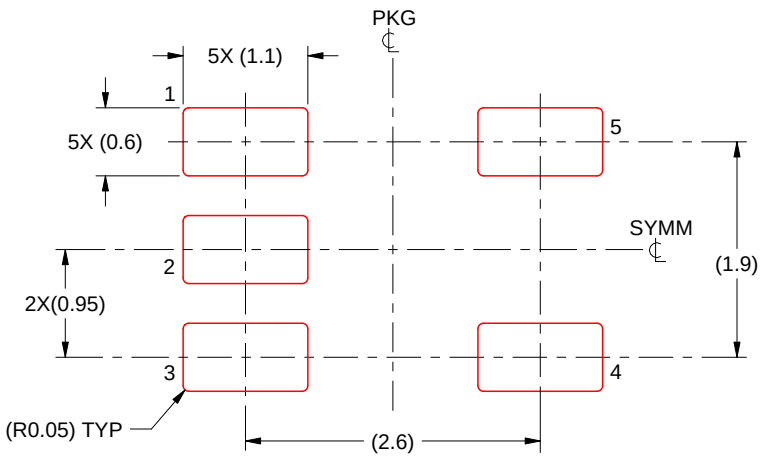
chanhvinh.com

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



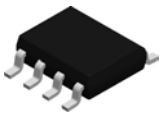
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

chanhvinh.com

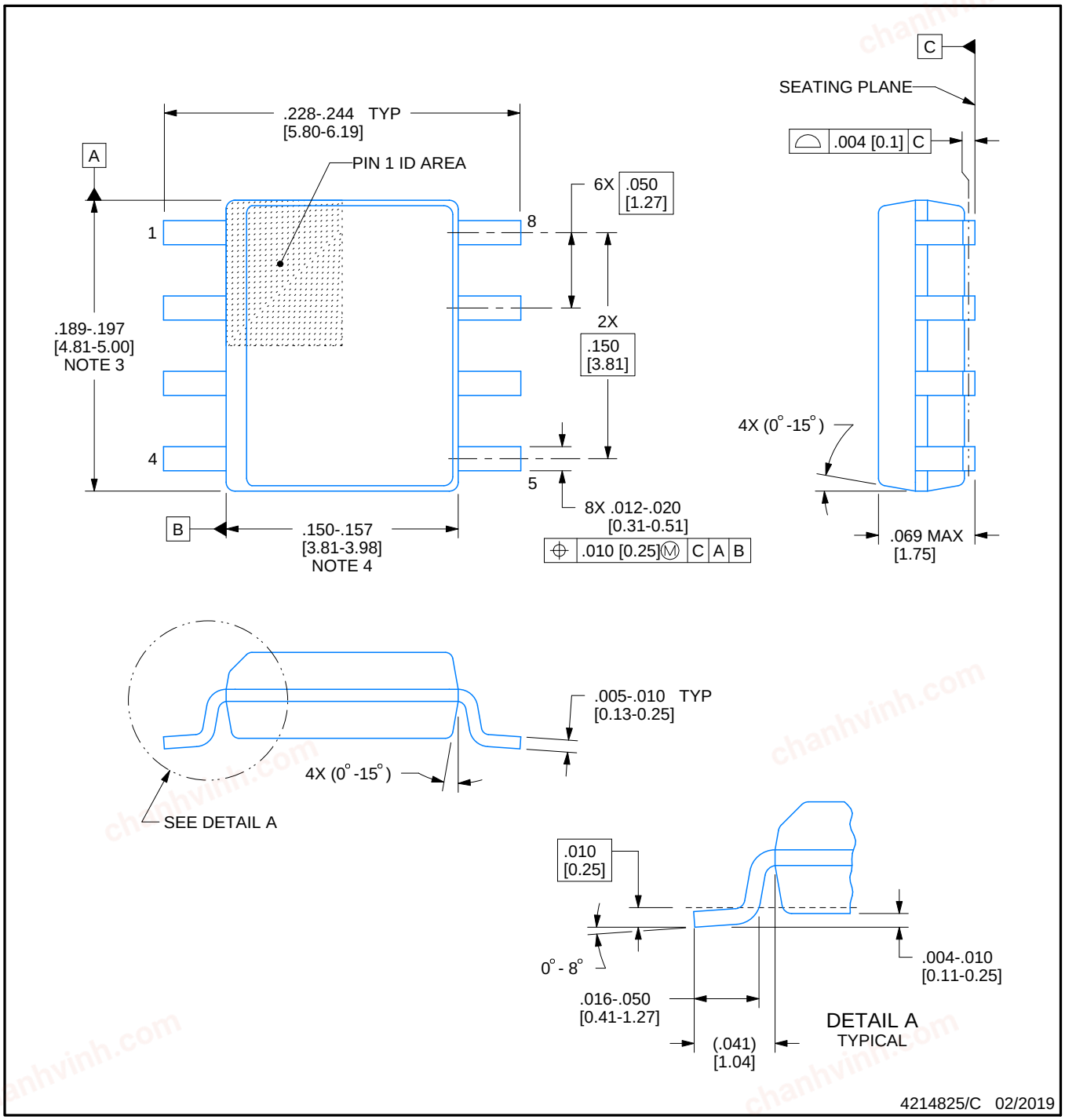


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

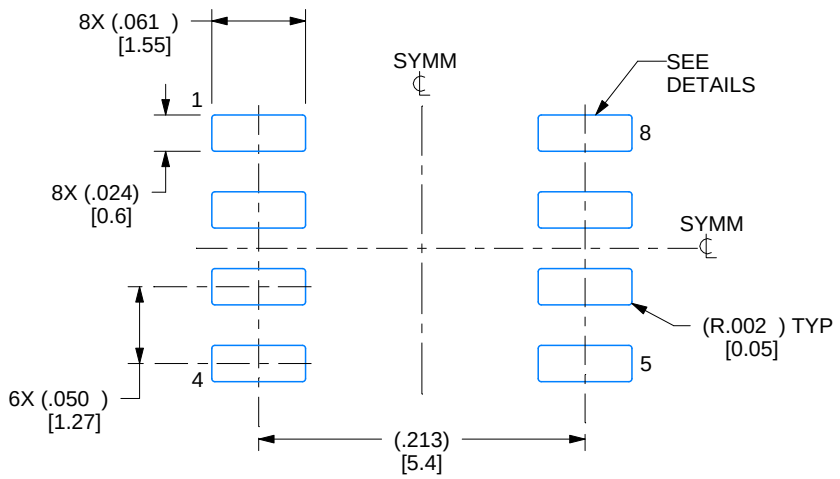
chanhvinh.com

EXAMPLE BOARD LAYOUT

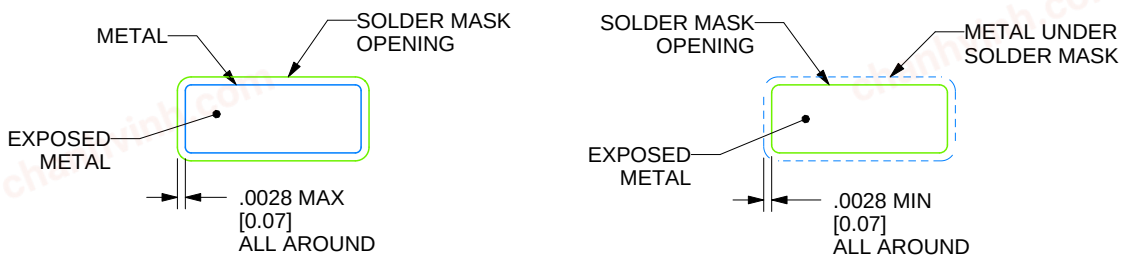
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

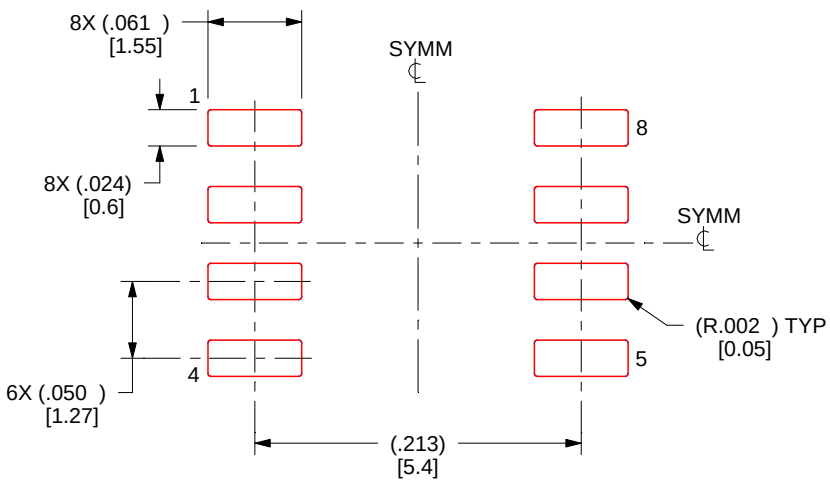
chanhvinh.com

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

chanhvinh.com

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025