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INA301 36-V, High-Speed, Zero-Drift, Voltage-Output, Current-Shunt Monitor with High-Speed, Overcurrent Comparator

1 Features

- Wide Common-Mode Input Range: 0 V to 36 V
- Dual Output: Amplifier and Comparator Output
- High Accuracy Amplifier:
  - Offset Voltage: 35 µV (Max)
  - Offset Voltage Drift: 0.5 µV/°C (Max)
  - Gain Error: 0.1% (Max)
  - Gain Error Drift: 10 ppm/°C
- Available Amplifier Gains:
  - INA301A1: 20 V/V
  - INA301A2: 50 V/V
  - INA301A3: 100 V/V
- Programmable Alert Threshold Set Through a Single Resistor
- Total Alert Response Time: 1 µs
- Open-Drain Output With Latching Mode
- Package: VSSOP-8

2 Applications

- Overcurrent Protection
- Power-Supply Protection
- Circuit Breakers
- Computers and Servers
- Telecom Equipment
- Battery Management

3 Description

The INA301 includes both a high common-mode, current-sensing amplifier and a high-speed comparator configured to detect overcurrent conditions through measuring the voltage developed across a current-sensing or current-shunt resistor and comparing that voltage to a defined threshold limit. The device features an adjustable limit threshold range that is set using a single external limit-setting resistor. This current-shunt monitor can measure differential voltage signals on common-mode voltages that can vary from 0 V up to 36 V, independent of the supply voltage.

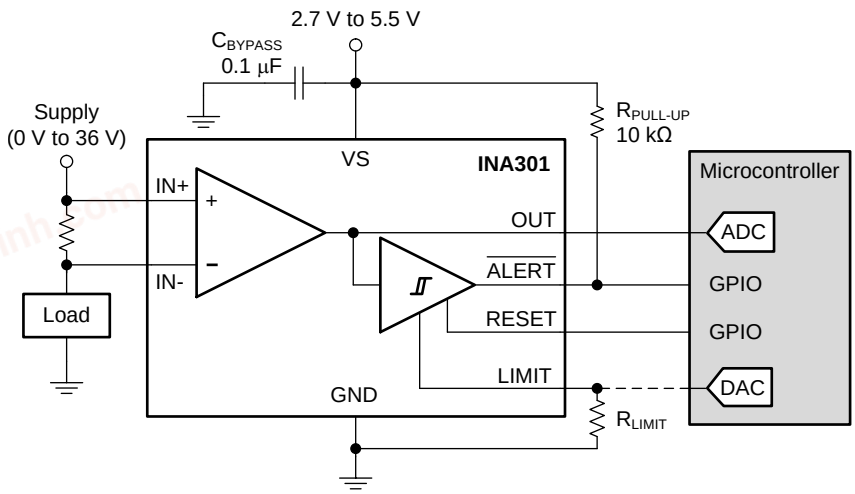
The open-drain alert output can be configured to operate in either a transparent mode where the output status follows the input state or in a latched mode where the alert output is cleared when the latch is reset. The device alert response time is under 1 µs, allowing for quick detection of overcurrent events.

This device operates from a single 2.7-V to 5.5-V supply, drawing a maximum supply current of 700 µA. The device is specified over the extended operating temperature range (–40°C to +125°C), and is available in an 8-pin VSSOP package.

Device Information

PART NUMBER	PACKAGE	BODY SIZE
INA301	VSSOP (8)	3.00 mm × 3.00 mm

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

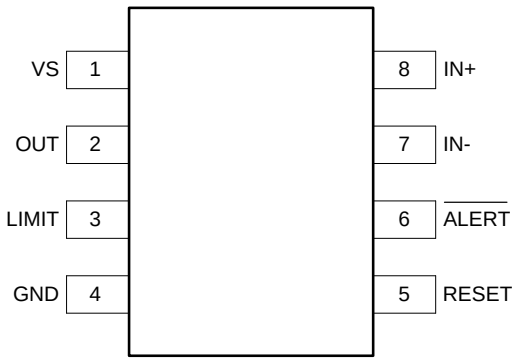
Changes from Original (September 2015) to Revision A	Page
• Released to production	1

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5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VS	Analog	Power supply, 2.7 V to 5.5 V
2	OUT	Analog output	Output voltage
3	LIMIT	Analog input	Alert threshold limit input; see the *Setting The Current-Limit Threshold* section for details on setting the limit threshold
4	GND	Analog	Ground
5	RESET	Digital input	Transparent or latch mode selection input
6	$\overline{\text{ALERT}}$	Digital output	Overlimit alert, active-low, open-drain output
7	IN–	Analog input	Connect to load side of the shunt resistor
8	IN+	Analog input	Connect to supply side of the shunt resistor

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs (IN+, IN–)	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–40	40	V
	Common-mode(3)	GND – 0.3	40	
Analog input	LIMIT pin	GND – 0.3	(V_S) + 0.3	V
Analog output	OUT pin	GND – 0.3	(V_S) + 0.3	V
Digital input	RESET pin	GND – 0.3	(V_S) + 0.3	V
Digital output	$\overline{\text{ALERT}}$ pin	GND – 0.3	6	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage can exceed the voltage shown without causing damage to the device if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage		5		V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA301 DGK (MSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	161.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

at T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 10 mV, V_S = 5 V, V_{IN+} = 12 V, and V_{LIMIT} = 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input voltage range		0		36	V
V_{IN}	Differential input voltage range	V_{IN} = V_{IN+} – $V_{IN–}$, INA301A1	0		250	mV
		V_{IN} = V_{IN+} – $V_{IN–}$, INA301A2	0		100	
		V_{IN} = V_{IN+} – $V_{IN–}$, INA301A3	0		50	
CMR	Common-mode rejection	INA301A1, V_{IN+} = 0 V to 36 V, T_A = –40ºC to +125ºC	100	110		dB
		INA301A2, V_{IN+} = 0 V to 36 V, T_A = –40ºC to +125ºC	106	118		
		INA301A3, V_{IN+} = 0 V to 36 V, T_A = –40ºC to +125ºC	110	120		
V_{OS}	Offset voltage, RTI(1)	INA301A1		±25	±125	µV
		INA301A2		±15	±50	
		INA301A3		±10	±35	
dV_{OS}/dT	Offset voltage drift, RTI(1)	T_A= –40ºC to +125ºC		0.1	0.5	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, V_{IN+} = 12 V, T_A = –40ºC to +125ºC		±0.1	±10	µV/V
I_B	Input bias current	I_{B+}, $I_{B–}$		120		µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV		±0.1		µA
OUTPUT						
G	Gain	INA301A1		20		V/V
		INA301A2		50		
		INA301A3		100		
	Gain error	INA301A1, V_{OUT} = 0.5 V to V_S – 0.5 V		±0.03%	±0.1%	
		INA301A2, V_{OUT} = 0.5 V to V_S – 0.5 V		±0.05%	±0.15%	
		INA301A3, V_{OUT} = 0.5 V to V_S – 0.5 V		±0.11%	±0.2%	
		T_A= –40ºC to 125ºC		3	10	ppm/°C
	Nonlinearity error	V_{OUT} = 0.5 V to V_S – 0.5 V		±0.01%		
	Maximum capacitive load	No sustained oscillation		500		pF
VOLTAGE OUTPUT						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND, T_A = –40ºC to +125ºC		V_S – 0.05	V_S – 0.1	V
	Swing to GND	R_L = 10 kΩ to GND, T_A = –40ºC to +125ºC		V_{GND} + 20	V_{GND} + 30	mV
FREQUENCY RESPONSE						
BW	Bandwidth	INA301A1		550		kHz
		INA301A2		500		
		INA301A3		450		
SR	Slew rate			4		V/µs
NOISE, RTI(1)						
	Voltage noise density			30		nV/√Hz

(1) RTI = referred-to-input.

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Electrical Characteristics (continued)

at T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 10 mV, V_S = 5 V, V_{IN+} = 12 V, and V_{LIMIT} = 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMPARATOR						
t_p	Total alert propagation delay	Input overdrive = 1 mV		0.75	1	µs
	Slew-rate-limited t_p	V_{OUT} step = 0.5 V to 4.5 V, V_{LIMIT} = 4 V		1	1.5	
I_{LIMIT}	Limit threshold output current	T_A = 25ºC	79.7	80	80.3	µA
		T_A = –40ºC to +125ºC	79.2		80.8	
V_{OS}	Comparator offset voltage	INA301A1		1	3.5	mV
		INA301A2		1	4	
		INA301A3		1.5	4.5	
HYS	Hysteresis	INA301A1		20		mV
		INA301A2		50		
		INA301A3		100		
V_{IH}	High-level input voltage		1.4		6	V
V_{IL}	Low-level input voltage		0		0.4	V
V_{OL}	Alert low-level output voltage	I_{OL} = 3 mA		70	300	mV
	$\overline{\text{ALERT}}$ pin leakage input current	V_{OH} = 3.3 V		0.1	1	µA
	Digital leakage input current	0 ≤ V_{IN} ≤ V_S		1		µA
POWER SUPPLY						
V_S	Operating supply range	T_A = –40ºC to +125ºC	2.7		5.5	V
I_Q	Quiescent current	V_{SENSE} = 0 mV, T_A = 25ºC		500	650	µA
		T_A = –40ºC to +125ºC			700	
TEMPERATURE RANGE						
	Specified range		–40		125	°C

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6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

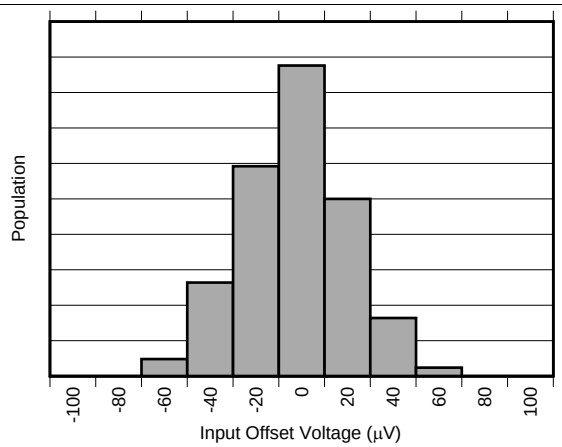


Figure 1. Input Offset Voltage Distribution (INA301A1)

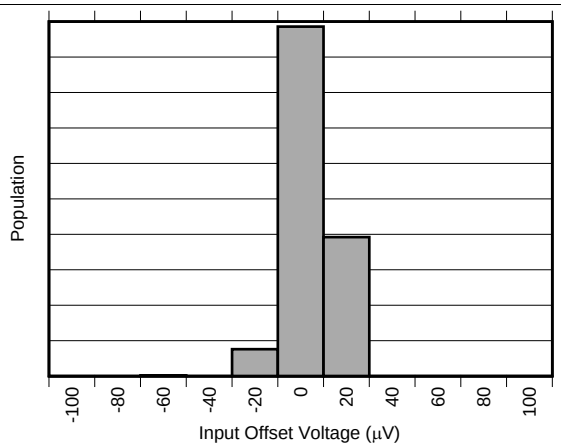


Figure 2. Input Offset Voltage Distribution (INA301A2)

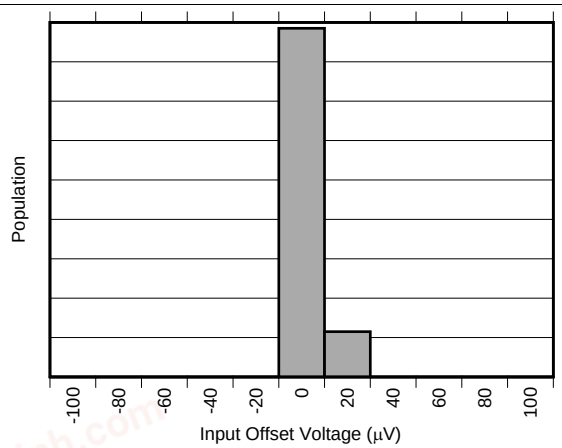


Figure 3. Input Offset Voltage Distribution (INA301A3)

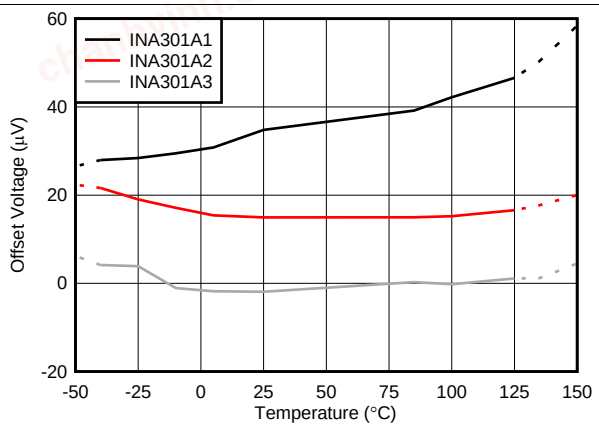


Figure 4. Input Offset Voltage vs Temperature

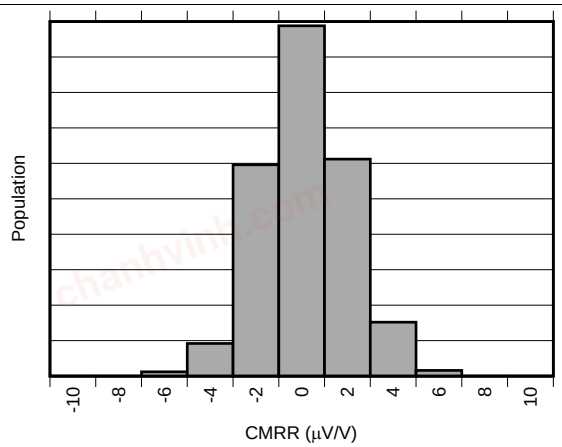


Figure 5. Common-Mode Rejection Ratio Distribution (INA301A1)

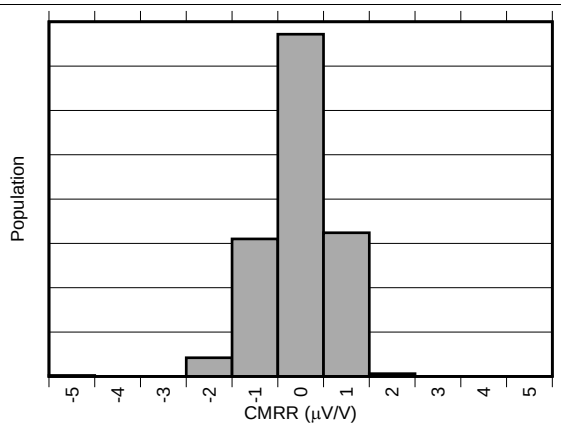


Figure 6. Common-Mode Rejection Ratio Distribution (INA301A2)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

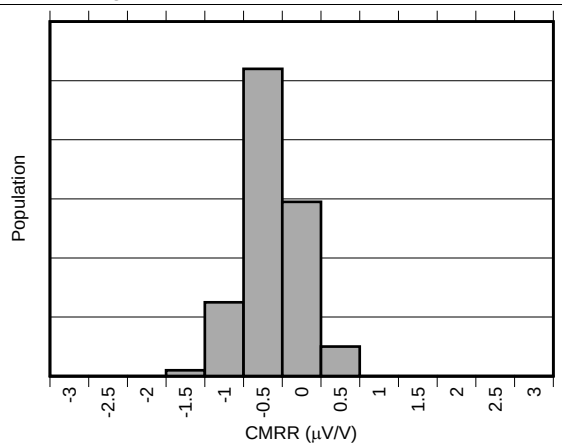


Figure 7. Common-Mode Rejection Ratio Distribution (INA301A3)

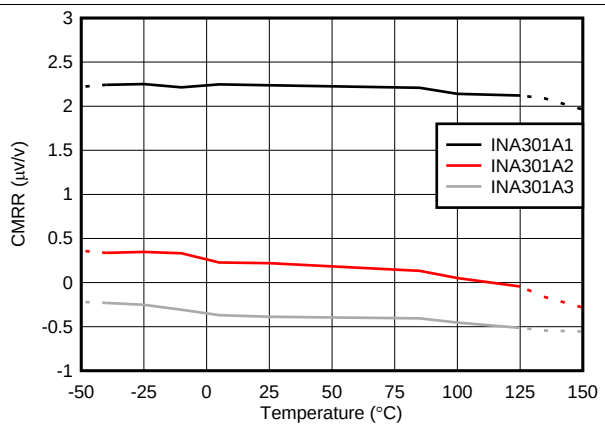


Figure 8. Common-Mode Rejection Ratio vs Temperature

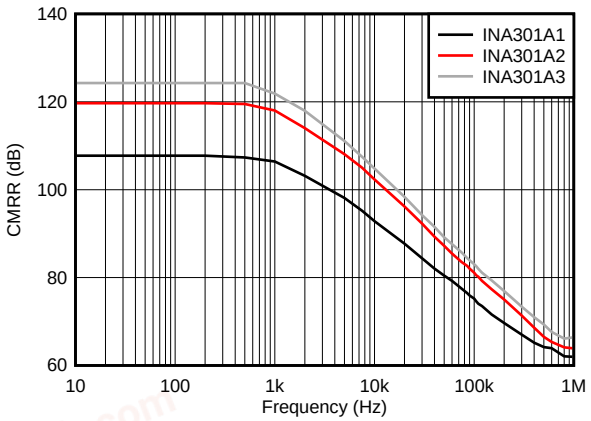


Figure 9. Common-Mode Rejection Ratio vs Frequency

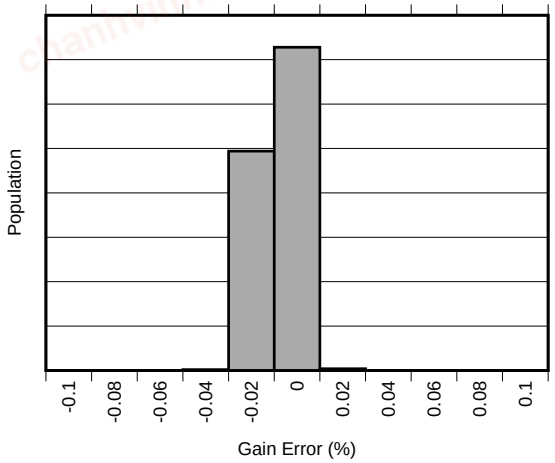


Figure 10. Gain Error Distribution (INA301A1)

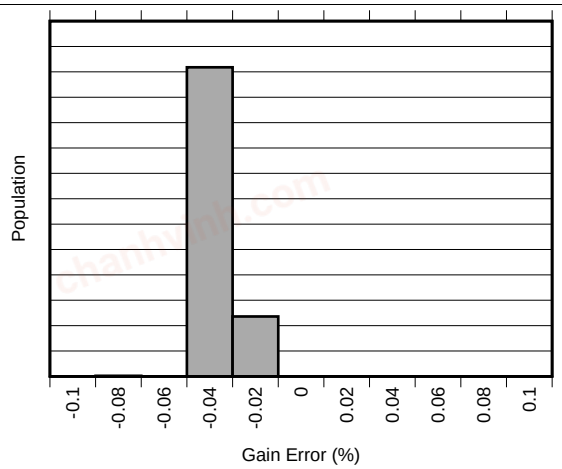


Figure 11. Gain Error Distribution (INA301A2)

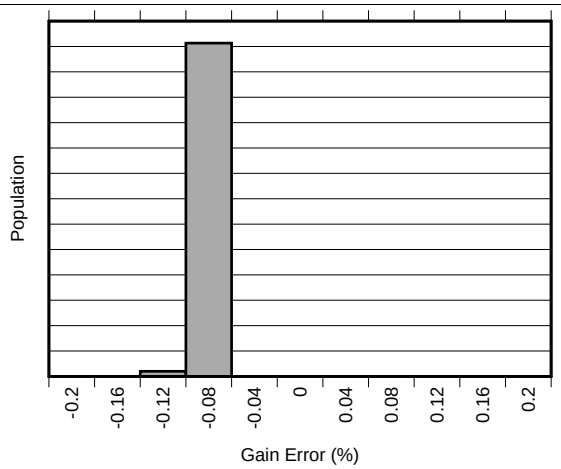


Figure 12. Gain Error Distribution (INA301A3)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

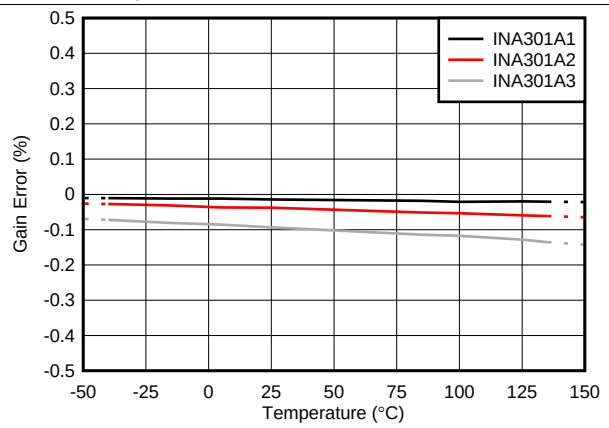


Figure 13. Gain Error vs Temperature

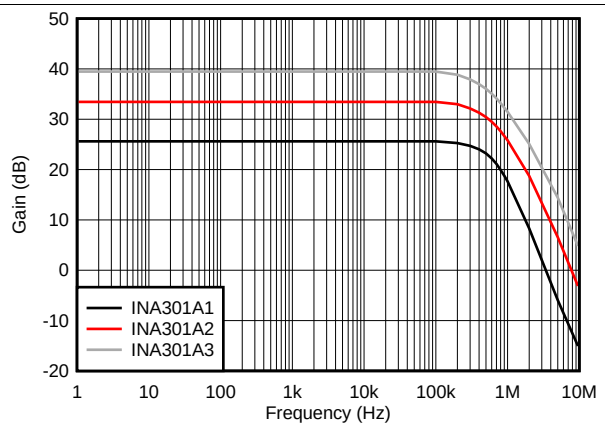


Figure 14. Gain vs Frequency

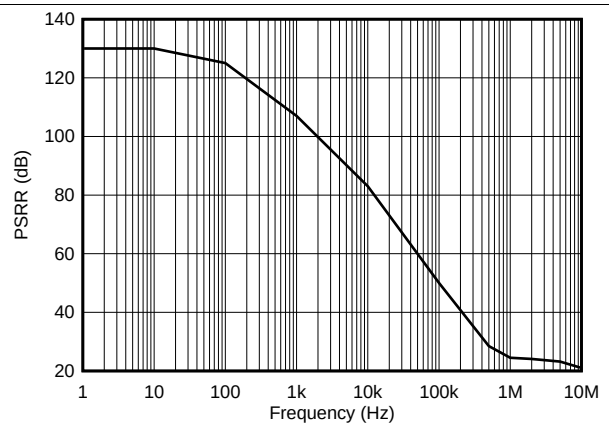


Figure 15. Power-Supply Rejection Ratio vs Frequency

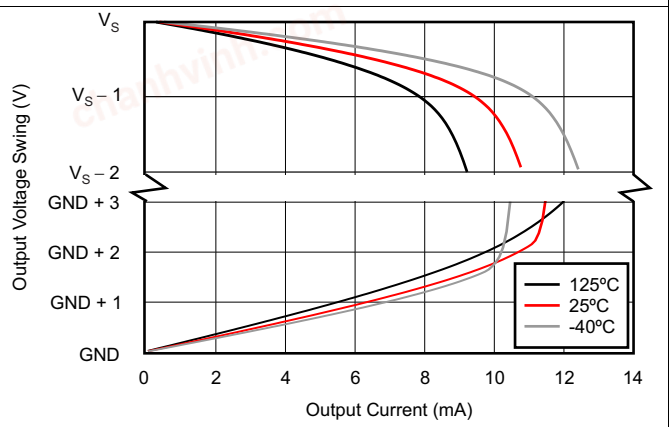


Figure 16. Output Voltage Swing vs Output Current

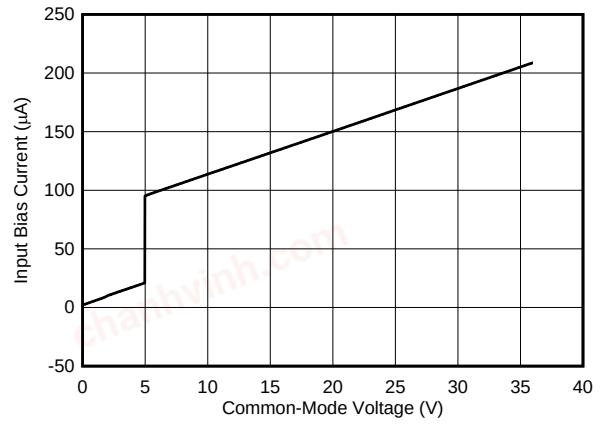


Figure 17. Input Bias Current vs Common-Mode Voltage (V_S = 5 V)

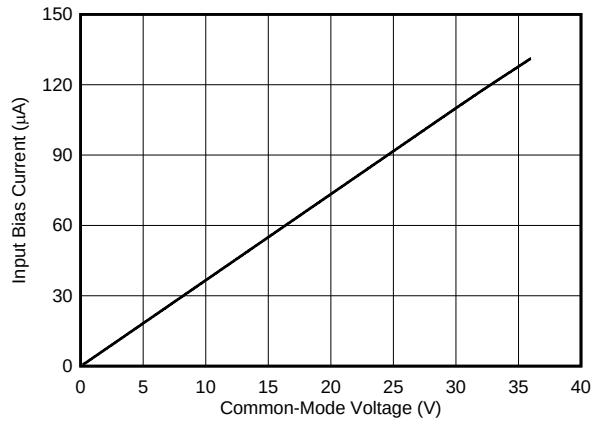


Figure 18. Input Bias Current vs Common-Mode Voltage (V_S = 0 V)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

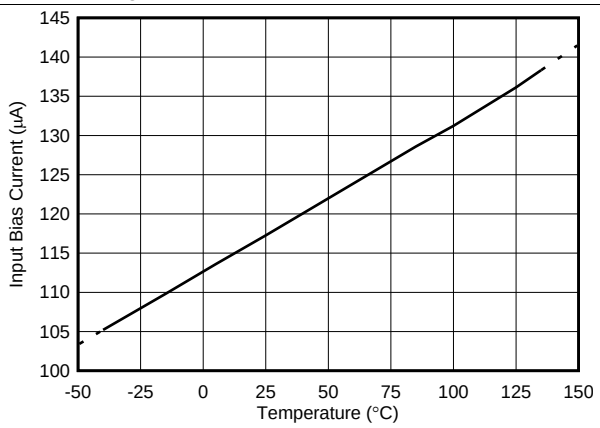


Figure 19. Input Bias Current vs Temperature

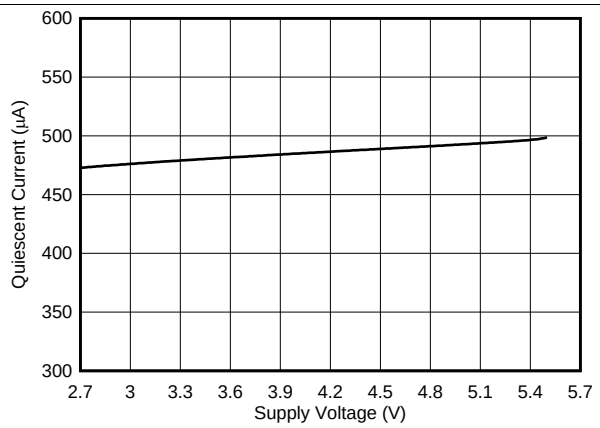


Figure 20. Quiescent Current vs Supply Voltage

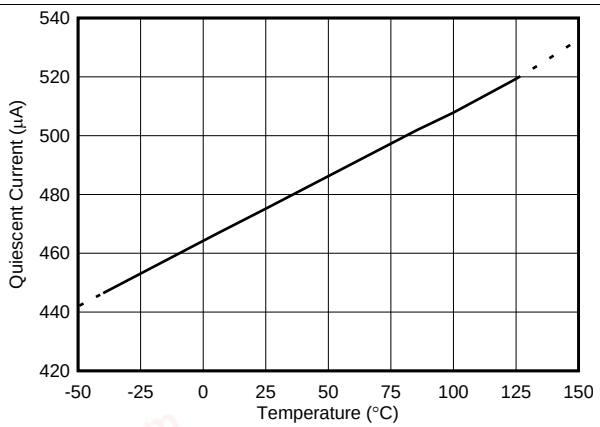


Figure 21. Quiescent Current vs Temperature

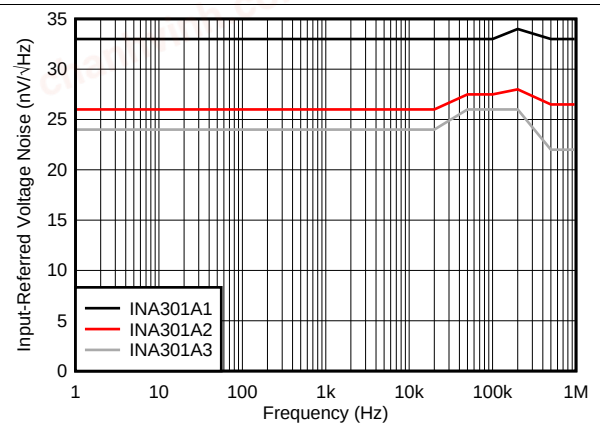


Figure 22. Input-Referred Voltage Noise vs Frequency

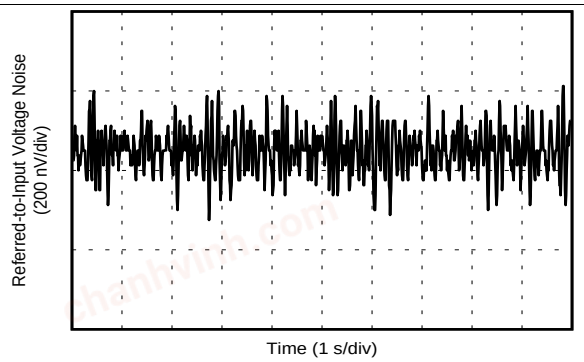


Figure 23. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

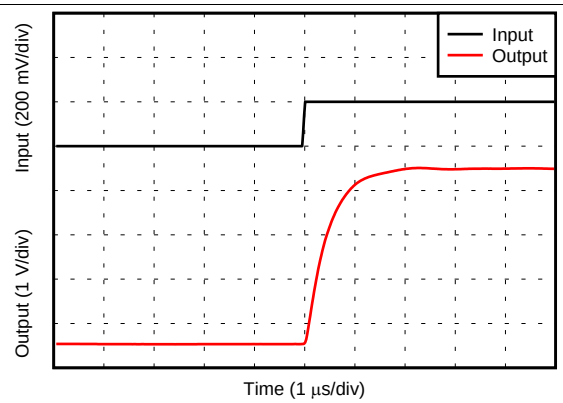


Figure 24. Voltage Output Rising Step Response ($4\text{-}V_{PP}$ Output Step)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

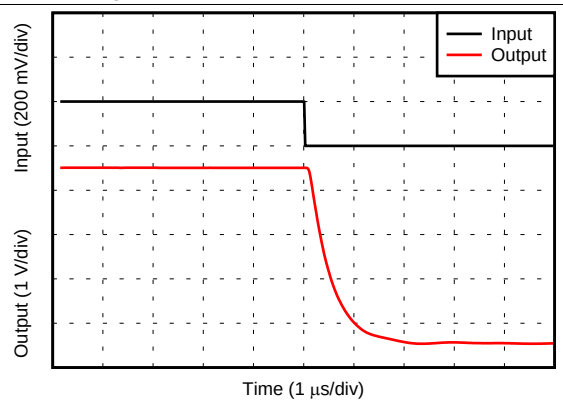


Figure 25. Voltage Output Falling Step Response (4-V_{PP} Output Step)

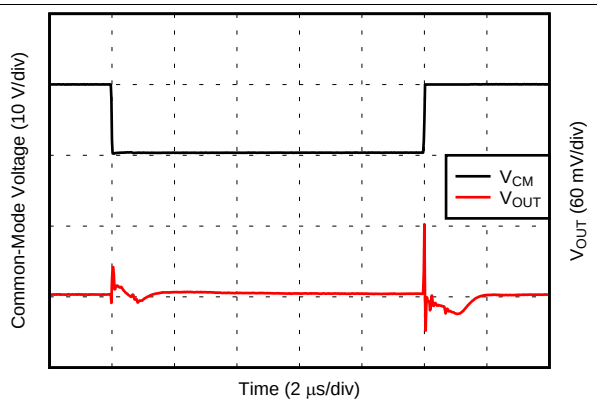


Figure 26. Common-Mode Voltage Transient Response

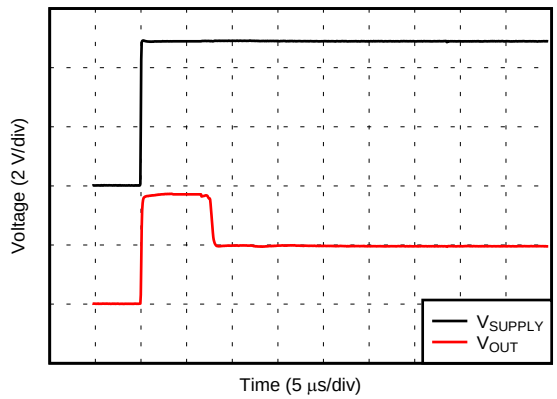


Figure 27. Start-Up Response

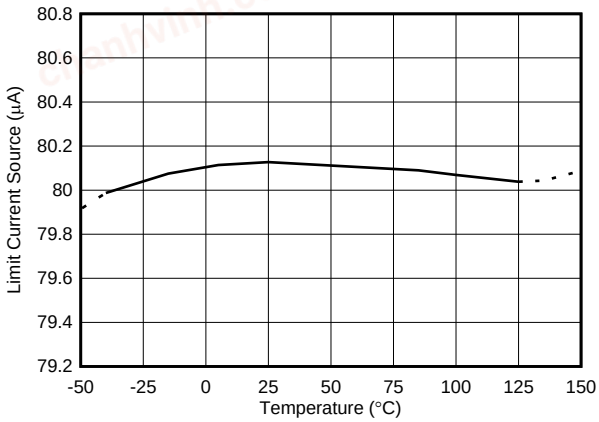


Figure 28. Limit Current Source vs Temperature

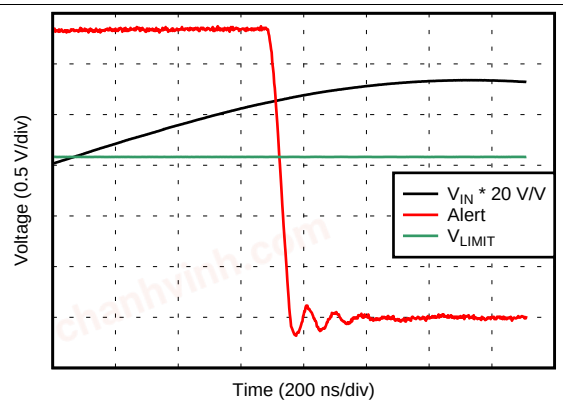


Figure 29. Total Propagation Delay (INA301A1)

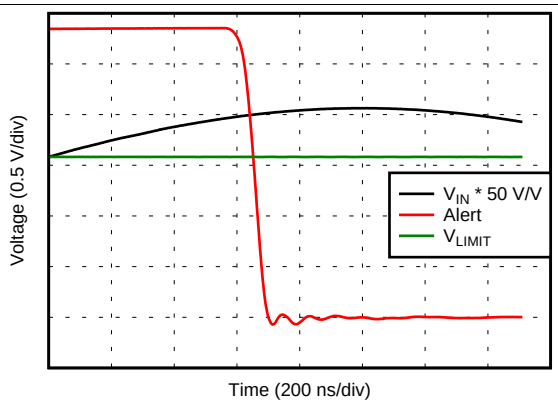


Figure 30. Total Propagation Delay (INA301A2)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

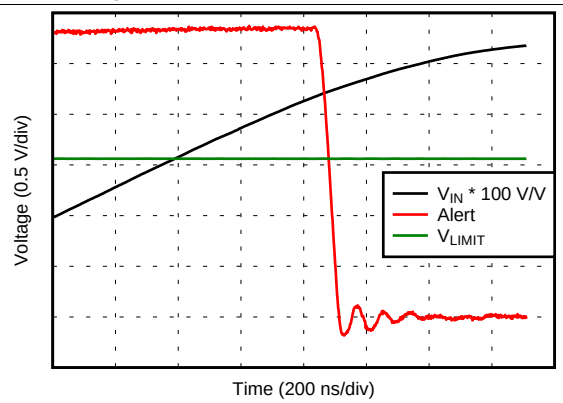


Figure 31. Total Propagation Delay (INA301A3)

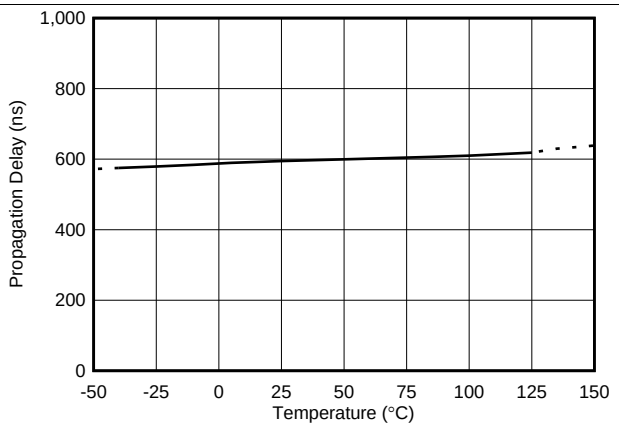


Figure 32. Comparator Propagation Delay vs Temperature (V_{OD} = 1 mV)

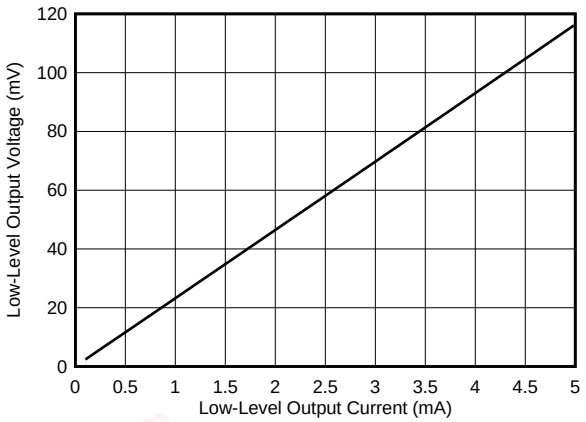


Figure 33. Comparator Alert V_{OL} vs I_{OL}

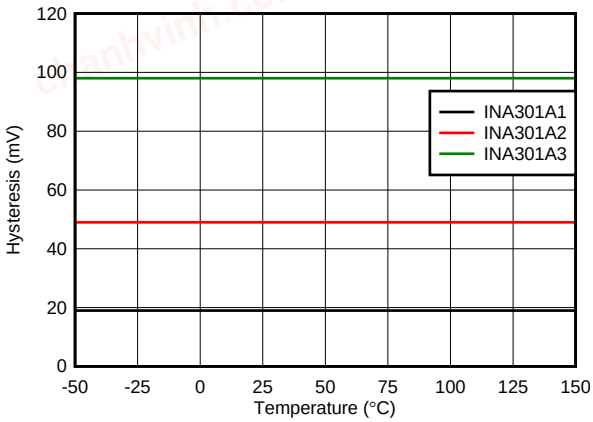


Figure 34. Hysteresis vs Temperature

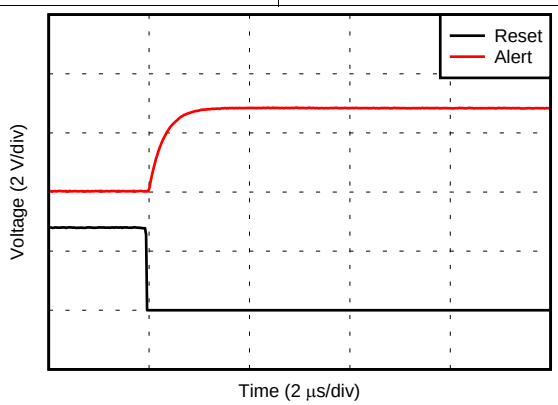


Figure 35. Comparator Reset Response

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7 Detailed Description

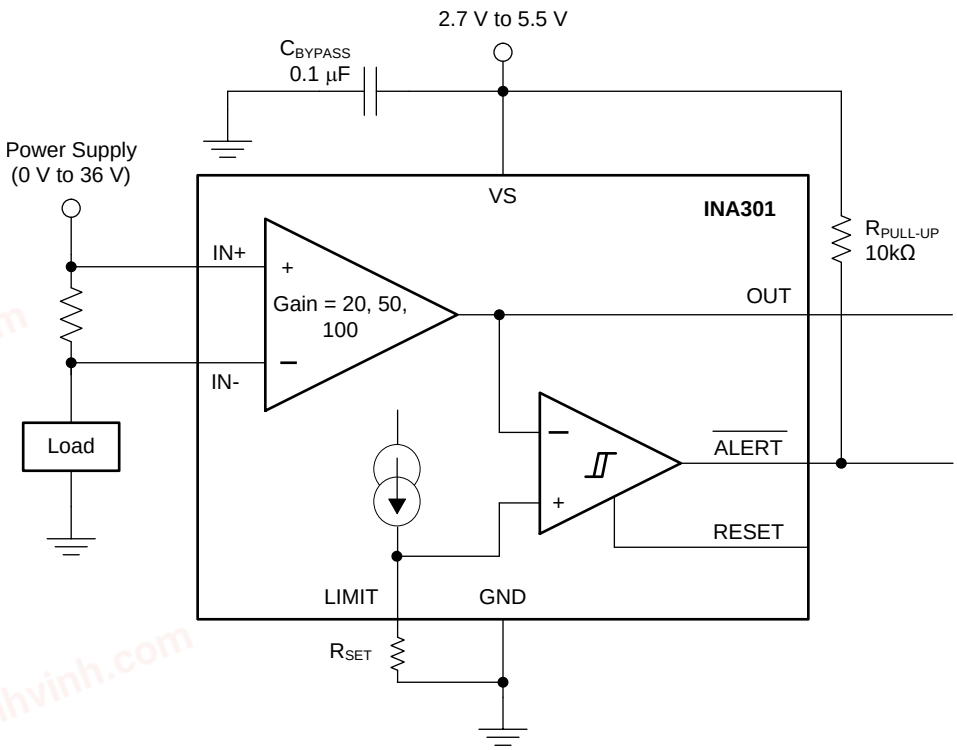
7.1 Overview

The INA301 is a 36-V common-mode, zero-drift topology, current-sensing amplifier that can be used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers are able to accurately measure voltages developed across current-sensing resistors (also known as current-shunt resistors) on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 36 V, and the device can be powered from supply voltages as low as 2.7 V. The device can also withstand the full 36-V common-mode voltage at the input pins when the supply voltage is removed without causing damage.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 35 µV with a temperature contribution of only 0.5 µV/°C over the full temperature range of –40°C to +125°C. The low total offset voltage of the INA301 enables smaller current-sense resistor values to be used, and allows for a more efficient system operation without sacrificing measurement accuracy resulting from the smaller input signal.

The INA301 uses a single external resistor to allow for a simple method of setting the corresponding current threshold level for the device to use for out-of-range comparison. Combining the precision measurement of the current-sense amplifier and the on-board comparator enables an all-in-one overcurrent detection device. This combination creates a highly-accurate solution that is capable of fast detection of out-of-range conditions and allows the system to take corrective actions to prevent potential component or system-wide damage.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Alert Output

The device $\overline{\text{ALERT}}$ pin is an active-low, open-drain output that is designed to be pulled low when the input conditions are detected to be out-of-range. This open-drain output pin is recommended to include a 10-kΩ, pullup resistor to the supply voltage. This open-drain pin can be pulled up to a voltage beyond the supply voltage, V_S, but must not exceed 5.5 V.

Figure 36 shows the alert output response of the internal comparator. When the output voltage of the amplifier is lower than the voltage developed at the LIMIT pin, the comparator output is in the default high state. When the amplifier output voltage exceeds the threshold voltage set at the LIMIT pin, the comparator output becomes active and pulls low. This active low output indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent or out-of-range condition has occurred.

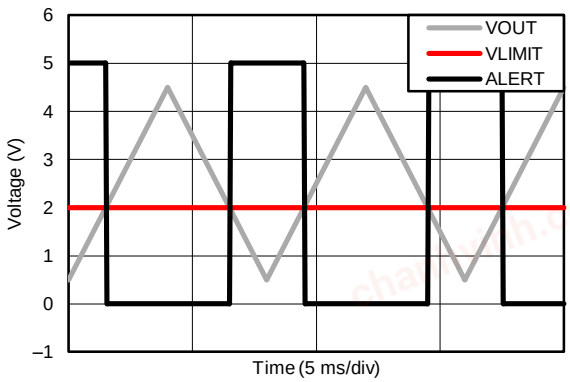


Figure 36. Overcurrent Alert Response

7.3.2 Alert Mode

The device has two output operating modes, transparent and latched, that are selected based on the RESET pin setting. These modes change how the $\overline{\text{ALERT}}$ pin responds following an alert when the overcurrent condition is removed.

7.3.2.1 Transparent Output Mode

The device is set to transparent mode when the RESET pin is pulled low, thus allowing the output alert state to change and follow the input signal with respect to the programmed alert threshold. For example, when the differential input signal rises above the alert threshold, the alert output pin is pulled low. As soon as the differential input signal drops below the alert threshold, the output returns to the default high output state. A common implementation using the device in transparent mode is to connect the $\overline{\text{ALERT}}$ pin to a hardware interrupt input on a microcontroller. As soon as an overcurrent condition is detected and the $\overline{\text{ALERT}}$ pin is pulled low, the controller interrupt pin detects the output state change and can begin making changes to the system operation required to address the overcurrent condition. Under this configuration, the $\overline{\text{ALERT}}$ pin transition from high to low is captured by the microcontroller so the output can return to the default high state when the overcurrent event is removed.

7.3.2.2 Latch Output Mode

Some applications do not have the functionality available to continuously monitor the state of the output $\overline{\text{ALERT}}$ pin to detect an overcurrent condition as described in the *Transparent Output Mode* section. A typical example of this application is a system that is only able to poll the $\overline{\text{ALERT}}$ pin state periodically to determine if the system is functioning correctly. If the device is set to transparent mode in this type of application, the state change of the $\overline{\text{ALERT}}$ pin can be missed when $\overline{\text{ALERT}}$ is pulled low to indicate an out-of-range event if the out-of-range condition does not appear during one of these periodic polling events. Latch mode is specifically intended to accommodate these applications.

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Feature Description (continued)

The device is placed into the corresponding output modes based on the signal connected to RESET, as shown in Table 1. The difference between latch mode and transparent mode is how the alert output responds when an overcurrent event ends. In transparent mode (RESET = low), when the differential input signal drops below the limit threshold level after the $\overline{\text{ALERT}}$ pin asserts because of an overcurrent event, the ALERT pin state returns to the default high setting to indicate that the overcurrent event has ended.

Table 1. Output Mode Settings

OUTPUT MODE	RESET PIN SETTING
Transparent mode	RESET = low
Latch mode	RESET = high

In latch mode (RESET = high), when an overlimit condition is detected and the $\overline{\text{ALERT}}$ pin is pulled low, the $\overline{\text{ALERT}}$ pin does not return to the default high state when the differential input signal drops below the alert threshold level. In order to clear the alert, the RESET pin must be pulled low for at least 100 ns. Pulling the RESET pin low allows the $\overline{\text{ALERT}}$ pin to return to the default high level provided that the differential input signal has dropped below the alert threshold. If the input signal is still above the threshold limit when the RESET pin is pulled low, the $\overline{\text{ALERT}}$ pin remains low. When the alert condition is detected by the system controller, the RESET pin can be set back to high in order to place the device back in latch mode.

The latch and transparent modes are represented in Figure 37. In Figure 37, when V_{IN} drops back below the V_{LIMIT} threshold for the first time, the RESET pin is pulled high. With the RESET pin is pulled high, the device is set to latch mode so that the alert output state does not return high when the input signal drops below the V_{LIMIT} threshold. Only when the RESET pin is pulled low does the $\overline{\text{ALERT}}$ pin return to the default high level, thus indicating that the input signal is below the limit threshold. When the input signal drops below the limit threshold for the second time, the RESET pin is already pulled low. The device is set to transparent mode at this point and the $\overline{\text{ALERT}}$ pin is pulled back high as soon as the input signal drops below the alert threshold.

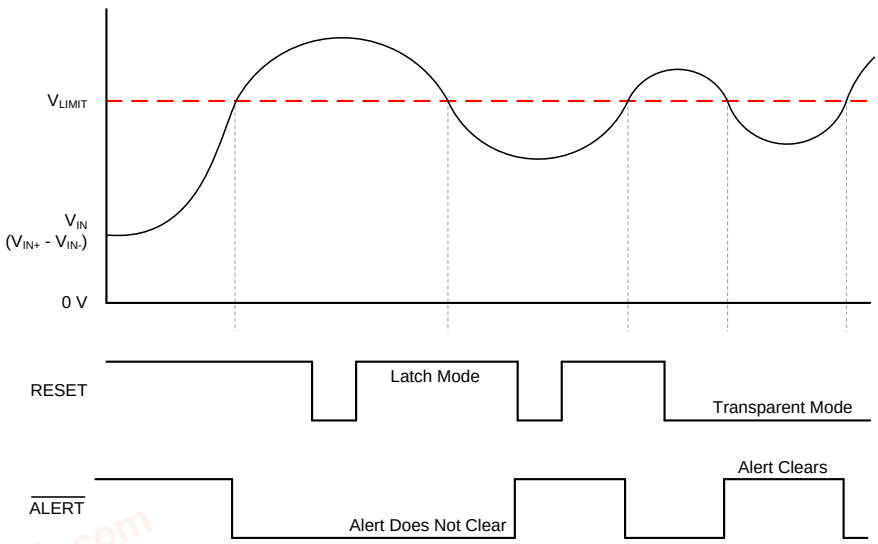


Figure 37. Transparent versus Latch Mode

7.3.3 Setting The Current-Limit Threshold

The INA301 determines if an overcurrent event is present by comparing the amplified measured voltage developed across the current-sensing resistor to the corresponding signal developed at the LIMIT pin. The threshold voltage for the LIMIT pin can be set using a single external resistor or by connecting an external voltage source to the LIMIT pin.

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7.3.3.1 Resistor-Controlled Current Limit

The typical approach for setting the limit threshold voltage is to connect a resistor from the LIMIT pin to ground. The value of this resistor, R_{LIMIT}, is chosen in order to create a corresponding voltage at the LIMIT pin equivalent to the output voltage, V_{OUT}, when the maximum desired load current is flowing through the current-sensing resistor. An internal 80-µA current source is connected to the LIMIT pin to create a corresponding voltage used to compare to the amplifier output voltage, depending on the value of the R_{LIMIT} resistor.

In the equations from Table 2, V_{TRIP} represents the overcurrent threshold that the device is programmed to monitor for and V_{LIMIT} is the programmed signal set to detect the V_{TRIP} level.

Table 2. Calculating the Limit Threshold Setting Resistor, R_{LIMIT}

PARAMETER		EQUATION
V_{TRIP}	V_{OUT} at the desired current trip value	$I_{LOAD} \times R_{SENSE}$ x Gain
V_{LIMIT}	Threshold limit voltage	$V_{LIMIT} = V_{TRIP}$
		$I_{LIMIT} \times R_{LIMIT}$
R_{LIMIT}	Calculate the threshold limit-setting resistor	V_{LIMIT} / I_{LIMIT}
		V_{LIMIT} / 80 µA

7.3.3.1.1 Resistor-Controlled Current Limit: Example

For example, if the current level indicating an out-of-range condition is present is 20 A and the current-sense resistor value is 10 mΩ, then the input threshold signal is 200 mV. The INA301A1 has a gain of 20 so the resulting output voltage at the 20-A input condition is 4 V. The value for R_{LIMIT} is selected to allow the device to detect to this 20-A threshold, indicating an overcurrent event has occurred. When the INA301 detects this out-of-range condition, the $\overline{\text{ALERT}}$ pin asserts and pulls low. For this example, the value of R_{LIMIT} to detect a 4-V level is calculated to be 50 kΩ, as shown in Table 3.

Table 3. Calculating the Limit Threshold Setting Resistor, R_{LIMIT}: Example

PARAMETER		EQUATION
V_{TRIP}	V_{OUT} at the desired current trip value	$I_{LOAD} \times R_{SENSE}$ x Gain
		20 A x 10 mΩ x 20 V/V = 4 V
V_{LIMIT}	Threshold limit voltage	$V_{LIMIT} = V_{TRIP}$
		$I_{LIMIT} \times R_{LIMIT}$
R_{LIMIT}	Calculate the threshold limit-setting resistor	V_{LIMIT} / I_{LIMIT}
		4 V / 80 µA = 50 kΩ

7.3.3.2 Voltage-Source-Controlled Current Limit

The second method for setting the limit voltage is to connect the LIMIT pin to a programmable digital-to-analog converter (DAC) or other external voltage source. The benefit of this method is the ability to adjust the current-limit threshold to account for different threshold voltages that are used for different system operating conditions. For example, this method can be used in a system that has one current-limit threshold level that must be monitored during a power-up sequence but different threshold levels that must be monitored during other system operating modes.

In Table 4, V_{TRIP} represents the overcurrent threshold that the device is programmed to monitor for and V_{SOURCE} is the programmed signal set to detect the V_{TRIP} level.

Table 4. Calculating the Limit Threshold Voltage Source, V_{SOURCE}

PARAMETER		EQUATION
V_{TRIP}	V_{OUT} at the desired current trip value	$I_{LOAD} \times R_{SENSE} \times$ Gain
V_{SOURCE}	Program the threshold limit voltage	$V_{SOURCE} = V_{TRIP}$

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7.3.4 Selecting a Current-Sensing Resistor

The device measures the differential voltage developed across a resistor when current flows through the component to determine if the current being monitored exceeds a defined limit. This resistor is commonly referred to as a *current-sensing resistor* or a *current-shunt resistor*, with each term commonly used interchangeably. The flexible design of the device allows for measuring a wide differential input signal range across this current-sensing resistor.

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the current-sensing resistor. Larger voltages developed across this resistor allow for more accurate measurements to be made. Amplifiers have fixed internal errors that are largely dominated by the inherent input offset voltage. When the input signal decreases, these fixed internal amplifier errors become a larger portion of the measurement and increase the uncertainty in the measurement accuracy. When the input signal increases, the measurement uncertainty is reduced because the fixed errors are a smaller percentage of the signal being measured. Therefore, the use of larger value current-sensing resistors inherently improves the measurement accuracy.

However, a system design trade-off must be evaluated through use of larger input signals for improving the measurement accuracy. Increasing the current sense resistor value results in an increase in power dissipation across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through the component. This increase in voltage across the resistor increases the power that the resistor must be able to dissipate. Decreasing the value of the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreased input signal. Selecting the optimal value for the shunt resistor requires factoring both the accuracy requirement for the specific application and the allowable power dissipation of this component.

An increasing number of very low ohmic-value resistors are becoming more widely available with values reaching down as low as 200 μΩ or lower with power dissipations of up to 5 W that enable large currents to be accurately monitored with sensing resistors.

7.3.4.1 Selecting a Current-Sensing Resistor: Example

In this example, the trade-offs involved in selecting a current-sensing resistor are discussed. This example requires 2.5% accuracy for detecting a 10-A overcurrent event where only 250 mW is allowable for the dissipation across the current-sensing resistor at the full-scale current level. Although the maximum power dissipation is defined as 250 mW, a lower dissipation is preferred to improve system efficiency. Some initial assumptions are made that are used in this example: the limit-setting resistor (R_{LIMIT}) is a 1% component and the maximum tolerance specification for the internal threshold setting current source (0.5%) is used. Given the total error budget of 2.5%, up to 1% of error is available to be attributed to the measurement error of the device under these conditions.

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As shown in Table 5, the maximum value calculated for the current-sensing resistor with these requirements is 2.5 mΩ. Although this value satisfies the maximum power dissipation requirement of 250 mW, headroom is available from the 2.5% maximum total overcurrent detection error to reduce the value of the current-sensing resistor and reduce the power dissipation further. Selecting a 1.5-mΩ, current-sensing resistor value offers a good tradeoff for reducing the power dissipation in this scenario by approximately 40% and still remaining within the accuracy region.

Table 5. Calculating the Current-Sensing Resistor, R_{SENSE}

PARAMETER		EQUATION	VALUE	UNIT
I_{MAX}	Maximum current		10	A
P_{D_MAX}	Maximum allowable power dissipation		250	mW
R_{SENSE_MAX}	Maximum allowable R_{SENSE}	P_{D_MAX} / I_{MAX}^2	2.5	mΩ
V_{OS}	Offset voltage		150	µV
V_{OS_ERROR}	Initial offset voltage error	$(V_{OS} / (R_{SENSE_MAX} \times I_{MAX}) \times 100$	0.6%	
E_G	Gain error		0.25%	
$ERROR_{TOTAL}$	Total measurement error	$\sqrt{(V_{OS_ERROR}^2 + E_G^2)}$	0.65%	
	Allowable current threshold accuracy		2.5%	
$ERROR_{INITIAL}$	Initial threshold error	I_{LIMIT} Tolerance + R_{LIMIT} Tolerance	1.5%	
$ERROR_{AVAILABLE}$	Maximum allowable measurement error	Maximum Error – $ERROR_{INITIAL}$	1%	
$V_{OS_ERROR_MAX}$	Maximum allowable offset error	$\sqrt{(ERROR_{AVAILABLE}^2 - E_G^2)}$	0.97%	
V_{DIFF_MIN}	Minimum differential voltage	$V_{OS} / V_{OS_ERROR_MAX\ (1\%)}$	15	mV
R_{SENSE_MIN}	Minimum sense resistor value	V_{DIFF_MIN} / I_{MAX}	1.5	mΩ
P_{D_MIN}	Lowest possible power dissipation	$R_{SENSE_MIN} \times I_{MAX}^2$	150	mW

7.3.5 Hysteresis

The on-board comparator in the INA301 is designed to reduce the possibility of oscillations in the alert output when the measured signal level is near the overlimit threshold level because of noise. When the output voltage (V_{OUT}) exceeds the voltage developed at the LIMIT pin, the $\overline{ALERT}$ pin is asserted and pulls low. The output voltage must drop below the LIMIT pin threshold voltage by the gain-dependent hysteresis level in order for the $\overline{ALERT}$ pin to de-assert and return to the nominal high state, as shown in Figure 38.

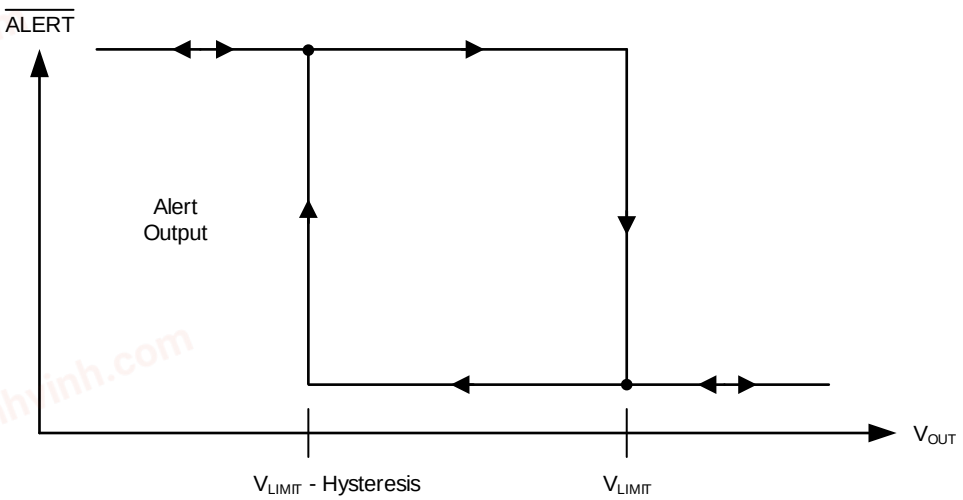


Figure 38. Typical Comparator Hysteresis

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7.4 Device Functional Modes

7.4.1 Input Filtering

External system noise can significantly affect the ability of a comparator to accurately measure and detect whether input signals exceed the reference threshold levels, thus reliably indicating an overrange condition. The most obvious effect that external noise can have on the operation of a comparator is to cause a false alert condition. If a comparator detects a large noise transient coupled into the signal, the device can easily interpret this transient as an overrange condition.

External filtering can help reduce the amount of noise that reaches the comparator and reduce the likelihood of a false alert from occurring. The tradeoff to adding this noise filter is that the alert response time is increased because of the input signal being filtered as well as the noise. Figure 39 shows the implementation of an input filter for the device.

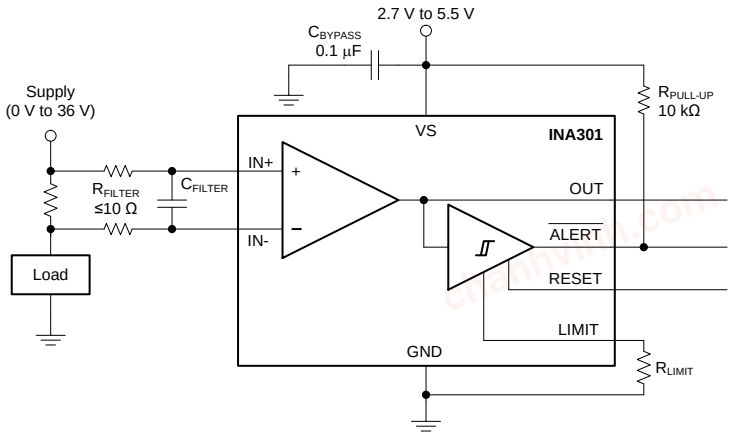


Figure 39. Input Filter

Limiting the amount of input resistance used in this filter is important because this resistance can have a significant affect on the input signal that reaches the device input pins resulting from the device input bias currents. A typical system implementation involves placing the current-sensing resistor very near the device so the traces are very short and the trace impedance is very small. This layout helps reduce the ability of coupling additional noise into the measurement. Under these conditions, the characteristics of the input bias currents have minimal affect on device performance.

As illustrated in Figure 40, the input bias currents increase in opposite directions when the differential input voltage increases. This increase results from the design of the device that allows common-mode input voltages to far exceed the device supply voltage range. With input filter resistors now placed in series with these unequal input bias currents, there are unequal voltage drops developed across these input resistors. The difference between these two drops appears as an added signal that (in this case) subtracts from the voltage developed across the current-sensing resistor, thus reducing the signal that reaches the device input pins. Smaller value input resistors reduce this effect of signal attenuation to allow for a more accurate measurement.

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Device Functional Modes (continued)

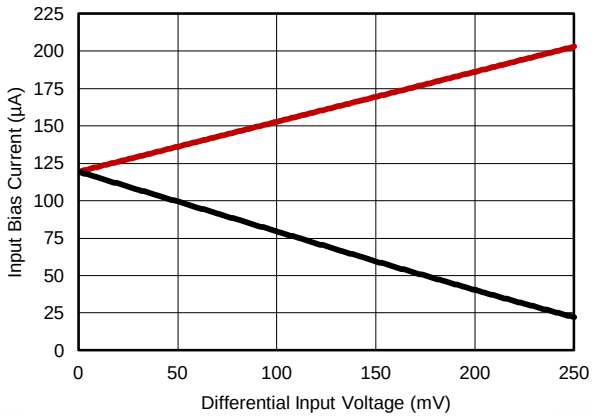


Figure 40. Input Bias Current vs Differential Input Voltage

For example, with a differential voltage of 10 mV developed across a current-sensing resistor and using 20-Ω resistors, the differential signal that actually reaches the device is 9.85 mV. A measurement error of 1.5% is created as a result of these external input filter resistors. Using 10-Ω input filter resistors instead of the 20-Ω resistors reduces this added error from 1.5% down to 0.75%.

7.4.2 Using The INA301 with Common-Mode Transients Above 36 V

With a small amount of additional circuitry, the device can be used in circuits subject to transients higher than 36 V. Use only zener diodes or zener-type transient absorbers (sometimes referred to as *transzorbs*). Any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors, as shown in Figure 41, as a working impedance for the zener diode. Keeping these resistors as small as possible is best, preferably 10 Ω or less. Larger values can be used with an additional induced error resulting from a reduced signal that actually reaches the device input pins. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional zener diodes of the lowest power rating available. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

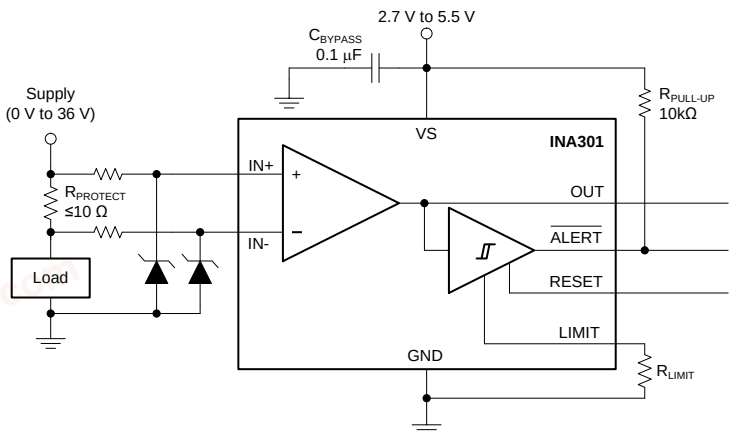


Figure 41. Transient Protection

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8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA301 is designed to enable easy configuration for detecting overcurrent conditions in an application. This device is individually targeted towards unidirectional overcurrent detection of a single threshold. However, this device can also be paired with additional devices and circuitry to create more complex monitoring functional blocks.

8.2 Typical Application

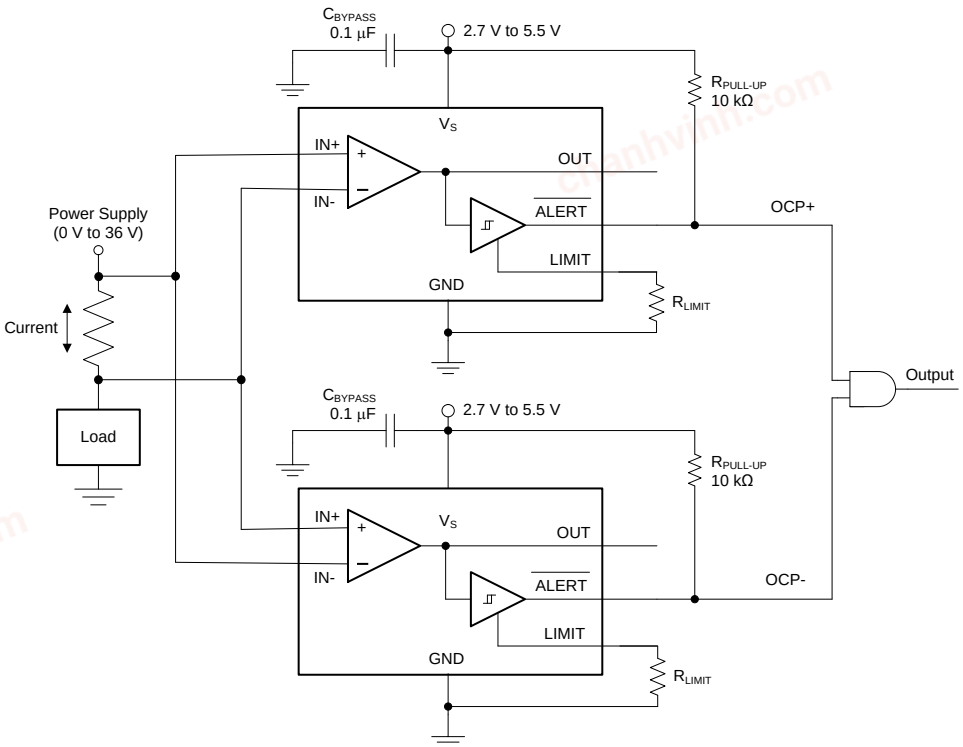


Figure 42. Bidirectional Application

8.2.1 Design Requirements

Although the device is only able to measure current through a current-sensing resistor flowing in one direction, a second INA301 can be used to create a bidirectional monitor.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

With the input pins of a second device reversed across the same current-sensing resistor, the second device is now able to detect current flowing in the other direction relative to the first device; see Figure 42. The outputs of each device connect to an AND gate to detect if either of the limit threshold levels are exceeded. As shown in Table 6, the output of the AND gate is high if neither overcurrent limit thresholds are exceeded. A low output state of the AND gate indicates that either the positive overcurrent limit or the negative overcurrent limit are surpassed.

Table 6. Bidirectional Overcurrent Output Status

OCP STATUS	OUTPUT
OCP+	0
OCP–	0
No OCP	1

8.2.3 Application Curve

Figure 43 shows two INA301 devices being used in a bidirectional configuration and an output control circuit to detect if one of the two alerts is exceeded.

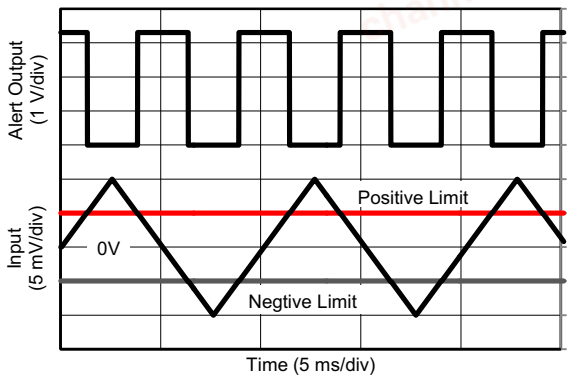


Figure 43. Bidirectional Application Curve

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9 Power Supply Recommendations

The device input circuitry can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the V_S power-supply pin can be 5 V, whereas the load power-supply voltage being monitored (V_{CM}) can be as high as 36 V. Note also that the device can withstand the full –0.3 V to 36 V range at the input pins, regardless of whether the device has power applied or not.

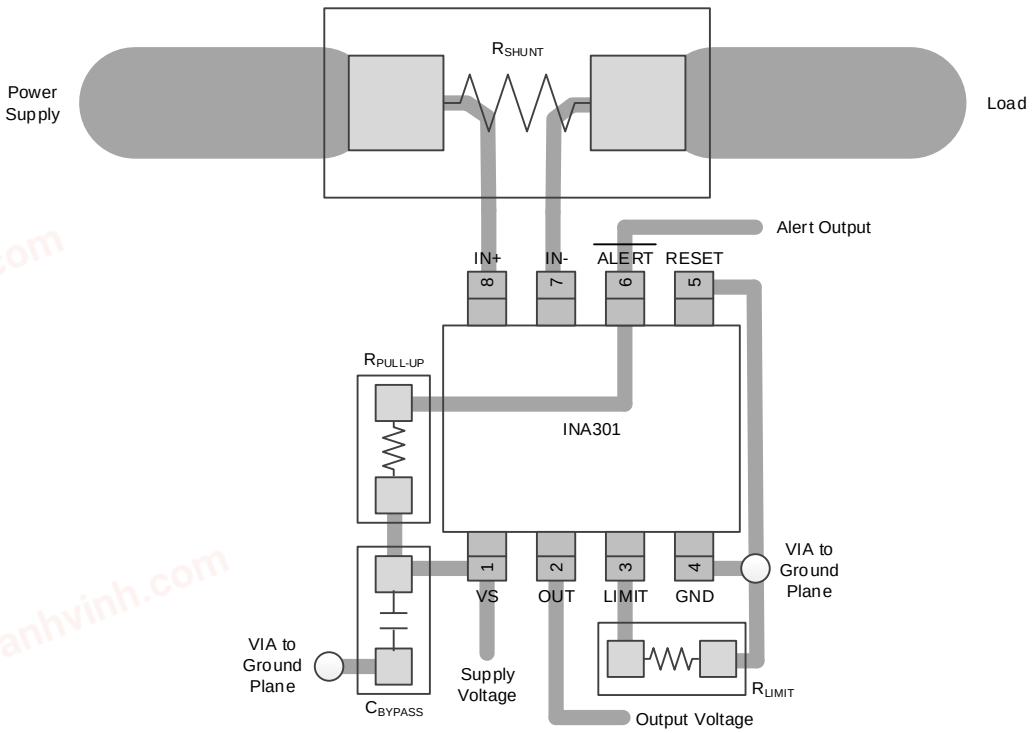
Power-supply bypass capacitors are required for stability and must be placed as closely as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Make the connection of R_{LIMIT} to the ground pin as direct as possible to limit additional capacitance on this node. Routing this connection must be limited to the same plane if possible to avoid vias to internal planes. If the routing can not be made on the same plane and must pass through vias, ensure that a path is routed from R_{LIMIT} back to the ground pin and that R_{LIMIT} is not simply connected directly to a ground plane.
- The open-drain output pin is recommended to be pulled up to the supply voltage rail through a 10-kΩ pullup resistor.

10.2 Layout Example



NOTE: Connect the limit resistor directly to the GND pin.

Figure 44. Recommended Layout

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11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

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10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA301A1IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGD6	Samples
INA301A1IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGD6	Samples
INA301A2IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGI6	Samples
INA301A2IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGI6	Samples
INA301A3IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGH6	Samples
INA301A3IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZGH6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF INA301 :

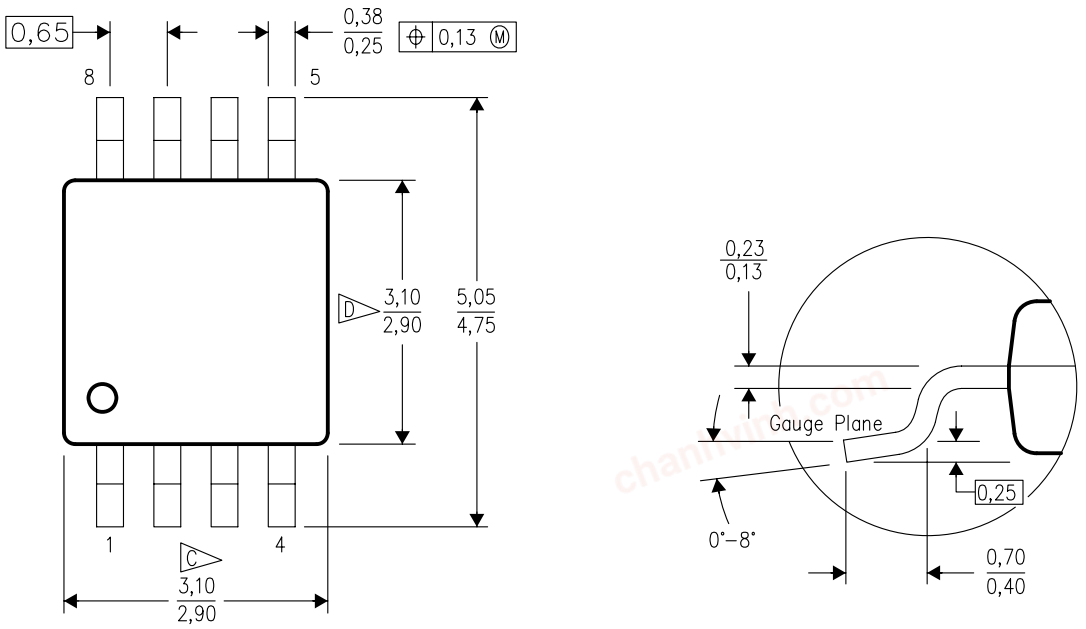
- Automotive: INA301-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

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DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE

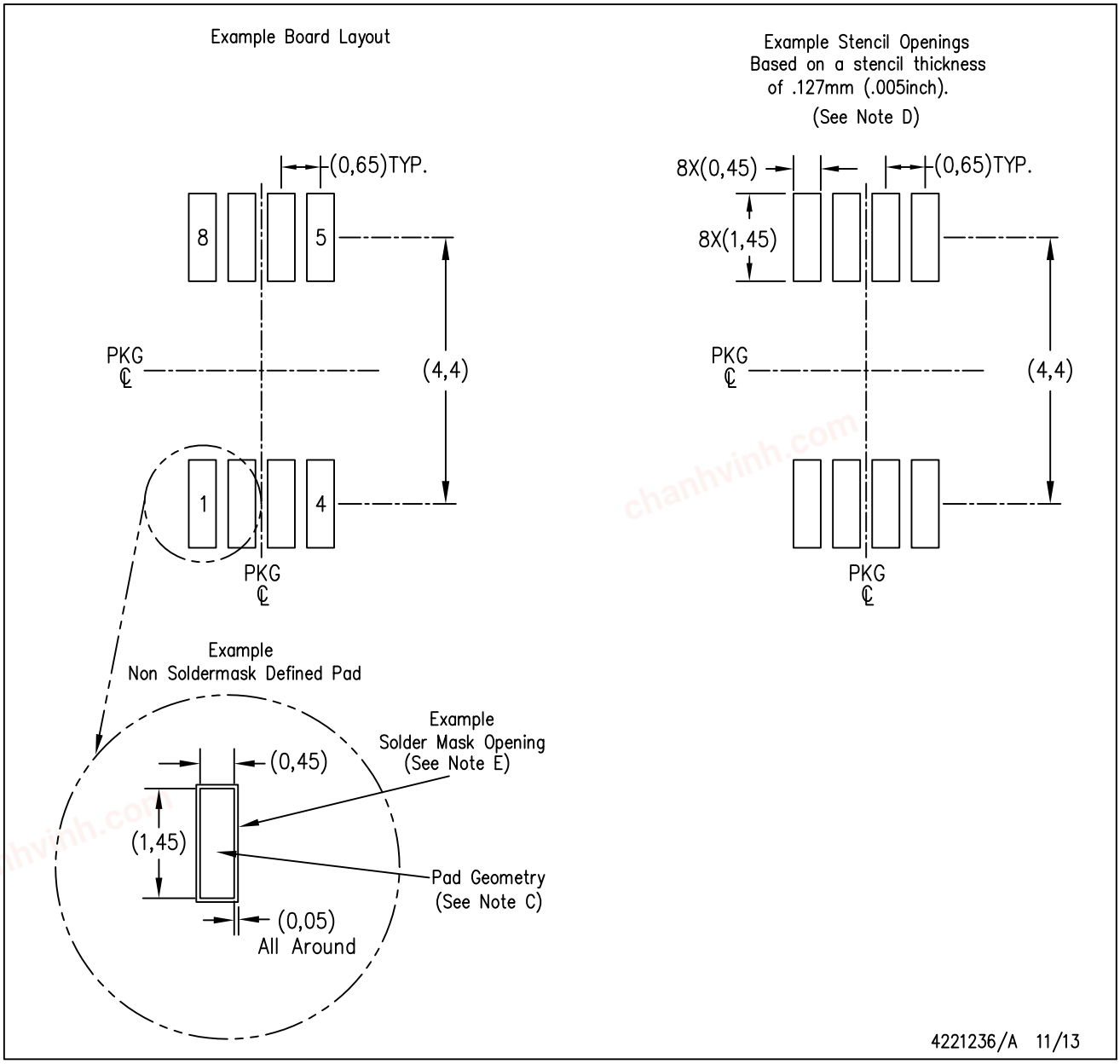


4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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