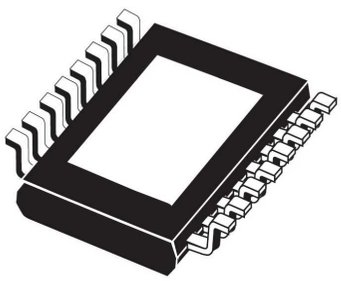
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VNQ9080AJ

Datasheet

Quad channel high-side driver with Current Sense analog feedback for automotive applications



PowerSSO-16

Product status link
VNQ9080AJ

Product summary	
Order code	VNQ9080AJTR
Package	PowerSSO-16
Packing	Tape and reel

Features

Description	Parameter	Value
Max transient supply voltage	V_{CC}	36 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	86 mΩ
Current limitation (typ)	I_{LIMH}	13.6 A
Standby current (max)	I_{STBY}	0.5 µA

- AEC-Q100 qualified
- Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
- General
  - Quad channel smart high-side driver with current sense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- CurrentSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection (with external pull-up)
  - Output short to V_{CC} detection
  - Sense enable/disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery with external components
  - Electrostatic discharge protection

Applications

- Automotive resistive, inductive and capacitive loads
- Protected supply for ADAS systems: radars and sensors
- Automotive signal lamp: R10W and LEDs

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Description

The device is a quad channel high-side driver manufactured using ST proprietary VIPower M0-9 technology and housed in PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers diagnostic functions including high precision proportional load current sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

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1 Block diagram and pin description

Figure 1. Block diagram

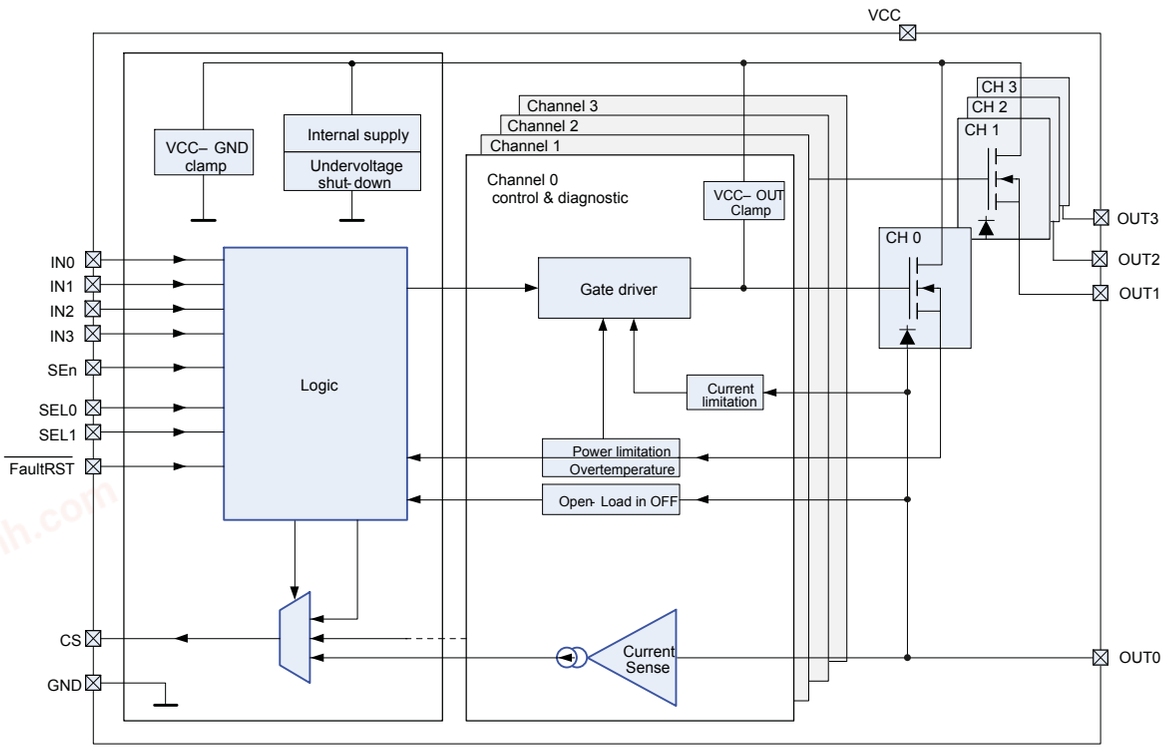
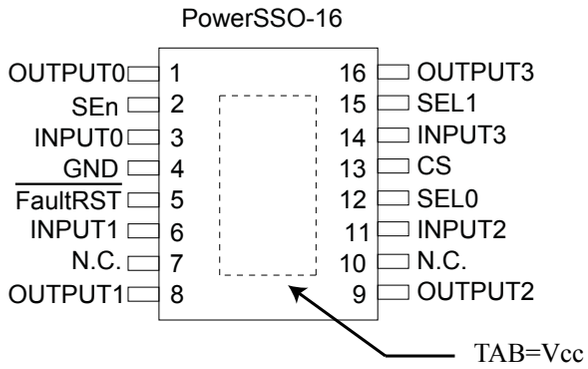


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{0,1,2,3}$	Power output
GND	Ground connection; must be reverse battery protected by an external diode / resistor network.
$INPUT_{0,1,2,3}$	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs; controls output switch state.
CS	analog current sense output pin; it delivers a current proportional to the selected load current.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; enables the CS diagnostic pin.
$SEL_{0,1}$	Active high compatible with 3 V and 5 V CMOS outputs pin; it addresses the CS multiplexer.
$\overline{FaultRST}$	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault - if kept low, sets the output to auto-restart mode.

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Figure 2. **Configuration diagram (top view)**



GADG010318144RI

Table 2. **Suggested connections for unused and not connected pins**

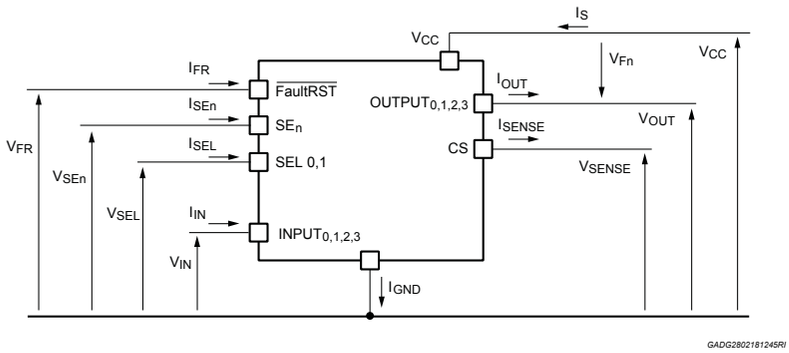
Connection / pin	CS	N.C.	Output	Input	SEn, SELx, $\overline{\text{FaultRST}}$
Floating	Not allowed	X	X(1)	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. *X: do not care.*

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2 Electrical specification

Figure 3. **Current and voltage conventions**



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 3. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect the device reliability.

Table 3. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	36	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	$OUTPUT_{0,1,2,3}$ DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	2.2	
I_{IN}	$INPUT_{0,1,2,3}$ DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current	-1 to 3	
$I_{SEL0,1}$	$SEL_{0,1}$ DC input current	-1 to 10	
I_{FR}	$\overline{FaultRST}$ DC input current		
I_{SENSE}	CS pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	10	mA
	CS pin DC output current in reverse ($V_{CC} < 0$ V)	-20	
E_{MAX}	Maximum switching energy (single pulse); T_{jstart} = 150 °C)	4	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)		
	$INPUT_{0,1,2,3}$	2000	V
	CS	2000	
	SEn, $SEL_{0,1}$, $\overline{FaultRST}$	2000	
	$OUTPUT_{0,1,2,3}$	4000	

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Symbol	Parameter	Value	Unit
V_{ESD}	V_{CC}	4000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8)(1)(2)	9.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(1)(3)	54.5	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)(2)	22.5	

1. *One channel ON.*
2. *Device mounted on four-layer 2s2p PCB.*
3. *Device mounted on two-layer 2s0p PCB with 2 cm^2 heatsink copper trace.*

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2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown			2.1	2.7	V
$V_{USDReset}$	Undervoltage shutdown reset				4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.15		V
R_{ON}	On-state resistance(1)	I_{OUT} = 0.7 A; T_j = 25°C		86		mΩ
		I_{OUT} = 0.7 A; T_j = 150°C			190	
		I_{OUT} = 0.7 A; V_{CC} = 4 V; T_j = 25°C			149	
		I_{OUT} = 0.07 A; V_{CC} = 2.7 V; V_{CC} decreasing			516	
V_{clamp}	Clamp voltage	I_S = 20 mA; 25°C < T_j < 150°C	36	38	45	V
		I_S = 20 mA; T_j = -40°C	36			V
I_{STBY}	Supply current in standby at V_{CC} = 13 V (2)	V_{CC} = 13 V; $V_{IN0,1,2,3}$ = $V_{OUT0,1,2,3}$ = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; $V_{IN0,1,2,3}$ = $V_{OUT0,1,2,3}$ = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0; T_j = 85°C (3)			0.5	
		V_{CC} = 13 V; $V_{IN0,1,2,3}$ = $V_{OUT0,1,2,3}$ = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 125°C			3	
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = $V_{SEL0,1}$ = 0 V; V_{SEn} = 5 V to 0 V	60	260	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = V_{FR} = $V_{SEL0,1}$ = 0 V; $V_{IN0,1,2,3}$ = 5 V; $I_{OUT0,1,2,3}$ = 0 A		5.5	7.5	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; $V_{IN0,1,2,3}$ = 5 V; $I_{OUT0,1,2,3}$ = 0.7 A;			9	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V(2)	$V_{IN0,1,2,3}$ = $V_{OUT0,1,2,3}$ = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		$V_{IN0,1,2,3}$ = $V_{OUT0,1,2,3}$ = 0 V; V_{CC} = 13 V; T_j = 125°C	0		3	
V_F	Output - V_{CC} diode voltage at T_j = 150°C	I_{OUT} = -0.7 A; T_j = 150°C			0.7	V

1. *For each channel.*
2. *PowerMOS leakage included*
3. *Parameter specified by design; not subject to production test.*

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Table 6. Switching

V_{CC} = 13 V; -40°C < T_j < 150°C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{d(on)}$ (1)	Turn-on delay time at T_j = 25 °C	R_L = 18.6 Ω	10	26	120	µs
$t_{d(off)}$ (1)	Turn-off delay time at T_j = 25 °C		10	30	100	
$(dV_{OUT}/dt)_{on}$ (1)	Turn-on voltage slope at T_j = 25 °C		0.2	0.42	0.7	V/µs
$(dV_{OUT}/dt)_{off}$ (1)	Turn-off voltage slope at T_j = 25 °C		0.2	0.45	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})		—	0.06	0.095 (2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})		—	0.06	0.095(2)	mJ
t_{SKEW}	Differential pulse skew (t_{PHL} - t_{PLH})		-45	5	+55	µs

1. See *Figure 4. Switching time and pulse skew.*
2. *Parameter guaranteed by design and characterization; not subject to production test.*

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Table 7. Logic inputs

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$INPUT_{0,1,2,3}$ characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	6		8.5	V
		I_{IN} = -1 mA		-0.7		
$\overline{FaultRST}$ characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	6		8.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1}$ characteristics (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	6		8.5	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{SEN} = 1 mA	9		12	V
		I_{SEN} = -1 mA		-0.7		

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Table 8. Protections

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LIMH} (1)	DC short- circuit current	V_{CC} = 16 V; T_j = -40°C	-15%	14	15%	A
		V_{CC} = 16 V; T_j = 150°C	-15%	10	15%	
I_{LIMH2} (2)		V_{CC} = 19 V; T_j = -40°C	-15%	11.2	15%	
		V_{CC} = 19 V; T_j = 150°C	-15%	8.9	15%	
I_{LIMH} at 22 V		V_{CC} = 22 V; T_j = 25°C		4.2		
T_{TSD}	Shutdown temperature		150	175	210	°C
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_{RS}) (3)			7		
ΔT_{J_SD}	Dynamic temperature	V_{CC} = 19 V		55		K
		V_{CC} = 16 V		80		
t_{LATCH_RST}	Fault reset time for output unlatch (3)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; E.g. Ch_0: V_{IN0} = 5 V; $V_{SEL0,1}$ = 0 V	3	10	20	µs
$t_{D_Restart}$	Latch-OFF delay time before automatic restart	T_j > 125°C		50	75	ms
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 0.7 A; L = 6 mH; T_j = -40°C	V_{CC} - 36			V
		I_{OUT} = 0.7 A; L = 6 mH; T_j = 25°C to 150°C	V_{CC} - 36	V_{CC} - 38	V_{CC} - 45	V

1. *I_{LIMH} guaranteed between 7V and 16V, -40°C < T_j < 150°C*
2. *I_{LIMH2} guaranteed between 16V and 19V, -40°C < T_j < 150°C*
3. *Parameter guaranteed by design and characterization; not subject to production test.*

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Table 9. Current Sense

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{SENSE_CL}	CurrentSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-9	-8	-7	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		
CurrentSense characteristics						
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.01 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	810			
dK_{OL}/K_{OL} (1)(2)	Current sense ratio drift at calibration point		-25		25	%
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-35%	1500	+35%	
dK_0/K_0 (1) (2)	CurrentSense ratio drift		-25		25	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.15 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-15%	1500	15%	
dK_1/K_1 (1) (2)	CurrentSense ratio drift		-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 0.7 A; V_{SENSE} = 3.5 V; V_{SEn} = 5 V	-7%	1500	7%	
dK_2/K_2 (1) (2)	CurrentSense ratio drift		-7		7	%
K_{850}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.85 A; V_{SENSE} = 3.5 V; V_{SEn} = 5 V	-7%	1500	7%	
dK_{850}/K_{850} (1) (2)	CurrentSense ratio drift		-7		7	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 2.1 A; V_{SENSE} = 3.5 V; V_{SEn} = 5 V	-5%	1500	5%	
dK_3/K_3 (1) (2)	CurrentSense ratio drift		-5		5	%
I_{SENSE0}	CurrentSense leakage current	CS disabled: V_{SEn} = 0 V	0		0.5	µA
		CS disabled: -1 V < V_{SENSE} < 5 V (1)	-0.5		0.5	
		CS enabled: V_{SEn} = 5 V; all channel ON; I_{OUTX} = 0 A; Ch_X diagnostic selected; E.g. Ch_0: V_{IN0} = 5 V; $V_{IN1,2,3}$ = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 0 A; $I_{OUT1,2,3}$ = 0.7 A	0		10	
		CS enabled: V_{SEn} = 5 V; Ch_X OFF; I_{OUTX} = 0 A; Ch_X diagnostic selected; E.g. Ch_0: V_{IN0} = 0 V; $V_{IN1,2,3}$ = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 0 A; $I_{OUT1,2,3}$ = 0.7 A	0		1	
V_{OUT_MSD} (1)	Output voltage for CurrentSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ; E.g. Ch_0: V_{IN0} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 0.7 A		5		V
V_{SENSE_SAT}	CurrentSense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 10 kΩ; V_{SEn} = 5 V; V_{IN0} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 6 A; T_j = -40 °C	4.8			V

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7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{SENSE_SAT} (1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 3.5 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; T_j = 150°C	2			mA
I_{OUT_SAT} (1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 3.5 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; T_j = 150°C	4			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	V_{SEn} = 5 V; C_{hX} OFF; C_{hX} diagnostic selected E.g: C_{h0}□ V_{IN0} = 0 V; $V_{SEL0,1}$ = 0 V;	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40°C to 125°C	-150	-40	-5	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 6. T_{DSTKON})	V_{SEn} = 5 V; C_{hX} ON to OFF transition; C_{hX} diagnostic selected E.g: C_{h0}□ V_{IN0} = 5 V to 0 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	100	170	250	µs
$t_{D_OL_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	$V_{IN0,1,2,3}$ = 0 V; V_{FR} = 0 V; V_{OUT0} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{SEn} = 5 V; C_{hX} OFF; C_{hX} diagnostic selected E.g: C_{h0}□ V_{IN0} = 0 V; $V_{SEL0,1}$ = 0 V; V_{OUT0} = 0 V to 4 V		5	30	µs
Fault diagnostic feedback (see Table 10. Truth table)						
V_{SENSEH}	CurrentSense output voltage in fault condition	13 V < V_{CC} < 18 V; • E.g: C_{h0} in open load; R_{SENSE} = 0.7 kΩ; V_{IN0} = 0 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 0 A; V_{OUT0} = 4 V	5		7.5	V
		V_{CC} = 7 V; • E.g: C_{h0} in open load; R_{SENSE} = 0.7 kΩ; V_{IN0} = 0 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 0 A; V_{OUT0} = 4 V	4.3			
I_{SENSEH}	CurrentSense output current in fault condition	13 V < V_{CC} < 18 V; V_{SENSE} = 5 V • E.g: C_{h0} in open load; V_{IN0} = 0 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 0 A; V_{OUT0} = 4 V	7	8.6	12	mA

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7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{SENSEH}	CurrentSense output current in fault condition	V_{CC} = 7 V; V_{SENSE} = 5 V • E.g: C_{h0} in open load; V_{IN0} = 0 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 0 A; V_{OUT0} = 4 V	4.4			mA
CurrentSense timings (current sense mode - see Figure 5. Current Sense timings (current sense mode))(3)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 18.6 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn			5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 18.6 Ω		100	200	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; I_{SENSE} = 90 % of $I_{SENSEMAX}$; R_L = 18.6 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 18.6 Ω		70	250	µs
$t_{DSENSE3H}$	Current sense latch-OFF filtering time		1.4	2	2.6	ms
CurrentSense timings (Multiplexer transition times)(3)						
t_{D_XtoY}	CurrentSense transition delay from Ch_X to Ch_Y	V_{IN0} = 5 V; V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 0 A; I_{OUT1} = 0.7 A; R_{SENSE} = 1 kΩ			30	µs
$t_{D_CStoVSENSEH}$	CurrentSense transition delay from stable current sense on Ch_X to V_{SENSEH} on Ch_Y	V_{IN0} = 5 V; V_{IN1} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 0.7 A; V_{OUT1} = 4 V; R_{SENSE} = 1 kΩ			20	

1. *Parameter specified by design; not subject to production test.*
2. *All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.*
3. *Transition delay is measured up to +/- 10% of final conditions.*

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Figure 4. **Switching time and pulse skew**

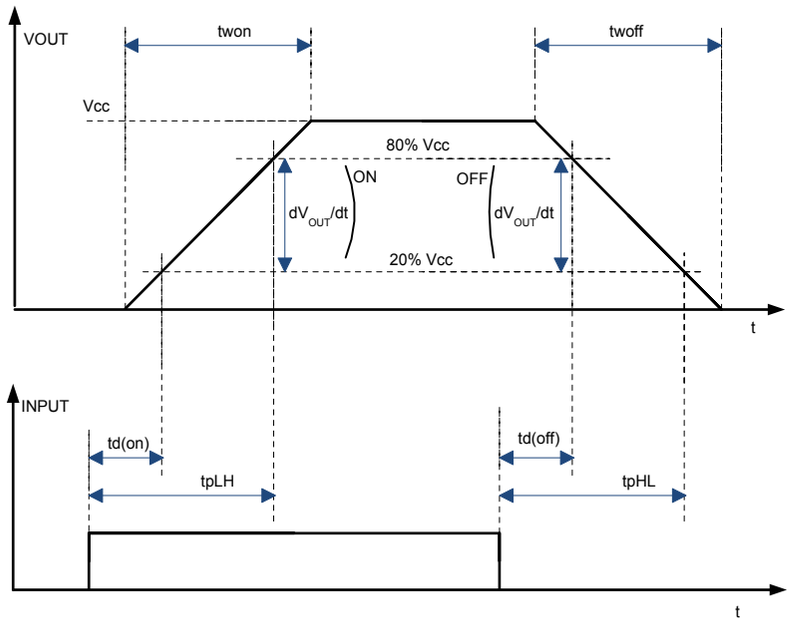
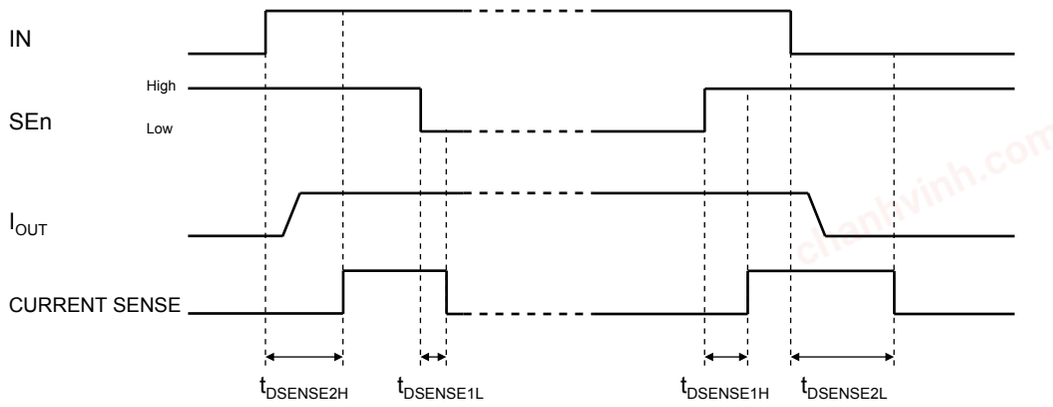


Figure 5. **Current Sense timings (current sense mode)**



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Figure 6. T_{DSTKON}

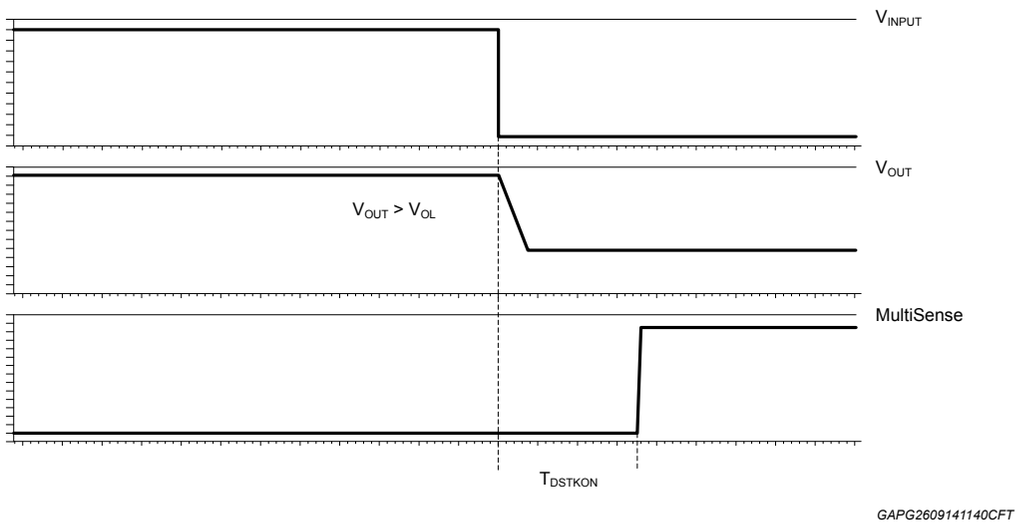


Table 10. **Truth table**

Mode	Conditions	IN_X	FR	SEn	SEL_X	OUT_X	CS	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150 °C	L	X	See (1)		L	See (1)	
		H	L			H		Outputs configured for auto-restart
		H	H			H		Outputs configured for Latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j_SD}$	L	X	See (1)		L	See (1)	
		H	L			H		Output cycles with temperature hysteresis
		H	H			L		Output latches-off
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD}$ + $V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	See (1)		H	See (1)	
	Open-load	L	X			H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	See (1)		< 0 V	See (1)	

1. *Refer to Table 11. Current sense multiplexer addressing*

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Table 11. **Current sense multiplexer addressing**

SEn	SEL_1	SEL_0	MUX channel	CS output			
				Normal mode	Overload	OFF-state diag.	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0 diagnostic	I_{SENSE} = 1/K * I_{OUT0}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H	Channel 1 diagnostic	I_{SENSE} = 1/K * I_{OUT1}			
H	H	L	Channel 2 diagnostic	I_{SENSE} = 1/K * I_{OUT2}			
H	H	H	Channel 3 diagnostic	I_{SENSE} = 1/K * I_{OUT3}			

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2.4 Waveforms

Figure 7. **Latch-off mode - Intermittent short circuit**

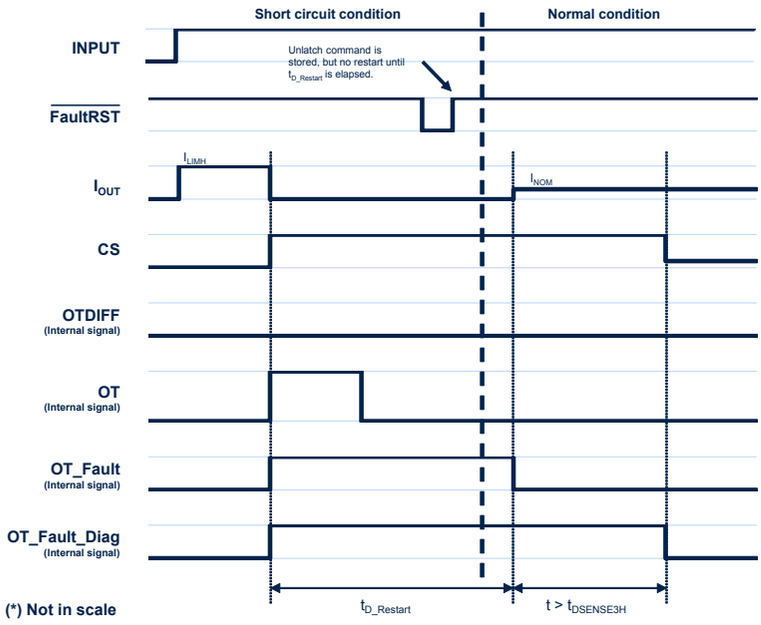
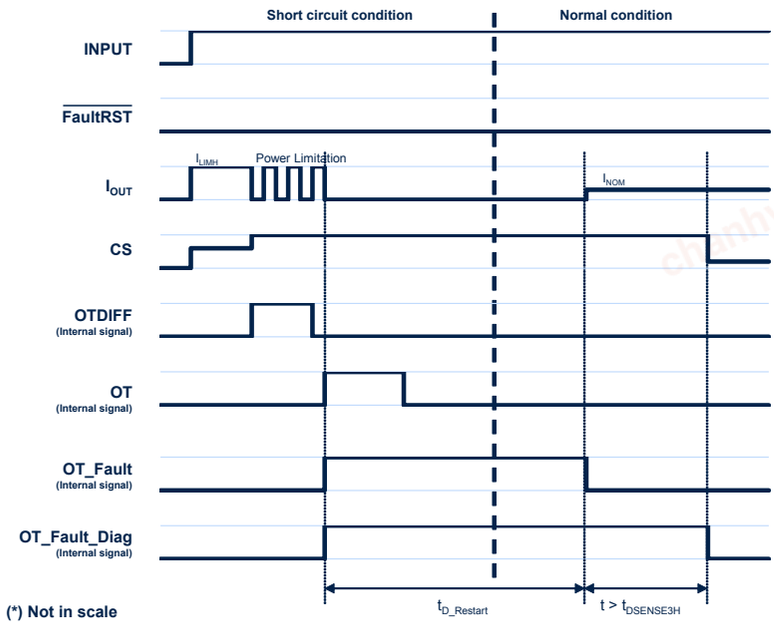


Figure 8. **Auto-restart mode - Intermittent short circuit**



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Figure 9. **Auto-restart mode - Permanent short circuit**

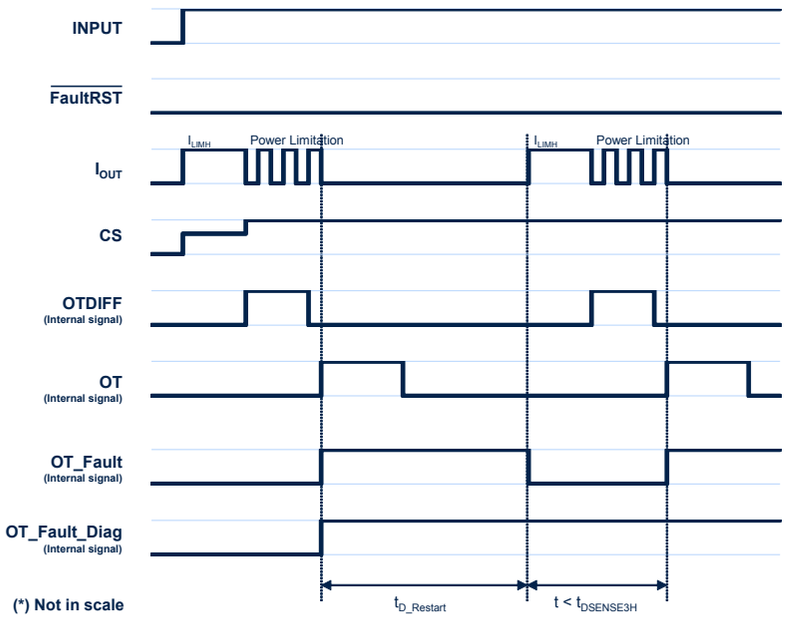


Figure 10. **Standby mode activation**

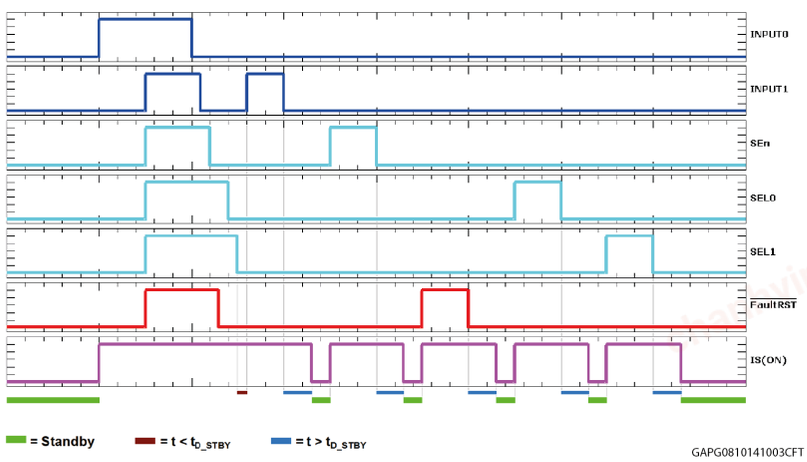
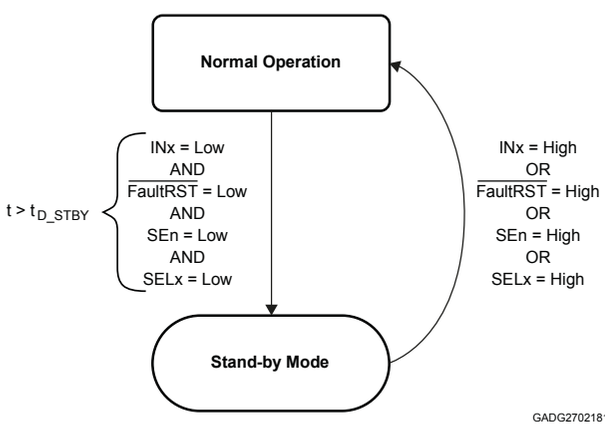


Figure 11. **Standby state diagram**



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3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_J through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_J exceeds the safety level of ΔT_{J_SD}. According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled ($\overline{\text{FaultRST}}$ = Low) or remains off ($\overline{\text{FaultRST}}$ = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the device switches on again as soon as its junction temperature drops to T_R ($\overline{\text{FaultRST}}$ = Low) or remains off ($\overline{\text{FaultRST}}$ = High).

3.3 Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

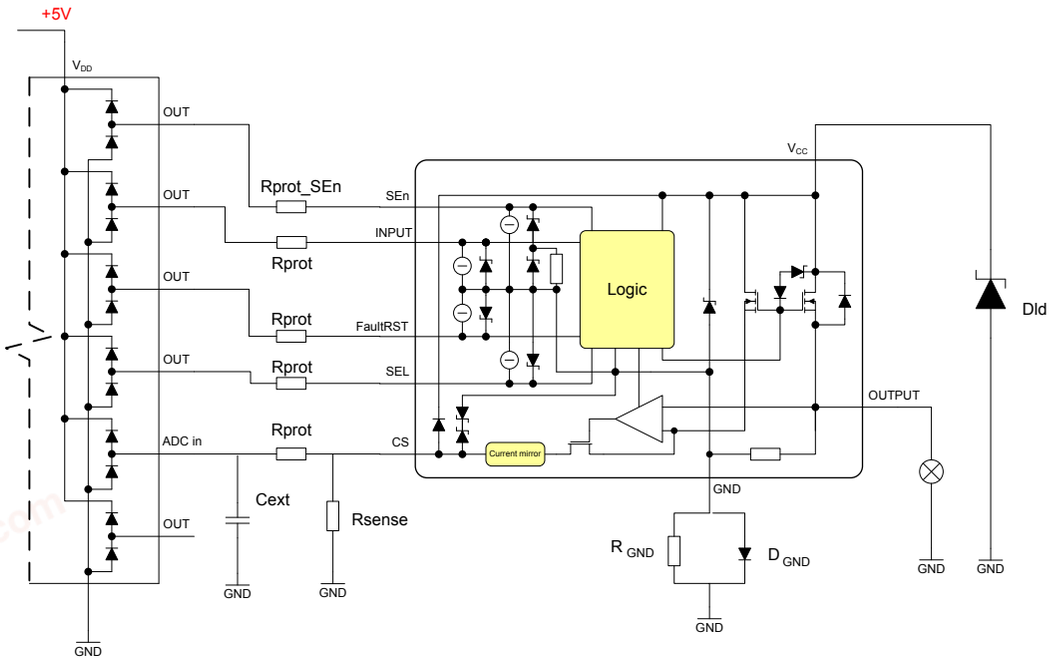
3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

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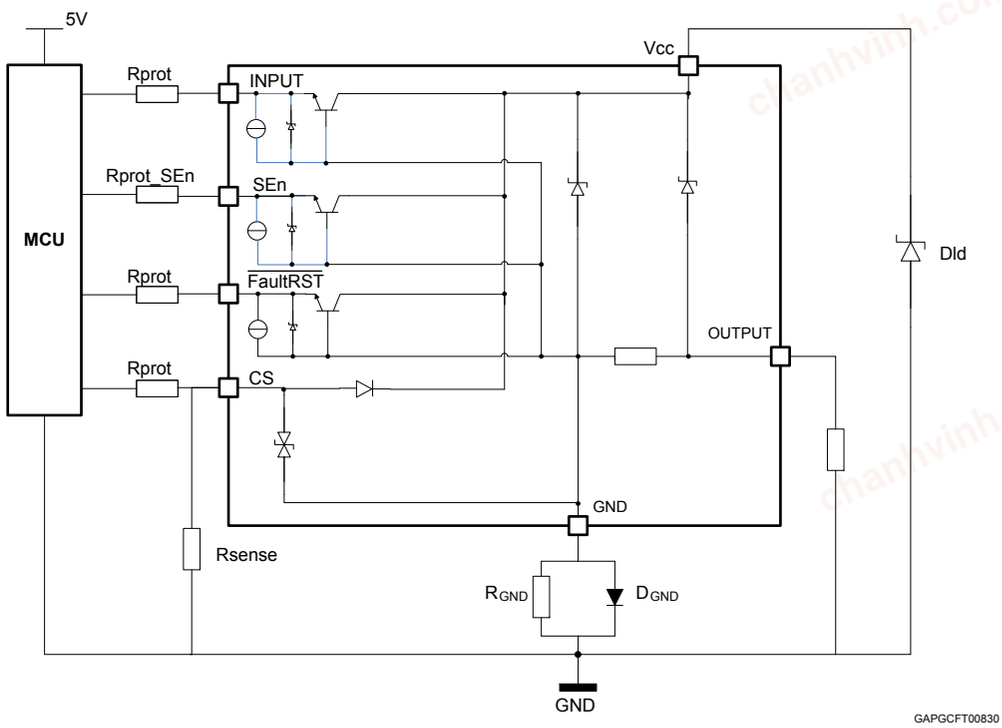
4 Application information

Figure 12. **Application diagram**



4.1 GND protection network against reverse battery

Figure 13. **Simplified internal structure**



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4.1.1 Diode (DGND) in the ground line

A resistor (typ. R_{GND} = 4.7 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in Table 12. ISO 7637-2 - electrical transient conduction along supply line.

Test pulses are applied directly to DUT (device under uest) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4.

The DUT is intended as the current device only, with external components as shown in Figure 14. M0-9 application schematic.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

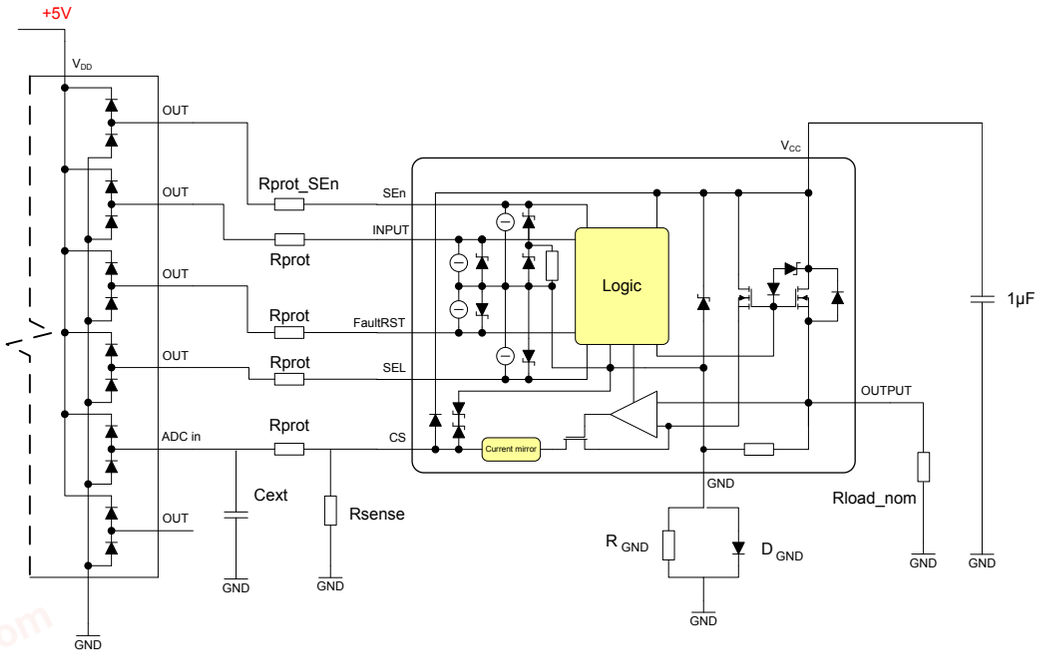
Table 12. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S (1)		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4 (2)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B (3)		35 V	5 pulse	1 min		400 ms, 2 Ω

1. *U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.*
2. *Test pulse from ISO 7637-2:2004(E).*
3. *With 35 V external suppressor referred to ground (-40°C < T_j < 150 °C).*

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Figure 14. **M0-9 application schematic**



Note: In case of multiple channels, each OUTPUT must be connected to the resistive nominal load.

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4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

7.5 kΩ ≤ R_{prot} ≤ 140 kΩ.

Recommended values: R_{prot} = 15 kΩ

A different value of the resistor has to be used for SEn pin, Rprot_SEn, as reported in Figure 12. Application diagram.

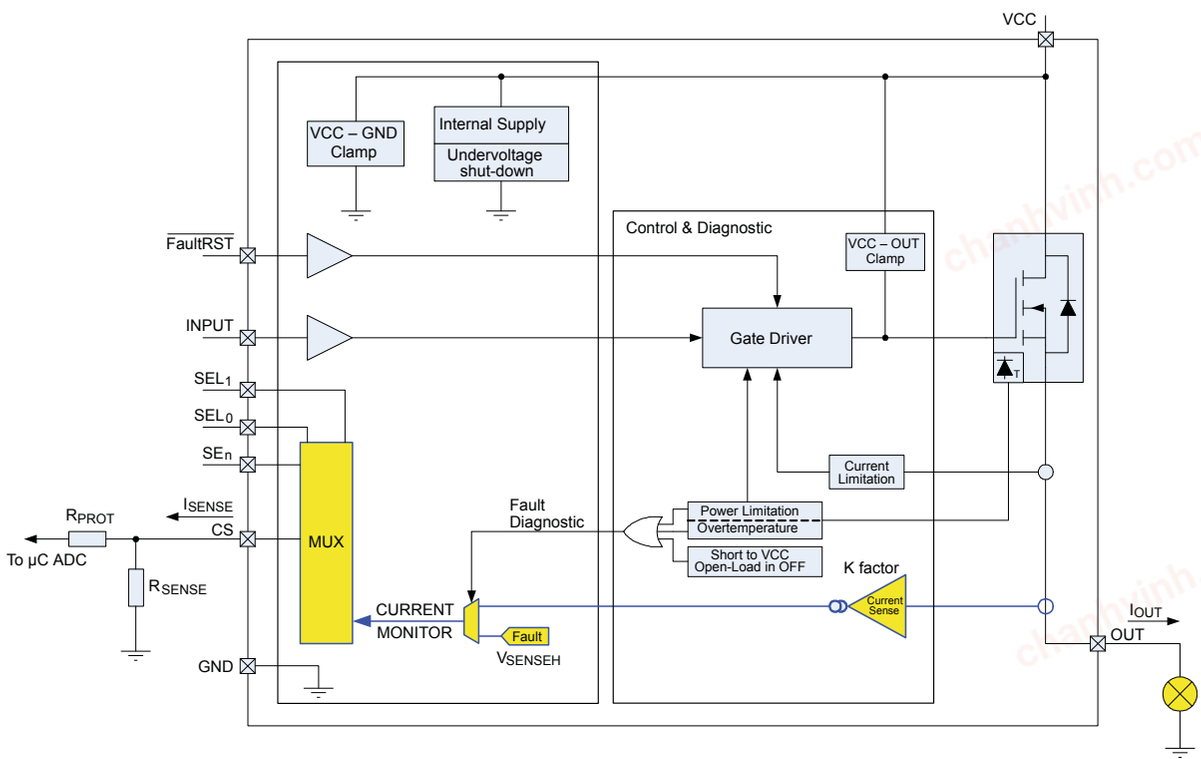
4.4 CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signals:

- Current monitor: current mirror of channel output current

Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in Table 11. Current sense multiplexer addressing.

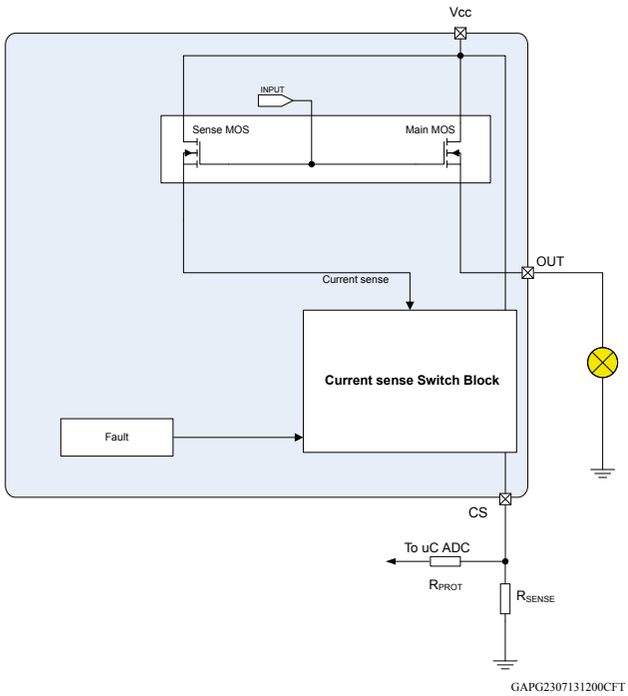
Figure 15. Current Sense and diagnostic – block diagram



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4.4.1 Principle of Current Sense signal generation

Figure 16. **Current Sense block diagram**



Current sense

The output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted into a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While the device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by CS output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on R_{SENSE} resistor
- I_{SENSE} is the current provided from CS pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of the overall circuitry, specifying the ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CS pin which is switched to a “current limited” voltage source, V_{SENSEH}.

In any case, the current sourced by the CS in this condition is limited to I_{SENSEH}.

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Figure 17. **Analog HSD – open-load detection in off-state**

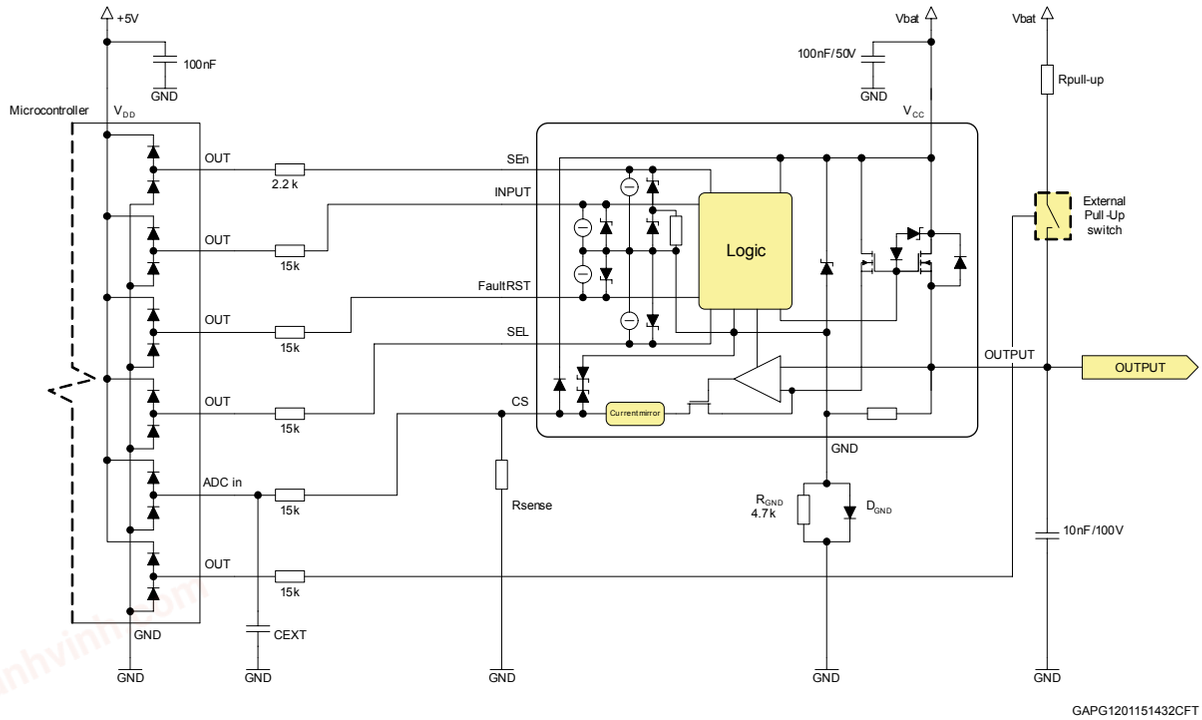
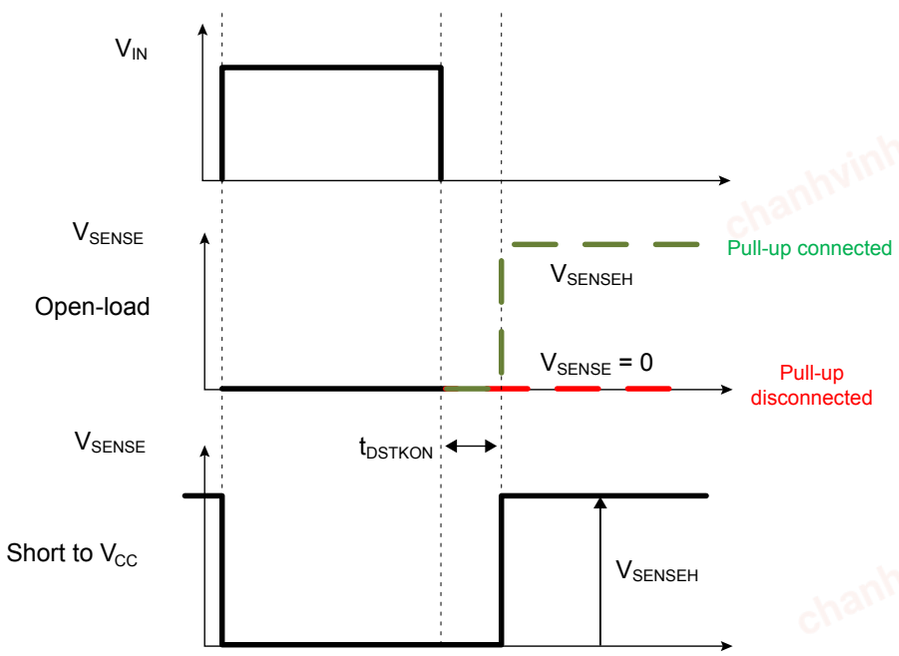


Figure 18. **Open-load / short to V_{CC} condition**



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Table 13. **Current Sense pin levels in off-state**

Condition	Output	CS	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

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5 Maximum demagnetization energy (Vcc = 16 V)

Figure 19. **Maximum turn off current versus inductance**

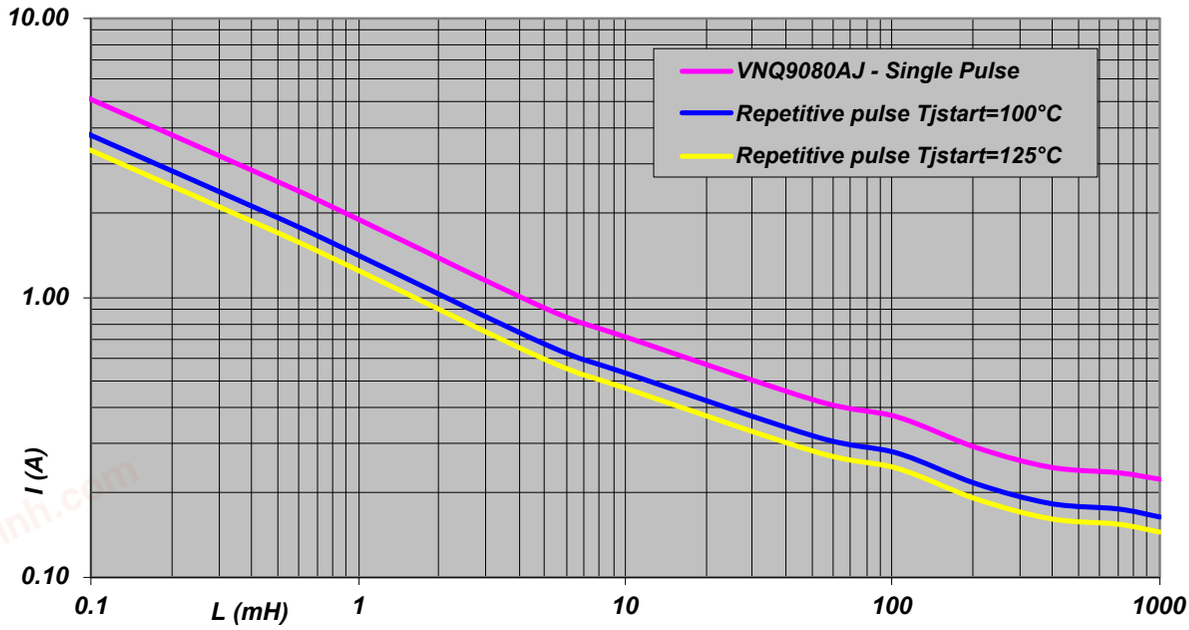
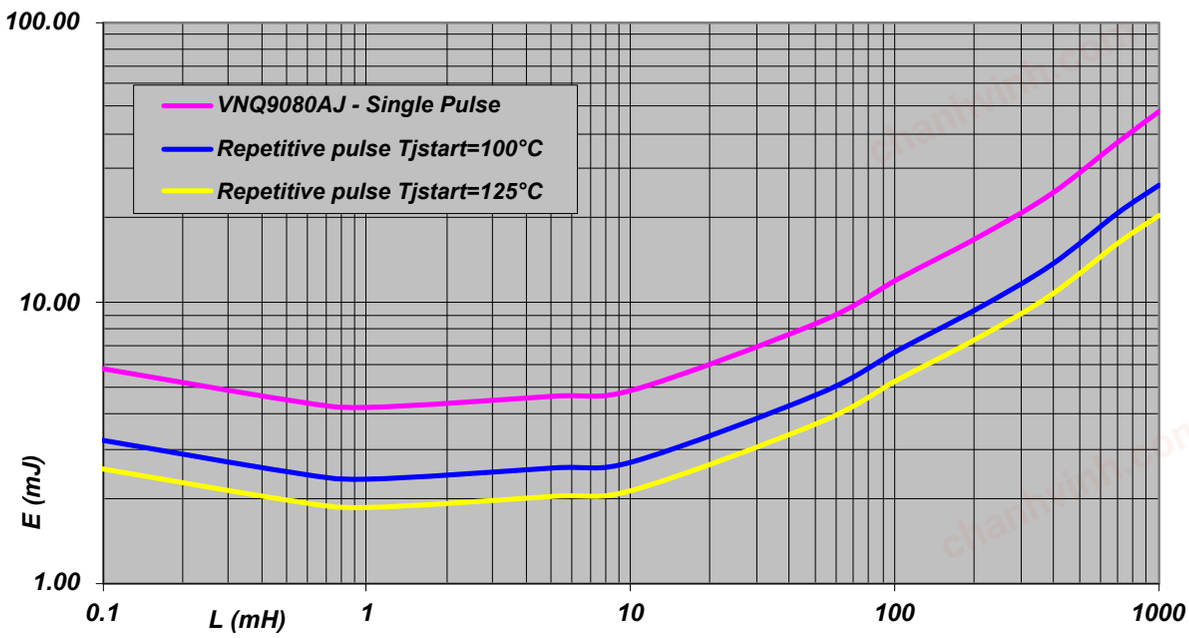


Figure 20. **Maximum turn off energy versus inductance**



Note: Values are generated with R_L = 0 Ω.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

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6 Package and PCB thermal data

6.1 PowerSSO-16 thermal data

Figure 21. **PowerSSO-16 on two-layer PCB (2s0p to JEDEC JESD 51-5)**

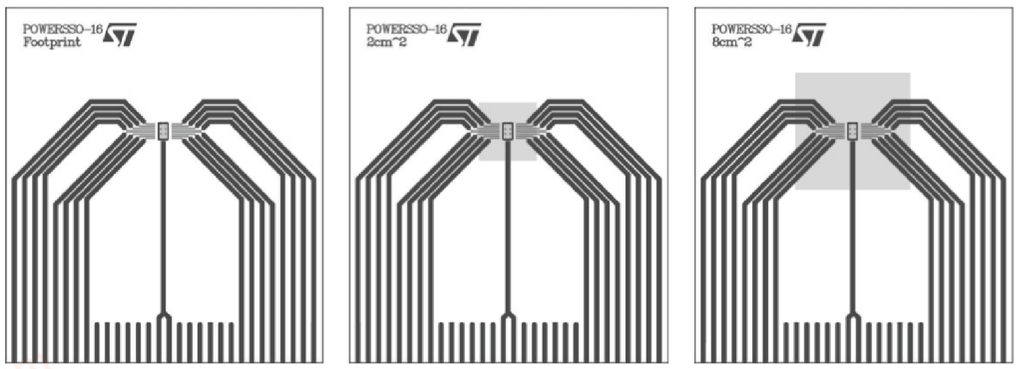


Figure 22. **PowerSSO-16 on four-layer PCB (2s2p to JEDEC JESD 51-7)**

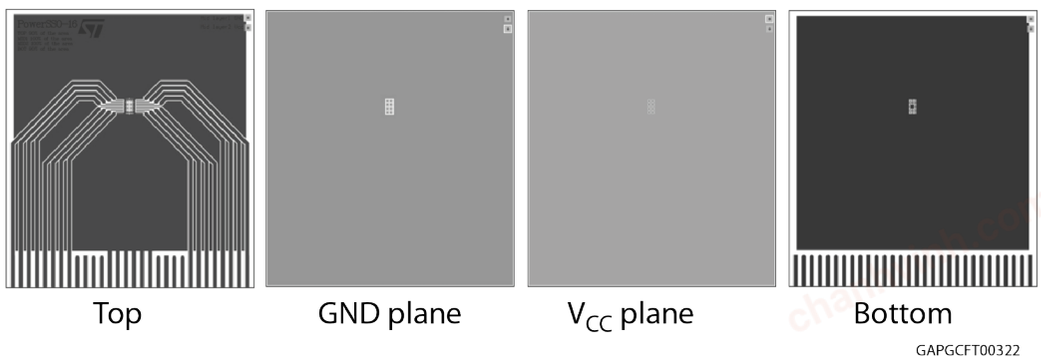


Table 14. **PCB properties**

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

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Figure 23. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

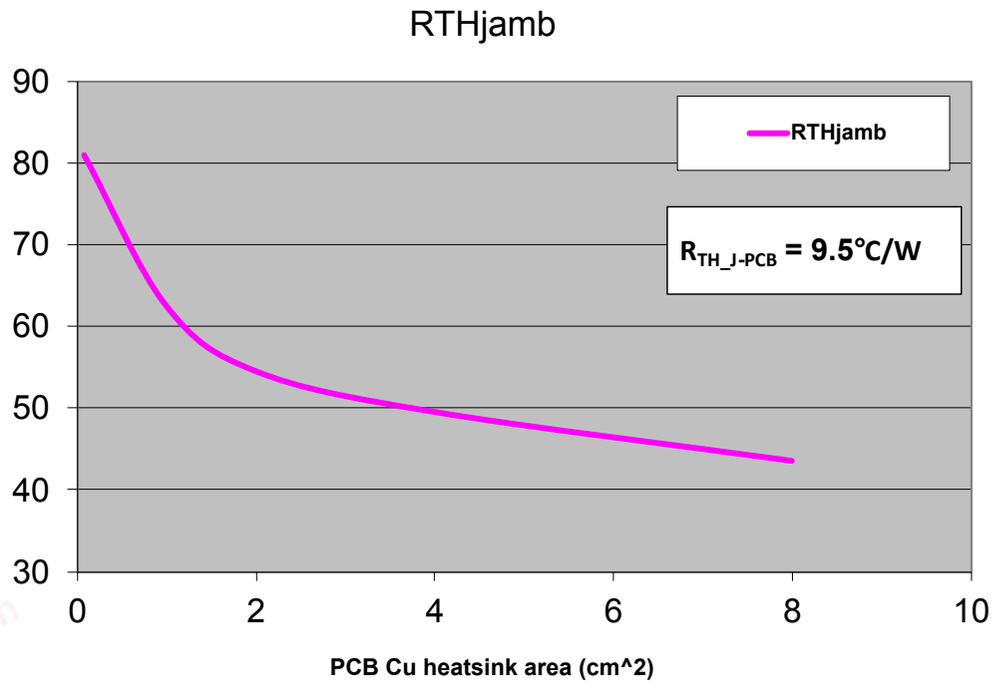
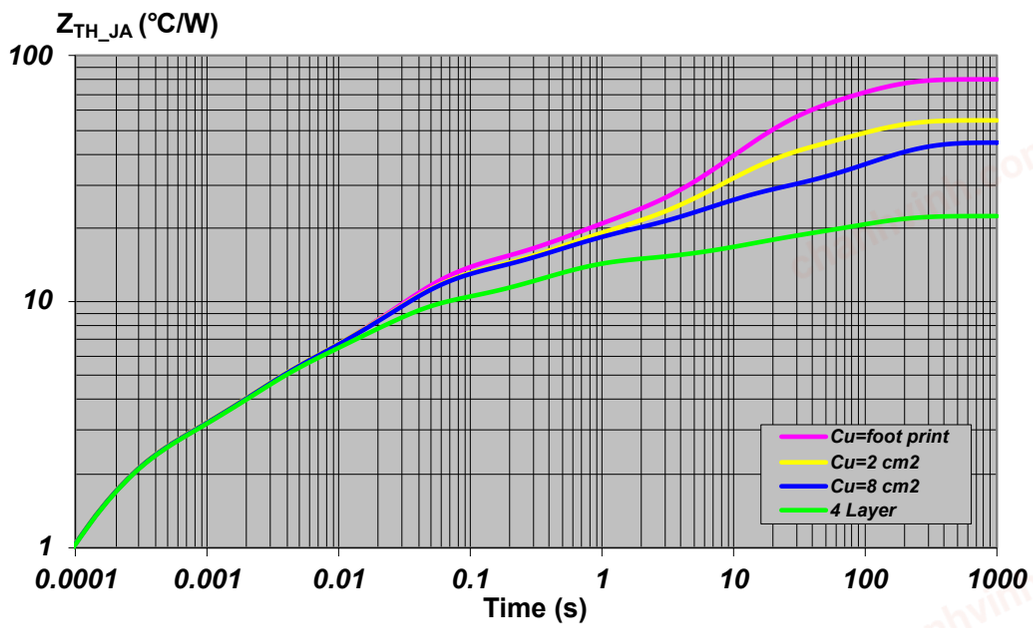


Figure 24. PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)



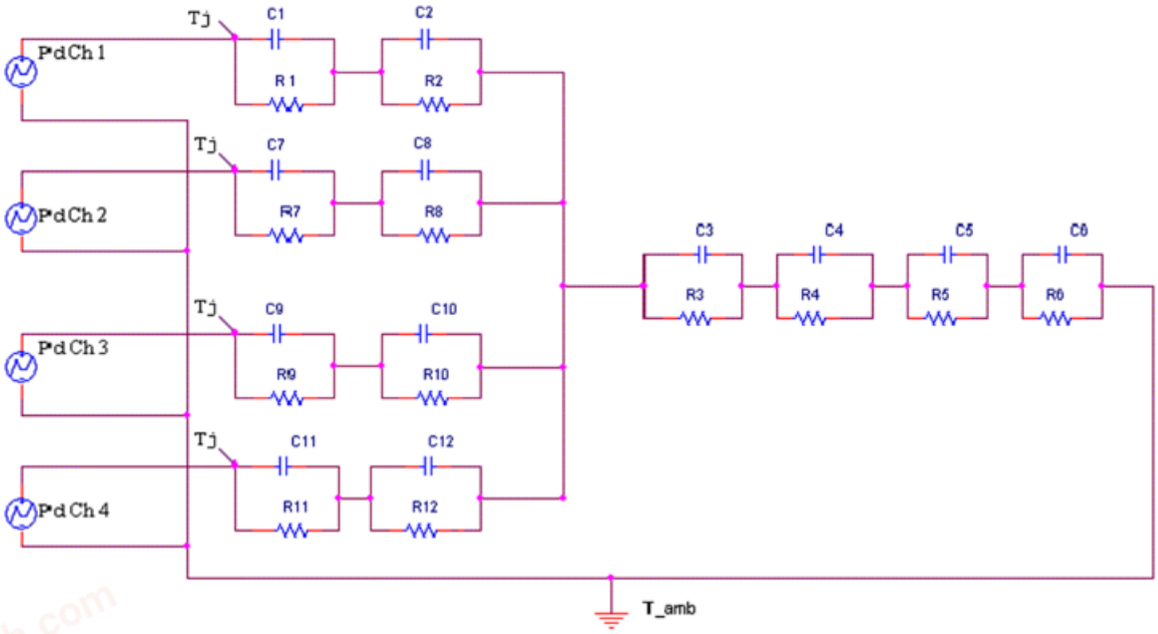
Equation: pulse calculation formula

$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$

where $\delta = t_P/T$

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Figure 25. **Thermal fitting model of a double-channel HSD in PowerSSO-16**



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. **Thermal parameters**

Area/island (cm^2)	FP	2	8	4L
R1 = R7 = R9 = R11 (°C/W)	2	-	-	-
R2 = R8 = R10 = R12 (°C/W)	2.5	-	-	-
R3 (°C/W)	6	5.5	5.5	5
R4 (°C/W)	8.5	7.5	7.5	6
R5 (°C/W)	33	19	9	3
R6 (°C/W)	29	18	18	6
C1 = C7 = C9 = C11 (W·s/°C)	0.00008	-	-	-
C2 = C8 = C10 =C12 (W·s/°C)	0.0008	-	-	-
C3 (W·s/°C)	0.08	-	-	-
C4 (W·s/°C)	0.004	0.004	0.004	0.004
C5 (W·s/°C)	0.4	0.5	0.7	3.5
C6 (W·s/°C)	3	5	7	18

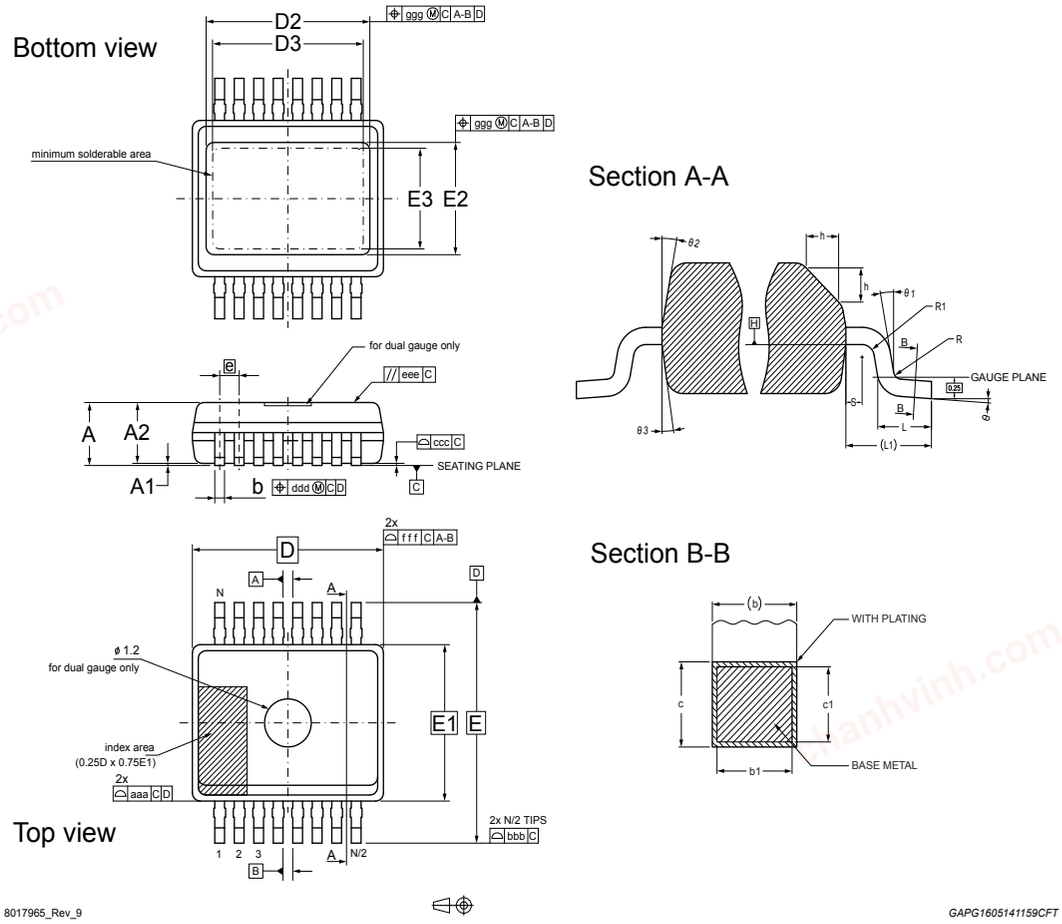
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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-16 package information

Figure 26. PowerSSO-16 package dimensions



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Table 16. **PowerSSO-16 mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	0°		
Θ2	5°		15°
Θ3	5°		15°
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D	4.90 BSC		
D2	3.31		3.91
D3	2.61		
e	0.50 BSC		
E	6.00 BSC		
E1	3.90 BSC		
E2	2.20		2.80
E3	1.49		
h	0.25		0.50
L	0.40	0.60	0.85
L1	1.00 REF		
N	16		
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.08		
eee	0.10		
fff	0.10		
ggg	0.15		

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7.2 PowerSSO-16 packing information

Figure 27. **PowerSSO-16 reel 13"**

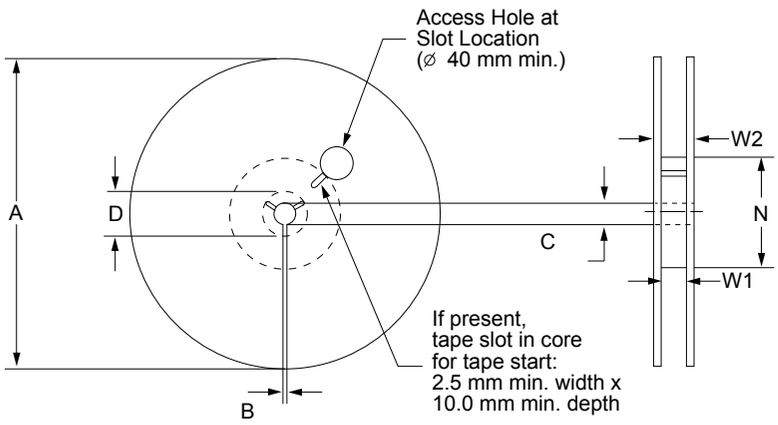


Table 17. **Reel dimensions**

Description	Value[1]
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2 /-0)	12.4
W2 (max)	18.4

1. *All dimensions are in mm.*

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Figure 28. **PowerSSO-16 carrier tape**

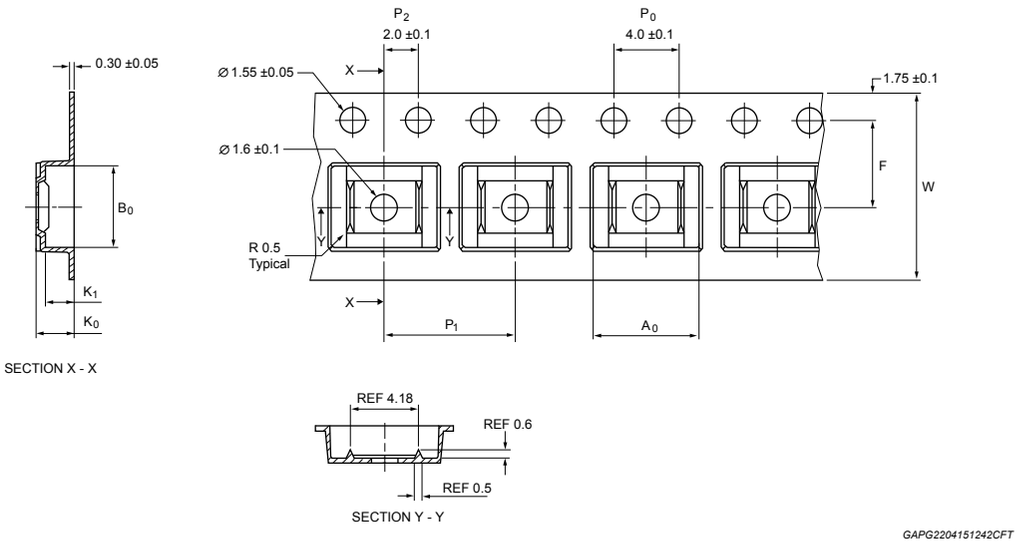
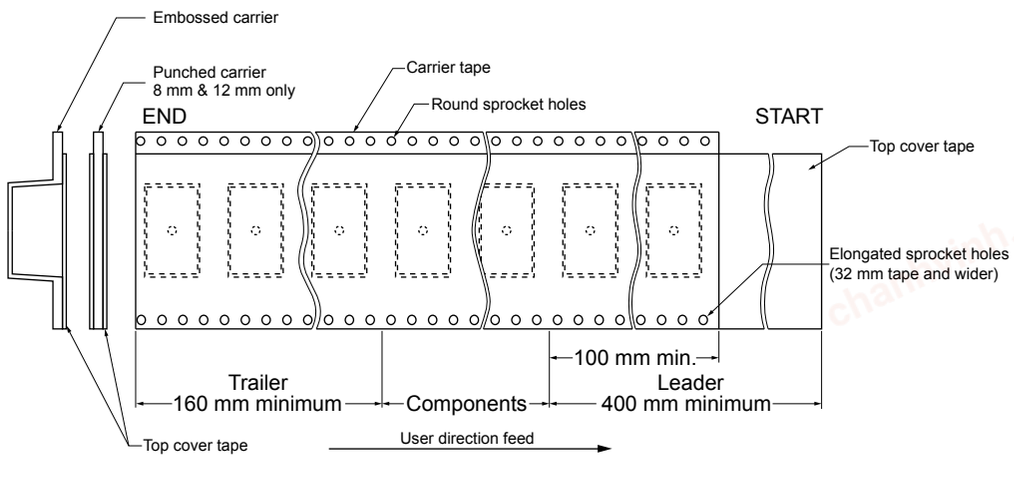


Table 18. **PowerSSO-16 carrier tape dimensions**

Description	Value(1)
A_0	6.50 ± 0.1
B_0	5.25 ± 0.1
K_0	2.10 ± 0.1
K_1	1.80 ± 0.1
F	5.50 ± 0.1
P_1	8.00 ± 0.1
W	12.00 ± 0.3

1. *All dimensions are in mm.*

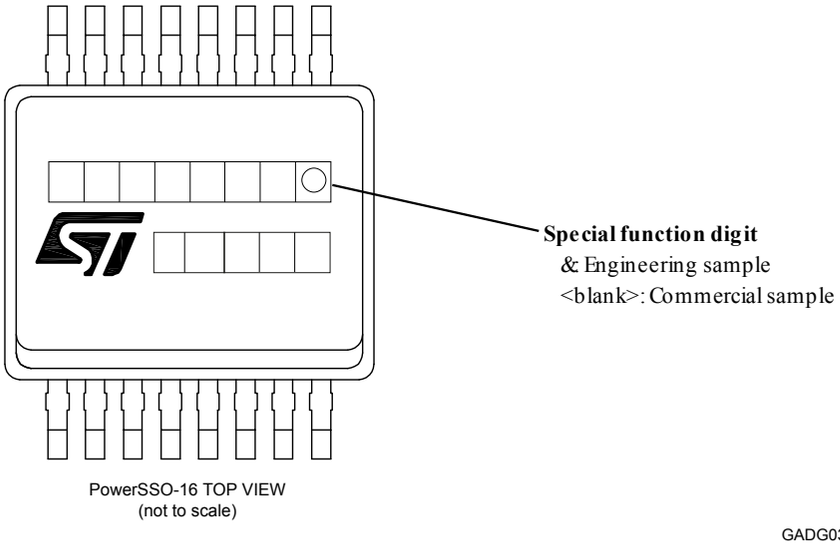
Figure 29. **PowerSSO-16 schematic drawing of leader and trailer tape**



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7.3 PowerSSO-16 marking information

Figure 30. **PowerSSO-16 marking information**



Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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Revision history

Table 19. **Document revision history**

Date	Revision	Changes
11-Sep-2018	1	Initial release.
24-Sep-2020	2	Updated cover page, *Figure 1. Block diagram*, *Table 3. Absolute maximum ratings.* Updated Main electrical characteristics, *Section 2.4 Waveforms* and *Section 3 Protections*. Added *Application information*.
17-Sep-2021	3	Added: • *Section 5 Maximum demagnetization energy (Vcc = 16 V)*; • *Section 6 Package and PCB thermal data*. Updated: • *Figure 12. Application diagram;* • *Figure 16. Analog HSD – open-load detection in off-state;* • *Table 4. Thermal data;* • *Table 6. Switching;* • *Table 9. Current Sense;* • *Section 7.1 PowerSSO-16 package information.* Minor text changes in: • *Table 3. Absolute maximum ratings;* • *Table 5. Power section.*
26-Jan-2022	4	Updated features list in cover page. Updated Table 8. Protections and Table 9. Current Sense. Updated Figure 12. Application diagram, Figure 13. Simplified internal structure, Section 4.2 Immunity against transient electrical disturbances and Section 4.3 MCU I/Os protection.

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