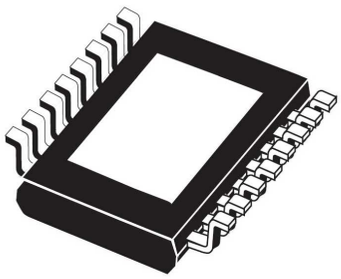
chanhvinh.com

life.augmented

VN9016AJ

Datasheet

Single channel high-side driver with current sense analog feedback for automotive applications



PowerSSO-16

Product status link
VN9016AJ

Product summary	
Order code	VN9016AJTR
Package	PowerSSO-16
Packing	Tape and reel

Features

Max. transient supply voltage	V_{CC}	36 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per channel)	R_{ON}	16 mΩ
Current limitation (typ.)	I_{LIMH}	50.6 A
Standby current (max.)	I_{STBY}	0.5 µA

- AEC-Q100 qualified
- Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
- General
  - Single channel smart high-side driver with current sense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- Current sense diagnostic functions
  - Multiplexed analog feedback of load current with high precision proportional current mirror
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection (with external pull-up)
  - Output short to V_{CC} detection
  - Sense enable/disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery through self turn-on
  - Electrostatic discharge protection

Applications

- Automotive resistive, inductive and capacitive loads
- Protected supply for ADAS systems: radars and sensors

chanhvinh.com

Description

The VN9016AJ is a single channel high-side driver manufactured using ST proprietary VIPower M0-9 technology and housed in a PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

chanhvinh.com

1 Block diagram and pin description

Figure 1. Block diagram

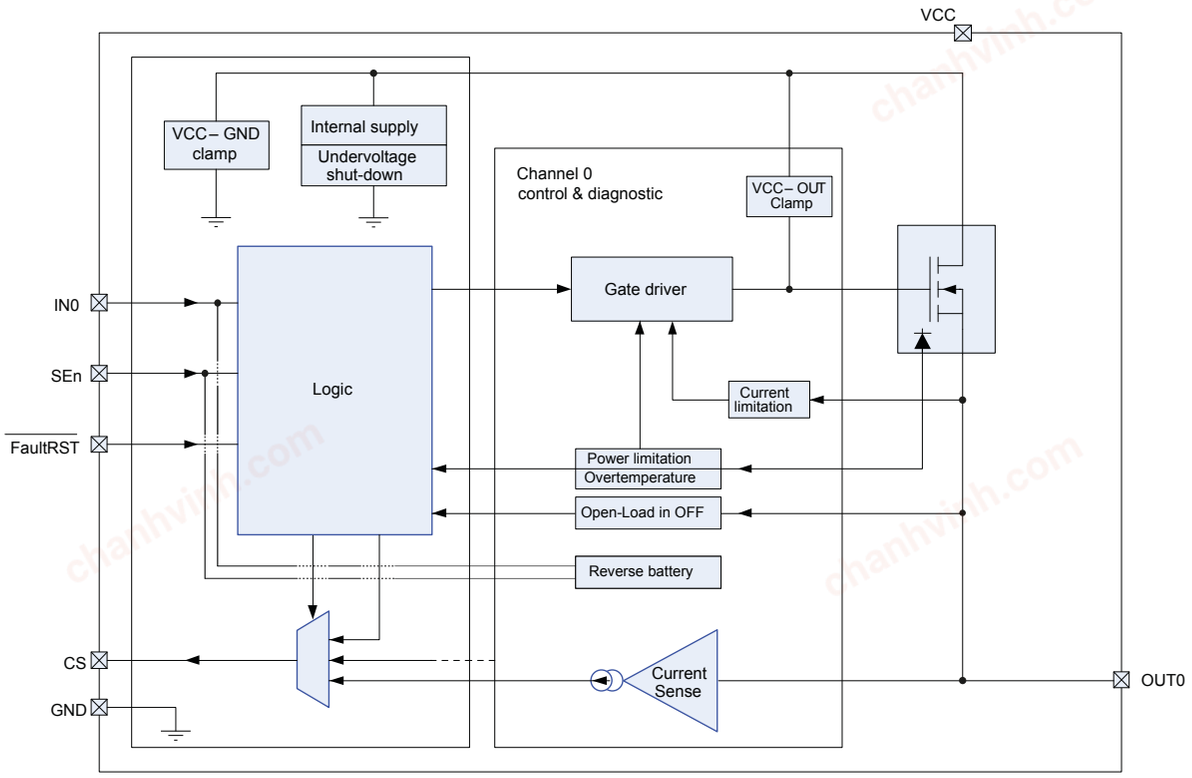


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_0$	Power outputs.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
$INPUT_0$	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
CS	Multiplexed analog sense output pin; it delivers a current proportional to the selected load current.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the CS diagnostic pin.
$\overline{FaultRST}$	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

chanhvinh.com

Figure 2. **Configuration diagram (top view)**

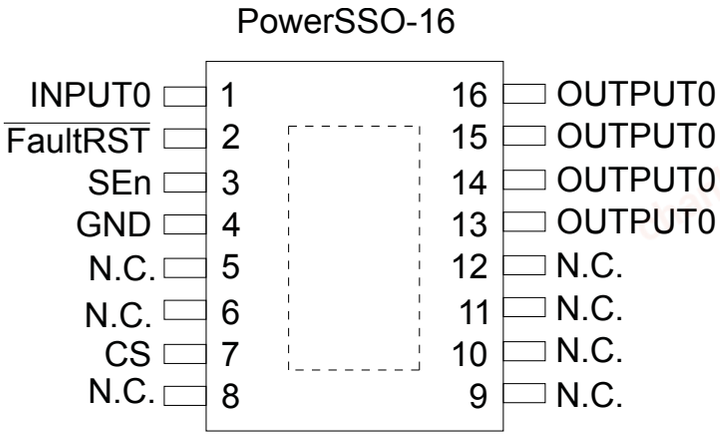


Table 2. **Suggested connections for unused and not connected pins**

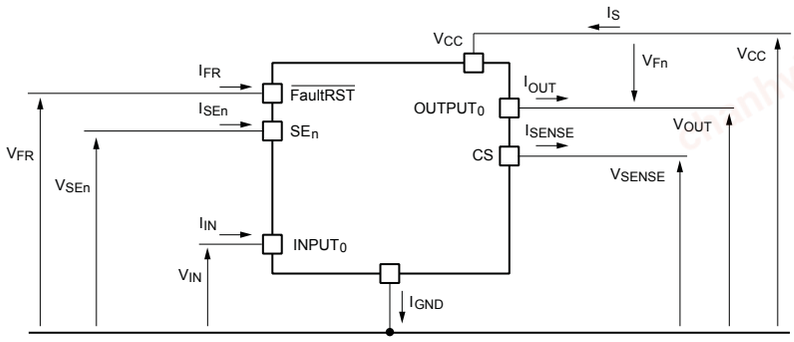
Connection/pin	CS	NC	Output	Input	SEn, $\overline{\text{FaultRST}}$
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. *X: do not care.*

chanhvinh.com

2 Electrical specification

Figure 3. **Current and voltage conventions**



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 3. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect the device reliability.

Table 3. **Absolute maximum ratings**

Symbol	Parameter		Value	Unit
V_{CC}	DC supply voltage		36	V
$-V_{CC}$	Reverse DC supply voltage		16	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection		28	V
$-I_{GND}$	DC reverse ground pin current		200	mA
I_{OUT}	$OUTPUT_0$ DC output current		Internally limited	A
$-I_{OUT}$	Reverse DC output current		13	A
I_{IN}	$INPUT_0$ DC input current		-1 to 10	mA
I_{SEn}	SEn DC input current		-1 to 3	mA
I_{FR}	$\overline{FaultRST}$ DC input current		-1 to 10	mA
I_{SENSE}	CS pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)		10	mA
	CS pin DC output current in reverse ($V_{CC} < 0$ V)		-20	
E_{MAX}	Maximum switching energy single pulse (T_{Jstart} = 150 °C)		16	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)	$INPUT_0$	2000	V
		CS	2000	
		SEn, $\overline{FaultRST}$	2000	
		$OUTPUT_0$	4000	
		V_{CC}	4000	
	Charge device model (CDM-AEC-Q100-011)		750	
T_J	Operating junction temperature range		-40 to 150	°C
T_{stg}	Storage temperature range		-55 to 150	°C

chanhvinh.com

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
R_{thJB}	Thermal resistance, junction-to-board (JEDEC JESD 51-5 / 51-8)(1)	7	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient (JEDEC JESD 51-5)(2)	53.6	°C/W
	Thermal resistance, junction-to-ambient (JEDEC JESD 51-7)(1)	22	°C/W

1. *Device mounted on four-layer 2s2p PCB.*
2. *Device mounted on two-layer 2s0p PCB with 2 cm^2 heatsink copper trace.*

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_J < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_J = 25 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown			2.1	2.7	V
$V_{USDReset}$	Undervoltage shutdown reset				4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.15		V
R_{ON}	On-state resistance	I_{OUT} = 3.7 A; T_J = 25 °C		16		mΩ
		I_{OUT} = 3.7 A; T_J = 150 °C			35.2	
		I_{OUT} = 3.7 A; V_{CC} = 4 V; T_J = 25 °C			27.2	
		I_{OUT} = 1 A; V_{CC} = 2.7 V; V_{CC} decreasing			96	
R_{ON_Rev}	R_{DSON} in reverse battery condition	V_{CC} = -13 V; I_{OUT} = -3.7 A; T_J = 25 °C		16		mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA; 25 °C < T_J < 150 °C	36	38	45	V
		I_S = 20 mA; T_J = -40 °C	36			
I_{STBY}	Supply current in standby at V_{CC} = 13 V(1)	V_{CC} = 13 V; T_J = 25 °C; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V;			0.5	µA
		V_{CC} = 13 V; T_J = 85 °C(2) V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V;			0.5	
		V_{CC} = 13 V; T_J = 125 °C V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V;			3	
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = 0 V; V_{SEn} = 5 V to 0 V	60	260	550	µs
$I_{S(ON)}$	Supply current at V_{CC} = 13 V	V_{CC} = 13 V; V_{SEn} = V_{FR} = 0 V; V_{IN0} = 5 V; I_{OUT0} = 0 A		1.6	2.5	mA
$I_{GND(ON)}$	Control stage current consumption in ON-state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = 0 V; V_{IN0} = 5 V; I_{OUT0} = 3.7 A			3	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V(1)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_J = 25 °C	0	0.01	0.5	µA

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V(1)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_J = 125 °C	0		3	µA
V_F	Output - V_{CC} diode voltage at T_J = 150 °C	I_{OUT} = -3.7 A; T_J = 150 °C			0.7	V

1. *Power MOSFET leakage included.*
2. *Parameter specified by design, not tested in production.*

Table 6. Switching

V_{CC} = 13 V; -40 °C < T_J < 150 °C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{d(on)}$(1)	Turn-on delay time at T_J = 25 °C	R_L = 3.5 Ω	10	30	120	µs
$t_{d(off)}$(1)	Turn-off delay time at T_J = 25 °C		10	25	100	µs
$(dV_{OUT}/dt)_{on}$(1)	Turn-on voltage slope at T_J = 25 °C	R_L = 3.5 Ω	0.2	0.5	0.7	V/µs
$(dV_{OUT}/dt)_{off}$(1)	Turn-off voltage slope at T_J = 25 °C	R_L = 3.5 Ω	0.2	0.6	0.9	V/µs
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 3.5 Ω		0.2	0.85(2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 3.5 Ω		0.25	0.55(2)	mJ
t_{SKEW}(1)	Differential Pulse skew (t_{PHL} - t_{PLH})	R_L = 3.5 Ω	-60	-10	40	µs

1. *See Figure 4. Switching time and pulse skew.*
2. *Parameter guaranteed by design and characterization; not subject to production test.*

Table 7. Logic inputs

7 V < V_{CC} < 28 V; -40 °C < T_J < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
INPUT$_0$ characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	6		8.5	V
		I_{IN} = -1 mA		-0.7		
$\overline{\text{FaultRST}}$ characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	6		8.5	V
		I_{IN} = -1 mA		-0.7		

chanhvinh.com

7 V < V_{CC} < 28 V; -40 °C < T_J < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{SEn} = 1 mA	9		12	V
		I_{SEn} = -1 mA		-0.7		

Table 8. Protections

7 V < V_{CC} < 18 V; -40 °C < T_J < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LIMH}(1)	DC short-circuit current	V_{CC} = 16 V; T_J = -40 °C	-15%	55	15%	A
		V_{CC} = 16 V; T_J = 150 °C	-15%	43.5	15%	
I_{LIMH2}(2)		V_{CC} = 19 V; T_J = -40 °C	-15%	43	15%	
		V_{CC} = 19 V; T_J = 150 °C	-15%	33.7	15%	
I_{LIMH} at 22 V		V_{CC} = 22 V; T_J = 25 °C		14.5		
T_{TSD}	Shutdown temperature		150	175	210	°C
	Shutdown temperature (V_{CC} decreasing)	V_{CC} = 2.7 V	140			
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V	135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_{RS}) (3)			7		°C
ΔT_{J_SD}	Dynamic temperature	V_{CC} = 16 V		80		K
		V_{CC} = 19 V		55		K
t_{LATCH_RST}	Fault reset time for output unlatch(3)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; V_{IN0} = 5 V	3	10	20	µs
$t_{D_Restart}$	Latch-OFF delay time before automatic restart			50	75	ms
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 1 A; L = 6 mH; T_J = -40 °C	V_{CC} - 36			V
		I_{OUT} = 1 A; L = 6 mH; T_J = 25 °C to 150 °C	V_{CC} - 36	V_{CC} - 38	V_{CC} - 45	

1. *I_{LIMH}, guaranteed between 7 V and 16 V, -40 °C < T_J < 150 °C.*
2. *I_{LIMH2}, guaranteed between 16 V and 19 V, -40 °C < T_J < 150 °C.*
3. *Parameter specified by design and evaluated by characterization, not tested in production.*

chanhvinh.com

Table 9. Current sense

7 V < V_{CC} < 18 V; -40 °C < T_J < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{SENSE_CL}	CS clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-9	-8	-7	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		
Current sense characteristics						
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-35%	8390	+35%	
dK_{LED}/K_{LED} (1) (2)	Current sense ratio drift	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-20%	8390	20%	
dK_0/K_0 (1) (2)	Current sense ratio drift	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-15		15	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.7 A; V_{SENSE} = 3.5 V; V_{SEn} = 5 V	-15%	8390	15%	
dK_1/K_1 (1) (2)	Current sense ratio drift	I_{OUT} = 0.7 A; V_{SENSE} = 3.5 V; V_{SEn} = 5 V	-10		10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 3.7 A; V_{SENSE} = 3.5 V; V_{SEn} = 5 V	-7%	8390	7%	
dK_2/K_2 (1) (2)	Current sense ratio drift	I_{OUT} = 3.7 A; V_{SENSE} = 3.5 V; V_{SEn} = 5 V	-7		7	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 11 A; V_{SENSE} = 3.5 V; V_{SEn} = 5 V	-5%	8390	5%	
dK_3/K_3 (1) (2)	Current sense ratio drift	I_{OUT} = 11 A; V_{SENSE} = 3.5 V; V_{SEn} = 5 V	-5		5	%
I_{SENSE0}	Current sense leakage current	CS disabled: V_{SEn} = 0 V	0		0.5	µA
		CS disabled: -1 V < V_{SENSE} < 5 V (1)	-1		1	
		CS enabled: V_{SEn} = 5 V; Channel ON: V_{IN0} = 5 V; I_{OUT0} = 0 A;	0		10	
		CS enabled: V_{SEn} = 5 V; Channel OFF: V_{IN0} = 0 V; I_{OUT0} = 0 A	0		1	
V_{OUT_MSD} (1)	Output voltage for CS shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ; V_{IN0} = 5 V; I_{OUT0} = 3.7 A		5		V
V_{SENSE_SAT}	CS saturation voltage	V_{CC} = 7 V; R_{SENSE} = 10 kΩ; V_{SEn} = 5 V; V_{IN0} = 5 V; I_{OUT0} = 11 A; T_J = -40 °C	4.8			V
I_{SENSE_SAT} (1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 3.5 V; V_{IN0} = 5 V; V_{SEn} = 5 V; T_J = 150 °C	2			mA
I_{OUT_SAT} (1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 3.5 V; V_{IN0} = 5 V; V_{SEn} = 5 V; T_J = 150 °C	22			A

chanhvinh.com

7 V < V_{CC} < 18 V; -40 °C < T_J < 150 °C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	V_{SEn} = 5 V; Ch OFF; V_{IN0} = 0 V;	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_J = -40 °C to 125 °C	-150	-40	-5	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 6. T_{DSTKON})	V_{SEn} = 5 V; Ch ON to OFF transition; V_{IN0} = 5 V to 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	100	170	250	µs
$t_{D_OL_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN} = 0 V; V_{FR} = 0 V; V_{OUT0} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{SEn} = 5 V; Ch OFF; V_{IN0} = 0 V; V_{OUT} = 0 V to 4 V		5	30	µs
Fault diagnostic feedback (see Table 10. Truth table)						
V_{SENSEH}	Multisense output voltage in fault condition	13 V < V_{CC} < 18 V; Ch0 in open load; R_{SENSE} = 0.7 kΩ; V_{IN0} = 0 V; V_{SEn} = 5 V; I_{OUT0} = 0 A; V_{OUT0} = 4 V	5		7.5	V
		V_{CC} = 7 V; Ch0 in open load; R_{SENSE} = 0.7 kΩ; V_{IN0} = 0 V; V_{SEn} = 5 V; I_{OUT0} = 0 A; V_{OUT0} = 4 V	4.3			
I_{SENSEH}	Current sense output current in fault condition	13 V < V_{CC} < 18 V; V_{SENSE} = 5 V; Ch0 in open load; V_{IN0} = 0 V; V_{SEn} = 5 V; I_{OUT0} = 0 A; V_{OUT0} = 4 V	7	8.6	12	mA
		V_{CC} = 7 V; V_{SENSE} = 5 V; Ch0 in open load; V_{IN0} = 0 V; V_{SEn} = 5 V; I_{OUT0} = 0 A; V_{OUT0} = 4 V	4.4			
Current sense timings (current sense mode - see Figure 5. Current sense timings (current sense mode))(3)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 3.5 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 3.5 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 3.5 Ω		100	200	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 3.5 Ω; I_{SENSE} = 90 % of $I_{SENSEMAX}$			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 3.5 Ω		70	250	µs

chanhvinh.com

7 V < V_{CC} < 18 V; -40 °C < T_J < 150 °C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE3H}$	Current sense latch-OFF filtering time		1.4	2.0	2.6	ms

1. *Parameter specified by design, not tested in production.*
2. *All values refer to V_{CC} = 13 V; T_J = 25 °C, unless otherwise specified.*
3. *Transition delay is measured up to ±10% of final conditions.*

Figure 4. Switching time and pulse skew

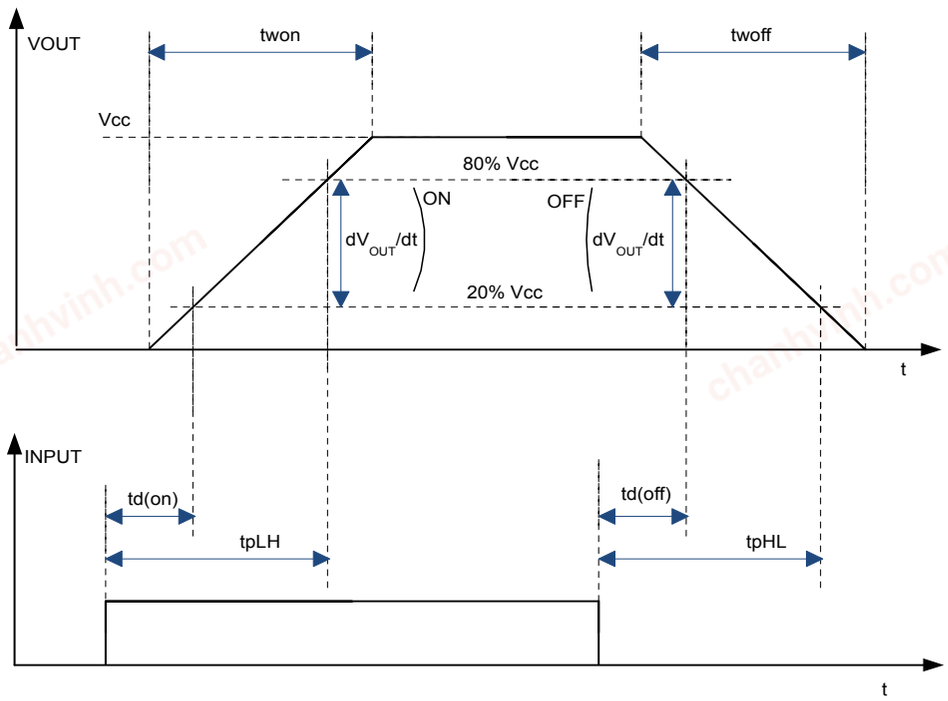
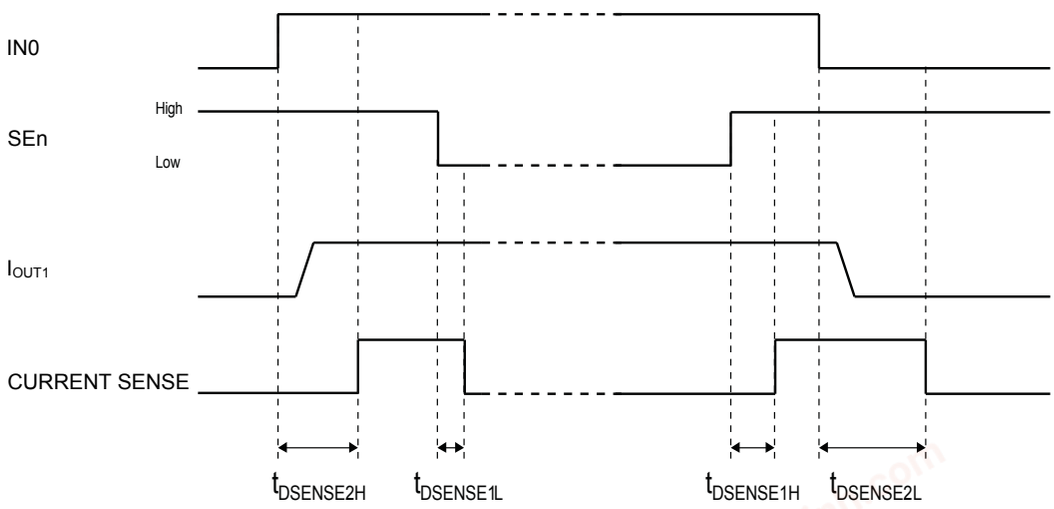


Figure 5. Current sense timings (current sense mode)



chanhvinh.com

Figure 6. T_{DSTKON}

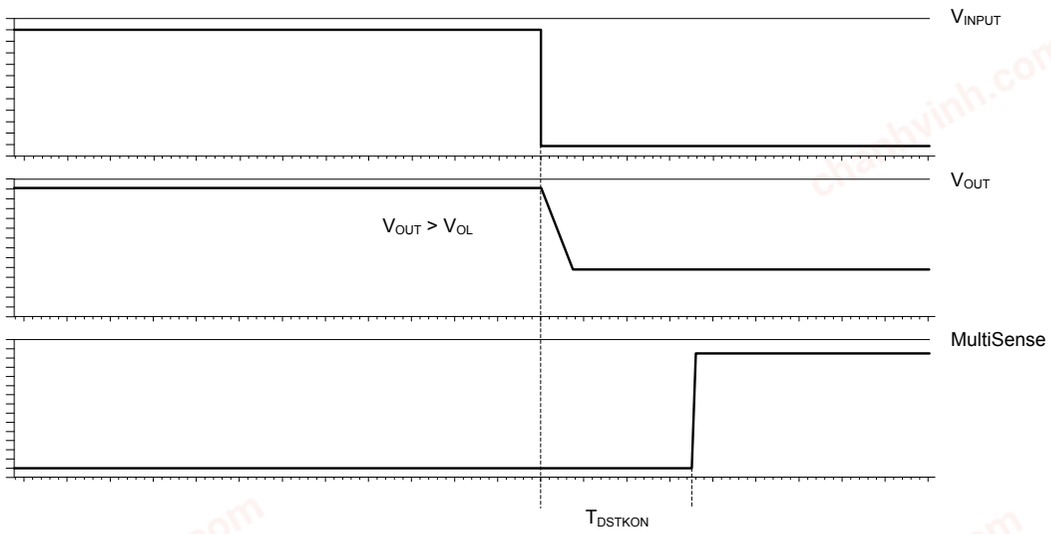


Table 10. **Truth table**

Mode	Conditions	IN_X	FR	SEn	OUT_X	CS	Comments
Standby	All logic inputs low	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_J < 150 °C	L	X	See (1)	L	See (1)	
		H	L		H	See (1)	Outputs configured for auto-restart
		H	H		H	See (1)	Outputs configured for latch-off
Overload	Overload or short to GND causing: $T_J > T_{TSD}$ or $\Delta T_J > \Delta T_{J_SD}$	L	X	See (1)	L	See (1)	
		H	L		H	See (1)	Output cycles with temperature hysteresis
		H	H		L	See (1)	Output latches-off
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	See (1)	H	See (1)	
	Open-load	L	X		H	See (1)	External pull-up
Negative output voltage	Inductive loads turn-off	L	X	See (1)	< 0 V	See (1)	

1. *Refer to Table 11. Current sense multiplexer addressing*

Table 11. **Current sense multiplexer addressing**

SEn	MUX channel	CS output			
		Normal mode	Overload	OFF-state diag.	Negative output
L		Hi-Z			
H	Channel 0 diagnostic	I_{SENSE} = 1/K * I_{OUT0}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z

chanhvinh.com

2.4 Waveforms

Figure 7. **Latch-off mode - Intermittent short circuit**

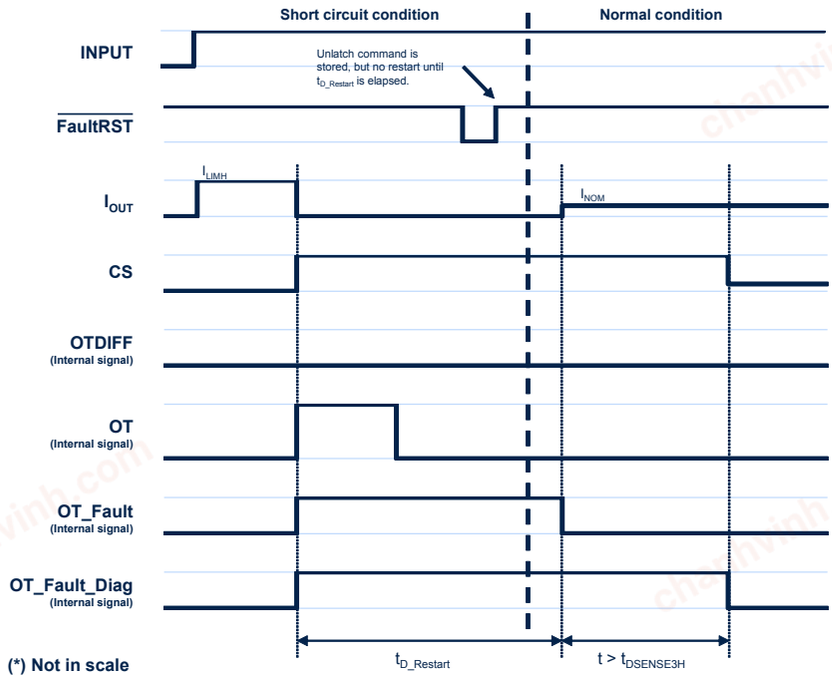
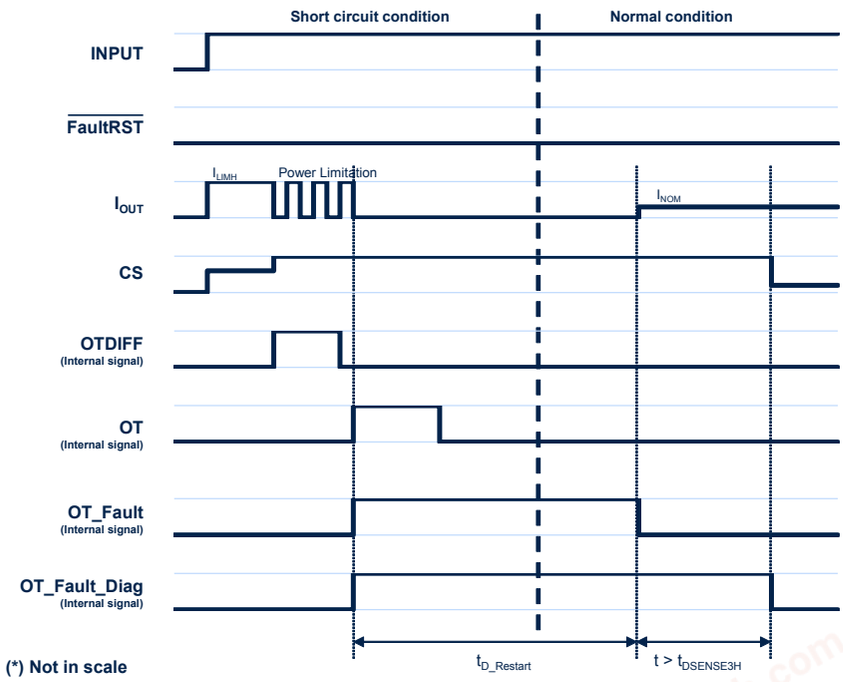


Figure 8. **Auto-restart mode - Intermittent short circuit**



chanhvinh.com

Figure 9. **Auto-restart mode - Permanent short circuit**

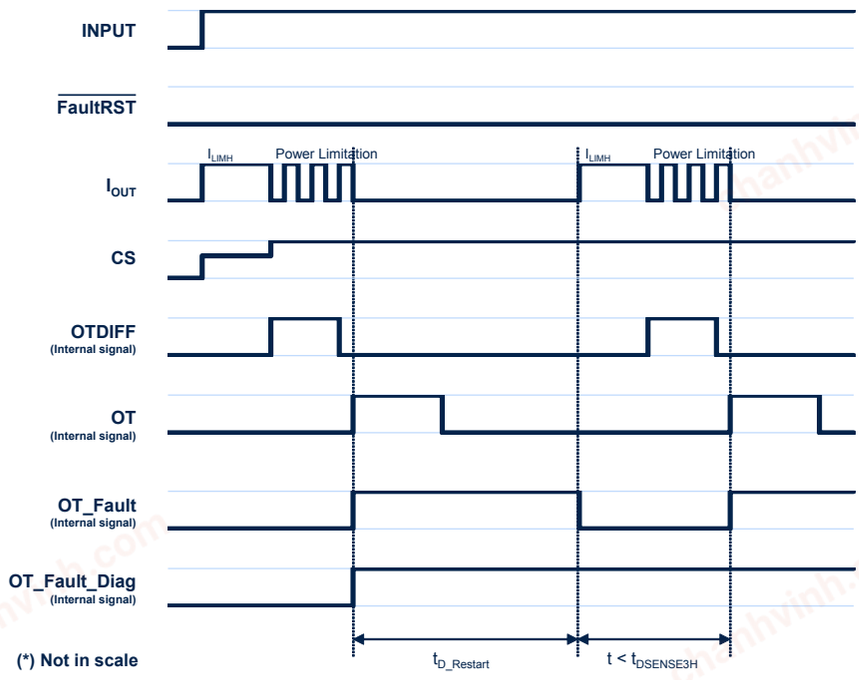


Figure 10. **Standby mode activation**

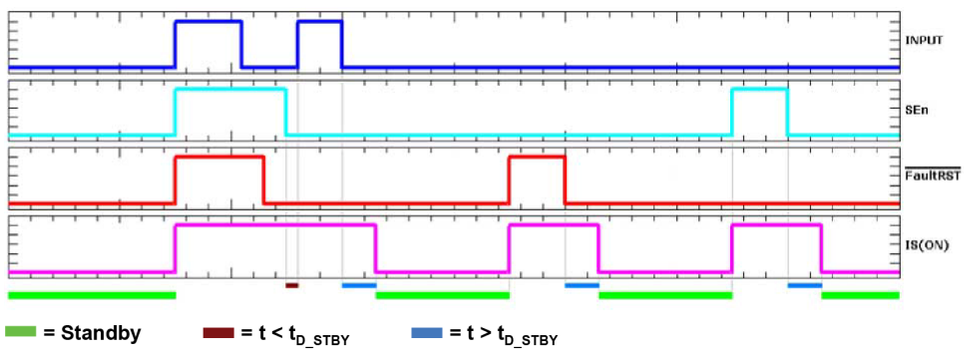
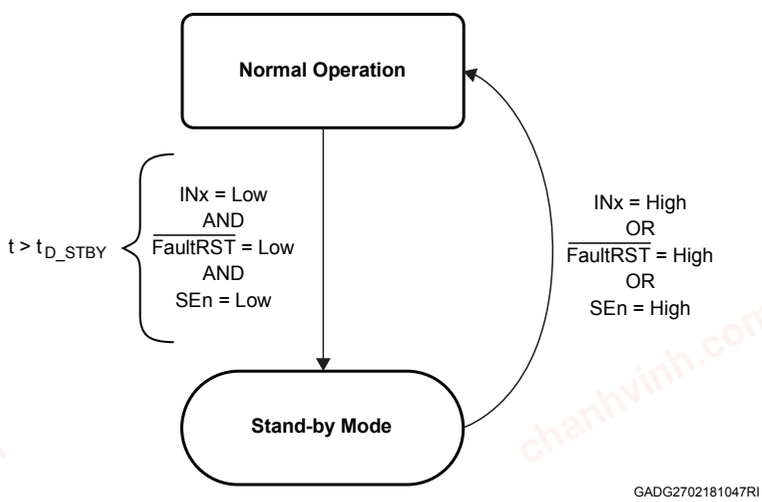


Figure 11. **Standby state diagram**



chanhvinh.com

2.5 Electrical characteristics (curves)

Figure 12. OFF-state output current

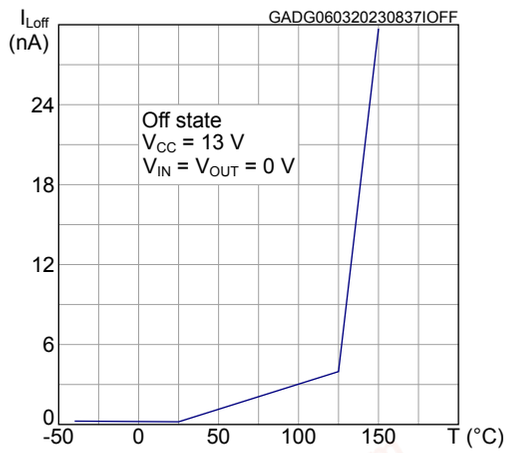


Figure 13. Standby current

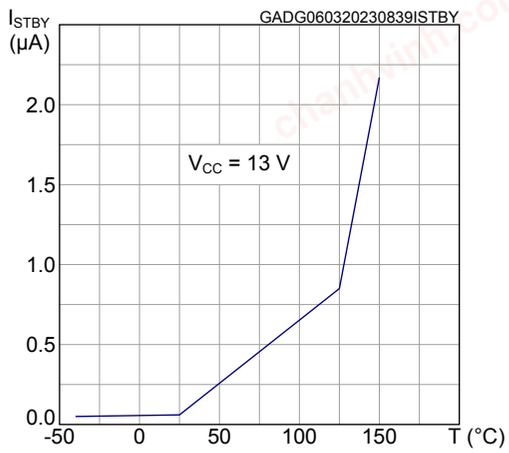


Figure 14. $I_{GND(ON)}$ vs T_C

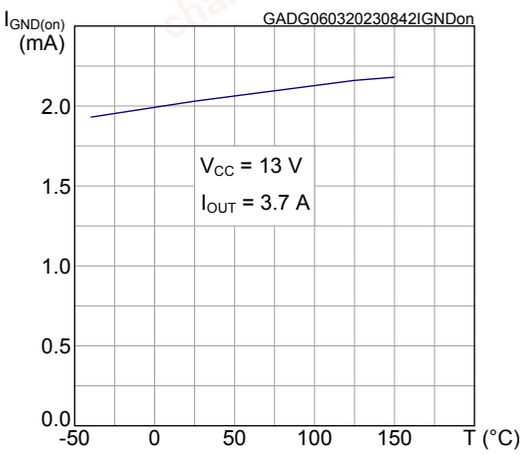


Figure 15. Logic input high level voltage

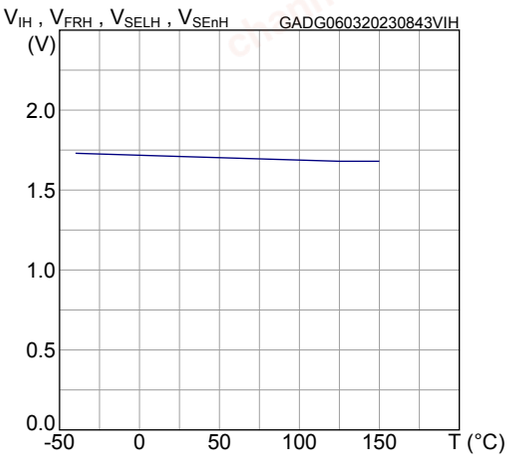


Figure 16. Logic input low level voltage

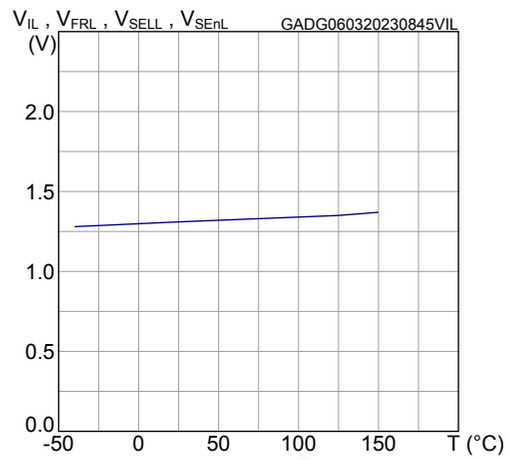
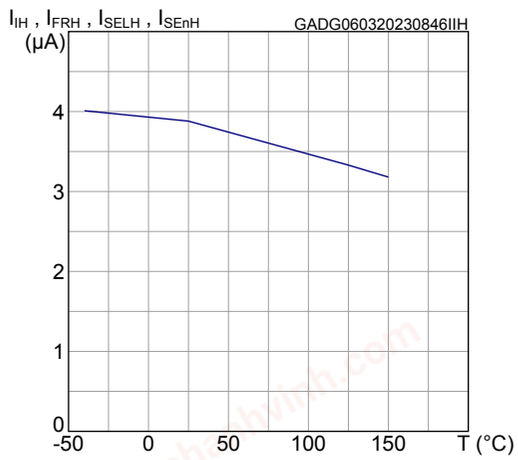


Figure 17. High level logic input current



chanhvinh.com

Figure 18. Low level logic input current

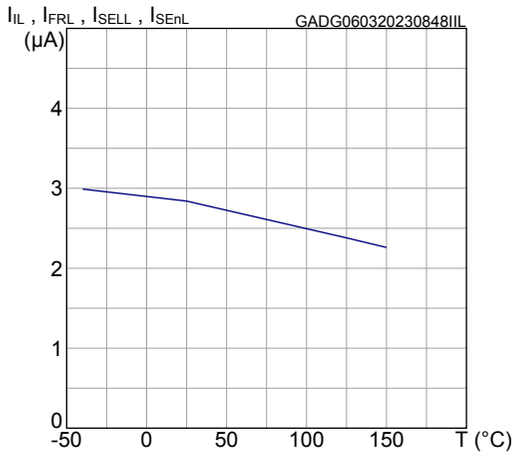


Figure 19. Logic input hysteresis voltage

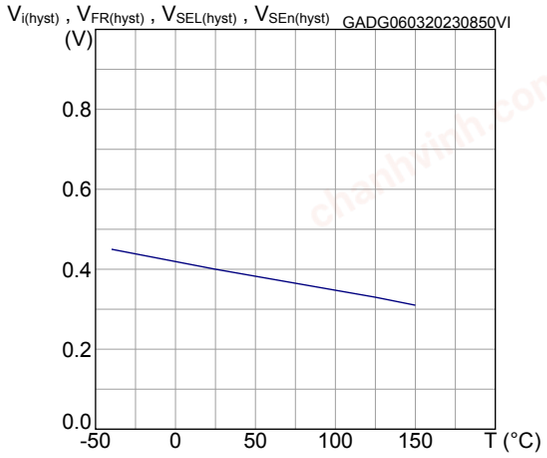


Figure 20. FaultRST input clamp voltage

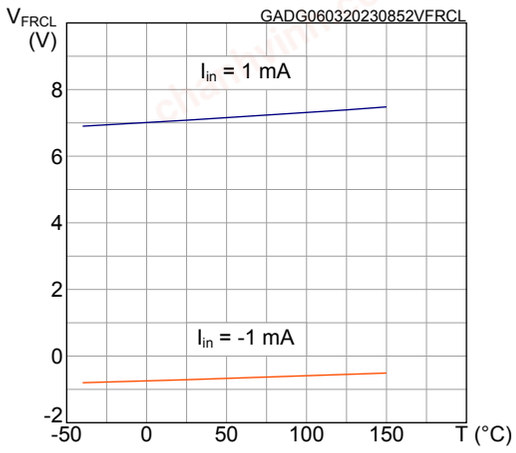


Figure 21. Undervoltage shutdown

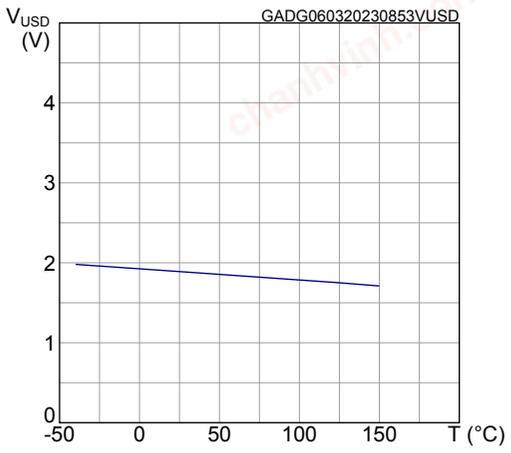


Figure 22. On-state resistance vs T_C

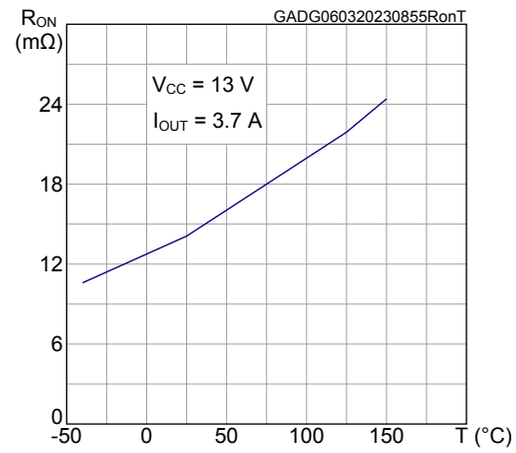
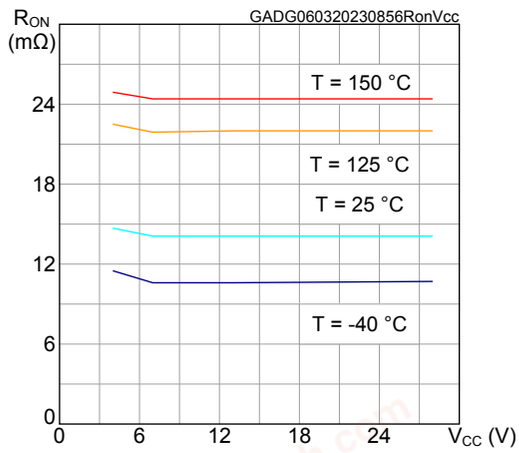


Figure 23. On-state resistance vs V_{CC}



chanhvinh.com

Figure 24. Turn-on voltage slope

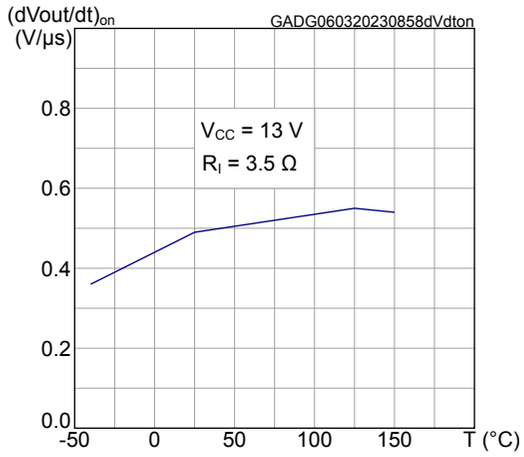


Figure 25. Turn-off voltage slope

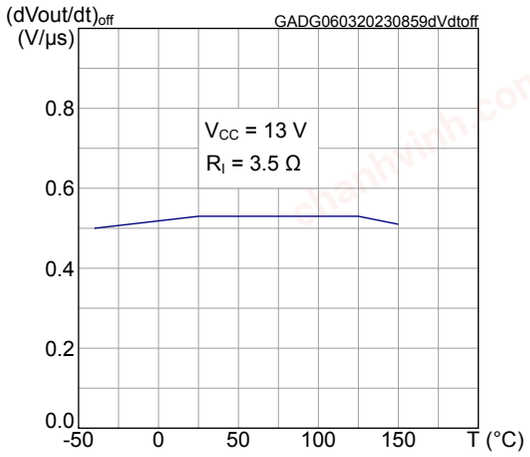


Figure 26. W_{ON} vs T_C

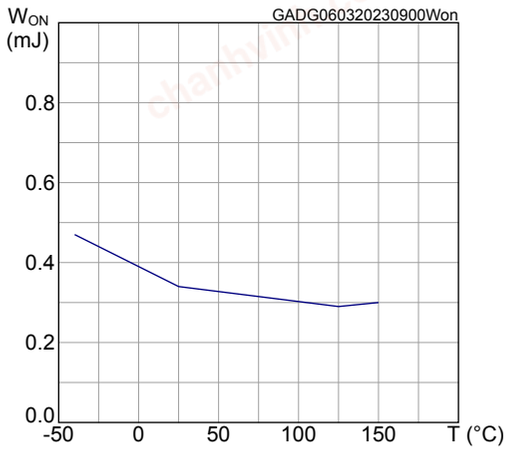


Figure 27. W_{OFF} vs T_C

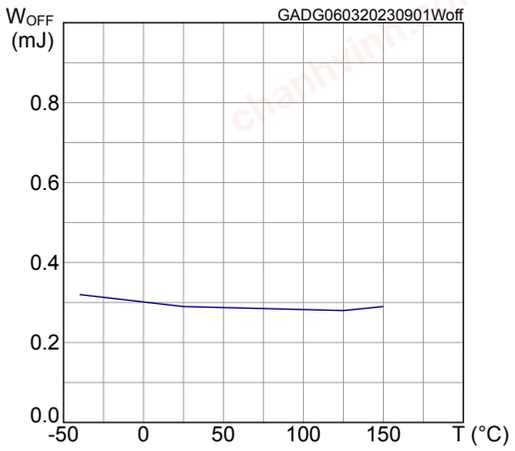


Figure 28. I_{LIMH} vs T_C

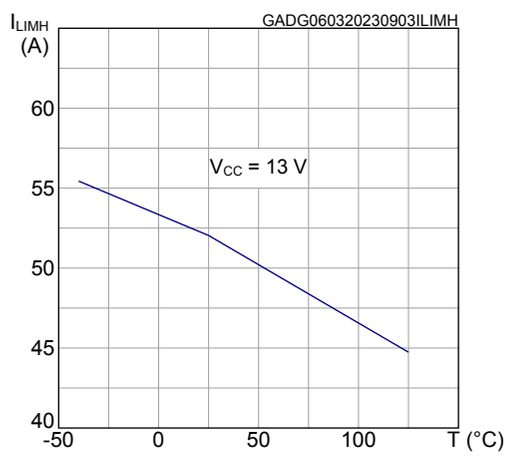
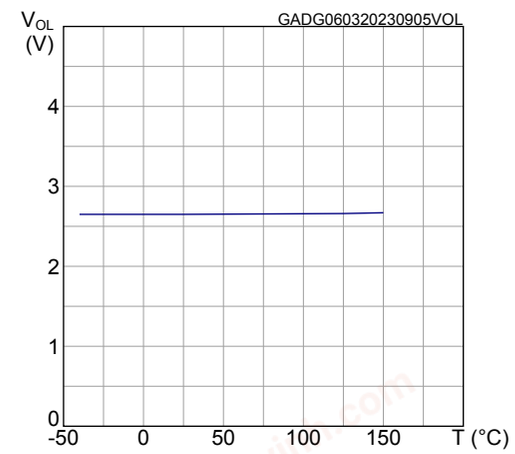


Figure 29. OFF-state open-load voltage detection threshold



chanhvinh.com

Figure 30. V_{Sense} clamp vs T_C

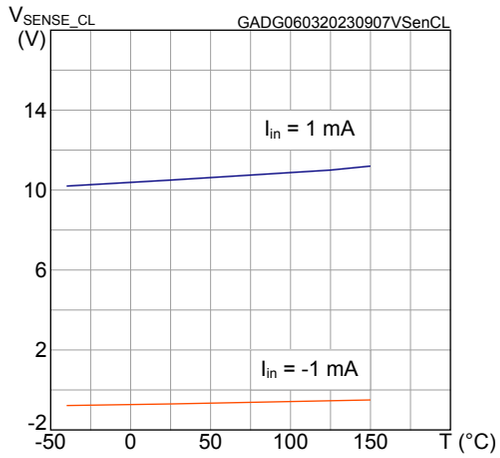
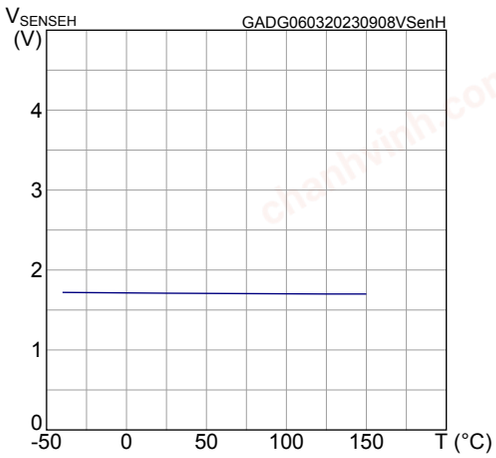


Figure 31. V_{senseh} vs T_C



chanhvinh.com

3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_J through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_J exceeds the safety level of ΔT_{J_SD}. According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled ($\overline{\text{FaultRST}}$ = Low) or remain off ($\overline{\text{FaultRST}}$ = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175 °C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the device switches on again as soon as its junction temperature drops to T_R ($\overline{\text{FaultRST}}$ = Low) or remains off ($\overline{\text{FaultRST}}$ = High).

3.3 Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (for example bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short-circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

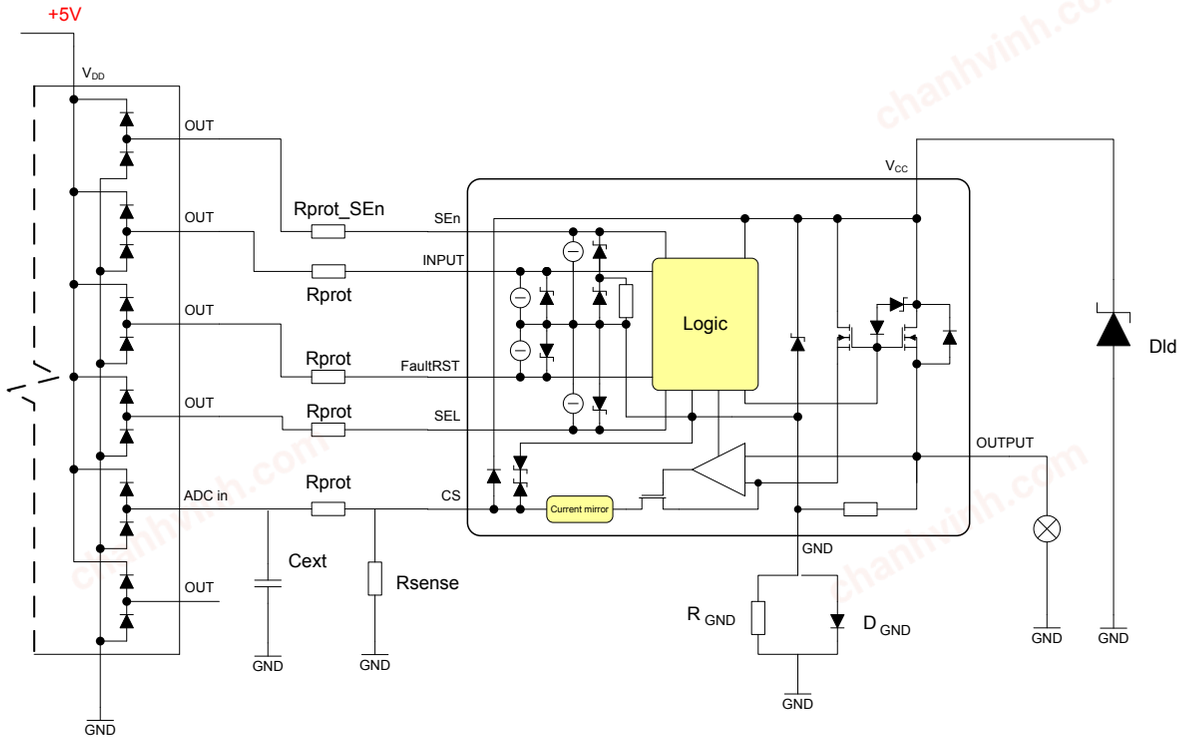
3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

chanhvinh.com

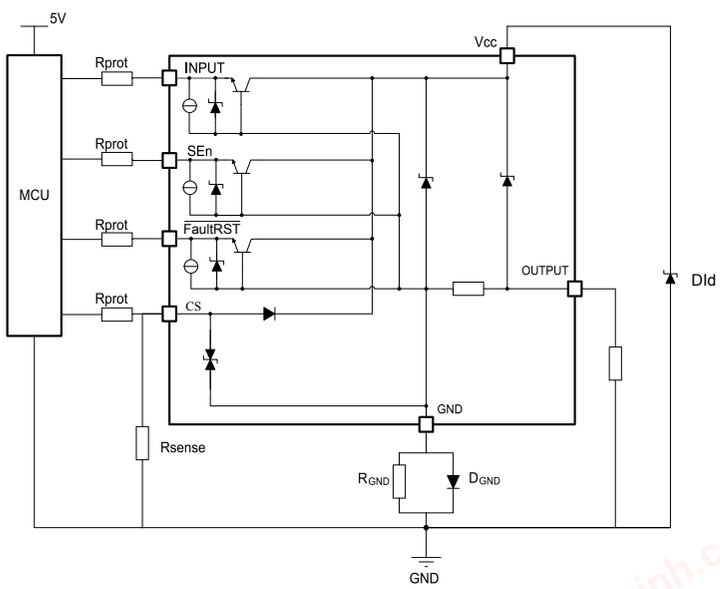
4 Application information

Figure 32. **Application diagram**



4.1 GND protection network against reverse battery

Figure 33. **Simplified internal structure**



chanhvinh.com

4.1.1 Diode (DGND) in the ground line

A resistor (typ. R_{GND} = 4.7 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in Table 12. ISO 7637-2 - electrical transient conduction along supply line.

Test pulses are applied directly to DUT (device under test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4.

The DUT is intended as the current device only, with external components as shown in Figure 34. M0-9 application schematic.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

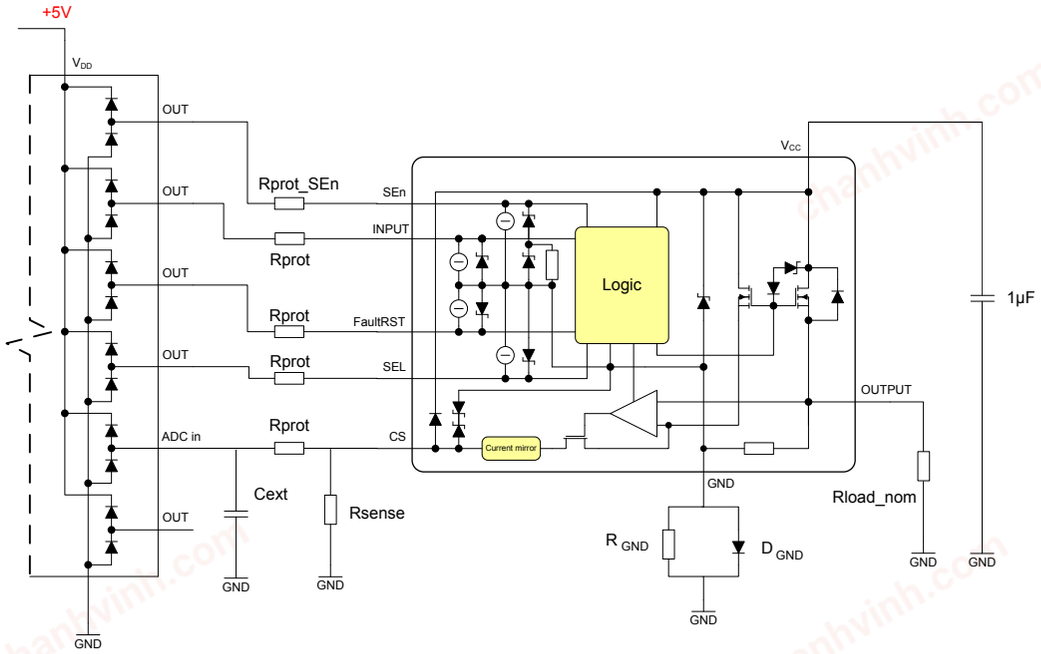
Table 12. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S (1)		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4 (2)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B (3)		35 V	5 pulse	1 min		400 ms, 2 Ω

1. *U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.*
2. *Test pulse from ISO 7637-2:2004(E).*
3. *With 35 V external suppressor referred to ground (-40°C < T_j < 150 °C).*

chanhvinh.com

Figure 34. **M0-9 application schematic**



4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$$\frac{V_{ccpeak}}{I_{latchup}} \leq R_{prot} \leq \frac{(V_{OH\mu C} - V_{IH} - V_{GND})}{I_{IH\max}} \quad (1)$$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup}$ ≥ 20 mA; $V_{OH\mu C}$ ≥ 4.5 V

7.5 kΩ ≤ R_{prot} ≤ 140 kΩ.

Recommended values: R_{prot} = 15 kΩ

4.4 CS - analog current sense

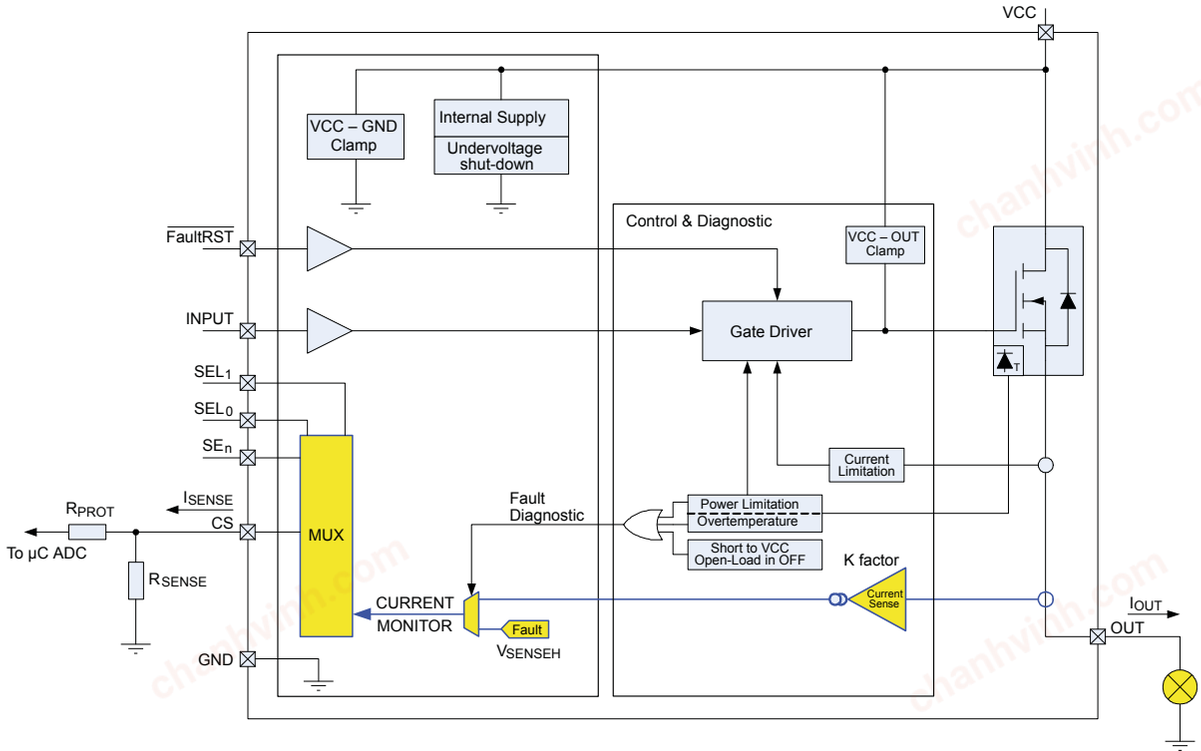
Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signals:

- Current monitor: current mirror of channel output current

Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in Table 11. Current sense multiplexer addressing.

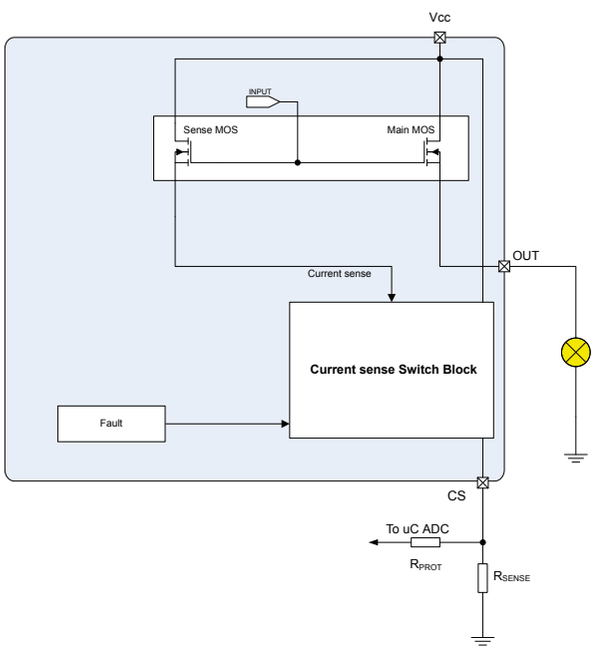
chanhvinh.com

Figure 35. **Current Sense and diagnostic – block diagram**



4.4.1 Principle of current sense signal generation

Figure 36. **Current sense block diagram**



Current sense

The output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

chanhvinh.com

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While the device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations.

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on the R_{SENSE} resistor
- I_{SENSE} is the current provided from CurrentSense pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

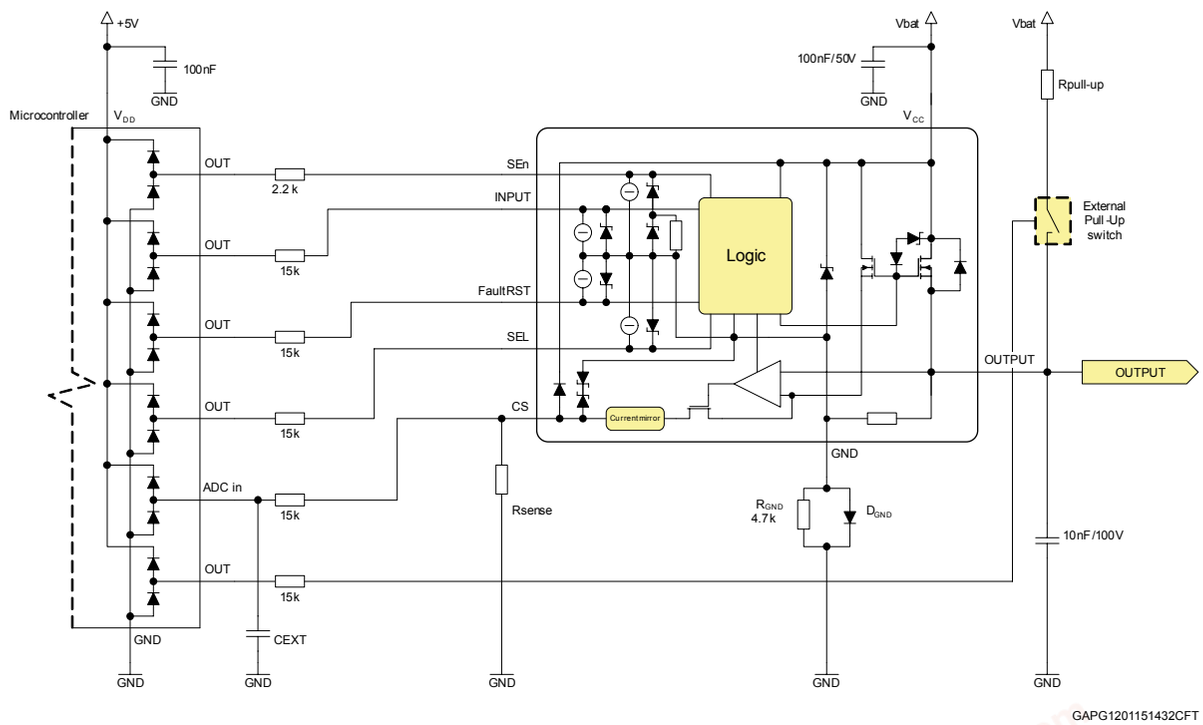
Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CurrentSense pin, which is switched to a “current limited” voltage source, V_{SENSEH}.

In any case, the current sourced by the CurrentSense in this condition is limited to I_{SENSEH}.

The typical behavior in case of overload or hard short-circuit is shown in Waveforms.

Figure 37. Analog HSD – open-load detection in off-state



chanhvinh.com

Figure 38. **Open-load / short to V_{CC} condition**

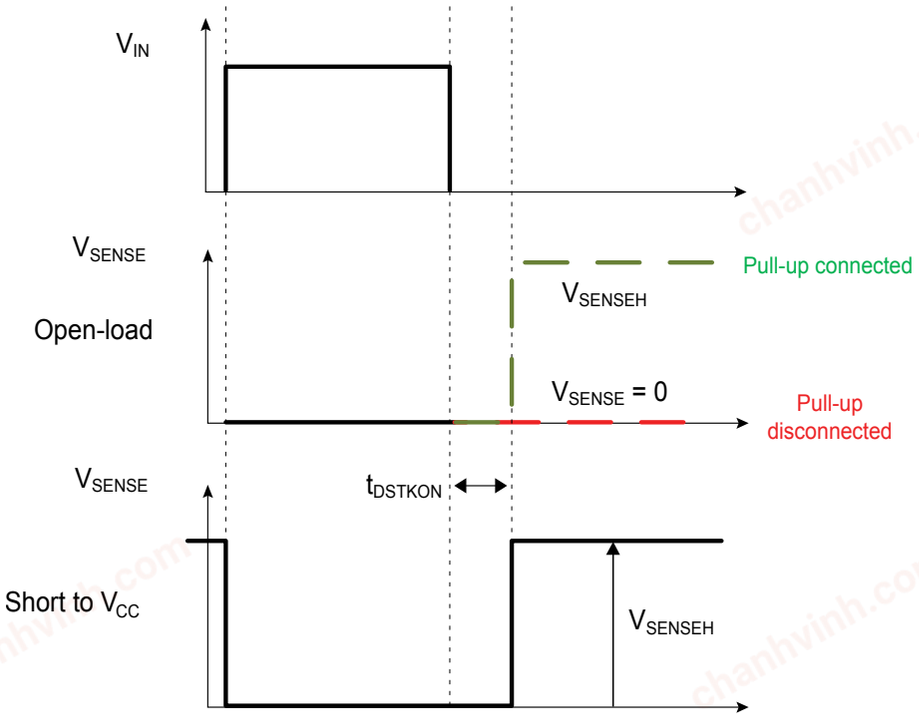


Table 13. **CS pin levels in off-state**

Condition	Output	CS	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)\min@\ 4V}} \quad (2)$$

chanhvinh.com

5 Maximum demagnetization energy (V_{CC} = 16 V)

Figure 39. **Maximum turn off current versus inductance**

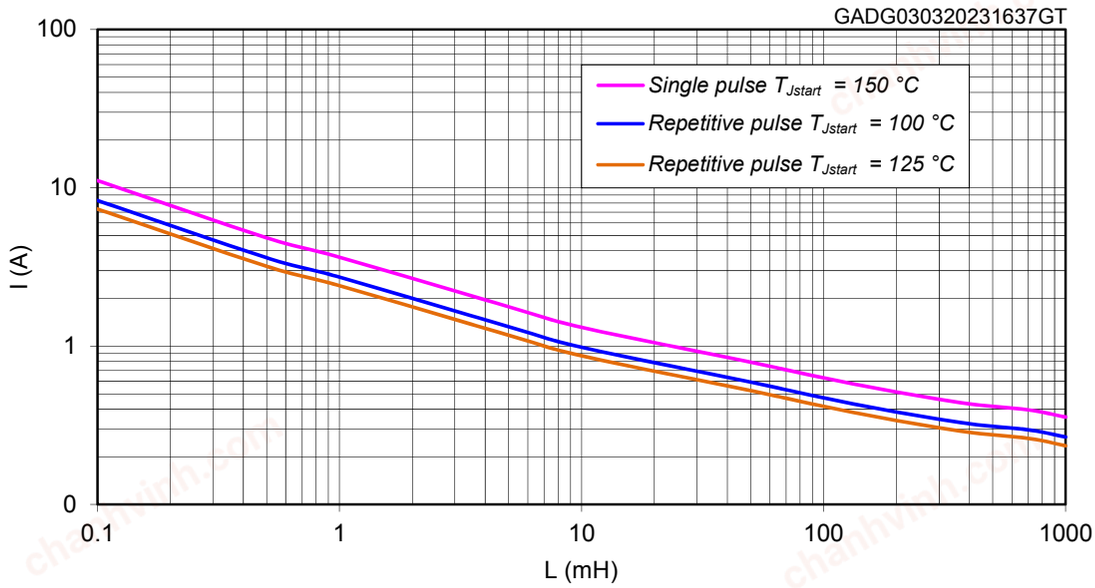
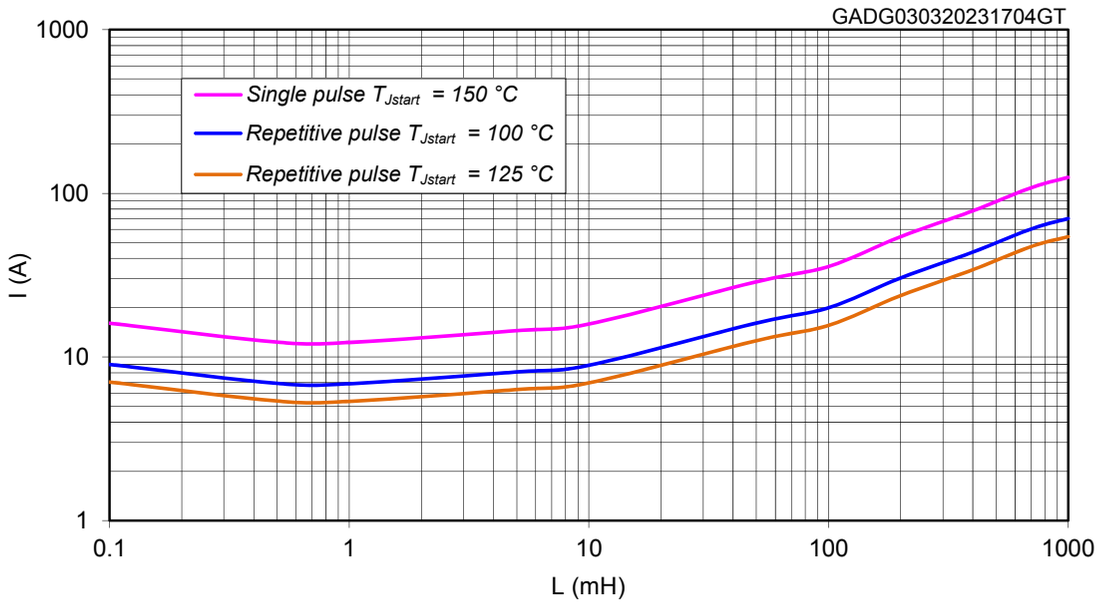


Figure 40. **Maximum turn off energy versus inductance**



chanhvinh.com

6 Package and PCB thermal data

6.1 PowerSSO-16 thermal data

Figure 41. **PowerSSO-16 on two-layer PCB (2s0p to JEDEC JESD 51-5)**

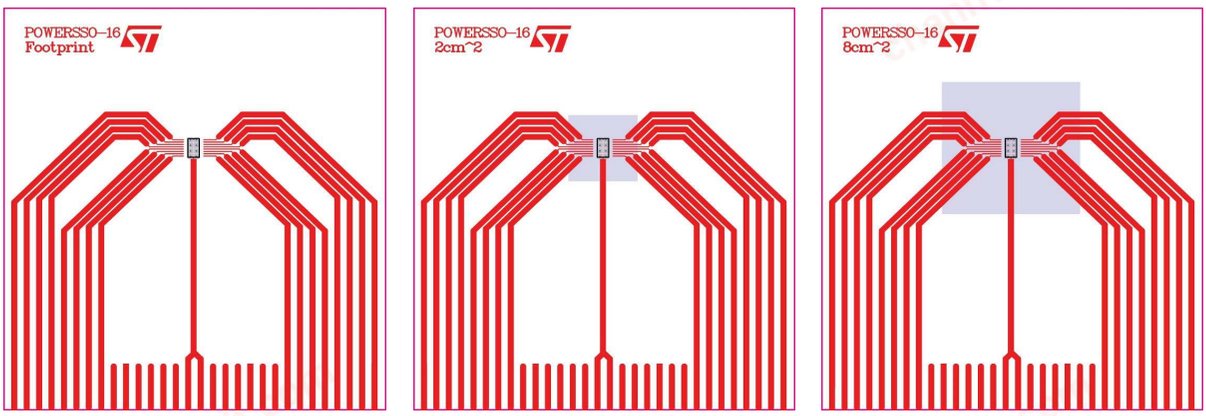


Figure 42. **PowerSSO-16 on four-layer PCB (2s2p to JEDEC JESD 51-7)**

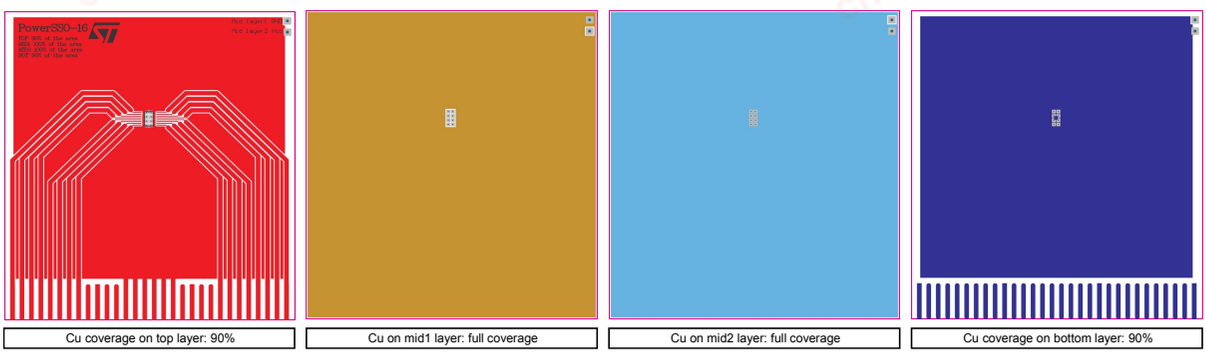


Table 14. **PCB properties**

Dimension	Value
Board finish thickness	1.6 mm ±10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm ±0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

chanhvinh.com

Figure 43. R_{thJA} vs PCB copper area in open box free air condition (one channel on)

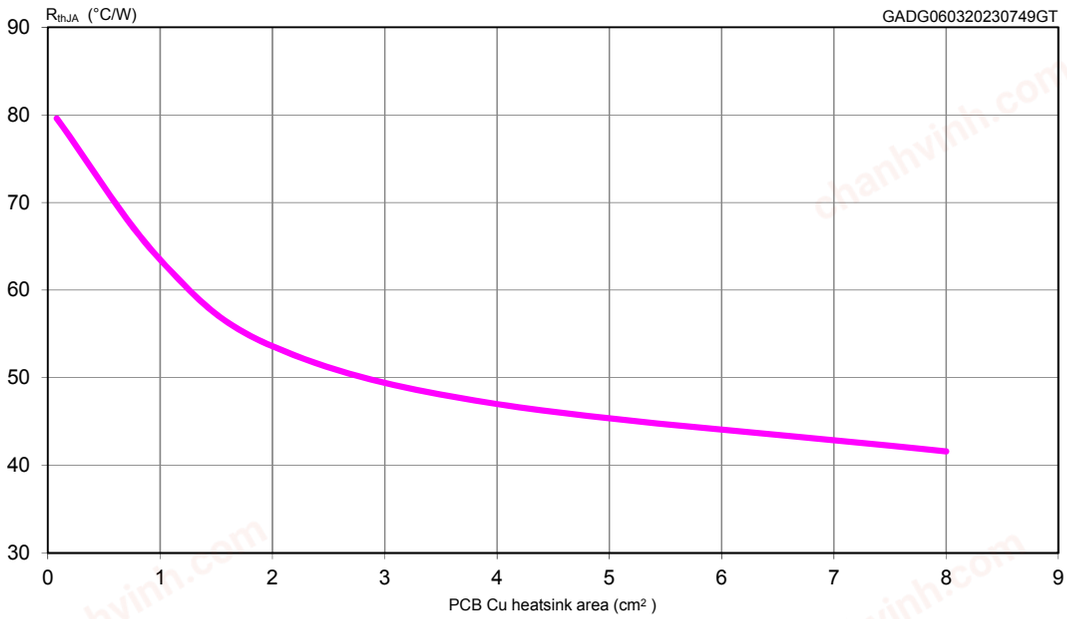
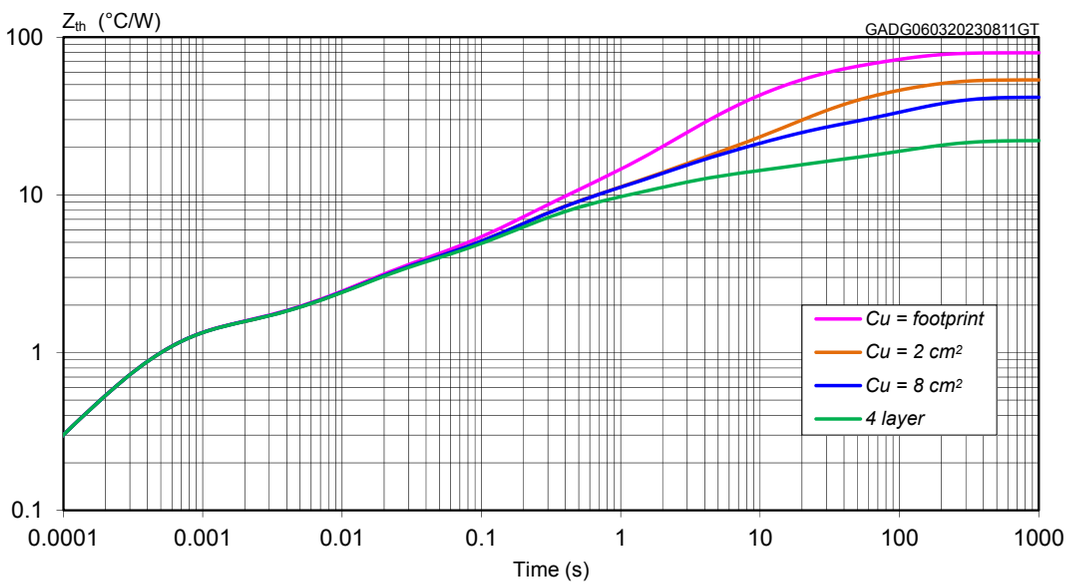


Figure 44. PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)



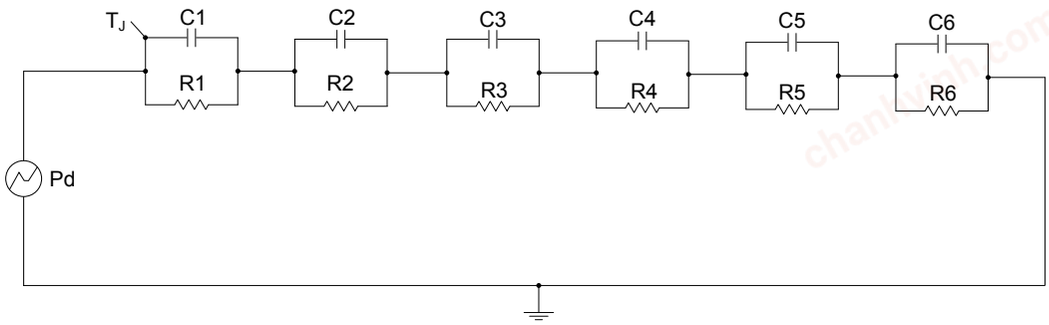
Equation: pulse calculation formula

$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$

where $\delta = t_P/T$

chanhvinh.com

Figure 45. **Thermal fitting model of a double-channel HSD in PowerSSO-16**



GAPGCFT00280

Note: the fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. **Thermal parameters**

Area/island (cm²)	FP	2	8	4L
R1 (°C/W)	1.3			
R2 (°C/W)	1.68			
R3 (°C/W)	4.6	4.6	4.6	4.6
R4 (°C/W)	16	6	6	4.5
R5 (°C/W)	30	20	20	3
R6 (°C/W)	26	20	18	7
C1 (W·s/°C)	0.0003			
C2 (W·s/°C)	0.0078			
C3 (W·s/°C)	0.048	0.05	0.05	0.06
C4 (W·s/°C)	0.2	0.3	0.3	0.4
C5 (W·s/°C)	0.4	1	1	4
C6 (W·s/°C)	3	5	7	18

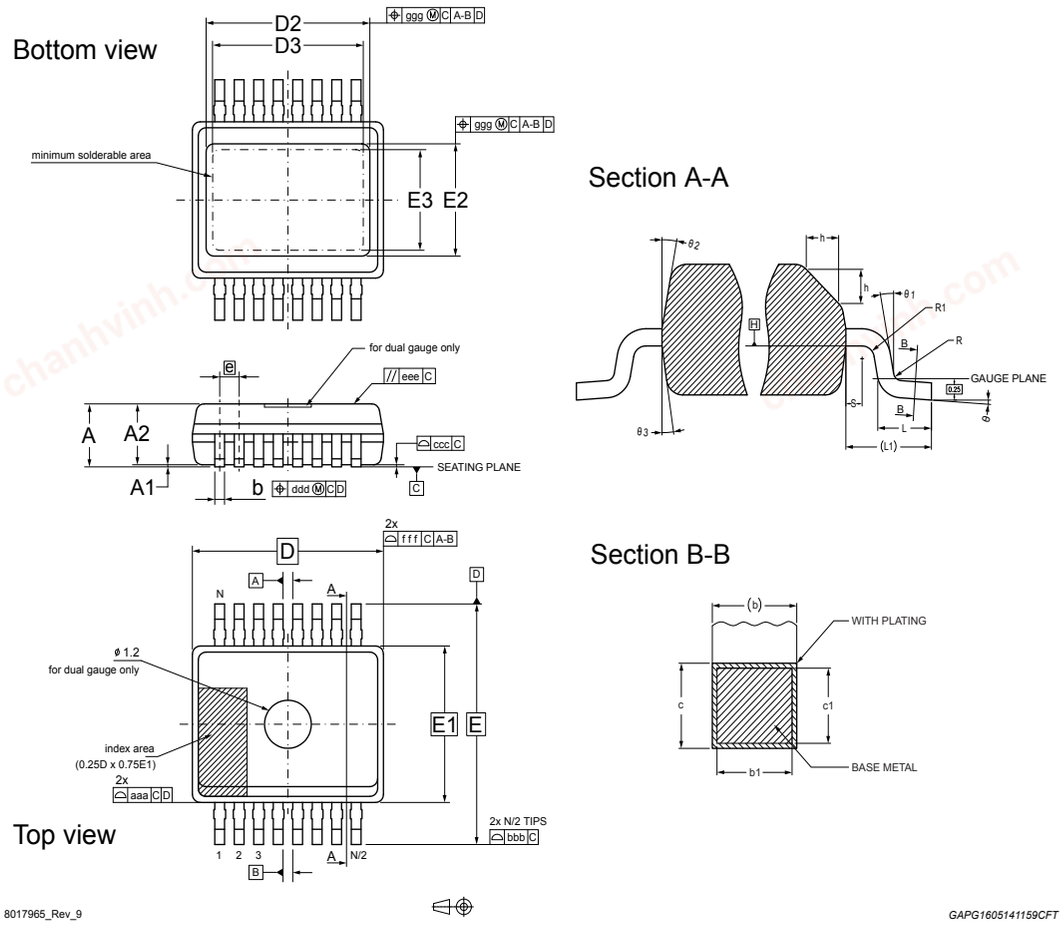
chanhvinh.com

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-16 package information

Figure 46. PowerSSO-16 package dimensions



chanhvinh.com

Table 16. **PowerSSO-16 mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	0°		
Θ2	5°		15°
Θ3	5°		15°
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D		4.9 BSC	
D2	3.31		3.91
D3	2.61		
e		0.50 BSC	
E		6.00 BSC	
E1		3.90 BSC	
E2	2.20		2.80
E3	1.49		
h	0.25		0.50
L	0.40	0.60	0.85
L1		1.00 REF	
N		16	
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.08	
eee		0.10	
fff		0.10	
ggg		0.15	

chanhvinh.com

7.2 PowerSSO-16 packing information

Figure 47. **PowerSSO-16 reel 13"**

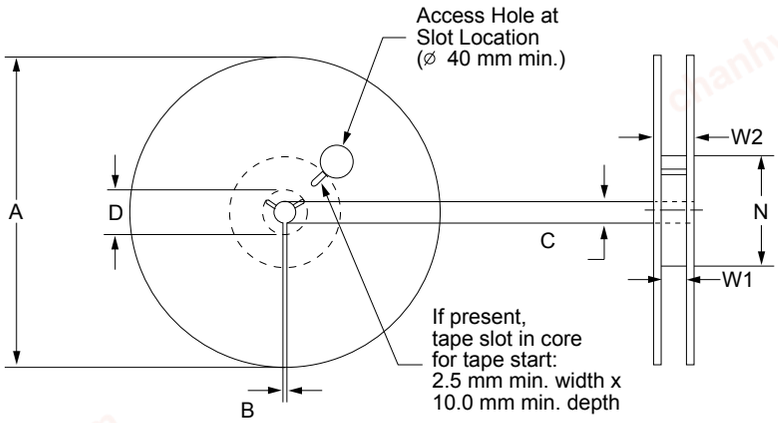


Table 17. **Reel dimensions**

Description	Value[1]
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2 /-0)	12.4
W2 (max)	18.4

1. *All dimensions are in mm.*

chanhvinh.com

Figure 48. **PowerSSO-16 carrier tape**

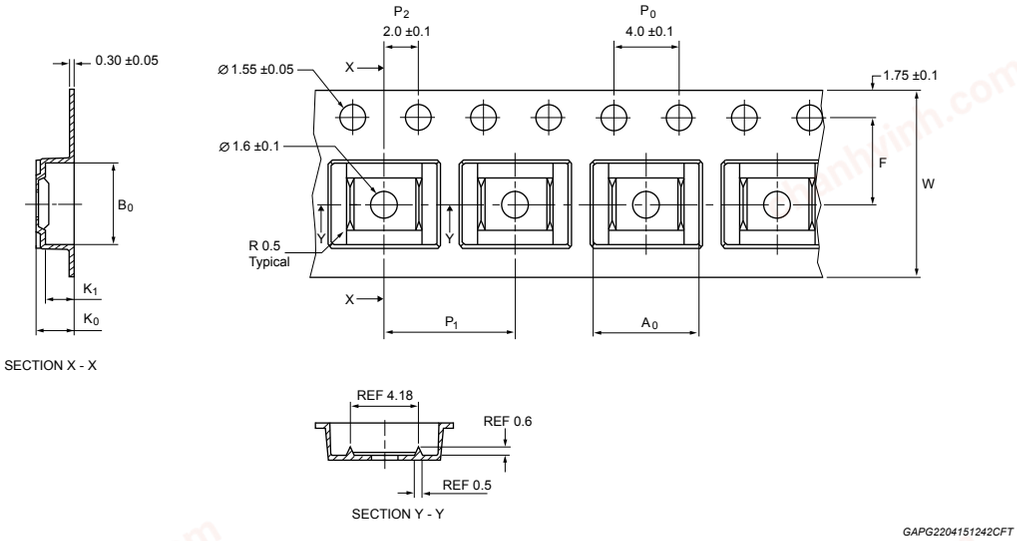
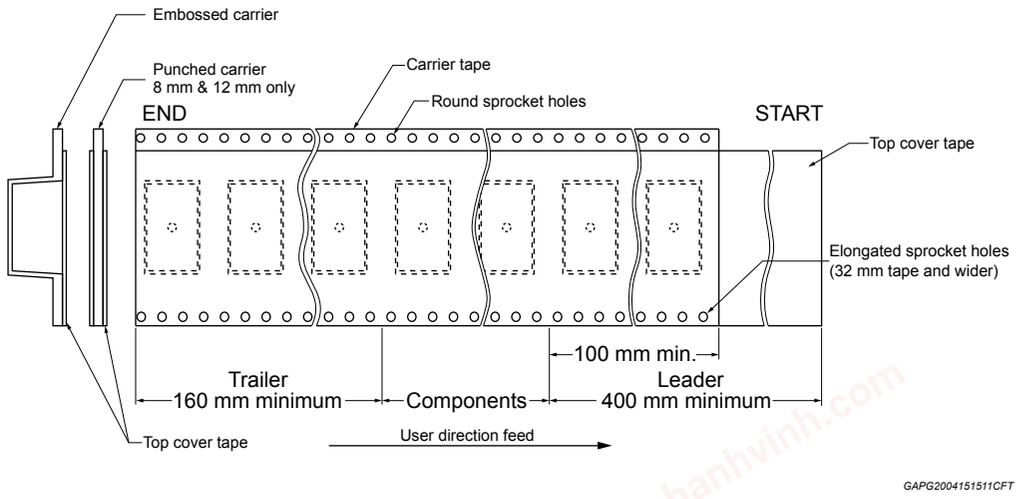


Table 18. **PowerSSO-16 carrier tape dimensions**

Description	Value(1)
A_0	6.50 ± 0.1
B_0	5.25 ± 0.1
K_0	2.10 ± 0.1
K_1	1.80 ± 0.1
F	5.50 ± 0.1
P_1	8.00 ± 0.1
W	12.00 ± 0.3

1. *All dimensions are in mm.*

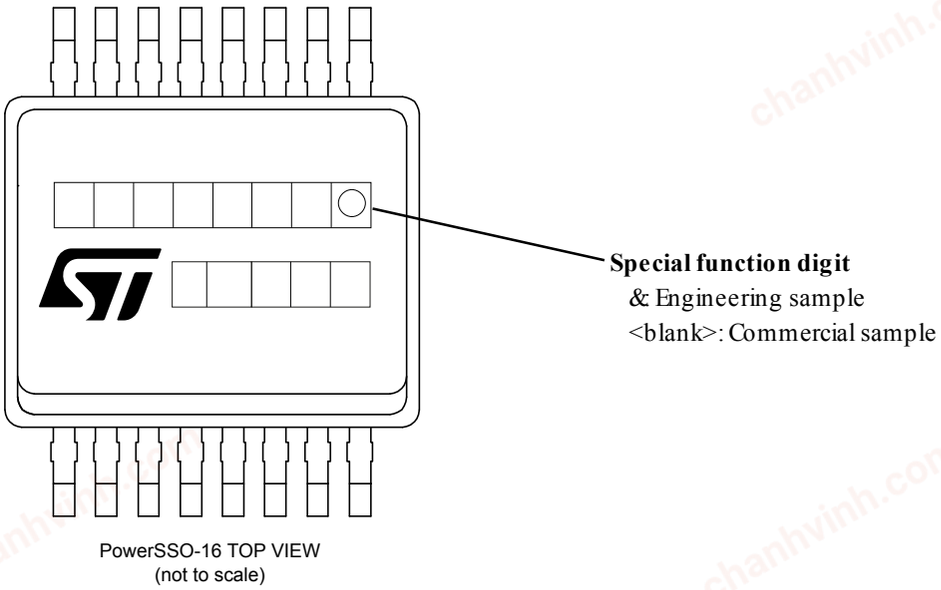
Figure 49. **PowerSSO-16 schematic drawing of leader and trailer tape**



chanhvinh.com

7.3 PowerSSO-16 marking information

Figure 50. **PowerSSO-16 marking information**



Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

chanhvinh.com

Revision history

Table 19. **Document revision history**

Date	Revision	Changes
28-Jun-2018	1	Initial release.
18-May-2021	2	Added: • *Section 4 Application information*; • *Section 5 Package information*. Updated: • *Figure 1. Block diagram*; • *Figure 2. Configuration diagram (top view)*; • *Figure 3. Current and voltage conventions*; • *Table 3. Absolute maximum ratings*; • *Table 5. Power section*; • *Table 6. Switching*; • *Table 8. Protections*; • *Table 9. Current Sense*; • *Section Features*; • *Section 2.4 Waveforms*. Minor text changes in: • *Table 1. Pin functions*; • *Table 7. Logic inputs*.
13-Mar-2023	3	Updated Features and Applications on cover page. Updated Table 2. Suggested connections for unused and not connected pins. Updated Table 3. Absolute maximum ratings, Table 4. Thermal data, Table 5. Power section, Table 6. Switching, Table 8. Protections, Table 9. Current sense. Updated Figure 11. Standby state diagram. Added Section 2.5 Electrical characteristics (curves), Section 5 Maximum demagnetization energy (V_{CC} = 16 V) and Section 6 Package and PCB thermal data. Minor text changes.

chanhvinh.com

Contents

1 **Block diagram and pin description** 3
2 **Electrical specification** 5
2.1 Absolute maximum ratings 5
2.2 Thermal data 6
2.3 Main electrical characteristics 6
2.4 Waveforms 13
2.5 Electrical characteristics (curves) 15
3 **Protections** 19
3.1 Power limitation 19
3.2 Thermal shutdown 19
3.3 Current limitation 19
3.4 Negative voltage clamp 19
4 **Application information** 20
4.1 GND protection network against reverse battery 20
4.1.1 Diode (DGND) in the ground line 21
4.2 Immunity against transient electrical disturbances 21
4.3 MCU I/Os protection 22
4.4 CS - analog current sense 22
4.4.1 Principle of current sense signal generation 23
4.4.2 Short to V_{CC} and OFF-state open-load detection 25
5 **Maximum demagnetization energy (V_{CC} = 16 V)** 26
6 **Package and PCB thermal data** 27
6.1 PowerSSO-16 thermal data 27
7 **Package information** 30
7.1 PowerSSO-16 package information 30
7.2 PowerSSO-16 packing information 32
7.3 PowerSSO-16 marking information 34
Revision history 35

chanhvinh.com

List of tables

Table 1. Pin functions . . . 3
Table 2. Suggested connections for unused and not connected pins . . . 4
Table 3. Absolute maximum ratings . . . 5
Table 4. Thermal data . . . 6
Table 5. Power section . . . 6
Table 6. Switching . . . 7
Table 7. Logic inputs . . . 7
Table 8. Protections . . . 8
Table 9. Current sense . . . 9
Table 10. Truth table . . . 12
Table 11. Current sense multiplexer addressing . . . 12
Table 12. ISO 7637-2 - electrical transient conduction along supply line . . . 21
Table 13. CS pin levels in off-state . . . 25
Table 14. PCB properties . . . 27
Table 15. Thermal parameters . . . 29
Table 16. PowerSSO-16 mechanical data . . . 31
Table 17. Reel dimensions . . . 32
Table 18. PowerSSO-16 carrier tape dimensions . . . 33
Table 19. Document revision history . . . 35

chanhvinh.com

List of figures

Figure 1. Block diagram . . . 3
Figure 2. Configuration diagram (top view) . . . 4
Figure 3. Current and voltage conventions . . . 5
Figure 4. Switching time and pulse skew . . . 11
Figure 5. Current sense timings (current sense mode) . . . 11
Figure 6. T_{DSTKON} . . . 12
Figure 7. Latch-off mode - Intermittent short circuit . . . 13
Figure 8. Auto-restart mode - Intermittent short circuit . . . 13
Figure 9. Auto-restart mode - Permanent short circuit . . . 14
Figure 10. Standby mode activation . . . 14
Figure 11. Standby state diagram . . . 14
Figure 12. OFF-state output current . . . 15
Figure 13. Standby current . . . 15
Figure 14. $I_{GND(ON)}$ vs T_C . . . 15
Figure 15. Logic input high level voltage . . . 15
Figure 16. Logic input low level voltage . . . 15
Figure 17. High level logic input current . . . 15
Figure 18. Low level logic input current . . . 16
Figure 19. Logic input hysteresis voltage . . . 16
Figure 20. FaultRST input clamp voltage . . . 16
Figure 21. Undervoltage shutdown . . . 16
Figure 22. On-state resistance vs T_C . . . 16
Figure 23. On-state resistance vs V_{CC} . . . 16
Figure 24. Turn-on voltage slope . . . 17
Figure 25. Turn-off voltage slope . . . 17
Figure 26. W_{ON} vs T_C . . . 17
Figure 27. W_{OFF} vs T_C . . . 17
Figure 28. I_{LIMH} vs T_C . . . 17
Figure 29. OFF-state open-load voltage detection threshold . . . 17
Figure 30. V_{Sense} clamp vs T_C . . . 18
Figure 31. V_{senseh} vs T_C . . . 18
Figure 32. Application diagram . . . 20
Figure 33. Simplified internal structure . . . 20
Figure 34. M0-9 application schematic . . . 22
Figure 35. Current Sense and diagnostic – block diagram . . . 23
Figure 36. Current sense block diagram . . . 23
Figure 37. Analog HSD – open-load detection in off-state . . . 24
Figure 38. Open-load / short to V_{CC} condition . . . 25
Figure 39. Maximum turn off current versus inductance . . . 26
Figure 40. Maximum turn off energy versus inductance . . . 26
Figure 41. PowerSSO-16 on two-layer PCB (2s0p to JEDEC JESD 51-5) . . . 27
Figure 42. PowerSSO-16 on four-layer PCB (2s2p to JEDEC JESD 51-7) . . . 27
Figure 43. R_{thJA} vs PCB copper area in open box free air condition (one channel on) . . . 28
Figure 44. PowerSSO-16 thermal impedance junction ambient single pulse (one channel on) . . . 28
Figure 45. Thermal fitting model of a double-channel HSD in PowerSSO-16 . . . 29
Figure 46. PowerSSO-16 package dimensions . . . 30
Figure 47. PowerSSO-16 reel 13" . . . 32
Figure 48. PowerSSO-16 carrier tape . . . 33
Figure 49. PowerSSO-16 schematic drawing of leader and trailer tape . . . 33
Figure 50. PowerSSO-16 marking information . . . 34

chanhvinh.com

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved