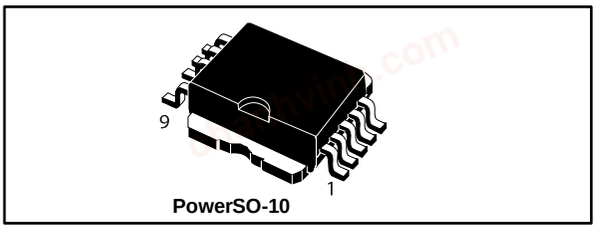
chanhvinh.com

VN340SP-33-E

Quad high-side smart power solid-state relay

Datasheet - production data



PowerSO-10

Features

Type	V_{demag} (1)	$R_{DS(on)}$ (1)	I_{OUT} (1)	V_{CC}
VN340SP-33-E	V_{CC}-55 V	0.2 Ω	1 A	36 V

Notes:

(1)Per channel

- Output current: 1 A per channel
- Digital I/O clamped at 32 V minimum voltage
- Shorted load and overtemperature protections
- Protection against loss of ground
- Built-in current limiter
- Undervoltage shutdown
- Open drain diagnostic output
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2

Description

The VN340SP-33-E is a monolithic device developed using STMicroelectronics' VIPower technology, intended to drive four independent resistive or inductive loads with one side connected to ground. Active current limitation prevents dropping of the system power supply in case of shorted load. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. The open drain diagnostic output indicates overtemperature conditions. Each I/O is pulled down when the overtemperature condition of the relative channel is verified.

Table 1: Device summary

Order code	Package	Packing
VN340SP-33-E	PowerSO-10	Tube
VN340SPTR-33-E		Tape and reel

This is information on a product in full production. www.st.com

chanhvinh.com

Contents

1 Block diagram 5
2 Pin connection 6
3 Maximum ratings 7
4 Electrical characteristics 8
5 Test circuits 10
6 Switching time waveforms and truth table 12
7 Package information 14
7.1 PowerSO-10 package information 14
7.2 PowerSO-10 packing information 16
8 Revision history 18

chanhvinh.com

List of tables

Table 1: Device summary 1
Table 2: Absolute maximum ratings 7
Table 3: Thermal data 7
Table 4: Power section 8
Table 5: Switching (V_{CC} = 24 V, T_J= 25 °C) 8
Table 6: Logic inputs 9
Table 7: Protection and diagnostic 9
Table 8: Truth table 13
Table 9: PowerSO-10 package mechanical data 15
Table 10: PowerSO-10 career tape dimension mechanical data 16
Table 11: PowerSO-10 reel dimension mechanical data 17
Table 12: PowerSO-10 base and bulk quantity 17
Table 13: Document revision history 18

chanhvinh.com

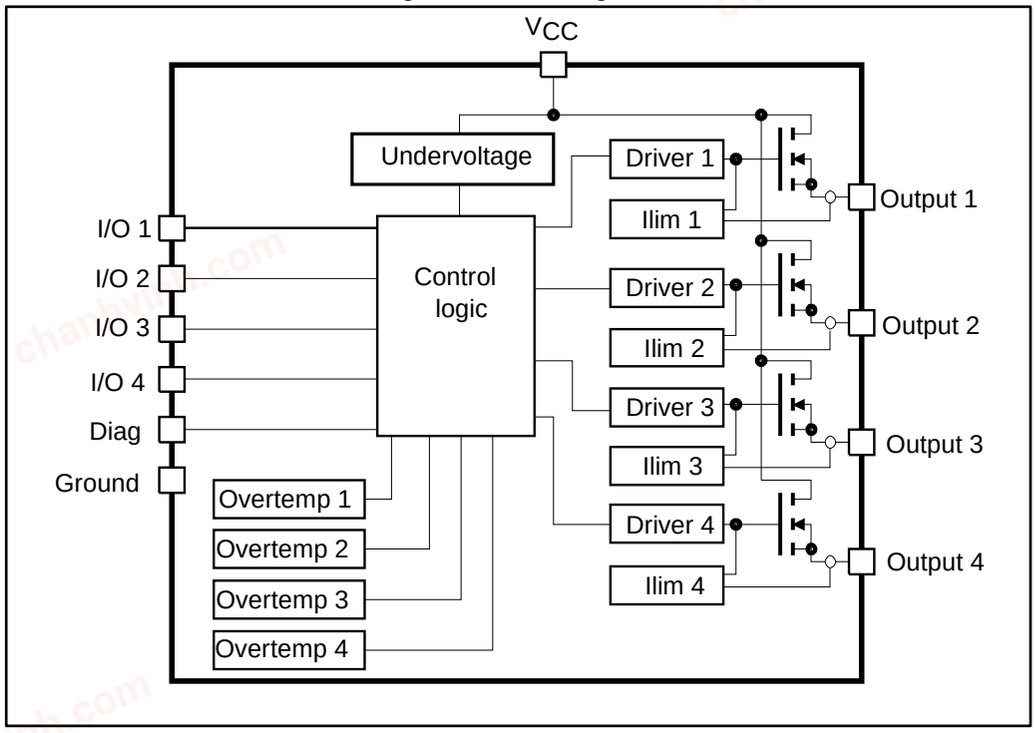
List of figures

Figure 1: Block diagram 5
Figure 2: Connection diagram (top view) 6
Figure 3: Current and voltage conventions 6
Figure 4: Avalanche energy test circuit 10
Figure 5: Peak short-circuit test diagram 10
Figure 6: I_{LGND} test configuration 11
Figure 7: Switching waveforms 12
Figure 8: Switching parameter test conditions 12
Figure 9: Driving circuit 13
Figure 10: PowerSO-10 package outline 14
Figure 11: PowerSO-10 career tape outline 16
Figure 12: PowerSO-10 reel outline 17

chanhvinh.com

1 Block diagram

Figure 1: Block diagram



chanhvinh.com

2 Pin connection

Figure 2: Connection diagram (top view)

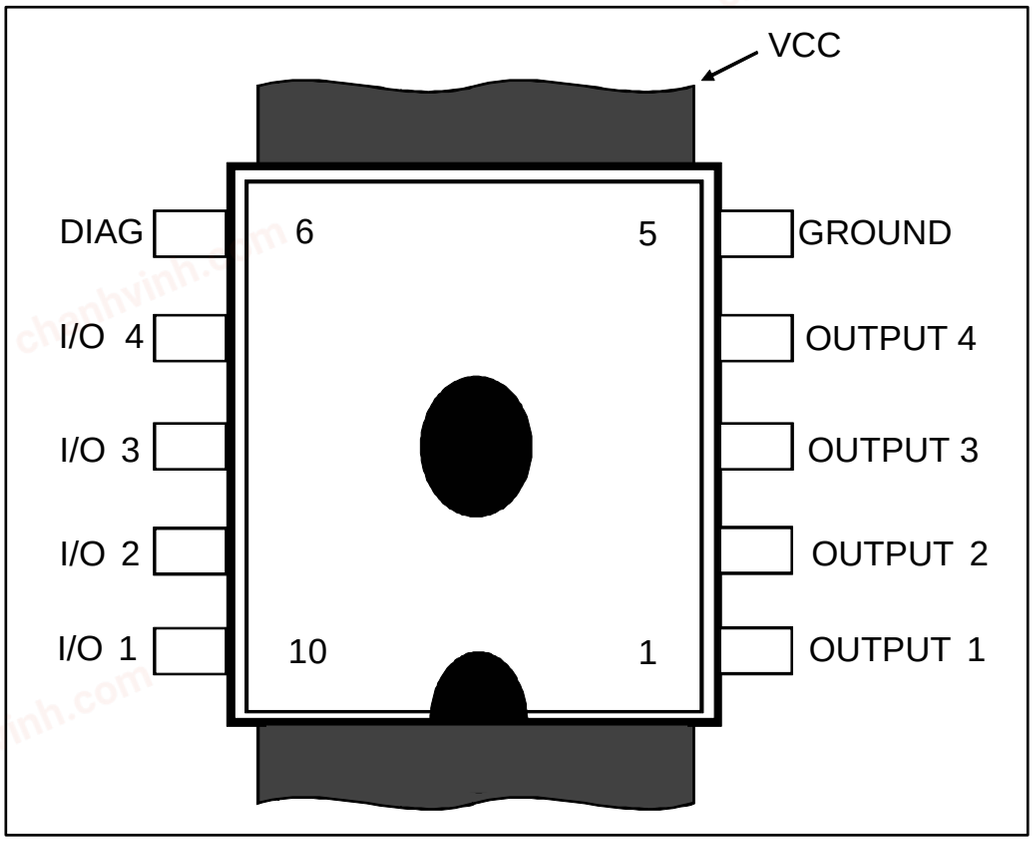
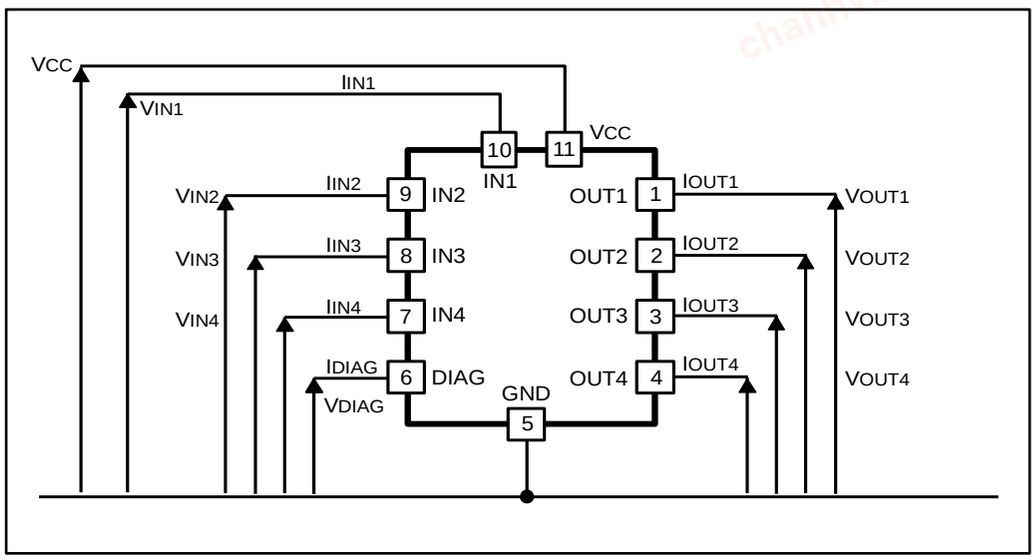


Figure 3: Current and voltage conventions



chanhvinh.com

3 Maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-4	V
I_{OUT}	Output current	Internally limited	A
I_R	Reverse output current (per channel)	-6	A
I_{IN}	Input current range	-1 to +10	mA
I_{DIAG}	Diag pin current	-1 to +10	mA
V_{ESD}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)	2000	V
E_{AS}	Single pulse avalanche energy one channel active T_J = 125 °, I_{LOAD} = 0.625 A	10	J
	Single pulse avalanche energy all channel active simultaneously T_J = 125 °, I_{LOAD} = 0.625 A	2	J
P_{TOT}	Power dissipation at T_C = 25 °C	Internally limited	W
T_J	Junction operating temperature	Internally limited	°C
T_{STG}	Storage temperature	-55 to 150	°C

Table 3: Thermal data

Symbol	Parameter		Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case (1)	Max.	3	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient (2)	Max.	50	°C/W

Notes:

(1)Per channel.

(2)When mounted on a four-layer FR4, with the minimum recommended pad size.

chanhvinh.com

4 Electrical characteristics

10 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified

Table 4: Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		10		36	V
$R_{DS(on)}$	On-state resistance	I_{OUT} = 0.5 A at T_J = 25 °C			0.2	Ω
		I_{OUT} = 0.5 A at T_J = 85 °C			0.32	
		I_{OUT} = 0.5 A at T_J = 125 °C			0.4	
I_S	Supply current	All channels in OFF-state, V_{IN} = 30 V, I_{OUT} = 0 V, T_J = 125 °C			1	mA
					6	mA
V_{OL}	Low state output voltage	V_{IN} = V_{IL}; R_{LOAD} > = 10 MΩ			1.5	µA
I_{LGND}	Output current at turn-off	V_{CC} = V_{IN} = V_{GND} = V_{STAT} = 18 to 30 V T_A = - 25 °C to 85 °C			2	mA
V_{demag}	Output current at turn-off	I_{OUT} = 0.5 A; L_{LOAD} >= 1 mH	V_{CC}-65	V_{CC}-55	V_{CC}-45	V

Table 5: Switching (V_{CC} = 24 V, T_J = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(ON)}$	Turn-on delay time	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs		52	100	µs
t_r	Rise timeof output current	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs		94	250	µs
$t_{d(OFF)}$	Turn-off delay time of output current	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs		34	50	µs
t_f	Fall time	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs		8	20	µs

chanhvinh.com

Table 6: Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	I/O input low level voltage				2	V
V_{IH}	I/O input high level voltage		3.5			V
$V_{I(HYST)}$	I/O input hysteresis voltage			0.5		V
I_{IN}	I/O input current	V_{IN} = 30 V			25	µA
V_{ICL}	I/O input clamp voltage(1)	I_{IN} = 1 mA	32	36		V
		I_{IN} = -1 mA		-0.7		V

Notes:

(1)The input voltage is internally clamped at 32 V minimum, the input pins can be connected to a higher voltage by an external resistor, which cannot exceed 10 mA

Table 7: Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DIAG}(1)	Status voltage output low	I_{DIAG} = 5 mA (fault condition)			1	V
V_{SCL}	Status clamp voltage	I_{DIAG} = 1 mA	32	36		
				-0.7		
V_{USD}	Undervoltage shutdown		5		8	V
I_{lim}	DC short-circuit current	V_{CC} = 24 V; R_{LOAD} < 10 mΩ	1		2	A
I_{OVPK}	Peak short-circuit current	V_{CC} = 24 V; V_{IN} = 30 V; R_{LOAD} < 10 mΩ			4	V
I_{DIAGH}	Leakage on DIAG pin in high state	V_{DIAG} = 24 V			25	µA
I_{LOAD}	Output leakage current	V_{CC} = 10 to 36 V; V_{IN}=V_{IL}			50	µA
t_{SC}	Delay time of current limiter				100	µs
T_{TSD}	Junction shutdown temperature		150	170		°C
T_R	Junction reset temperature		135	155		°C

Notes:

(1)Status determination > 100 µs after the switching edge.

If the INPUT pin is left floating, the corresponding channel automatically switches off. If GND pin is disconnected, the channel switches off provided that V_{CC} does not exceed 36 V.

chanhvinh.com

5 Test circuits

Figure 4: Avalanche energy test circuit

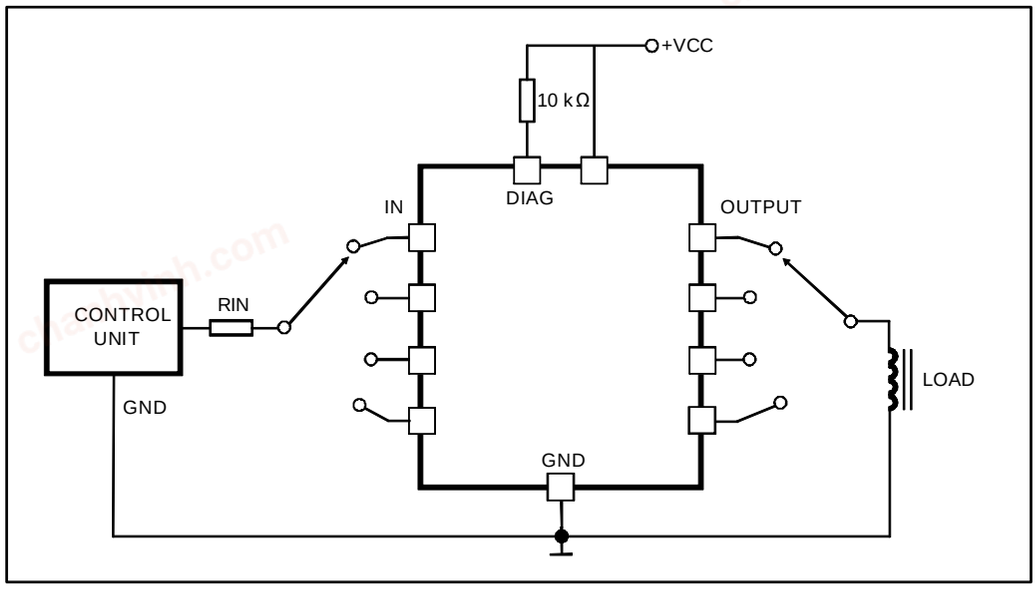
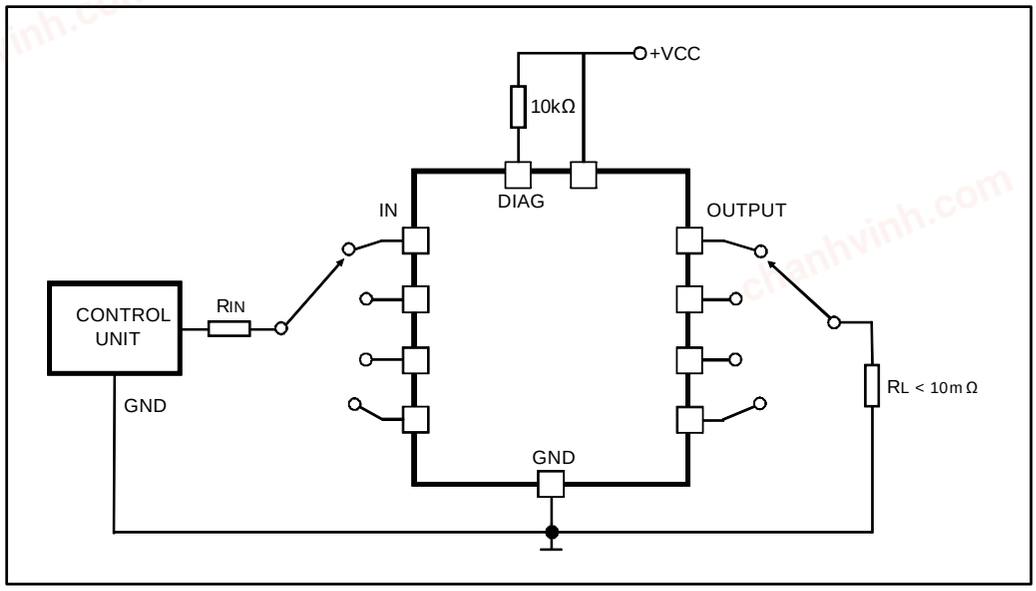
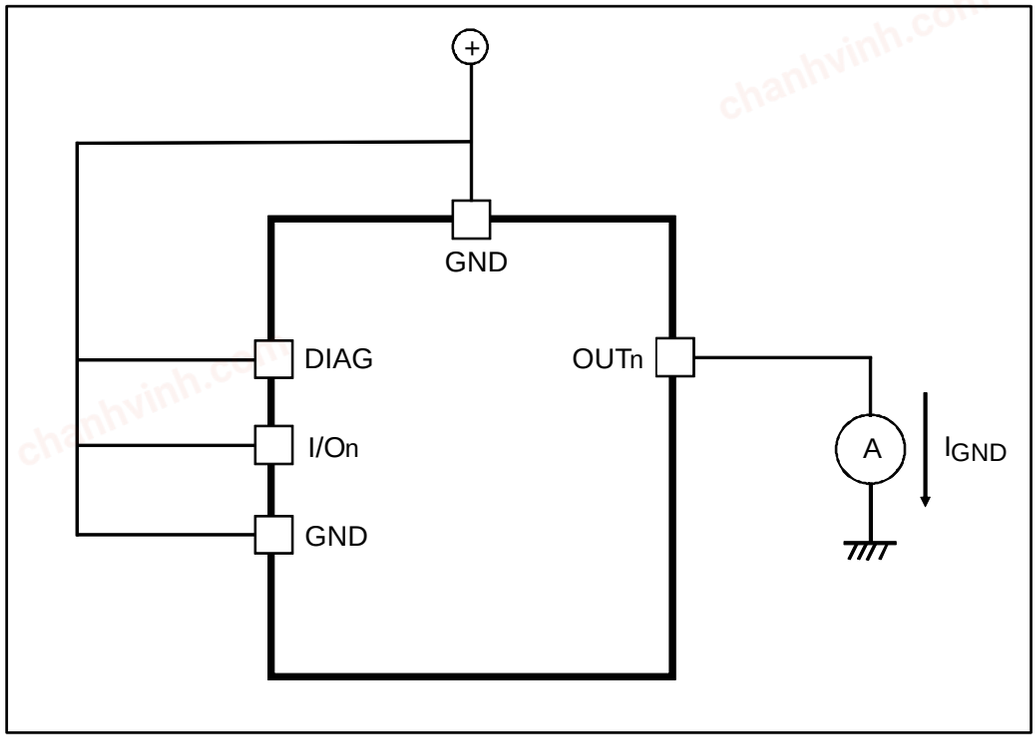


Figure 5: Peak short-circuit test diagram



chanhvinh.com

Figure 6: I_{LGND} test configuration



chanhvinh.com

6 Switching time waveforms and truth table

Figure 7: Switching waveforms

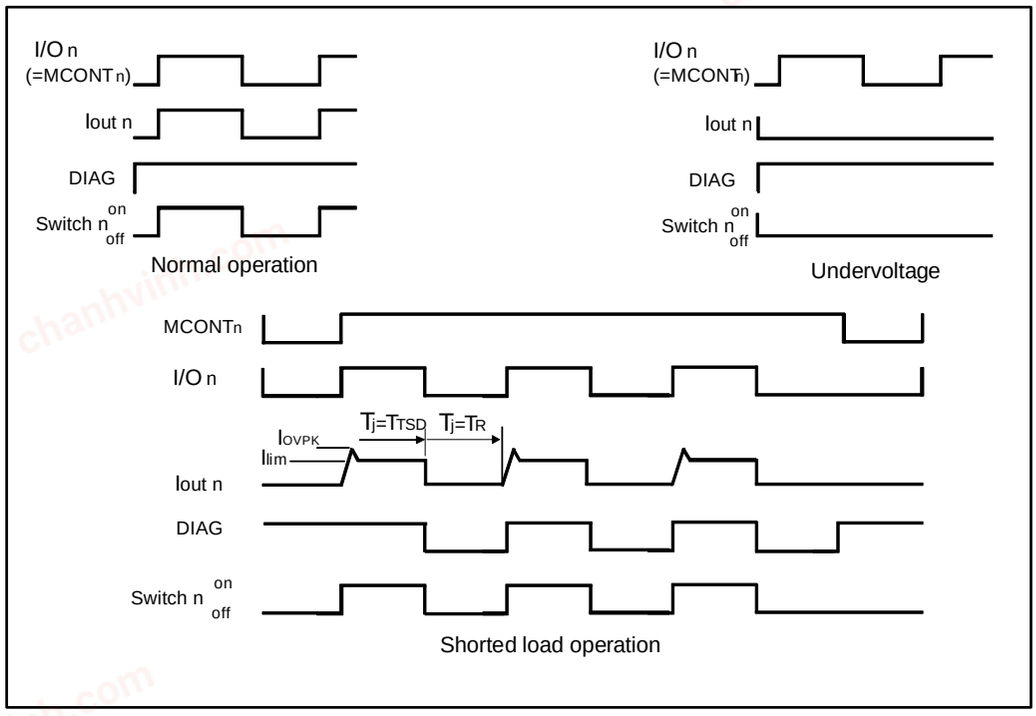
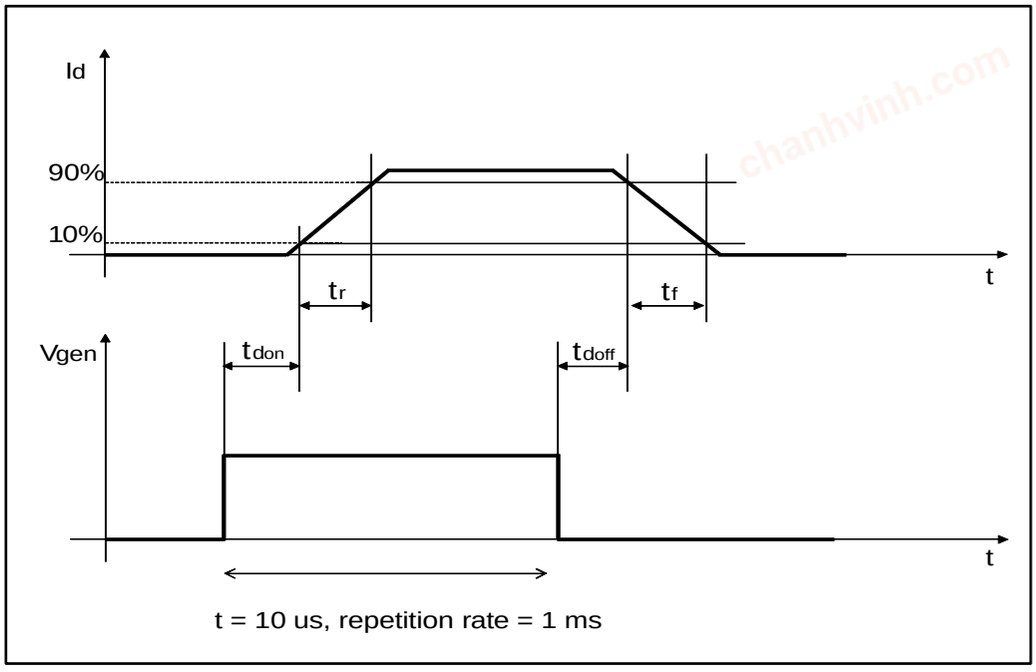


Figure 8: Switching parameter test conditions

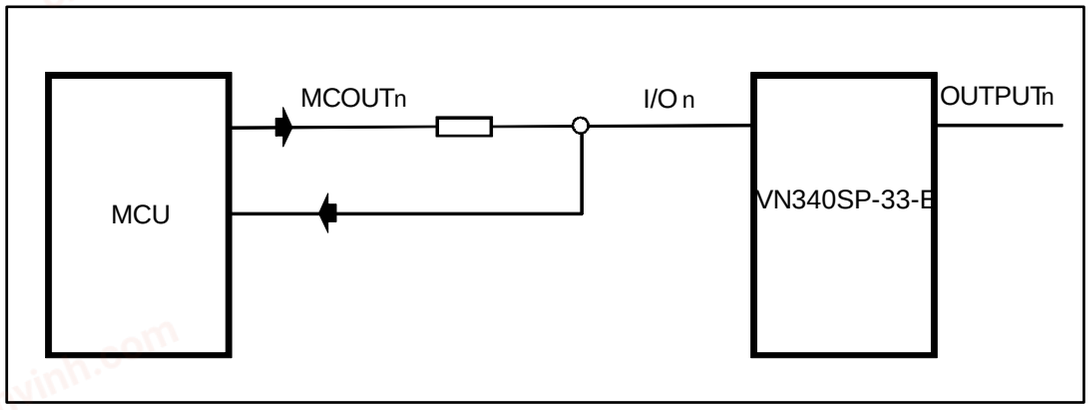


chanhvinh.com

Table 8: Truth table

Conditions	MCOUTn	I/On	OUTPUTn	Diagnostic
Normal operation	L	L	L	H
	H	H	H	H
Junction overtemperature	L	L	L	H
	H	L	L	L
Undervoltage	L	L	L	H
	H	H	L	H
Shorted load current limitation	L	L	L	H
	H	H	H	H

Figure 9: Driving circuit



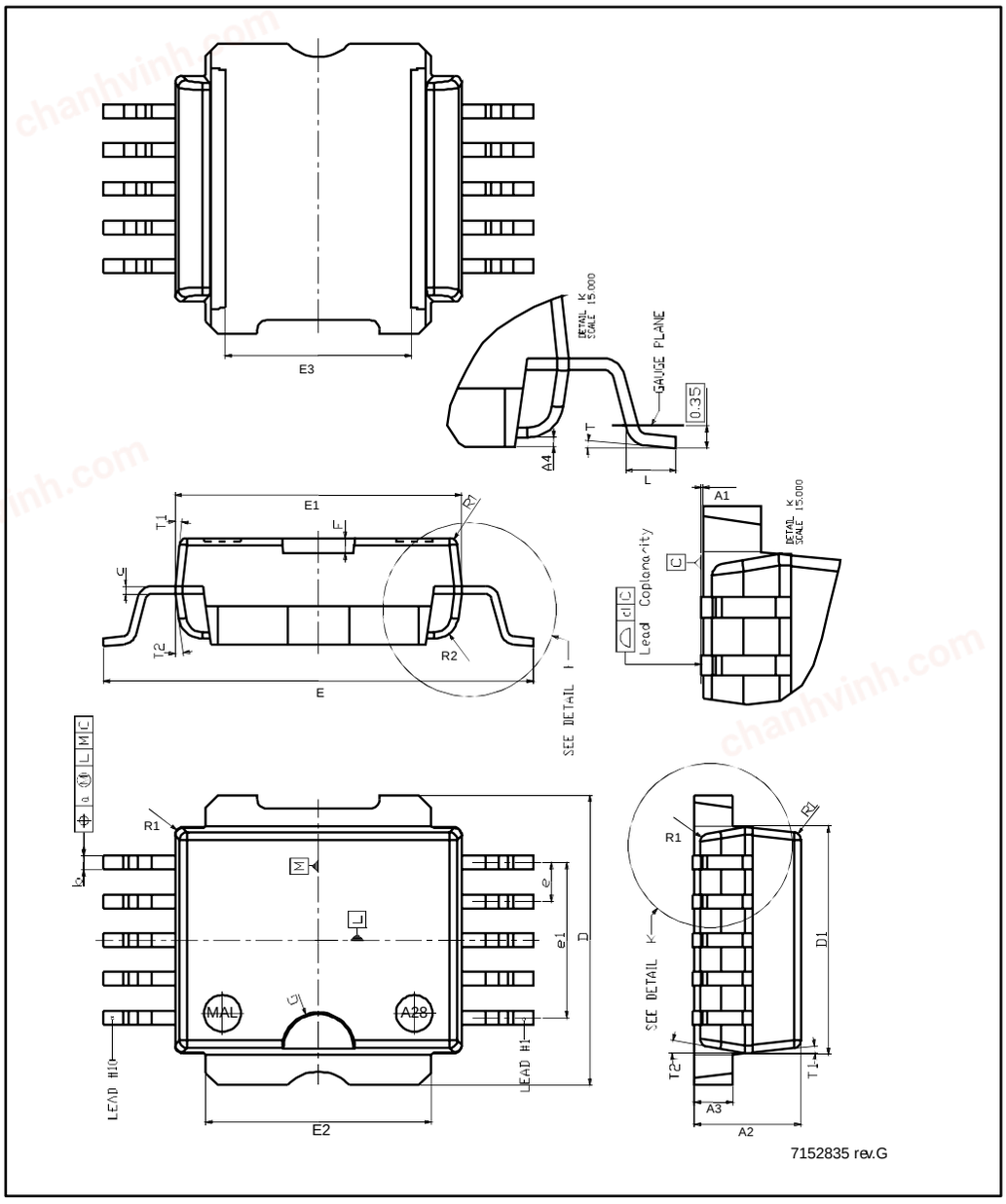
chanhvinh.com

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 PowerSO-10 package information

Figure 10: PowerSO-10 package outline



chanhvinh.com

Table 9: PowerSO-10 package mechanical data

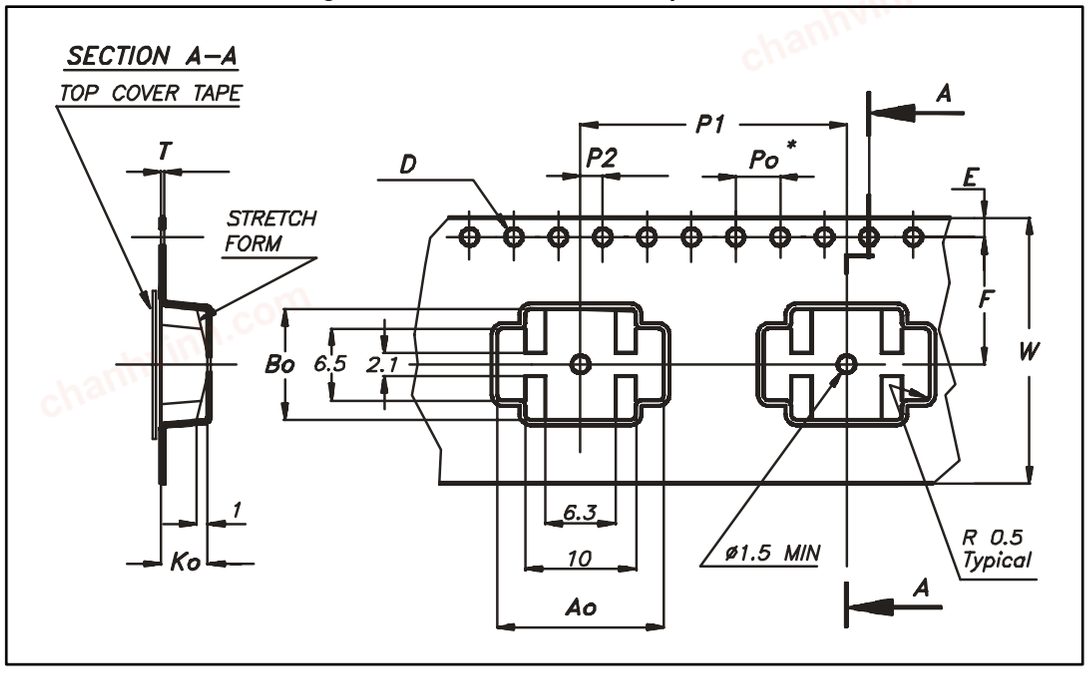
Dim.	mm		
	Min.	Typ.	Max.
A1	0.01	0.05	0.08
A2	3.45	3.5	3.55
A3	1.24	1.28	1.32
A4	0.15	0.2	0.25
a		0.2	
b	0.4	0.45	0.5
c	0.24	0.27	0.3
D	9.45	9.52	9.59
D1	7.42	7.5	7.58
d	0	0.04	0.09
E	13.9	14.1	14.3
E1[a]	9.33	9.4	9.47
E2	7.4	7.42	7.5
E3	5.95	6.1	6.25
e	1.22	1.27	1.32
e1		5.08	
F		0.5	
G		1.2	
L	0.85	1	1.1
R1			0.25
R2		0.8	
T	3 deg	5 deg	7 deg
T1		6 deg	
T2		10deg	

[a] Resin protrusions are not included (max. value: 0.15 mm per side).

chanhvinh.com

7.2 PowerSO-10 packing information

Figure 11: PowerSO-10 career tape outline



Drawing is not in scale

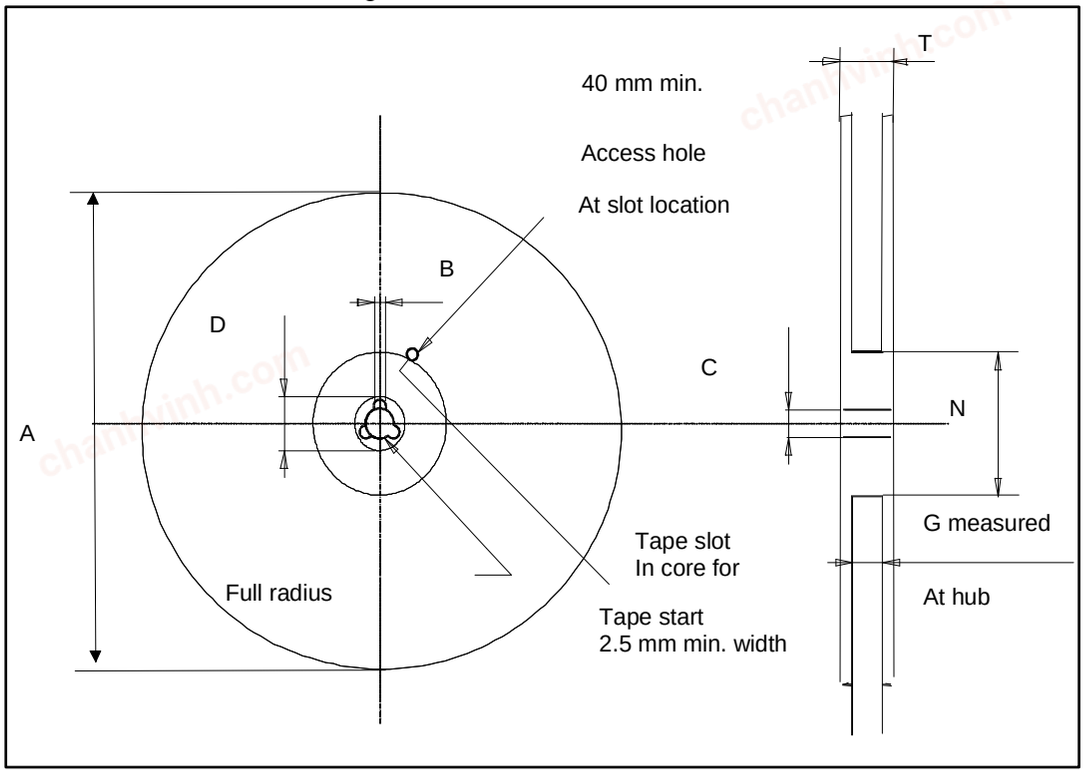
Table 10: PowerSO-10 career tape dimension mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	14.9	15.0	15.1
B0	9.9	10.0	10.1
K0	4.15	4.25	4.35
F	11.4	11.5	11.6
E	1.65	1.75	1.85
W	23.7	24.0	24.3
P2	1.9	2.0	2.1
P0	3.9	4.0	4.1
P1	23.9	24.0	24.1
T	0.025	0.30	0.35
D(Ø)	1.50	1.55	1.60

10 sprocket hole pitch cumulative tolerance ±0.2 mm

chanhvinh.com

Figure 12: PowerSO-10 reel outline



Drawing is not in scale

Table 11: PowerSO-10 reel dimension mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
B	1.5		
C	12.8	13	13.2
D	20.2		
N	60		
G	23.7	24.4	
T			30.4

10 sprocket hole pitch cumulative tolerance ±0.2 mm

Table 12: PowerSO-10 base and bulk quantity

Base quantity	Bulk quantity
600	600

chanhvinh.com

8 Revision history

Table 13: Document revision history

Date	Revision	Changes
05-Sep-2005	1	Initial release.
19-Mar-2007	2	Document reformatted, typo in note 1.
22-Aug-2008	3	Updated table 9.
07-Sep-2015	4	Updated the table of absolute maximum ratings.

chanhvinh.com

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved