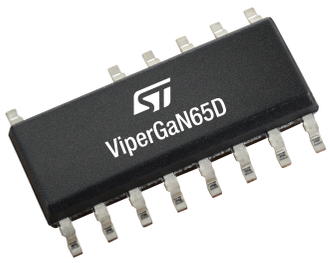
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VIPERGAN65D

Datasheet

Advanced quasi-resonant offline high voltage converter with E-mode GaN HEMT



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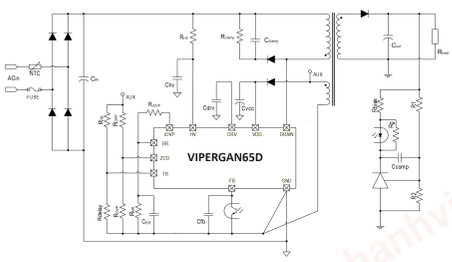
Product status link

VIPERGAN65D

Product label

SUSTAINABLE TECHNOLOGY

Figure 1. Typical application



Features

- Quasi-resonant (QR) flyback controller
- 700 V E-mode power GaN transistor
- Embedded sense FET
- Dynamic blanking time and adjustable valley synchronization delay functions, to maximize efficiency at any input line and load condition
- Valley-lock to ensure constant valley skipping
- Advanced power management for less than 30 mW standby power consumption with adaptive burst-mode
- Output overvoltage protection (OVP)
- Input voltage feed-forward compensation for mains independent OPP variation
- Brown-in and brown-out protection
- Input overvoltage protection (iOVP)
- Output overload protection (OVL)
- Output rectifier short circuit protection (OCP_LEB)
- Embedded thermal shutdown
- Frequency jitter for EMI suppression

Applications

- High efficiency power adapters
- Fast battery chargers
- Auxiliary power supply for appliances, industrial, consumers, lighting

Description

The VIPERGAN65D is a high voltage converter, designed for medium power quasi-resonant ZVS (Zero Voltage Switching at switch turn-on) flyback converters, capable to provide an output power up to 65 W in wide range.

It integrates a complete set of features that provide an extremely flexible and easy to use chip and helps to design a highly efficient offline power supply. The ZVS quasi-resonant operation with the dynamic blanking time feature and the valley synchronization function, that turns on the power switch always at the valley of the drain resonance, reduces the switching losses and maximizes the overall efficiency at any input line and load condition. The advanced power management with the low quiescent helps to achieve low stand-by consumptions. The feed-forward compensation minimizes the maximum output peak power variation over the entire input voltage range.

In addition to the above functions, the device offers protection features that considerably increase end-product's safety and reliability: the output overvoltage protection (OVP), the overload protection (OLP), the brown-in/out protection, that set the input voltage level to power on and power off the converter and the input overvoltage protection (iOVP), that protects the system in case of an abnormal increase of the input line. All the protections are auto-restart mode.

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1 Pin connections and function

Figure 2. **Connection diagram (top view)**

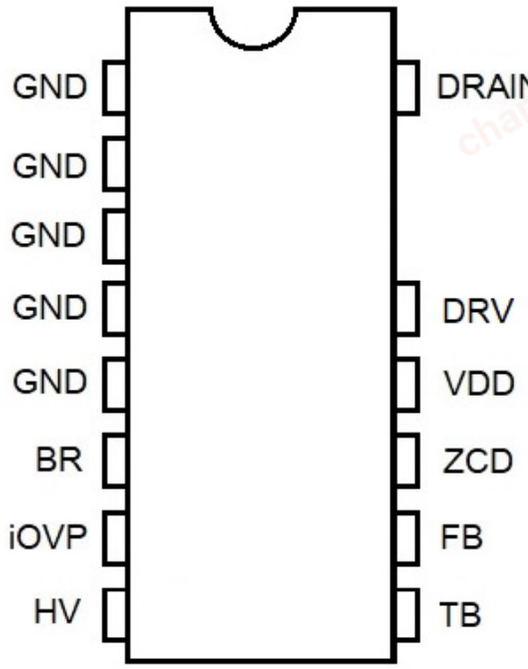


Table 1. **Pin function**

Pin N.	Name	Function
1,2,3,4, 5	GND	**Device ground for current return.**
6	BR	**Input brown-in and brown-out protection**. A 10nF capacitor between this pin and GND is required. If the feature is not used, the pin must be connected to GND.
7	iOVP	**Input OVP protection.** If the feature is not required, the pin must be connected to BR.
8	HV	**Start-up pin.** Connect to the main through a resistor to provide the bias to the HV start-up generator. It is also used as upper resistor to set the BR and iOVP functions. Select a value in the range 10-30 MΩ to minimize the residual consumptions. A 220 pF ceramic capacitor must be connected between this pin and GND for proper functionality of high voltage start-up control logic.
9	TB	**Blanking time adjustment and valley synchronization.** During on-time, a resistor connected between TB and the auxiliary winding increases the blanking time proportionally to the input voltage, to reduce the switching losses at high line. During off-time, a voltage divider connected to the auxiliary winding, allows adjusting the turn-on delay time after demagnetization, to precisely synchronize the GaN turn-on with the valley of the resonance. Connect the pin to GND if both functions are not used.
10	FB	**Feedback.** This pin is used to set the peak current value required by the control loop for a given output load. The pin is the input for the optocoupler. A level 100 mV below the threshold V_{FBB} activates the burst mode operation. A level close to the threshold V_{FBH} approaches the cycle-by-cycle overcurrent set point.
11	ZCD	**ZCD.** Transformer's demagnetization sensing for quasi-resonant operation. A voltage divider must be connected among auxiliary windings, ZCD, and GND. A negative-going edge across the pin triggers GaN turn-on.

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Pin N.	Name	Function
		During GaN's on-time, the current sourced by the pin is monitored to get an image of the input voltage to the converter, used for feed-forward compensation. During GaN's off-time, a voltage exceeding the OVP threshold shuts the IC down reducing the device consumption. This function is strobed and digitally filtered for high noise immunity.
12	VDD	**Controller supply.** An electrolytic capacitor, connected between this pin and GND, is initially charged by the internal HV start-up generator. A 100 nF ceramic cap between VDD and GND, as close as possible to the IC, might be required to reject high frequency disturbances from internal circuitries.
13	DRV	**GaN driver section supply.** An internal voltage regulator tightly sets the driving voltage for GaN to 6 V to obtain the best performance. A low ESR/ESL 1 µF ceramic capacitor placed between this pin and GND is required.
14	DRAIN	**Drain pin of the GaN switch**

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2 Electrical data

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value		Unit
			Min.	Max.	
V_{DRAIN}	14	Drain blocking DC voltage		700	V
		Drain transient voltage (Tpulse < 1µs)		850	
	6, 10	Analog Inputs & Outputs	-0.3	3.6	V
I_{ZCD}	11	Zero Current Detector current	-3	3	mA
I_{TB}	9	TB current	-3	3	mA
V_{DD}	12	Supply Voltage (IDD < 25mA)	-0.3	Self-limited	V
I_{DD}	12	Device supply current + internal zener capability		25	mA
I_{DRV}	13	Device supply current + external load		5	mA
V_{iOVP}	7	iOVP configuration according to Figure 28, Figure 29 or Figure 30		10	V
		iOVP externally biased		6	
V_{HV}	8	Startup pin	-0.3	Self-limited	
T_J		Junction Temperature Range	-40	150	°C
T_{STG}		Storage Temperature	-55	150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
R_{TH-JEP}	Thermal resistance junction to Exposed Pad (1)	1.5	°C/W
R_{TH-JA}	Thermal resistance junction to ambient (1)	32	°C/W

1. *Pdiss = 1 W – Natural Convection - Board: 11.4 mm x 7.6 mm FR4, 4 layer, 2 oz copper.*

2.3 Typical power capability

Table 4. Typical power capability

85-265 V_{AC}(1)	185-265 V_{AC}(1)
65 W	85 W

1. *Typical maximum output power rating in adapter design at 50°C ambient with adequate heatsinking.*

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3 Electrical characteristics

Table 5. Electrical characteristics

T_J = -25 °C to 125 °C, V_{DD}=14 V, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Power section						
$V_{(BL)DS}$	Drain-source blocking voltage	I_D < 12 uA	700			V
I_{DSS}	Off-state drain current	V_{DRAIN} = 700 V, LS On, HS Off, T_J = 25 °C		0.6	12	µA
		V_{DRAIN} = 700 V, LS On, HS Off, T_J = 125 °C		100		
$R_{DS(ON)HS}$	HS drain-source on-state resistance	T_J = 25 °C; I_D = 2 A		270	350	mΩ
		T_J = 125 °C; I_D = 2 A		580		
$R_{DS(ON)LS}$	LS drain-source on-state resistance	T_j = 25 °C, I_D = 2 A		72		mΩ
High voltage start-up generator						
V_{START}	Drain-source start voltage	R_{HV} = 10 MΩ, T_J = 25 °C			34.5	V
		R_{HV} = 20 MΩ, T_J = 25 °C			41	
I_{CHARGE}	V_{DD} start-up charge current	V_{DD} ≤ $V_{DD-FOLD}$	0.4	0.65	0.9	mA
		$V_{DD-FOLD}$ < V_{DD} <V_{DD-ON}	2.6	3.55	4.5	
I_{HV}	HV off current	V_{HV} = 22 V, T_J = 25 °C		124		nA
$V_{DD-FOLD}$	V_{DD} foldback threshold		1	1.4	2	V
Supply voltage						
V_{DD}	Operating range	After turn-on	9		23	V
V_{DRV-op}	Operating range	After turn-on	5.7		6.3	V
V_{DD-ON}	Turn-on threshold		14	15	16	V
V_{DD-OFF}	Turn-off threshold		7.5	8	8.5	V
$V_{DD-RESTART}$	Restart threshold		6.5	7	7.5	V
$V_{DD-ONREG}$	VDD voltage for regulator turn-on	V_{DD} rising after V_{UVLO}	6.5	7	7.5	V
V_{DD-CL}	V_{DD} clamping voltage	I_{DD} = 25 mA	23.8	25	27.2	V
V_{DRV}	Driver regulation voltage	I_{DRV} = 2 mA	5.7	6	6.3	V
V_{DRV-OK}	Driver UVLO voltage	Rising voltage	5.2		5.7	V
		Hysteresis		0.2		V
$V_{DRV-OVP}$	Driver OVP voltage	Rising voltage	6.8		7.5	V
$V_{DRV-HYST}$	Driver OVP hysteresis	Hysteresis		0.3		V
$I_{DRV-MAX}$	Driver short-circuit current	DRV = GND	4			mA
I_{DD-CL}	Shutdown clamping current		20	26	32	mA
T_{DD-CL}	Shutdown clamping delay			100		µs

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Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply current						
I_Q	Quiescent current	Burst-mode operation			900	µA
I_{DD}	Operating supply current	TB=GND; F_{SW} = 100 kHz Including DRV supply current, VFB = 0.9 V			3.2	mA
$I_{DD-FAULT}$	Fault quiescent current	$V_{DD} > V_{DD-OFF}$			620	µA
Current limitation						
I_{DLIM}	Drain current limitation	V_{FB} = 3.1 V	3.318	3.5	3.682	A
I_{OCP_LEB}	OCP_LEB current threshold			2.69		A
I_{BM}	Bust-mode current	V_{FB} = 0.7 V	718	840	956	mA
T_{SS}	Soft-start time			8		ms
T_D	Propagation delay	dI_{DRAIN}/dt = 50 mA/µs			150	ns
T_{LEB}	Leading-edge blanking		163	170	220	ns
T_{ON-MIN}	Minimum turn-on time	dI_{DRAIN}/dt = 50 mA/µs		260	350	ns
Startup timers and frequency limit						
F_{LIM_MAX}	Max internal frequency limit	TB = GND	176	240	330	kHz
Zero current detector						
I_{ZCDB}	Input bias current	V_{ZCD} = 0.1 to 2.7 V			1	µA
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 1 mA	3		3.5	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = -1 mA		-60		mV
V_{ZCDA}	Arming voltage	positive-going edge	100	110	120	mV
V_{ZCDT}	Triggering voltage	Negative-going edge	50	60	70	mV
T_{BLANK}	Trigger blanking time after GaN's turn-on	V_{FB}>= V_{FBR} , I_{TB-neg} = 0	3.04	4.16	5.66	µs
		V_{FB}>= V_{FBR} , I_{TB-neg} = 1 mA	10	15	20	
		V_{FB} = V_{FBB}	12	16	20	
T_{FORCE}	Force turn-on time after blanking	After soft-start	2	2.7	3.4	µs
		During soft-start		23		
Compensation						
V_{FBH}	Upper saturation		3			V
V_{FBR}	Frequency reduction threshold		0.98	1.15	1.32	V
V_{FBB}	Burst-mode threshold		0.63	0.7	0.77	V
V_{HYST}	Burst-mode hysteresis			60		mV
G_{FB}	Voltage to R_{FF} current			49.4		µA/V
R_{FF}	FB internal current sense resistor			1.55		kΩ
H_{FB}	Current sense gain			1.011		V/A

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Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{FB}	Source current	V_{FB} = 0 V	70	100	130	µA
R_{FB}	Dynamic feedback resistor			15		kΩ
Dynamic blanking time and turn-on delay setting						
K_{BLANK}	Blanking time gain	I_{TB} = 10 µA to 1 mA	7.64	10.91	14.18	µs/mA
V_{TBH}	TB upper clamp voltage	I_{TB} = 1 mA	3.1	3.3	3.5	V
V_{TBL}	TB lower clamp voltage	I_{TB} = 1 mA	-30		20	mV
$V_{D-ON(MIN)}$	TB lower delay voltage			0.6		V
$V_{D-ON(MAX)}$	TB upper delay voltage			2.6		V
$T_{D-ON(MIN)}$	Minimum turn-on delay time after triggering	$V_{TB} \leq V_{D-ON(MIN)}$		197		ns
$T_{D-ON(MAX)}$	Minimum turn-on delay time after triggering	$V_{TB} \geq V_{D-ON(MAX)}$		1.1		µs
V_{TB-DIS}	Disable TB pin voltage		80	100	120	mV
I_{TB-DIS}	Disable TB current		160	200	240	µA
Output overvoltage protection						
V_{OVP}	Output OVP threshold		2.375	2.5	2.625	V
Line voltage feed-forward						
α_{FF}	Feed-forward current modulation gain	V_{FB}>1.2 V	44	55	66	µA/mA
		V_{FB}<0.8 V	8.8	11	13.2	
Overload protection						
T_{OVL}	Overload time			50		ms
$T_{RESTART}$	Restart time after fault			1		s
Brown-in/out and input OVP						
V_{BR-IN}	Brown-in threshold		0.475	0.5	0.525	V
V_{BR-OUT}	Brown-out threshold		0.38	0.4	0.42	V
V_{BR-DIS}	Brown-in/out disable voltage		80	100	120	mV
I_{BR-DIS}	Brown-in/out disable current		12	15	18	µA
T_{BR-IN}	Brown-in delay time		200	250	300	µs
T_{BR-OUT}	Brown-out delay time		24	30	36	ms
V_{iOVP_th}	Input OVP threshold		4.75	5	5.25	V
T_{iOVP}	Input OVP delay time		200	250	300	µs
Frequency jittering						

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Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_D	Modulation frequency			10		kHz
D_{FD}	Modulation duty-cycle			50		%
ΔIpk	Peak current change			5		%
Thermal shutdown						
T_{SD}	Thermal shutdown temperature	Guaranteed by design and characterization	125	140	155	°C
$T_{SD-REST}$	Restart time after OTP and OCP_LEB activation			2		s

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4 Typical electrical characteristics

Figure 3. Typ. I_{DLIM} vs. T_J

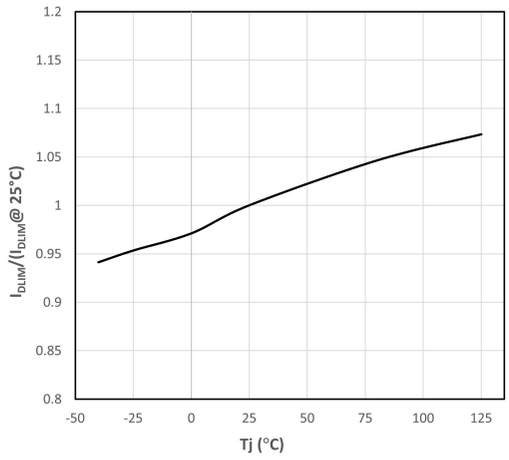


Figure 4. V_{START} vs. T_J @10 MΩ and 20 MΩ

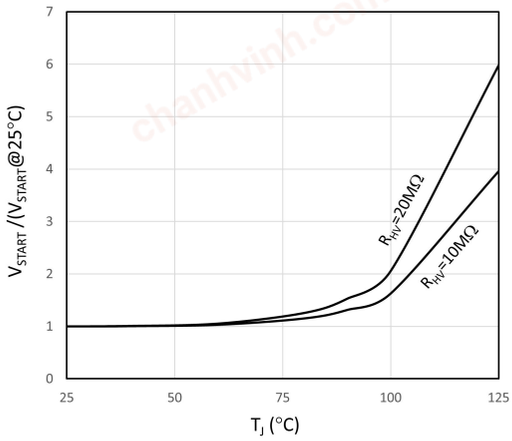


Figure 5. Typ. $R_{DS(ON)}$ vs. I_D

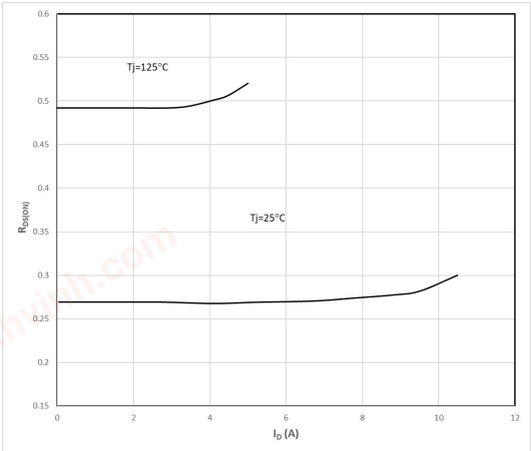


Figure 6. Typ. $R_{DS(ON)}$ vs. T_J

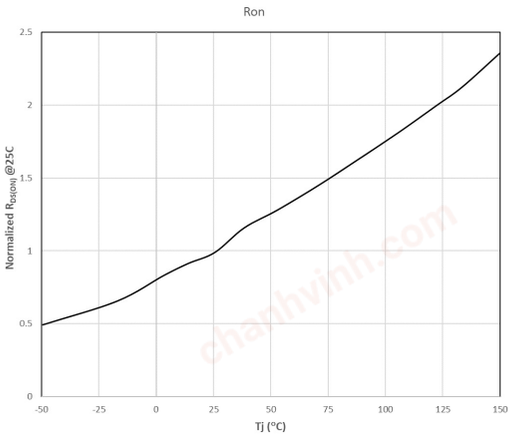


Figure 7. Typ. I_D vs. V_{DS}

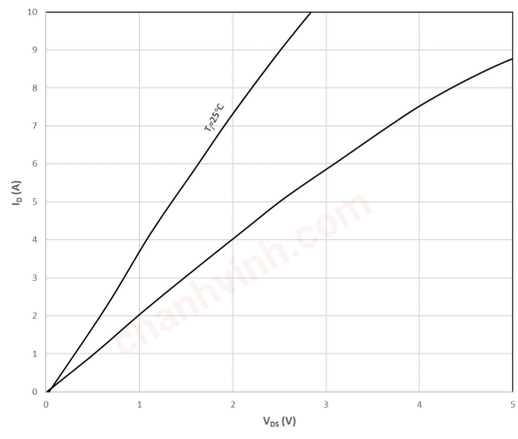
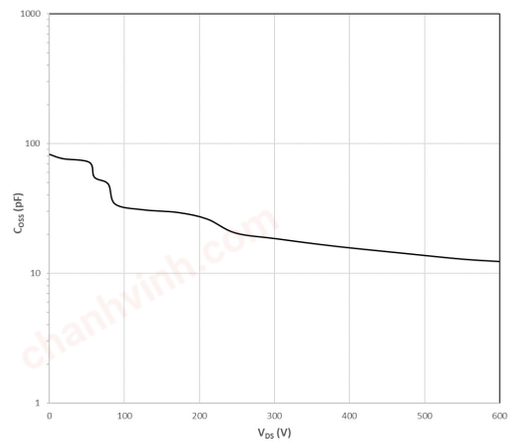
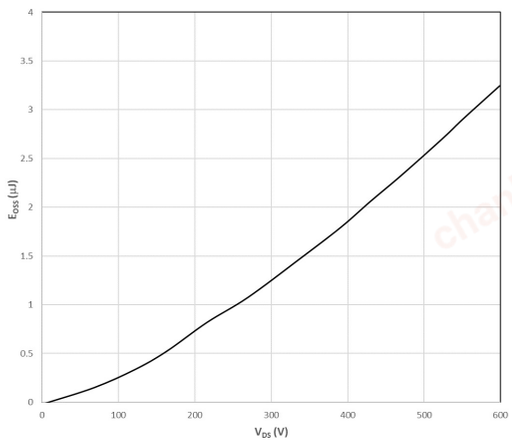


Figure 8. Typ. C_{OSS} vs. V_{DS}



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Figure 9. Typ. E_{OSS} vs. V_{DS}



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5 Application information

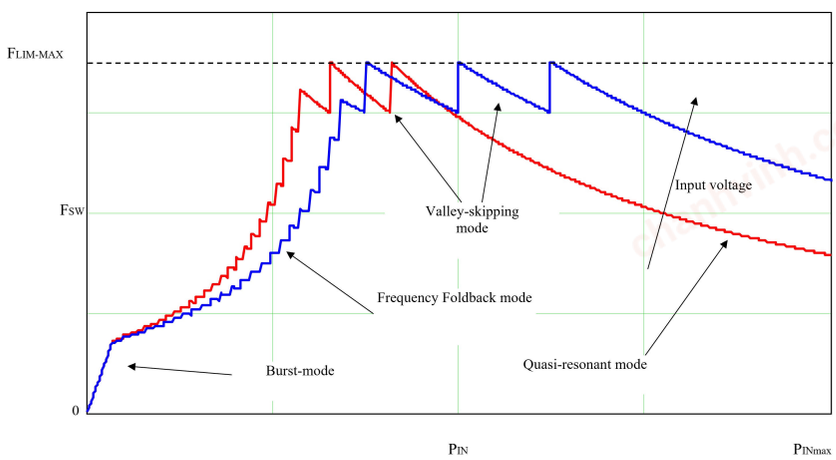
5.1 Multi-mode operations

The VIPERGAN65D is an offline Quasi-Resonant ZVS (Valley Switching at switch turn-on) flyback converter.

Depending on the converter's load condition, the device is able to work in different modes (see Figure 10):

1. QR mode at heavy load. Quasi-resonant operation is achieved by synchronizing the GaN turn-on to the transformer demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. The system then works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency is different for different line/load conditions (see the hyperbolic-like portion of the curves in Figure 10). The minimum turn-on losses, low EMI emission and safe behavior in short-circuit are the main benefits of this kind of operation.
2. Valley-skipping mode at heavy/medium load. The device defines the maximum operating frequency of the converter. As the load is reduced the GaN turn-on no longer occurs on the first valley but on the second one, the third one and so on. In this way the switching frequency no longer increases, limiting the switching losses.
3. Frequency foldback mode at medium/light load. The maximum switching frequency limit is progressively reduced with the FB pin voltage, still maintaining ZVS operation. This maximizes efficiency at light load, still ensuring noise-free operations, since the switching frequency is bottom limited above the audible frequency range.
4. Burst-mode with no or very light load. When the load is extremely light or disconnected, the converter enters a controlled on/off operation with constant peak current. Decreasing the load then results in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. As the peak current is very low, no issue of audible noise arises.

Figure 10. Multi-mode operation of VIPERGAN65D



5.2 High voltage start-up generator and supply structures

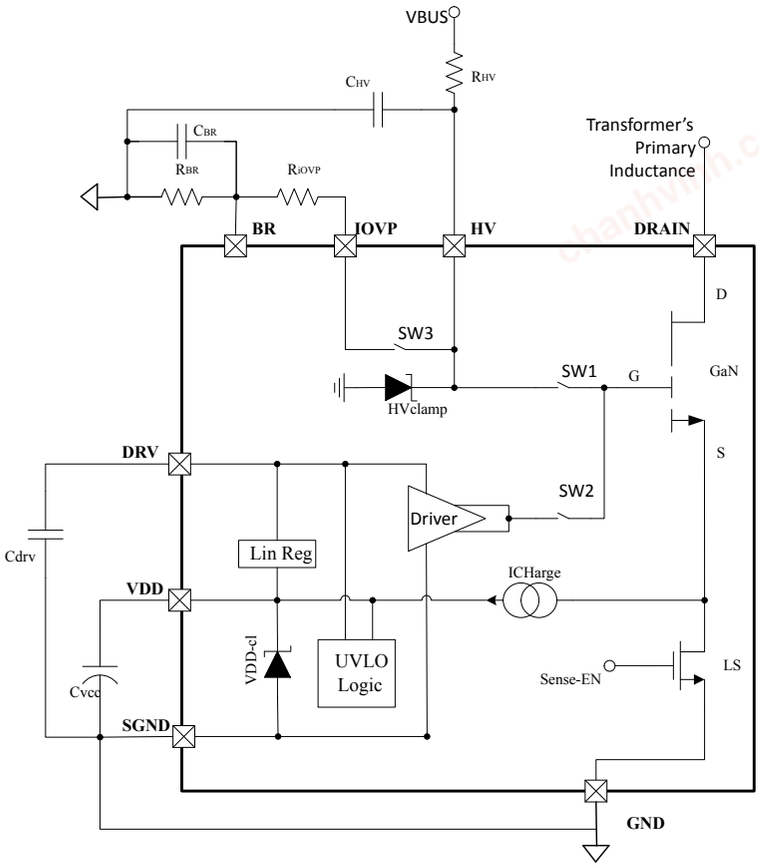
Based on a double FET structure, the HV current generator is supplied through the DRAIN pin and is used to start up the device.

The internal schematic is shown in Figure 11. Before startup, the switch SW1 is closed, SW2 and SW3 are open, whereas the low-side MOSFET (LS MOSFET) is open.

When the power is applied to the circuit, the gate of the high-side GaN (HS GaN) is pulled up through the resistor R_{HV} and capacitor C_{HV}. If the voltage is high enough, the internal current generator draws the current I_{CHARGE} (3.55 mA typ.) to charge the capacitor connected between V_{DD} and GND. To avoid excessive IC dissipation in case V_{DD} is accidentally shorted to GND, this current is initially reduced to 0.6 mA, until V_{DD} is lower than $V_{DD-FOLD}$.

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Figure 11. **High voltage start-up generator: internal schematic and pin configuration**



Once V_{DD} reaches the $V_{DD-ONREG}$ threshold, the linear regulator that feeds the DRV pin is turned on and DRV voltage is charged.

Once V_{DD} reaches the start-up threshold V_{DD-ON}:

1. The control logic disables the internal current generator;
2. The switch SW1 is open and the HV pin is clamped to 27 V through HVclamp;
3. The switch SW2 is closed to pull the GaN gate to zero;
4. The switch SW3 is closed, internally connecting the pins HV and iOVP;
5. Finally, the LS MOSFET is turned on and its drain-to-source resistance $R_{DS(ON)LS}$ is used as sense resistor.

The switching activity can commence only if V_{DRV} is higher than the V_{DRV-OK} threshold.

The DRV pin voltage is not upper limited, but the driver does not transfer gate signal if V_{DRV} is accidentally set to a voltage higher than 7 V typ.

The DRV linear regulator could experience voltage drops due to insufficient V_{DD} or excess of loading. To avoid incorrect GaN driving, the switching activity is interrupted if V_{DRV} drops below (V_{DRV-OK} – Hysteresis).

In case of V_{DD} reduction below V_{DD-OFF}, the switching activity is immediately interrupted and the GaN is converted to operate as high voltage startup.

The UVLO threshold is used to completely reset the internal logic when crossed downwards.

While the current generator is off, the residual consumption is few mWs depending on the value of the resistor R_{HV}; values in the range 10 to 30 MΩ help to minimize the residual losses, even if lower values may be required if the IC must operate at extremely low input voltage.

At power-down, the converter activity stops as the input voltage falls below V_{START} and V_{DD} below V_{DD-OFF}.

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5.3 Zero current detection and triggering block

The zero current detection (ZCD) and triggering block switches on the power GaN if a negative-going edge falling below 60 mV is applied to the ZCD pin. To do so, the triggering block must be previously armed by a positive-going edge exceeding 110 mV.

This feature is used to detect transformer demagnetization for the QR operation, where the signal for the ZCD input is obtained from the transformer auxiliary windings used also to supply the IC.

The triggering block is blanked after GaN turn-on to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously.

The switching frequency is top limited below 240 kHz.

To prevent the tendency of the system to excessively increase the frequency at light load, a variable blanking time, a function of the FB pin voltage, is implemented. This blanking time is maximum for $V_{FB} = V_{FBB}$ and decreases linearly down to the minimum for $V_{FB} = V_{FBR}$.

In QR systems the switching frequency also increases with the input line. To solve this issue, the VIPERGAN65 offers a special dynamic blanking time function, which reduces the maximum permitted switching frequency as the input line increases. This function is settable through the TB pin and is explained in the relevant section.

In this way, the switching frequency is progressively reduced with the input voltage and output load, resulting in lower frequency-related losses.

If the demagnetization completes - hence a negative-going edge appears on the ZCD pin - after a time exceeding time T_{BLANK} from the previous turn-on, the GaN is turned on again, with some delay to ensure minimum voltage at turn-on (“QR mode”).

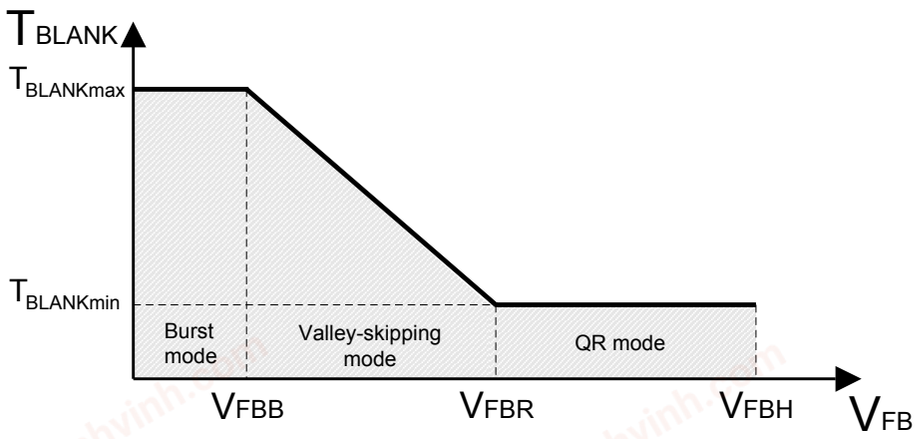
If the negative-going edge appears before T_{BLANK} has elapsed, it is ignored and only the first negative-going edge after T_{BLANK} turns on the GaN. In this way one or more drain ringing cycles is skipped (“valley-skipping mode”) and the switching frequency is prevented from exceeding $1/T_{BLANK}$.

The blanking time limits and the mode of operation are reported in Figure 12.

In case the amplitude of residual oscillation on ZCD is not enough to trigger again the switching (it could happen during low frequency operation), an internal function forces the GaN to turn on, T_{FORCE} after the blanking time is elapsed. A starter block is also used to start up the system when the signal on the ZCD pin is not high enough to trigger the GaN. After the first few cycles initiated by the starter, as the voltage developed across the auxiliary winding becomes large enough to arm the ZCD circuit, the GaN's turn-on starts to be locked to transformer demagnetization, hence setting up the QR operation.

The ZCD pin voltage is both top and bottom limited by a double clamp. The upper clamp is typically located at 3 V, the lower clamp at -60 mV. The interface between the pin and the auxiliary winding is a resistor divider. Its resistance ratio as well as the individual resistance values are properly chosen, see “Section 5.6” and “Section 5.11”.

Figure 12. Frequency limits and modes of operations



5.4 Valley-lock feature

When the system operates in the valley skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the off-time of the GaN is allowed to change with discrete steps of one ringing cycle, while the off-time needed for cycle-by-cycle energy balance may fall in between. Thus, one or more longer switching cycles are compensated by one or more shorter cycles and vice versa.

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This “valley-jump” phenomenon introduces a low-frequency component in the primary current that may fall in the audible range and if this periodic perturbation is sufficiently large in amplitude, audible noise can be generated by mechanical vibrations of the magnetic components.

To avoid this phenomenon a new patent-pending valley-lock feature is implemented that, for a certain input voltage and output load condition, fixes the number of skipped valleys during valley skipping mode operation, regardless of the DC bus voltage ripple.

The function is disabled when the V_{FB} falls below 1.3 V and re-enabled again when V_{FB} increases up to 1.43 V (typ.)

5.5 Constant voltage operation and burst-mode

The FB pin is connected to an optocoupler, which transmits the error signal from the regulation loop located on the secondary side of the converter, see Figure 13. Typically, a TS431 is used as a voltage reference.

The FB pin is driven directly by the phototransistor's collector to modulate the duty cycle.

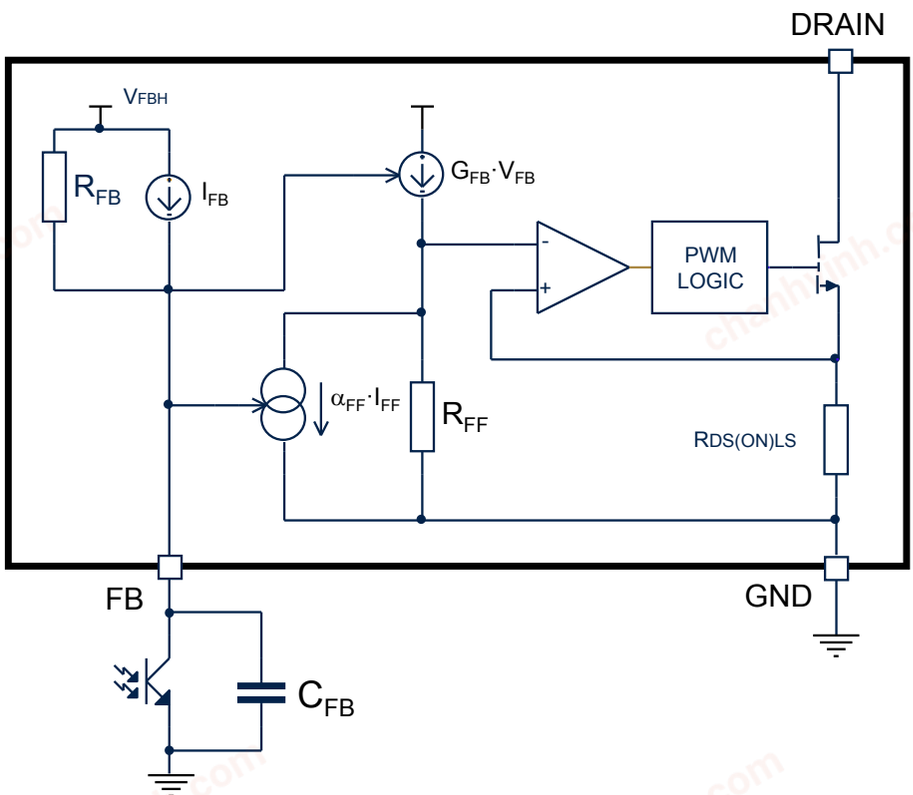
A capacitor across the pin is usually used to compensate the loop.

When the FB pin voltage falls 60 mV below V_{FBB}, the GaN is turned OFF and the IC consumption is reduced to I_Q to minimize the bias losses.

After the GaN turns OFF, the FB pin voltage increases as a reaction to the interruption of the energy delivery, and as it reaches V_{FBB} the device starts switching again.

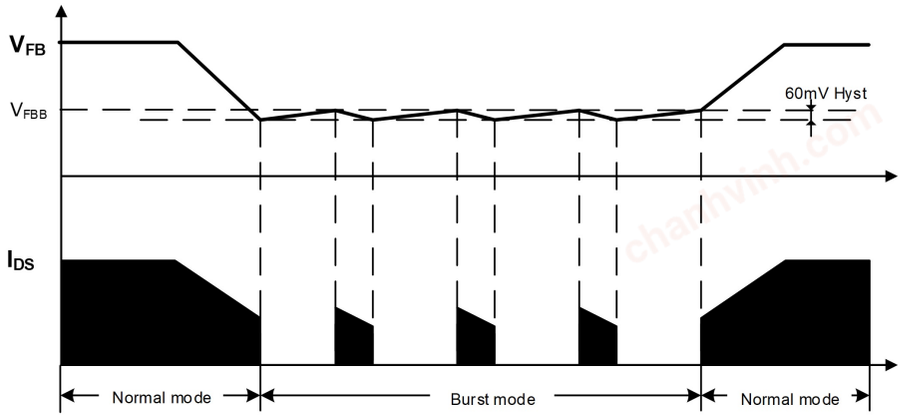
The effect of this burst-mode operation, shown in Figure 14, is to reduce the equivalent switching frequency, which can go down even to few hundred hertz, minimizing all frequency related losses and making it easier to comply with energy saving regulations. Also the low peak current ensures noise free operations.

Figure 13. Constant output voltage control principle: internal schematic and pin configuration



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Figure 14. **Burst-mode operation**



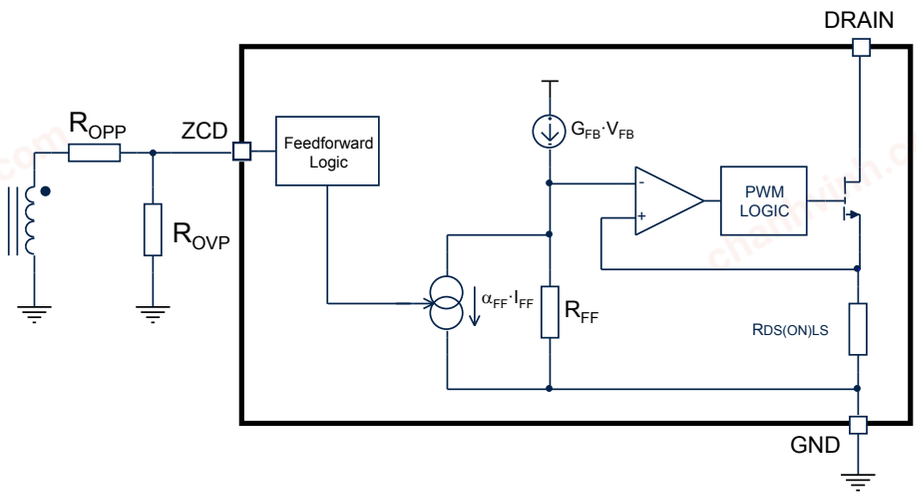
5.6 Line voltage feed-forward block

The power that a QR flyback converter with a fixed overcurrent set point can deliver changes considerably with the input voltage.

In wide-range mains applications, the deliverable power at high line can be more than twice than at minimum voltage. This is a problem because it means that at high line the system could be operated at a power level much higher than that which triggers overload at low lines, thus requiring an overrating of the power components.

The VIPERGAN65 implements a feed-forward function able to solve this issue: the voltage across the auxiliary winding is monitored and the information is used to compensate the converter (see Figure 15).

Figure 15. **Feed-forward compensation: simplified internal schematic and pin configuration.**



During GaN's on-time, the current sourced from the ZCD pin through the R_{OPP} resistor is mirrored inside the "Feed-forward Logic" block to provide a feed-forward current I_{FF}, proportional to the input voltage according to the formula:

Equation 1

$$I_{FF} = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{V_{IN}}{R_{OPP}} \quad (1)$$

where N_{AUX} and N_{PRI} are the turned number of the auxiliary and primary windings of the transformer respectively.

R_{OPP} value ensuring that the maximum deliverable output power is the same at the extremes of the input voltage range is referred to as $R_{OPP(OPT)}$ and can be calculated through the equation below:

Equation 2

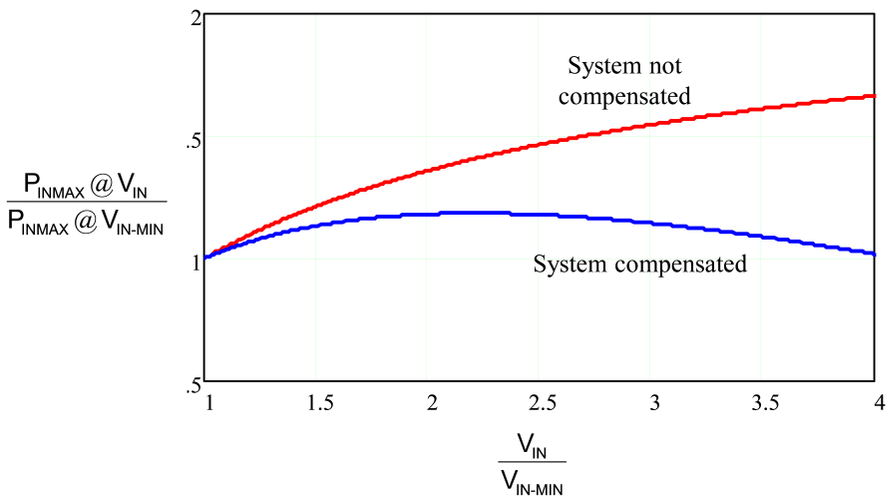
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$$R_{OPP(OPT)} = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{\alpha_{FF}}{G_{FB} \cdot V_{FBH}} \cdot \left(V_{INmin} + V_{INmax} + \frac{V_{INmin} \cdot V_{INmax}}{V_R} \right) \quad (2)$$

The $R_{OPP(OPT)}$ selection corresponds to the "system compensated" curve of Figure 16.

To minimize the difference between the power levels at which the converter enters burst mode at low line and high line, the effect of feedforward correction is linearly reduced as load decreases, from 100 % (at $V_{FB} \geq 1.2$ V) to 20 % (at $V_{FB} < 0.8$ V). The residual IFF in burst-mode ensures a certain level of compensation against the propagation delay TD.

Figure 16. Typical power capability variation vs. input voltage in QR flyback



The main effect of feedforward correction is to decrease the current setpoint as V_{IN} increases, and $R_{OPP(OPT)}$ could result into a too high I_{DLIM} reduction at V_{INmax} to supply the nominal output power, P_{OUTnom}.

If $I_{DRpk}(P_{OUTnom}, V_{INmax})$ is the DRAIN peak current value needed, the minimum value of R_{OPP} allowing to supply P_{OUTnom} at V_{INmax} is given by the following formula:

Equation 3

$$R_{OPP}(V_{INmax}) = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{\alpha_{FF} \cdot V_{INmax}}{G_{FB} \cdot V_{FBH} - I_{DRpk}(P_{OUTnom}, V_{INmax}) \cdot \frac{R_{DS(ON)LS}}{R_{FF}}} \quad (3)$$

At this point, if R_{OPP} is selected as:

Equation 4

$$R_{OPP} = \max\left(R_{OPP(OPT)}, R_{OPP(VINmax)}\right) \quad (4)$$

the nominal output power capability at V_{INmax} will be always guaranteed; and, if $R_{OPP(OPT)} > R_{OPP}(V_{INmax})$, also the power capability compensation at the extremes of the input voltage range.

5.7 Dynamic blanking time

Since the capacitive losses in a power system increase with the frequency, the tendency of the QR converters to increase the switching frequency with the input line is one of the major limitations to consider when designing high efficiency converters.

To solve this issue, the VIPERGAN65 offers a special dynamic blanking time function, which reduces the maximum permitted switching frequency as a function of the input line.

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Connecting the pin TB to the auxiliary winding through the resistor R_{TB}, the current sourced by the pin during the on-time, which is proportional to the input voltage, is sampled and used to adjust the blanking time during the off-time.

The advantage of this technique is that the frequency reduction is higher where mostly required, i.e., at high line, and minimum at low line.

The following equation can be used to dynamically adjust the dynamic blanking time $T_{BLANK(dyn)}$:

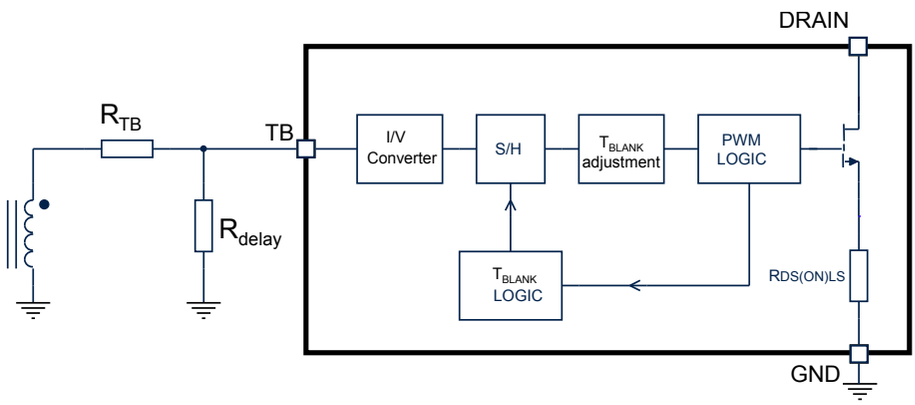
Equation 5

(5)

$$R_{TB} = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{K_{BLANK} \cdot V_{IN}}{T_{BLANK(dyn)} - T_{BLANK}}$$

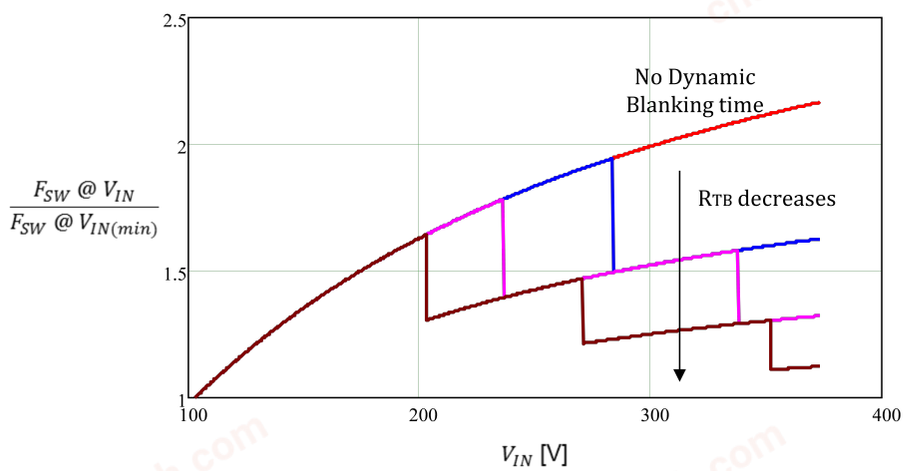
In this formula, T_{BLANK} is the default value at $V_{FB} \geq V_{FBR}$ and K_{BLANK} is the blanking time gain.

Figure 17. Dynamic blanking time: internal schematic and pin configuration



The result of such dynamic variation is shown in Figure 18: at low input line the switching frequency does not change (or changes slightly) compared to the case in which dynamic blanking time is not implemented, while decreases more and more as the input voltage increases.

Figure 18. Typical normalized switching frequency variation over the input voltage range



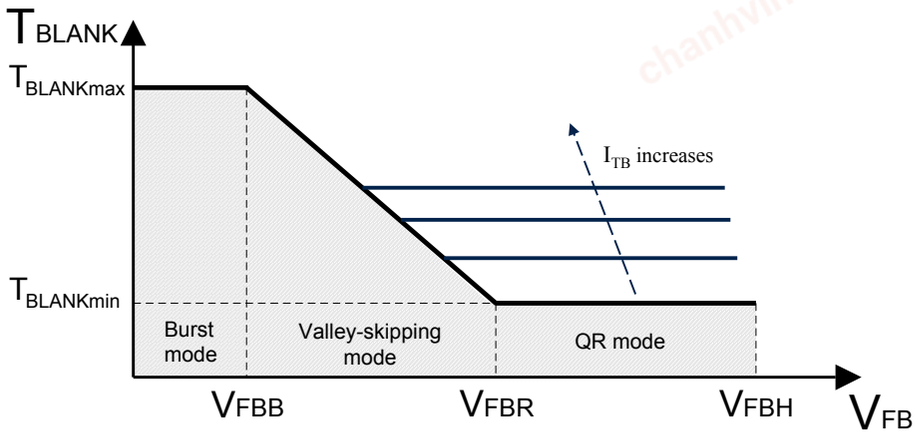
The function beneficially impacts also on the blanking time profile variation versus FB voltage, as shown in Figure 19: depending on the input voltage, the dynamic blanking time reduces the maximum permitted switching frequency also at medium/light load, thus further minimizing the related losses.

This method reduces the frequency variation span and, consequently, increases the peak of the primary side current. The Line Feed-forward compensation must be adjusted to guarantee the same power capability at any line condition.

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Dynamic blanking time and valley synchronization (see relevant section) functions can be disabled connecting the pin TB to ground. The decision if the function is used or not is taken at power-up: before the pin V_{DD} reaches the V_{DD-ON} threshold, the current I_{TB-DIS} (200 µA typ.) is sourced from the pin. If the TB pin voltage is lower than the V_{TB-DIS} threshold (100 mV typ.), the pin is assumed to be connected to GND, the related circuitry is disabled, and the information is latched until the next power-on.

Figure 19. Blanking time variation vs. FB voltage with dynamical blanking time active



5.8 Valley synchronization

The main feature of the QR converters is that the turn-on occurs at the valley of the resonance after the secondary demagnetization, which is a function of primary inductance, L_P and total capacitance of the drain node, C_D. With respect to the transformers' demagnetization instant, the first valley occurs with a delay given by the formula:

Equation 6

(6)

$$T_{VALLEY} = \pi \cdot \sqrt{L_P \cdot C_D}$$

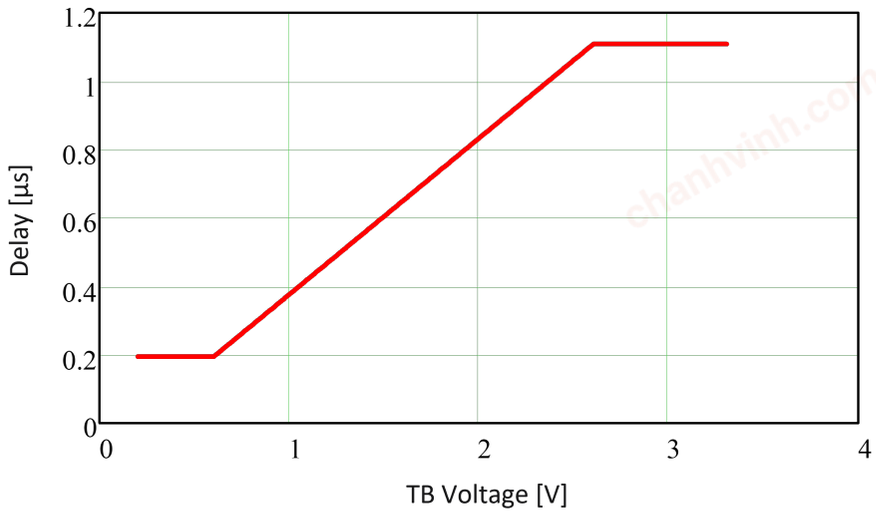
Since T_{VALLEY} can change a lot between one design and another, it is not easy to minimize the turn-on losses using a fixed turn-on delay time after ZCD triggering. For this reason, the VIPERGAN65 integrates a special function that can increase the default turn-on delay time after trigger, $T_{D-ON(MIN)}$ (197 ns typ.) to exactly synchronize the turn-on time at the valley of the resonance, minimizing the turn-on losses.

The pinout configuration is shown in Figure 17: the voltage divider made up by R_{TB} and R_{delay} samples the auxiliary winding voltage, which, during the GaN off-time, is representative of the output voltage.

Since in steady-state the output voltage is constant, and R_{TB} value has already been selected to get the desired dynamic blanking time, R_{delay} can now be chosen to set the TB pin sampled voltage to the value corresponding to the desired turn-on delay, according to Figure 20.

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Figure 20. **Typical Turn-on delay after triggering as a function of the voltage on TB pin.**



The required delay to exactly synchronize the Turn-On at the valley, T_{DELAY}, can be calculated as below:

Equation 7

(7)

$$T_{DELAY} = T_{VALLEY} - T_{ZCD\text{-}DELAY}$$

In the equation $T_{ZCD\text{-}DELAY}$ represents the delay between the demagnetization time and the instant of time in which the ZCD voltage crosses the triggering threshold V_{ZCDT}: this delay is in the range of few tens ns up to hundred ns but can be easily experimentally measured during converter's operation.

The value of V_{TB} can be directly read from the curve also.

Once V_{TB} voltage is known, the value of the resistor can be easily derived:

Equation 8

(8)

$$R_{delay} = \frac{R_{TB}}{\frac{N_{AUX}}{N_{SEC}} \cdot \frac{V_{OUT}}{V_{TB}} - 1}$$

The resistor R_{TB} can be calculated as reported in Section 5.7: Dynamic blanking time.

The T_{DELAY} is set to the default value when R_{delay} is lower than:

Equation 9

(9)

$$R_{delay-default} < \frac{R_{TB}}{\frac{N_{AUX}}{N_{SEC}} \cdot \frac{V_{OUT}}{V_{D-ON(MIN)}} - 1}$$

Dynamic blanking time and valley synchronization functions can be disabled connecting TB to GND.

The decision if the function is used or not is taken at power-up: before the pin V_{DD} reaches the $V_{DD\text{-}ON}$ threshold, the current $I_{TB\text{-}DIS}$ (200 µA typ.) is sourced from the pin. If the TB pin voltage is below the $V_{TB\text{-}DIS}$ threshold (100 mV typ.), the pin is assumed to be connected to GND, the related circuitry is disabled, and the information is latched until the next power-on.

Please note that to ensure a correct check of the disabling function, the resistor R_{delay} cannot be lower than:

Equation 10

(10)

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$$R_{delay_min} < \frac{V_{TB\text{-}DIS(\max)}}{I_{TB\text{-}DIS(\max)}}$$

5.9 TB pin configuration

The pin TB can be easily configured in different combinations, as reported in Table 6 and in Figure 21, Figure 22, Figure 23, Figure 24.

Table 6. TB pin matrix configuration

Dynamic Blanking Time	Valley Synchronization	Schematic Configuration
Yes	Yes	Figure 21
No	Yes	Figure 22
Yes	No	Figure 23
No	No	Figure 24

Figure 21. TB pin: (external configuration: dynamic blanking time and valley synch)

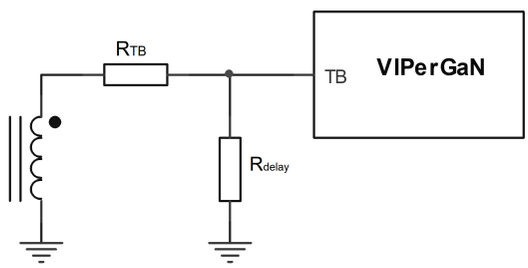


Figure 22. TB pin: external configuration: (only valley synch)

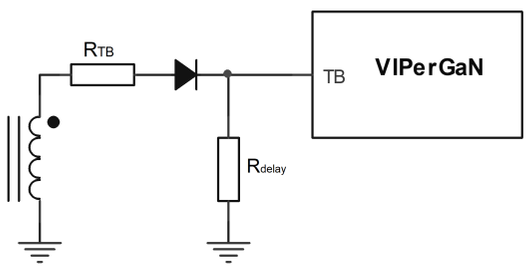


Figure 23. TB pin: external configuration (only dynamic blanking time)

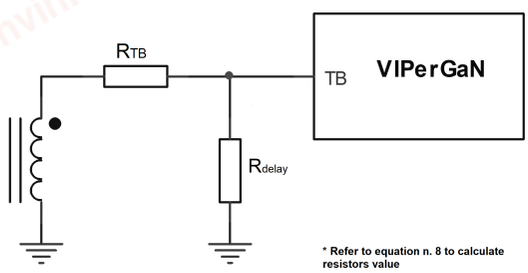
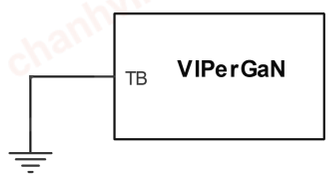


Figure 24. TB pin: external configuration (no dynamic blanking time nor valley synch)



5.10 Overload and short-circuit protection

To manage an overload or a short-circuit condition, an internal up-down counter is incremented or decremented with an internal clock, if the FB pin voltage is, respectively, above or below the upper saturation limit V_{FBH}.

If the overload/short-circuit event persists for a time greater than T_{OVL} (50 ms typical value), the switching is inhibited and V_{DD} is recycled between $V_{DD\text{-}RESTART}$ and $V_{DD\text{-}ON}$ by the periodical activation of the HV current source. After $T_{RESTART}$ from protection tripping, the IC restarts switching with soft-start as soon as V_{DD} is recharged to $V_{DD\text{-}ON}$. After soft-start (during which the overload counter is disabled), if overload is still present, the switching activity is disabled again as previously described, otherwise it resumes normal operation. If the overload/short-circuit event persists for a time smaller than T_{OVL}, the counter is decremented cycle-by-cycle down to zero and the IC is not stopped.

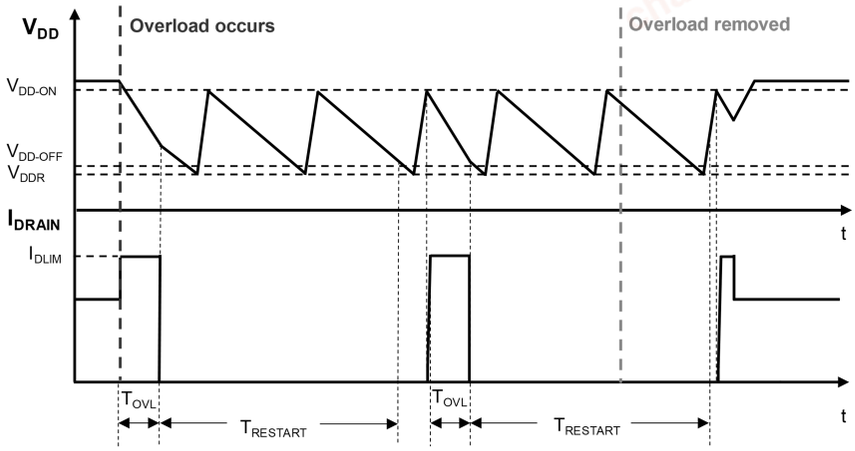
This fault management ensures low repetition rate restart attempts, so that the converter works safely with extremely low power throughput and avoids the IC overheating in case of repeated overload events, and a prompt resumption of normal operation at fault removal.

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In case of transformer saturation, short-circuit of secondary side rectifier or deep CCM, a further protection feature named OCP_LEB is embedded: if, for two consecutive switching cycles, the drain current exceeds I_{OCP_LEB} at the end of LEB time, the VIPERGAN65 is shut down for $T_{SD-REST}$ and performs a new startup as V_{DD} recycles to V_{DD-ON}.

In case of V_{DD} clamp activation with a current sunk from the pin higher than I_{DD-CL} (26 mA typ.) and for a time duration higher than T_{DD-CL} (100 us typ.), the IC is shut down then restart after V_{DD} recycling.

Figure 25. Timing diagram of OLP protection



5.11 Output overvoltage protection

The voltage on the ZCD pin is monitored at the end of the transformer's demagnetization, where the auxiliary winding accurately tracks the converter output voltage and compares with an internal reference.

If the sampled voltage exceeds the OVP threshold V_{OVP} (2.5 V typ.), an overvoltage condition is assumed.

With reference to the external configuration of Figure 1, once R_{OPP} is fixed by feed-forward considerations (see relevant section), it is possible to calculate the value of the R_{OVP} resistor to activate the OVP protection for a certain output voltage level, $V_{OUT-OVP}$.

Equation 11

(11)

$$R_{OVP} = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} \cdot V_{OUT\text{-}OVP} - V_{OVP}} \cdot R_{OPP}$$

To reduce sensitivity to external noise and prevent the protection from being erroneously activated, the OVP comparator must be triggered for four consecutive oscillator cycles before the device is stopped.

A counter, which is reset every time the OVP comparator is not triggered in one oscillator cycle, is provided for this purpose.

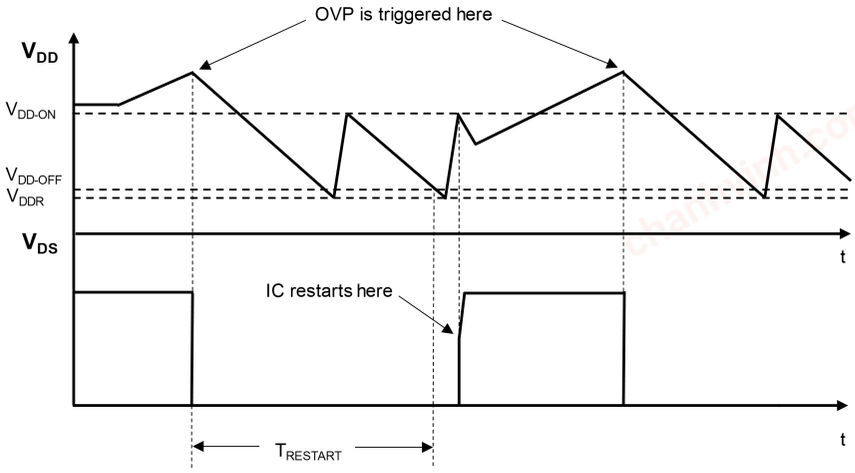
The best accuracy of OVP protection is achieved when demagnetization time is longer than 2 µs.

Once the protection is tripped, the switching is inhibited for $T_{RESTART}$ and V_{DD} is recycled between $V_{DD-RESTART}$ and V_{DD-ON} by the periodical activation of the HV current source. At the end of $T_{RESTART}$, switching is enabled with soft-start at the first V_{DD} recharge to V_{DD-ON}. If overvoltage is still present, the protection is invoked again in the same way, resulting in a low-frequency intermittent operation, which increases the end-product's safety and reliability; otherwise, the IC resumes normal operation.

The OVP protection timing diagrams are shown in Figure 26.

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Figure 26. **OVP timing diagram**



5.12 Input OVP protection

The input overvoltage protection is intended to protect the converter in case of overvoltage on the main line, which can cause exceeding of the GaN's breakdown voltage. It can be easily realized connecting iOVP to the voltage to be monitored (usually the DC rectified input mains) through a voltage divider.

When the iOVP pin voltage exceeds the internal threshold V_{iOVP_th} (5 V typ.), for a time greater than T_{iOVP} (250 µs typ.), the IC is shut down, while V_{DD} is recycled between $V_{DD-RESTART}$ and V_{DD-ON} by the periodical activation of the internal HV current source. Switching is resumed when V_{iOVP} falls below V_{iOVP_th}.

The delay time T_{iOVP} is intended to filter out possible disturbances that may be coupled during operations: it is implemented through an up/down counter which is incremented when V_{iOVP} exceeds V_{iOVP_th} and decremented otherwise, on a cycle-by-cycle base. In this way, temporary disturbances can be distinguished from a real overvoltage, with great advantage to the operative continuity.

Regarding the setting, different configurations are possible, depending on whether brown-in/brown-out protection (described in the following section) is also implemented or not, as shown in Table 1 and Figure 1.

The resistors of the voltage divider are calculated through equations Eq. (12) and Eq. (13). The function can be disabled connecting iOVP to BR.

5.13 Brown-In and Brown-Out protection

The brown-in protection is used to define the minimum input voltage from which the converter starts operating. Similarly, the brown-out protection defines the minimum input voltage below which the converter stops operating.

There are several reasons why it may be desirable to disable the converter below a certain input voltage range. Firstly, a very low input voltage may cause overheating of the primary power section due to an excess of RMS current. Secondly, spurious restarts may occur during converter power-down, which causes the output voltage not to decay to zero monotonically.

At power-up, as $V_{IN} > V_{START}$, the internal HV-current source is activated, and the capacitor connected to V_{DD} is charged to V_{DD-ON}. During this charging phase, the current I_{BR-DIS} = 15 uA is sourced from BR, while V_{BR} is monitored.

If $V_{BR} < V_{BR-DIS}$ (100 mV, typ.), BR is assumed to be connected to GND, the related circuitry is disabled, the information is latched until the next power-on, and the IC is allowed to start up.

If $V_{BR} > V_{BR-DIS}$, the BR block is enabled and the information is latched until the next power-on, but the device is allowed to switch only if V_{BR} exceeds the brown-in internal threshold V_{BR-IN} (0.5 V typ.).

After the IC has entered normal operation: if V_{BR} falls below the brown-out internal threshold, V_{BR-OUT} (0.4 V typ.) for more than the brown-out delay time, T_{BR-OUT} (30 msec, typ.), brown-out protection is triggered, which stops the switching, while V_{DD} is recycled between $V_{DD-RESTART}$ and V_{DD-ON} by the periodical activation of the HV-current source.

After the IC has been stopped by brown-out: if V_{BR} exceeds V_{BR-IN} for more than the brown-in delay time, T_{BR-IN} (250 usec, typ.), brown-in is triggered and the IC resumes switching.

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To reject temporary disturbances across the line, the delay times are implemented through up/down counters. T_{BR-OUT} is also intended to avoid false protection triggerings due to the input capacitor voltage ripple and to guarantee some hold-up in case of a missing cycle of the input line.

Input OVP, brown-in and brown-out conditions can be set connecting a voltage divider across the rectified input mains, iOVP, BR, and GND and selecting the resistor values according to the equations below:

Equation 12

(12)

$$R_{iOVP} = R_{HV} \cdot \left(\frac{V_{iOVP_th}}{V_{IN\text{-}OVP}} - \frac{V_{BR\text{-}IN}}{V_{IN\text{-}ON}} \right)$$

Equation 13

(13)

$$R_{BR} = R_{HV} \cdot \frac{V_{BR-IN}}{V_{IN-ON} - V_{BR-IN}}$$

In the above formulas, V_{IN-ON} and V_{IN-OVP} are the DC input voltages which trigger brown-in and input overvoltage protection respectively.

The resistor R_{HV} is used to start up the converter and also as part of the voltage divider, once HV and iOVP are connected together. Its value is arbitrarily selected, with the recommendation to be few tens MΩ at least to minimize the residual consumptions from the input mains.

It is worth noting that the thresholds $V_{IN\text{-}ON}$ and $V_{IN\text{-}OFF}$ (the input voltage values triggering brown-in and brown-out respectively) cannot be set independently but are linked to each other. The DC bus voltage value that turns off the device is thus calculated with the following equation.

Equation 14

(14)

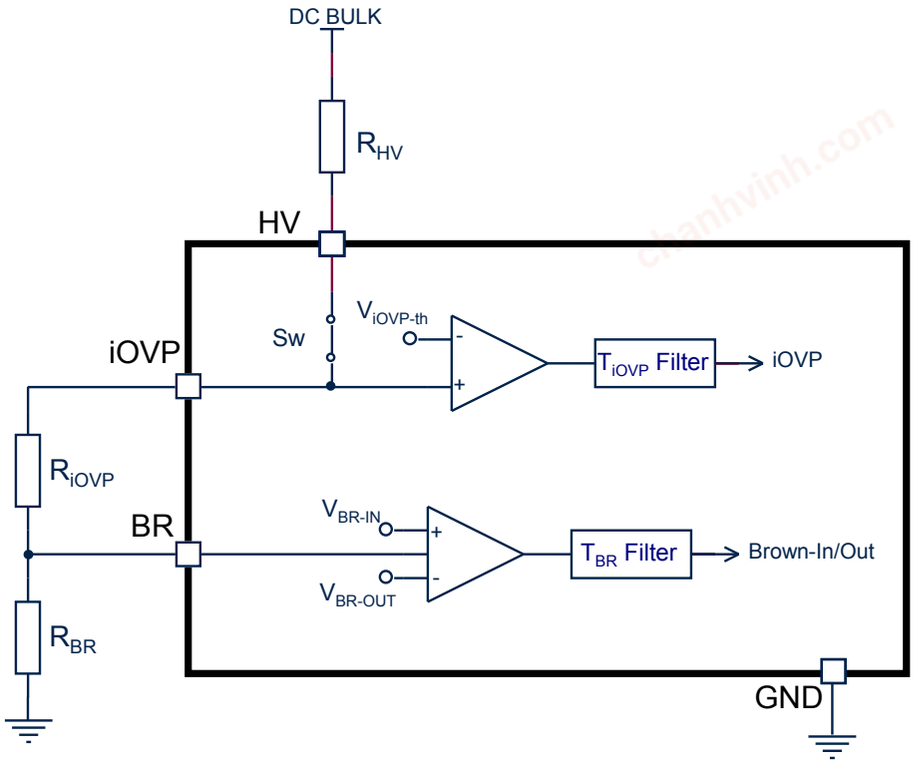
$$V_{IN\text{-}OFF} = V_{IN\text{-}ON} \frac{V_{BR\text{-}OUT}}{V_{BR\text{-}IN}}$$

A 10 nF filter capacitor placed between BR pin and GND is necessary to avoid misbehavior of the brown-out logic when a high voltage start-up unit is activated.

The brown-in/out function can be disabled connecting BR to GND.

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Figure 27. **Brown-in/out and input OVP: internal schematic**



5.14 Configure Brown-In/Out and OVP protection

The pins iOVP and BR can be easily configured in different combinations, as reported in Table 7.

Table 7. **Brown-in/out and OVP matrix configuration**

iOVP Protection	Brown-In/Out	Schematic Configuration
Yes	Yes	Figure 28
Yes	No	Figure 29
No	Yes	Figure 30
No	No	Figure 31

Figure 28. **Brown-In/Out and input OVP: external configuration (Input OVP and BR)**

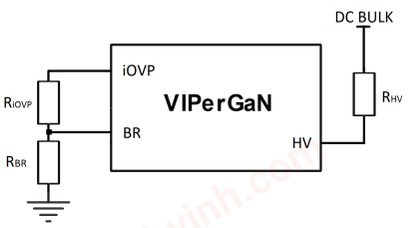
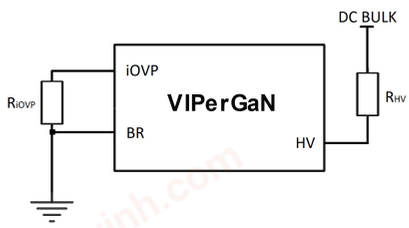


Figure 29. **Brown-In/Out and input OVP: external configuration (Only input OVP)**



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Figure 30. Brown-In/Out and input OVP: external configuration (Only BR)

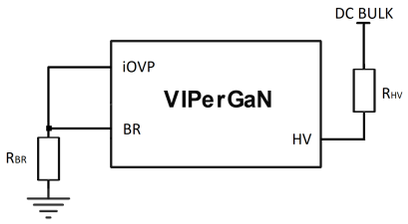
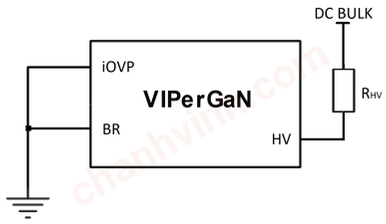


Figure 31. Brown-In/Out and input OVP: external configuration (No input iOVP nor BR)



5.15 Frequency jittering for EMI reduction

Although the VIPERGAN65 works in QR mode and the switching frequency is already modulated at twice the mains frequency, it implements a proprietary frequency jitter technique to further reduce EMI. This technique is based on the injection, on the current sense signal, of a square waveform at 10 kHz (above the feedback loop bandwidth) with 50 % duty cycle which modulates the amplitude of the peak primary current. The percentage of this amplitude modulation is set as a default at 5 %. As the peak current reduces with decreasing load levels, the effect automatically attenuates at lower loads, where the energy of EMI noise is highly reduced.

5.16 Thermal shutdown protection

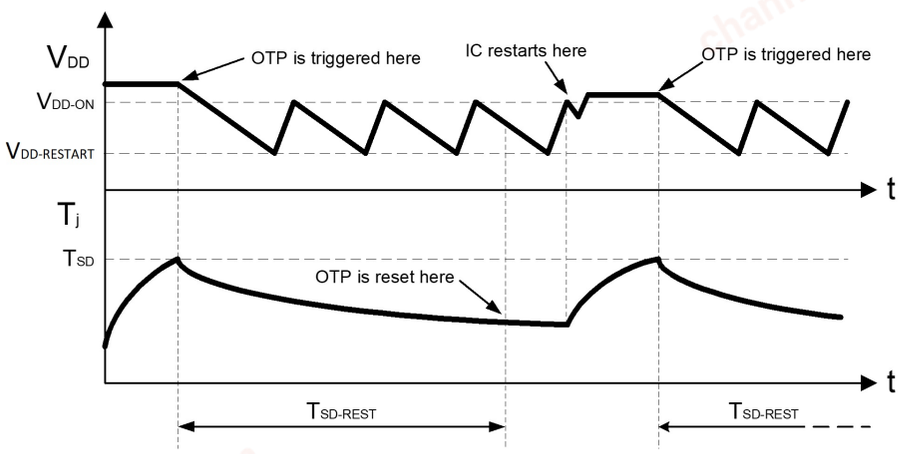
When the controller temperature exceeds the shutdown threshold, T_{SD} (140 °C typ.) the device is shut down and maintained off for the time $T_{SD-REST}$ (2 s typ.) to prevent any dangerous overheating of the system and the V_{DD} pin is continuously recycled between V_{DD-ON} and V_{DD-OFF} to keep the controller alive. During this time, the IC consumption is reduced to $I_{DD-FAULT}$ to further minimize the HV start-up losses.

After $T_{SD-REST}$, the IC restarts as V_{DD} reaches V_{DD-ON}.

Please note that the thermal sensor is embedded into the controller chip and the power GaN chip may have a higher temperature.

The OTP timing diagram is shown in Figure 32.

Figure 32. OTP timing diagram



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6 Typical schematics

Figure 33. **Typical configuration: full features**

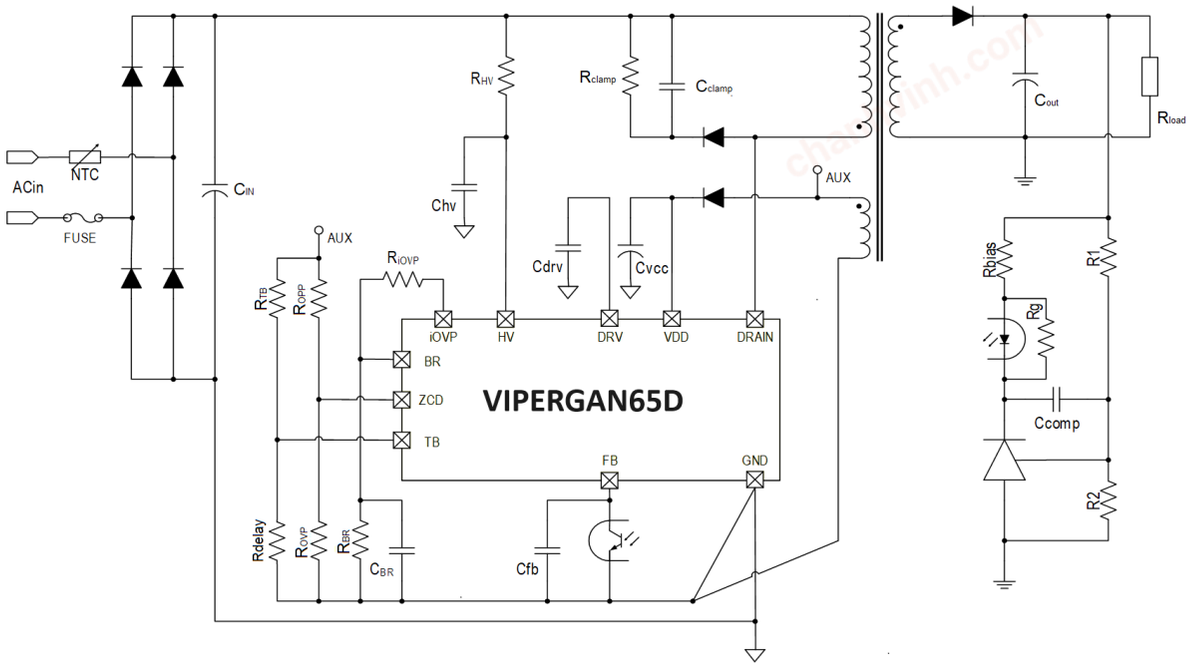
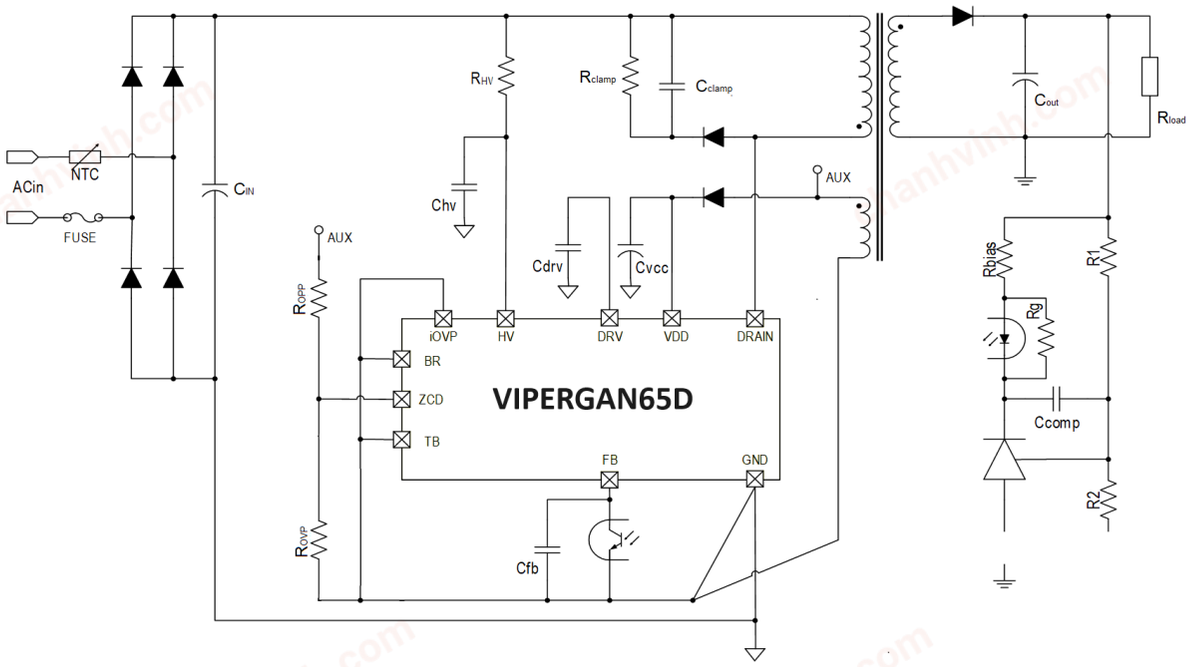


Figure 34. **Typical configuration: basic features**



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7 Layout guidelines and design recommendations

A proper printed circuit board layout is essential for correct operation of any switch-mode converter and this is also true for the VIPERGAN65D. The main reasons for having a proper PCB layout are to:

• Provide clean signals to the IC, ensuring good immunity against external noises and switching noises

• Reduce the electromagnetic interferences, both radiated and conducted, to pass more easily the EMC

When designing an SMPS using VIPerGaN, the following basic rules should be considered:

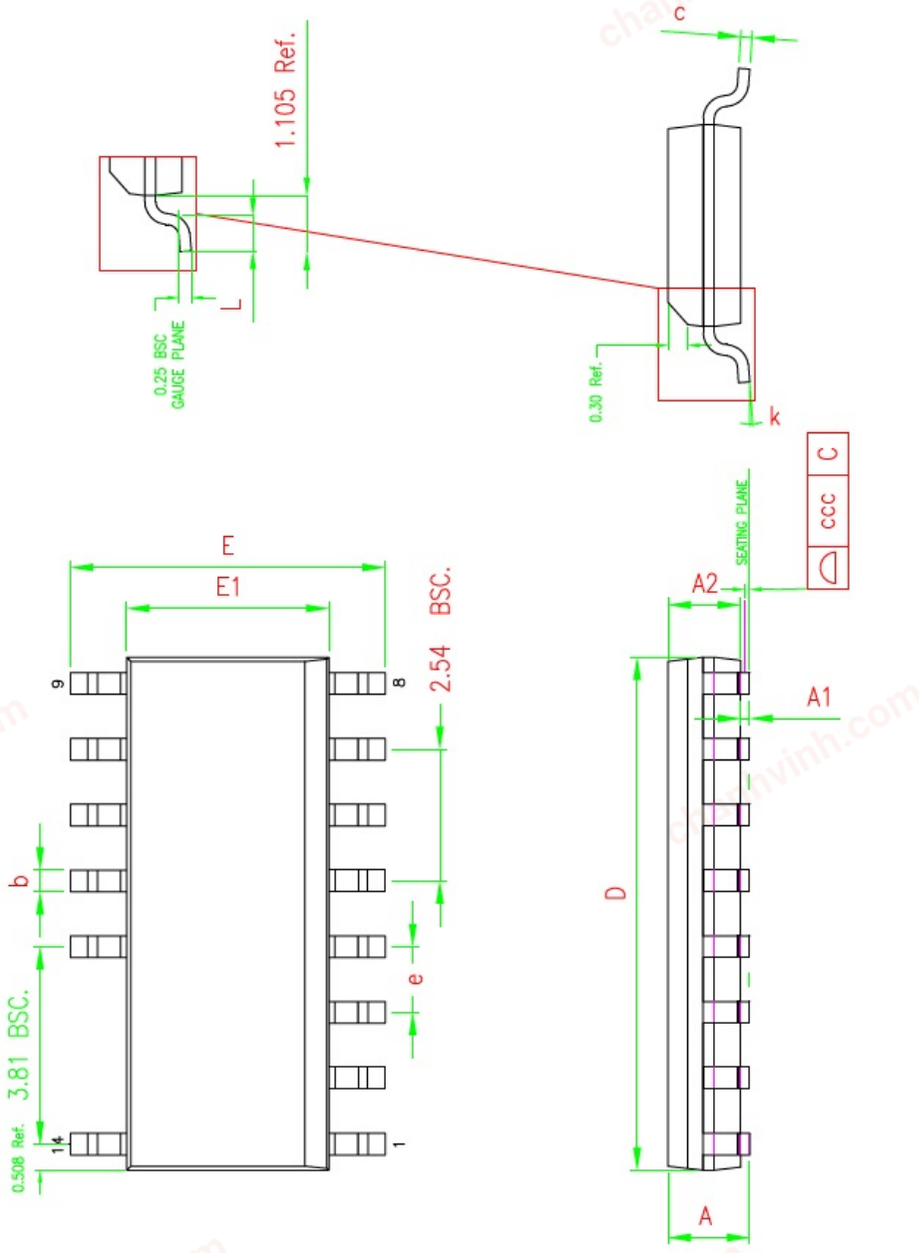
- **Separating signal from power tracks:** generally, traces carrying signal currents should run far from those carrying pulsed currents or with quickly swinging voltages. Signal ground traces should be routed separately from the power ground traces then connected one to the other using a single “star point”, placed close to the IC.
- The compensation network should be connected to the FB pin, maintaining the trace to GND as short as possible. In case of a two-layer PCB, it is a good practice to route signal traces on one PCB side and power traces on the other side.
- **Filtering sensitive pins:** some crucial points of the circuit need or may need filtering. A small high frequency bypass capacitor to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests. A low ESL ceramic capacitor (a few hundreds pF up to 0.1 µF) should be connected across VDD and GND, placed as close as possible to the IC. With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VDD capacitor on the auxiliary return and then to the main GND using a single track. A small 10 nF capacitance is also required between BR and GND to filter the noise in this high impedance path.
- **Keep power loops as confined as possible:** minimize the area circumscribed by current loops where high pulsed currents flow, in order to reduce its parasitic self-inductance and the radiated electromagnetic field: this greatly reduces the electromagnetic interferences produced by the power supply during the switching. In a flyback converter the most critical loops are the ones including the input bulk capacitor, the power switch, the power transformer, the one including the snubber, the one including the secondary winding, the output rectifier, and the output capacitor.
- **Reduce line lengths:** any wire acts as an antenna. With the very short rise times exhibited by EFT pulses, any antenna has the capability of receiving high voltage spikes. By reducing line lengths, the level of radiated energy that is received is reduced, and the resulting spikes from electrostatic discharges are lower. This also keeps both resistive and inductive effects to a minimum. In particular, all of the traces carrying high currents, especially if pulsed (tracks of the power loops) should be as short and fat as possible. It is a good practice to minimize also the areas circumscribed by the paths from TB to GND and from BR to GND, to ensure good immunity against EFT tests.
- **Optimize track routing:** as levels of pickup from static discharges are likely to be greater closer to the extremities of the board, it is wise to keep any sensitive lines away from these areas. Input and output lines often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable. Since vias are to be considered inductive elements, it is recommended to minimize their number in the signal path and avoid them when designing the power path.
- **Improve thermal dissipation:** an adequate copper area has to be provided under the EP pad as heatsink. Since this pad is mechanically connected to the GaN substrate, which is also connected to GND, a large copper area can be used without affecting the EMC performances.

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8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 35. SO16 narrow package information



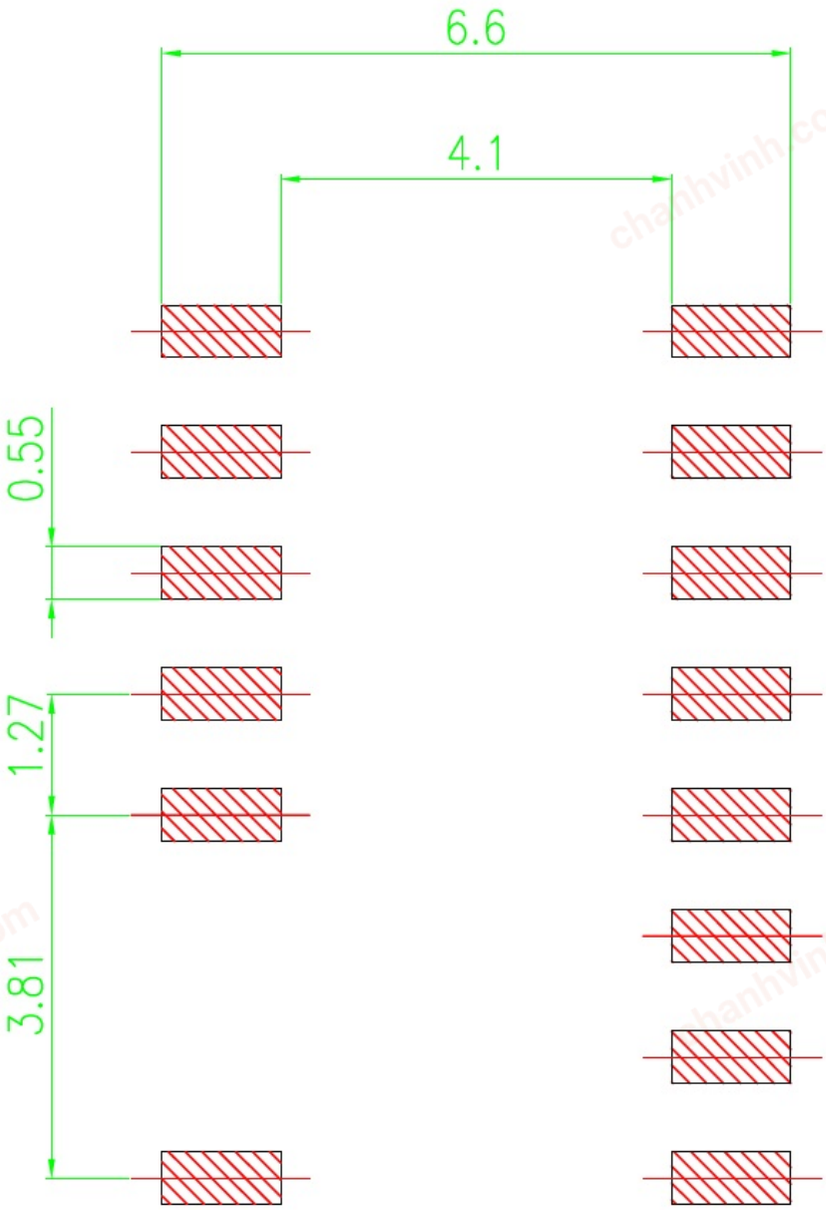
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Table 8. **SO16 narrow mechanical data**

DRAWING (mm)				
Ref.	Min.	Typ.	Max.	Notes
A	--	--	1.68	
A1	0.10	--	0.25	
A2	1.30	1.384	1.50	
b	0.35	0.381	0.49	
c	0.19	0.203	0.25	
D	9.80	9.906	10.00	(1) (3)
E	5.95	6.071	6.20	
E1	3.80	3.861	4.00	(2) (3)
e		1.27 BSC		
L	0.56	0.66	0.82	
k	0	4	8	Degrees
ccc	--	--	0.10	

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Figure 36. **SO16 narrow package information**



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9 Order code

Table 9. **Order code**

Order code	Package	Packing
VIPERGAN65DTR	SO16n	Tape and reel

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Revision history

Table 10. **Document revision history**

Date	Version	Changes
01-Oct-2024	1	Initial release.

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