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TSV782

Datasheet

High bandwidth (30 MHz) low offset (200 µV) rail-to-rail 5 V op amp



TSV782
DFN8
2 mm x 2 mm



TSV782
MiniSO8



TSV782
SO8

Features

- Gain bandwidth product 30 MHz, unity gain stable
- Slew rate 20 V/µs
- Low input offset voltage 50 µV typ., 200 µV max.
- Low input bias current: 2 pA typ.
- Low input voltage noise density 7 nV/√Hz @ 10 kHz
- Wide supply voltage range: 2.0 V to 5.5 V
- Rail-to-rail input and output
- Extended temperature range: -40 °C to +125 °C
- Automotive grade version available
- Benefits:
  - Accuracy of measurement virtually unaffected by noise or input bias current
  - Signal conditioning for high frequencies

Applications

- High bandwidth low-side and high-side current sensing
- Photodiode transimpedance amplification
- A/D converters input buffers
- Power management in solar-powered systems
- Power management in HEV and EV

Product status link	Channel	Automotive	Package
TSV782IQ2T	2		DFN8
TSV782IST	2		MiniSO8
TSV782IDT	2		SO8
TSV782IYST	2	•	MiniSO8
TSV782IYDT	2	•	SO8

Related products	
TSV7722	22 MHz low-rail input op amp for more power savings
TSV772	20 MHz rail-to-rail op amp for more power savings
TSV792	50 MHz rail-to-rail op amp for higher gain bandwidth

Description

The TSV782 is a 30 MHz-bandwidth unity-gain-stable amplifier. The rail-to-rail input stage and the slew rate of 20 V/µs make the TSV782 ideal for low-side current measurement.

The TSV78x can operate from 2.0 V to 5.5 V single supply and it is fully specified on a load of 47 pF, therefore allowing easy usage as A/D converters input buffer. The TSV78x series offers rail-to-rail input and output, excellent speed/power consumption ratio, and 30 MHz gain bandwidth product, while consuming just 3.3 mA at 5 V.

The devices also feature an ultra-low input bias current that enables connection to photodiodes and other sensors where current is the key value to be measured.

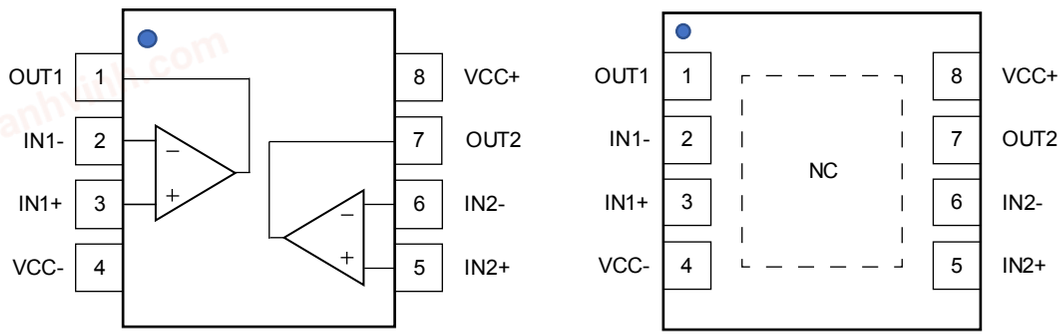
These features make the TSV78x series ideal for high-accuracy, high-bandwidth sensor interfaces.

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1 Pin description

1.1 TSV782 dual operational amplifier

Figure 1. Pin connections (top view)



MiniSO8 and SO8

DFN8 2 x 2 mm(1)

1. The exposed pad of the DFN8 2x2 can be connected to VCC- or left floating.

Table 1. Pin description

Pin n°	Pin name	Description
1	OUT1	Output channel 1
2	IN1-	Inverting input channel 1
3	IN1+	Non-inverting input channel 1
4	VCC-	Negative supply voltage
5	IN2+	Non-inverting input channel 2
6	IN2-	Inverting input channel 2
7	OUT2	Output channel 2
8	VCC+	Positive supply voltage

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2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter (1)	Value	Unit
V_{CC}	Supply voltage	6	V
V_{id}	Input voltage differential (V_{IN+} - V_{IN-}) (2)	$\pm V_{CC}$	V
V_{in}	Input voltage	(V_{CC-}) -0.2 to (V_{CC+}) +0.2	V
I_{in}	Input current	±10	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{th-ja} (3)	Thermal resistance junction-to-ambient		°C / W
	SOT23-5	250	
	DFN8 2x2	76	
	MiniSO8	127	
	SO8	113	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model (industrial grade) (4)	4	kV
	HBM: human body model (automotive grade) (5)	4	kV
	CDM: charged device model for DFN8 and SO8 (6)	1.5	kV
	CDM: charged device model for MiniSO8 (6)	1	kV

1. *All voltage values are with respect to the VCC- pin, unless otherwise specified.*
2. *The maximum input voltage differential value may be extended to the condition that the input current is limited to ±10 mA.*
3. *R_{th-ja} is a typical value, obtained with PCB according to JEDEC 2s2p without vias.*
4. *Human body model: HBM test according to the standard ESDA-JS-001-2017.*
5. *Human body model: HBM test according to the standard AEC-Q100-002.*
6. *Charged device model: the test CDM is done according to the standard AEC-Q100-011.*

Table 3. Operating conditions

Symbol	Parameter	Value
V_{CC}	Supply voltage	2.0 V to 5.5 V
V_{icm}	Common mode input voltage range	V_{CC-} – 0.1 V to V_{CC+} + 0.1 V
T_{oper}	Operating free air temperature range	-40 °C to +125 °C

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3 Electrical characteristics

Table 4. Electrical characteristics at V_{CC} = 5 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C, C_L = 47 pF and R_L = 10 kΩ connected to V_{CC} / 2 (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		± 50	± 200	µV
		-40 °C ≤ T ≤ 125 °C			± 700	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
I_{ib} (1)	Input bias current	T = 25 °C		1	2	pA
		-40 °C ≤ T ≤ 85 °C		10	30	
		-40 °C ≤ T ≤ 125 °C		75	200	
I_{io} (1)	Input offset current	T = 25 °C		1	2	pA
		-40 °C ≤ T ≤ 85 °C		5	20	
		-40 °C ≤ T ≤ 125 °C		20	100	
A_{VD}	Open loop gain	V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, T = 25 °C	110	133		dB
		V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, -40 °C ≤ T ≤ 125 °C	95	113		
		V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV, R_L = 600 Ω, T = 25 °C	105	130		
		V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV, R_L = 600 Ω, -40 °C ≤ T ≤ 125 °C	85			
CMR1	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} - 100 mV ≤ V_{icm} ≤ V_{CC+} - 1.8 V, T = 25 °C	98	120		dB
		V_{CC-} - 100 mV ≤ V_{icm} ≤ V_{CC+} - 1.8 V, -40 °C ≤ T ≤ 125 °C	90	120		
CMR2		V_{CC-} -100 mV ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	80	100		dB
		V_{CC-} -100 mV ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	76	92		
SVR	Supply-voltage rejection ratio 20.log ($\Delta V_{io}/\Delta V_{CC}$)	2.0 V ≤ V_{CC} ≤ 5.5 V, T = 25 °C, V_{icm} = 0 V	90	110		dB
		2.0 V ≤ V_{CC} ≤ 5.5 V, -40 °C ≤ T ≤ 125 °C, V_{icm} = 0 V	90	110		
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{SINK}	R_L connected to V_{CC+}, T = 25 °C	55	70		mA
		R_L connected to V_{CC+}, -40 °C ≤ T ≤ 125 °C	37			
	I_{SOURCE}	R_L connected to V_{CC-}, T = 25 °C	55	60		
		R_L connected to V_{CC-}, -40 °C ≤ T ≤ 125 °C	45			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		3.3	3.7	mA
		-40 °C ≤ T ≤ 125 °C			3.7	

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ	23	30		MHz
SR	Slew rate	R_L = 10 kΩ, A_V = 1 V/V, 10% to 90%	17	20		V/µs
t_{rec}	Overload recovery time	V_{OUT} = 100 mV from rail, A_V = +1 V/V		170		ns
CR	Cross talk	V_{OUT} = 4 V_{pp}, R_L = 10 kΩ, A_V = +101 V/V, f = 1 kHz		120		dB
Φm	Phase margin			47		degrees
GM	Gain margin			9		dB
en	Input voltage noise density	f = 10 kHz		7		nV/√Hz
		f = 1 kHz		14		
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		9		$µV_{pp}$
C_{in}	Input capacitance	Differential		6.3		pF
		Common mode		1.6		

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Table 5. Electrical characteristics at V_{CC} = 3.3 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C, C_L = 47 pF and R_L = 10 kΩ connected to V_{CC} / 2 (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		± 50	± 200	µV
		-40 °C ≤ T ≤ 125 °C			± 700	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
I_{ib} (1)	Input bias current	T = 25 °C		1	2	pA
		-40 °C ≤ T ≤ 85 °C		10	30	
		-40 °C ≤ T ≤ 125 °C		75	200	
I_{io} (1)	Input offset current	T = 25 °C		1	2	pA
		-40 °C ≤ T ≤ 85 °C		5	20	
		-40 °C ≤ T ≤ 125 °C		20	100	
A_{VD}	Open loop gain	V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, T = 25 °C	105	130		dB
		V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, -40 °C ≤ T ≤ 125 °C	90	113		
		V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV, R_L = 600 Ω, T = 25 °C	100	129		
		V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV, R_L = 600 Ω, -40 °C ≤ T ≤ 125 °C	85	99		
CMR1	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} - 100 mV ≤ V_{icm} ≤ V_{CC+} - 1.8 V, T = 25 °C	93	116		dB
		V_{CC-} - 100 mV ≤ V_{icm} ≤ V_{CC+} - 1.8 V, -40 °C ≤ T ≤ 125 °C	85	111		
CMR2		V_{CC-} - 100 mV ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	77	97		dB
		V_{CC-} - 100 mV ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	70	90		
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{SINK}	R_L connected to V_{CC+}, T = 25 °C	55	63		mA
		R_L connected to V_{CC+}, -40 °C ≤ T ≤ 125 °C	36			
	I_{SOURCE}	R_L connected to V_{CC-}, T = 25 °C	55	63		
		R_L connected to V_{CC-}, -40 °C ≤ T ≤ 125 °C	43			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		3.2	3.6	mA
		-40 °C ≤ T ≤ 125 °C			3.6	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ	23	30		MHz
SR	Slew rate	R_L = 10 kΩ, A_V = 1 V/V, 10% to 90%	17	20		V/µs

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time	V_{OUT} 100 mV from rail, A_V = +1 V/V		180		ns
Φm	Phase margin			45		degrees
GM	Gain margin			9		dB
en	Input voltage noise density	f = 10 kHz		7		nV/√Hz
		f = 1 kHz		14		
C_{in}	Input capacitance	Differential		6.3		pF
		Common mode		1.6		

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Table 6. Electrical characteristics at V_{CC} = 2.0 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C, C_L = 47 pF and R_L = 10 kΩ connected to V_{CC} / 2 (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage (V_{icm} = 0 V)	T = 25 °C		± 50	± 200	µV
		-40 °C ≤ T ≤ 125 °C			± 700	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
I_{ib}	Input bias current (1)	T = 25 °C		1	2	pA
		-40 °C ≤ T ≤ 85 °C		10	30	
		-40 °C ≤ T ≤ 125 °C		75	200	
I_{io}	Input offset current (1)	T = 25 °C		1	2	pA
		-40 °C ≤ T ≤ 85 °C		5	20	
		-40 °C ≤ T ≤ 125 °C		20	100	
A_{VD}	Open loop gain	V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, T = 25 °C	95	120		dB
		V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, -40 °C ≤ T ≤ 125 °C	85	107		
		V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV, R_L = 600 Ω, T = 25 °C	90	119		
		V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV, R_L = 600 Ω, -40 °C ≤ T ≤ 125 °C	80	99		
CMR	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} - 100 mV ≤ V_{icm} ≤ V_{CC+}, T = 25°C	73			dB
		V_{CC-} - 100 mV ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	67			
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{SINK}	R_L connected to V_{CC+}, T = 25 °C	45	51		mA
		R_L connected to V_{CC+}, -40 °C ≤ T ≤ 125 °C	32			
	I_{SOURCE}	R_L connected to V_{CC-}, T = 25 °C	45	56		
		R_L connected to V_{CC-}, -40 °C ≤ T ≤ 125 °C	38			
I_{CC}	Supply current (by operational amplifier, V_{icm} = 0 V)	T = 25 °C		3	3.4	mA
		-40 °C ≤ T ≤ 125 °C			3.4	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ	23	30		MHz
SR	Slew rate	R_L = 10 kΩ, A_V = 1 V/V, 10% to 90%	13	17		V/µs
t_{rec}	Overload recovery time	V_{OUT} 100 mV from rail, A_V = +1 V/V		200		ns
THD+N	Total harmonic distortion + noise	V_{IN} = 1 V_{pp}, R_L = 10 kΩ, A_V = +1, f = 1 kHz, BW = 22 kHz		0.004		%
Φm	Phase margin			50		degrees
GM	Gain margin			9		dB

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
en	Input voltage noise density	f = 10 kHz		13		nV/√Hz
		f = 1 kHz		35		
C_{in}	Input capacitance	Differential		6.3		pF
		Common mode		1.6		

1. *Guaranteed by design and characterization on a sample of parts, not tested in production*

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4 Typical performance characteristics

R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 47 pF, unless otherwise specified.

Figure 2. Supply current vs. supply voltage

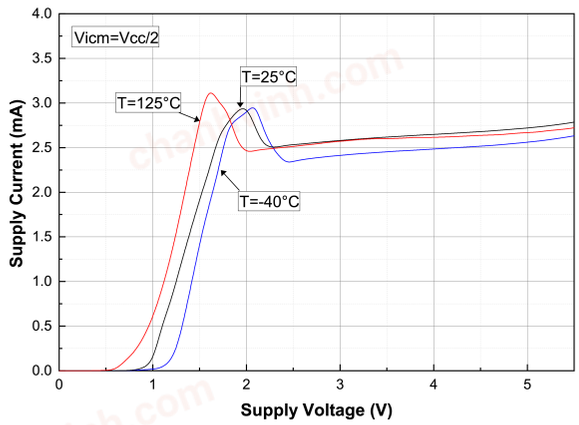


Figure 3. Input offset voltage distribution at V_{CC} = 5 V

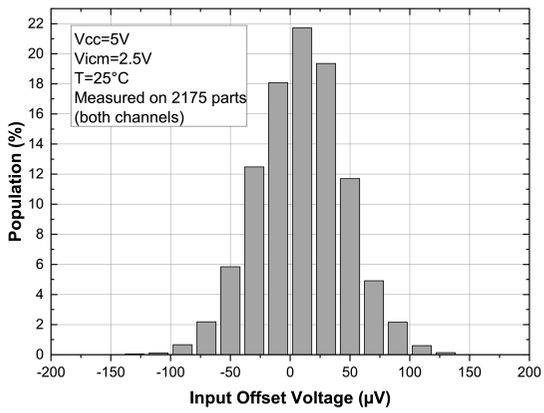


Figure 4. Input offset voltage distribution at V_{CC} = 2 V

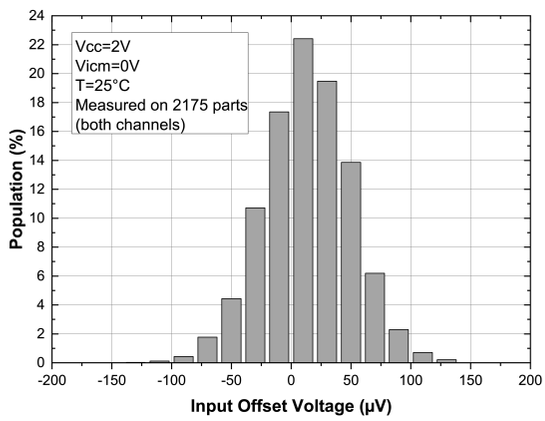
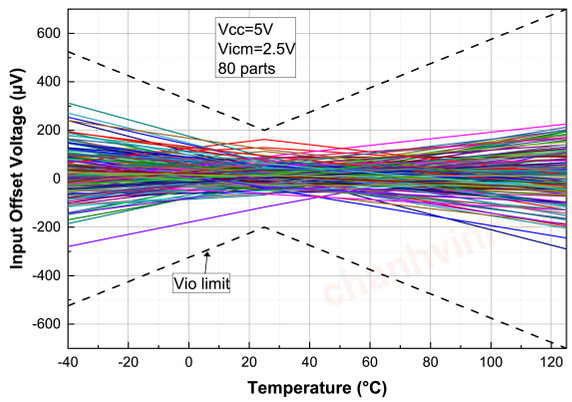


Figure 5. Input offset voltage vs. temperature at V_{CC} = 5 V



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Figure 6. Input offset voltage vs. temperature at V_{CC} = 2 V

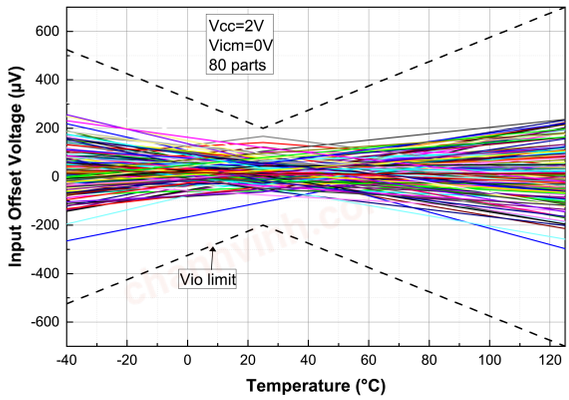


Figure 7. Input offset voltage thermal drift distribution at V_{CC} = 5 V

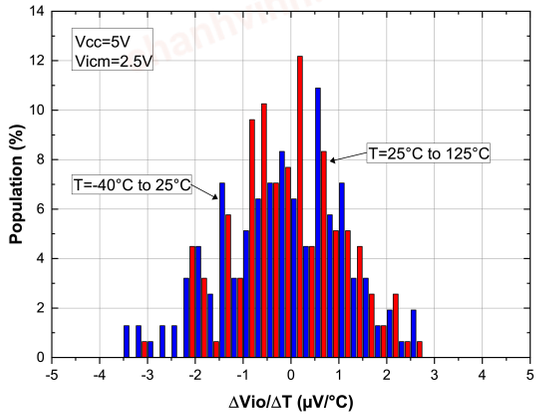


Figure 8. Input offset voltage thermal drift distribution at V_{CC} = 2 V

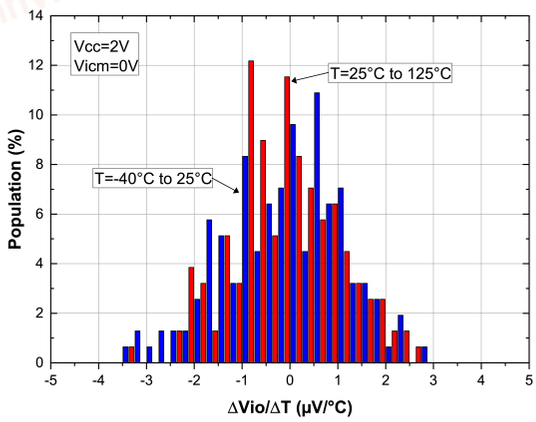


Figure 9. Input offset voltage vs. supply voltage

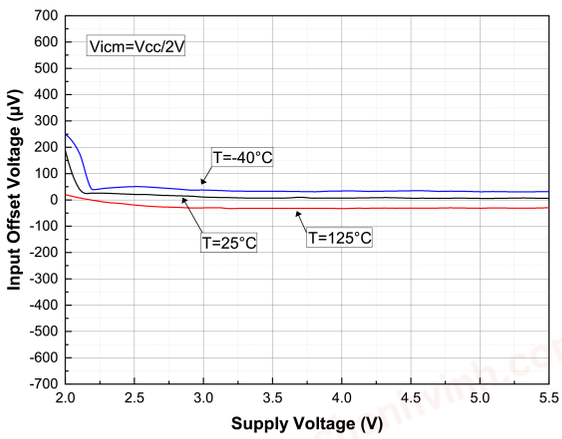


Figure 10. Input offset voltage vs. common-mode voltage at V_{CC} = 5 V

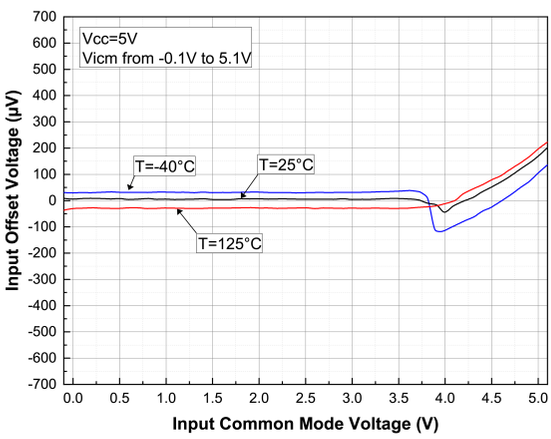
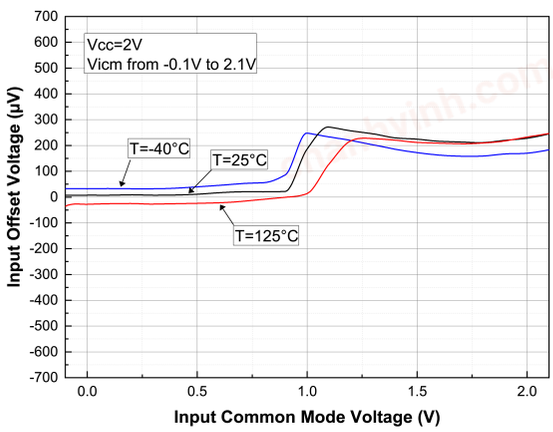


Figure 11. Input offset voltage vs. common-mode voltage at V_{CC} = 2 V



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Figure 12. Input offset voltage vs. supply voltage

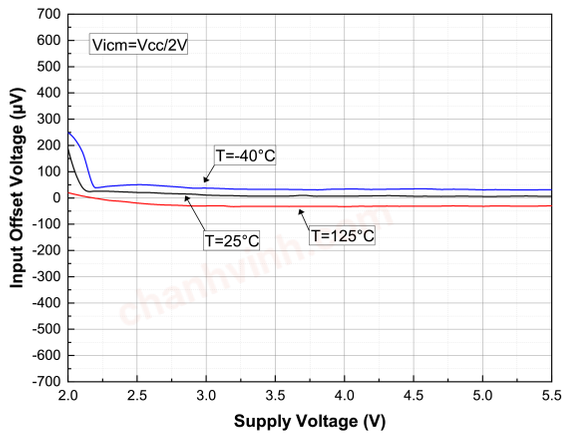


Figure 13. Input bias current vs. common-mode voltage at V_{CC} = 5 V

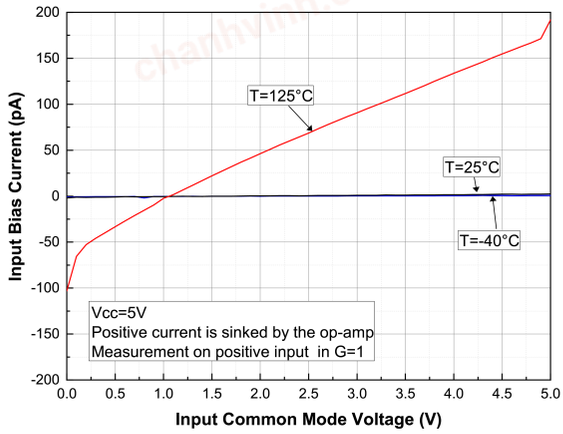


Figure 14. Output current vs. output voltage at V_{CC} = 5 V

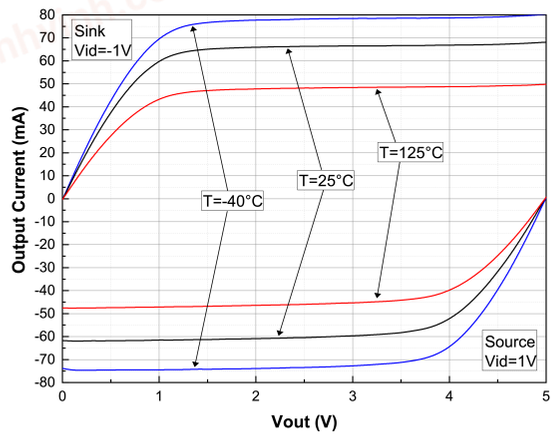


Figure 15. Output current vs. output voltage at V_{CC} = 2 V

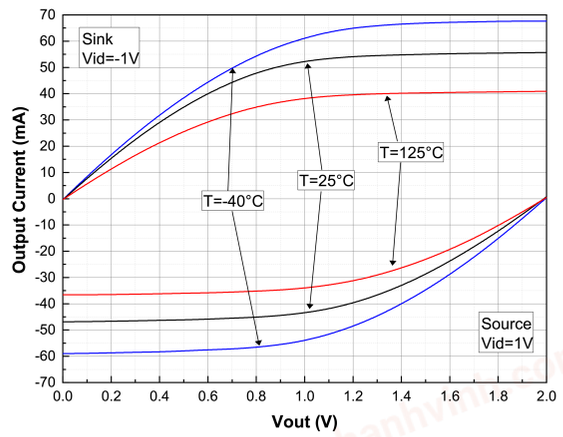


Figure 16. Output saturation voltage (V_{OL}) vs. supply voltage

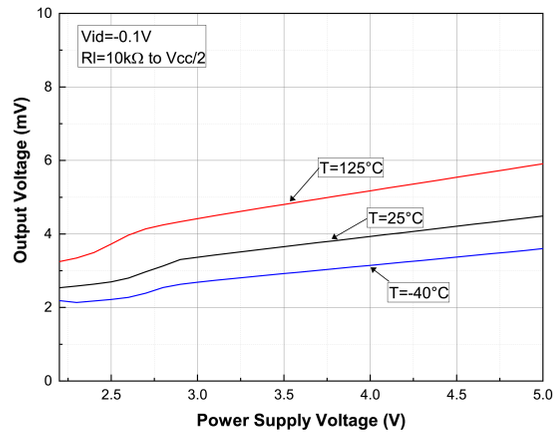
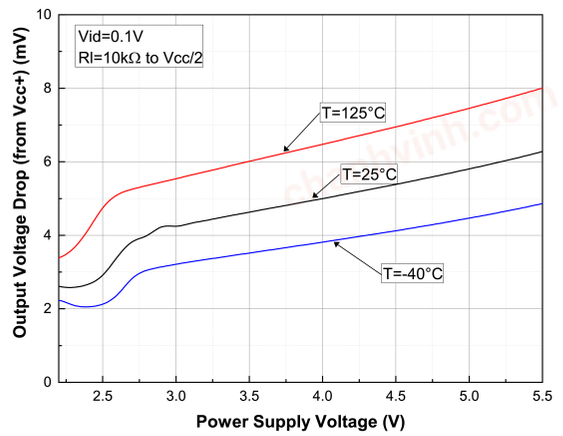


Figure 17. Output saturation voltage (V_{OH}) vs. supply voltage



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Figure 18. Positive slew rate at V_{CC} = 5 V

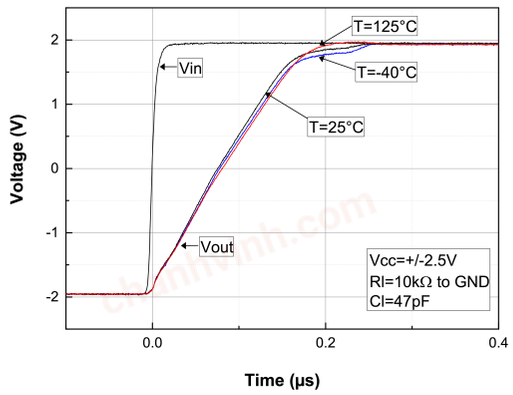


Figure 19. Negative slew rate at V_{CC} = 5 V

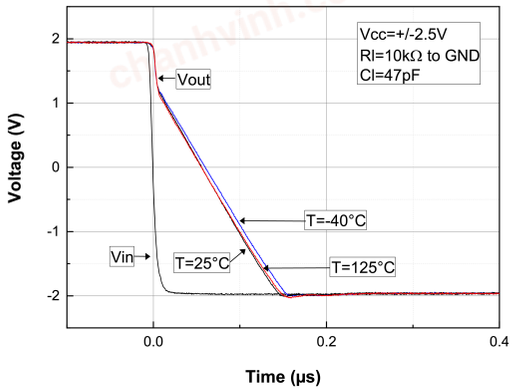


Figure 20. Slew rate vs. V_{CC}

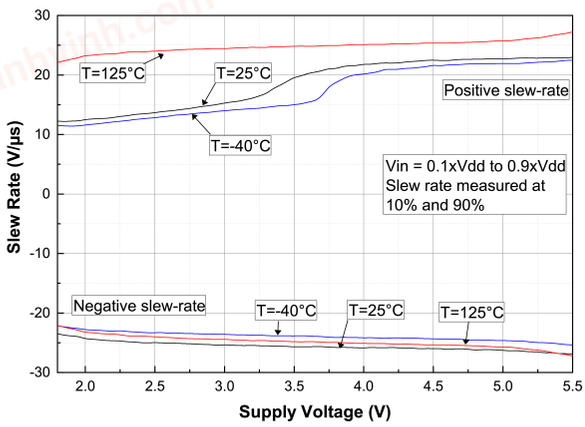


Figure 21. Open loop bode diagram at V_{CC} = 5 V

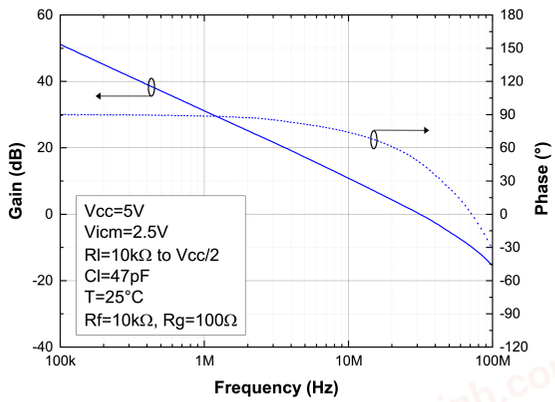


Figure 22. Open loop bode diagram at V_{CC} = 2 V

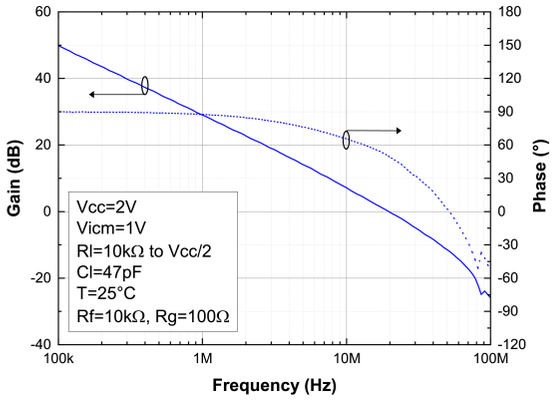
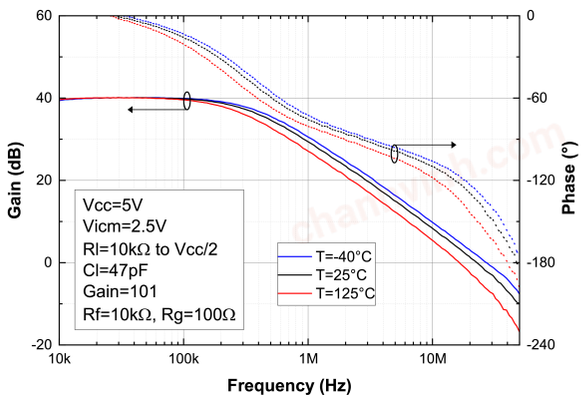


Figure 23. Closed loop bode diagram at V_{CC} = 5 V



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Figure 24. Closed loop bode diagram at V_{CC} = 2 V

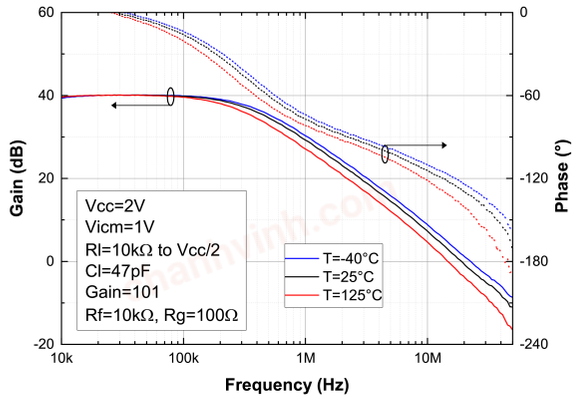


Figure 25. Phase margin vs. common mode-voltage and load current at V_{CC} = 5 V

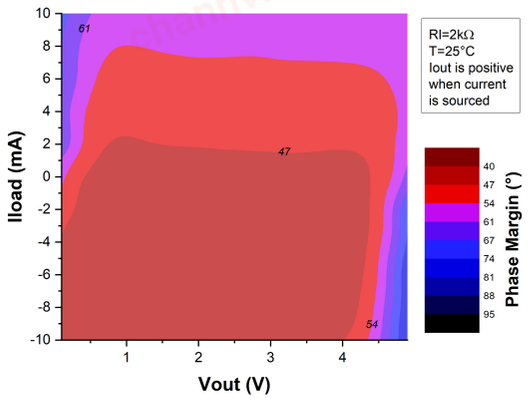


Figure 26. Phase margin vs. capacitive load

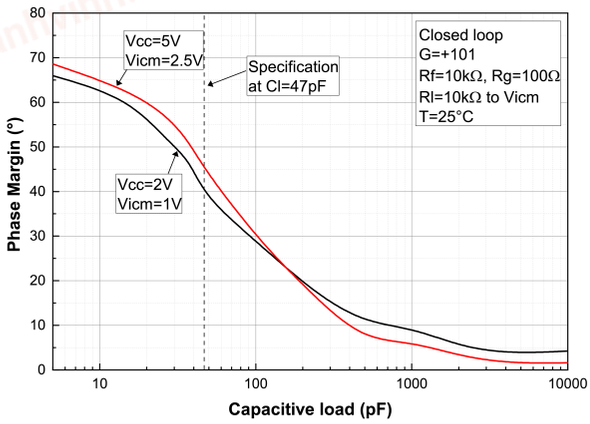


Figure 27. Small step response at V_{CC} = 5 V

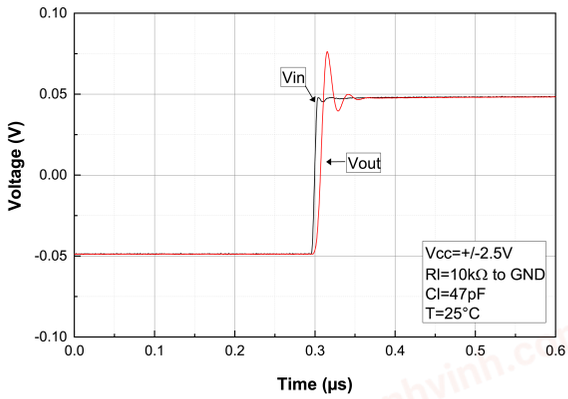


Figure 28. Small step response at V_{CC} = 2 V

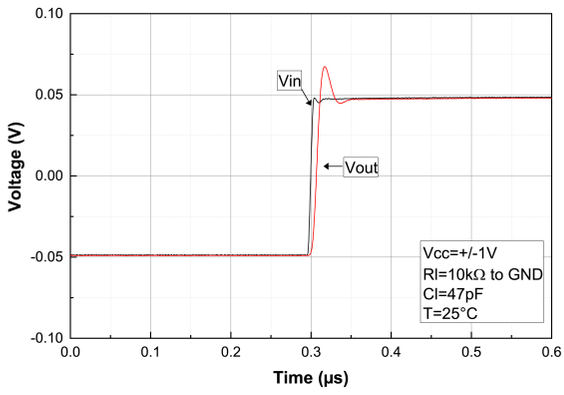
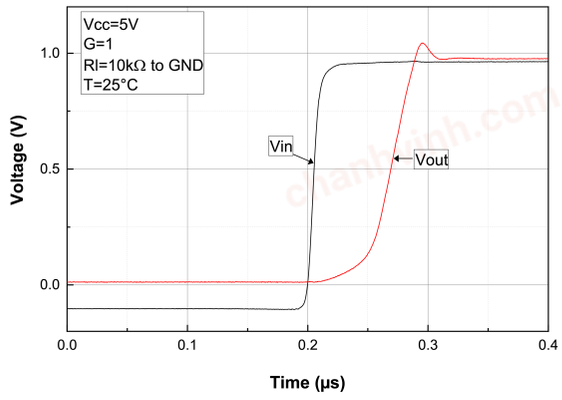


Figure 29. Desaturation from low rail at V_{CC} = 5 V



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Figure 30. Desaturation from high rail at V_{CC} = 5 V

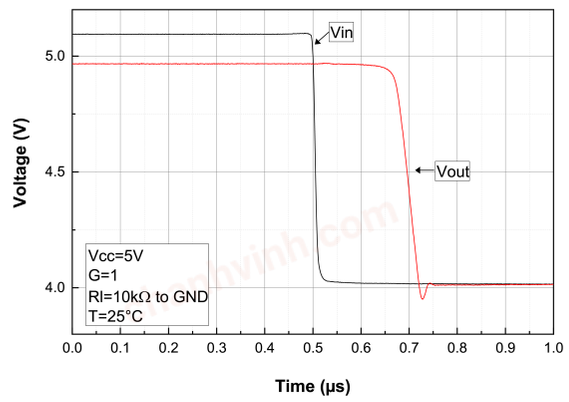


Figure 31. Small step overshoot vs. load capacitance

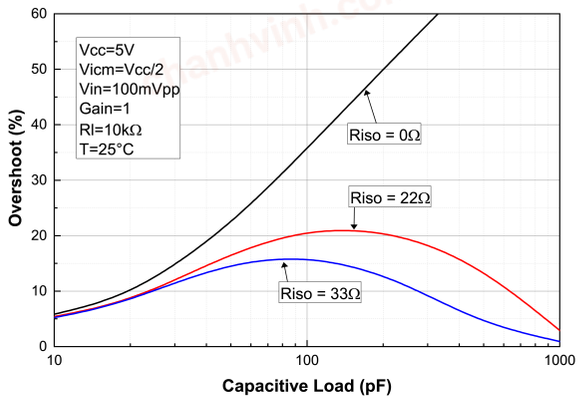


Figure 32. Linearity vs. load resistance at V_{CC} = 5 V

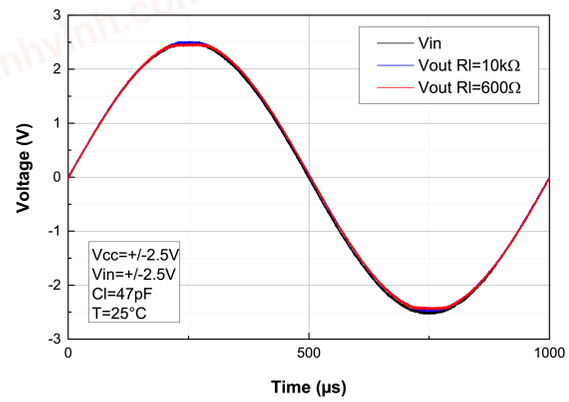


Figure 33. Noise vs. frequency

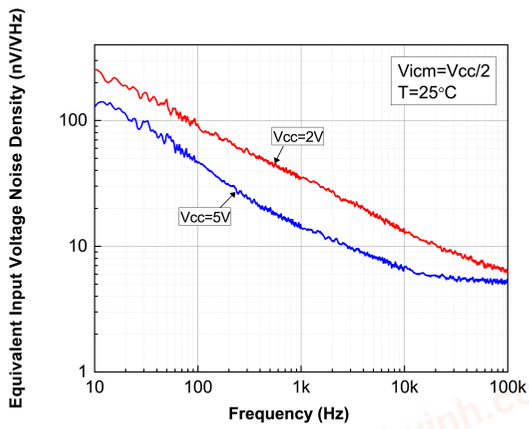


Figure 34. Noise vs. time at V_{CC} = 5 V

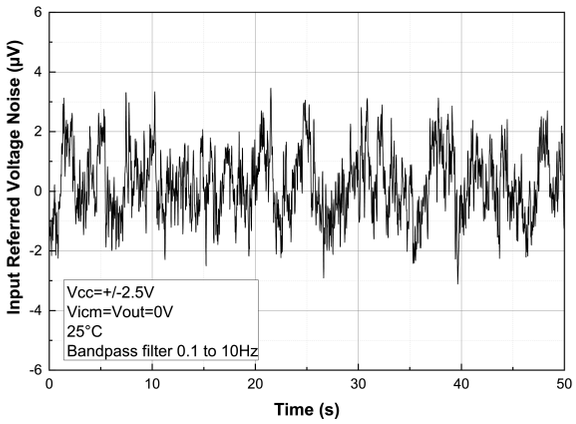
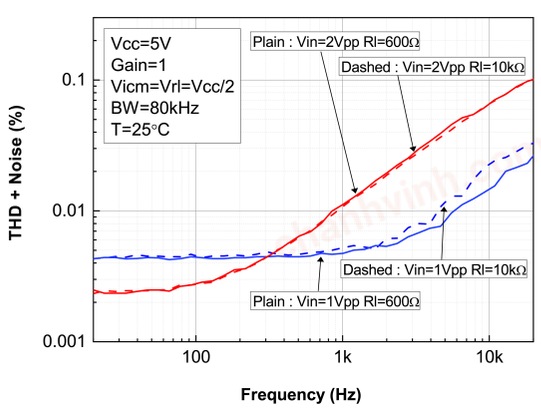


Figure 35. THD+N vs. frequency



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Figure 36. THD+N vs. output voltage

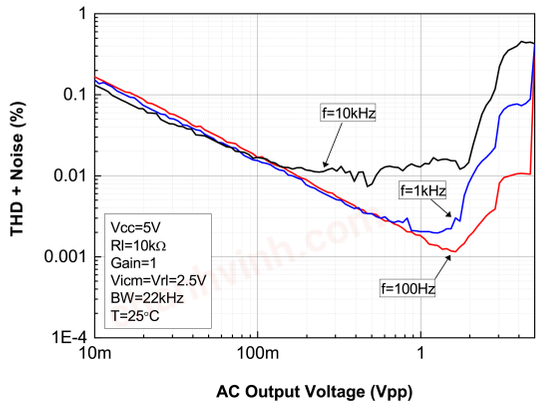


Figure 37. CMRR vs. frequency at V_{CC} = 5 V

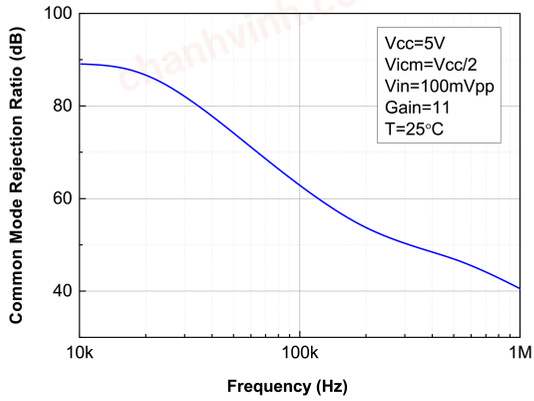


Figure 38. PSRR vs. frequency at V_{CC} = 5 V

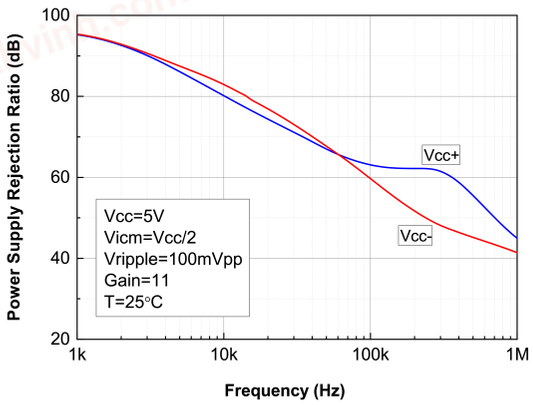


Figure 39. Turn-on time at V_{CC} = 5 V

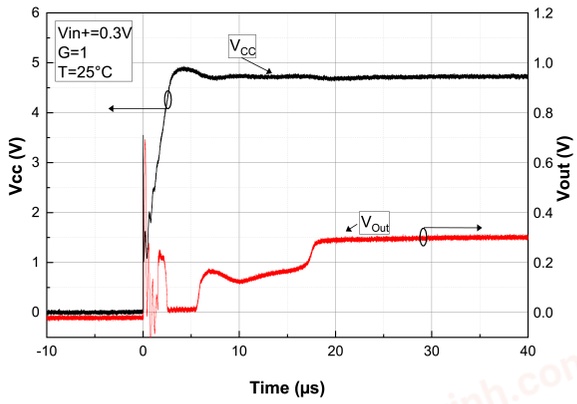
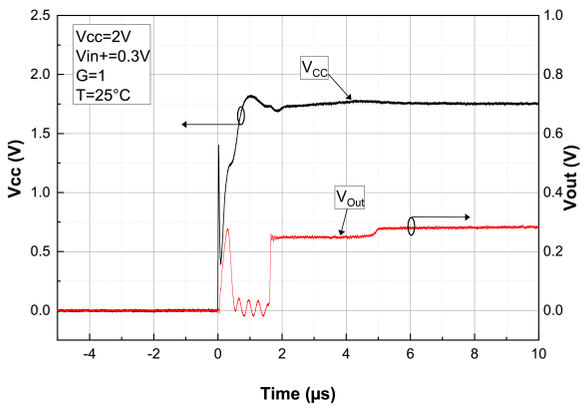


Figure 40. Turn-on time at V_{CC} = 2 V



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5 Application information

5.1 Operating voltages

The TSV782 device can operate from 2.0 to 5.5 V. The parameters are fully specified at 2.0 V, 3.3 V and 5 V power supplies. However, the parameters are very stable over the full V_{CC} range and several characterization curves show the TSV782 device characteristics over the full operating range. Additionally, the main specifications are guaranteed in extended temperature range from -40 to 125 °C.

5.2 Input offset voltage drift over the temperature

The maximum input voltage drift variation overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset (V_{io}) is a major contributor to the chain accuracy.

The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations. The maximum input voltage drift overtemperature is computed using Eq. (1).

$$\frac{\Delta V_{io}}{\Delta T} = max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|_{T = -40°C \; and \; T = 125°C} \quad (1)$$

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.3 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using Eq. (2).

$$A_{FV} = e^{\beta \cdot (V_S - V_U)} \quad (2)$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in Eq. (3).

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)} \quad (3)$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173×10^{-5} eV . K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die undertemperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (Eq. (4)).

$$A_F = A_{FT} \cdot A_{FV} \quad (4)$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in Eq. (5) to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

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$$Months = A_F \times 1000\,h \times 12\,months/(24\,h \times 365.25\ days) \quad (5)$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules). The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see Eq. (6)).

$$V_{CC} = max(V_{op})\ with\ V_{icm} = \frac{V_{cc}}{2} \quad (6)$$

The long term drift parameter ΔV_{io} (in µV.month$^{-1/2}$), estimating the reliability performance of the product, is obtained using the ratio of the Vio (input offset voltage value) drift over the square root of the calculated number of months (Eq. (7)).

$$\Delta V_{io} = \frac{V_{io}drift}{\sqrt{months}} \quad (7)$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

The V_{io} final drift, in µV, to be measured on the device in real operation conditions can be computed from Eq. (8).

$$V_{io\ final\ drift}(t_{op}, T_{op}, V_{CC}) = \Delta V_{io} \cdot \sqrt{t_{op} \cdot e^{\beta \cdot (V_{CC} - V_{CC\ nom})} \cdot e^{\frac{E_a}{k} \cdot \left(\frac{1}{297} - \frac{1}{T_{op}}\right)}} \quad (8)$$

Where:

ΔV_{io} is the long term drift parameter in µV.√month

t_{op} is the operating time seen by the device, in months

T_{op} is the operating temperature

V_{CC} is the power supply during operating time

V_{CC} nom is the nominal V_{CC} at which the ΔV_{io} is computed (5 V for TSV782)

E_a is the activation energy of the technology (here 0.7 eV).

5.4 Unused channel

When one of the two channels of the TSV782 is not used, it must be properly connected in order to avoid internal oscillations that can negatively impact the signal integrity on the other channel, as well as the current consumption. Two different configurations can be used:

Gain configuration: the channel can be set in gain, the input can be set to any voltage within the V_{icm} operating range.

Comparator configuration: the channel can be set to a comparator configuration (without negative feedback). In this case, positive and negative inputs can be set to any value provided these values are significantly different (100 mV or more, to avoid oscillation between positive and negative state) and the differential input is lower than the maximum specified in the operating range (maximum 2 V), or the input current is limited to less than 10 mA to avoid damaging the circuit.

5.5 EMI rejection

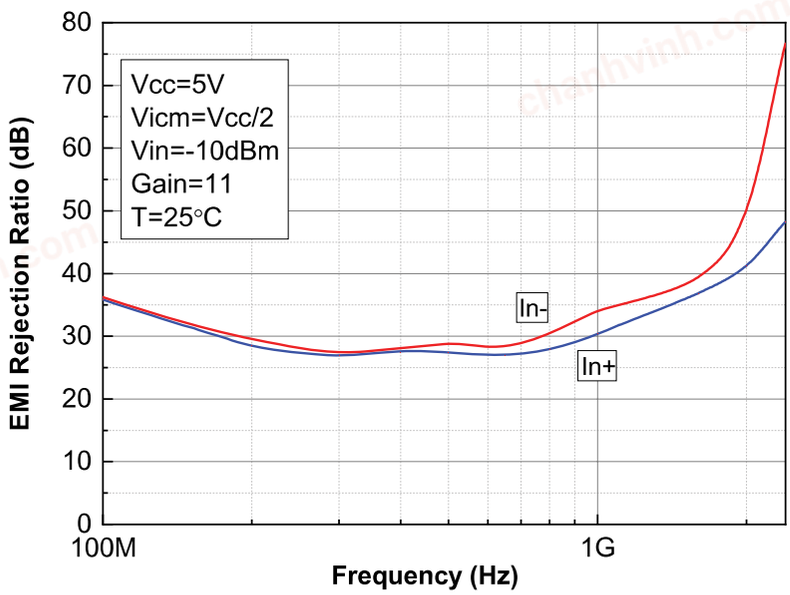
The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. EMIRR is defined in Eq. (9):

$$EMIRR = 20 \cdot log\left(\frac{V_{in\ pp}}{\Delta V_{io}}\right) \quad (9)$$

The TSV782 has been specially designed to minimize susceptibility to EMIRR and shows a low sensitivity. As visible in Figure 41, EMI rejection ratio has been measured on both inputs and output, from 400 MHz to 2.4 GHz.

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Figure 41. **EMIRR on In+ and In- pins**



EMIRR performances might be improved by adding small capacitances (in the pF range) on the inputs, power supply and output pins. These capacitances help minimize the impedance of these nodes at high frequencies.

5.6 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSV782 is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A \quad (10)$$

T_J is the die junction temperature

P_D is the power dissipated in the package

θ_{JA} is the junction to ambient thermal resistance of the package.

T_A is the ambient temperature.

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$P_D = (V_{CC} \times I_{CC}) + (V_{CC+} - V_{OUT}) \times ILoad$ when the op amp is sourcing the current.

$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} - V_{CC-}) \times ILoad$ when the op amp is sinking the current.

Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

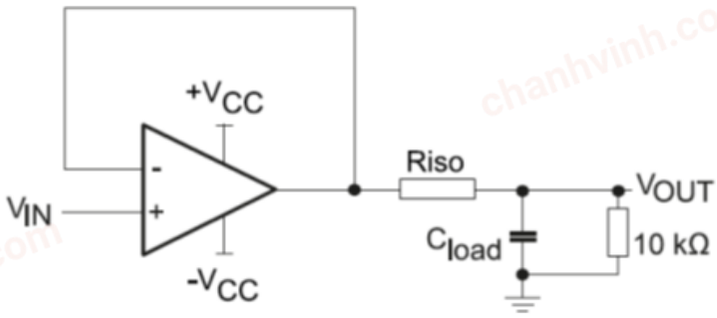
5.7 Capacitive load and stability

A stability analysis must be performed for large capacitive loads over 22 pF. Increasing the load capacitance to high values produces gain peaking in the frequency response, with overshoot and ringing in the step response.

Generally, unity gain configuration is the worst situation for stability and the ability to drive large capacitive loads. For additional capacitive load drive capability in unity-gain configurations, stability can be improved by inserting a small resistor R_{ISO} (10 Ω to 22 Ω) in series with the output. This resistor significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L. R_{ISO} modifies the maximum capacitive load acceptable from a stability point-of-view as described in the figure below:

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Figure 42. **Test configuration for R_{ISO}**



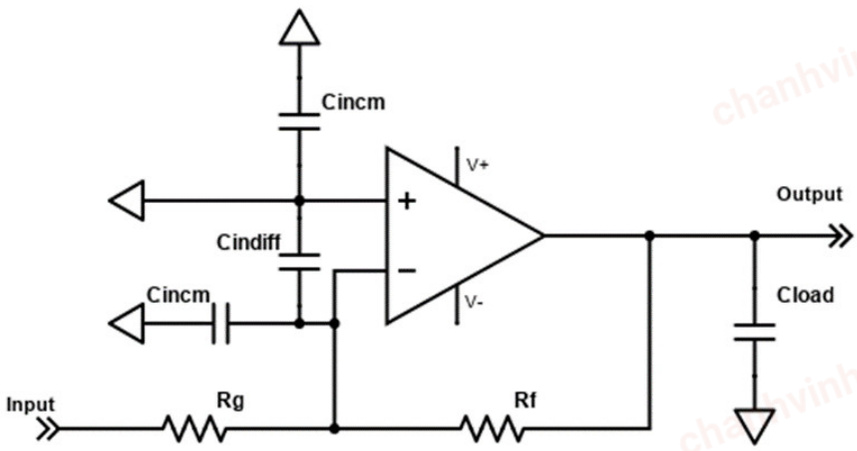
Please note that R_{ISO} = 22 Ω is sufficient to make the TSV782 stable whatever the capacitive load.

5.8 Resistor values for high speed op amp design

Due to its high gain bandwidth product (GBP), this op amp is particularly sensitive to parasitic impedances. Board parasitics should be taken into account in any sensitive design. Indeed, excessive parasitics (both capacitive and inductive) in the op amp frequency range can alter performances and stability. These issues can often be mitigated by lowering the resistive impedances.

More specifically, the RC network created by the schematic resistors (R_f and R_g) and the parasitic capacitances of both the op amp and the PCB can generate a pole below or in the same order of magnitude as the closed-loop bandwidth of the circuit. In this case, the feedback circuit is not able to fully play its role at high frequency, and the application can be unstable. This issue can happen when the schematic gain is low (typically < 5), or the device is used in follower mode with a resistor in the feedback. In these cases, it is advised to use a low value feedback resistor (R_f), typically 600 Ω.

Figure 43. **Inverting amplifier configuration with parasitic input capacitances**



Also, some designs use an input resistor on the positive input, generally of the same value as the input on the negative resistor. This resistor can be useful to balance the input currents on the positive and negative inputs, and reduce the impact of those input currents on precision. However, this is not useful on the TSV782 as the input currents are very low. Furthermore, this resistor can also interact with the input capacitances to generate a pole. The frequency of this pole should be kept higher than the closed-loop bandwidth frequency.

The macromodel provided takes into account the circuit parasitic capacitors. Thus, a transient spice simulation (100 mV step) is an easy way to evaluate the stability of the application. However, this cannot replace a hardware evaluation of the application circuit.

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5.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.10 Decoupling capacitor

In order to ensure op amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op amp supply pin. A good decoupling helps to reduce electromagnetic interference impact.

5.11 Macromodel

Accurate macromodels of the TSV782 device are available on the STMicroelectronics' website at: www.st.com. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSV782 operational amplifier. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, but they do not replace on-board measurements.

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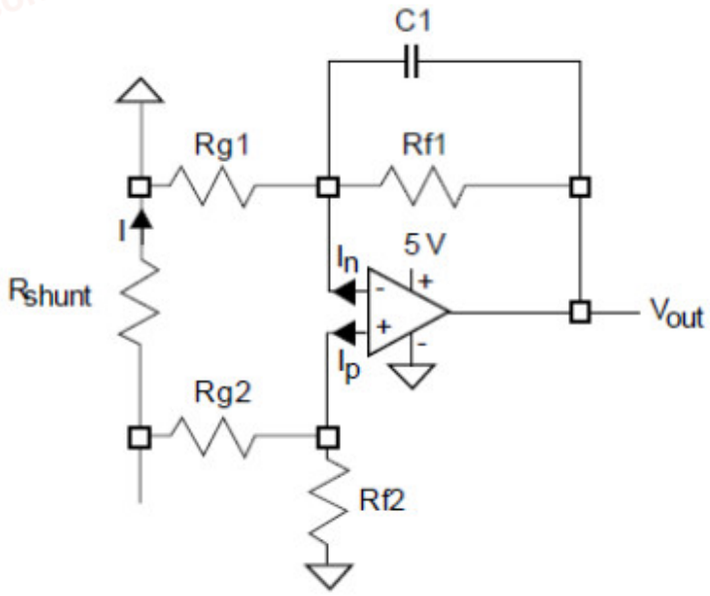
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6 Typical applications

6.1 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSV782 (see Figure below).

Figure 44. Low-side current sensing schematic



V_{out} can be expressed as follows:

$$V_{Out} = R_{shunt} \cdot I \left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right) \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p \cdot \frac{R_{g2} \cdot R_{f2}}{R_{g2} + R_{f2}} \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \cdot R_{f1} - V_{io} \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) \quad (11)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, Equation 10 can be simplified as follows:

$$V_{Out} = R_{shunt} \cdot I \cdot \frac{R_f}{R_g} - V_{io} \cdot \left(1 + \frac{R_f}{R_g}\right) + R_f \cdot I_{io} \quad (12)$$

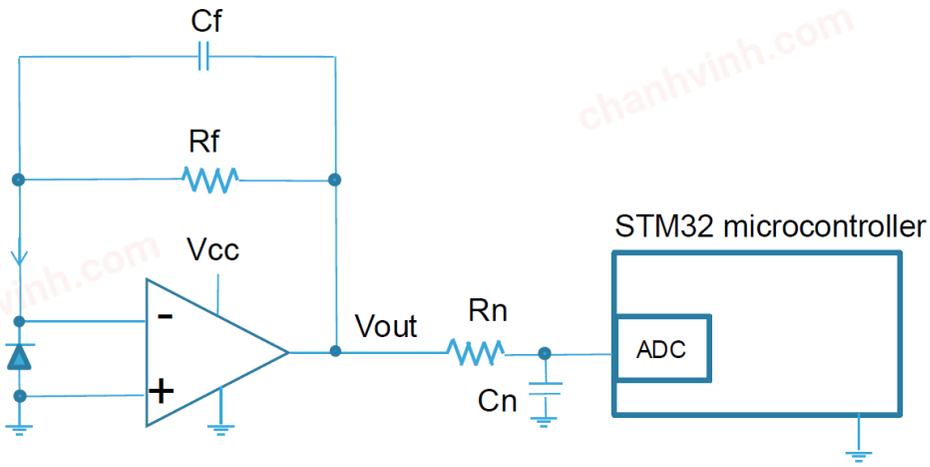
The main advantage of using the TSV782 for a low-side current sensing relies on its low V_{io}, compared to general purpose operational amplifiers. For the same current and targeted accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost. Particular attention must be paid to the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement.

6.2 Photodiode transimpedance amplification

The TSV782, with high bandwidth and slew rate, is well suited for photodiode signal conditioning in a transimpedance amplifier circuit. This application is useful in high performance UV sensors, smoke detectors or particle sensors.

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Figure 45. **Photodiode transimpedance amplifier circuit**



The transimpedance amplifier circuit converts the small photodiode output current in the nA range, into a voltage signal readable by an ADC following Eq. (13):

$$V_{Out} = R_f \cdot I_{photodiode} \quad (13)$$

The feedback resistance is usually in the MΩ range, in order to get a large enough voltage output range. However, together with the diode parasitic capacitance, the op amp input capacitances and the PCB stray capacitance, this feedback network creates a pole that makes the circuit oscillate. Using a small (few pF) capacitor in parallel with the feedback resistor is mandatory to stabilize the circuit.

The value of this capacitor can be tuned to optimize the application settling time with a spice simulation using the op amp macromodel, or by prototyping.

For more details on tuning this circuit, please read the application note AN4451.

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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 DFN8 2x2 package information

Figure 46. **DFN8 2x2 package outline**

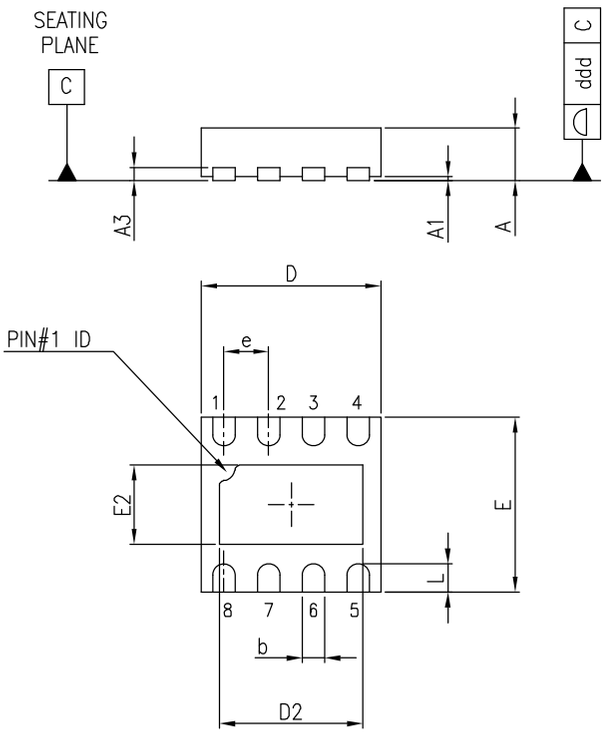
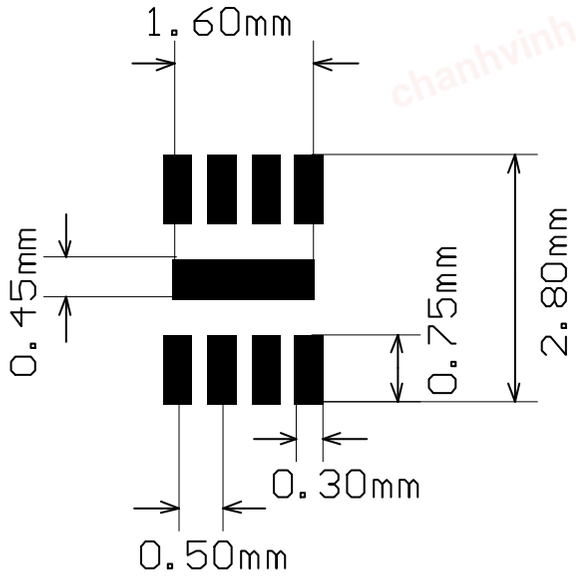


Table 7. **DFN8 2x2 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

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Figure 47. **DFN8 2x2 recommended footprint**



Note: The exposed pad of the DFN8 2x2 can be connected to VCC- or left floating.

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7.2 MiniSO8 package information

Figure 48. **MiniSO8 package outline**

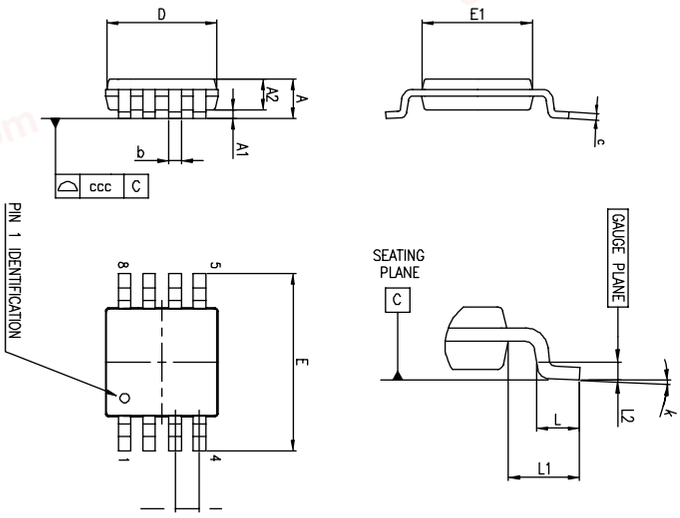


Table 8. **MiniSO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

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7.3 SO8 package information

Figure 49. **SO8 package outline**

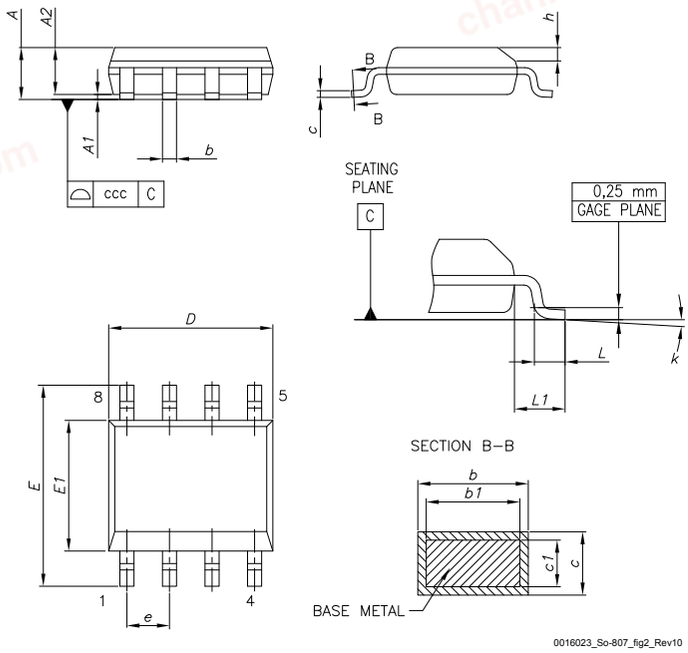
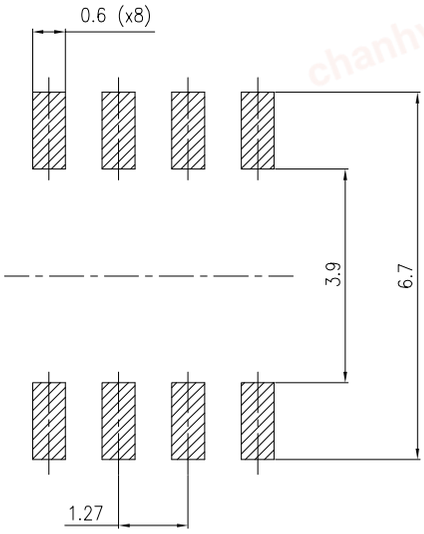


Table 9. **SO8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

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Figure 50. **SO8 recommended footprint**



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8 Ordering information

Table 10. **Order code**

Order code	Temperature range	Package	Marking
TSV782IQ2T	-40 °C to 125 °C	DFN8 2x2	K2M
TSV782IST		MiniSO8	K2M
TSV782IDT		SO8	TSV782I
TSV782IYST	-40 °C to 125 °C automotive grade (1)	MiniSO8	K232
TSV782IYDT		SO8	TSV782Y

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent. For qualification status detail, check "Maturity Status Link" on the first page of the datasheet, then, the "Quality & Reliability" tab on www.st.com.*

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Revision history

Table 11. **Document revision history**

Date	Revision	Changes
04-Jul-2022	1	Initial release.
02-Aug-2022	2	Added new Section 4 Typical performance characteristics.
19-Dec-2022	3	Added I_{ib} and I_{io} new values, -40 °C ≤ T ≤ 85 °C conditions in Table 4, Table 5 and Table 6

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