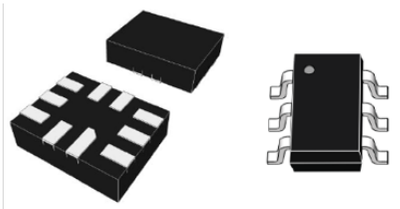
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TSC210, TSC211, TSC212
TSC213, TSC214, TSC215

Datasheet

High/low-side, bidirectional, zero-drift current sense amplifiers



QFN10 (1.8x1.4) SC70-6

Features

- Wide common mode voltage: -0.3 to 26 V
- Offset voltage: ±35 µV max. (TSC210)
- 2.7 to 26 V supply voltage
- Different gain available
  - TSC210 (200 V/V)
  - TSC211 (500 V/V)
  - TSC212 (1000 V/V)
  - TSC213 (50 V/V)
  - TSC214 (100 V/V)
  - TSC215 (75 V/V)
- Gain error: ±1% max.
- Offset drift: 0.1 µV/°C max.
- Gain drift: 20 ppm/°C max.
- Quiescent current: 100 µA
- QFN10 (1.8x1.4) and SC70-6

Applications

- Telecom equipment
- Power management
- Notebook computers
- Industrial applications
- Battery chargers

Product status link
TSC210, TSC211, TSC212, TSC213, TSC214 and TSC215

Description

The TSC210, TSC211, TSC212, TSC213, TSC214 and TSC215 are a series of zero-drift current sense amplifiers that can sense current via a shunt resistor over a wide range of common mode voltages from -0.3 to +26 V, whatever the supply voltage is. They are available in three different versions, each of them having a different gain. The TSC21x are designed with a specific zero-drift architecture, which can achieve high precision.

The TSC21x are current sense amplifiers that may be used in various functions such as precision current measurement, over current protection, current monitoring, feedback loops.

These devices fully operate over the broad supply voltage range of 2.7 to 26 V and over the industrial temperature range -40 to 125 °C.

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1 Pin connections and description

Figure 1. Pin connections (top view)

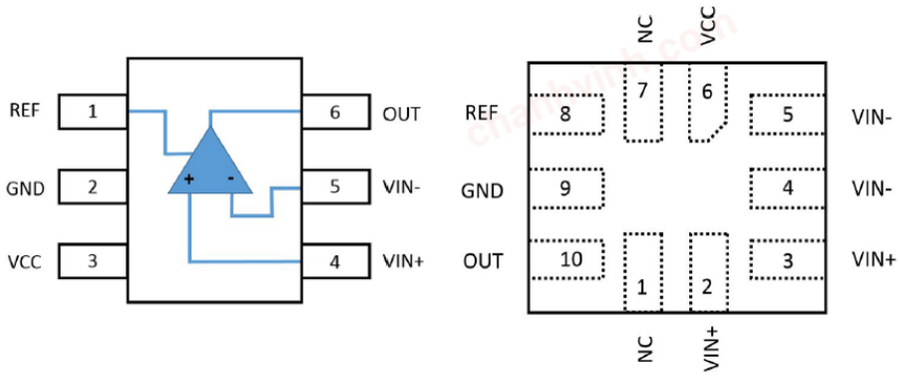


Table 1. Pin description

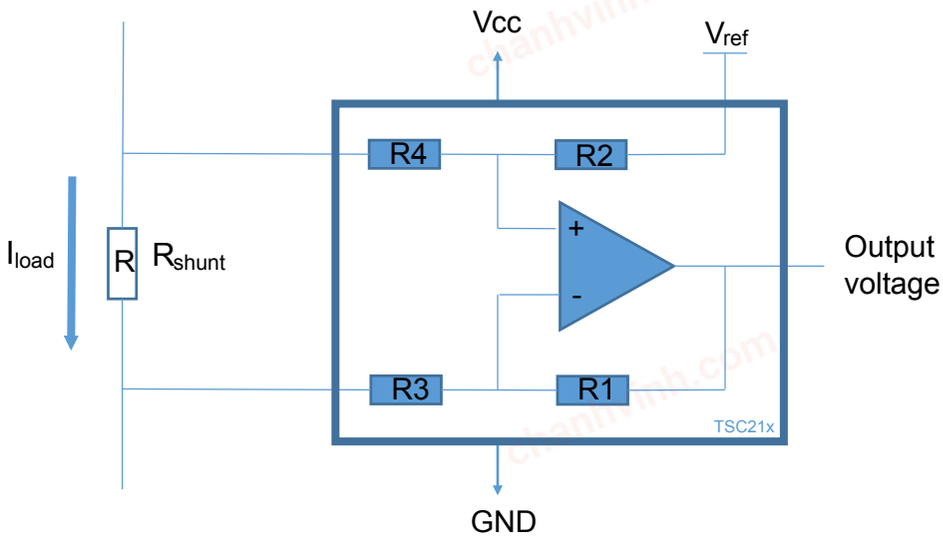
Name	SC70-6	QFN10	Description
REF	1	8	Reference voltage input
GND	2	9	Ground
Vcc	3	6	Power supply voltage
Vin+	4	2, 3	Connection to the external sense resistor
Vin-	5	4, 5	Connection to the external sense resistor
OUT	6	10	Output voltage
NC		1, 7	Not connected(1)

1. *Pins can be left floating or connected to VCC or GND.*

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2 Block diagram

Figure 2. **Block diagram**



$$\text{Output voltage} = (R_{shunt} \times I_{load}) \times \text{Gain} + V_{ref}$$

Table 2. **Resistors and gain values**

Product	R1 and R2	R3 and R4	Gain
TSC210	1 MΩ	5 kΩ	200
TSC211	1 MΩ	2 kΩ	500
TSC212	1 MΩ	1 kΩ	1000
TSC213	1 MΩ	20 kΩ	50
TSC214	1 MΩ	10 kΩ	100
TSC215	1 MΩ	13.3 kΩ	75

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3 Absolute maximum ratings and operating conditions

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	26	V
V_{IN}	Differential voltage between input pins (In+, In-)	-26 to +26	V
	Common mode voltage on input pins	Gnd-0.3 to 26	
Ref	Reference input voltage	Gnd-0.3 to Vcc+0.3	V
I_{in}	Input current to any pin(2)	5	mA
V_{out}	Output voltage	Gnd-0.3 to Vcc+0.3	V
T_{Lead}	Lead temperature for 10 s(3)	260	°C
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Junction temperature	150	°C
R_{th-ja}	Thermal resistance junction to ambient (4)(5) QFN10 SC70-6	 124 232	°C/W
ESD	HBM: human body model(6)	4000	V
	CDM: charged device model (7)	1000	

1. *All voltage values, except the differential voltage are with respect to the network ground terminal.*
2. *Due to AMR on input current (Iin), differential voltage may be limited.*
3. *Reflow at peak temperature of 260 °C. Time above 255 °C must not exceed 30 s.*
4. *Short-circuits can cause excessive heating and destructive dissipation.*
5. *R_{th} are typical values.*
6. *According to JEDEC standard JESD22-A114F.*
7. *According to ANSI/ESD STM5.3.1.*

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 26	V
V_{icm}	Common mode voltage on input pins	-0.3 to +26	V
T	Operating free-air temperature range	-40 to 125	°C

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4 Electrical characteristics

Table 5. Electrical characteristics, T = 25 °C, V_{SENSE} = V_{IN+}- V_{IN-} (unless otherwise specified), TSC210, TSC213, TSC214, TSC215: V_{CC}= 5 V, V_{IN+}=12 V, V_{REF}= V_{CC}/2 (unless otherwise specified), TSC211, TSC212: V_{CC} = 12 V, V_{IN+} = 12 V, V_{REF} = V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
V_{cc}	Supply voltage		2.7		26	V
I_{cc}	Quiescent current	V_{SENSE} = 0 mV		65	100	µA
		Tmin. < T < Tmax.			115	
Input						
V_O	Offset voltage (RTI) (1)					
	TSC210, TSC211, TSC212	V_{SENSE} = 0 mV	-35		35	µV
	TSC214, TSC215	V_{SENSE} = 0 mV	-60		60	
	TSC213	V_{SENSE} = 0 mV	-100		100	
$\|\Delta V_O/\Delta_T\|$	Offset voltage variation (RTI) vs. temperature	V_{SENSE} = 0 mV, Tmin.< T < Tmax.		0.05	0.3	µV/°C
CMRR	Common mode rejection ratio					
	TSC210, TSC211, TSC212	V_{IN}+= 0 to 26 V, V_{SENSE} = 0 mV, Tmin. < T < Tmax.	105	140		dB
	TSC213, TSC214, TSC215	V_{in}+= 0 to 26 V, V_{SENSE} = 0 mV, Tmin. < T < Tmax.	100	120		
PSRR	Power supply rejection ratio	V_{cc}= 2.7 to 26 V V_{IN}+=18 V, V_{SENSE} = 0 mV		0.1	10	µV/V
I_{IB}	Input bias current	V_{SENSE} = 0 mV	15	28	35	µA
I_{IO}	Input offset current	V_{SENSE} = 0 mV		0.02		
Output						
G	Gain	TSC210		200		V/V
		TSC211		500		
		TSC212		1000		
		TSC213		50		
		TSC214		100		
		TSC215		75		
E_G	Gain error	V_{SENSE} = -5 to + 5 mV Tmin. < T < Tmax.		0.02	±1	%
T_G	Gain error vs. temperature	Tmin. < T < Tmax.		7	20	ppm/°C
NLE	Linearity error	V_{SENSE} = -5 to + 5 mV		0.01		%

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_L	Maximum capacitive load	No sustained oscillation		470		pF
$V_{sw}+$	Output swing close to V_{CC}	R_L=10 kΩ to Gnd Tmin. < T < Tmax.	V_{cc}-0.2	V_{cc}-0.05		V
$V_{sw}-$	Output swing close to Gnd	R_L=10 kΩ to Gnd Tmin. < T < Tmax.		5	30	mV
R_{Load}	Load regulation	I_{OUT}= -10 to +10 mA		0.5		Ω
Dynamic performance						
BW	Bandwidth	V_{CC} = 5 V, V_{icm} = 12 V, Cl = 100 pF				kHz
		TSC210		25		
		TSC211		8		
		TSC212		6		
		TSC213		100		
		TSC214		40		
		TSC215		60		
SR	Slew rate	V_{CC} = 5 V, V_{icm} = 12 V, Cl = 100 pF				V/µs
		TSC210		0.2		
		TSC211		0.075		
		TSC212		0.05		
		TSC213		0.85		
		TSC214		0.32		
		TSC215		0.42		
E_N	Noise (RTI)(1)	f = 1 kHz				nV/√Hz
		TSC210		40		
		TSC211		48		
		TSC212		50		
		TSC213		38		
		TSC214		40		
		TSC215		39		

1. *RTI stands for "related to input"*

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5 Typical characteristics

The TSC210 is used for typical characteristics, unless otherwise specified

Figure 3. Input offset voltage production distribution

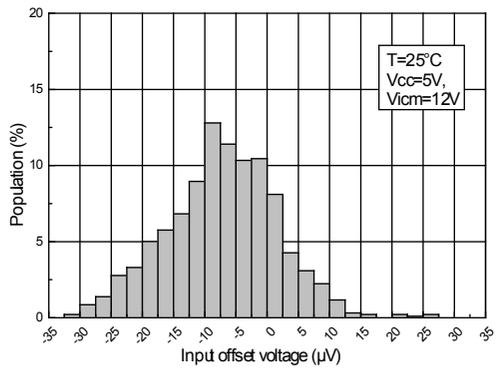


Figure 4. Input offset voltage vs. temperature

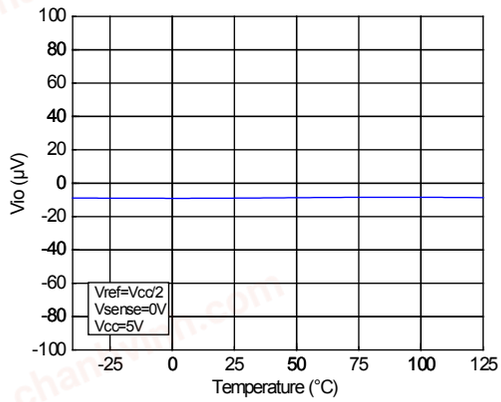


Figure 5. Common-mode rejection ratio production distribution

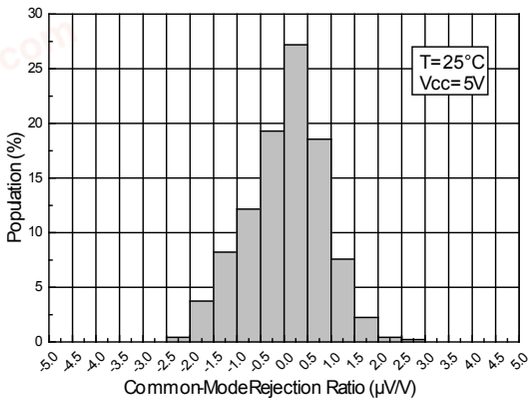
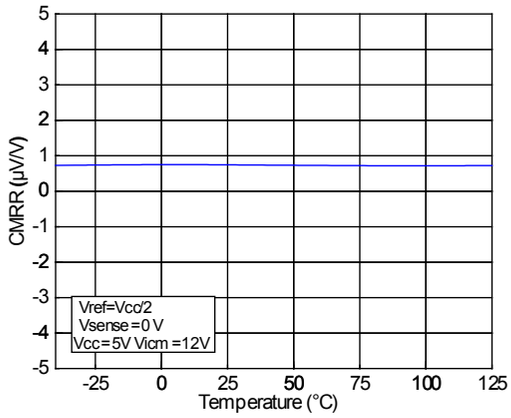


Figure 6. Common mode rejection ratio vs. temperature



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Figure 7. Gain vs. frequency

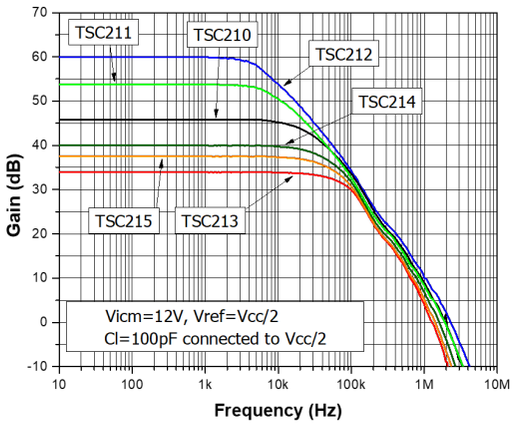


Figure 8. Power supply rejection ratio vs. frequency

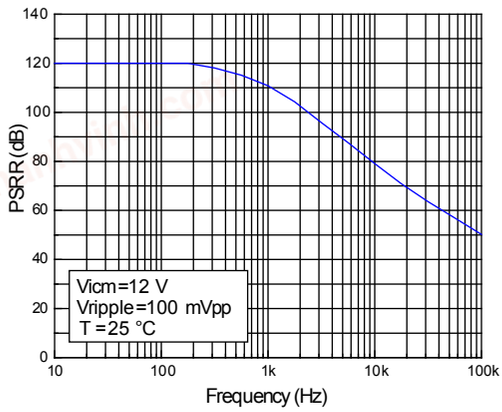


Figure 9. Common mode rejection ratio vs. frequency

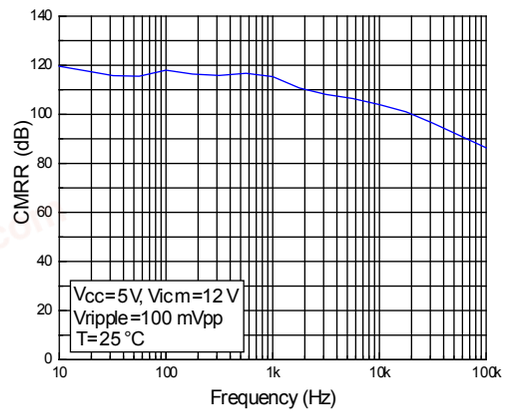


Figure 10. Positive output voltage swing vs. output current V_{CC} = 2.7 V

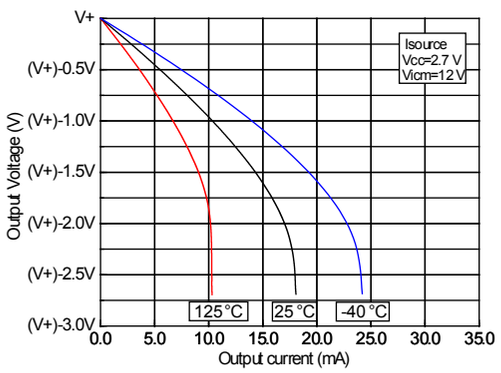


Figure 11. Negative output voltage swing vs. output current V_{CC} = 2.7 V

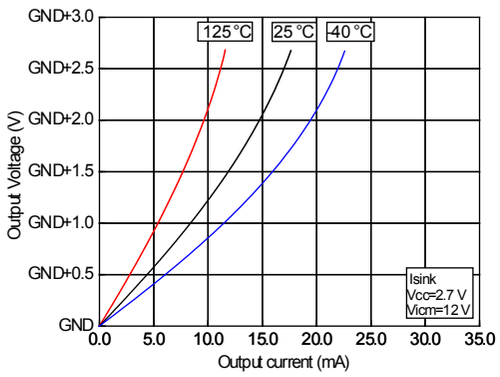
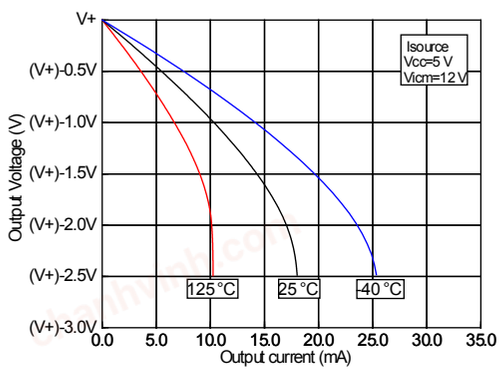


Figure 12. Positive output voltage swing vs. output current V_{CC} = 5 V



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Figure 13. Negative output voltage swing vs. output current V_{CC} = 5 V

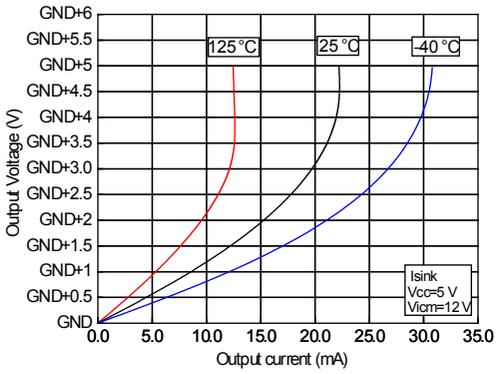


Figure 14. Positive output voltage swing vs. output current V_{CC} = 26 V

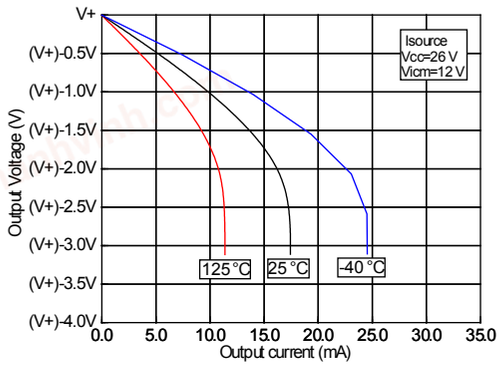


Figure 15. Negative output voltage swing vs. output current V_{CC} = 26 V

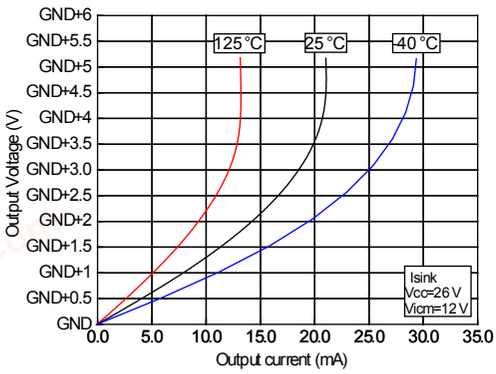


Figure 16. Input bias current vs. input common mode voltage with supply voltage = 5 V

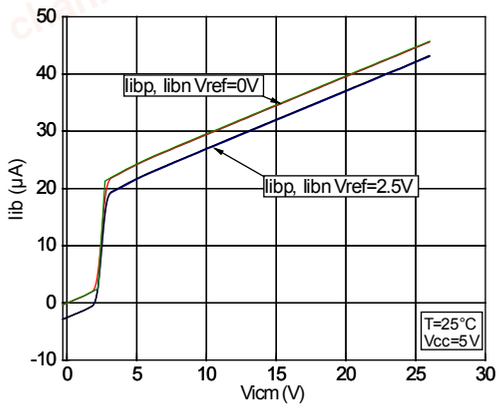


Figure 17. Input bias current vs. input common mode voltage with supply voltage = 0 V

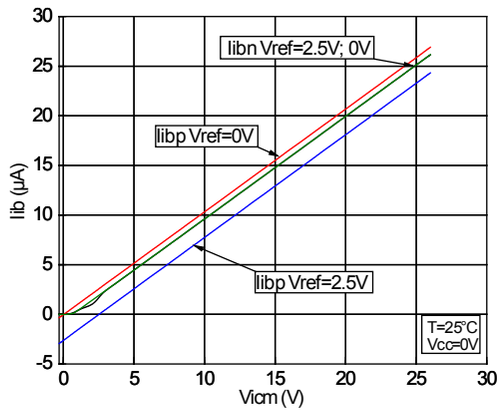
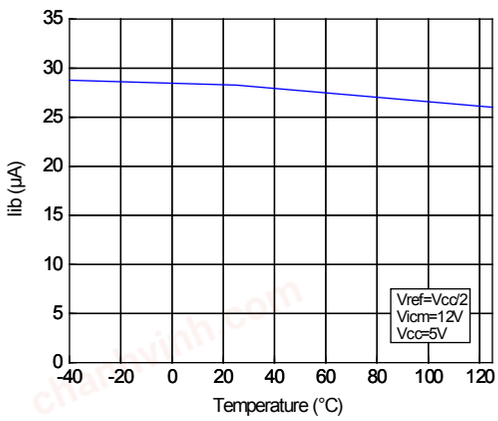


Figure 18. Input bias current vs. temperature



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Figure 19. Quiescent current vs. temperature

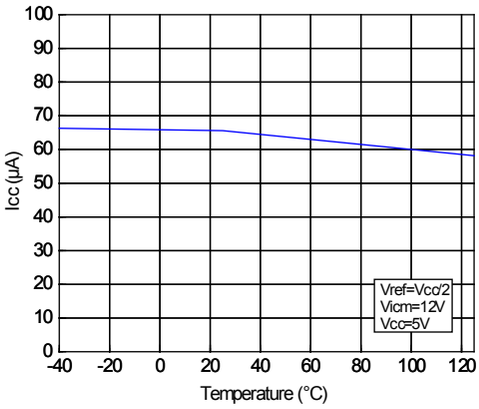


Figure 20. Input referred noise vs. frequency

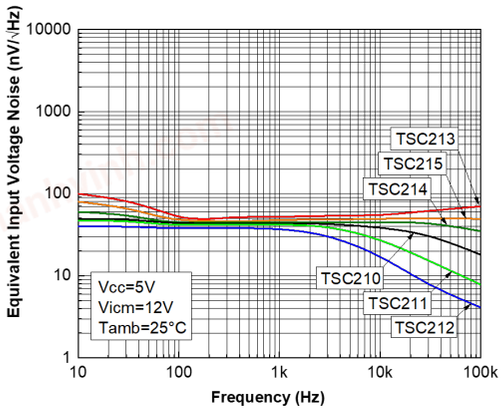


Figure 21. 0.1 Hz to 10 Hz voltage noise (referred to input)

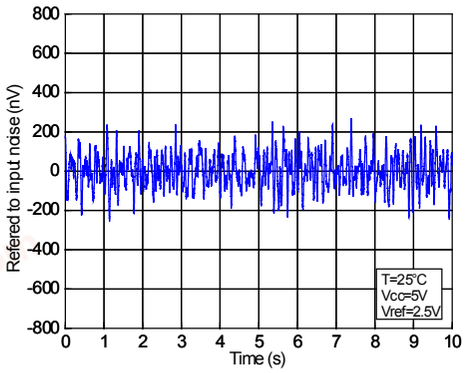


Figure 22. Step response (10-mVpp input step)

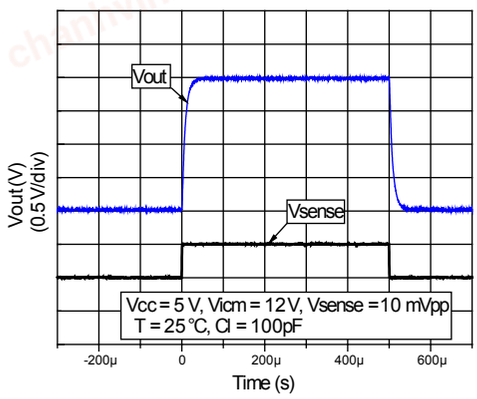


Figure 23. Common mode voltage transient response

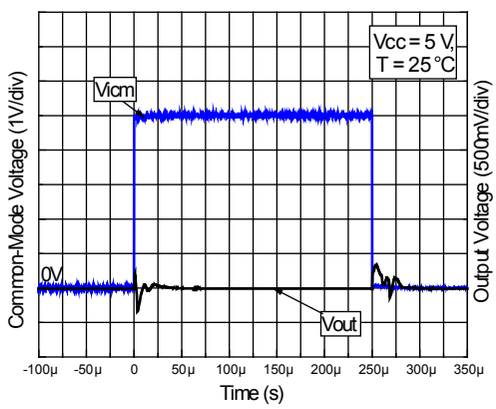
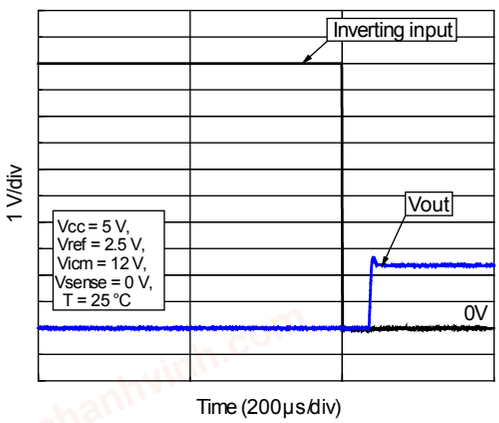


Figure 24. Inverting differential input overloaded



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Figure 25. Non inverting differential input overload

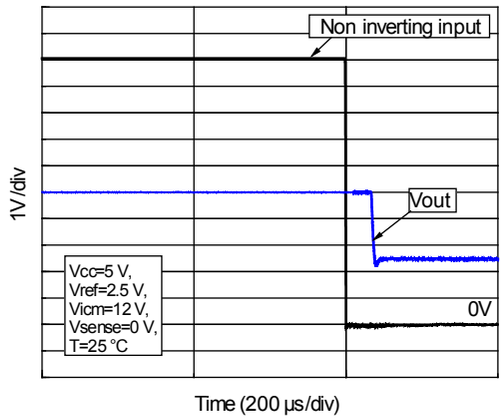


Figure 26. Start-up response

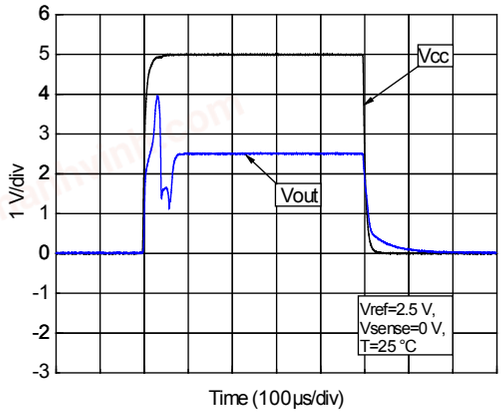
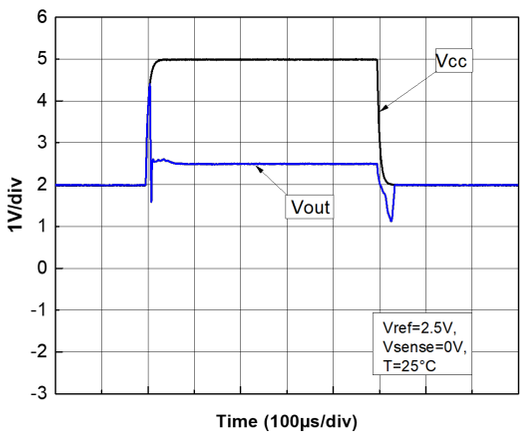


Figure 27. Brownout recovery



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6 Application information

6.1 Overview

TSC21x series are specially designed to accurately measure current by amplifying the voltage across a shunt resistor connected to its input. This voltage drop Vsense, is then amplified by an instrumentation amplifier providing a max. input offset voltage of 35 µV (25 °C) for an input common voltage of 12 V for gain higher than 200.

TSC21x series with the use of thin film resistor and zero-drift architecture, offer an extremely precise input offset voltage, gain error and very high CMRR performance even in high frequency range. Moreover, thanks to the possibility to fix the output common mode voltage, the TSC21x can be either used as unidirectional or bidirectional current sensing amplifier.

TSC21x provide an extended input common range from ground, and up to 26 V allowing either low-side or high-side current sensing, while the TSC21x devices can operate from 2.7 to 26 V.

The parameters are very stable in the full V_{CC} range and several characterization curves show the TSC21x device characteristics at 5.0 V. Additionally, the main specifications are guaranteed in extended temperature ranges from - 40 to 125 °C.

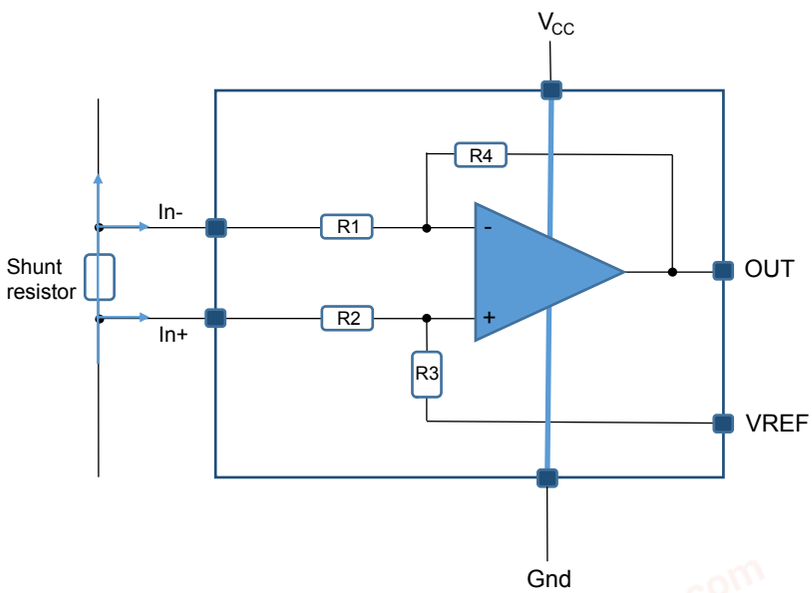
6.2 Theory of operation

The main particularity of the TSC21x is the ability to work with input common mode voltage largely beyond the power supply V_{cc} range.

- **V_{icm} > 2.5 V**

In this case, the power supply of the TSC21x is issued from the input and not only from the V_{cc} power supply. More precisely a current is drawn from the common mode rail as depicted in Figure 28 to power it.

Figure 28. Power supply when V_{icm} > 2.5 V

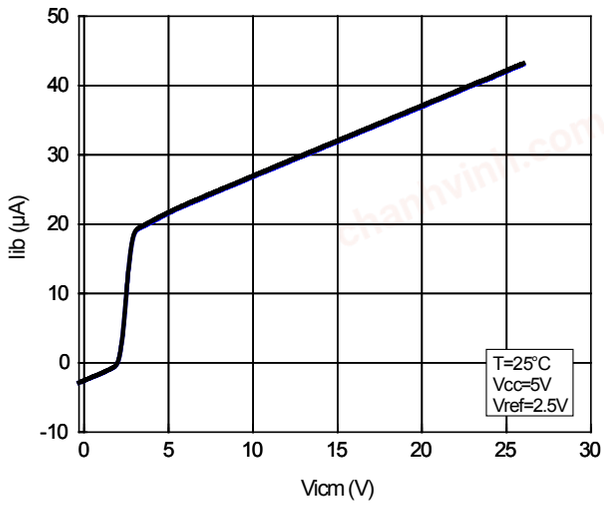


In Figure 29 we can see that the current used to power the TSC21x is increasing with the V_{icm} voltage. The slope is representing the internal common mode resistances. Part of it being V_{icm} / (R4 + R1) and part of it serving to supply the input stage of the circuit, roughly 20 µA.

So due to the architecture of the TSC21x the current to be measured through the shunt resistor must be much larger than the input bias current. In case of small current to measure the I_{ib}, current must be taken into account.

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Figure 29. **Input bias current vs. common mode voltage V_{cc} = 5 V**



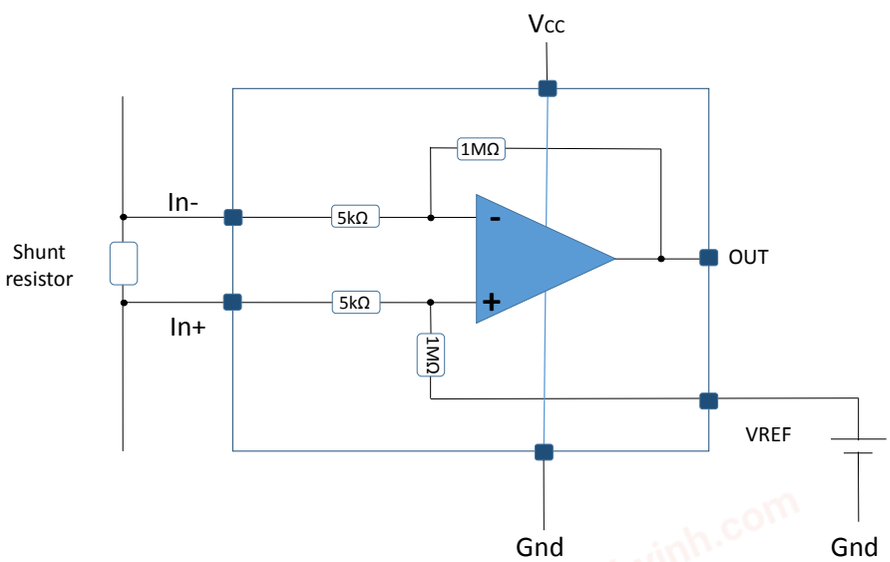
- **Output common mode range**

The TSC21x output common mode voltage level can be set thanks to voltages applied on the V_{ref} pin. This pin allows to set the device either in bidirectional or in unidirectional operation. The voltage applied on this pin must not exceed the V_{cc} range. The different configurations are detailed in the chapter Unidirectionnal/Bidirectionnal operation.

As depicted by Figure 30 and using a TSC210, the V_{ref} pin can be driven by an external voltage source capable of sourcing/sinking a current following the below equation 1:

$$Iref = \frac{Vicm - Vref}{R1 + R4} = \frac{Vicm - Vref}{5k\Omega + 1M\Omega} \quad (1)$$

Figure 30. **V_{ref} powered by an external voltage source with a TSC210**



When the output common mode voltage is supplied by an external power supply, in order to improve the output voltage measurement, it is recommended to measure the V_{out} differentially with respect to V_{ref} voltage. It provides a best CMRR measurement, a best noise immunity and also a more accurate V_{out} voltage. A decoupling capacitance of 1 nF minimum can be also added in order to better filter the power supply, and can also be used as a tank capacitance in case an ADC is connected to this reference voltage.

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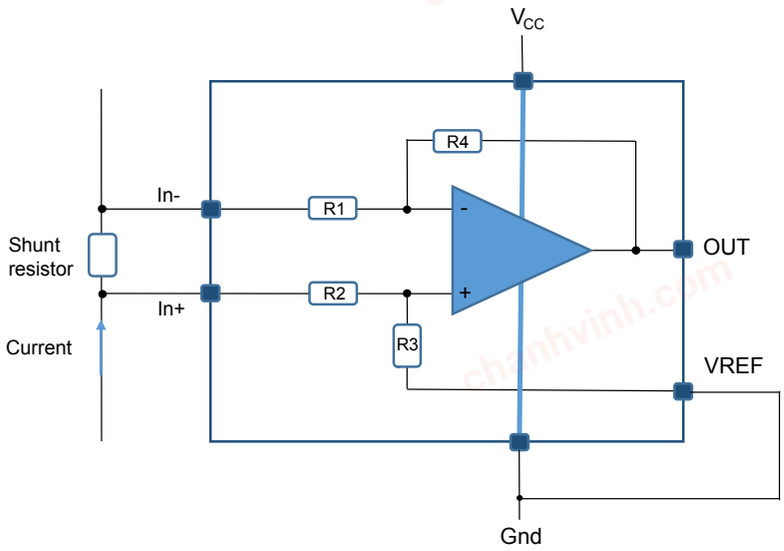
6.3 Unidirectionnal / bidirectionnal operation

- Unidirectional operation

Unidirectional mode of operation allows the device to measure the current through a shunt resistor in one direction only. The output reference can be Ground or V_{cc} and can be set by using V_{ref} pins for adjustment.

- Ground referenced

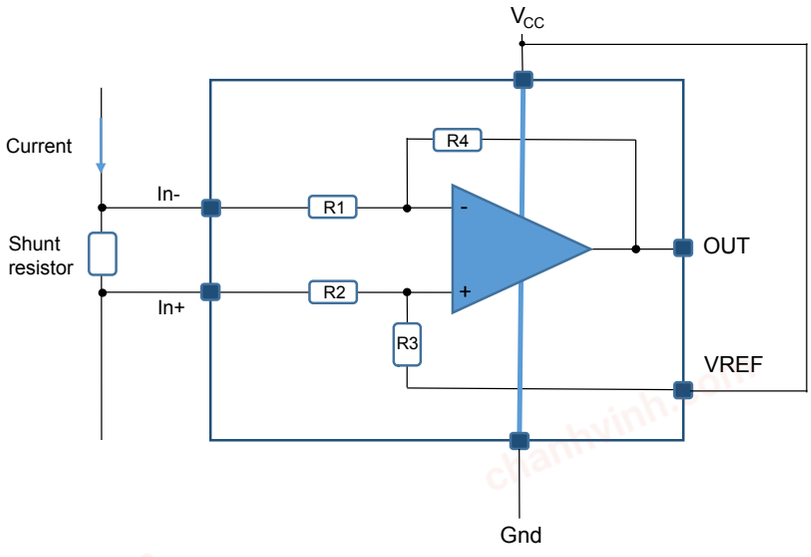
Figure 31. Output reference to ground



In this configuration the V_{ref} pin is connected to the ground. The output common mode voltage is then automatically set to GND when no current flows through the Rshunt resistance. This configuration allows the full-scale output in unidirectional mode. It allows to measure a current as described in Figure 31.

- V_{cc} referenced

Figure 32. Output reference to V_{cc}



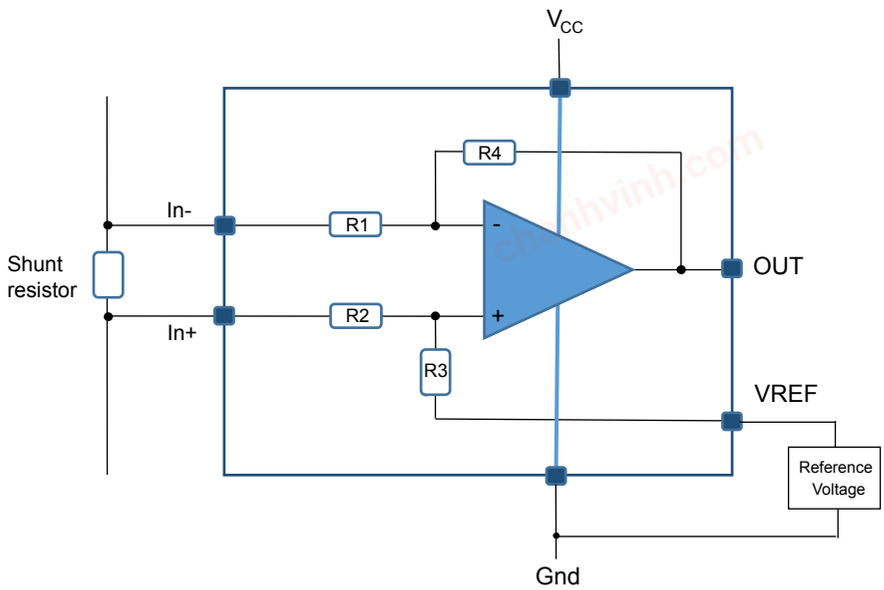
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In this configuration the V_{ref} pin is connected to the V_{cc} power supply. The output common mode voltage is then automatically set to V_{cc} voltage when no current flows through the R_{shunt} resistance. This configuration allows the full-scale output in unidirectional mode. It allows to measure a current as described in Figure 32

- Bidirectional operation

Bidirectional mode of operation allows the device to measure currents through a shunt resistor in two directions. The output reference can be set anywhere within the power supply range. If the output common mode voltage is set at mid-range, the full-scale current measurement range is equal in both directions. It can be done by connecting V_{ref} pins to a reference voltage as suggested by Figure 33. In case the current measurement is not equal in both directions, users can set the output in a non-symmetrical configuration, adjusting V_{ref} according to user needs.

Figure 33. External supply



Another simpler way to generate the reference voltage to fix the output common mode voltage can be used. As, for example, a resistive divider; in this case, as the V_{REF} pin must be connected to a low impedance, it is important to add a buffer stage between the V_{REF} pin and the resistive divider. The buffer can be simply done with an opamp as TSB611 in follower configuration.

If for any reason the voltage on the V_{ref} pin exceeds the power supply by 0.5 V, the ESD diodes become conductive and excessive current can flow through them. Without limitation this overcurrent can damage the device. In this case, it is important to limit the current to 5 mA.

6.4 R_{SENSE} selection

The selection of the shunt resistor is a trade-off between dynamic range and power dissipation.

Generally, in high current sensing application, the main focus is to reduce as much as possible the power dissipation (I^2R) by choosing the smallest value of shunt. It could be quite easy if full-scale current to measure is small.

In low current application, the R_{sense} value could be higher, to minimize the impact of the offset voltage of the circuit. Still keep in mind that due to input bias of several µA the TSC21x cannot measure current in the same range, when the common mode voltage overpasses 2.5 V (refer to Section 6.2 Theory of operation).

The trade-off is mainly when a dynamic range of current to measure is large, meaning ability to measure with the same shunt value low current to high current. Generally, the current full scale (Imax-Imin) defines the shunt value thanks to the full output voltage range, the gain of the TSC21x.

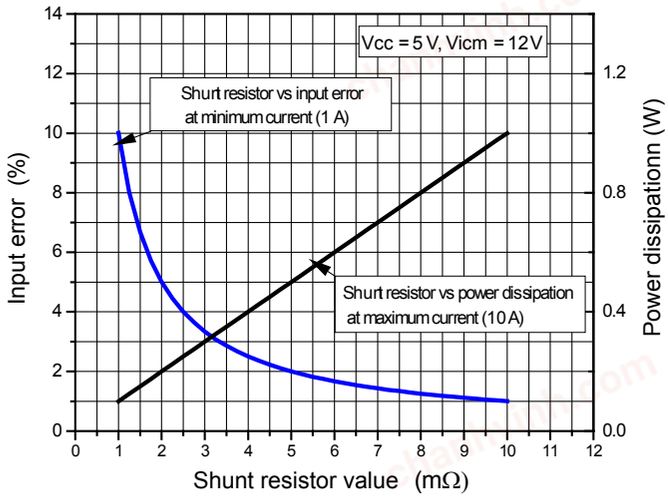
Let's illustrate with a simple example. In battery application a current in the range of 1 A to 10 A must be measured. A TSC213 with a gain of 50 is chosen.

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Even if the TSC213 is a zero-drift current sensor allowing small shunt use, at first order the input offset voltage (V_{io}) and the input bias current (I_{ib}) should be put in with regards to the differential voltage in the shunt resistance.

Figure 34 shows the trade-off between the accuracy at minimum current and power dissipation.

Figure 34. Shunt resistor value trade-off (TSC213)



Increasing the shunt resistor values improves current accuracy, but also increases power dissipation!

- If power dissipation in the shunt is the key point, R_{Sense} should be chosen as

$$Rsense \leq \frac{Pmax}{Imax^2}$$

and then chose the right TSC21x gain products. For example, for high current to sense, it is better to use the TSC212 offering a gain of 1000, allowing to use a smaller shunt and so limited power losses. But accuracy can be lower.

- Or choose the TSC21x gain product available on the shelf, and then size the shunt resistor value accordingly.

6.5 Input offset voltage drift overtemperature

The maximum input offset voltage drift overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift overtemperature is computed using equation 2:

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right| \quad (2)$$

where T = - 40 °C and 125 °C

The TSC21x datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

6.6 Error calculation

The principal source of error as input offset voltage, gain error, common mode rejection ration, are described separately in the electrical characteristics. This section summarizes the most important error to take into account during a design phase.

- Input offset voltage error

In a precision domain most of the time the input offset can be a major influence in the output error. It is so important to take it into account and also the derivation in temperature as depicted by equation 3:

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$$Vio\ Error = (\pm Vio \pm Dvio/Dt)*Gain \quad (3)$$

The TSC21x series have a zero drift architecture allowing to present very small input offset and also an extremely low variation in temperature.

- Gain error and shunt resistance accuracy

$$Gain\ error = Gain(1 + \varepsilon gain) \quad (4)$$

$$Rsense\ error = Gain(1 + \varepsilon Rsense) \quad (5)$$

where $\varepsilon gain$ is the gain error 1% max. for the TSC21x.

Where $\varepsilon Rsense$ is the shunt resistance error. Shunt resistors from 5 mΩ to 100 mΩ are available with 1% accuracy or better.

- CMR error

In the electrical characteristics CMR is specified at one input common mode voltage. So in order to take into consideration the variation of the input voltage offset depending on the Vicm, the calculus must be done till this known point. V_{icm} = 12 V is the reference point.

So the error on V_{out} due to a common mode voltage variation can be written as in equation 6:

$$CMR\ error = \pm \frac{Vicm - 12V}{CMR} * Gain \quad (6)$$

- Noise

One of the other advantages of the zero-drift architecture, is to reject the low frequency noise over the bandwidth, and allow to have a white noise on all the bandwidth of the current sensing.

This is a real added value for the precision measurement especially in DC environment. Figure 20 express the noise referred to the input of the TSC210. The TSC213 has white noise density of 38 nV/√Hz, on its whole bandwidth.

The RMS value of the output noise of the TSC213 is the integration of the spectral noise over the bandwidth of interest and can be expressed as equation 7:

$$\text{enRMS} = \left(\sqrt{\int_{0.1}^{100000 \cdot \frac{\pi}{2}} \left(38 \cdot 10^{-9}\right)^2 df}\right) * \text{Gain} \quad (7)$$

- Total output voltage

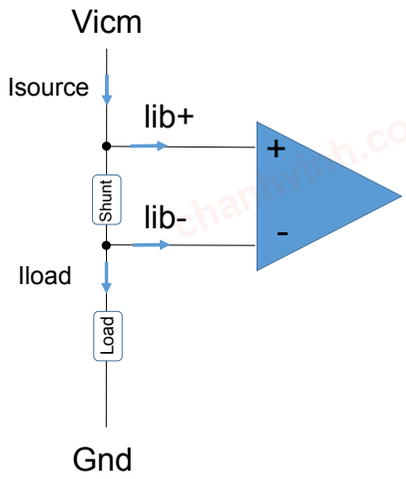
The maximum total error that might happen on the output of the device in worst case condition can be described as the sum of the different source described just above. The total output voltage can be written as equation (8).

$$Vout = G\left(1 + \varepsilon G + \frac{dG}{dT} * \Delta T\right) \cdot \left(Rshunt\left(1 + \varepsilon shunt\right) \cdot \left(Isense\right) + \left(Vio + \left(\frac{dVio}{dT}\right) * \Delta T\right) + \left(\frac{Vicm - 12V}{CMRR}\right)\right) + noise \quad (8)$$

Note that the input bias currents are not considered in this section, as it has been already integrated in the V_{sense}. Figure 35 below depicts the current flowing from the source to the load when the input common mode voltage is higher than 2.5 V.

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Figure 35. **Input current**



From a calculation approach when working with a V_{icm} over 2.5 V, if I_{source} is considered to be known rather than the I_{load}, in this case the input bias current should be taken into consideration.

Figure 35 express also the fact that the TSC21x cannot measure current in the same order than input bias current (several hundreds of µA).

- Example

Let's take an example to get a better understanding of the maximum total error that can happen on the output of the TSC213.

Use case:

- V_{cc} = 5 V
- V_{icm} = 24 V
- V_{ocm} = 2.5 V
- Temperature = 25 °C
- I_{load} = 5 A
- Shunt 5 mΩ with 1% accuracy

Theoretically the expected output voltage should be $V_{out} = R_{shunt} * I_{load} * 50 + V_{ref}$ = 3.75 V.

From the above equations let's detail all the error terms by using the maximum value of the electrical characteristic (when available), in order to express as much as possible, the worst case condition. The % error on output of the following table is expressed in reference to $V_{out} – V_{ref}$, so in this typical example: 1.25 V.

Table 6. **Gain error**

Error source	Calculus	Output voltage error	% error on output
Gain error	$50*5.10^{-3}*5*1\%$	12.5 mV	1%
V_{io} error	$50*100\mu V$	5 mV	0.4%
CMRR error	$50*\frac{24V-12V}{\frac{100}{10\sqrt{20}}}$	6 mV	0.5%
Noise	$50*\frac{38nV}{\sqrt{Hz}}\sqrt{100kHz*\frac{\pi}{2}-0.1Hz}$	0.75 mV_{RMS}	0.2%
Total		18.1 mV +0.75 mV_{RMS}	2.1%

1. *The percentage is based on voltage peak value and is 3 times RMS value.*

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So the maximum output voltage in worst case condition at ambient temperature is 3.768 V + 0.75 mVRMS instead of 3.75 V expected. This represents an error on the current reading of about 2.1%. 1% more must be added due to the shunt accuracy.

It is important to note that this calculus has been done by using all the maximum values and all the error terms have been added to each other, meaning that the chance of getting 2.1% precision in the above use case is extremely low and on the whole population, the error is considerably smaller.

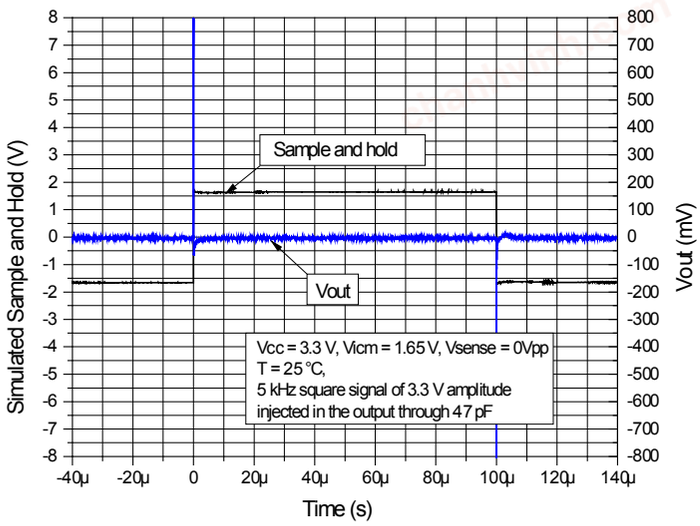
6.7 Stability

- Driving switched capacitive loads

Some ADC get their signal thanks to a sample and hold capacitor. If before a sampling this capacitance is fully discharged, a fast current load can appear on the output of the TSC21x during the sampling phase.

The scope probe below in Figure 36 shows the output voltage of the TSC213 excited through a 40 pF capacitor with a 3.3 Vpp signal at 5 kHz to simulate the sample and hold circuit of an ADC.

Figure 36. Capacitive load response at V_{cc} = 3.3 V

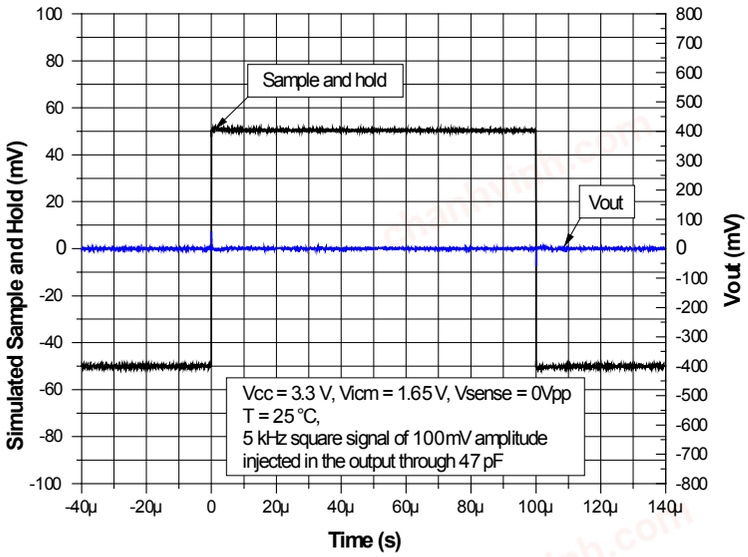


The graph in Figure 36 shows the behavior of the output of the TSC213 under worst case condition, as for example, when there is an ADC channel change between two measurements.

If a single channel is used, the change on the sample and hold capacitance is certainly very small, and so the recovery time is extremely low as described by Figure 37.

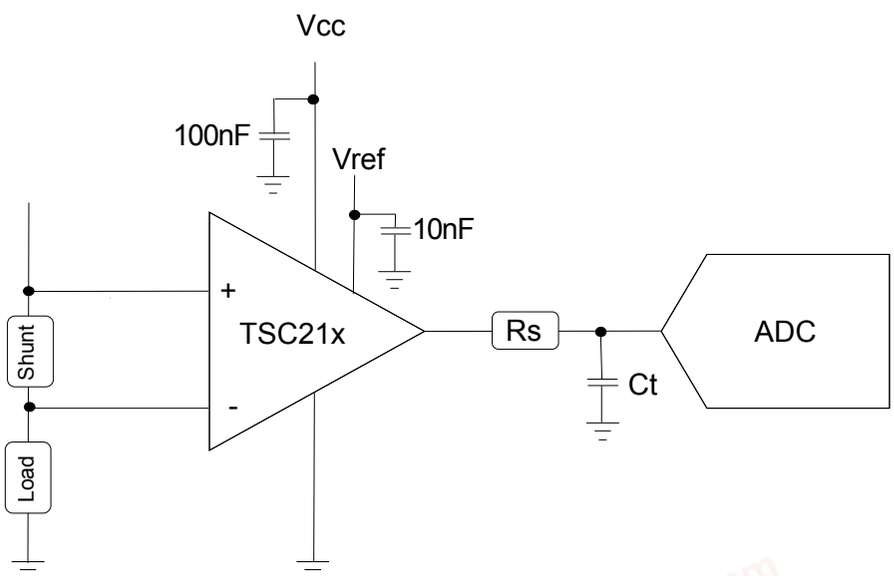
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Figure 37. **Capacitive load response at V_{cc} = 3.3 V with a step of 100 mV**



The effect of the ADC sampling and hold can be easily smoothed thanks to an RC filter. As suggested in the schematic below in Figure 38. The capacitor of the external filter much be chosen much higher than the internal ADC capacitor, in order to easily absorb the sudden voltage variation on the output due to the sampling and hold of the ADC. And the resistance must be chosen according to the application speed of the system in order not to impact the whole application. The main advantage to using an RC filter is to have an anti-aliasing system. The ADC used must certainly have sample and hold conversion in accordance with the RC filter value, in order to let the output recover before sampling.

Figure 38. **RC filter when driving ADC**



In Figure 39 below an R_s = 1.3 kΩ resistance and a C_t = 470 pF capacitance have been set. Given a low pass filter of 260 kHz and a response time of roughly 1.8 µs.

In Figure 40 below an R_s = 1.3 kΩ resistance and a C_t = 470 pF capacitance have been set. A load resistance of 10 kΩ is added in parallel of the C_t capacitance

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Figure 39. Capacitive load response at V_{cc} = 3.3 V with 260 kHz RC filter

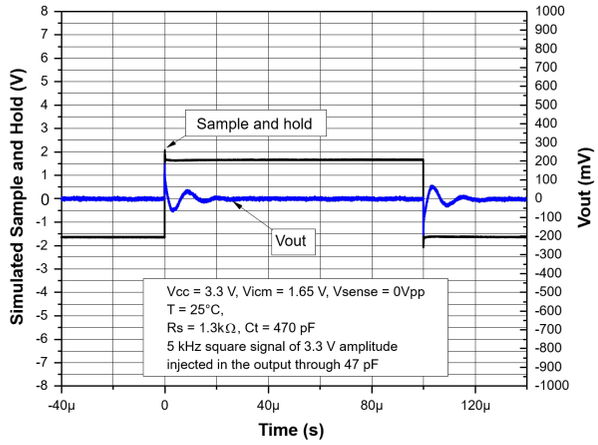
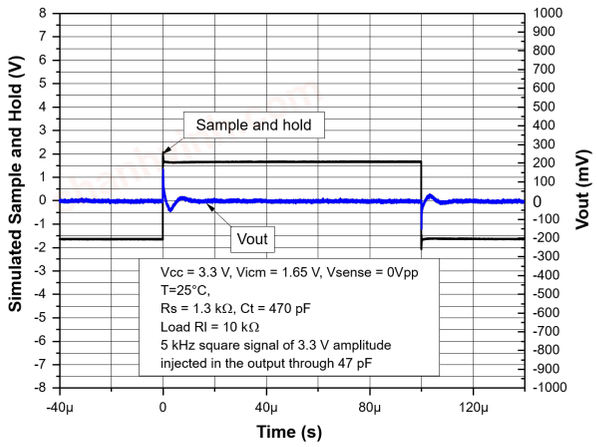


Figure 40. Capacitive load response at V_{cc} = 3.3 V with 260 kHz RC filter and R_l = 10 kΩ



Special care must be also taken on the value of the added external capacitor. Indeed, if this is chosen with an excessive value and the serial resistance with a too small value, there is a risk of instability on the output of the TSC213.

- Driving large capacitive C_{load}

  Increasing the load capacitance produces gain peaking in the frequency response, with overshoot and ringing in the step response.

  Figure 41 shows the serial resistors that must be added to the output, to make a system stable.

  Figure 42 shows that the stability of the TSC213 can be improved when a load of 10k is added on the output in order to source a small current.

Figure 41. Stability criteria with a serial resistor at V_{cc} = 5 V

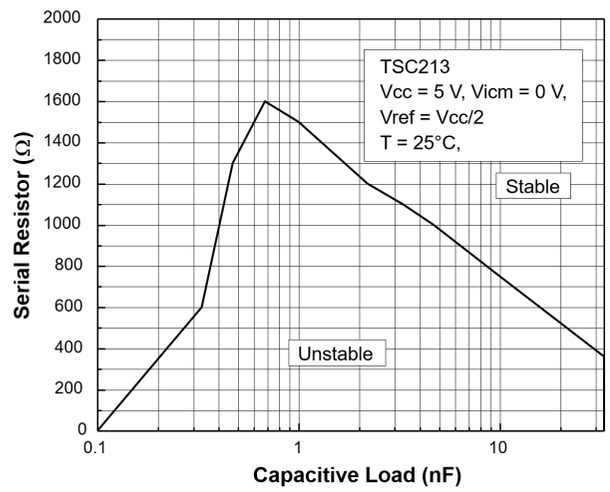
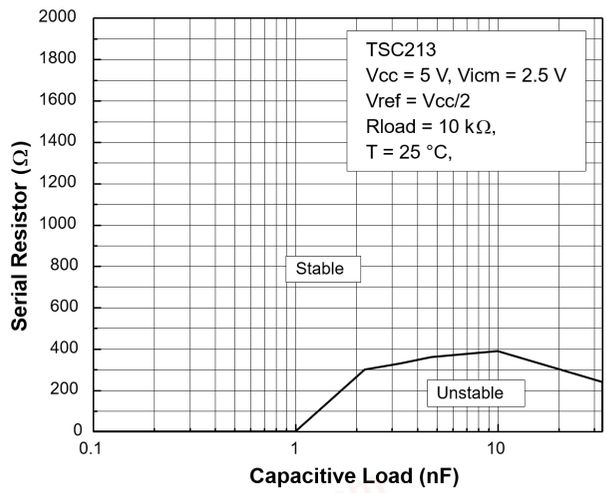


Figure 42. Stability criteria with a serial resistor and a R_{load} = 10 kΩ at V_{cc} = 5 V



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6.8 Improving precision

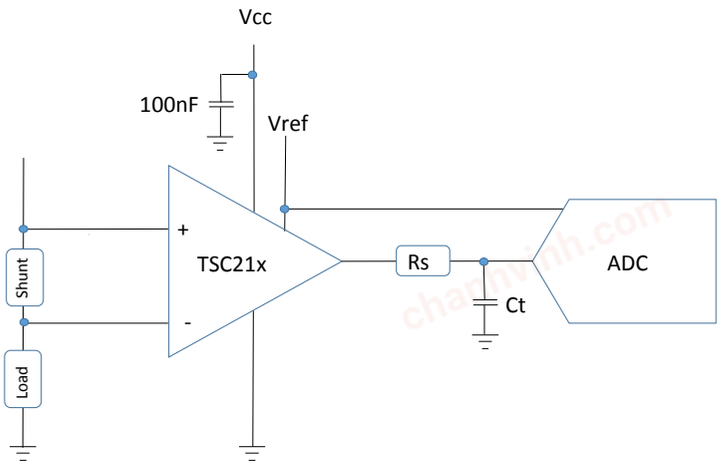
If the TSC21x series current sensing is used with an ADC, it can be interesting to sense the output and the reference voltage applied on the Ref pin in a differential way as depicted in Figure 43.

There are least two benefits to realizing the measurement in this way.

Firstly, in case of the output common voltage being fixed thanks to the ref pin, done only with a resistor divider, without any buffer, it can cancel the effect of this external impedance.

And secondly, it cancels the imprecision of the voltage reference source as well, as it serves as reference also for the ADC.

Figure 43. ADC in differential mode



6.9 Power supply recommendation

In order to decouple correctly the TSC21x, it is recommended to place a 100 nF bypass capacitor between V_{cc} and Gnd. This capacitor must be placed as close as possible of the supply pins.

It is also important to take into consideration the V_{ref} pin which is used to fix the output common mode voltage. Effectively this pin must be driven by a low impedance voltage source and can be decoupled thanks to a 10 nF bypass capacitor.

Larger bypass capacitor added on V_{cc} pin and V_{ref} pin should help to enhance CMRR and PSRR performance.

6.10 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the current sensing, load and power supply. It is good practice to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

When using shunt resistance lower than 1 Ω, it is important to use a 4-wire connection technique to sense the current as described in the schematic below. Effectively, this technique allows to separate pairs of current carrying and voltage-sensing electrodes to make more accurate measurements by eliminating the lead and contact resistance from the measurement.

It is also important to treat the track connected to the input pin of the TSC21x as a differential pair; it must have the same length and width, and ideally be placed on the same PCB plane, and above all must be routed as far as possible from noisy source. As this track carries the input bias current, in a range of hundreds of µA, it can be designed small but always by taking care of their resistivity. Any via in these input tracks are non-recommended to avoid any parasitic resistance in this path.

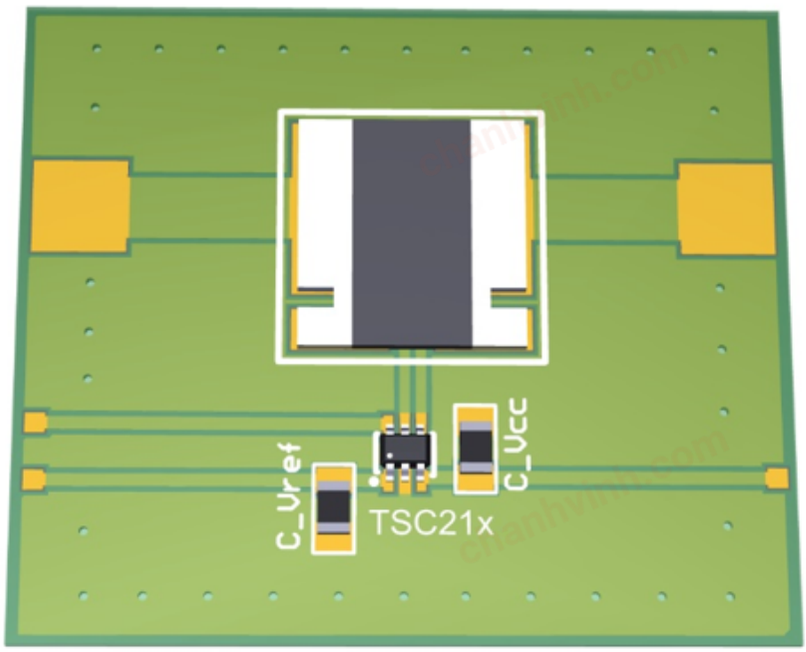
To minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

A ground plane generally helps to reduce EMI, which is why it is generally recommended to use a multi-layer PCB and use the ground planes as a shield to protect the internal track. In this case, pay attention to separate the digital from the analog ground and avoid any ground loop. To further minimize EMI impact, it is important to reduce loop area or antenna.

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Figure 44 suggests a possible routing for the TSC21x, in order to minimize as much as possible parasitic effect.

Figure 44. Recommended layout



6.11 EMI rejection ration (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of a current sensing device. An adverse effect that is common to many current sensings is a change in the offset voltage as a result of RF signal rectification.

A first order internal low pass filter is included on the input of the TSC21x to minimize susceptibility to EMIRR. Figure 45 shows the EMIRR on pin IN+, Figure 46 shows the EMIRR on pin IN- of the TSC21x measured from 10 MHz up to 2.4 GHz.

Figure 45. EMIRR on pin+

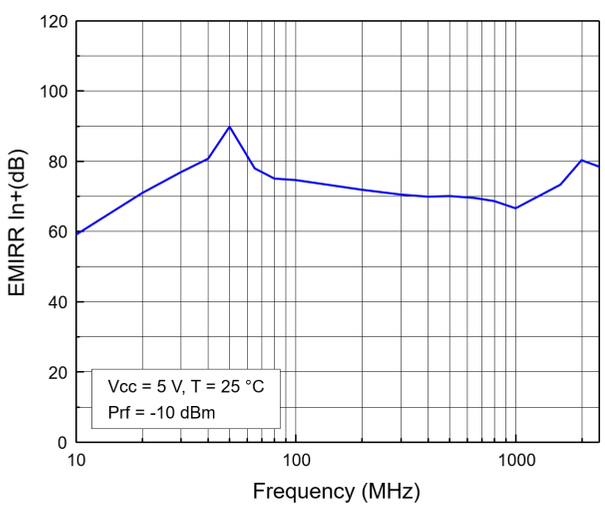
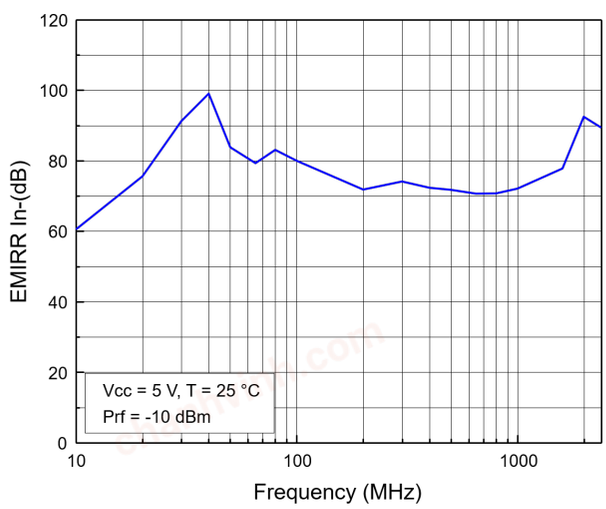


Figure 46. EMIRR on pin-



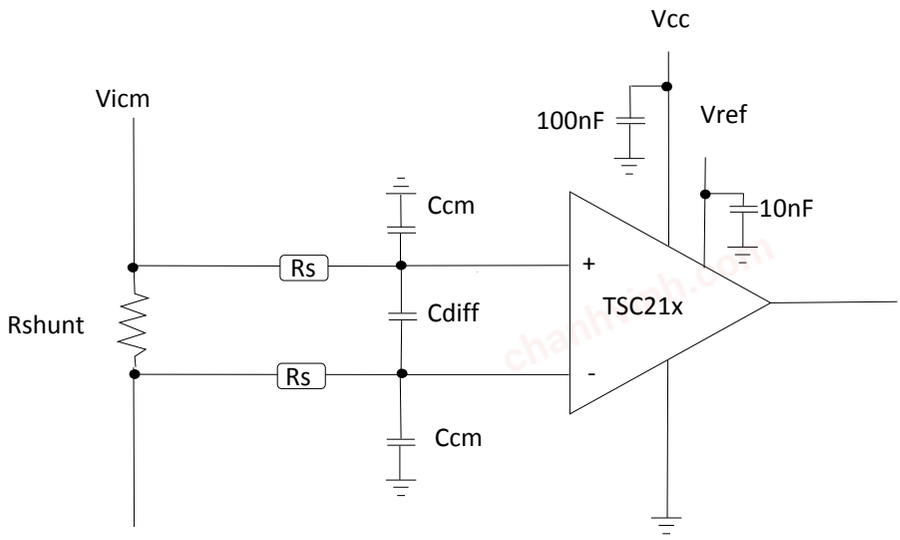
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6.12 Filtering input stage

When a current sensing works in a high frequency noisy environment, it is mandatory to correctly filter the input of the TSC21x device, avoiding any parasitic offset due to the high frequency spikes. Both common mode and differential mode paths must be filtered. The best scenario is to match the capacitance between them to avoid adding differential error on the input of the current sensing.

Otherwise, it is important to combine a common mode filter and a differential mode filter to compensate the mismatch of the capacitance. (Refer to Application note AN4304).

Figure 47. Input filtering



The differential voltage error due to the mismatch of the Ccm capacitance can be written:

$$Vdiff \cong Vin.\frac{Ccm2 - Ccm1}{Rs.\omega 3.\left(2.Cdiff.Ccm1 + Ccm1^2\right)} \quad (9)$$

where ω3 is the input signal frequency.

It is still possible to improve the filtering by increasing the differential capacitance value. The drawback is that the response time increases.

The TSC21x current sensing family have some trimmed input resistance; any external resistance added in series produces mismatches leading to both gain and CMR errors, typically calculated as follows (Rin is the specified amplifier input resistance):

$$Gain\ error\left(\%\right) = 100 - 100.\frac{Rin}{Rin + Rs} \quad (10)$$

$$CMR\ (dB) = 20log.\frac{Rs.(Rs_{error}\%).2}{Rin} \quad (11)$$

The internal resistance of the TSC210 is 5 kΩ. Assuming that an external resistor of 100 Ω, with a tolerance of 1%, is used for filtering, the common mode rejection ratio due to these external components is 68 dB. There is a direct impact on the whole CMR as the TSC210 has a minimum CMR of 105 dB.

The fact that Rs is quite big adds 2%. to the gain error. Therefore, care must be taken when introducing input filters. The only way to control this additional gain error is to ensure that the input series resistor, Rs, is small compared to Rin. Using a filter resistor that is less than 10 Ω is strongly recommended.

This ensures that the high original accuracy of the TSC21x is maintained. Other parameters such as process variation or the temperature coefficient of the resistances must also be taken into consideration as possible error factors of current measurement. The calculation of total error due to external resistances is detailed in the application note AN4369.

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6.13 AMR limitation

In case of important differential input voltage, a high current above the maximum Iin = 5 mA specified in the AMR table may appear on the input pins.

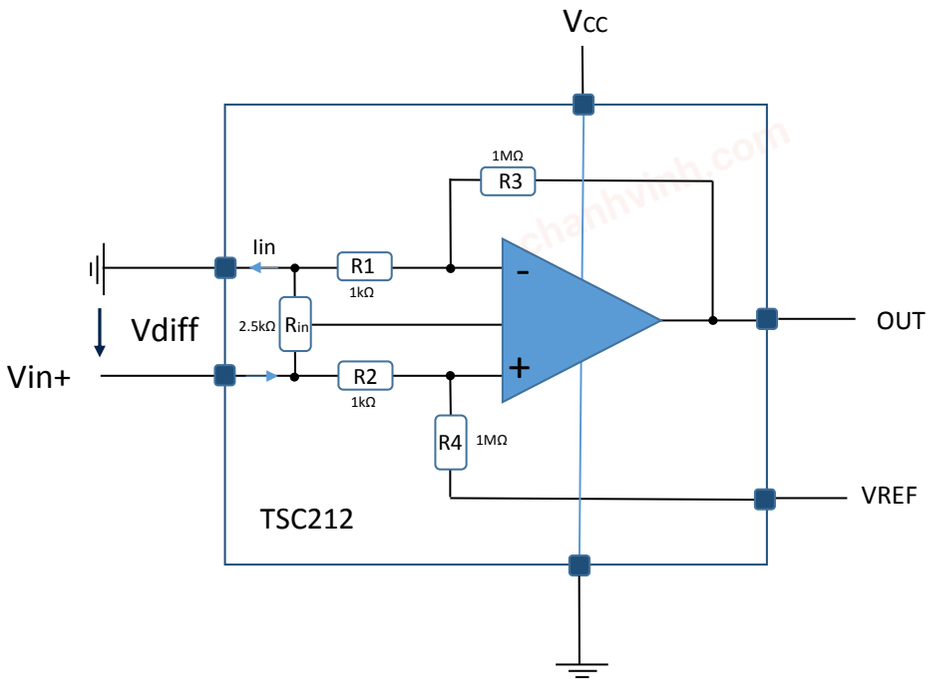
As shown in Figure 48, for example, when using the TSC212 current sensing device, a differential input voltage generates a current thru the input pins defined by:

$$Iin = \frac{Vdiff}{Rin//(R1+R2)} \quad (12)$$

If Vdiff = 26 V, the current Iin can rise, up to 23.4 mA

$$Iin = \frac{26V}{1.1k\Omega} = 23.4mA \quad (13)$$

Figure 48. TSC212 with input differential voltage



Therefore, to avoid silicon damage, the input current must be limited to 5 mA.

The differential input voltages should be limited to:

- Vdiff = +/- 10 V for the TSC210
- Vdiff = +/- 7.7 V for the TSC211
- Vdiff = +/- 5.6 V for the TSC212
- Vdiff = +/- 11.8 V for the TSC213
- Vdiff = +/- 11.1 V for the TSC214
- Vdiff = +/- 11.4 V for the TSC215

To match this requirement a serial resistance can be used, but precision would be affected, see Section 6.12 Filtering input stage.

Alternative methods can be the use of Zener diode or even application restriction.

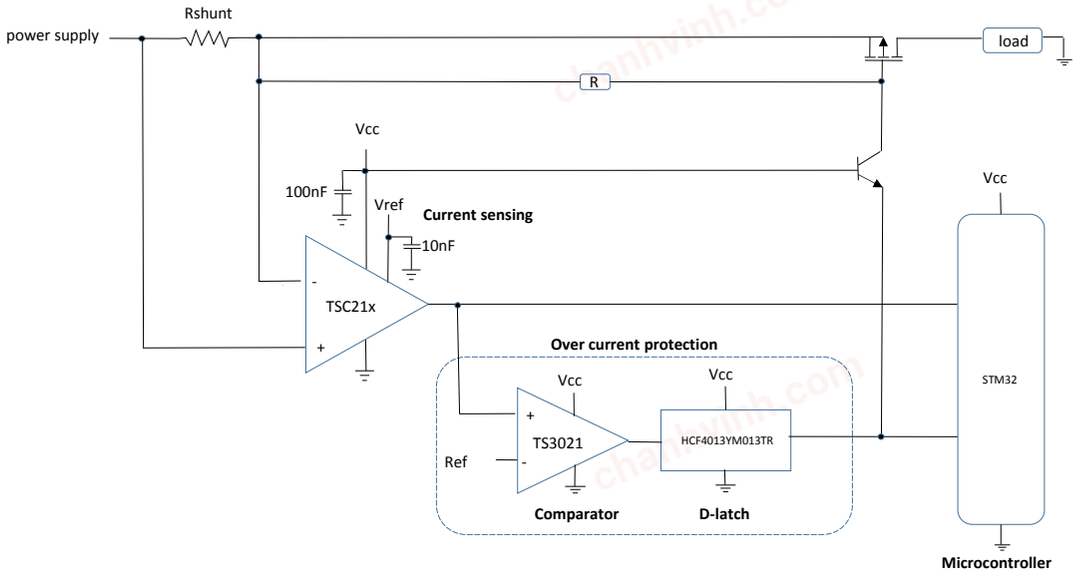
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6.14 Application example

Power supply monitoring and OCP function.

The TSC21x is used to sense the current into the load, and thus in both directions, in a very accurate way.

Figure 49. Power supply monitoring and OCP function



When a short-circuit or overcurrent occurs, the application must be switched off as quickly as possible. And moreover, after such event, the application must not restart by itself and must stay switched off until a manual reload is applied. The TS3021 is a high speed comparator, which combined with D flip-flop HCF4013, is used to realize a latch function in case of an overcurrent event.

In case of overcurrent, the output of the current sensing rises above the Ref voltage and so the output of the comparator changes from a low state to a high state.

This information is directly latched because of the D flip-flop HCF4013. And after such an event, the output of the HCF4013 ($\overline{Q1}$) changes from high state to a low state.

The ($\overline{Q1}$) is also supervised by a GPIO of the MCU, which can be informed in case of an overcurrent event.

To restart the application and un-latch the D flip-flop, a clock signal must be applied on pin CLOCK1 of the HCF4013.

A first approach calculation by considering a Vcc voltage at 3.3 V.

The current sensing TSC213 has a slew rate of 0.85 V/µs. After an overcurrent event, its output is saturated and may rise up to its maximum output voltage, here 3.3 V. If we consider the worst case the output of the TSC213 is close to 0 V, the current sensing would need 3.9 µs to pass from 0 V to 3.3 V, after the overcurrent event.

The comparator TS3021 is a high speed comparator with a propagation delay T_{PLH} of 75 ns max. to change its state from low to high.

The D flip-flop has a propagation delay T_{PHL} of 400 ns to change its state from high to low.

So after an overcurrent, the system takes, in worst condition, less than 4.4 µs to switch off the power (extra margin should be taken considering that the propagation delay of the comparator depends on the overdrive).

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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SC70-6 package information

Figure 50. SC70-6 package outline

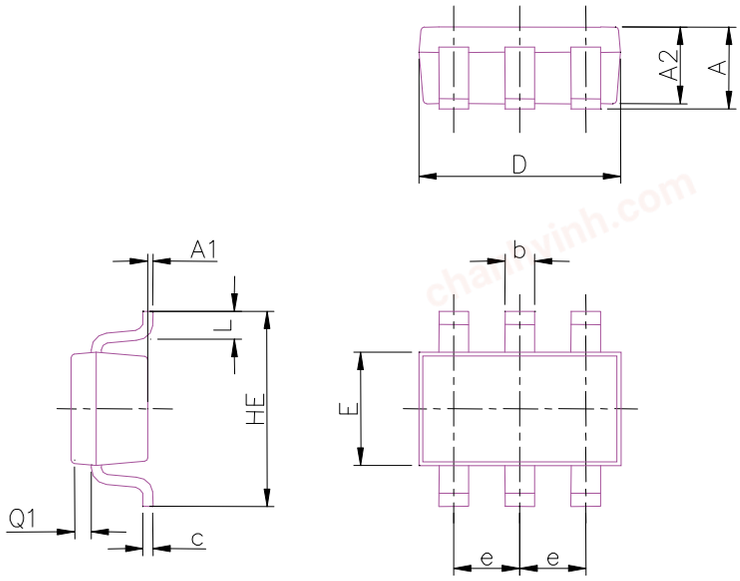


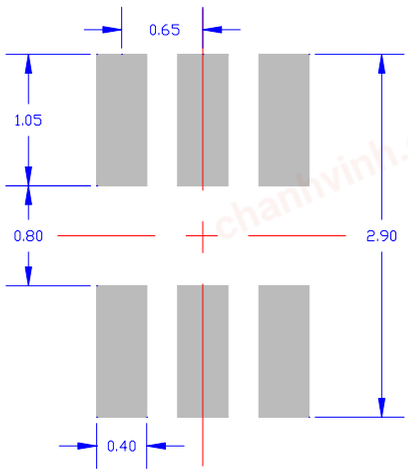
Table 7. SC70-6 mechanical data

Symbol	Milimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.037		0.041
A1	0		0.10	0.000		0.004
A2	0.80		1.00	0.035		0.039
b	0.15		0.30	0.008		0.010
c	0.10		0.18	0.004		0.004
D	1.80		2.20	0.078		0.086
E	1.15		1.35	0.050		0.052
e		0.65		0.025		0.026
HE	1.8		2.4	0.083		0.090
L	0.10		0.40	0.013		0.015
Q1	0.10		0.40	0.011		0.013

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

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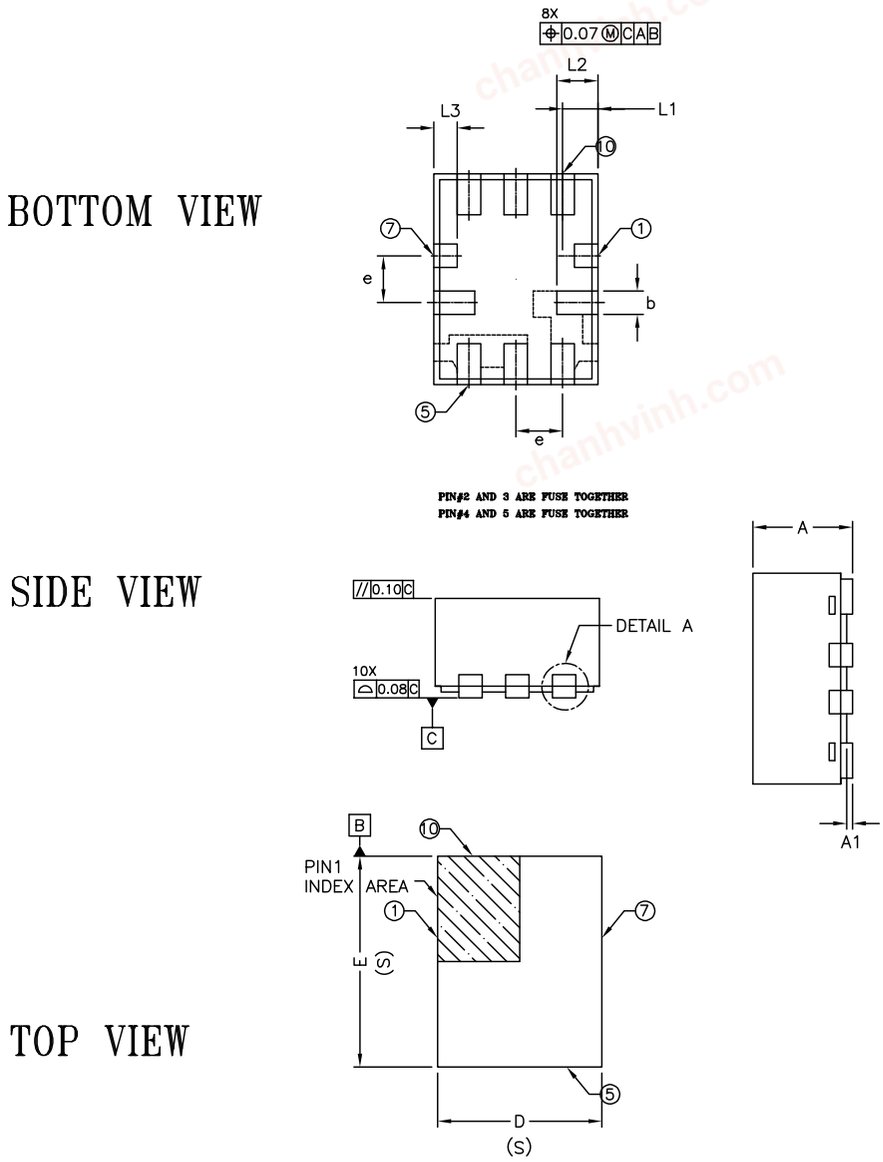
Figure 51. **SC70-6 recommended footprint**



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7.2 QFN10 package information

Figure 52. **QFN10 package outline**



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Figure 53. **QFN10 detail A package outline**

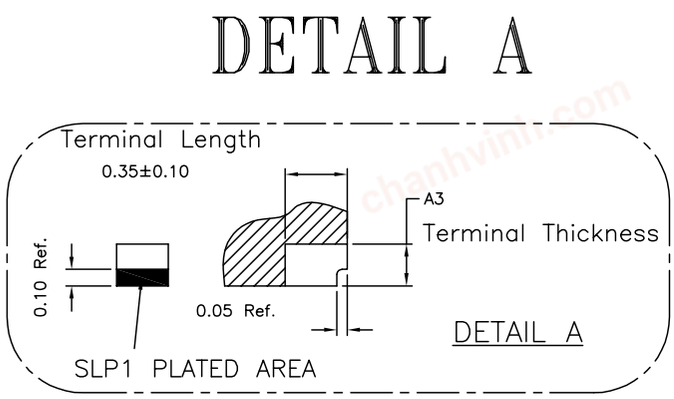
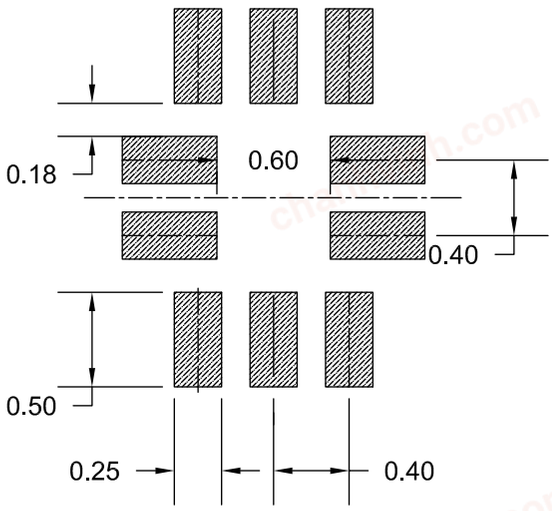


Table 8. **QFN10 mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.0		0.05
A3		0.203REF	
b	0.15	0.20	0.25
D	1.35	1.40	1.45
e		0.40 BSC	
E	1.75	1.80	1.85
L1	0.10	0.20	0.30
L2	0.25	0.35	0.45
L3	0.10	0.20	0.30

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Figure 54. **QFN10 recommended footprint**



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8 Ordering information

Table 9. **Ordering information**

Order code	Gain (V/V)	Temperature range	Package	Packing	Marking
TSC210ICT	200	-40°C to 125°C	SC70-6	Tape and reel	O10
TSC210IYCT(1)					O16
TSC210IQT			QFN10		O10
TSC210IYQT(1)					O16
TSC211ICT	500		SC70-6		O11
TSC211IYCT(1)					O17
TSC211IQT			QFN10		O11
TSC211IYQT(1)					O17
TSC212ICT	1000		SC70-6		O12
TSC212IYCT(1)					O18
TSC212IQT			QFN10		O12
TSC212IYQT(1)					O18
TSC213ICT	50		SC70-6		O13
TSC213IYCT(1)					O19
TSC213IQT			QFN10		O13
TSC213IYQT(1)					O19
TSC214ICT	100		SC70-6		O14
TSC214IYCT(1)					O1A
TSC214IQT			QFN10		O14
TSC214IYQT(1)					O1A
TSC215ICT	75		SC70-6		O15
TSC215IYCT(1)					O1B
TSC215IQT			QFN10		O15
TSC215IYQT(1)					O1B

1. *Qualified and characterized according to the AEC Q100 and Q003 or equivalent, advanced screening according to the AEC Q001 and Q002 or equivalent.*

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Revision history

Table 10. **Document revision history**

Date	Version	Changes
13-Feb-2020	1	Initial release.
27-Feb-2020	2	Update features in cover page and Section 4 Electrical characteristics.
24-Nov-2020	3	Added the part numbers: TSC211, TSC214 and TSC215. Updated cover page. Updated Table 2. Resistors and gain values, Section 4 Electrical characteristics and Section 7 Ordering information.
29-Mar-2021	4	Updated Table 3. Absolute maximum ratings and Section 4 Electrical characteristics.
02-Aug-2021	5	Updated Figure 7 and Figure 20. Added new Section 6 Application information.
06-Sep-02	6	Updated Figure 52. QFN10 package outline Updated Figure 53. QFN10 detail A package outline Updated Table 8. QFN10 mechanical data

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Contents

1 Pin connections and description 2
2 Block diagram 3
3 Absolute maximum ratings and operating conditions 4
4 Electrical characteristics 5
5 Typical characteristics 7
6 Application information 12
6.1 Overview 12
6.2 Theory of operation 12
6.3 Unidirectionnal / bidirectionnal operation 14
6.4 R_{SENSE} selection 15
6.5 Input offset voltage drift overtemperature 16
6.6 Error calculation 16
6.7 Stability 19
6.8 Improving precision 22
6.9 Power supply recommendation 22
6.10 PCB layout recommendations 22
6.11 EMI rejection ration (EMIRR) 23
6.12 Filtering input stage 24
6.13 AMR limitation 25
6.14 Application example 26
7 Package information 27
7.1 SC70-6 package information 27
7.2 QFN10 package information 29
8 Ordering information 32
Revision history 33

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List of tables

Table 1. Pin description . . . 2
Table 2. Resistors and gain values . . . 3
Table 3. Absolute maximum ratings . . . 4
Table 4. Operating conditions . . . 4
Table 5. Electrical characteristics, T = 25 °C, V_{SENSE} = V_{IN+}- V_{IN-} (unless otherwise specified), TSC210, TSC213, TSC214, TSC215: V_{CC}= 5 V, V_{IN+}=12 V, V_{REF}= V_{CC}/2 (unless otherwise specified), TSC211, TSC212: V_{CC} = 12 V, V_{IN+} = 12 V, V_{REF} = V_{CC}/2 (unless otherwise specified) . . . 5
Table 6. Gain error . . . 18
Table 7. SC70-6 mechanical data . . . 27
Table 8. QFN10 mechanical data . . . 30
Table 9. Ordering information . . . 32
Table 10. Document revision history . . . 33

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List of figures

Figure 1. Pin connections (top view) . . . 2
Figure 2. Block diagram . . . 3
Figure 3. Input offset voltage production distribution . . . 7
Figure 4. Input offset voltage vs. temperature . . . 7
Figure 5. Common-mode rejection ratio production distribution . . . 7
Figure 6. Common mode rejection ratio vs. temperature . . . 7
Figure 7. Gain vs. frequency . . . 8
Figure 8. Power supply rejection ratio vs. frequency . . . 8
Figure 9. Common mode rejection ratio vs. frequency . . . 8
Figure 10. Positive output voltage swing vs. output current V_{CC} = 2.7 V . . . 8
Figure 11. Negative output voltage swing vs. output current V_{CC} = 2.7 V . . . 8
Figure 12. Positive output voltage swing vs. output current V_{CC} = 5 V . . . 8
Figure 13. Negative output voltage swing vs. output current V_{CC} = 5 V . . . 9
Figure 14. Positive output voltage swing vs. output current V_{CC} = 26 V . . . 9
Figure 15. Negative output voltage swing vs. output current V_{CC} = 26 V . . . 9
Figure 16. Input bias current vs. input common mode voltage with supply voltage = 5 V . . . 9
Figure 17. Input bias current vs. input common mode voltage with supply voltage = 0 V . . . 9
Figure 18. Input bias current vs. temperature . . . 9
Figure 19. Quiescent current vs. temperature . . . 10
Figure 20. Input referred noise vs. frequency . . . 10
Figure 21. 0.1 Hz to 10 Hz voltage noise (referred to input) . . . 10
Figure 22. Step response (10-mVpp input step) . . . 10
Figure 23. Common mode voltage transient response . . . 10
Figure 24. Inverting differential input overloaded . . . 10
Figure 25. Non inverting differential input overload . . . 11
Figure 26. Start-up response . . . 11
Figure 27. Brownout recovery . . . 11
Figure 28. Power supply when V_{icm} > 2.5 V . . . 12
Figure 29. Input bias current vs. common mode voltage V_{cc} = 5 V . . . 13
Figure 30. V_{ref} powered by an external voltage source with a TSC210 . . . 13
Figure 31. Output reference to ground . . . 14
Figure 32. Output reference to V_{cc} . . . 14
Figure 33. External supply . . . 15
Figure 34. Shunt resistor value trade-off (TSC213) . . . 16
Figure 35. Input current . . . 18
Figure 36. Capacitive load response at V_{cc} = 3.3 V . . . 19
Figure 37. Capacitive load response at V_{cc} = 3.3 V with a step of 100 mV . . . 20
Figure 38. RC filter when driving ADC . . . 20
Figure 39. Capacitive load response at V_{cc} = 3.3 V with 260 kHz RC filter . . . 21
Figure 40. Capacitive load response at V_{cc} = 3.3 V with 260 kHz RC filter and R_l = 10 kΩ . . . 21
Figure 41. Stability criteria with a serial resistor at V_{cc} = 5 V . . . 21
Figure 42. Stability criteria with a serial resistor and a R_{load} = 10 kΩ at V_{cc} = 5 V . . . 21
Figure 43. ADC in differential mode . . . 22
Figure 44. Recommended layout . . . 23
Figure 45. EMIRR on pin+ . . . 23
Figure 46. EMIRR on pin- . . . 23
Figure 47. Input filtering . . . 24
Figure 48. TSC212 with input differential voltage . . . 25
Figure 49. Power supply monitoring and OCP function . . . 26
Figure 50. SC70-6 package outline . . . 27
Figure 51. SC70-6 recommended footprint . . . 28

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Figure 52. QFN10 package outline 29
Figure 53. QFN10 detail A package outline 30
Figure 54. QFN10 recommended footprint 31

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