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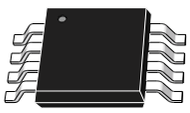
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TSB7191, TSB7191A
TSB7192, TSB7192A

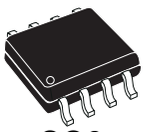
Datasheet

Precision rail-to-rail input / output 36 V, 22 MHz op-amps

TSB7192 and TSB7192A

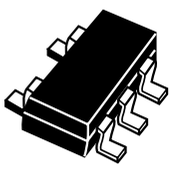


MiniSO8



SO8

TSB7191 and TSB7191A



SOT23-5

Product status link
TSB7191, TSB7191A, TSB7192, TSB7192A

Related products	
TSB572	Dual op-amps for the low-power consumption version (380 µA with 2.5 MHz GBP)
TSB712	Precision rail-to-rail input / output 36 V, 6 MHz dual op-amps
TSB712A	

Features

- Rail-to-rail input and output
- Low offset voltage: 300 µV maximum
- Wide supply voltage range: 2.7 V to 36 V
- Gain bandwidth product: 22 MHz
- Slew rate: 12 V/µs
- Low noise: 12 nV/√Hz
- Stable with gain +10/-9
- Integrated EMI filter
- 2 kV HBM ESD tolerance
- Extended temperature range: -40 °C to +125 °C
- Automotive-grade available

Applications

- High-side and low-side current sensing
- Hall effect sensors
- Data acquisition and instrumentation
- Test and measurement equipments
- Motor control
- Industrial process control
- Strain gauge

Description

The TSB7191, TSB7191A, TSB7192 and the TSB7192A 22 MHz bandwidth amplifier feature rail-to-rail input and output, which is guaranteed to operate from +2.7 V to +36 V single supply as well as from ±1.35 V to ±18 V dual supplies.

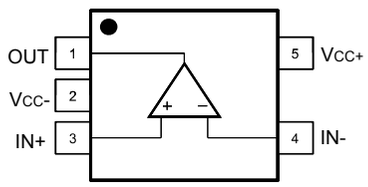
These amplifiers have the advantage of offering a large span of supply voltage and an excellent input offset voltage of 300 µV maximum at 25 °C.

The combination of wide bandwidth, slew rate, low noise, rail-to-rail capability and precision makes the TSB7191, TSB7191A, TSB7192 and the TSB7192A useful in a wide variety of applications such as: filters, power supply and motor control, actuator driving, hall effect sensors and resistive transducers.

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1 Pin description

Figure 1. Pin connections (top view)

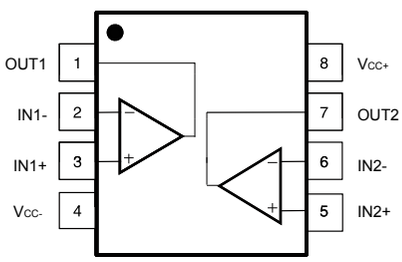


SOT23-5

Table 1. Pin description (SOT23-5)

Pin n°	Pin name	Description
1	OUT	Output channel
2	V_{CC-}	Negative supply voltage
3	IN1+	Non-inverting input channel
4	IN-	Inverting input channel
5	V_{CC+}	Positive supply voltage

Figure 2. Pin connections (top view)



MiniSO8/SO8

Table 2. Pin description (MiniSO8/SO8)

Pin n°	Pin name	Description
1	OUT1	Output channel 1
2	IN1-	Inverting input channel 1
3	IN1+	Non-inverting input channel 1
4	V_{CC-}	Negative supply voltage
5	IN2+	Non-inverting input channel 2
6	IN2-	Inverting input channel 2
7	OUT2	Output channel 2
8	V_{CC+}	Positive supply voltage

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2 Absolute maximum ratings and operating conditions

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	+40 or ±20	V
V_{id}	Input voltage differential (2)	±2	V
V_{in}	Input voltage	(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	V
I_{in}	Input current (3)	±10	mA
	Storage temperature	-65 to +150	°C
R_{th-ja}	Thermal resistance junction-to-ambient (4) (5)		°C / W
	MiniSO-8	190	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model (6)	2	kV
	CDM: charged device model (7)	1	kV
	Latch-up immunity	100	mA

1. *All voltage values, except the differential voltage are with respect to the network ground terminal.*
2. *Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. The maximum input voltage differential value may be extended to the condition that the input current is limited to ±10 mA. See Input pin voltage range.*
3. *Input current must be limited by a resistor in series with the inputs when the input voltage is beyond the rails (see Input pin voltage range).*
4. *Short-circuits can cause excessive heating and destructive dissipation.*
5. *R_{th} are typical values.*
6. *Human body according to JEDEC standard JESD22-A114F.*
7. *According to ANSI/ESD STM5.3.1.*

Table 4. Operating conditions

Symbol	Parameter	Value
V_{CC}	Supply voltage	2.7 V to 36 V
V_{icm}	Common mode input voltage range	(V_{CC-}) to (V_{CC+}) + 0.1 V
T_{oper}	Operating free air temperature range	-40 °C to +125 °C

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3 Electrical characteristics

Table 5. Electrical characteristics at V_{CC} = 36 V, V_{ICM} = V_{OUT} = V_{CC} / 2, T_{amb} = 25 °C and R_L connected to V_{CC} / 2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	TSB7191A, TSB7192A, T = 25 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$ -1.5 V			± 300	µV
		TSB7191A, TSB7192A, T = 25 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$			± 650	
		TSB7191A, TSB7192A, -40 °C < T < 125 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$ -1.5 V			± 580	
		TSB7191A, TSB7192A, -40 °C < T < 125 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$			± 930	
		TSB7191, TSB7192, T = 25 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$ -1.5 V			± 800	
		TSB7191, TSB7192, T = 25 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$			± 1200	
		TSB7191, TSB7192, -40 °C < T < 125 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$ -1.5 V			± 1100	
		TSB7191, TSB7192, -40 °C < T < 125 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$			± 1400	
ΔV_{io} / ΔT	Input offset voltage drift	-40 °C < T < 125 °C (1)			2.8	µV/°C
ΔV_{io}	Long-term input offset voltage drift	T = 25 °C (2)		0.57		µV/√mo
I_{IB}	Input bias current (3)	$V_{ICM} = V_{CC+}$, T = 25 °C	0		300	nA
		$V_{ICM} = V_{CC+}$, -40 °C < T < 125 °C	0		900	
		$V_{ICM} = V_{CC-}$, T = 25 °C	-100		0	
		$V_{ICM} = V_{CC-}$, -40 °C < T < 125 °C	-200		0	
I_{IO}	Input offset current(4)	$V_{ICM} = V_{CC+}$		10		
		$V_{ICM} = V_{CC-}$		10		

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
A_{VD}	Open loop gain	R_L ≥ 10 kΩ, (V_{CC-}) + 0.5 V ≤ V_{OUT} ≤ (V_{CC+}) -0.5 V, T = 25 °C	110	125		dB
		R_L ≥ 10 kΩ, (V_{CC-}) + 0.5 V ≤ V_{OUT} ≤ (V_{CC+}) -0.5 V, -40 °C < T < 125 °C	105			
CMR	Common-mode rejection ratio 20 log (ΔV_{INCM} / ΔV_{IO})	(V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}) - 1.5 V, T = 25 °C	115	130		
		(V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}) - 1.5 V, -40 °C < T < 125 °C	110			
		TSB7191A, TSB7192A (V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}), T = 25 °C	100	120		
		TSB7191A, TSB7192A (V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}), -40 °C < T < 125 °C	95			
		TSB7191, TSB7192 (V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}), T = 25 °C	90	120		
		TSB7191, TSB7192 (V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}), -40 °C < T < 125 °C	85			
SVR	Power supply rejection ratio 20 log (ΔV_{CC} / ΔV_{IO})	5 V < V_{CC} < 36 V, V_{ICM} = V_{CC}/2 -40 °C < T < 125 °C	100	125		
V_{OH}	High level output voltage (drop voltage from V_{CC+})	No load, -40 °C < T < 125 °C			120	mV
		I_{SOURCE} = 2 mA, -40 °C < T < 125 °C			200	
		I_{SOURCE} = 15 mA, -40 °C < T < 125 °C			1000	
V_{OL}	Low level output voltage	No load , -40 °C < T < 125 °C			120	
		I_{SINK} = 2 mA, -40 °C < T < 125 °C			200	
		I_{SINK} = 15 mA , -40 °C < T < 125 °C			1000	
I_{OUT}	I_{SINK}	V_{OUT} = V_{CC}, T = 25 °C	25	50		mA
		V_{OUT} = V_{CC}, -40 °C < T < 125 °C	20			
	I_{SOURCE}	V_{OUT} = 0 V, T = 25 °C	25	50		
		V_{OUT} = 0 V, -40 °C < T < 125 °C	20			
I_{CC}	Supply current by op-amp	No load, T = 25 °C		1.8		mA
		No load, -40 °C < T < 125 °C			3	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	16	22		MHz

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
A_{stab}	Minimum gain for stability	No sustained oscillations. Positive gain configuration: V_{cc}- < V_{icm} < V_{cc}+ + 0.1 V, -40 °C < T < 125 °C		10		V/V
		No sustained oscillations. Negative gain configuration. V_{cc}- < V_{icm} < V_{cc}+ + 0.1 V , -40 °C < T < 125 °C		-9		
SR	Slew rate	9 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = 1 V/V, 10% to 90%	8.5	12		V/µs
THD+N	Total harmonic distorsion + noise	V_{IN} = 0.1 Vrms , R_L = 10 kΩ, A_V = +1, f = 1 kHz, BW = 22 kHz		0.0022		%
		V_{IN} = 0.1 Vrms , R_L = 1 kΩ, A_V = +1, f = 1 kHz, BW = 22 kHz		0.0022		
CR	Crosstalk	V_{OUT} = 5 Vpp, f = 1 kHz, A_V = +11, R_L = 10 kΩ		125		dB
		V_{OUT} = 5Vpp, f = 10 kHz, A_V = +11, R_L = 10 kΩ		100		
Φm	Phase margin	At gain= +10, 25 °C, 10 kΩ, 100 pF		68		°
C_{LOAD}	Capacitive load drive			100(5)		pF
e_n	Input voltage noise density	f = 10 Hz		20		nV/√Hz
		f = 100 Hz		13		
		f = 10 kHz		12		
$e_{n\ p-p}$	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		0.5		$µV_{PP}$
i_n	Input current noise density	f = 1 kHz		0.15(6)		pA/√Hz

1. *See Input offset voltage drift over the temperature in application information.*
2. *Typical value is based on the V_{IO} drift observed after 1000 h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See Long term input offset voltage drift.*
3. *Current is positive when it is sinked into the op-amp.*
4. *I_{io} is defined as $|I_{ibp} – I_{ibn}|$*
5. *For higher capacitive values see Figure 24. Phase margin vs. output current at V_{CC} = 36 V and Figure 25. Phase margin vs. capacitive load*
6. *Theoretical value of the input current noise density based on the measurement of the input transistor base current:* $i_n = \sqrt{2.q.i_b}$

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Table 6. Electrical characteristics at V_{CC} = 5 V, V_{ICM} = V_{OUT} = V_{CC} / 2, T_{amb} = 25 °C and R_L connected to V_{CC} / 2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	TSB7191A, TSB7192A, T = 25 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$ -1.5 V			± 350	µV
		TSB7191A, TSB7192A, T = 25 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$			± 650	
		TSB7191A, TSB7192A, -40 °C < T < 125 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$ -1.5 V			± 750	
		TSB7191A, TSB7192A, -40 °C < T < 125 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$			± 1050	
		TSB7191, TSB7192, T = 25 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$ -1.5 V			±800	
		TSB7191, TSB7192, T = 25 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$			±1200	
		TSB7191, TSB7192, -40 °C < T < 125 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$ -1.5 V			±1100	
		TSB7191, TSB7192, -40 °C < T < 125 °C, $V_{CC-} \le V_{ICM} \le V_{CC+}$			±1400	
ΔV_{io} / ΔT	Input offset voltage drift	-40°C < T < 125 °C[1]			4	µV/°C
I_{IB}	Input bias current [2]	$V_{ICM} = V_{CC+}$, T = 25 °C	0		300	nA
		$V_{ICM} = V_{CC+}$, -40 °C < T < 125 °C	0		900	
		$V_{ICM} = V_{CC-}$, T = 25 °C	-100		0	
		$V_{ICM} = V_{CC-}$, -40 °C < T < 125 °C	-200		0	
I_{IO}	Input offset current [3]	$V_{ICM} = V_{CC+}$		10		
		$V_{ICM} = V_{CC-}$		10		

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
A_{VD}	Open loop gain	R_L ≥ 10 kΩ, (V_{CC-}) + 0.5 V ≤ V_{OUT} ≤ (V_{CC+}) -0.5 V, T = 25 °C	105	120		dB
		R_L ≥ 10 kΩ, (V_{CC-}) + 0.5 V ≤ V_{OUT} ≤ (V_{CC+}) -0.5 V, -40 °C < T < 125 °C	100			
CMR	Common-mode rejection ratio 20 log ($\Delta V_{INCM}/\Delta V_{IO}$)	(V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}) -1.5 V, T = 25 °C	95	125		
		(V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}) - 1.5 V, -40 °C < T < 125 °C	90			
		TSB7191A,TSB7192A (V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}), T = 25 °C	80	105		
		TSB7191A, TSB7192A (V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}), -40 °C < T < 125 °C	75			
		TSB7191, TSB7192 (V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}), T = 25 °C	75	105		
		TSB7191, TSB7192 (V_{CC-}) ≤ V_{ICM} ≤ (V_{CC+}), -40 °C < T < 125 °C	70			
V_{OH}	High level output voltage (drop voltage from V_{CC+})	No load, -40 °C < T < 125 °C			90	mV
		I_{SOURCE} = 2 mA, -40 °C < T < 125 °C			200	
V_{OL}	Low level output voltage	No load, -40 °C < T < 125 °C			90	
		I_{SINK} = 2 mA, -40 °C < T < 125 °C			200	
I_{OUT}	I_{SINK}	V_{OUT} = V_{CC}, T = 25 °C	20	50		mA
		V_{OUT} = V_{CC}, -40 °C < T < 125 °C	15			
	I_{SOURCE}	V_{OUT} = 0 V, T = 25 °C	20	50		
		V_{OUT} = 0 V, -40 °C < T < 125 °C	15			
I_{CC}	Supply current by op-amp	No load, T = 25 °C		1.4		mA
		No load, -40 °C < T < 125 °C			2.3	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	16	22		MHz
A_{stab}	Minimum gain for stability	No sustained oscillations. Positive gain configuration: V_{cc-} < V_{icm} < V_{cc}+ + 0.1 V, -40 °C < T < 125 °C		10		V/V
		No sustained oscillations. Negative gain configuration. V_{cc-} < V_{icm} < V_{cc}+ + 0.1 V, -40 °C < T < 125 °C		-9		

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew rate	3 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = 1 V/V, 10% to 90%	7.5	11		V/µs
THD+N	Total harmonic distorsion + noise	V_{IN} = 0.1 Vrms , R_L = 10 kΩ, A_V = +1, f = 1 kHz, BW = 22 kHz		0.0022		%
		V_{IN} = 0.1 Vrms , R_L = 1 kΩ, A_V = +1, f = 1 kHz, BW = 22 kHz		0.0024		
Φm	Phase margin	At gain = +10, 25 °C, 10 kΩ, 100 pF		63		°
C_{LOAD}	Capacitive load drive			100(4)		pF
e_n	Input voltage noise density	f = 10 Hz		20		nV/√Hz
		f = 100 Hz		13		
		f = 10 kHz		12		
$e_{n\ p\text{-}p}$	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		0.8		$µV_{PP}$
i_n	Input current noise density	f = 1 kHz		0.15(5)		pA/√Hz

1. *See Input offset voltage drift over the temperature in application information.*
2. *Current is positive when it is sinked into the op-amp.*
3. *I_{io} is defined as $|I_{ibp} - I_{ibn}|$.*
4. *For higher capacitive values see Figure 23. Phase margin vs. output current at V_{CC} = 5 V and Figure 25. Phase margin vs. capacitive load*
5. *Theoretical value of the input current noise density based on the measurement of the input transistor base current:* $i_n = \sqrt{2.q.i_b}$

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4 Typical performance characteristics

R_L connected to V_{CC} / 2 (unless otherwise specified).

Figure 3. Supply current vs. supply voltage

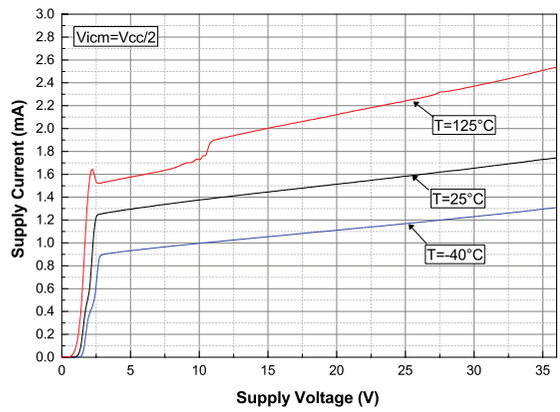


Figure 4. Input offset voltage distribution at V_{CC} = 5 V TSB7191A, TSB7192A

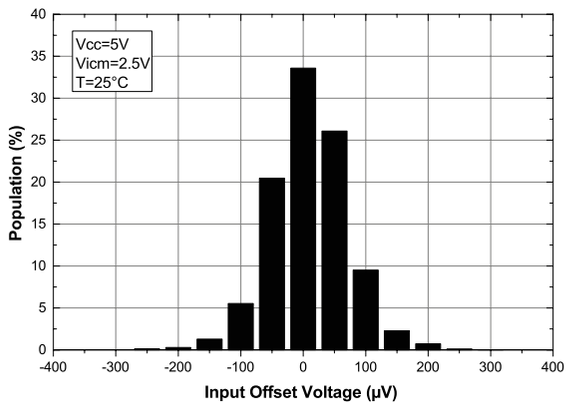


Figure 5. Input offset voltage distribution at V_{CC} = 36 V TSB7191A, TSB7192A

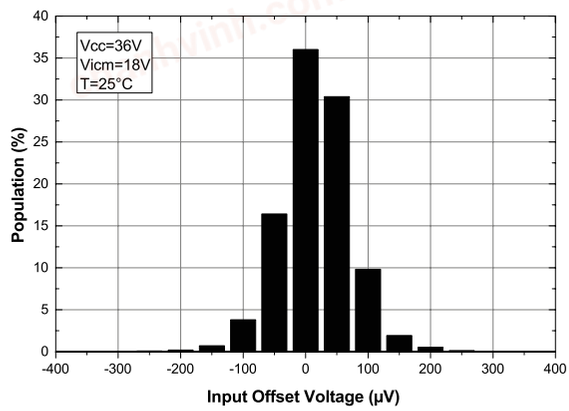
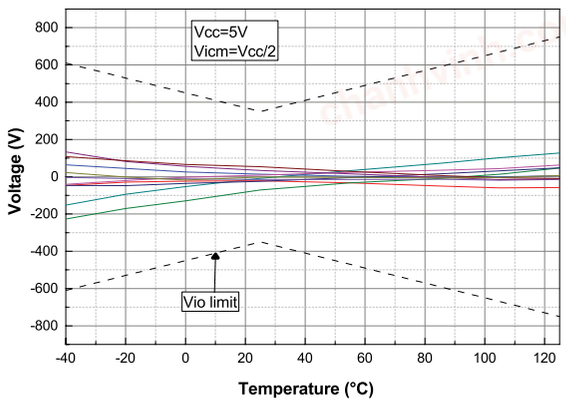


Figure 6. Input offset voltage vs. temperature at V_{CC} = 5 V



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Figure 7. Input offset voltage vs. temperature at V_{CC} = 36 V

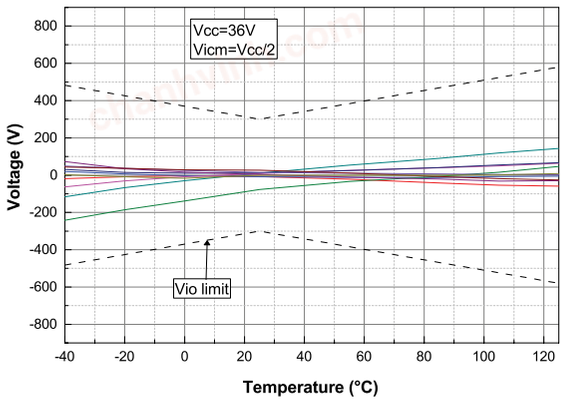


Figure 8. Input offset voltage thermal coefficient distribution at V_{CC} = 5 V

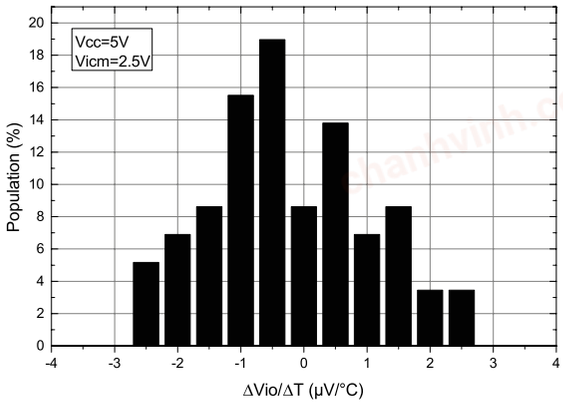


Figure 9. Input offset voltage vs. supply voltage

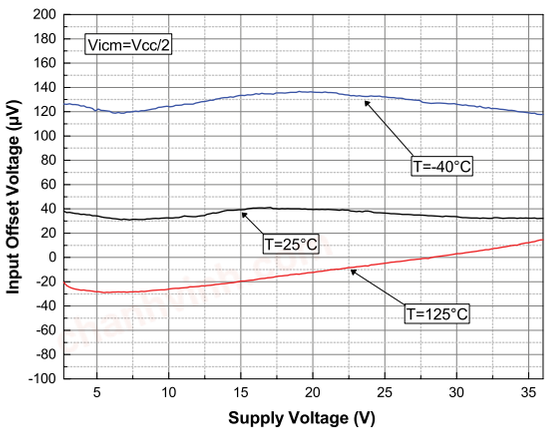


Figure 10. Input offset voltage vs. common mode voltage at V_{CC} = 5 V

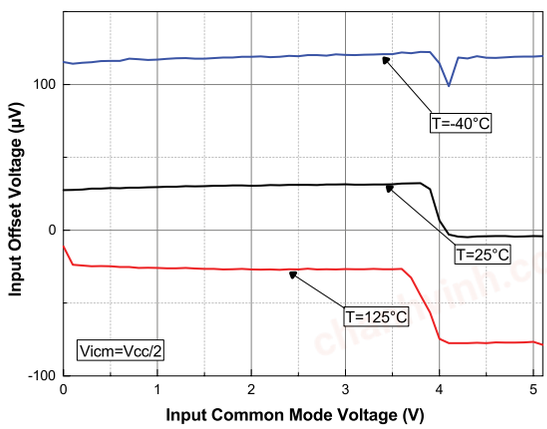


Figure 11. Input offset voltage vs. common mode voltage at V_{CC} = 36 V

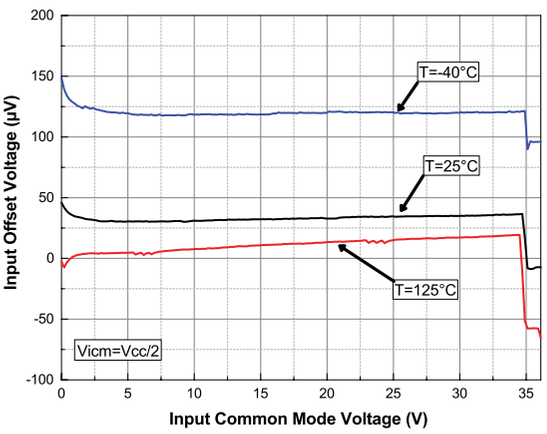
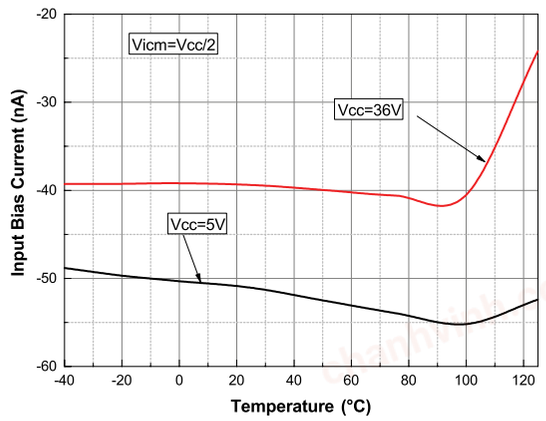


Figure 12. Input bias current vs. temperature at $V_{ICM} = V_{CC} / 2$



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Figure 13. Output current vs. output voltage at V_{CC} = 5 V

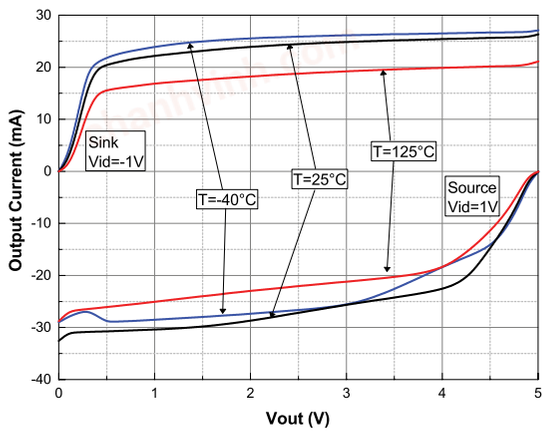


Figure 14. Input bias current vs. common mode voltage at V_{CC} = 5 V

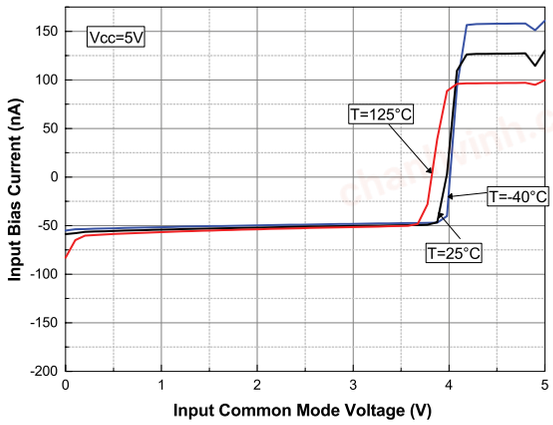


Figure 15. Input bias current vs. common mode voltage at V_{CC} = 36 V

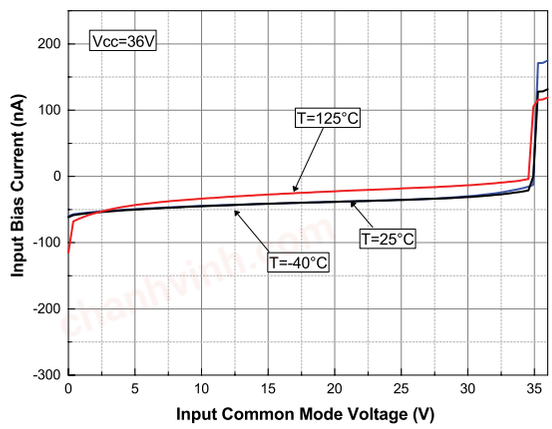


Figure 16. Output current vs. output voltage at V_{CC} = 36 V

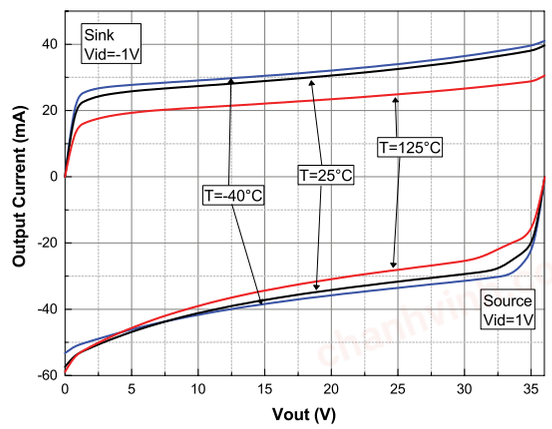


Figure 17. Output voltage (V_{OH}) vs. supply voltage

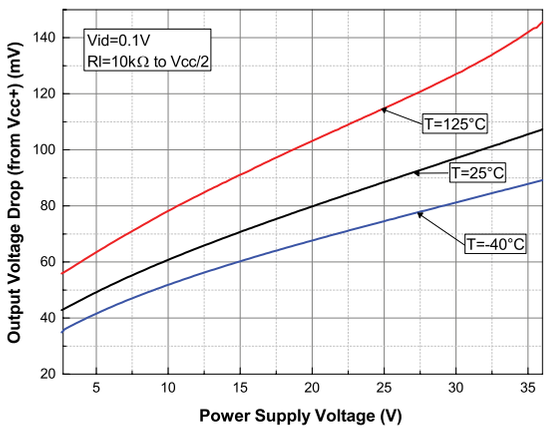
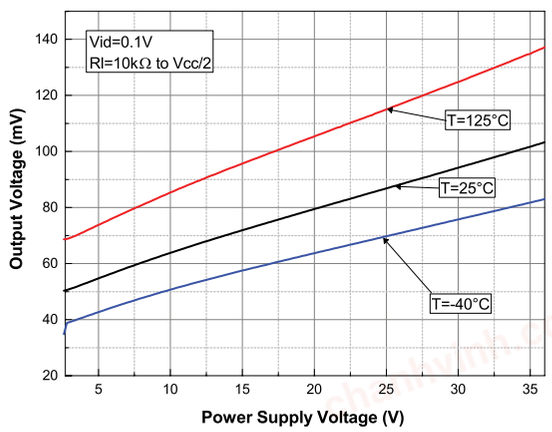


Figure 18. Output voltage (V_{OL}) vs. supply voltage



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Figure 19. Positive slew rate at V_{CC} = 36 V

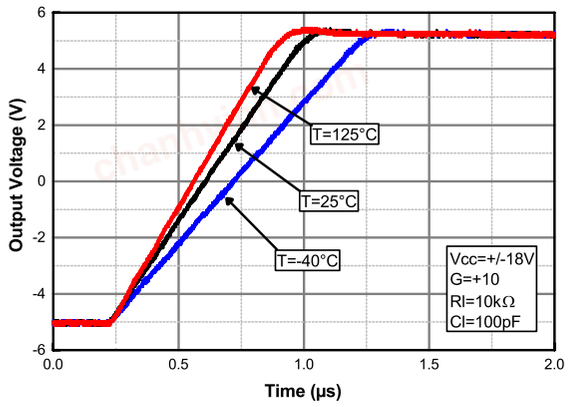


Figure 20. Negative slew rate at V_{CC} = 36 V

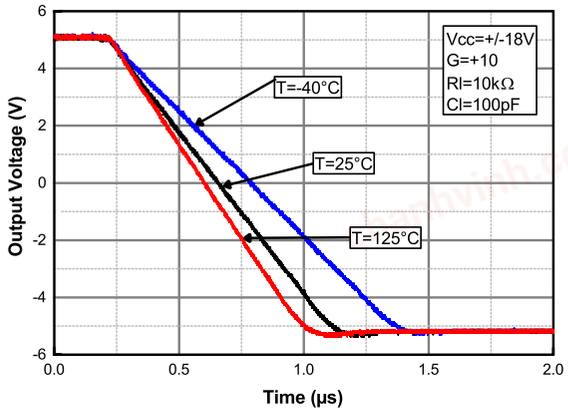


Figure 21. Bode diagram at V_{CC} = 5 V

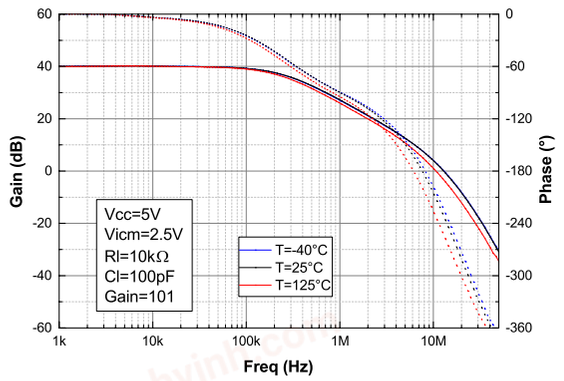


Figure 22. Bode diagram at V_{CC} = 36 V

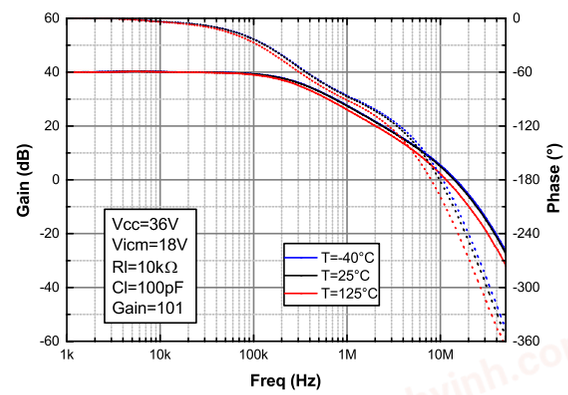


Figure 23. Phase margin vs. output current at V_{CC} = 5 V

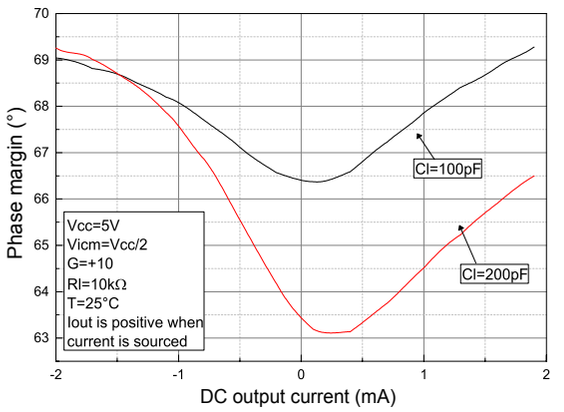
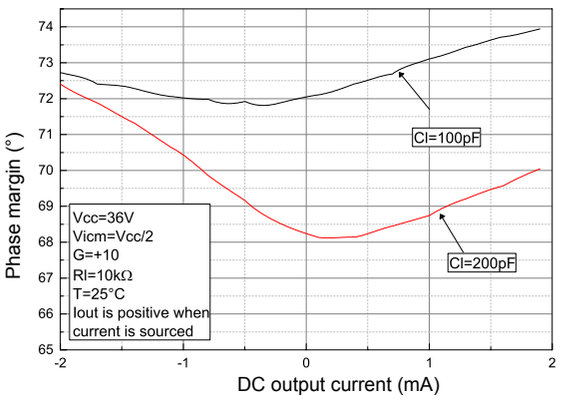


Figure 24. Phase margin vs. output current at V_{CC} = 36 V



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Figure 25. Phase margin vs. capacitive load

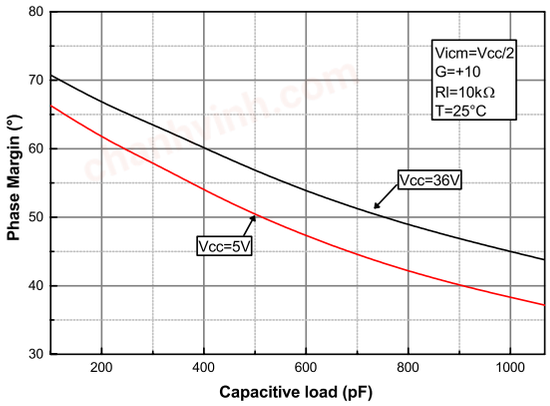


Figure 26. Small step response vs. time at V_{CC} = 5 V

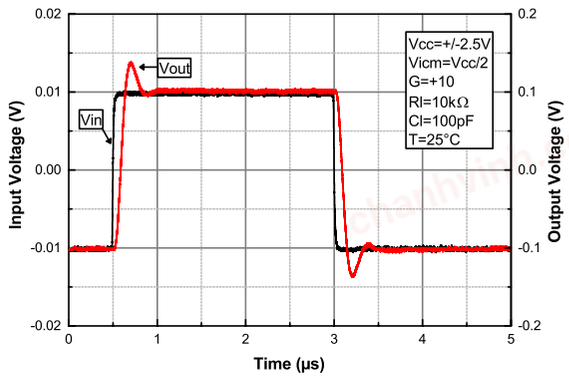


Figure 27. Desaturation time at low rail at V_{CC} = 5 V

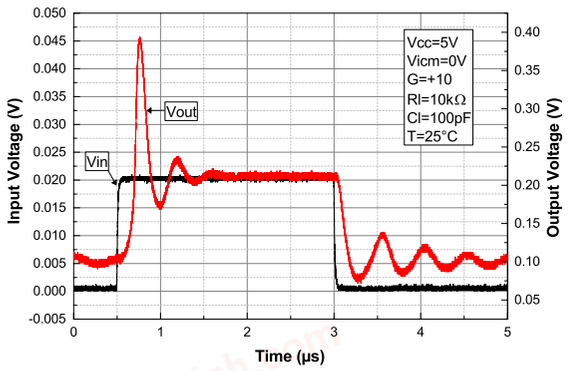


Figure 28. Desaturation time at high rail at V_{CC} = 5 V

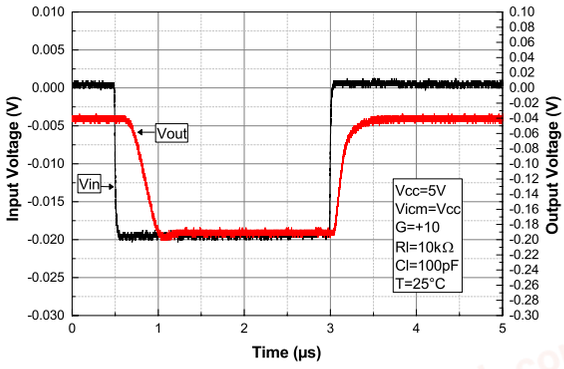


Figure 29. Small step response vs. time at V_{CC} = 36 V

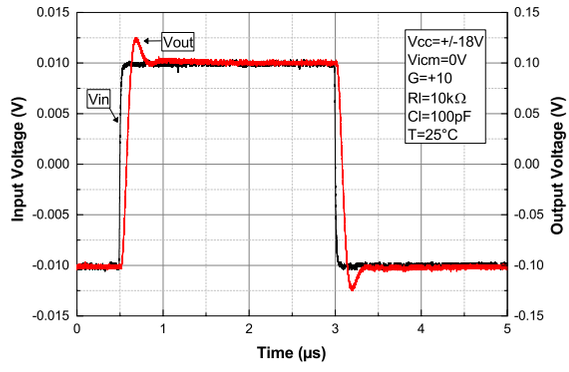
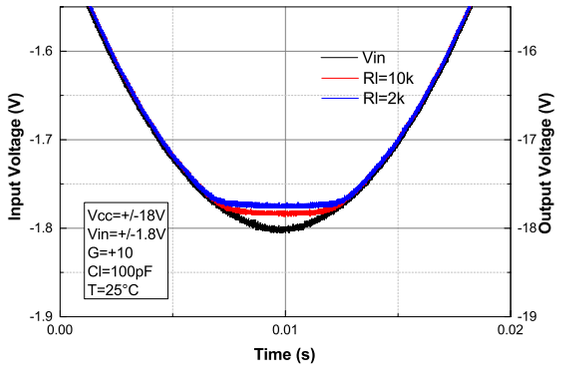


Figure 30. Amplifier behavior close to the low rail at V_{CC} = 36 V



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Figure 31. Amplifier behavior close to the high rail at V_{CC} = 36 V

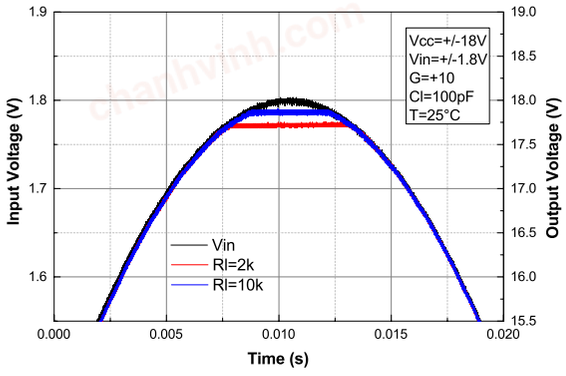


Figure 32. Noise vs. frequency at V_{CC} = 5 V

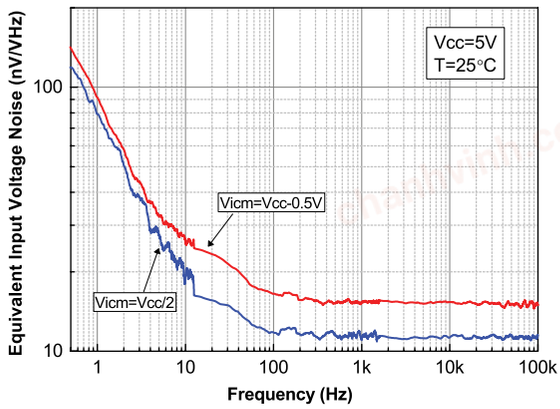


Figure 33. Noise vs. frequency at V_{CC} = 36 V

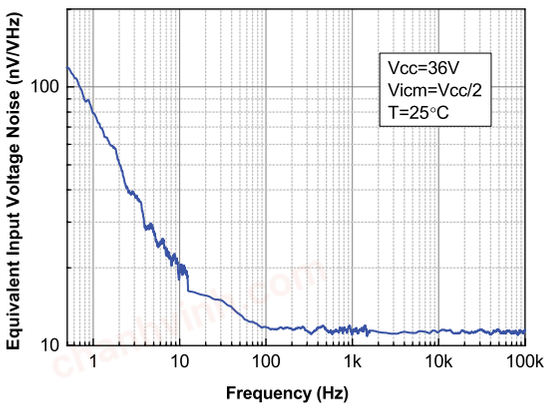


Figure 34. Noise vs. time at V_{CC} = 36 V

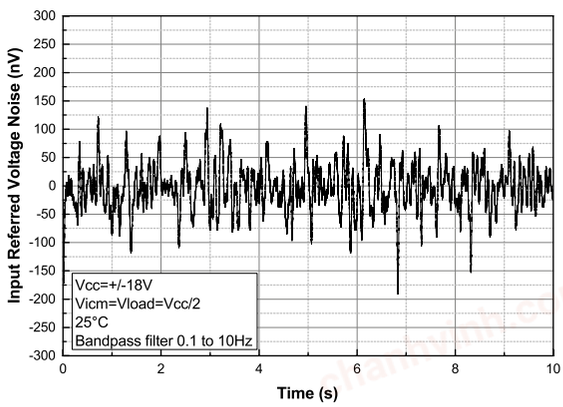


Figure 35. THD+N vs. frequency

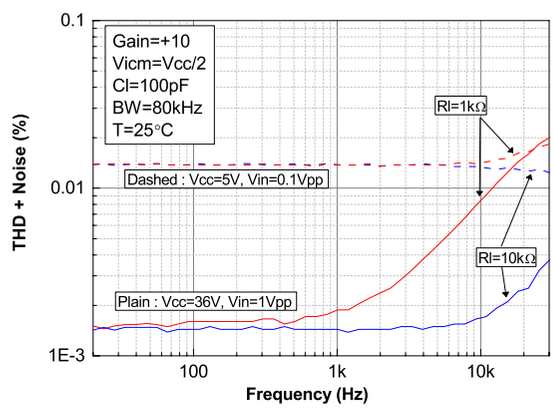
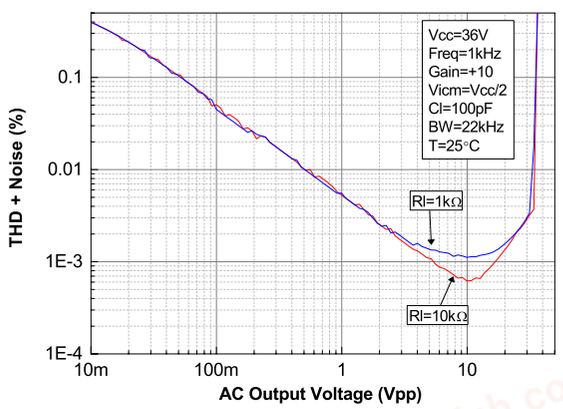


Figure 36. THD+N vs. output voltage



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Figure 37. **PSRR vs. frequency at V_{CC} = 10 V**

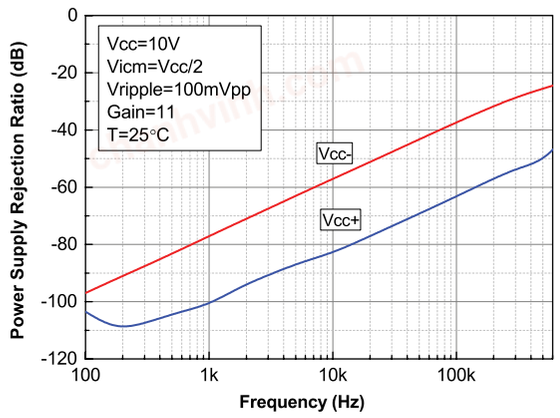


Figure 38. **CMRR vs. frequency at V_{CC} = 10 V**

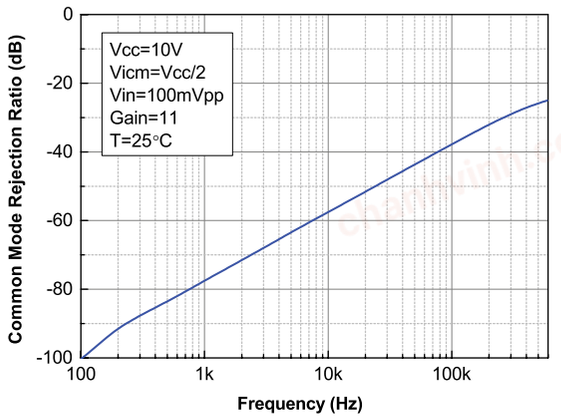
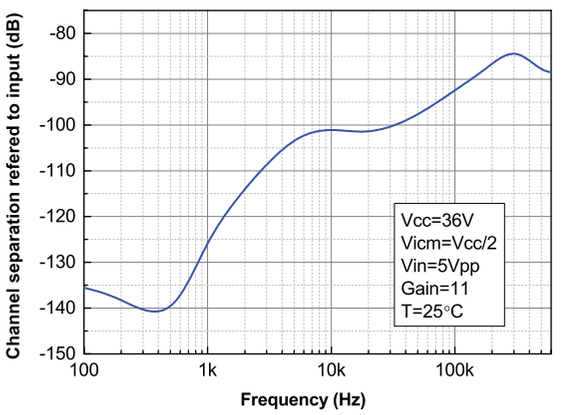


Figure 39. **Channel separation vs. frequency at V_{CC} = 36 V**



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5 Application information

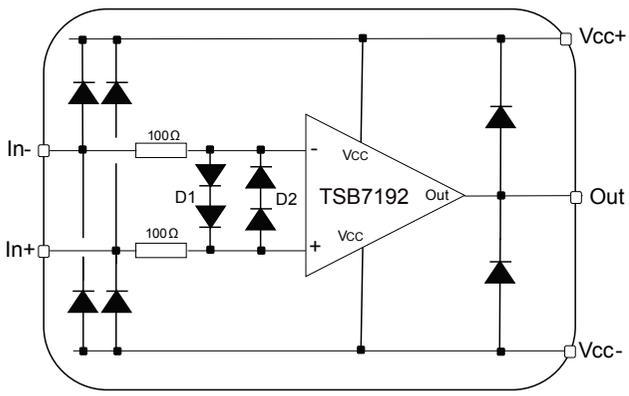
5.1 Operating voltages

The TSB7191, TSB7191A, TSB7192 and TSB7192A devices can operate from 2.7 to 36 V. The parameters are fully specified at 5 V and 36 V power supplies. However, the parameters are very stable over the full V_{CC} range and several characterization curves show the TSB7191, TSB7191A, TSB7192 and TSB7192A device characteristics over the full operating range. Additionally, the main specifications are guaranteed in extended temperature range from -40 to 125 °C.

5.2 Input pin voltage range

The TSB7191, TSB7191A, TSB7192 and TSB7192A devices have an internal ESD diode protection on the inputs. These diodes are connected between the inputs and each supply rail to protect the input stage from electrical discharge, as shown in the figure below.

Figure 40. Input current limitation



When the input pin voltage exceeds the power supply, the ESD diodes become conductive and, depending on this voltage, excessive current can flow through them. Without limitation this overcurrent can damage the device. In this case, the current has to be limited to 10 mA by adding a resistance in series with the input pin.

Similarly, in order to avoid excessive current in the protection diodes between the positive and negative inputs, the differential voltage should be limited to ± 2 V, or the current limited to 10 mA. Such a high differential voltage can be reached when the output is in saturation mode, or slew rate limited. In particular, it can happen when the device is used in comparator mode.

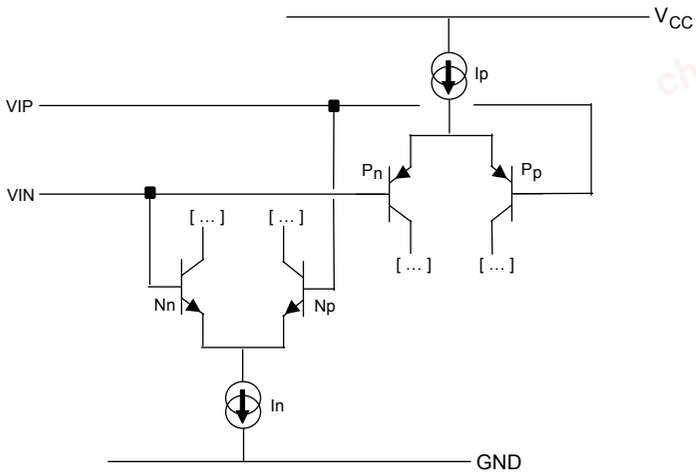
The TSB7191, TSB7191A, TSB7192 and TSB7192A do not show any phase reversal for any input common mode voltage inside the absolute maximum ratings (AMR) voltage window, $(V_{CC-}) - 200\ mV < V_{ICM} < (V_{CC+}) + 200\ mV$.

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5.3 Rail-to-rail input stage

The TSB7191, TSB7191A, TSB7192 and TSB7192A devices are built with two complementary NPN and PNP input differential pairs, as shown in the figure below.

Figure 41. Rail-to-rail input stage



The device has rail-to-rail inputs, and the input common mode range is extended from V_{CC-} to (V_{CC+}) + 0.1 V. However, the performance of these devices is optimized for the P-channel differential pair (which means from V_{CC-} to (V_{CC+}) - 1.5 V). Around (V_{CC+}) – 1 V, and with slight variations depending on the process, a transition occurs between the P-channel and the N-channel differential pair, impacting the input offset voltage (see Figure 10. Input offset voltage vs. common mode voltage at V_{CC} = 5 V and Figure 11. Input offset voltage vs. common mode voltage at V_{CC} = 36 V). As a consequence, CMRR can be degraded around this transition region. In order to achieve the best possible performance, this operating point should be avoided.

Please also notice that the input bias current polarity depends on the operation of NPN or PNP input stage. This transition is visible in figures Figure 14. Input bias current vs. common mode voltage at V_{CC} = 5 V and Figure 15. Input bias current vs. common mode voltage at V_{CC} = 36 V.

5.4 Input offset voltage drift over the temperature

The maximum input voltage drift variation over temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during the production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations. The maximum input voltage drift overtemperature is computed using the following formula:

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|_{T = -40\,°C \text{ and } T = 125\,°C} \quad (1)$$

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a Cpk (process capability index) greater than 1.3.

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5.5 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage.
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using:

(2)

$$A_{FV} = e^{\beta.(V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration coefficient in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined as follows:

(3)

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}.$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173 x 10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor.

(4)

$$A_F = A_{FT} \cdot A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in Equation 5 to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

(5)

$$Months = A_F \times 1000\ h \times 12\ months / (24\ h \times 365.25\ days)$$

To evaluate the op-amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum ratings (as recommended by JEDEC rules). V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions.

(6)

$$V_{CC} = max(V_{OP})\ with\ V_{icm} = V_{CC}/2$$

The long term drift parameter ΔV_{io} (in µV.$month^{-1/2}$), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months.

(7)

$$\Delta V_{io} = \frac{V_{io}drift}{\sqrt{months}}$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

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The Vio final drift, in µV, to be measured on the device in real operation conditions can be computed from:

(8)

$$V_{io\ final\ drift}(t_{op}, T_{op}, V_{CC}) = \Delta V_{io,\ 25°C} \cdot \sqrt{t_{op} \cdot e^{\beta \cdot (V_{CC} - V_{CC\ nom})} \cdot e^{\frac{E_a}{k} \cdot \left(\frac{1}{297} - \frac{1}{T_{op}}\right)}}$$

Where:

ΔV_{io} is the long term drift parameter in µV.month$^{-1/2}$

t_{op} is the operating time seen by the device, in months

T_{op} is the operating temperature

V_{CC} is the power supply during operating time

V_{CC} nom is the nominal V_{CC} at which the ΔV_{io} is computed (36 V for the TSB7192A).

E_a is the activation energy of the technology (here 0.7 eV).

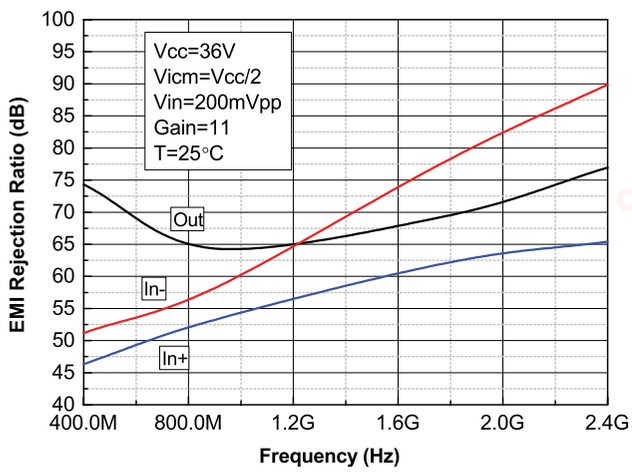
5.6 EMI rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op-amps is a change in the offset voltage as a result of RF signal rectification. EMIRR is defined as follows:

$$EMIRR = 20.\log\left(\frac{V_{in\ pp}}{\Delta V_{io}}\right) \quad (9)$$

The TSB7191, TSB7191A, TSB7192 and TSB7192A have been specially designed to minimize susceptibility to EMIRR and shows a low sensitivity. As visible on figure below, EMI rejection ratio has been measured on both inputs and outputs, from 400 MHz to 2.4 GHz.

Figure 42. EMIRR on In+, In- and out pins



EMIRR performance might be improved by adding small capacitances (in the pF range) on the inputs, power supply and output pins. These capacitances help in minimizing the impedance of these nodes at high frequencies.

5.7 Minimum gain

The TSB7191 and TSB7192 series is non-compensated op-amp, and thus it is not stable at unity gain. The minimum gain advised for this family is +10 or -9, for a capacitive load C_{load} = 100 pF; that guarantees a good stability at all biases and temperatures. For a lower gain, the TSB712 series must be preferred.

However, a TSB7191 and TSB7192 op-amp can be used in follower mode at low frequency, provided that the circuit is externally compensated. This can be useful for the second channel, when the TSB7192 frequency or slew rate performance is needed for the first channel. In this case, the circuit topology described in the figure below can be used. At low frequency, the circuit behaves as a follower, but at high frequency (>1 MHz), the circuit is stabilized by attenuating the feedback injected into the negative input.

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Figure 43. **Proposed circuit configuration for unity gain stability**

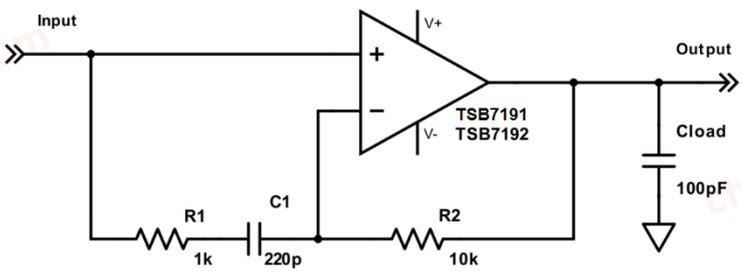


Figure 44. **Small step response vs. time in follower configuration**

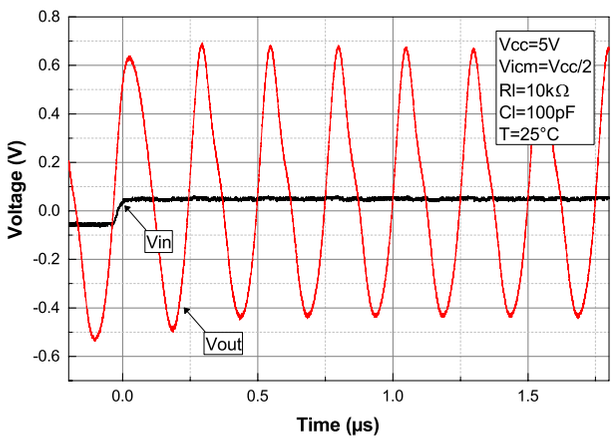
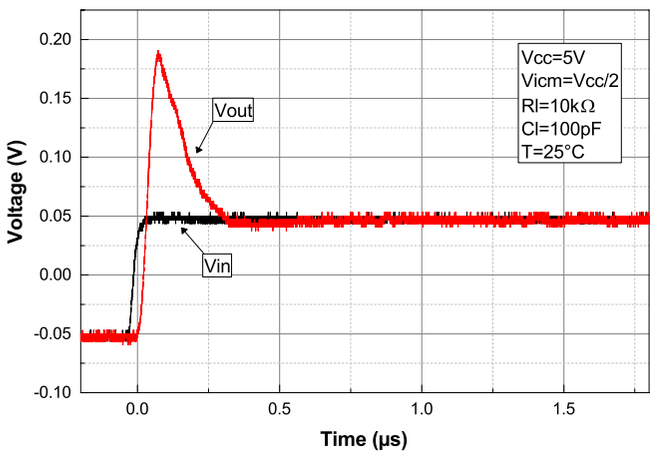


Figure 45. **Small step response vs. time in the proposed compensated circuit configuration**



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5.8 Unused channel

When one of the two channels of the TSB7192 and TSB7192A is not used, it must be properly connected in order to avoid internal oscillations that can negatively impact the signal integrity on the other channel, as well as the current consumption. Two different configurations can be used:

- Gain configuration: the channel can be set in gain at which the stability is guaranteed (+10/-9 or more). The input can be set to any voltage within the V_{icm} operating range.
- Comparator configuration: the channel can be set to a comparator configuration (without negative feedback). In this case, positive and negative inputs can be set to any value provided that these values are significantly different (100 mV or more, to avoid oscillations between positive and negative state) and the differential input is lower than the maximum specified in the operating range (maximum 2 V), or the input current is limited to less than 10 mA to avoid damaging the circuit.

5.9 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSB7191, TSB7191A, TSB7192 and TSB7192A is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times R_{th-ja} + T_A \quad (10)$$

T_J is the die junction temperature

P_D is the power dissipated in the package

$R_{th\text{-}ja}$ is the junction to ambient thermal resistance of the package

T_A is the ambient temperature

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$$P_D = (V_{CC} \times I_{CC}) + (V_{CC+} - V_{OUT}) \times ILoad \quad (11)$$

when the op-amp sources the current

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} - V_{CC-}) \times ILoad \quad (12)$$

when the op-amp is sinks the current.

Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

5.10 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces connecting the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.11 Decoupling capacitor

In order to ensure op-amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op-amp supply pin. A good decoupling helps to reduce electromagnetic interference impact.

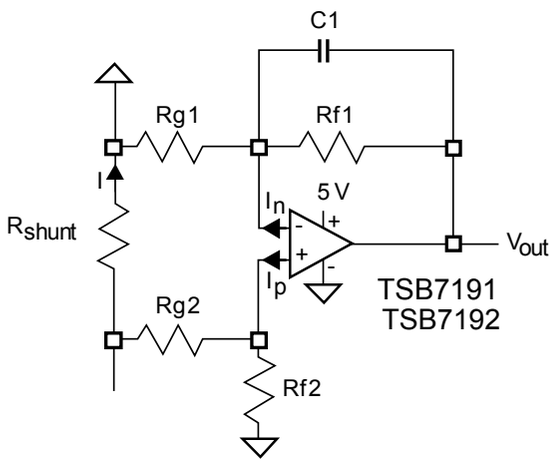
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6 Typical applications

6.1 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful to protect applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSB7191 and the TSB7192 (see the following figure).

Figure 46. Low-side current sensing schematic



V_{out} can be expressed as follows:

$$V_{OUT} = R_{shunt}.I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right).\left(1 - \frac{R_{f1}}{R_{g1}}\right) + I_p.\frac{R_{g2}.R_{f2}}{R_{g2} + R_{f2}}.\left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n.R_{f1} - V_{io}.\left(1 - \frac{R_{f1}}{R_{g1}}\right) \quad (13)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, can be simplified in the following manner:

$$V_{OUT} = R_{shunt}.I.\frac{R_f}{R_g} - V_{io}.\left(1 + \frac{R_f}{R_g}\right) + R_f.I_{io} \quad (14)$$

The main advantage of using the TSB7191 and the TSB7192 for a low-side current sensing relies on its low V_{io}, compared to general purpose operational amplifiers. For the same current and targeted accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost. Particular attention must be paid to the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement.

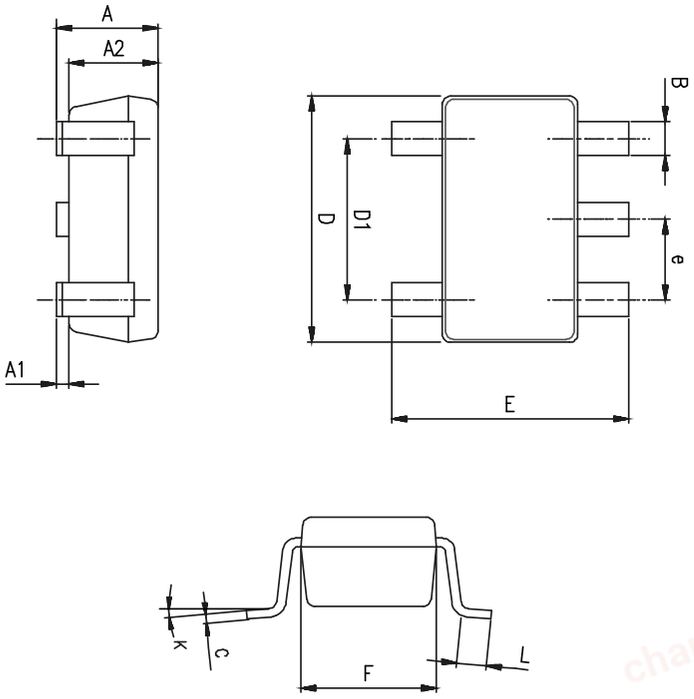
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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SOT23-5 package information

Figure 47. SOT23-5 package outline



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Table 7. **SOT23-5 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.020
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0°		10°	0°		10°

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7.2 MiniSO8 package information

Figure 48. **MiniSO8 package outline**

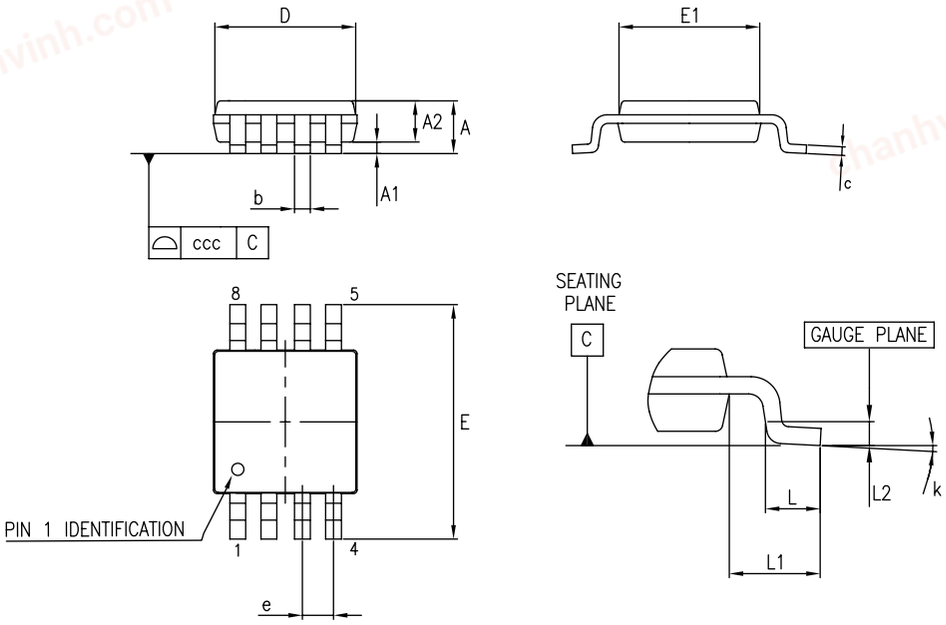


Table 8. **MiniSO8 mechanical data**

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

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7.3 SO8 package information

Figure 49. **SO8 package outline**

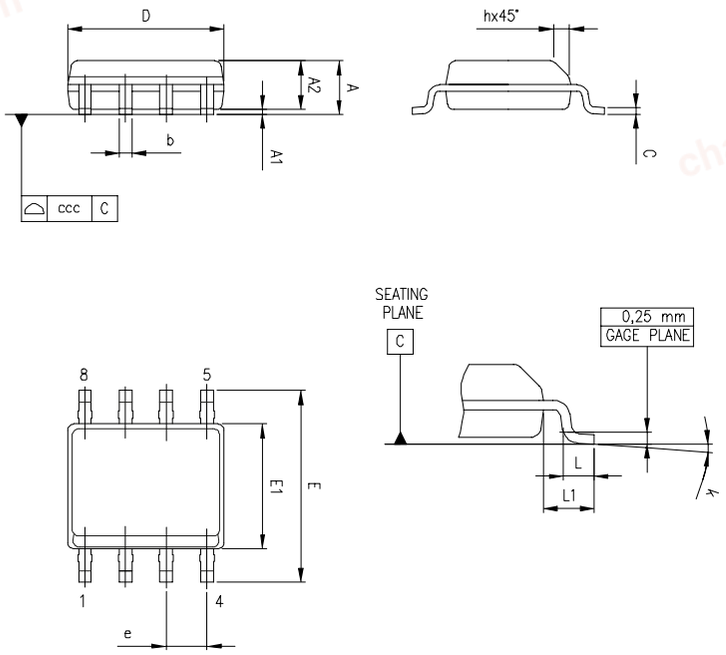


Table 9. **SO-8 mechanical data**

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

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8 Ordering information

Table 10. Order code

Order code	Temperature range	Package	Packing	Marking
TSB7191AILT	-40 °C to +125 °C	SOT23-5	Tape and reel	K224
TSB7191ILT		SOT23-5		K220
TSB7191AIYLT	-40 °C to +125 °C automotive grade	SOT23-5		K226
TSB7191IYLT		SOT23-5		K222
TSB7192AIST	-40 °C to +125 °C	MiniSO8		K21A
TSB7192AIDT		SO8		7192AI
TSB7192IDT		SO8		7192I
TSB7192IST		MiniSO8		792S
TSB7192AIYDT	-40 °C to 125 °C automotive grade(1)	SO8		7192AIY
TSB7192AIYST		MiniSO8		792Y
TSB7192IYDT		SO8		7192IY
TSB7192IYST		MiniSO8		K21Y

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.*

SO8 package for single op-amp may be available for qualification upon customer request. Please contact sales office for such request.

DFN8 package for dual op-amp may be available for qualification under customer request. Please contact sales office for such request.

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Revision history

Table 11. **Document revision history**

Date	Revision	Changes
29-Jun-2018	1	Initial release.
26-Sep-2018	2	Added the TSB7192 as root part number; cover page has been updated accordingly. Updated Section 3 Electrical characteristics, Section 4 Typical performance characteristics, Section 5.1 Operating voltages, Section 5.2 Input pin voltage range, Section 5.3 Rail-to-rail input stage and Section 5.6 EMI rejection, Section 8 Ordering information. Added Section 7.2 SO8 package information.
29-Nov-2018	3	Updated Table 5. Electrical characteristics at VCC = 36 V, VICM = VOUT = VCC / 2, Tamb = 25 °C and RL connected to VCC / 2 (unless otherwise specified) and Table 6. Electrical characteristics at VCC = 5 V, VICM = VOUT = VCC / 2, Tamb = 25 °C and RL connected to VCC / 2 (unless otherwise specified).
17-Jun-2019	4	Added root part numbers TSB7191A and TSB7192A, therefore the whole document has been updated accordingly.
15-Oct-2019	5	Updated Table 10. Order code.

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