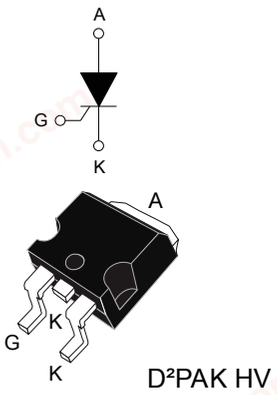
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TN4050HP-12G2YTR

Datasheet

40 A 1200 V automotive grade thyristor (SCR)



D²PAK HV

Features

- AEC-Q101 qualified
- High junction temperature: 150 °C
- AC off state voltage: +/- 1200 V
- Nominal on-state RMS current: 40 A_{RMS}
- High EFT noise immunity: 1000 V/µs
- Max. gate triggering current: 50 mA
- D²PAK HV creepage distance (anode to cathode):
  - With top coating: 5.38 mm min.
  - Without top coating: 3.48 mm min.
- ECOPACK2 compliant component

Application

- On board charger
- Capacitor discharge
- Overvoltage crowbar protection
- Power supplies
- AC switches
- Solid state relays

Product status
TN4050HP-12G2YTR

Product summary	
$I_{T(RMS)}$	40 A
V_{DRM}/V_{RRM}	1200 V
V_{DSM}/V_{RSM}	1400 V
I_{GT}	50 mA
T_j	-40 to 150 °C

Description

The TN4050HP-12G2YTR is an automotive grade SCR thyristor designed for applications such as automotive on board and stationary battery chargers.

This SCR Thyristor, rated for a 40 A RMS power switching, offers superior performances in peak voltage robustness up to 400 V sine wave pulse. Its key features allow the design of functions such as a 56 A RMS AC switch and a 50 A AC-DC controlled rectifier-bridge.

The TN4050HP-12G2YTR is available in D²PAK HV surface mount package, ideal for automatic assembly lines.

D²PAK HV package offers increased creepage distance of 5.38 mm, simplifying design conformity with insulation coordination standards such as IEC60664-1 and UL-840.

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1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (180 ° conduction angle)		T_C = 135 °C	40	A
$I_{T(AV)}$	Average on-state current (180 ° conduction angle)			25	
I_{TSM}	Non repetitive surge peak on-state current, V_R = 0 V	t_p = 8.3 ms	T_j initial = 25 °C	440	A
		t_p = 10 ms		400	
I^2t	I^2t value for fusing	t_p = 10 ms	T_j = 25 °C	800	A^2s
dI/dt	Critical rate of rise of on-state current, I_G = 2 x I_{GT} , tr ≤ 100 ns	f = 50 Hz	T_j = 150 °C	200	A/µs
V_{DRM} / V_{RRM}	Repetitive off-state voltage		T_j = 150 °C	1200	V
V_{DSM} / V_{RSM}	Non repetitive surge peak off-state voltage	t_p = 10 ms	T_j = 25 °C	1400	V
V_{GM}	Peak forward gate voltage	t_p = 20 µs	T_j = 150 °C	10	V
I_{GM}	Peak forward gate current	t_p = 20 µs	T_j = 150 °C	8	A
V_{RGM}	Maximum peak reverse gate voltage		T_j = 25 °C	5	V
$P_{G(AV)}$	Average gate power dissipation		T_j = 150 °C	1	W
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature			-40 to +150	°C

Table 2. Electrical characteristics (T_j = 25 °C unless otherwise specified)

Symbol	Test Conditions			Value	Unit
I_{GT}	V_D = 12 V, R_L = 33 Ω		Min.	10	mA
			Max.	50	
V_{GT}			Max.	1.3	V
I_{GD}	V_D = 800 V, R_L = 3.3 Ω	T_j = 150 °C	Min.	3	mA
V_{GD}	V_D = 800 V, R_L = 3.3 Ω	T_j = 150 °C	Min.	0.2	V
I_H	I_T = 500 mA, gate open		Max.	100	mA
I_L	I_G = 1.2 x I_{GT}		Max.	125	mA
dV/dt	V_D = 800 V, gate open	T_j = 150 °C	Min.	1000	V/µs

Table 3. Timing Parameters

Symbol	Test Conditions			Value	Unit
t_{gt}	I_T = 80 A , V_D = 800 V, I_G = 100 mA, dI_G/dt = 0.2 A/µs		Typ.	1	µs
t_q	I_{TM} = 25 A, V_D = 800 V, dI_T/dt = 10 A/µs, V_R = 75 V, dV_D/dt = 20 V/µs, t_p = 100 µs	T_j = 150 °C	Typ.	150	µs

Table 4. Static Characteristics

Symbol	Test Conditions			Value	Unit
V_{TM}	I_{TM} = 80 A, t_P = 380 µs	T_j = 25 °C	Max.	1.55	V

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Symbol	Test Conditions			Value	Unit
V_{TO}	On-state threshold voltage	T_j = 150 °C	Max.	0.83	V
R_D	On-state dynamic resistance	T_j = 150 °C	Max.	10	mΩ
I_{DRM}/I_{RRM}	$V_D = V_{DRM}$, $V_R = V_{RRM}$	T_j = 25 °C	Max.	5	µA
		T_j = 125 °C		0.9	mA
		T_j = 150 °C		6	mA
I_{DSM}/I_{RSM}	$V_D = V_{DSM}$, $V_R = V_{RSM}$	T_j = 25 °C	Max.	10	µA

Table 5. Thermal parameters

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (DC)	Max.	0.4	°C/W
$R_{th(j-a)}$	Junction to ambient (DC, S_{CU} = 2.5 cm², e_{CU} = 70 µm)	Typ.	45	

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1.1 Characteristics (curves)

Figure 1. Maximum average power dissipation versus average on-state current

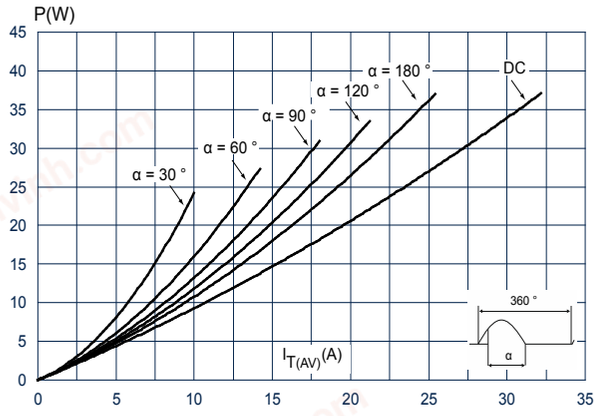


Figure 2. Average and D.C. on-state current versus case temperature

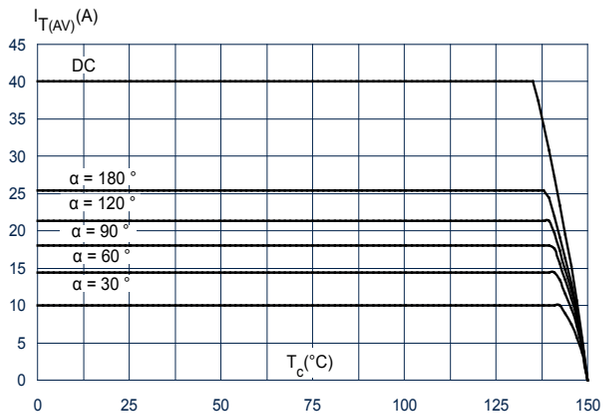


Figure 3. Average and D.C. on-state current versus ambient temperature

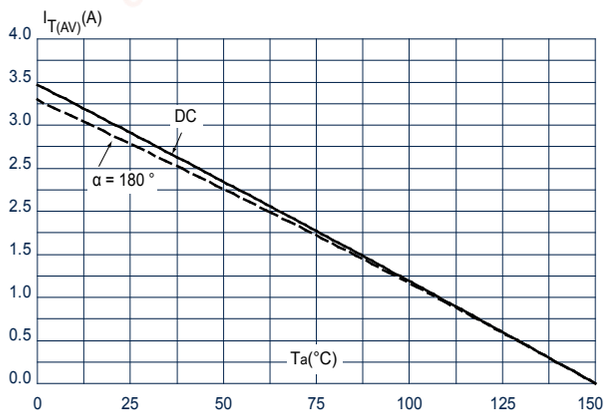


Figure 4. On-state characteristics (maximum values)

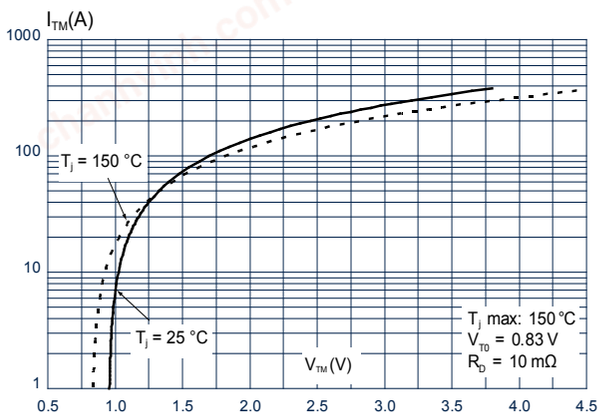


Figure 5. Surge peak on-state current versus number of cycles

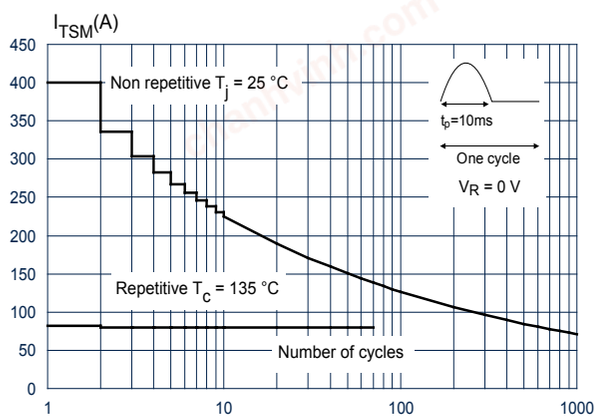
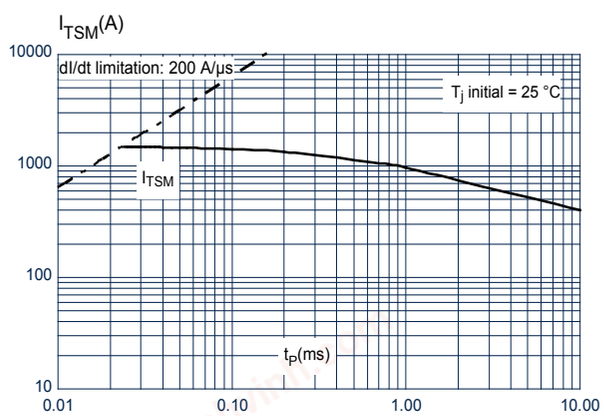


Figure 6. Non repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms



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Figure 7. Relative variation of leakage current versus junction temperature for different values of blocking voltage (typical values)

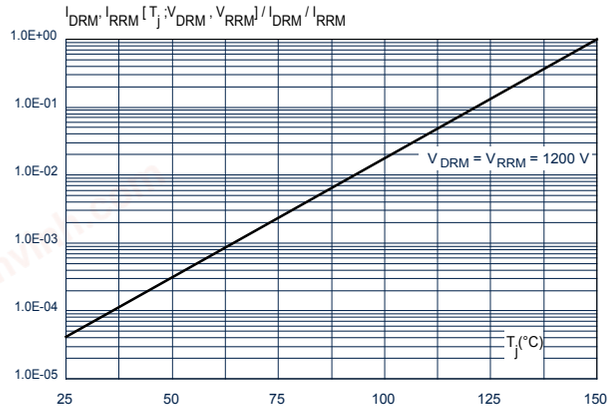


Figure 8. Relative variation of holding and latching current versus junction temperature (typical values)

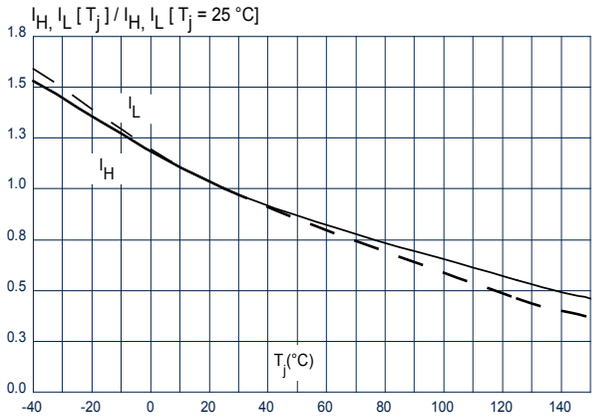


Figure 9. Relative variation of gate trigger current and gate voltage versus junction temperature (typical values)

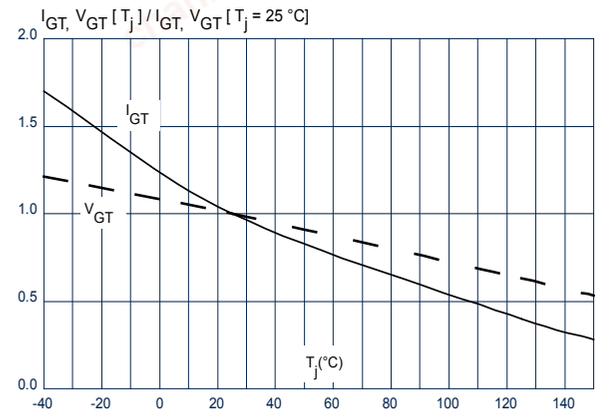


Figure 10. Relative variation of thermal impedance junction to case and junction to ambient versus pulse duration

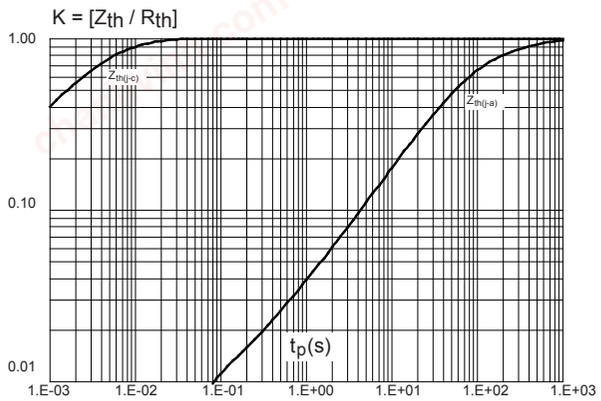


Figure 11. Thermal resistance junction to ambient versus copper surface under tab (typical values, epoxy printed board FR4) (D²PAK)

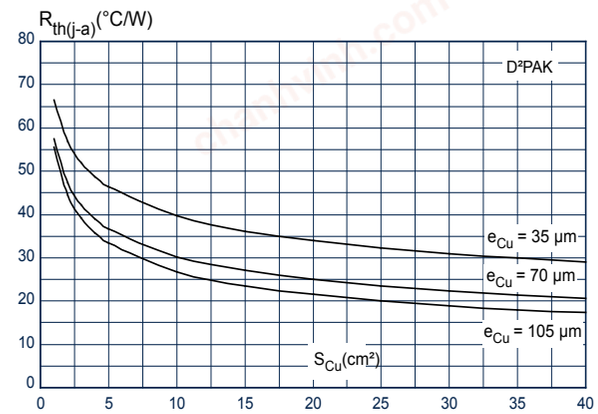
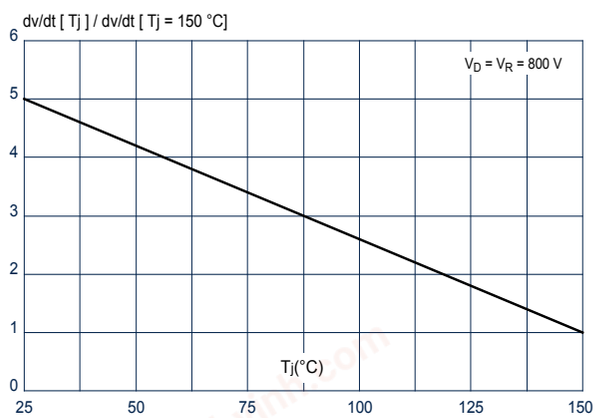


Figure 12. Relative variation of static dV/dt immunity versus junction temperature



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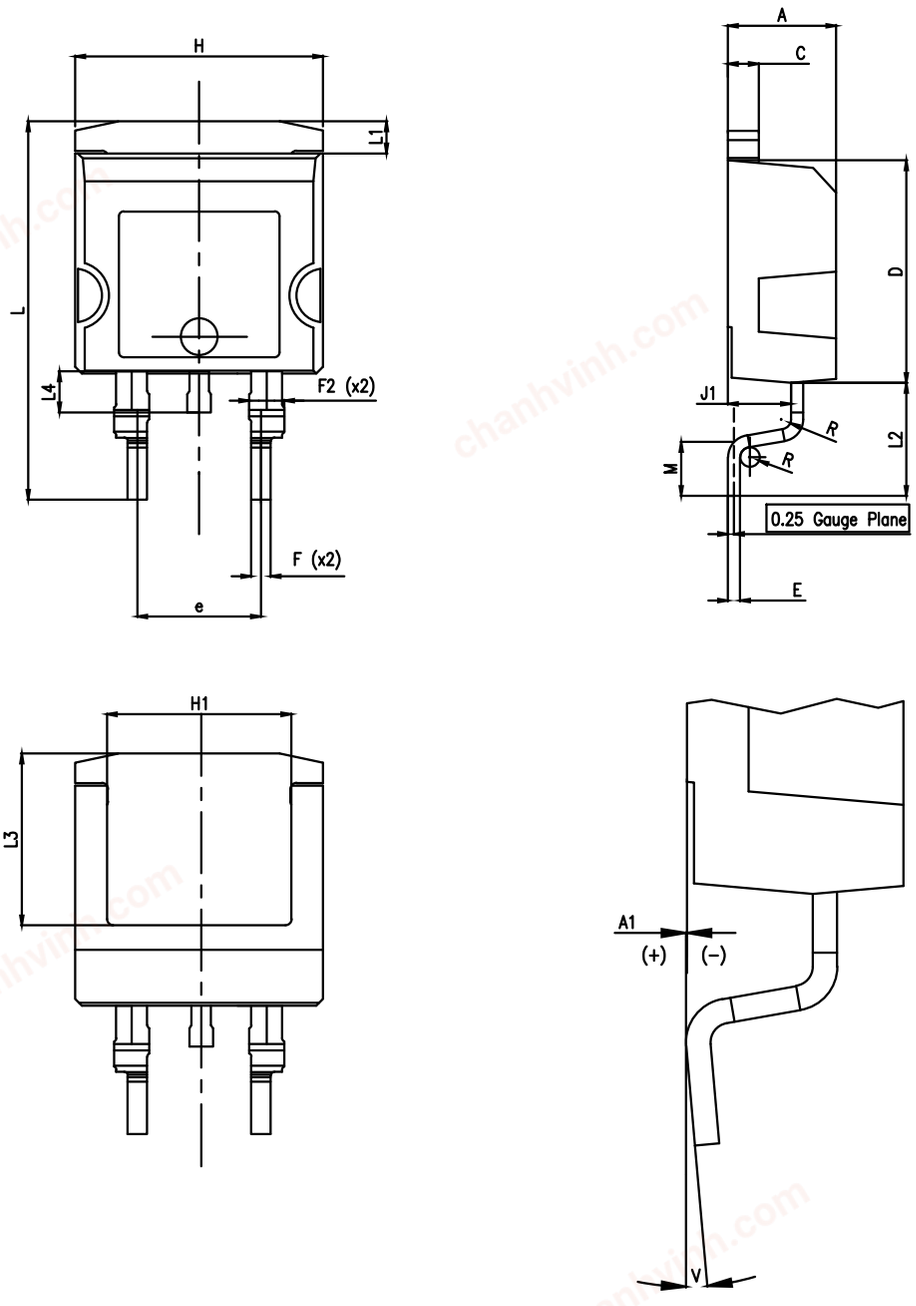
2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 D²PAK high voltage package information

- Epoxy meets UL94, V0

Figure 13. D²PAK high voltage package outline

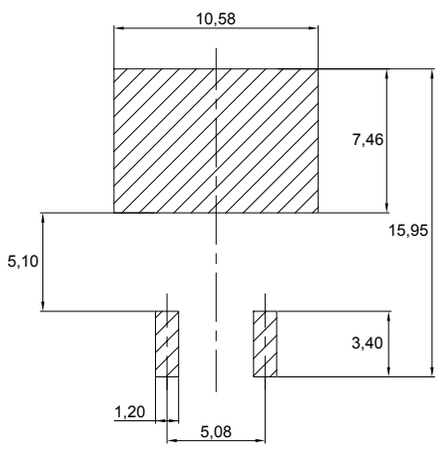


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Table 6. **D²PAK high voltage package mechanical data**

Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.30	4.70	0.1692	0.1851
A1	0.03	0.20	0.0011	0.0079
C	1.17	1.37	0.0460	0.0540
D	8.95	9.35	0.3523	0.3682
e	4.98	5.18	0.1960	0.2040
E	0.50	0.90	0.0196	0.0355
F	0.78	0.85	0.0307	0.0335
F2	1.14	1.70	0.0448	0.0670
H	10.00	10.40	0.3937	0.4095
H1	7.40	7.80	0.2913	0.3071
J1	2.49	2.69	0.0980	0.1060
L	15.30	15.80	0.6023	0.6221
L1	1.27	1.40	0.0500	0.0552
L2	4.93	5.23	0.1940	0.2060
L3	6.85	7.25	0.2696	0.2855
L4	1.50	1.7	0.0590	0.0670
M	2.60	2.9	0.1023	0.1142
R	0.20	0.60	0.0078	0.0237
V	0°	8°	0°	8°

Figure 14. **D²PAK high voltage footprint in mm**



Note: For package and tape orientation, reel and inner box dimensions and tape outline please check TN1173.

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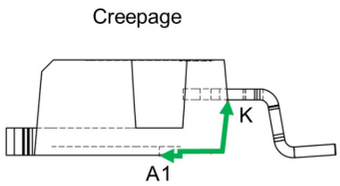
2.1.1 Creepage distance between anode and cathode

Table 7. Creepage distance between anode and cathode

Symbol	Parameter		Value	Unit
Cd_{K-A1}	Minimum creepage distance between K and A1 (with top coating)	D²PAK HV	5.38	mm
Cd_{K-A2}	Minimum creepage distance between K and A2 (without top coating)		3.48	

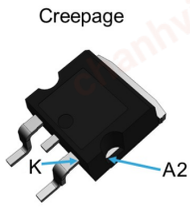
Note: D²PAK HV creepage distance (anode to cathode) = 5.38 mm min. (refer to IEC 60664-1)

Figure 15. Creepage with top coating



Minimum distance between K & A1 = 5.38 mm (with top coating)

Figure 16. Creepage without top coating



Minimum distance between K & A2 = 3.48 mm (without top coating)

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3 Ordering information

Figure 17. **Ordering information scheme**

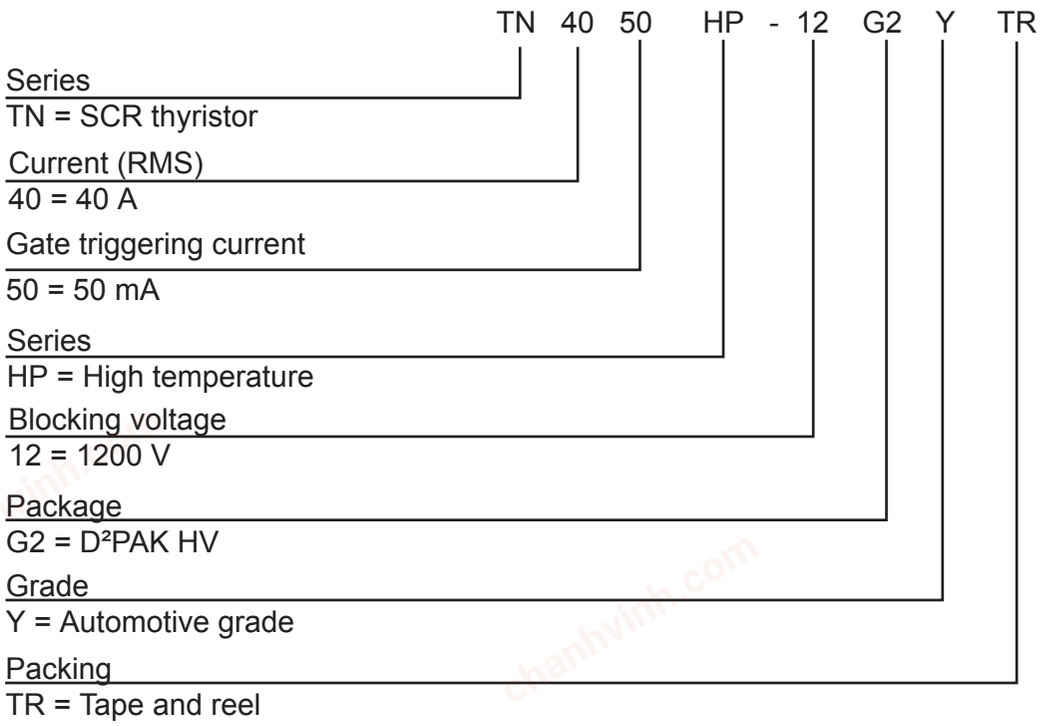


Table 8. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TN4050HP-12G2YTR	TN40P12YB2	D²PAK HV	1.38 g	1000	Tape and reel 13"

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Revision history

Table 9. **Document revision history**

Date	Revision	Changes
03-Aug-2021	1	Initial release.
16-Dec-2021	2	Updated Table 2. Added Figure 6 and Figure 11.

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