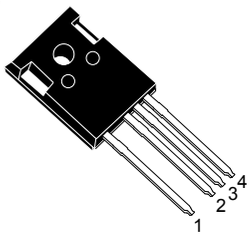
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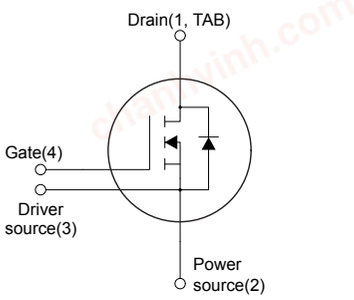
STW65N045M9-4

Datasheet

N-channel 650 V, 39 mΩ typ., 54 A MDmesh M9 Power MOSFET in a TO247-4 package



TO247-4



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW65N045M9-4	650 V	45 mΩ	54 A

- Worldwide best FOM $R_{DS(on)}$*Q_g among silicon-based devices
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance thanks to the extra driving source pin
- Easy to drive
- 100% avalanche tested

Applications

- High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

Product status link
STW65N045M9-4

Product summary	
Order code	STW65N045M9-4
Marking	65N045M9
Package	TO247-4
Packing	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	54	A
	Drain current (continuous) at T_C = 100 °C	34	
I_{DM}(1)	Drain current (pulsed)	170	A
P_{TOT}	Total power dissipation at T_C = 25 °C	312	W
dv/dt(2)	Peak diode recovery voltage slope	50	V/ns
di/dt(2)	Peak diode recovery current slope	850	A/µs
dv/dt(3)	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 28 A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.40	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	775	mJ

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2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			200	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 28 A		39	45	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 1 MHz, V_{GS} = 0 V	-	4610	-	pF
C_{oss}	Output capacitance		-	76	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	885	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, open drain	-	1	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 28 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	80	-	nC
Q_{gs}	Gate-source charge		-	26.5	-	nC
Q_{gd}	Gate-drain charge		-	23.5	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 28 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	28	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	85	-	ns
t_f	Fall time		-	4	-	ns

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Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		54	A
I_{SDM}(1)	Source-drain current (pulsed)		-		170	A
V_{SD}(2)	Forward on voltage	I_{SD} = 55 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 55 A, di/dt = 100 A/µs,	-	288		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	4		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	26		A
t_{rr}	Reverse recovery time	I_{SD} = 55 A, di/dt = 100 A/µs,	-	400		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	7.5		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	34		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

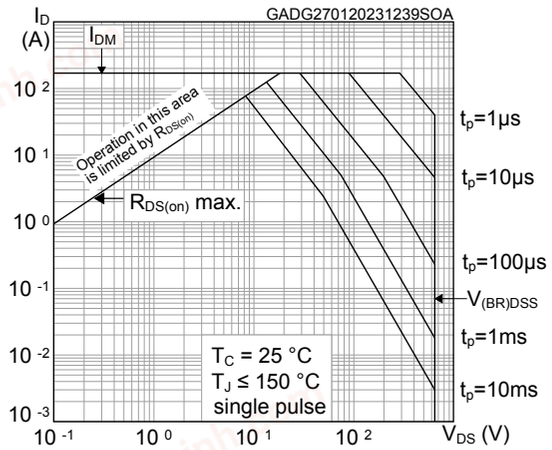


Figure 2. Maximum transient thermal impedance

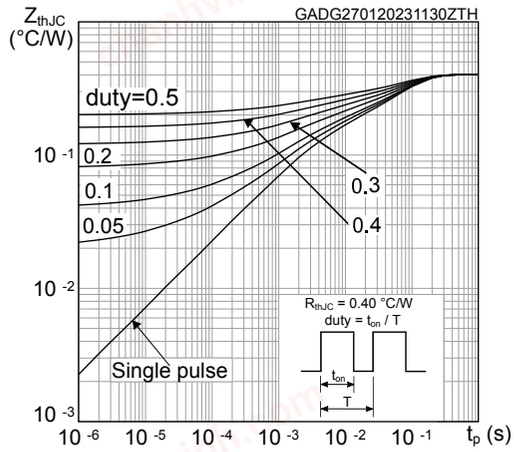


Figure 3. Typical output characteristics

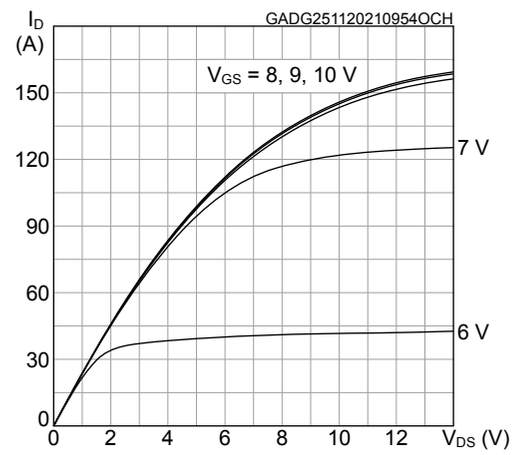


Figure 4. Typical transfer characteristics

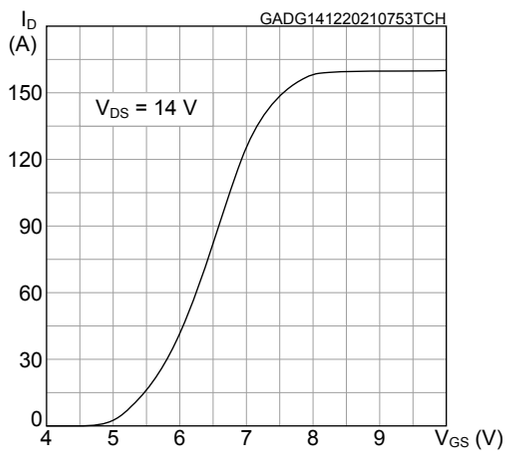


Figure 5. Typical gate charge characteristics

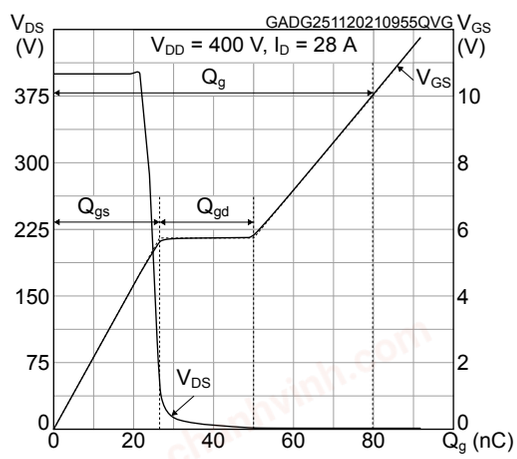
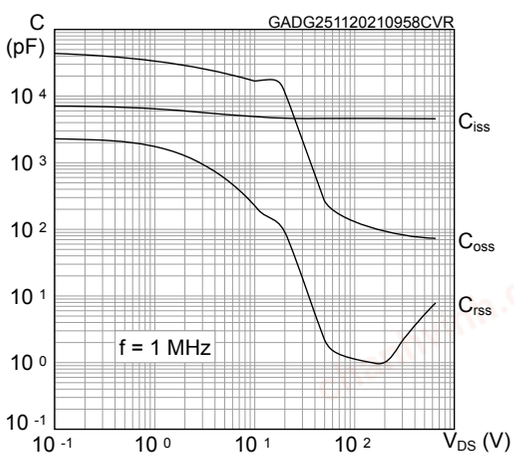


Figure 6. Typical capacitance characteristics



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Figure 7. Typical drain-source on-resistance

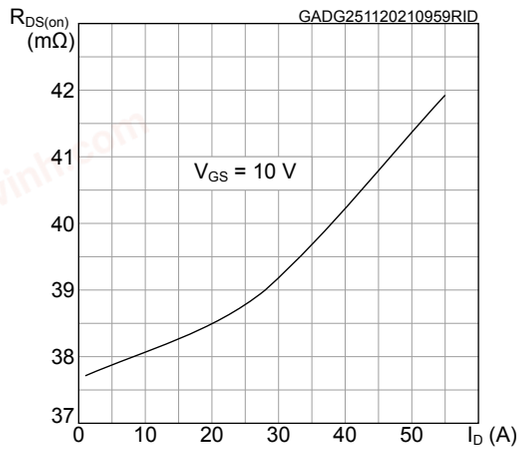


Figure 8. Normalized on-resistance vs temperature

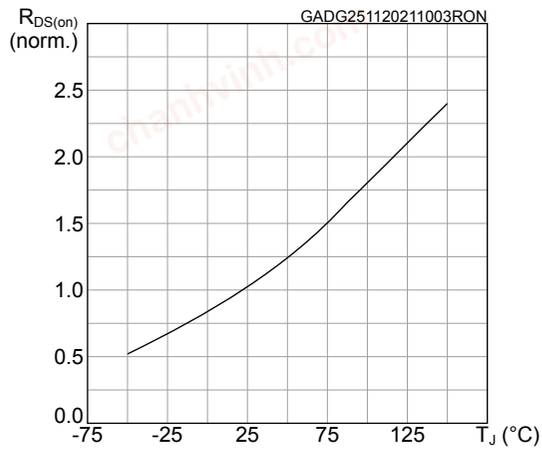


Figure 9. Normalized gate threshold vs temperature

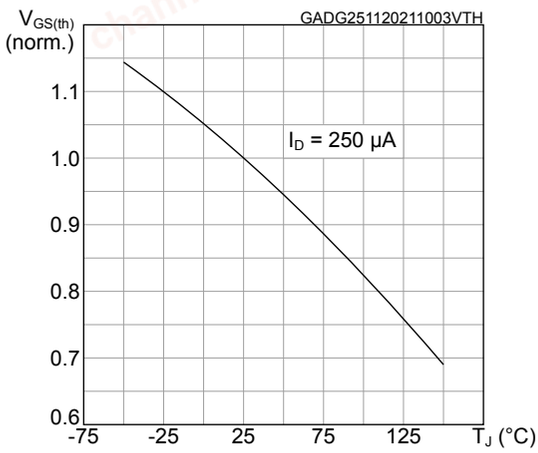


Figure 10. Normalized breakdown voltage vs temperature

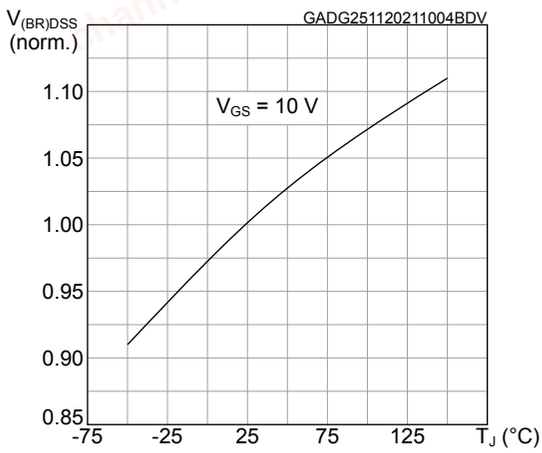


Figure 11. Typical reverse diode forward characteristics

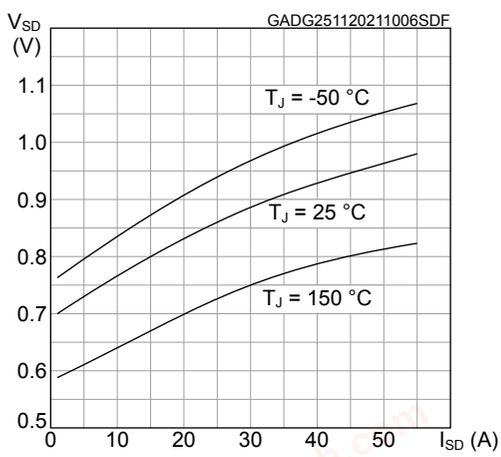
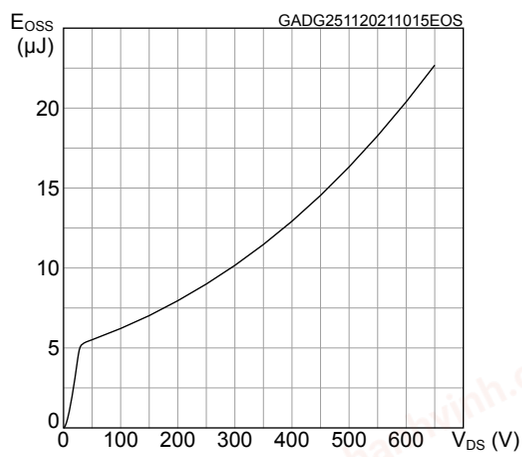


Figure 12. Typical output capacitance stored energy



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3 Test circuits

Figure 13. Switching times test circuit for resistive load

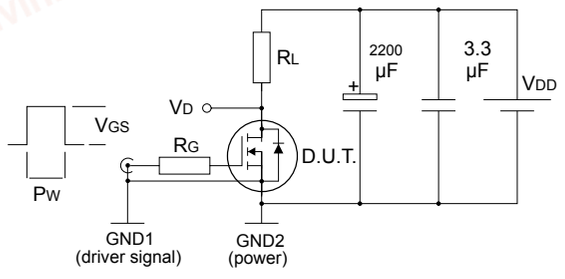


Figure 14. Test circuit for gate charge behavior

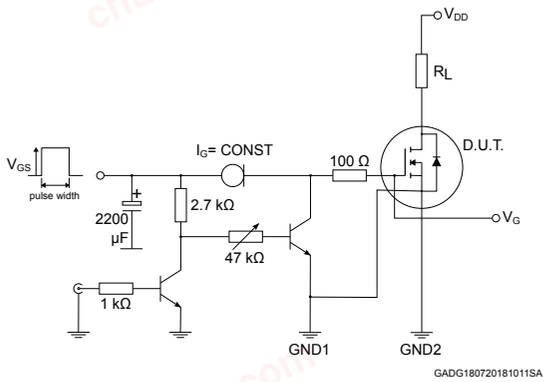


Figure 15. Test circuit for inductive load switching and diode recovery times

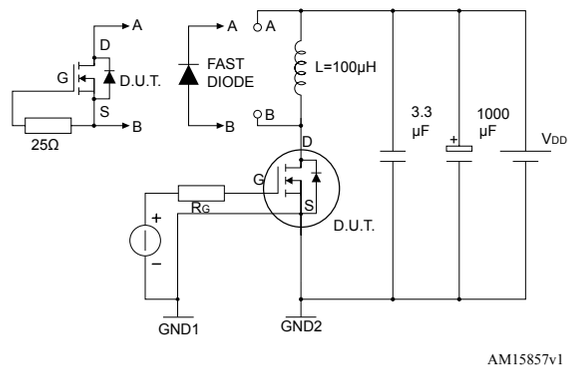


Figure 16. Unclamped inductive load test circuit

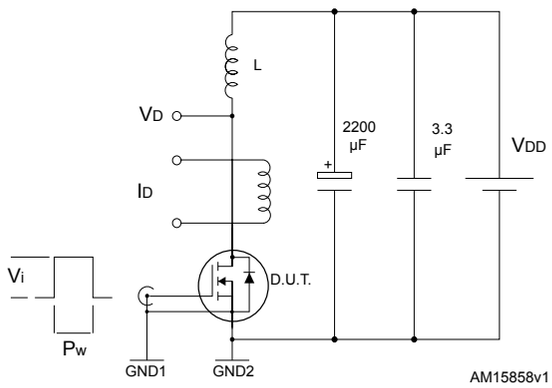


Figure 17. Unclamped inductive waveform

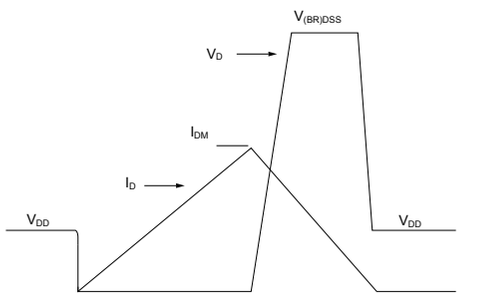
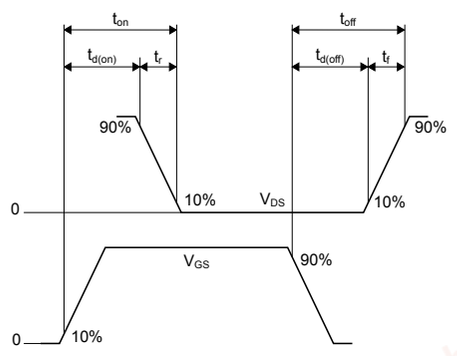


Figure 18. Switching time waveform



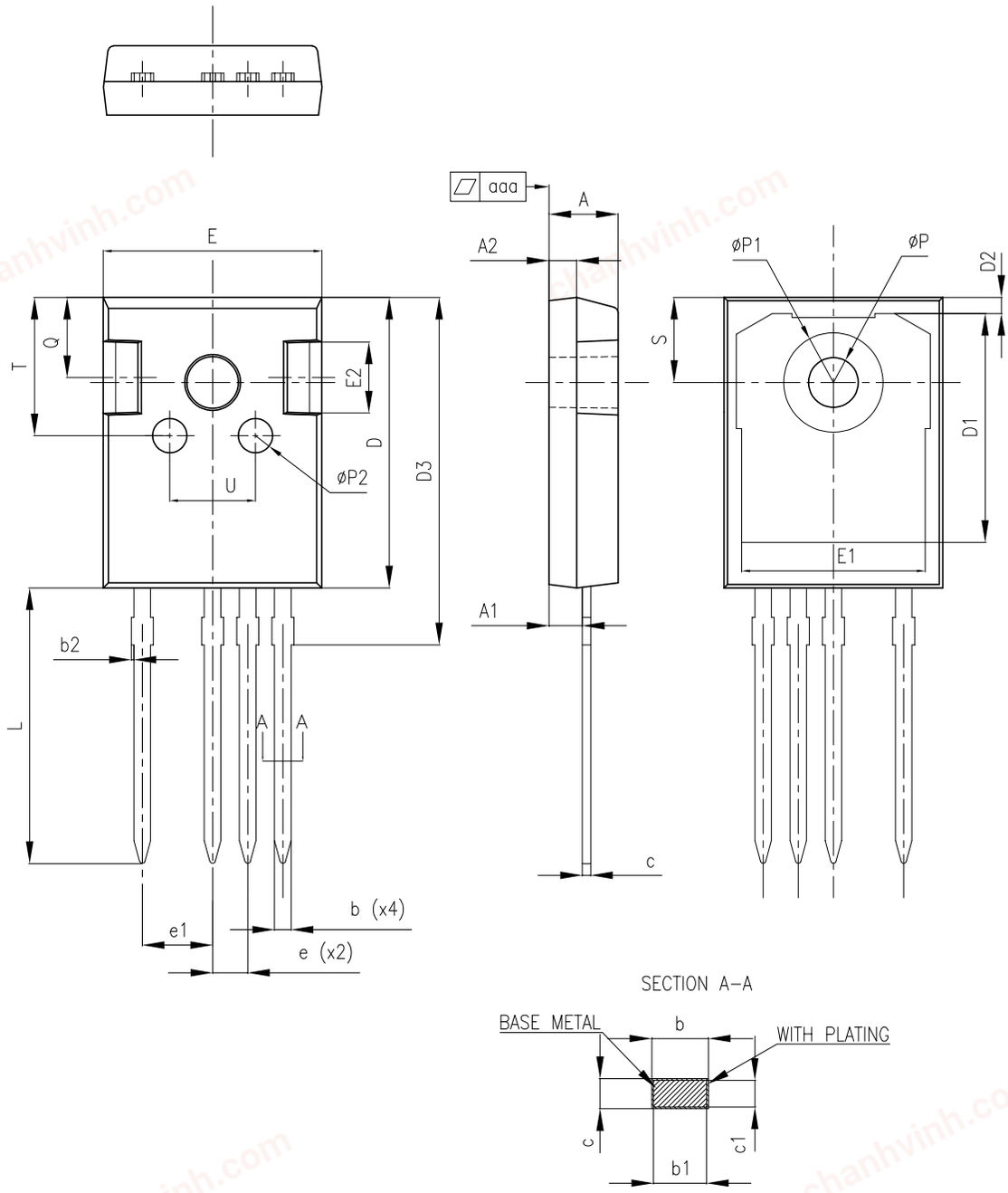
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO247-4 package information

Figure 19. TO247-4 package outline



8405626_Rev_3

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Table 8. **TO247-4 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40
aaa		0.04	0.10

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Revision history

Table 9. **Document revision history**

Date	Revision	Changes
16-May-2023	1	First release.

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