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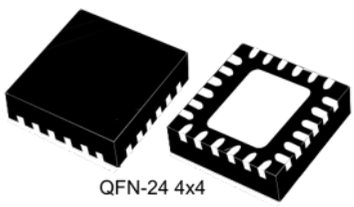
STUSB4500L

Datasheet

Standalone USB Type-C™ sink port controller



WLCSP-25 2.6x2.6



QFN-24 4x4

Product status link
STUSB4500L

Product summary	
Order code	STUSB4500LQTR
	STUSB4500LBJR
Description	Standalone USB Type-C controller (auto-run mode)
Package	QFN-24 EP (4x4)
	WLCSP-25 (2.6x2.6x0.5)
Marking	4500L

Features

- Auto-run Type-C™ sink controller
- Dead battery mode support
- Integrated V_{BUS} switch gate drivers (PMOS)
- Integrated V_{BUS} voltage monitoring
- Short-to-VBUS protections on CC pins
- High voltage capability on V_{BUS} pins
- V_{BUS} powered:
  - Zero consumption on local battery or application
  - V_{DD} = [4.1 V; 22 V]
- Temperature range: -40 °C up to 105 °C
- ESD: 3 kV HBM - 1.5 kV CDM
- Certified:
  - USB Type-C™ rev 1.4
  - Power sinking device (TID #1455)

Applications

- Printers, camcorders, cameras
- IoT, drones, accessories and battery powered devices
- Computer accessories (keyboards, mouse)
- Toys, gaming, POS, scanner, LED lighting
- Healthcare, e-cigarettes, handheld devices
- USB accessories
- 5 V DC barrel, USB STD-B and micro-B replacement
- Any 5 V Type-C sink device

Description

The STUSB4500L is a USB Type-C controller that addresses sink devices.

This device supports dead battery mode and is suited for sink devices powered from dead battery state. It is able to operate without any external software support for quick application power-on and immediate charging process start. At type-C connection, the STUSB4500L seeks CC pin for SOURCE termination and monitors V_{BUS} voltage in order to protect the application from an incorrect SOURCE operation. When V_{BUS} is within the appropriate range, the STUSB4500L powers the application by closing the input switch. The available current advertised by the SOURCE is reported to the application in order to align the sinking current. Port status can be optionally monitored by the software through I²C interface.

Thanks to its 20 V technology, it implements high voltage features to protect the CC pins against short-circuits to V_{BUS}.

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1 Functional description

The STUSB4500L is a USB Type-C™ IC controller addressing 5 V sink applications. It supports dead battery mode to allow a system to be powered from a V_{BUS} power source directly.

The STUSB4500L major role is to:

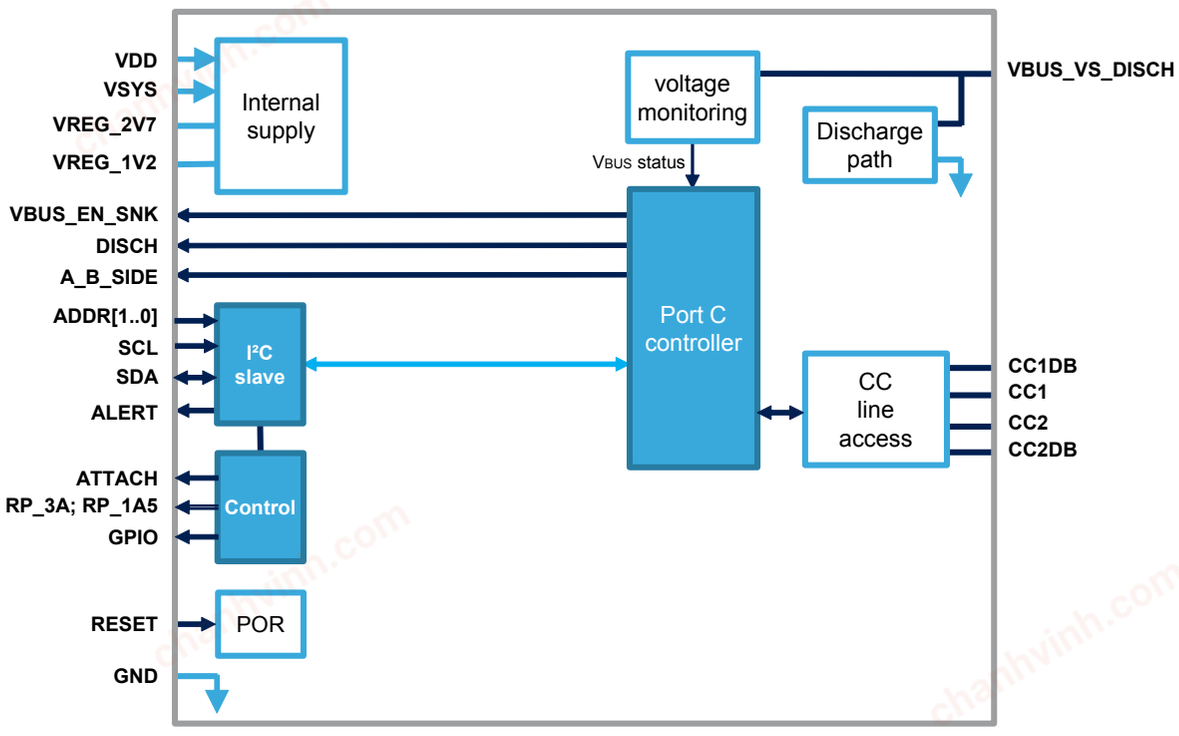
1. Detect the connection between two USB Type-C ports (attach detection)
2. Establish a valid source-to-sink connection
3. Identify the attached device: source or debug accessory
4. Resolve cable orientation and twist connections to establish USB 3 data routing (MUX control) if any
5. Configure the incoming V_{BUS} power path
6. Monitor the V_{BUS} power path
7. Report the available power advertised by the source
8. Handle the high voltage protections

The STUSB4500L also provides:

- Dead battery mode
- Internal and/or external V_{BUS} discharge paths
- Debug accessory mode detection
- Customization of the device configuration through NVM to support specific applications

1.1 Block overview

Figure 1. Functional block diagram



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2 Inputs/outputs

2.1 Pinout

Figure 2. QFN-24 pin connections (top view)

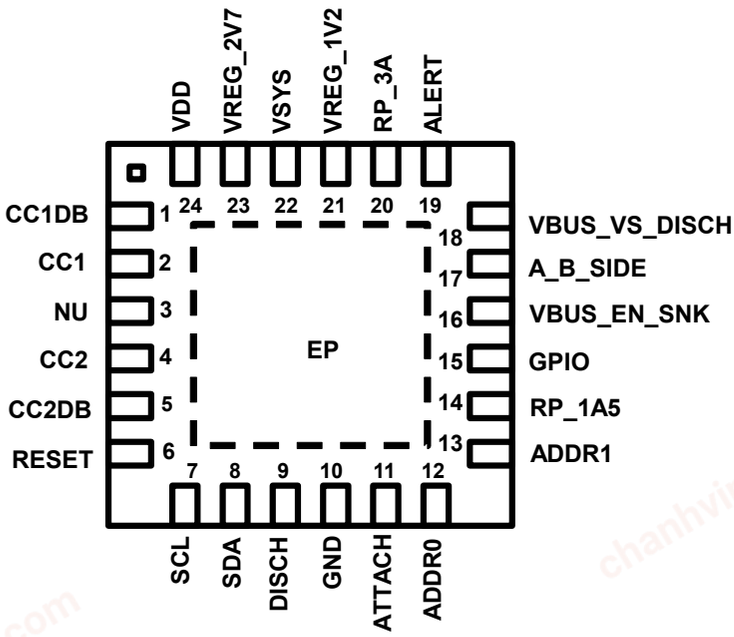
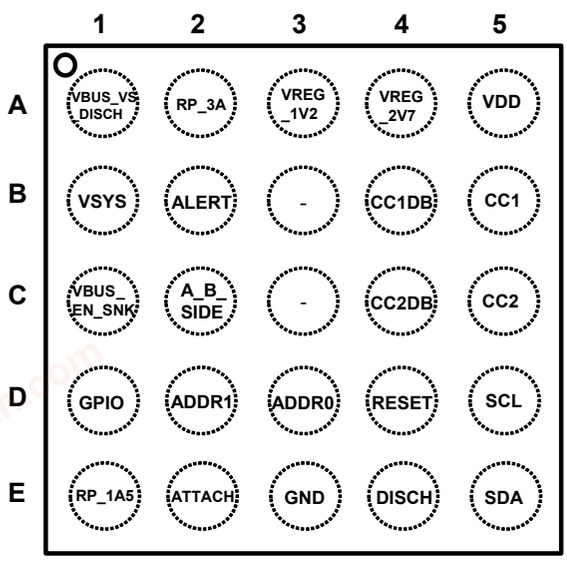


Figure 3. WLCSP-25 pin connections (top view)



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Table 1. Pin function list

QFN	CSP	Name	Type	Description	Typical connection
1	B4	CC1DB	HV AIO	Dead battery enable on CC1 pin	To CC1 pin if used or ground
2	B5	CC1	HV AIO	Type-C configuration channel 1	To Type-C receptacle A5
3	B3, C3	NU	-	-	To ground
4	C5	CC2	HV AIO	Type-C configuration channel 2	To Type-C receptacle B5
5	C4	CC2DB	HV AIO	Dead battery enable on CC2 pin	To CC2 pin if used or ground
6	D4	RESET	DI	Reset input, active high	From system
7	D5	SCL	DI	I^2C clock input	To I²C master, ext. pull-up or floating (if not used
8	E5	SDA	DI/OD	I^2C data input/output, active low open drain	To I²C master, ext. pull-up or floating (if not used
9	E4	DISCH	HV AI/OD	Internal discharge path or external discharge path enable, active low open drain	From power system (internal path) or to the discharge path switch (external path), ext. pull-up
10	E3	GND	GND	Ground	Ground
11	E2	ATTACH	OD	Attachment detection, active low open drain	To MCU if any, ext. pull-up
12	D3	ADDR0	DI	I²C device address setting	Static, to ground or ext. pull-up for address selection, to ground if no connection to MCU
13	D2	ADDR1	DI	I²C device address setting	Static, to ground or ext. pull-up for address selection, to ground if no connection to MCU
14	E1	RP_1A5	OD	1.5 A source flag, active low open drain	To power system, ext. pull-up
15	D1	GPIO	OD	General purpose output, active low open drain	To system, ext. pull-up
16	C1	VBUS_EN_SNK	HV OD	V_{BUS} sink power path enable, active low open drain	To power switch or to power system, ext. pull-up
17	C2	A_B_SIDE	OD	Cable orientation, active low open drain	USB super speed MUX select, ext. pull-up
18	A1	VBUS_VS_DISCH	HV AI	V_{BUS} voltage monitoring and discharge path	From $V_{BUS,}$ receptacle side
19	B2	ALERT	OD	I^2C interrupt, active low open drain	To I²C master, ext. pull-up
20	A2	RP_3A	HV OD	3 A source flag, active low open drain	To power switch or to power system, ext. pull-up
21	A3	VREG_1V2	PWR	1.2 V internal regulator output	1 µF typ. decoupling capacitor
22	B1	VSYS	PWR	Power supply from system	From power system, connect to ground if not used
23	A4	VREG_2V7	PWR	2.7 V internal regulator output	1 µF typ. decoupling capacitor
24	A5	VDD	HV PWR	Power supply from USB power line	From V_{BUS}, receptacle side
EP	-	EP	GND	Exposed pad is connected to ground	To ground

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Table 2. **Pin function descriptions**

Type	Description
D	Digital
A	Analog
O	Output pad
I	Input pad
IO	Bidirectional pad
OD	Open drain output
PD	Pull-down
PU	Pull-up
HV	High voltage
PWR	Power
GND	Ground

2.2 Pin description

2.2.1 CC1 / CC2

CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination. CC1 and CC2 are HiZ during reset.

2.2.2 CC1DB / CC2DB

CC1DB and CC2DB are enabled by dead battery mode by connecting CC1DB and CC2DB respectively to CC1 and CC2. Thanks to this connection, the pull-down terminations on the CC pins are present by default even if the device is not supplied (see Section 3.3 Dead battery mode).

Warning: CC1DB and CC2DB must be connected to ground when dead battery mode is not supported, then V_{sys} must be used.

2.2.3 RESET

Active high reset.

2.2.4 I²C interface pins

Table 3. **I²C interface pin list**

Name	Description
SCL	I²C clock, need external pull-up
SDA	I²C data, need external pull-up
ALERT	I²C interrupt, need external pull-up
ADDR0, ADDR1	I²C device address bits (see Section 4 I²C Interface)

Warning: ADDR0 and ADDR1 pins must be connected to ground when there is no connection to an MCU.

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2.2.5 DISCH

This input/output pin can be used to implement a discharge path for highly capacitive V_{BUS} line on power system side.

When used as input, the discharge is internal and a serial resistor must connected to the pin to limit the discharge current through the pin. Maximum discharge current is 500 mA.

The pin can be also used as an open drain output to control an external V_{BUS} discharge path when higher discharge current is required by the application, for instance.

The pin is activated at the same time as the internal discharge path on VBUS_VS_DISCH pin. The discharge is activated automatically during cable disconnection and error recovery state. The discharge time is programmable by NVM (see Section 5 Start-up configuration).

2.2.6 GND

Ground.

2.2.7 ATTACH

This pin is asserted when a valid source-to-sink connection is established. It is also asserted when a connection to a debug accessory device is detected.

2.2.8 RP_3A/RP_1A5

These pins report by default the status of the USB source current capabilities.

Table 4. Source current capability

Pin name	Value	Description
VBUS_EN_SNK	Hi-Z	No source attached
	0	Source attached
RP_3A	Hi-Z	No source attached or source supplies default USB Type-C current at 5 V
	0	Source supplies 3.0 A USB Type-C current at 5 V
RP_1A5	Hi-Z	No source attached or source supplies default USB Type-C current at 5 V.
	0	Source supplies 1.5 A USB Type-C current at 5 V.

Note: RP_3A and RP_1A5 signals are valid when a SOURCE is attached.

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2.2.9 GPIO

This pin is an active low open drain output that can be configured by NVM as per table below (see Section 5 Start-up configuration).

Table 5. GPIO pin configuration

NVM parameter GPIO_CFG[1:0]	Pin name	Pin function	Value	Description
00b	SW_CTRL_GPIO	Software controlled GPIO. The output state is defined by the value of I^2C register bit #0 at address 2Dh	Hi-Z	When bit #0 value is 0b (at start-up)
			0	When bit #0 value is 1b
01b	ERROR_RECOVERY	Hardware fault detection (see Section 3.4 Hardware fault management)	Hi-Z	No hardware fault detected
			0	Hardware fault detected
10b	DEBUG	Debug accessory detection (see Section 3.6 Debug accessory mode detection)	Hi-Z	No debug accessory detected
			0	Debug accessory detected
11b (default)	SINK_POWER	Indicates USB Type-C current capability advertised by the source	Hi-Z	Source supplies default or 1.5 A USB Type-C current at 5 V
			0	Source supplies 3.0 A USB Type-C current at 5 V

2.2.10 VBUS_EN_SNK

This pin allows the incoming V_{BUS} power from the USB Type-C receptacle to be enabled when a source is connected according to different operating conditions stated in the table below. VBUS_EN_SNK pin is a high voltage open drain output that allows a PMOS transistor to be directly driven to enable the VBUS power path.

2.2.11 A_B_SIDE

This output pin provides the cable orientation. It is used to establish USB SuperSpeed signal routing. This signal is not required in case of USB 2.0 support.

Table 6. USB data MUX select

Value	Description
HiZ	CC1 pin is attached to CC line
0	CC2 pin is attached to CC line

2.2.12 VBUS_VS_DISCH

This input pin is used to sense V_{BUS} presence, monitor V_{BUS} voltage, and discharge V_{BUS} from the USB Type-C receptacle side.

A serial resistor connected to the pin must be used to limit the discharge current through the pin. Maximum discharge current is 50 mA.

The discharge is activated automatically during cable disconnection, and error recovery state. The discharge time is programmable by NVM (see Section 5 Start-up configuration).

2.2.13 VREG_1V2

This pin is used only for external decoupling of the 1.2 V internal regulator. The recommended decoupling capacitor is: 1 µF typ. (0.5 µF min., 10 µF max.)

2.2.14 VSYS

This is the low power supply from the system, if there is any. It can be connected directly to a single cell Lithium battery or to the system power supply delivering 3.3 V up to 5 V. It is recommended to connect the pin to ground when it is not used.

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2.2.15 VREG_2V7

This pin is used only for external decoupling of the 2.7 V internal regulator. The recommended decoupling capacitor is: 1 µF typ. (0.5 µF min., 10 µF max.)

2.2.16 VDD

This is the main STUSB4500L power supply. Whatever the application is VBUS powered or not, VDD mandatory connection is to USB power line (VBUS). The STUSB4500L can indeed work in dead battery mode, even for self-powered application, in order to reduce power consumption to ZERO when the port is not attached, therefore having no impact on application power leakage.

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3 Description of the features

3.1 CC interface

The STUSB4500L controls the connection to the configuration channel (CC) pins, CC1 and CC2, through two main blocks: the CC line interface block and the CC control logic block.

The CC line interface block is used to:

- Set pull-down termination mode on the CC pins
- Monitor the CC pin voltage values related to the attachment detection thresholds
- Protect the CC pins against overvoltage

The CC control logic block is used to:

- Execute the Type-C FSM related to the sink power role with debug accessory support
- Determine the electrical state for each CC pin related to the detected thresholds
- Evaluate the conditions related to the CC pin states and the V_{BUS} voltage value to transition from one state to another in the Type-C FSM
- Advertise a valid source-to-sink connection
- Determine the identity of the attached device: source or debug accessory
- Determine cable orientation to allow external routing of the USB data
- Manage USB Type-C power capability on V_{BUS}: USB default, medium or high current mode
- Handle hardware faults

3.2 VBUS power path control

3.2.1 VBUS monitoring

The V_{BUS} monitoring block supervises from the VBUS_VS_DISCH input pin the V_{BUS} voltage on the USB Type-C receptacle side.

It is used to check that V_{BUS} is within a valid voltage range to establish a valid source-to-sink connection and to enable safely the V_{BUS} power path through the VBUS_EN_SNK pin.

It allows detection of unexpected V_{BUS} voltage conditions such as undervoltage or overvoltage related to the valid V_{BUS} voltage range. When such conditions occur, the STUSB4500L reacts as follows:

- At attachment, it prevents the source-to-sink connection to be established and the V_{BUS} power path to be asserted
- After attachment, it goes into unattached state and it disables the V_{BUS} power path

The valid V_{BUS} voltage range is defined by a low limit V_{THUSB} and a high limit $V_{MONUSBH}$ (overvoltage condition):

- V_{THUSB} low limit is fixed by hardware at 3.3 V in order to detect a V_{BUS} rising edge (connection) or falling edge (disconnection)
- The minimum value of $V_{MONUSBH}$ is V_{BUS} +5% and can be shifted by fraction of 1% from V_{BUS}+5% to V_{BUS} +20%. The value is preset by default in the NVM (see Section 7.3 Electrical and timing characteristics) and can be changed independently through NVM programming (see Section 5 Start-up configuration)

3.2.2 VBUS discharge

The monitoring block also handles the V_{BUS} discharge paths connected to the VBUS_VS_DISCH pin for the USB Type-C receptacle side and to the DISCH pin for the power system side. The discharge paths are activated at the same time when disconnection is detected or when the device goes into the error recovery state (see Section 3.4 Hardware fault management). At detachment, during error recovery state, the discharge is activated for $T_{DISUSB0V}$ time.

The discharge time durations are also preset by default in the NVM (see Section 7.3 Electrical and timing characteristics). The discharge time durations can be changed through NVM programming (see Section 5 Start-up configuration).

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The V_{BUS} discharge feature is enabled by default in the NVM and can be disabled through NVM programming (see Section 5 Start-up configuration).

3.2.3 VBUS power path assertion

The STUSB4500L can control the assertion of the V_{BUS} power path from the USB Type-C receptacle, directly or indirectly, through the VBUS_EN_SNK pin.

The table below summarizes the operating conditions that determine the electrical value of the VBUS_EN_SNK pin during system operation.

Table 7. VBUS_EN_SNK pin behavior depending on the operating conditions

Value	Operating conditions	
	Connection stage	V_{BUS} monitoring conditions on VBUS_VS_DISCH pin
0	At attachment or during operation	$V_{BUS} < V_{MONUSBH}$ and $V_{BUS} > V_{THUSB}$
Hi-Z	At detachment or during ErrorRecovery	$V_{BUS} > V_{MONUSBH}$ or $V_{BUS} < V_{THUSB}$

Type-C state column refers to the Type-C FSM states as defined in the USB Type-C standard specification.

3.3 Dead battery mode

Dead battery mode allows systems powered by a battery to be supplied by the V_{BUS} when the battery is discharged and therefore to start the battery charging process without any external support. This mode is also used in systems that are powered through the V_{BUS} only.

Dead battery mode operates only if the CC1DB and CC2DB pins are connected respectively to the CC1 and CC2 pins. Thanks to these connections, the STUSB4500L presents a pull-down termination on its CC pins and advertises itself as a sink even if the device is not supplied.

When a source system connects to a USB Type-C port, it detects the pull-down termination, establish the source-to-sink connection, and provide the V_{BUS}. The STUSB4500L is then supplied thanks to the VDD pin connected to V_{BUS} on the USB Type-C receptacle side. The STUSB4500L can finalize the connection and enable the power path on V_{BUS} thanks to the VBUS_EN_SNK pin to allow the system to be powered.

3.4 Hardware fault management

During system operation, the STUSB4500L handles some pre-identified hardware fault conditions. When such conditions happen, the circuit goes into an ErrorRecovery state as defined in the USB Type-C standard specifications.

The error recovery state is equivalent to force a detach event. When entering this state, the device de-asserts the V_{BUS} power path by disabling the VBUS_EN_SNK, RP_3A and RP_1A5 pins, and it removes the terminations from the CC pins. Then, it transitions to the unattached state.

The STUSB4500L goes into error recovery state when at least one condition listed below is met:

- If an overtemperature is detected (junction temperature above maximum T_J)
- If an overvoltage is detected on the CC pins (voltage on CC pins above V_{OVP})

The detection of a hardware fault is advertised through the GPIO pin when configured in ERROR_RECOVERY mode.

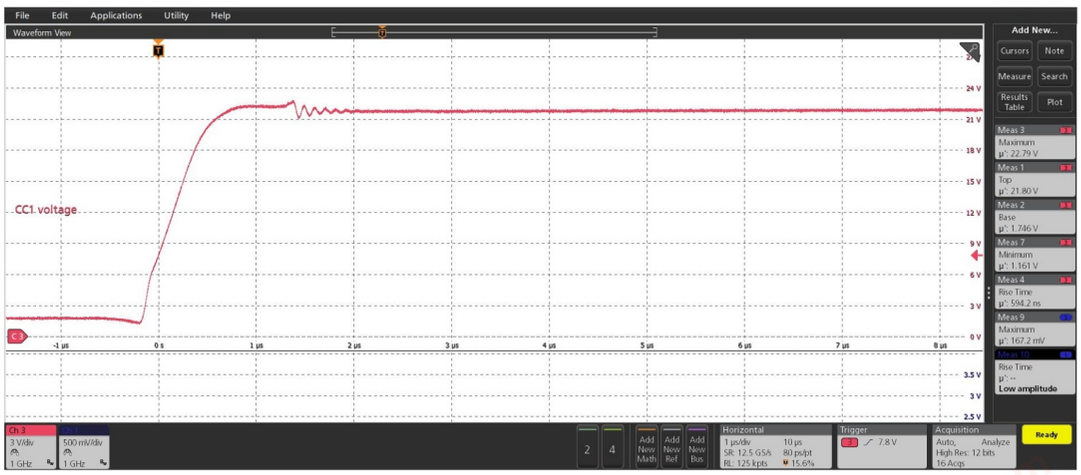
See Section 7 Electrical characteristics for threshold values.

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3.5 High voltage protections

The STUSB4500L can be used in systems or connected to systems that handle high voltage on the V_{BUS} power path. The device integrates an internal circuitry on the CC pins that tolerates high voltage and ensures protection up to 22 V in case of unexpected short-circuits with the V_{BUS} as per figure below.

Figure 4. Short-to-V_{BUS}



3.6 Debug accessory mode detection

The STUSB4500L detects a connection to a debug and test system (DTS) as defined in the USB Type-C standard specification. The debug accessory detection is advertised through the GPIO pin when configured in DEBUG mode.

A debug accessory device is detected when both the CC1 and CC2 pins are pulled up by an R_p resistor from the connected device. The voltage levels on the CC1 and CC2 pins give the orientation and current capability as described in the table below. The GPIO pin configured in DEBUG mode is asserted to advertise the DTS detection and the A_B_SIDE pin indicates the orientation of the connection.

Table 8. Orientation and current capability detection in sink power role

#	CC1 pin (CC2 pin)	CC2 pin (CC1 pin)	Charging current configuration	A_B_SIDE pin CC1/CC2 (CC2/CC1)
1	R_p 3 A	R_p 1.5 A	Default	Hi-Z (0)
2	R_p 1.5 A	R_p default	1.5 A	Hi-Z (0)
3	R_p 3 A	R_p default	3.0 A	Hi-Z (0)
4	R_p def/1.5 A/3 A	R_p def/1.5 A/3 A	Default	Hi-Z (Hi-Z)

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4 I²C Interface

4.1 Read and write operations

The I²C interface is used to configure, control and read the operation status of the device. It is compatible with the Philips I²C Bus® (version 2.1). The I²C is a slave serial interface based on two signals:

- SCL - serial clock line: input clock used to shift data
- SDA - serial data line: input/output bidirectional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity.

The bidirectional data line supports transfers up to 400 Kbit/s (fast mode). The data are shifted to and from the chip on the SDA line, MSB first.

The first bit must be high (START) followed by the 7-bit device address and the read/write control bit.

Four 7-bit device address are available for the STUSB4500 thanks to the external programming of DevADDR0 and DevADDR1 bits through ADDR0 and ADDR1 pins setting i.e. 0x28 or 0x29 or 0x2A or 0x2B. It allows four STUSB4500 devices to be connected on the same I²C bus.

Table 9. Device address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DevADDR6	DevADDR5	DevADDR4	DevADDR3	DevADDR2	DevADDR1	DevADDR0	R/W
0	1	0	1	0	ADDR1	ADDR0	0/1

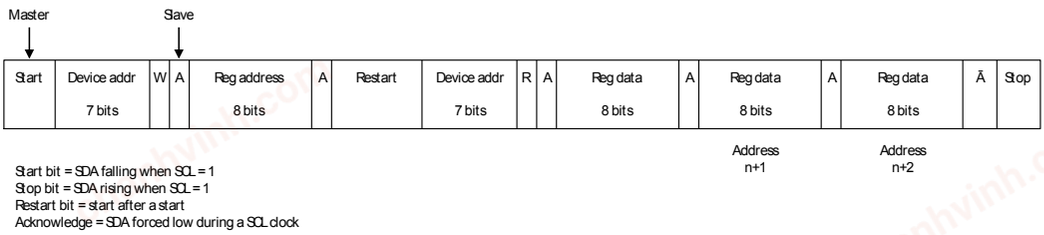
Table 10. Register address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RegADDR7	RegADDR6	RegADDR5	RegADDR4	RegADDR3	RegADDR2	RegADDR1	RegADDR0

Table 11. Register data format

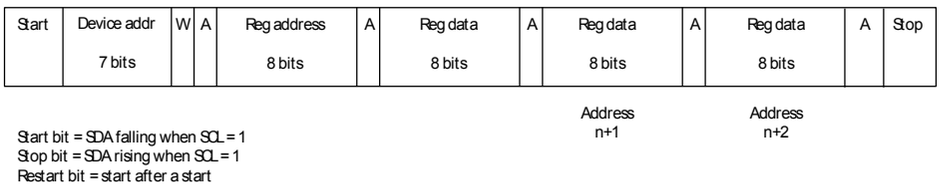
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 5. Read operation



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Figure 6. **Write operation**



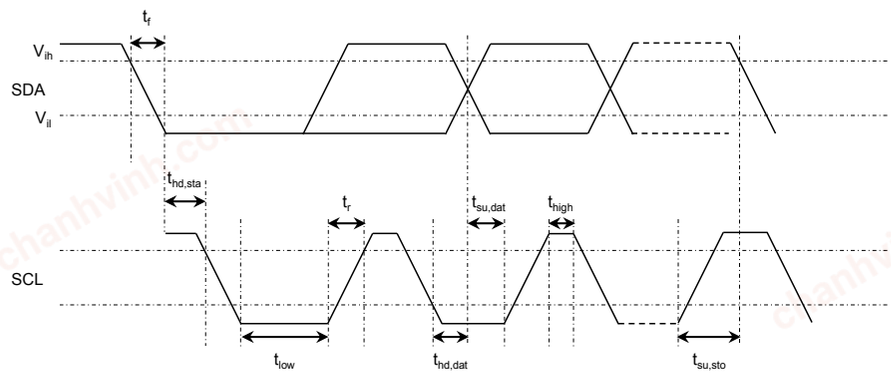
4.2 Timing specifications

The device uses a standard slave I²C channel at speed up to 400 kHz.

Table 12. **I²C timing parameters - VDD = 5 V**

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{scl}	SCL clock frequency	0	-	400	kHz
$t_{hd,sta}$	Hold time (repeated) START condition	0.6		-	µs
t_{low}	LOW period of the SCL clock	1.3		-	
t_{high}	HIGH period of the SCL clock	0.6		-	
$t_{su,dat}$	Setup time for repeated START condition	0.6		-	
$t_{hd,dat}$	Data hold time	0.04		0.9	
$t_{su,dat}$	Data setup time	100		-	
t_r	Rise time of both SDA and SCL signals	20 + 0.1 C_b		300	ns
t_f	Fall time of both SDA and SCL signals	20 + 0.1 C_b		300	
$t_{su,sto}$	Set-up time for STOP condition	0.6		-	µs
t_{buf}	Bus free time between a STOP and START condition	1.3		-	
C_b	Capacitive load for each bus line	-		400	pF

Figure 7. **I²C timing diagram**



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5 Start-up configuration

5.1 User-defined parameters

The STUSB4500L has a set of user-defined parameters that can be customized by NVM re-programming through the I^2C interface. This feature allows the customer to change the preset configuration of the USB Type-C interface and to define a new configuration to meet specific application requirements addressing various use cases, or specific implementations.

The NVM re-programming overrides the initial default setting to define a new default setting that is used at power-up or after a reset. The default setting is copied at power-up, or after a reset, from the embedded NVM into I^2C registers. The values copied in the I^2C registers are used by the STUSB4500L during the system operation.

The NVM re-programming is possible with a customer password. The I^2C registers must be re-initialized after each NVM re-programming to make effective the new parameters setting either through power-off and power-up sequence, or through reset.

5.2 Default start-up configuration

The table below lists the user-defined parameters and indicates the default start-up configuration of the STUSB4500L.

Table 13. STUSB4500L user-defined parameters and default settings

Parameter name	Parameter description	Reset value (default)	Value	Description
SHIFT_VBUS_HIGH_LIMIT	Coefficient to shift up nominal V_{BUS} high voltage limit applicable to 5 V	1010b (10%)	0000b to 1111b	0% ≤ V_{SHUSBH} ≤ 15% of VBUS by increment of 1% Default V_{SHUSBH} = 10%
VBUS_DISCH_TIME_TO_0V	Coefficient used to compute V_{BUS} discharge time to 0 V	1001b (9)	0001b to 1111b	1 ≤ $T_{DISPAR0V}$ ≤ 15 by increment of 1 Unit discharge time: 84 ms (typ.) Default coefficient $T_{DISPAR0V}$ = 9, discharge time $T_{DISUSB0V}$= 756 ms
VBUS_DISCH_DISABLE	VBUSdischarge deactivation on VBUS_VS_DISCH and DISCH pins	0b	0b	V_{BUS} discharge enabled
			1b	V_{BUS} discharge disabled
GPIO_CFG[1:0]	Selects GPIO pin configuration (see Section 2.2.9 GPIO)	11b	00b	SW_CTRL_GPIO
			01b	ERROR_RECOVERY
			10b	DEBUG
			11b	SINK_POWER (default)

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6 Application

The sections below are not part of the ST product specifications. They are intended to give a generic application overview to be used by the customer as a starting point for further implementation and customization. ST does not warrant compliance with customer specifications. Full system implementation and validation are under the customer's responsibility.

6.1 General information

6.1.1 Power supplies

The STUSB4500L can be supplied in three different ways depending on the targeted application:

- Through the VDD pin only for applications powered by V_{BUS} that operate with dead battery mode support
- Through the VSYS pin only for AC powered applications with a system power supply delivering from 3.3 V up to 5 V
- Through the VDD and VSYS pins either for applications powered by a battery with dead battery mode support or for applications powered by V_{BUS} with a system power supply delivering 3.3 V or 5 V. When both VDD and VSYS power supplies are present, the low power supply VSYS is selected when VSYS voltage is above 3.1 V. Otherwise VDD is selected

When possible, please prefer VDD supply only, and connect it to VBUS in order to minimize application power consumption. In this case, VSYS is not used and must be connected to GND.

6.1.2 Connection to MCU or application processor

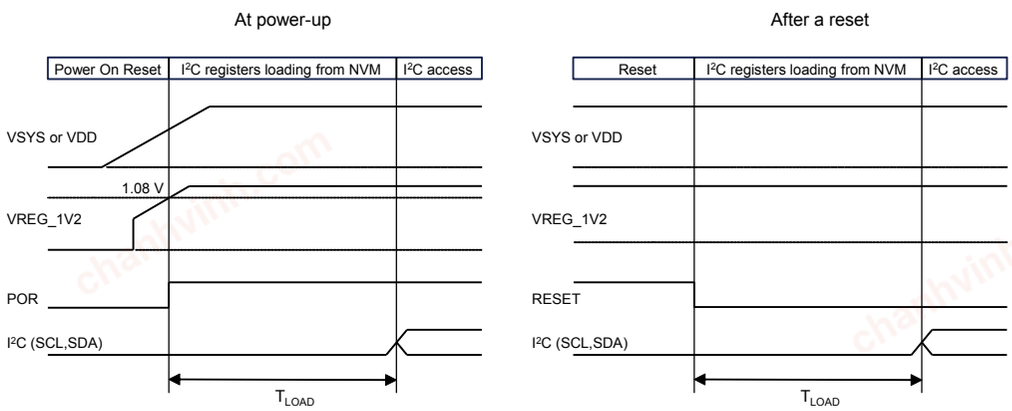
The STUSB4500L connection to an MCU or an application processor is optional. However, an I²C interface with an interrupt allows a simple connection to most of MCU and SOC of the market.

When a connection through the I²C interface is implemented, it provides an extensive functionality during the system operation. For instance, it may be used to:

1. Define the port configuration during system boot (in case the NVM parameters are not customized during manufacturing)
2. Provide a diagnostic of the Type-C connection in real time

At power-up or after a reset, the first software access to the I²C registers of the STUSB4500L can be done only after T_{LOAD} as shown in the figure below. T_{LOAD} corresponds to the time required to initialize the I²C registers with the default values from the embedded NVM. At power-up, the loading phase starts when the voltage level on the VREG_1V2 output pin of the 1.2 V internal regulator reaches 1.08 V to release the internal POR signal. After a reset, the loading phase starts when the signal on the RESET pin is released.

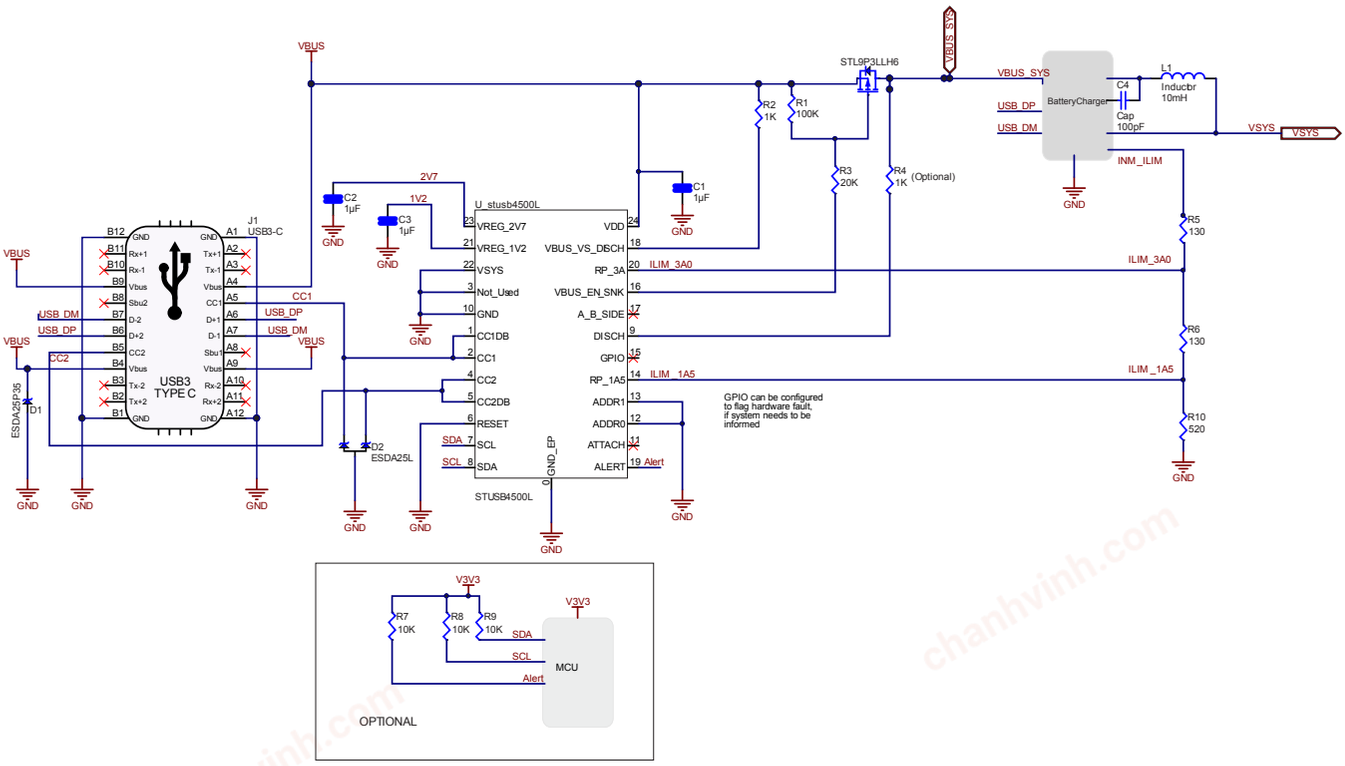
Figure 8. I²C register initialization sequence at power-up or after a reset



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6.2 Typical application

Figure 9. **Implementation example**



Note: The STUSB4500L can be connected to an application processor using I²C interface. This connection is optional.

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7 Electrical characteristics

7.1 Absolute maximum ratings

All voltages are referenced to GND.

Table 14. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage on VDD pin	28	V
V_{SYS}	Supply voltage on VSYS pin	6	
V_{CC1}, V_{CC2} V_{CC1DB}, V_{CC2DB}	High voltage on CC pins	22	
$V_{VBUS_EN_SNK}$ $V_{VBUS_VS_DISCH}$ V_{DISCH} V_{RP_3A}	High voltage on V_{BUS} pins	28	
V_{SCL}, V_{SDA} V_{ALERT} V_{RESET} V_{ATTACH} $V_{A_B_SIDE}$ V_{RP_1A5} V_{GPIO} V_{ADDR0}, V_{ADDR1}	Operating voltage on I/O pins	-0.3 to 6	
T_{STG}	Storage temperature	-55 to 150	°C
T_J	Maximum junction temperature	145	
ESD	HBM	3	kV
	CDM	1.5	

7.2 Operating conditions

Table 15. Operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage on VDD pin	3.3 to 6	V
V_{SYS}	Supply voltage on VSYS pin	3.0 to 5.5	
V_{CC1}, V_{CC2} V_{CC1DB}, V_{CC2DB}	CC pins	0 to 5.5	
$V_{VBUS_EN_SNK}$ $V_{VBUS_VS_DISCH}$ V_{DISCH}	High voltage pins	0 to 22	

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Symbol	Parameter	Value	Unit
V_{RP_3A}			V
V_{SCL}, V_{SDA} V_{ALERT} V_{RESET} V_{ATTACH} $V_{A_B_SIDE}$ V_{RP_1A5} V_{GPIO} V_{ADDR0}, V_{ADDR1}	Operating voltage on I/O pins	0 to 4.5	
T_A	Operating temperature	-40 to 105	°C

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7.3 Electrical and timing characteristics

Unless otherwise specified: V_{DD} = 5 V, T_A = 25 °C, all voltages are referenced to GND.

Table 16. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DD\ (SNK)}$	Current consumption	Device connected to VBUS V_{DD} @ VBUS level	110	160	210	µA
T_{LOAD}	I^2C registers loading time from NVM	At power-up or after a reset			30	ms
CC1 and CC2 pins						
R_d	CC pull-down resistors	-40 °C < T_A < +105 °C	-10%	5.1	+10%	kΩ
R_{INCC}	CC input impedance	Terminations off	200			kΩ
$V_{TH0.2}$	Detection threshold 1	Min. I_{P-USB} detection by sink on R_d, min CC voltage for connected sink	0.15	0.20	0.25	V
$V_{TH0.66}$	Detection threshold 2	Min. $I_{P_1.5}$ detection by sink on R_d	0.61	0.66	0.71	V
$V_{TH1.23}$	Detection threshold 3	Min. $I_{P_3.0}$ detection by sink on Rd	1.16	1.23	1.31	V
$V_{TH2.6}$	Detection threshold 4	Max. CC voltage for connected sink	2.45	2.60	2.75	V
V_{OVP}	Overvoltage protection on CC pins		5.82	6	6.18	V
VBUS_VS_DISCH pin monitoring and driving						
V_{THUSB}	V_{BUS} disconnection threshold	V_{DD}@ 5 V	3.2	3.3	3.4	V
I_{DISUSB}	V_{BUS} discharge current	Through external resistor connected to VBUS_VS_DISCH pin			50	mA
$T_{DISUSB0V}$	V_{BUS} discharge time to 0 V	At detachment, during error recovery state. Coefficient $T_{DISPAR0V}$ programmable by NVM, Default $T_{DISPAR0V}$ = 9, $T_{DISUSB0V}$ = 756 ms	70 *$T_{DISPAR0V}$	84 *$T_{DISPAR0V}$	100 *$T_{DISPAR0V}$	ms
$V_{MONUSBH}$	V_{BUS} monitoring high voltage limit	V_{BUS}+5% is nominal high voltage limit, Shift coefficient V_{SHUSBH} is programmable by NVM from 0% to 15% of V_{BUS} by step of 1% Default V_{SHUSBH} = 10%, $V_{MONUSBH}$ = V_{BUS} +15%		V_{BUS}+5% +V_{SHUSBH}		V
DISCH pin driving						
I_{DISPWR}	Power system discharge current	Through external resistor connected to DISCH pin			500	mA
Digital input/output (SCL, SDA, ALERT, RESET, ATTACH, A_B_SIDE, RP_1A5, GPIO, ADDR0, ADDR1)						
V_{IH}	High level input voltage		1.2			V
V_{IL}	Low level input voltage				0.35	V
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
20 V open drain outputs (VBUS_EN_SNK, DISCH, RP_3A)						
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V

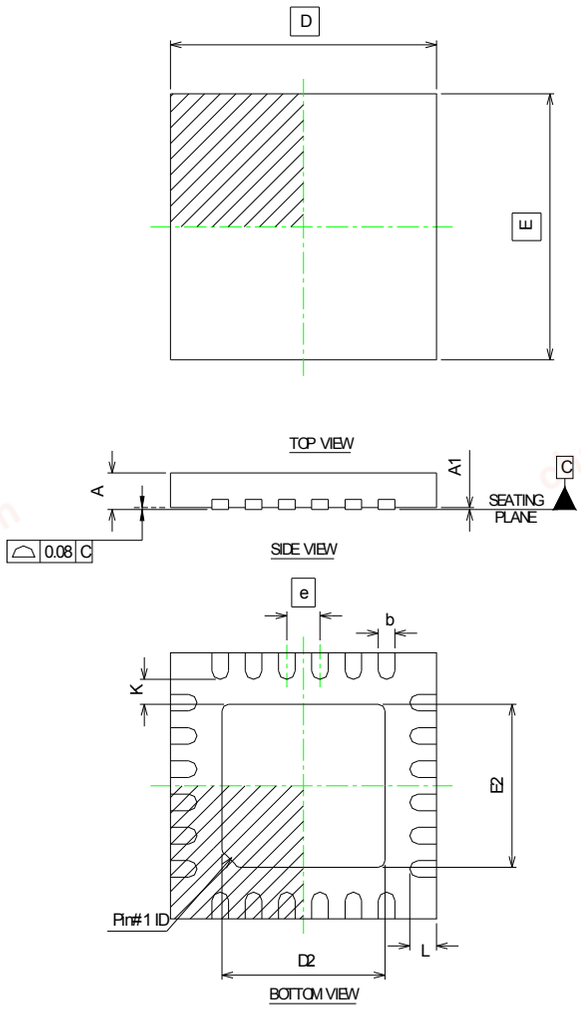
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8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 QFN-24 EP (4x4) package information

Figure 10. QFN-24 EP (4x4) package information

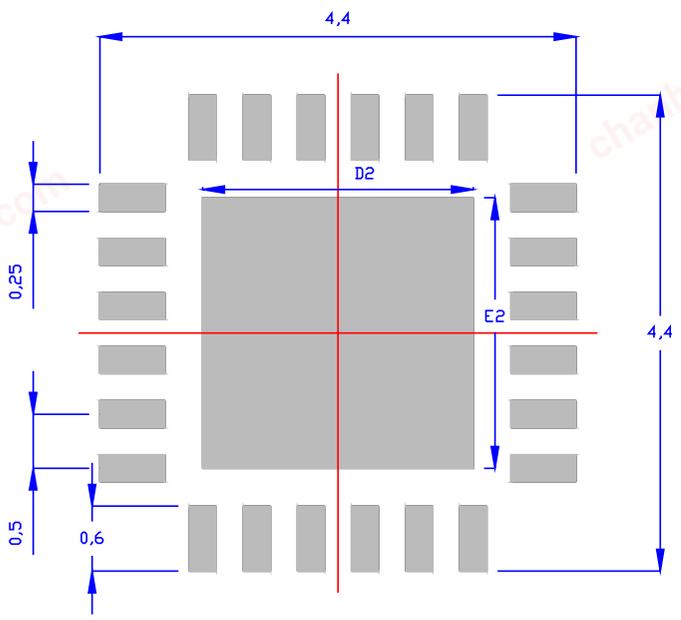


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Table 17. **QFN-24 EP (4x4) package mechanical data**

Ref.	mm			Inches		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.0010	0.012
D	3.95	4.00	4.05	0.156	0.157	0.159
D2	2.55	2.70	2.80	0.100	0.106	0.110
E	3.95	4.00	4.05	0.156	0.157	0.159
E2	2.55	2.70	2.80	0.100	0.106	0.110
e	0.45	0.50	0.55	0.018	0.020	0.022
K	0.15	-	-	0.006	-	-
L	0.30	0.40	0.50	0.012	0.016	0.020

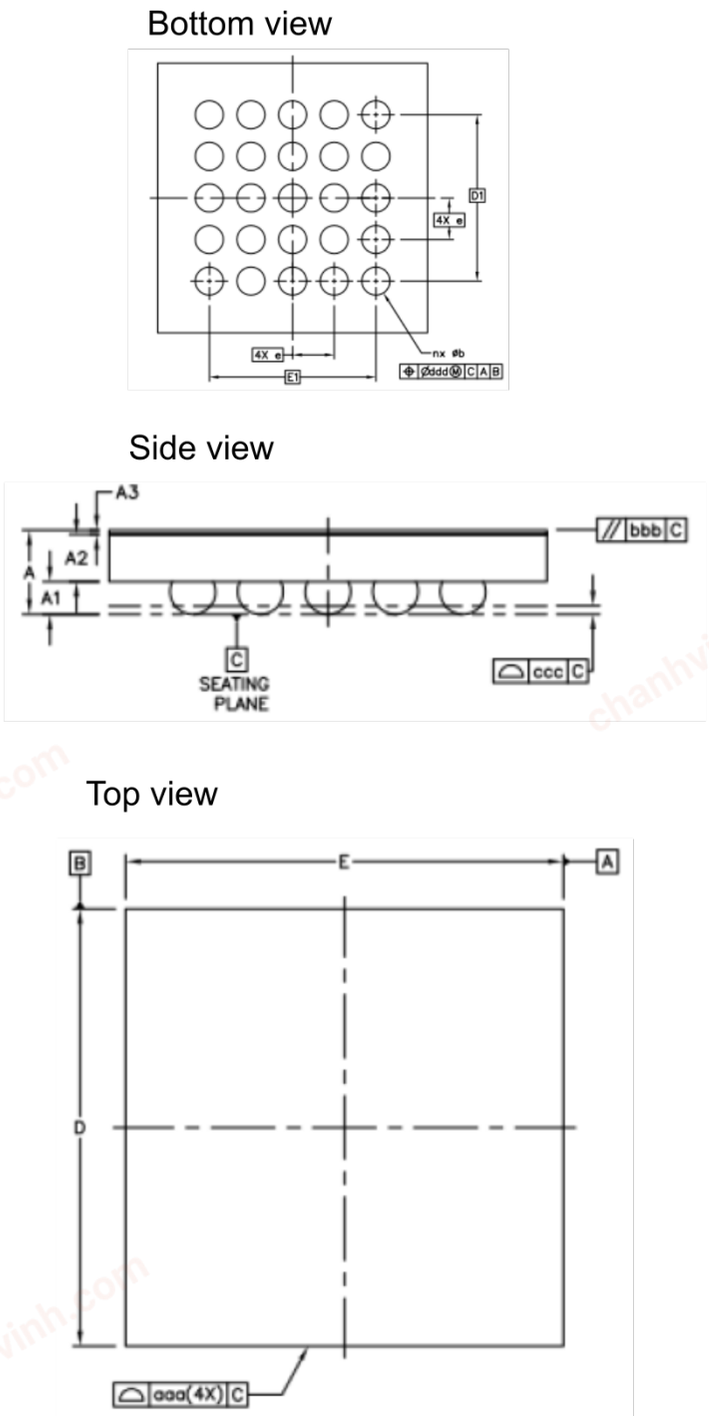
Figure 11. **QFN-24 EP (4x4) recommended footprint**



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8.2 WLCSP (2.6x2.6x0.5) 25 bumps package information

Figure 12. **WLCSP (2.6x2.6x0.5) package outline**



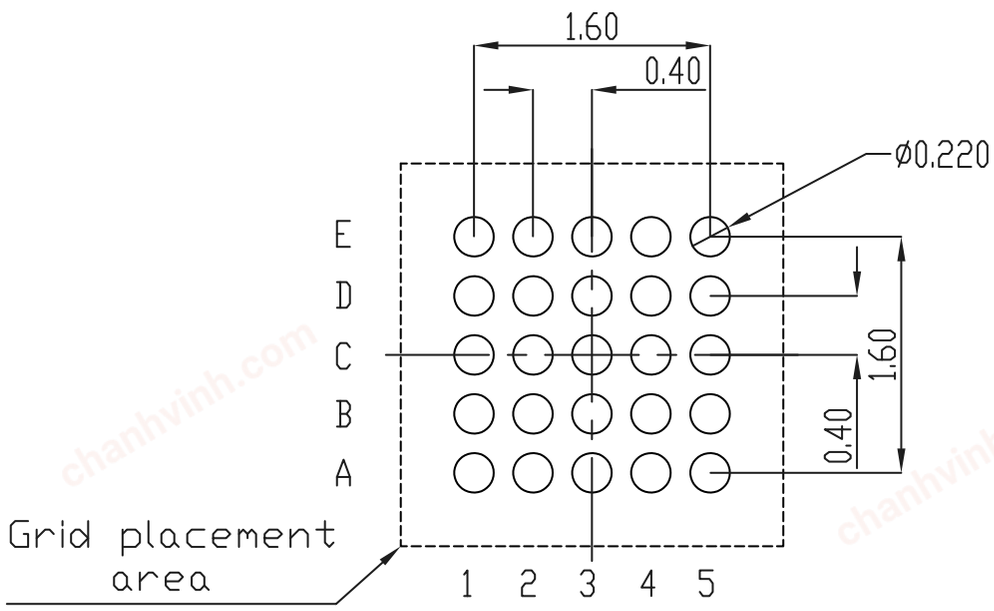
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Table 18. **WLCSP (2.6x2.6x0.5) package mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	0.456	0.50	0.544
A1	0.179	195	0.211
A2	0.255	0.28	0.305
A3	0.022	0.025	0.028
E	2.563	2.593	2.623
D	2.563	2.593	2.623
E1	1.6 BSC		
D1	1.6 BSC		
e	0.4 BSC		
b	0.245		0.295
n	25		
Tolerance of form and position			
aaa	0.03		
bbb	0.06		
ccc	0.05		
ddd	0.015		

Note: WLCSP stands for wafer level chip scale package. The typical ball diameter before mounting is 0.25 mm. The terminal A1 corner must be identified on the top surface by using a laser marking dot.

Figure 13. **WLCSP (2.6x2.6x0.5) recommended footprint**



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8.3 Thermal information

Table 19. **Thermal information**

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	5	

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9 Terms and abbreviations

Table 20. List of terms and abbreviations

Term	Description
Accessory mode	Debug accessory mode. It is defined by the presence of pull-up resistors R_p/R_p on CC1/CC2 pins in sink power role.
DFP	Downstream facing port, specifically associated with the flow of data in a USB connection. Typically the ports on a HOST or the ports on a hub to which devices are connected. In its initial state, the DFP sources V_{BUS} and optionally V_{CONN}, and supports data.
DRP	Dual-role port. A port that can operate as either a source or a sink. The port role may be changed dynamically.
Sink	Port asserting R_d on the CC pins and consuming power from the V_{BUS}.
Source	Port asserting R_p on the CC pins and providing power over the V_{BUS}.
UFP	Upstream facing port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks V_{BUS} and supports data.

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Revision history

Table 21. **Document revision history**

Date	Revision	Changes
10-Oct-2019	1	Initial release.
22-Oct-2019	2	Added Figure 13. WLCSP (2.6x2.6x0.5) recommended footprint.
29-Apr-2020	3	Added Section 3.5 High voltage protections.

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