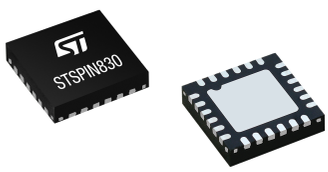
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STSPIN830

Datasheet

Compact and versatile three-phase and three-sense motor driver



Features

- Operating voltage from 7 to 45 V
- Maximum output current 1.5 A_{rms}
- R_{DSon} HS + LS = 1 Ω typ.
- Supporting both single and three shunts architectures
- Current control with adjustable OFF time
- Current sensing based on external shunt resistors
- Flexible driving methodology user settable between 6 inputs (high side & low side driving) and 3 inputs (direct PWM driving)
- FOC compatible thanks to three shunts sensing topology support
- Full protections set:
  - Non-dissipative overcurrent protection
  - Short-circuit protection
  - Underuoltage Lockout
  - Thermal shutdown
  - Interlocking function
- Low standby current consumption

Application

- Industrial robotics
- Medical and health care
- Factory automation end-points
- Home appliances
- Small pumps
- Server, computing and general purpose FANs
- Office and home automation

Product status link
STSPIN830

Product summary	
Order code	STSPIN830
Package	TFQFPN 4 x 4 x 1.05 - 24L
Packing	Tape and reel

Product label

SUSTAINABLE TECHNOLOGY

Description

STSPIN830 is a compact and versatile field oriented control FOC ready three-phase motor driver. It integrates in a very small 4 x 4 mm QFN package, both the control logic and a fully protected low R_{DSon} triple half-bridge power stage.Thanks to a dedicated MODE input pin the device offers the freedom to decide whether to drive it through 6 inputs (one for each power switch) or a more common 3 PWM direct driving inputs.

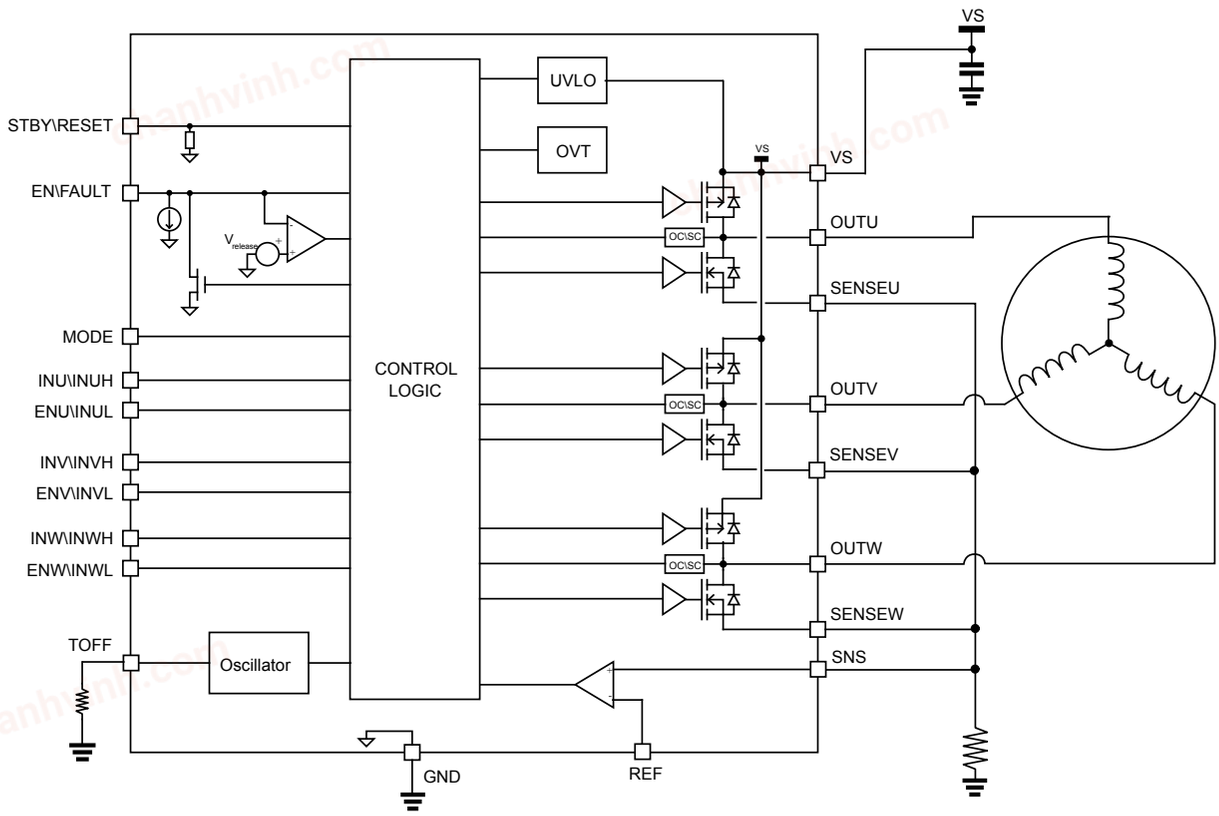
The STSPIN830 supports both single and three shunts architectures and embeds a PWM current limiter based on user settable values of reference voltage and OFF time.The devices can be forced in a low consumption state reducing the total current consumption down to less than 45 µA.

As with all other devices from the STSPIN family, the STSPIN830 integrates a complete set of protections for the power stages (non-dissipative overcurrent, thermal shutdown, short-circuit, undervoltage lockout and interlocking) making it a bulletproof solution for the new wave of demanding industrial applications.

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1 Block diagram

Figure 1. **STSPIN830 block diagram**



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2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Supply voltage	-0.3 to 48	V
V_{IN}	Logic input voltage	-0.3 to 5.5	V
$V_{OUT,diff}$	Differential voltage between VSx, OUTU, OUTV, OUTW and SENSEx pins	up to 48	V
V_{SENSE}	Sense pins voltage(1)	-2 to 2	V
V_{REF}	Reference voltage input	-0.3 to 2	V
$I_{OUT,RMS}$	Continuous power stage output current (each bridge)	1.5	A_{rms}
T_j	Junction temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. *SENSEU, SENSEV, SENSEW, SNS.*

2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_S	Supply voltage	7	-	45	V
V_{IN}	Logic input voltage		-	5	V
V_{SENSE}	Sense pins voltage	-1	-	+1	V
V_{REF}	Reference voltage input	0.1	-	1	V
f_{SW}	Switching frequency			400	kHz

2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Conditions	Value	Unit
R_{thJA}	Junction-to-ambient thermal resistance	Natural convection, according to JESD51-2a 1	36.5	°C/W
$R_{thJCtop}$	Junction-to-case thermal resistance (top side)	Cold plate on top package, according to JESD51-121	27.6	°C/W
$R_{thJCbot}$	Junction-to-case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-121	5.9	°C/W
R_{thJB}	Junction-to-board thermal resistance	according to JESD51-81	13.6	°C/W
Ψ_{JT}	Junction-to-top characterization	According to JESD51-2a1	1	°C/W
Ψ_{JB}	Junction-to-board characterization	According to JESD51-2a1	13.7	°C/W

1. *Simulated on a 76.2 x 114.3 x 1.6 mm, with vias underneath the component, 2s2p board as per standard Jedec (JESD51-7) in natural convection.*

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2.4 ESD protection ratings

Table 4. **ESD protection ratings**

Symbol	Parameter	Conditions	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS001	H2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS002 All pins	C2a	500	V
		Conforming to ANSI/ESDA/JEDEC JS002 Corner pins only (1, 6, 7, 12, 13, 18, 19, 24)	-	750	V
MM	Machine model	Conforming to EIA/JESD22-A115-C	NC	200	V

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3 Electrical characteristics

Testing conditions: V_S = 36 V, T_j = 25 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
General						
$V_{Sth(ON)}$	V_S turn-on threshold	V_S rising from 0 V		6.0	6.5	V
$V_{Sth(HYST)}$	V_S turn-off threshold hysteresis	V_S falling from 7 V		0.4		V
I_S	V_S supply current	No commutations EN = '0' R_{TOFF} = 10 kΩ		2.3	2.7	mA
		No commutations EN = '1' R_{TOFF} = 10 kΩ		2.7	3	mA
V_{STBYL}	Standby low voltage				0.8	V
V_{STBYH}	Standby high voltage		2			V
$I_{S, STBY}$	V_S supply standby current	STBY = 0 V			45	µA
Power stage						
$R_{DSon\ HS+LS}$	Total on resistance HS + LS	V_S = 21 V I_{OUT} = 1 A		1	1.3	Ω
		V_S = 21 V I_{OUT} = 1 A T_j = 150 °C (1)		1.4	1.6	
I_{DSS}	Output leakage current	OUTx = V_S= 48 V			20	µA
		OUTx = -0.3 V	-1			
V_{DF}	Freewheeling diode forward voltage	I_D = TBD A		1		V
t_{rise}	Rise time	V_S = 21 V		120		ns
t_{fall}	Fall time	V_S = 21 V		60		ns
Logic IO						
V_{IH}	High logic level input voltage		2			V
V_{IL}	Low logic level input voltage				0.8	V
V_{OL}	Low logic level output voltage	I_{OL} = 4 mA			0.3	V
$V_{RELEASE}$	FAULT open-drain release voltage				0.6	V
R_{STBY}	STBY pull-down resistance			60		kΩ
I_{PDEN}	Enable pull-down current			5		µA
t_{ENd}	EN input propagation delay	From EN falling edge to OUT high impedance		400		ns
$t_{INd(ON)}$	Turn-on propagation delay	From INxH rising edge to 10% of OUTx		450		ns

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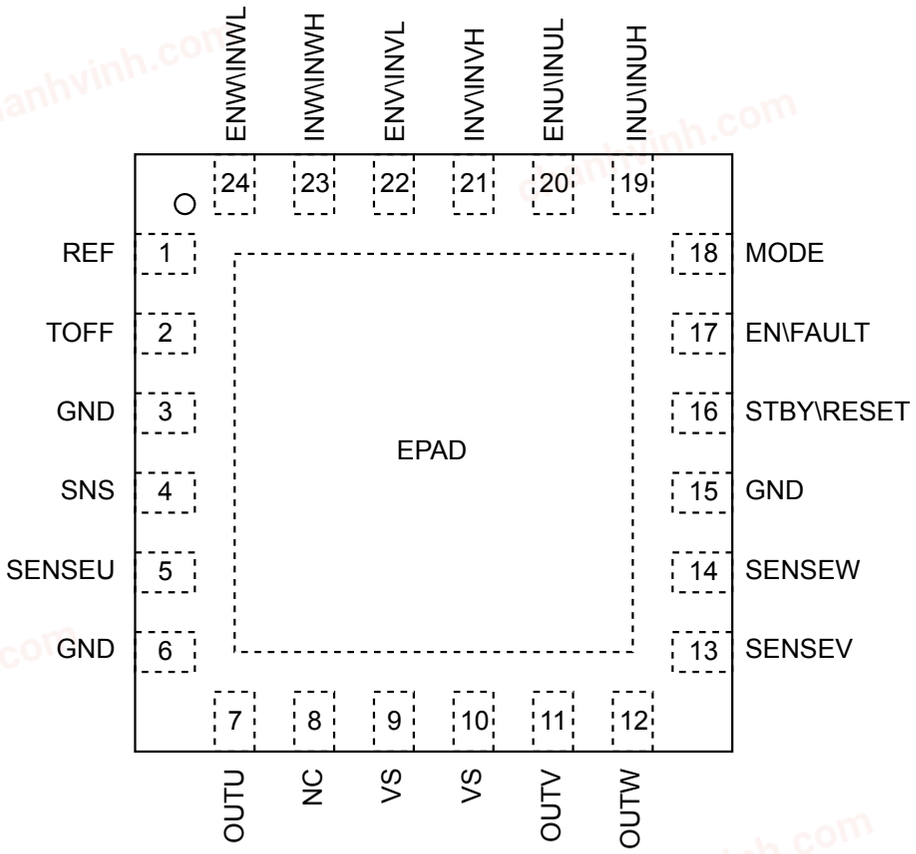
Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$t_{INd(OFF)}$	Turn-off propagation delay	From INxL rising edge to 90% of OUTx		250		ns
PWM current control						
$V_{SNS,OFFSET}$	Current control offset		-15		15	mV
t_{OFF}	Total OFF time	R_{OFF} = 10 kΩ		13		µs
		R_{OFF} = 160 kΩ		146		µs
Δt_{OFF}	OFF time precision	Full temperature range (1)	20%		+20%	%
$t_{OFF,jitter}$	Total OFF time jittering			±2%		
Protections						
T_{jSD}	Thermal shutdown threshold			160		°C
$T_{jSD,Hyst}$	Thermal shutdown hysteresis			40		°C
I_{OC}	Overcurrent threshold			3	3.5	A

1. *Based on characterization data on a limited number of samples, not tested during production.*

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4 Pin description

Figure 2. **Pin connection (top view)**



Note: the exposed pad must be connected to ground.

Table 6. **Pin description**

N.	Name	Type	Function
1	REF	Analog input	Reference voltage for the PWM current control circuitry
2	TOFF	Analog input	Internal oscillator frequency adjustment
3, 6, 15	GND	Ground	Device ground
4	SNS	Analog input	Current limiter sense input
5	SENSEU	Power output	Sense output of the bridge U
7	OUTU	Power output	Power bridge output U
9	VS	Supply	Device supply voltage
10	VS	Supply	Device supply voltage
11	OUTV	Power output	Power bridge output V
12	OUTW	Power output	Power bridge output W
13	SENSEV	Power output	Sense output of the bridge V
14	SENSEW	Power output	Sense output of the bridge W

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N.	Name	Type	Function
16	STBY\RESET	Logic input	Standby\Reset input When forced low the device enters in low consumption mode
17	EN\FAULT	Logic input\ Open drain output	Logic input 5 V compliant with open drain output. This is the power stage input enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs
18	MODE	Logic input	Inputs driving method selection. When low the ENx\INx option is selected, when high the INxH\INxL option is enabled
19	INU\INUH	Logic input	Output U high-side driving input (1)
20	ENU\INUL	Logic input	Output U low-side driving input (1)
21	INV\INVH	Logic input	Output V high-side driving input (1)
22	ENV\INVL	Logic input	Output V low-side driving input (1)
23	INW\INWH	Logic input	Output W high-side driving input (1)
24	ENW\INWL	Logic input	Output W low-side driving input (1)
8	NC	NC	Not connected.

1. *Refer to :Section 5.2 Logic inputs for more details*

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5 Functional description

The STSPIN830 is a 3-phase motor driver integrating a PWM current limiter and a power stage composed by three fully-protected half-bridges.

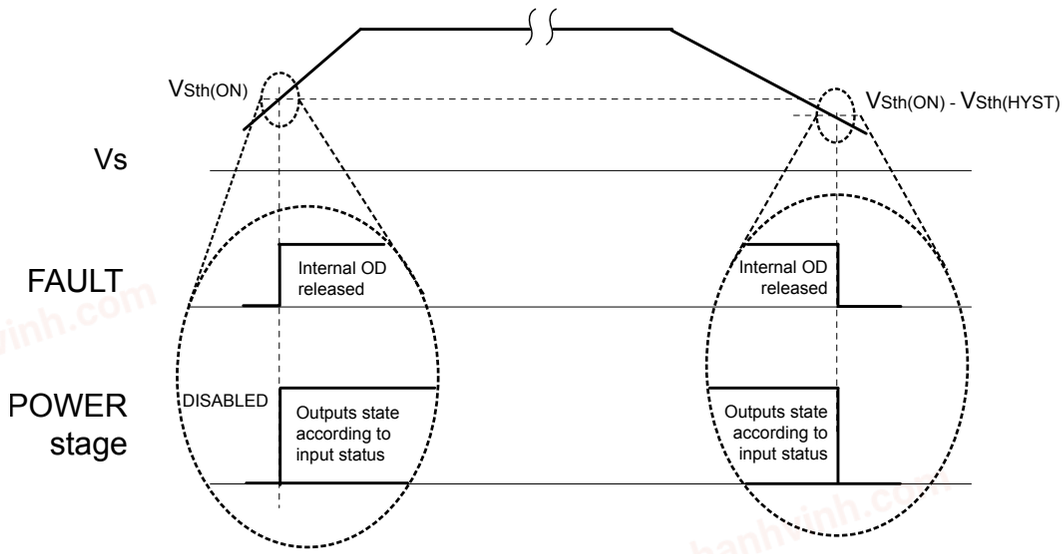
5.1 Power supply and standby

The device is supplied through the VS pins, the two pins **must** be at the same voltage.

At power-up the power stage is disabled and the FAULT pin is forced low until the VS voltage rise above the $V_{Sth(ON)}$ threshold.

If the V_S fall below the $V_{Sth(ON)}$ - $V_{Sth(HYST)}$ value the power stage is immediately disabled and the FAULT pins are forced low.

Figure 3. UVLO protection management



The device provides a low consumption mode which is set forcing the STBY\RESET input below the V_{STBYL} threshold.

When the device is in standby status the power stage is disabled (outputs are in high impedance) and the supply to the integrated control circuitry is strongly reduced. When the device leaves the standby status, all the control circuitry is reset at power-up condition.

5.2 Logic inputs

The STSPIN830 offers two alternative method to drive the power stage, the proper can be selected setting the status of MODE pin.

If MODE pin is set low (connected to GND) the output of each half bridge is controlled by the respective ENx and INx inputs.

If MODE pin is set high the output of each half bridge is controlled by the respective INxH and INxL inputs.

In both cases the status of the power bridge is also determined by the PWM current limiter as indicated in Section 5.3 PWM current limiter.

Note: The MODE pin status must not be changed during device working.

When the EN\FAULT input is forced low the power stage is immediately disabled (all MOSFETs are turned off). The pin is also used as FAULT indication through the integrated open-drain MOSFET as described in paragraph Section 5.4 Device protections and Section 5.5 ESD protection strategy.

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Table 7. ENx and INx inputs truth table (MODE = 'L')

MODE	EN\FAULT	ENx	INx	OUTx	'x' Half-bridge condition
0	0	X (1)	X(1)	High Z (2)	Disabled
0	1	0	X(1)	High Z (2)	Disabled
0	1	1	0	GND	LS on
0	1	1	1	V_S	HS on

1. *X: don't care.*
2. *High Z: high impedance*

Table 8. INxL and INxH inputs truth table (MODE = 'H')

MODE	EN\FAULT	INxH	INxL	OUTx	'x' Half-bridge condition
1	0	X(1)	X(1)	High Z (2)	Disabled
1	1	0	0	High Z (2)	Disabled
1	1	0	1	GND	LS on
1	1	1	0	V_S	HS on
1	1	1	1	High Z (2)	Disabled (interlocking)

1. *X: don't care.*

5.3 PWM current limiter

The device implements a PWM current limiter.

The load current is sensed through the SNS pin monitoring the voltage drop across an external resistor connected between the source of the low side power MOSFET (SENSEx pins) and ground.

The voltage of the sense pin (V_{SNS}) is compared to the reference voltage pin (V_{REF}).

When $V_{SNS} > V_{REF}$ the internal comparator is triggered, the OFF time counter is started and all the power outputs are disabled (high impedance) until the end of count of the timer.

During current decays the inputs values are ignored until the system returns to ON condition (decay time expired).

The reference voltage value, V_{REF}, has to be selected according the load current target value (peak value) and sense resistors value.

Equation 1

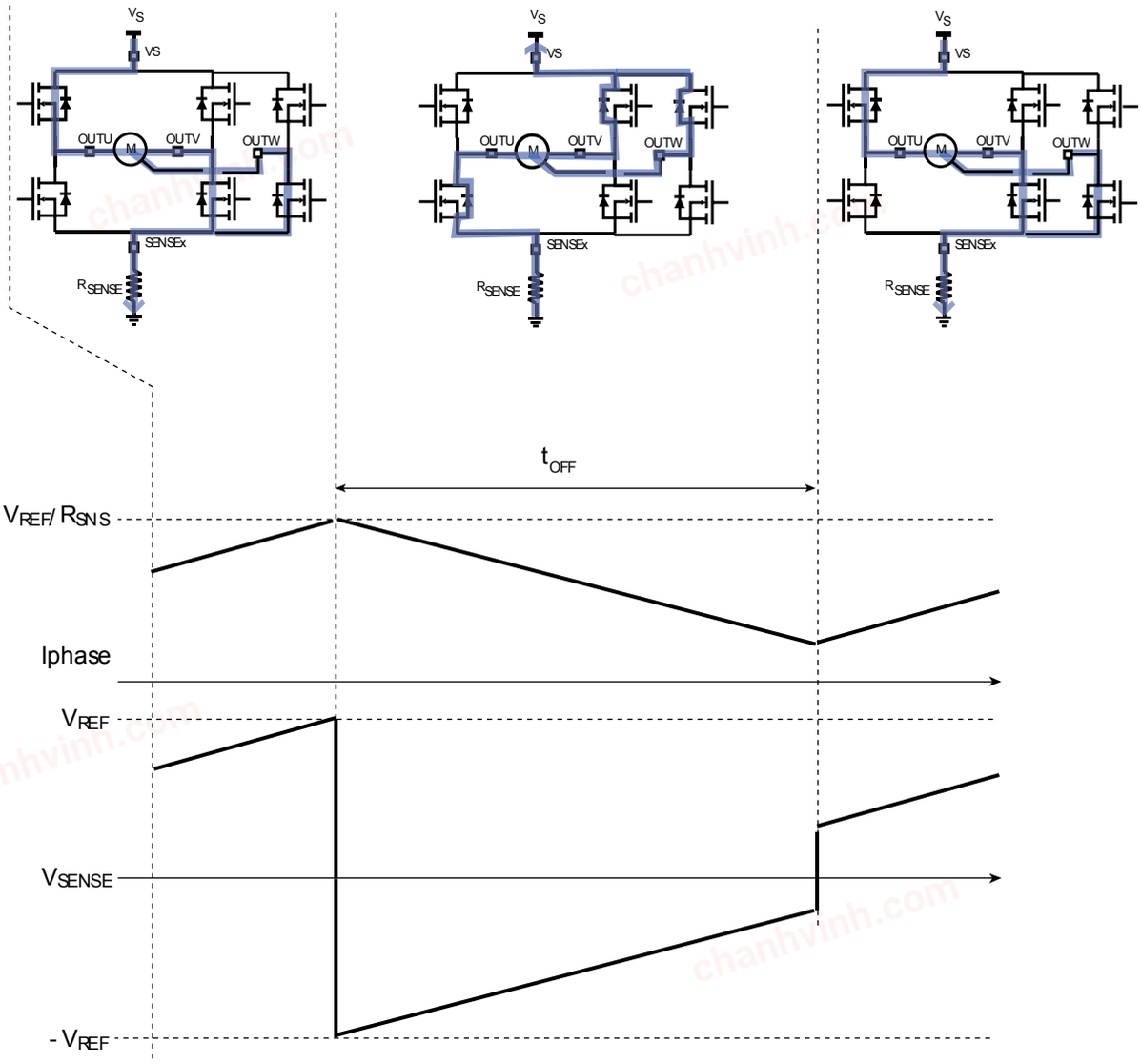
$$V_{REF} = R_{SENSE} \times I_{LOAD,peak} \quad (1)$$

The choice of sense resistors value must be take into account two main issues:

- The sensing resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during the current recirculation. For this reason the resistance of this component should be kept low (using multiple resistors in parallel will help obtaining the required power rating with standard resistors).
- The lower is the R_{SENSE} value, the higher is the peak current error due to noise on V_{REF} pin and to the input offset of the current sense comparator: too small values of R_{SENSE} must be avoided.

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Figure 4. **PWM current limit sequence example**



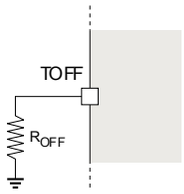
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Note: When the voltage on the SNS pin exceeds the absolute ratings, fault condition is triggered and the EN\FAULT output is forced low.

TOFF adjustment

The OFF time is adjusted through an external resistor connected between the TOFF pin and ground as shown in Figure 5. OFF time regulation circuit .

Figure 5. **OFF time regulation circuit**

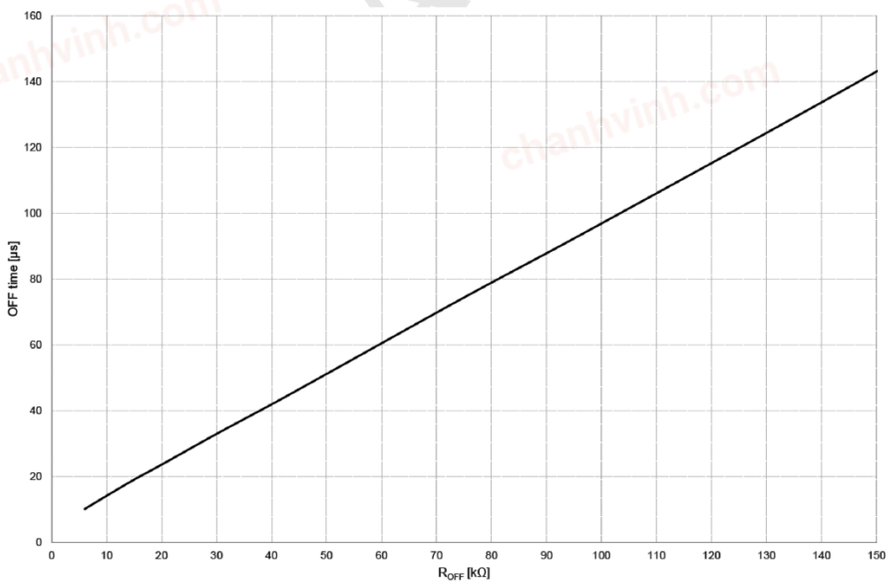


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The relation between the OFF time and the external resistor value is shown in the graph of Figure 6. OFF time vs ROFF value. The value typically ranges from 10 µs to 150 µs.
The recommended value for R_{OFF} is in the range between 5 kΩ kΩ

Figure 6. OFF time vs ROFF value



5.4 Device protections

5.4.1 Overcurrent and short circuit protections

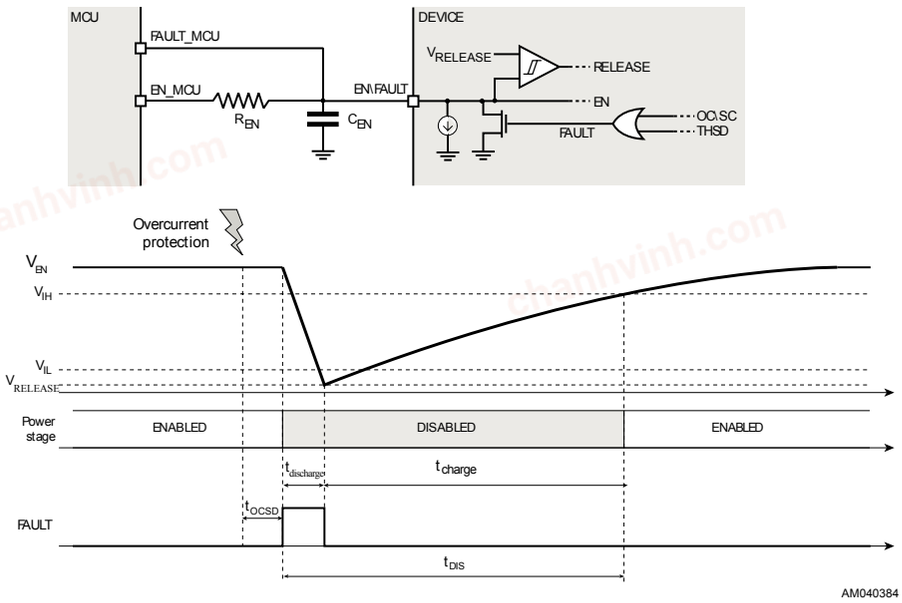
The device embeds a circuitry protecting each power MOSFET against the over load and short circuit conditions (short to ground, short to VS and short between outputs).

When the overcurrent or the short circuit protection is triggered the power stage is disabled and the EN\FAULT input is forced low through the integrated open drain MOSFET discharging the external C_{EN} capacitor.

The power stage is kept disabled and the open drain MOSFET is kept ON until the EN\FAULT input falls below the $V_{RELEASE}$ threshold, then the C_{EN} capacitor is charged through the external R_{EN} resistor.

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Figure 7. Overcurrent and short-circuit protections management



The total disable time after an overcurrent event is set sizing properly the external network connected to EN \FAULT pin (refer to Figure 8. Disable time versus REN and CEN values (VDD = 3.3 V)) and it is the sum of the discharging and charging time of the C_{EN} capacitor:

Equation 2

(2)

$$t_{DIS} = t_{discharge} + t_{charge}$$

Considering $t_{discharge}$ is normally significantly lower than t_{charge}, its contribution is negligible and the disable time is almost equal to t_{charge} only:

Equation 3

(3)

$$t_{DIS} \cong R_{EN} \times C_{EN} \times \ln \frac{(V_{DD} - R_{EN} \times I_{PD}) - V_{RELEASE}}{(V_{DD} - R_{EN} \times I_{PD}) - V_{IH}}$$

Where V_{DD} is the pull-up voltage of R_{EN} resistor.

The recommended value for R_{EN} and C_{EN} are respectively 39 kΩ and 10 nF that allow obtaining 200 µs disable time.

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Figure 8. **Disable time versus REN and CEN values (VDD = 3.3 V)**

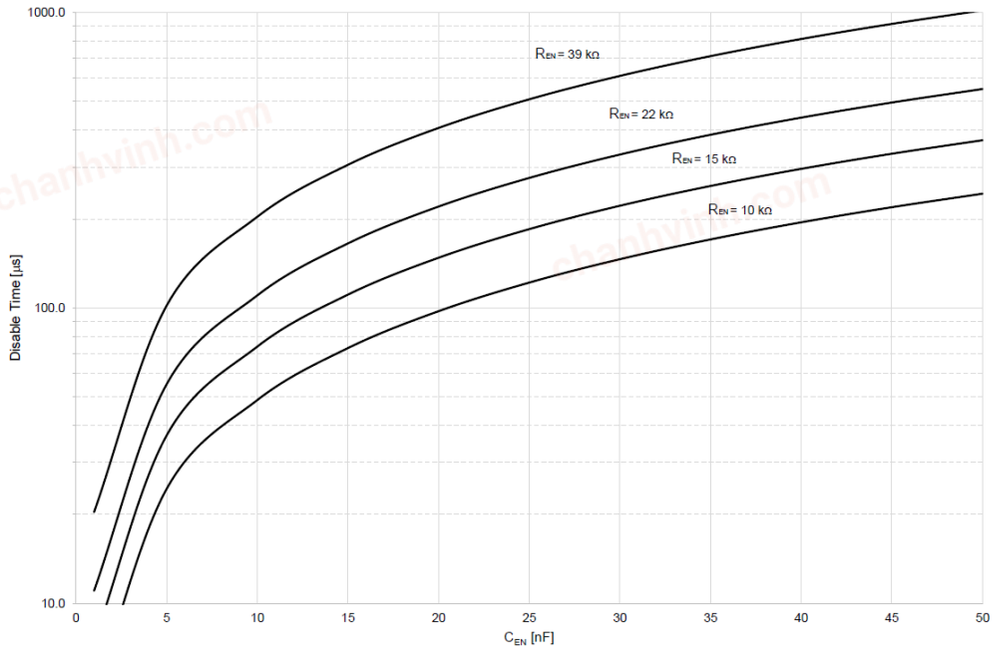
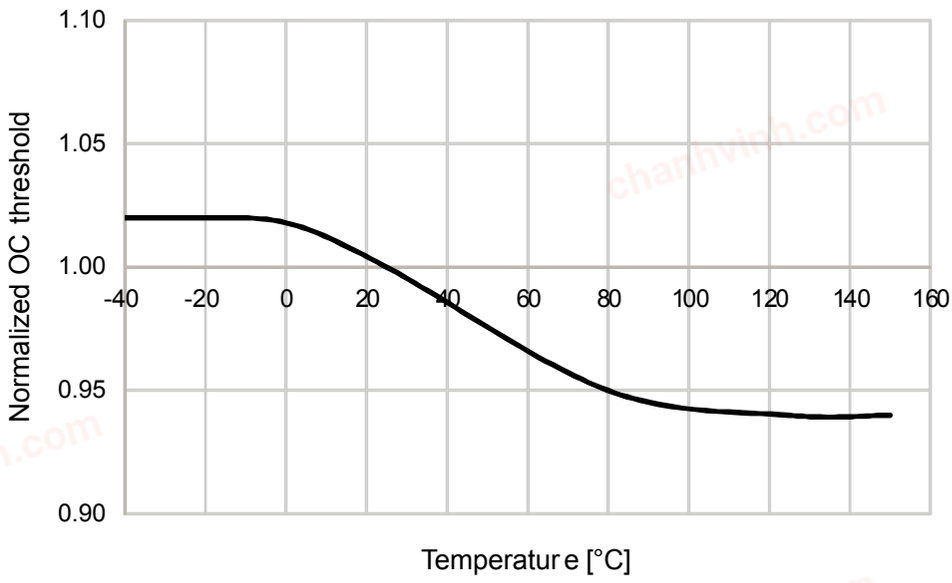


Figure 9. **Overcurrent threshold versus temperature (normalized at 25 °C)**



5.4.2 Thermal shutdown

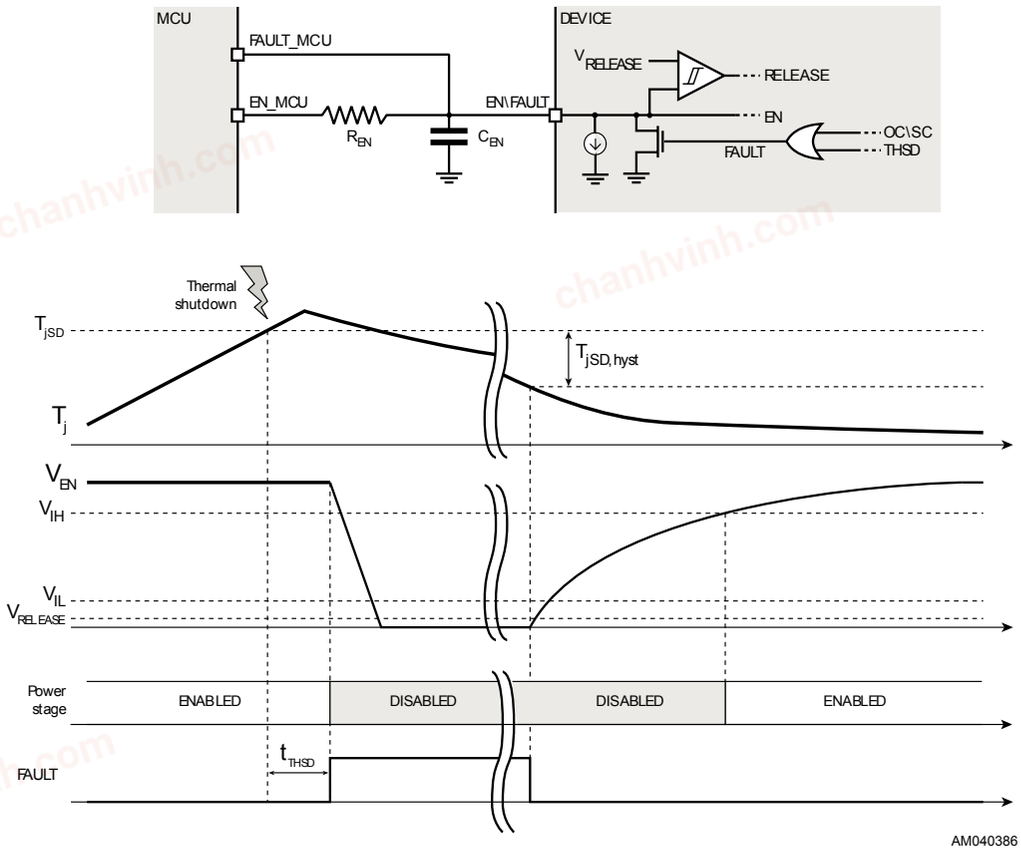
The device embeds a circuitry protecting it from the overtemperature condition.

When the thermal shutdown temperature is reached the power bridges are disabled and the EN\FAULT input is forced low through the integrated open drain MOSFET (refer to Figure 10. Thermal shutdown management).

The protection and the EN\FAULT output are released when the IC temperature returns below a safe operating value (T_{jSD} - $T_{jSD,Hyst}$).

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Figure 10. **Thermal shutdown management**



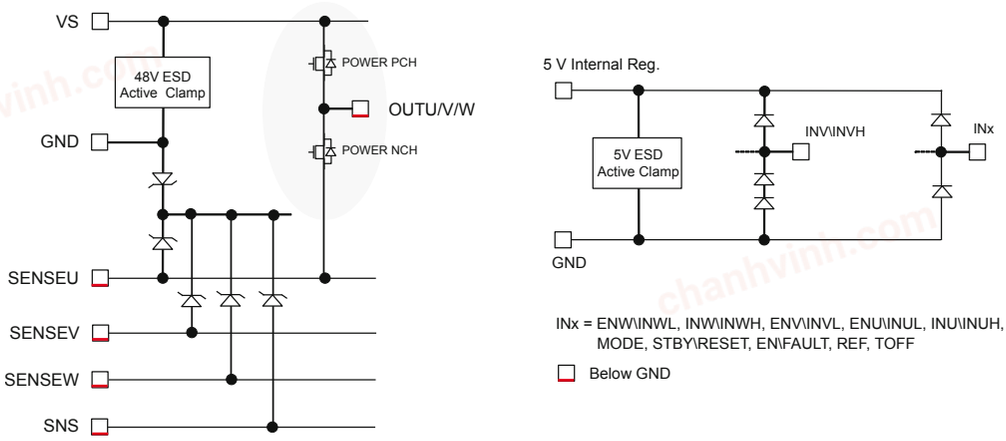
5.4.3 Blanking time

The device provides a blanking time t_{BLANK} after each power MOSFET commutation to prevent false triggering of protections and current limiter.

During blanking time the protections (overcurrent, short circuit, thermal shutdown) and the comparator of the current limiter are inhibit.

5.5 ESD protection strategy

Figure 11. **ESD protection strategy**



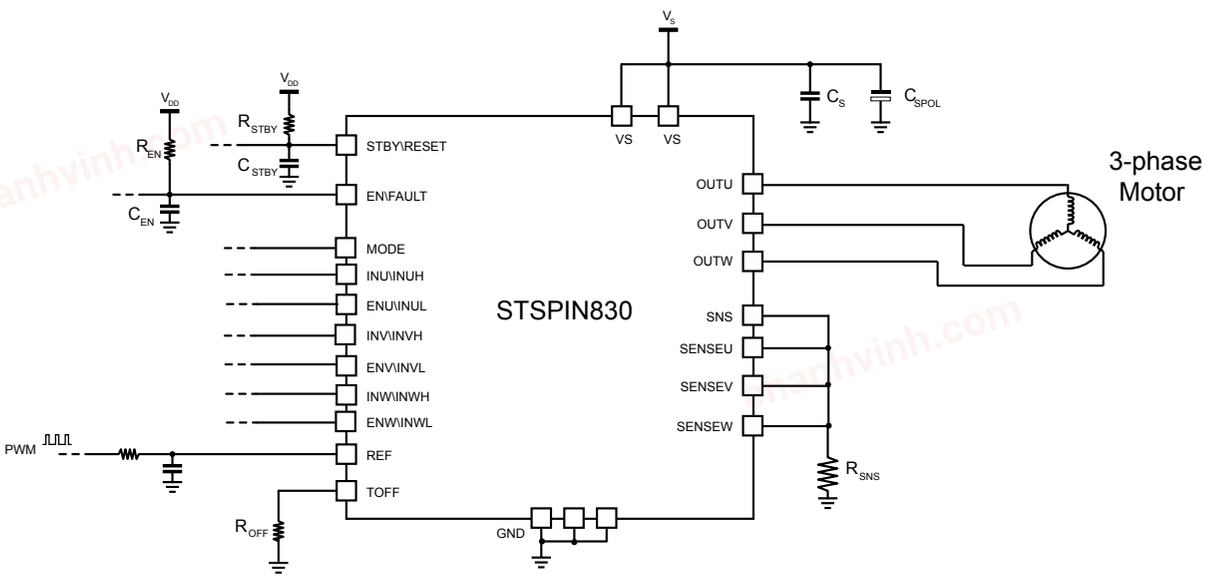
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6 Typical applications

Table 9. **Typical application values**

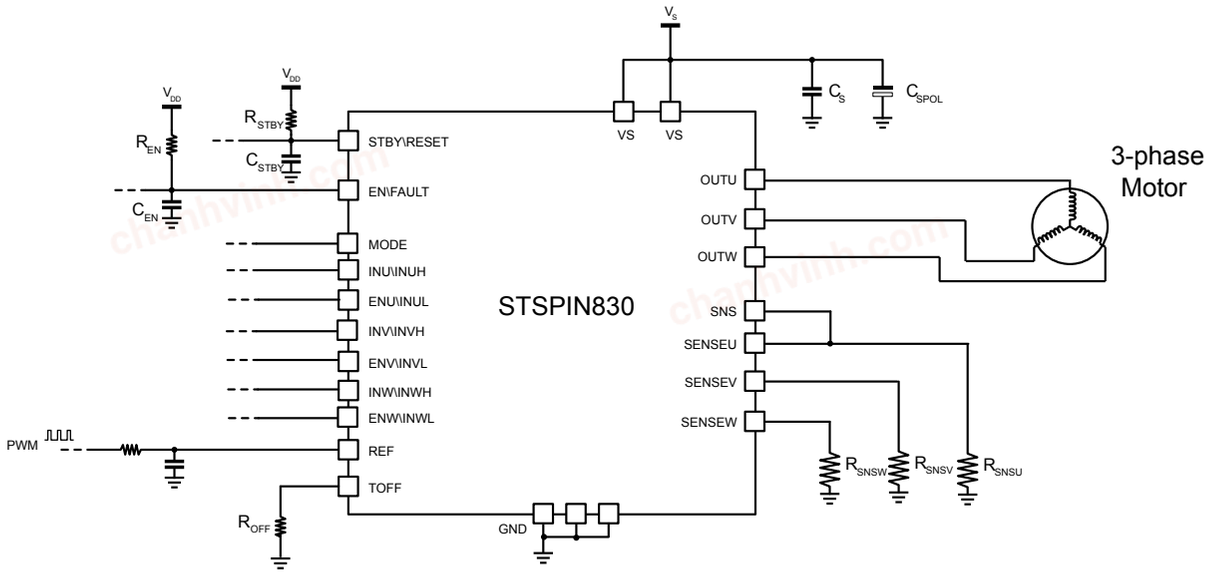
Name	Value
C_S	330 nF
C_{SPOL}	33 µF
R_{SNS}	330 mΩ / 1W
C_{EN}	10 nF
R_{EN}	39 kΩ
C_{STBY}	1 nF
R_{STBY}	18 kΩ
R_{OFF}	10 kΩ (T_{OFF} □ 13 µs)

Figure 12. **Typical application schematic with single shunt**



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Figure 13. **Typical application schematic with triple shunt**



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7 Layout recommendations

The integrates the power stage; in order to improve the thermal dissipation, the exposed pad must be connected to the ground plane on the bottom layer using multiple vias equally spaced. This ground plane acts as a heatsink, for this reason it should be as wide as possible.

The voltage supply VS must be stabilized and filtered with a ceramic bypass capacitor, typically 330nF. It must be placed on the same side and as close as possible to VS pin in order to reject high frequency noise components on the supply. A bulk capacitor could also be required (typically a 33 µF). The connection between the power supply connector and the VS pins must be as short as possible using wide traces.

In order to ensure the best ground connection between the and the other components, a GND plane surrounding the device is recommended.

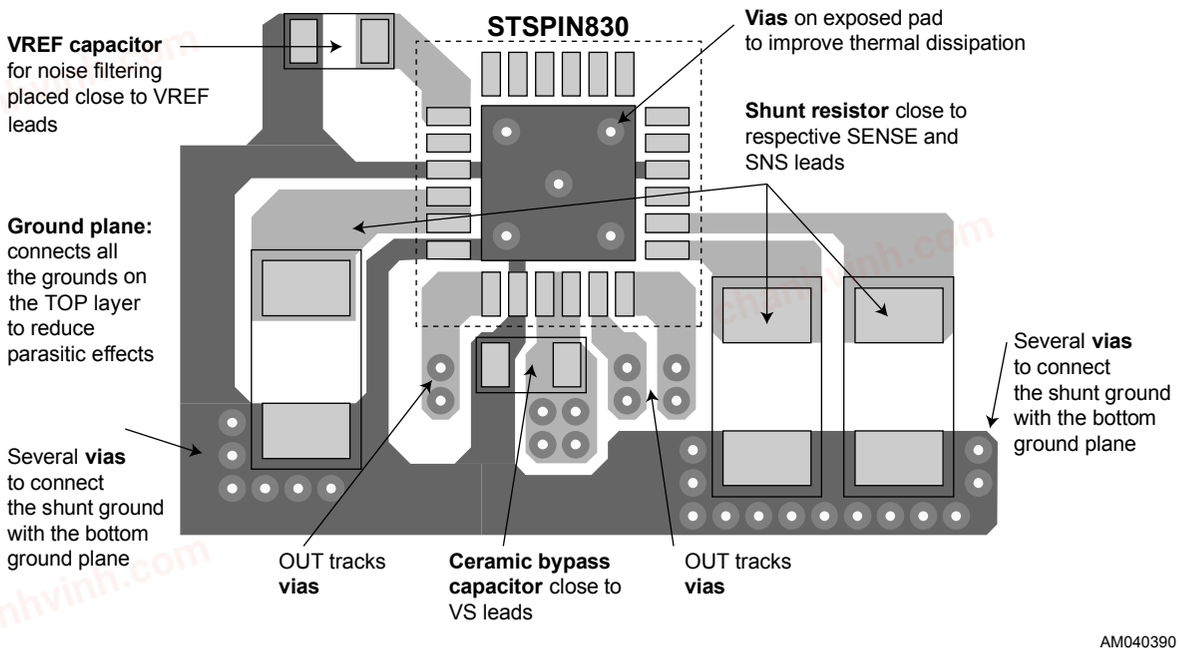
A capacitor between REF pins and ground should be positioned as near as possible to the device in order to filter the noise and stabilize the reference voltage.

Several vias should be positioned as near as possible each sense resistor connecting them to the ground plane on the bottom layer. In this way, both the GND planes provide a path for the current flowing into the power stage.

The path between the ground of the shunt resistors and the ceramic bypass capacitor of the device is critical; for this reason it must be as short as possible minimizing parasitic inductances that can cause voltage spikes on SENSE and OUT pins.

The OUT pins and the VS nets can be routed using the bottom layer, it is recommended to use two vias for output connections.

Figure 14. PCB layout example with triple shunt (top layer)



In case of single shunt configuration take special care for the SENSE and SNS pins connection.

As suggested in the Figure 15. PCB layout example with single shunt (top layer) and Figure 16. PCB layout example with single shunt (bottom layer), the shunt resistor can be placed in the top layer close to SENSEU and SNS pins with a wide copper area and vias. The connection with other sense pins (SENSEV and SENSEW) can be routed in the bottom layer taking care to maximize the track area and add more vias near to the pins.

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Figure 15. **PCB layout example with single shunt (top layer)**

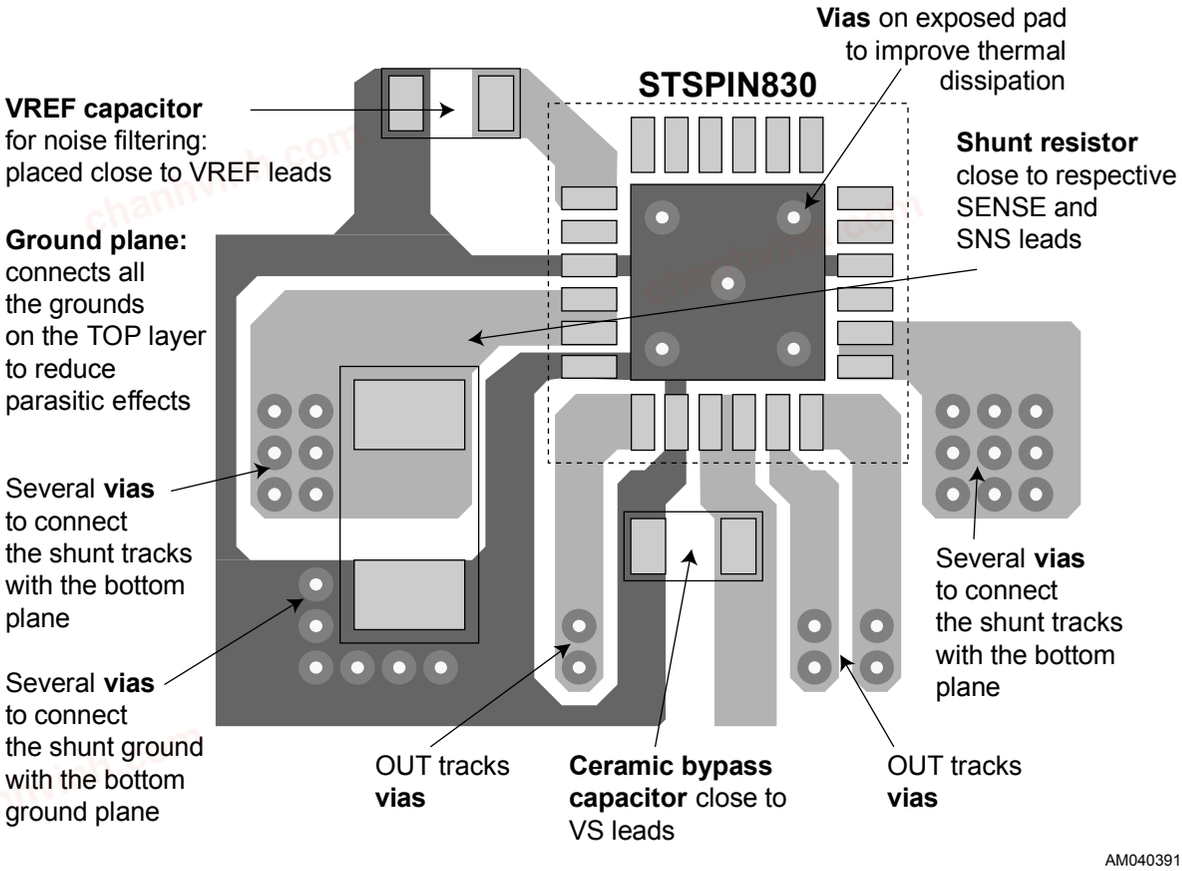
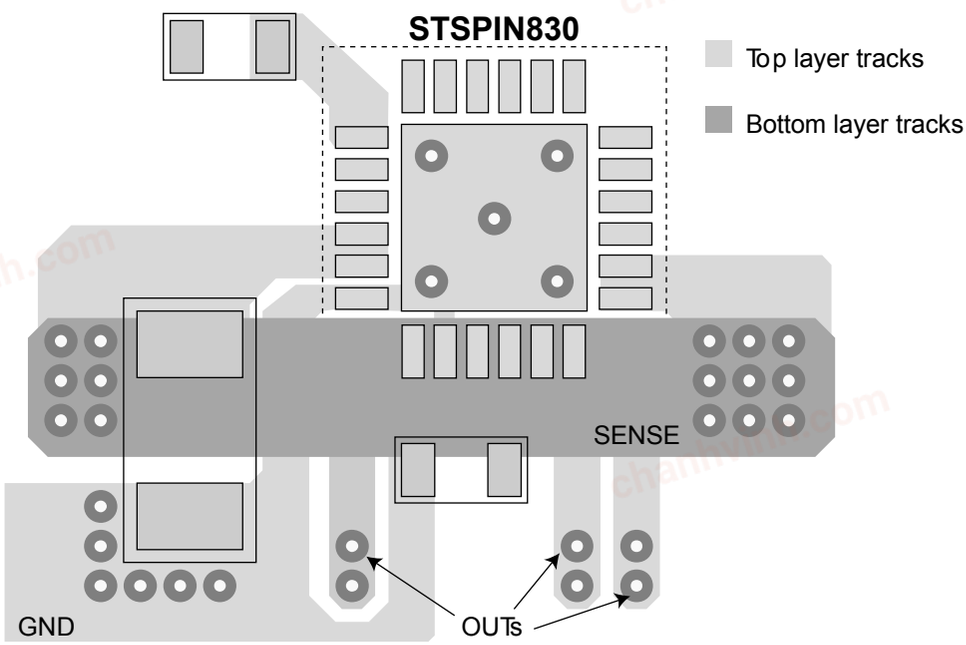


Figure 16. **PCB layout example with single shunt (bottom layer)**



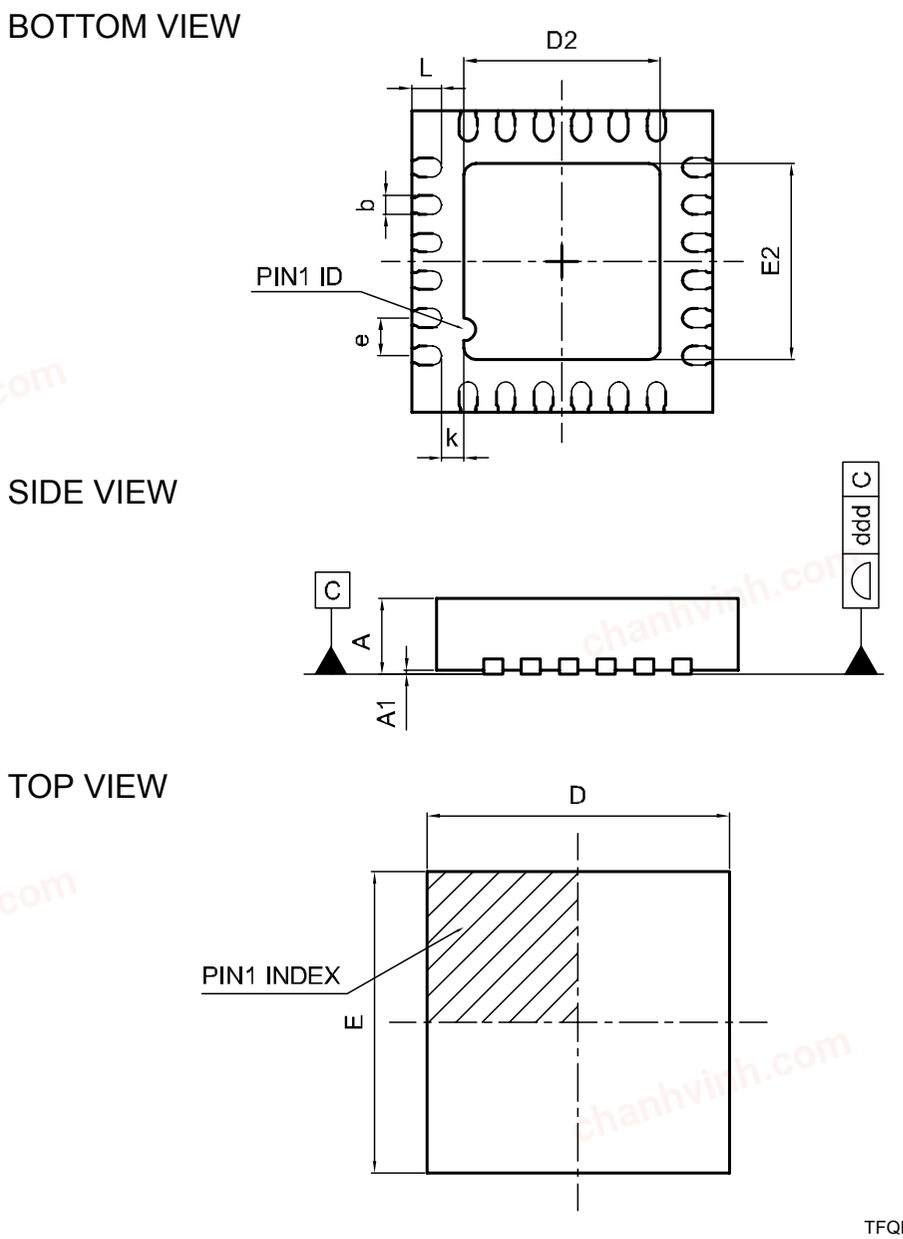
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8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK®packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 TFQFPN 4x4x1.05 24L package information

Figure 17. TFQFPN 4 x 4 x 1.05 - 24L package outline



TFQFPN-4x4x1.05-24

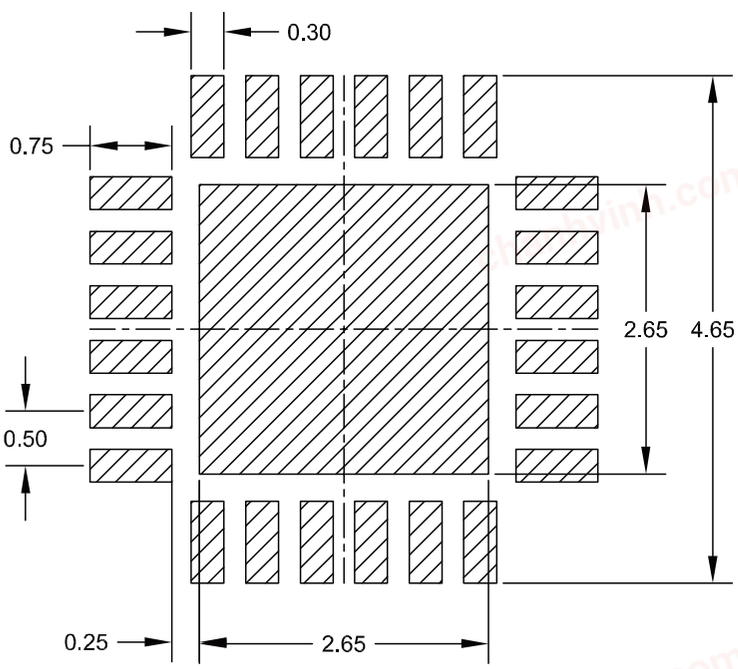
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Table 10. **TFQFPN 4x4x1.05 24L package mechanical data**

Symbol	Dimensions (mm)			
	Min.	Typ.	Max.	NOTES
A	0.90	1.00	1.10	
A1	0.00	0.02	0.05	
b	0.20	0.25	0.30	(1)
D	3.90	4.00	4.10	
D2	2.55	2.60	2.65	
E	3.90	4.00	4.10	
E2	2.55	2.60	2.65	
e		0.50		
L	0.35	0.40	0.45	
k		0.30		
ddd		0.05		

Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm

Figure 18. **TFQFPN 4 x 4 x 1.05 - 24L suggested footprint**



TFQFPN 4 x 4 x 1.05 - 24 L

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9 Ordering information

Table 11. **Ordering information**

Order code	Package	Packing
STSPIN830	TFQFPN 4 x 4 x 1.05 - 24L	Tape and reel

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Revision history

Table 12. **Document revision history**

Date	Version	Changes
18-May-2018	1	Initial release.
02 Aug-2019	2	Some minor text changes inside the document, cover image updated, updated Table 2. Recommended operating conditions

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