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STSPIN948

Datasheet

Scalable 4.5 A dual full-bridge driver for brushed DC motors



Features

- Operating voltage up to 58 V
- Maximum output current up to 4.5 Arms
- Five driving methods with full-bridge and dual half-bridge parallel mode
- $R_{DS(ON)}$ HS + LS = 0.36 Ω typ.
- Adjustable power MOS slew rate
- Integrated amplifiers with two different embedded current control techniques
- Adjustable OFF-time with slow or mixed decay
- Low consumption standby
- Protections
  - UVLO
  - Overcurrent protection
  - Thermal shutdown

STSPIN

Product status link

STSPIN948

Product label

SUSTAINABLE TECHNOLOGY

Application

- Stage lighting
- Factory automation
- ATM and money handling machines
- Textile machines
- Home appliances
- Robotics
- Antenna control
- Vending machines

Description

The STSPIN948 is a 4.5 A dual full-bridge driver for brushed DC motors or bipolar stepper motors.

The power stage is designed with high dynamic performance, allowing to achieve high frequency PWM control with precise duty-cycle.

Each full-bridge is totally independent with a current limiter with adjustable threshold and OFF-time with slow or mixed decay selection. Two amplifiers with fixed amplification factor are available for current sensing (using an external shunt resistor).

The adjustable slew-rate guarantees the best trade-off between performances and EMI.

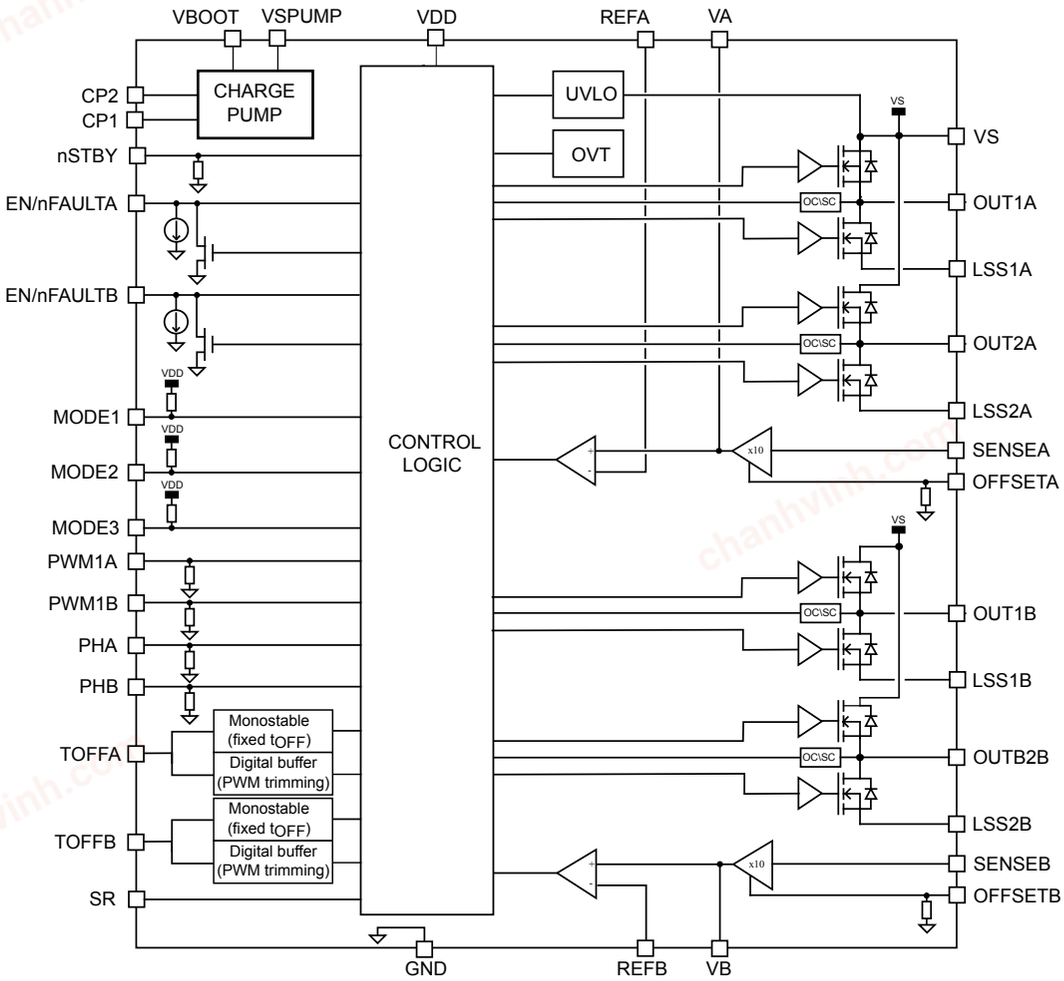
Versatile power stage offers several ways of operation for a high level of flexibility.

The device offers a complete set of protection features including overcurrent, overtemperature, and low bus voltage detection.

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1 Block diagram

Figure 1. **Block diagram**



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2 Electrical data

2.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 1 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_{DD}	Control logic supply voltage		-0.3 to 4	V
V_S	Power stage supply voltage		-0.3 to 62	V
dV_S/dt	Supply voltage gradient		0.5	V/µs
V_{SPUMP}	Charge pump input voltage		V_S +/- 0.1 V	V
V_{BOOT}	Bootstrap voltage		-0.3 to 62	V
V_{OUT}	Output voltage	V_S < 61.4 V	V_S + 0.6	V
		V_S ≥ 61.4 V	62	
I_{OUT}	DC output current	Each output	Up to 4.5	A_{rms}
$I_{OUT,peak}$	Peak output current		Limited by OC protection	A
V_{LSS}	Low-side source voltage (LSSxx pins)		-0.6 to +2	V
V_{REFA}, V_{REFB}	Voltage range at pins REFA and REFB	V_{DD} = 4 V	-0.3 to V_{DD}	V
V_{SR}	Voltage range at pin SR	V_{DD} = 4 V	-0.3 to V_{DD}	V
V_{TOFFx}	Voltage range at pins T_{OFFx}	V_{DD} = 4 V	-0.3 to V_{DD}	V
V_{IN}	Logic input voltage	All digital inputs excluded MODE1, MODE2, MODE3, OFFSETA and OFFSETB	-0.3 to 5.5	V
		MODE1, MODE2, MODE3, OFFSETA and OFFSETB	-0.3 to V_{DD}	V
I_{OD}	Open drain outputs sink current	nFAULTA, nFAULTB	Up to 8	mA
T_{stg}	Storage temperature		-55 to 150	°C
T_j	Junction temperature		-40 to 150	°C

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2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	Control logic supply voltage		2.8(1)	3.3	3.6	V
V_S(2)	Power stage supply voltage		5.2		58(3)	V
V_{SPUMP}	Charge pump input voltage			V_S		V
V_{BO}	Bootstrap overdrive voltage	$V_{BOOT} - V_S$		3		V
V_{REFA}, V_{REFB}	Voltage range at pins REFA and REFB		0.1		V_{DD}	V
V_{LSS1x}, V_{LSS2x}	Low-side source voltage		-0.6		+1	V
V_{OUT}	Output voltage		-0.6		V_S	V
V_{IN}(4)	Logic input voltage	MODE1, MODE2, MODE3, OFFSETA and OFFSETB	0		VDD	V
		All others	0		5	V
R_{TOFF}	Current limiter time setting resistor	Enabled fixed OFF-time current limiter mode (see Section 5.6.1)	10		120	kΩ
C_{TOFF}	Current limiter time setting capacitor	Enabled fixed OFF-time current limiter mode (see Section 5.6.1)	0.1		5.6	nF
R_{SR}	Slew rate selection resistor		See Section 5 Table 7			
t_{pulse}	Minimum PWM pulse width		280			ns
t_{BOOT}	Charge pump capacitor charging time	C_{CP} = 100 nF C_{BOOT} = 1 µF		170		µs
f_{PWM}	Switching frequency		0		500(5)	kHz
C_{BOOT}	Bootstrap capacitor			1		µF
C_{CP}	Charge pump capacitor			100		nF
T_{amb}	Ambient temperature		-40		85(2)	°C

1. *Actual operative range can be limited by UVLO protections*
2. *Actual operative range according to heat dissipation performance of the application*
3. *In specific conditions (Tj ≥ 75 °C and RH ≥ 60%), the maximum V_S voltage is sustainable for a limited period*
4. *All digital inputs (excluding MODE1,MODE2,MODE3,OFFSETA and OFFSETB) are 5 V tolerant*
5. *Actual operative range can be limited by the selected slew rate*

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2.3 ESD protection ratings

Table 3. ESD protection ratings

Symbol	Parameter	Condition	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	H2	2	kV
CDM	Charge device model	All pins Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2a	500	V
		Corner pins only Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2	750	V
MM	Machine model	Conforming to EIA/JESD22-A115-C	NC	200	V

2.4 Thermal data

Table 4. Thermal data

Symbol	Parameter	Condition	Value	Unit
R_{thJA}	Junction to ambient thermal resistance	Natural convection, according to JESD51-2a(1)	27.6	°C/W
$R_{thJCtop}$	Junction to case thermal resistance (top side)	Cold plate on package top, according to JESD51-12.01(1)	13.4	°C/W
$R_{thJCbot}$	Junction to case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-12.01(1)	2.4	°C/W
R_{thJB}	Junction to board thermal resistance	According to JESD51-8(1)	11.9	°C/W
Ψ_{JT}	Junction to top characterization	According to JESD51-12.01(1)	0.1	°C/W
Ψ_{JB}	Junction to board characterization	According to JESD51-12.01(1)	11.7	°C/W

1. *Simulated as per standard JEDEC (JESD51-7) in natural convection*

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3 Electrical characteristics

Testing conditions: V_S = 58 V, V_{BOOT} = 61 V, V_{DD} = 3.3 V, unless otherwise specified.
Typical values are tested at T_j = 25 °C, minimum and maximum values are guaranteed by thermal characterization in the temperature range of -40 to 125 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
$V_{DDth(ON)}$	V_{DD} power-on reset	V_{DD} rising			2.7	V
$V_{DDth(Hyst)}$	V_{DD} power-on reset hysteresis	V_{DD} falling ($V_{DDth(ON)}$ - $V_{DDth(OFF)}$)	100		300	mV
$V_{Sth(ON)}$	V_S turn-on threshold	V_S rising			5.2	V
$V_{Sth(Hyst)}$	V_S turn-on threshold hysteresis	V_S falling ($V_{Sth(ON)}$ - $V_{Sth(OFF)}$)	100		300	mV
$V_{BOth(ON)}$	V_{BO} turn-on threshold	V_{BO} rising			2	V
$I_{DD,STBY}$	V_{DD} consumption in standby	Standby			3	µA
$I_{S,STBY}$	V_S consumption in standby	Standby			1	µA
t_{STBY}	Standby time				600	µs
t_{WAKE}	Wake-up time				10	µs
Power stage						
$R_{DS(ON),LS}$	Low-side turn-on resistance	T_j = 25 °C		180		mΩ
$R_{DS(ON),HS}$	High-side turn-on resistance	T_j = 25 °C		180		mΩ
$t_{dIN(H)}$	Input high to high-side turn-on propagation delay	Maximum slew rate		300		ns
$t_{dIN(L)}$	Input low to low-side turn-on propagation delay	Maximum slew rate		300		ns
MT	Delay matching HS and LS turn-on/off	Maximum slew rate MT = $\lvert t_{dH} - t_{dL} \rvert$			50	ns
SR_{rise}	Rising slew rate	R_{SR} = 1 kΩ R_{SR} = 2.2 kΩ R_{SR} = 5.6 kΩ R_{SR} = 10 kΩ		2 1.2 0.6 0.3		V/ns
SR_{fall}	Falling slew rate	R_{SR} = 1 kΩ R_{SR} = 2.2 kΩ R_{SR} = 5.6 kΩ R_{SR} = 10 kΩ		2 1.2 0.6 0.3		V/ns
Logic input and outputs						
V_{IL}	Low logic input voltage				0.8	V
V_{IH}	High logic input voltage		2			V
$V_{IL(EN)}$	Enable low logic input voltage				0.4	V
$V_{IH(EN)}$	Enable high logic input voltage		2.55			V

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Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{OL(nFAULT)}$	Low logic level output voltage (EN/nFAULTx)	I_{SINK} = 4 mA			0.4	V
V_{FAULT}	FAULT open drain release threshold		0.4		0.6	V
I_{PD}	EN/nFAULTA and EN/nFAULTB pull-down current			5		µA
R_{PDin}	Input pull-down resistor			570		kΩ
R_{PUin}	Input pull-up resistor (MODE1, MODE2, and MODE3)			570		kΩ
Current limiter						
t_{OFF}	Current limiter off-time See Section 5 Figure 10	R_{OFF} = 10 kΩ C_{OFF} = 0.1 nF		1		µs
		R_{OFF} = 120 kΩ C_{OFF} = 5.6 nF		500		µs
Integrated amplifier						
A_{CL}	Gain	Full temp range	9.5	10	10.5	V/V
$t_{settling}$	Output voltage settling time	V_{in} 150 mV step C_L= 100 pF			200	ns
Protections						
I_{OC}	Overcurrent threshold	See Figure 13	7		14	A
T_{SD}	Thermal shutdown threshold		150			°C
$T_{SD(Hyst)}$	Thermal shutdown hysteresis			30		°C

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4 Pin description

Figure 2. **Pin connection**

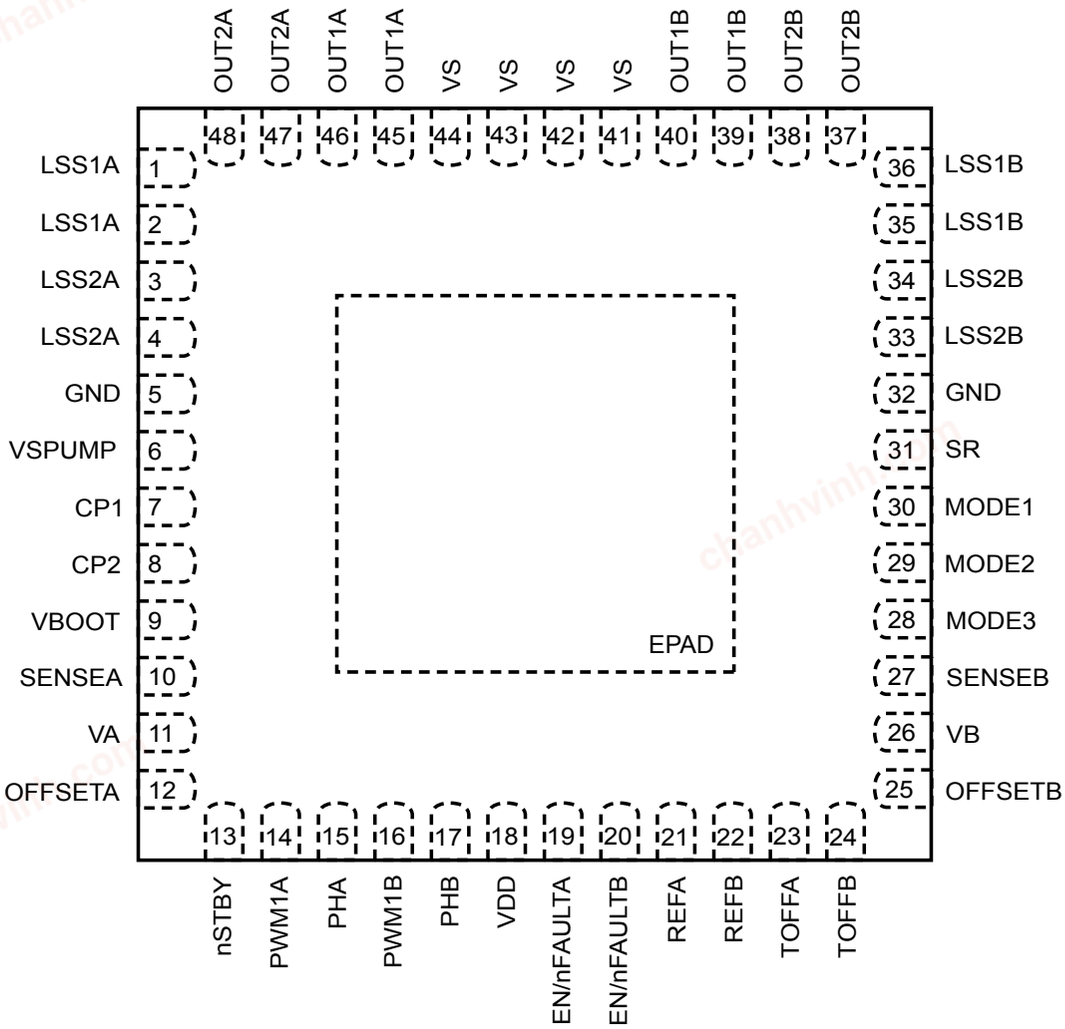


Table 6. **Pad list**

N.	Name	Type	Function
1	LSS1A	Power	Low-side source half-bridge 1A
2	LSS1A	Power	Low-side source half-bridge 1A
3	LSS2A	Power	Low-side source half-bridge 2A
4	LSS2A	Power	Low-side source half-bridge 2A
5	GND	Ground	Device ground
6	VSPUMP	Supply	Supply charge pump circuitry (internally connected to VS). In application must be connected to the CBOOT. It can be shorted to VS supply
7	CP1	Analog output	Charge pump oscillator output1
8	CP2	Analog output	Charge pump oscillator output2
9	VBOOT	Supply	Bootstrap voltage needed to drive the high-side MOSFETs
10	SENSEA	Analog input	Amplifier A input signal

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N.	Name	Type	Function
11	VA	Analog output	Amplifier A output signal
12	OFFSETA	Digital input	Voltage level shift (amplifier A)
13	nSTBY	Digital input	Active low standby input. When forced low the device enters in low consumption mode
14	PWM1A	Digital input	Half-bridge 1A PWM input
15	PHA	Digital input	Phase A input
16	PWM1B	Digital input	Half-bridge 1B PWM input
17	PHB	Digital input	Phase B input
18	VDD	Supply	Supply digital logic
19	EN/nFAULTA	Logic input/open drain output	Logic input with open drain output. Full-bridge A enable (when low, the power stage is turned off); it is forced low by the integrated open drain MOSFET when a failure occurs.
20	EN/nFAULTB	Logic input/open drain output	Logic input with open drain output. Full-bridge B enable (when low, the power stage is turned off); it is forced low by the integrated open drain MOSFET when a failure occurs.
21	REFA	Analog input	Reference voltage for PWM current limiter circuitry (half-bridge 1A-2A)
22	REFB	Analog input	Reference voltage for PWM current limiter circuitry (half-bridge 1B-2B)
23	TOFFA	Analog input Digital output	PWM current limiter off-time adjustment (full-bridge 1A-2A) in fixed off-time mode Decay output signal in PWM trimming mode
24	TOFFB	Analog input Digital output	PWM current limiter off-time adjustment (full-bridge 1B-2B) in fixed off-time mode Decay output signal in PWM trimming mode
25	OFFSETB	Digital input	Voltage level shift (amplifier A)
26	VB	Analog output	Amplifier B output signal
27	SENSEB	Analog output	Amplifier B input signal
28	MODE3	Digital input	Mode selector pin 3
29	MODE2	Digital input	Mode selector pin 2
30	MODE1	Digital input	Mode selector pin 1
31	SR	Analog input	Slew rate value selection
32	GND	Ground	Device ground
33	LSS2B	Power	Low-side source half-bridge 2B
34	LSS2B	Power	Low-side source half-bridge 2B
35	LSS1B	Power	Low-side source half-bridge 1B
36	LSS1B	Power	Low-side source half-bridge 1B
37	OUT2B	Power	Power output half-bridge 2B
38	OUT2B	Power	Power output half-bridge 2B
39	OUT1B	Power	Power output half-bridge 1B
40	OUT1B	Power	Power output half-bridge 1B
41	VS	Supply	Supply output power stages
42	VS	Supply	Supply output power stages
43	VS	Supply	Supply output power stages
44	VS	Supply	Supply output power stages

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N.	Name	Type	Function
45	OUT1A	Power	Power output half-bridge 1A
46	OUT1A	Power	Power output half-bridge 1A
47	OUT2A	Power	Power output half-bridge 2A
48	OUT2A	Power	Power output half-bridge 2A

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5 Description

The is a protected dual full-bridge with low $R_{DS(ON)}$ and high current capability.

The power stages are designed with high dynamic performance allowing to achieve high frequency PWM control with precise duty-cycle.

It integrates a full set of protections, PWM current limiter circuitry and amplifiers for the current sensing through an external shunt resistor.

5.1 Power supply

The device has three supply pins:

- VDD is the control logic supply voltage
- VS is the supply voltage for all the power stage
- VBOOT is the supply voltage for high-side gate drivers

During the power-up, the device is in Under Voltage Lock Out condition (UVLO) until the VS supply voltage rises above the $V_{Sth(ON)}$ threshold and the VBOOT supply voltage rises above the $V_{BOth(ON)}$ threshold.

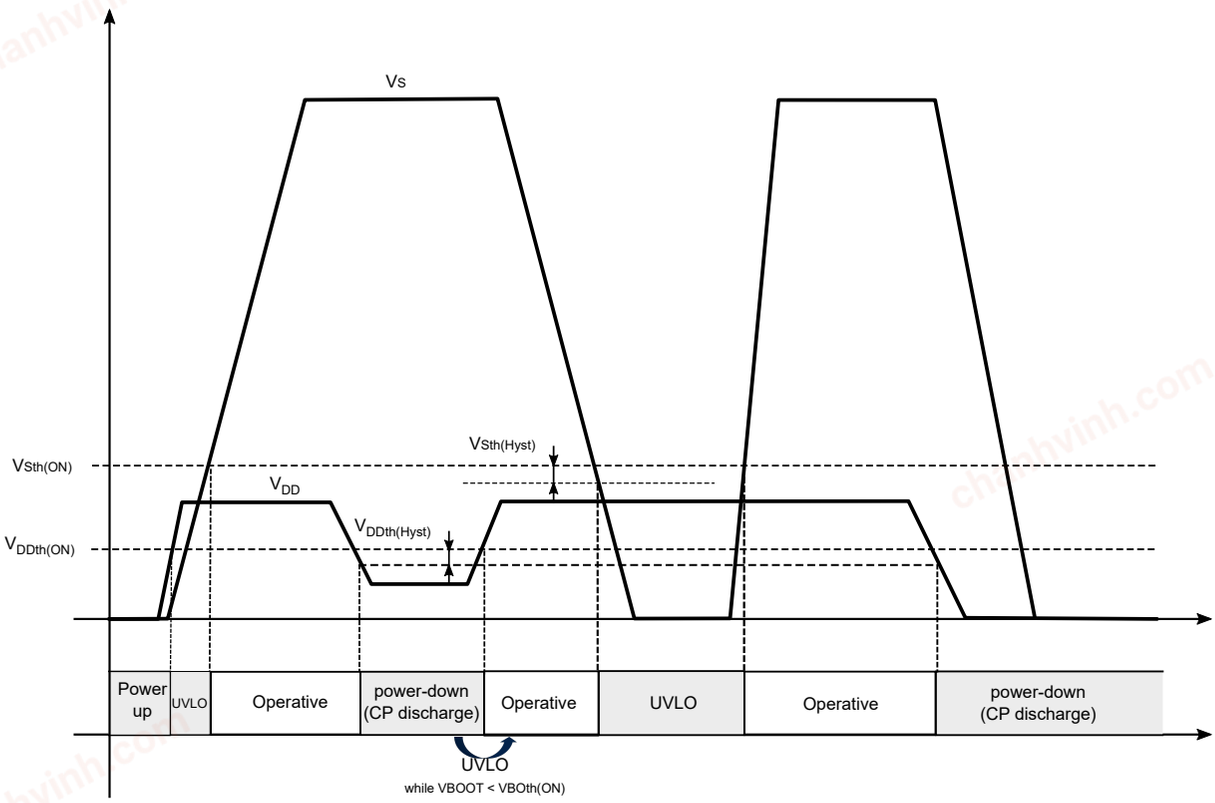
If during the operation the V_S supply falls below $V_{Sth(ON)} – V_{Sth(Hyst)}$, the device returns in UVLO status until the turn-on threshold is exceeded again by Vs.

If during the operation the V_{DD} supply falls below $V_{DDth(ON)} – V_{DDth(Hyst)}$, the device is powered down, power stages are disabled, and all the circuitry (charge pump included) is switched off. When VDD supply rises above $V_{DDth(ON)}$ the device is in UVLO condition and the charge pump is switched on; the device returns operative as soon as VBOOT rises above the $V_{BOth(ON)}$ threshold.

If during the operation the V_{BOOT} supply falls below $V_{BOth(ON)} – V_{BOth(Hyst)}$, the device returns in UVLO status until the turn-on threshold is exceeded again.

In UVLO condition, all the MOSFETs are off and the nFAULT is low.

Figure 3. Power-up and power-down sequences



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5.2 Power stages and charge pump circuitry

The STSPIN948 integrates power NMOS half-bridges. The input PWM signal drives a corresponding half-bridge according to the driving mode selected (see Section 5.4 Driving logic). In order to achieve a precise duty-cycle and low jitter between different half-bridge activation, the propagation delay of PWM signals is optimized. Cross conduction is prevented thanks to a deadtime between high-side and low-side MOSFET status change.

A blanking circuitry filters the internally generated noise at each commutation of the power stages.

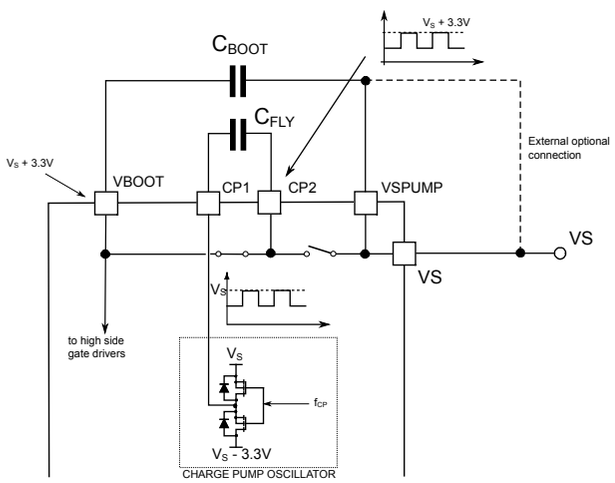
Each gate driving circuit for the high-side MOSFETs is supplied through a charge pump circuitry. The voltage VBOOT is obtained through an internal oscillator with integrated switches and external capacitors implementing a charge pump circuit as shown in Figure 4.

The slew rate of the power bridges output is set according to the value of the resistor connected to the SR pin as reported in Table 7.

Table 7. Slew rate selection

R_{SR} (± 5%)	Output slew rate (typ) [V/ns]
1 kΩ	2
2.2 kΩ	1.2
5.6 kΩ	0.6
10 kΩ	0.3

Figure 4. Charge pump circuitry



5.3 Integrated operational amplifiers

The device integrates two operational amplifiers with fixed A_{CL} amplification factor. The amplifier inputs are connected to the pins SENSEA and SENSEB.

The output is made externally available through a dedicated pin (VA and VB).

Two pins are also available (OFFSETA and OFFSETB) to allow a voltage level shift. When forced high, the corresponding amplifier output is shifted by $V_{DD}/2$.

5.4 Driving logic

The device supports five different driving modes according to the status of three input pins as listed in Table 8:

1. Dual independent full-bridge – fixed OFF-time
2. Dual half-bridge (parallel mode) – fixed OFF-time
3. Dual full-bridge (mixed decay operation) – fixed OFF-time
4. Dual independent full-bridge – PWM trimming
5. Dual half-bridge (parallel mode) – PWM trimming

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Table 8. Driving mode selection

MODE1	MODE2	MODE3	Mode	Current limiter mode
LOW	LOW	LOW	Reserved	Reserved
LOW	HIGH	LOW	Dual independent full-bridge	Fixed OFF-time
HIGH	LOW	LOW	Dual half-bridge (parallel mode)	Fixed OFF-time
HIGH	HIGH	LOW	Dual full-bridge (mixed decay)	Fixed OFF-time with mixed decay
LOW	LOW	HIGH	Reserved	Reserved
LOW	HIGH	HIGH	Dual independent full- bridge	PWM trimming
HIGH	LOW	HIGH	Dual half-bridge (parallel mode)	PWM trimming
HIGH	HIGH	HIGH	Reserved	Reserved

Important: It is not allowed to switch from one driving mode to another one during operation. In application, the MODE1, MODE2, and MODE3 inputs should be shorted to ground, left floating, or shorted to VDD.

MODE1, MODE2 and MODE3 inputs integrate an internal pull-up resistor.
PWM1A, PHA, PWM1B, PHB, OFFSETA, OFFSETB, and nSTDBY inputs have internal pull-down resistors.
EN/nFAULTA and EN/nFAULTB inputs have an internal pull-down current.

5.4.1 Dual independent full-bridge mode

In dual independent full-bridge mode:

- The outputs of each full-bridge are controlled by the respective PWM1x and PHx inputs
- The status of the power bridge is determined by the corresponding current limiter (A or B). When triggered, low-side MOS is turned on and slow decay is performed (see Section 5.6.1.1)
- If a fault condition occurs on full-bridge A, the EN/nFAULTA pin is forced low and both the half-bridges (1A and 2A) are disabled
- If a fault condition occurs on full-bridge B, the EN/nFAULTB pin is forced low and both the half-bridges (1B and 2B) are disabled

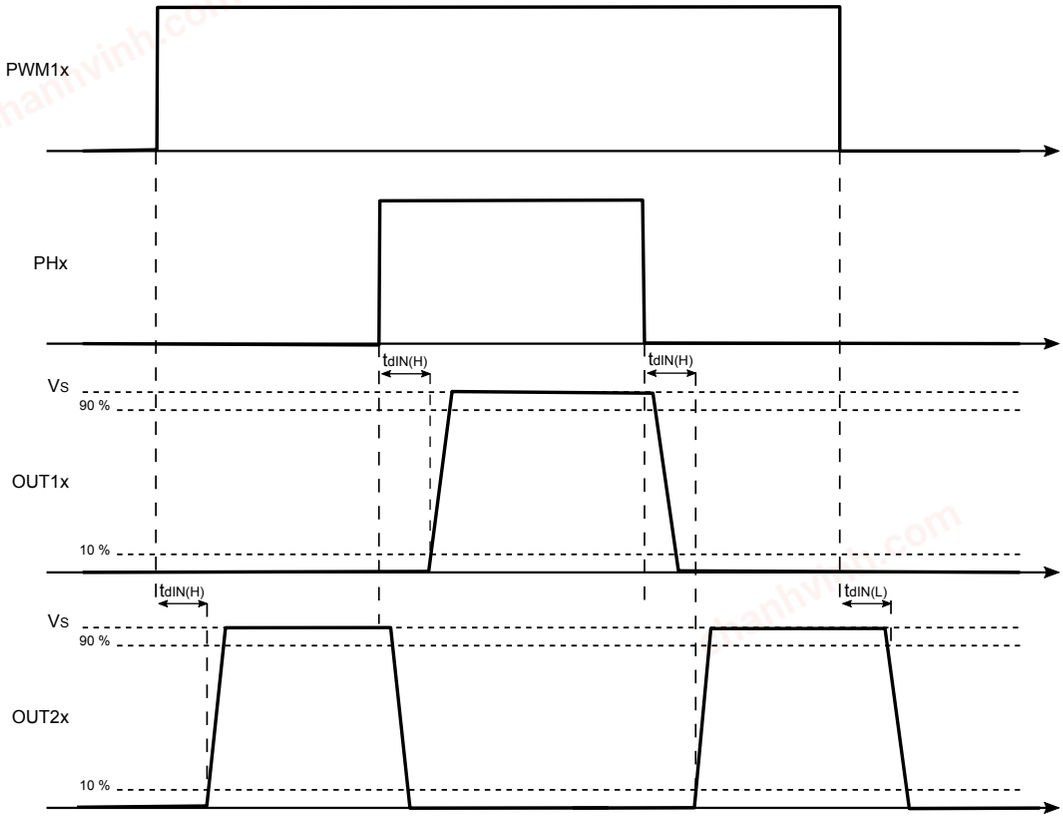
Table 9. Truth table – dual independent full-bridge mode

ENx	PWM1x	PHx	OUT1x	OUT2x
0	X(1)	X(1)	High-Z(2)	High-Z(2)
1	0	X	LS on	LS on
1	1	1	HS on	LS on
1	1	0	LS on	HS on

1. *X: don't care.*
2. *High-Z: high impedance.*

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Figure 5. **Driver time diagram - dual independent full-bridge mode**



5.4.2 Dual half-bridge mode - parallel operation

In this mode, two half-bridges are driven in parallel (1A with 2A and 1B with 2B) to obtain two high-current and low-resistance paths:

- PWM1A, PWM1B, PHA, and PHB drive the half-bridges as reported in Table 10.
- Current limit circuitry connected to Vx and REFx operates for both the half-bridges. when triggered slow decay is performed and the decay mode is selected through PHx (see Section 5.6.1.2 and Section 5.6.2.2):
  - if PHx is low, low-side MOS is turned on
  - if PHx is high, output is in high-Z
- If a fault condition occurs on full-bridge A, the EN/nFAULTA pin is forced low and both the half-bridges (1A and 2A) are disabled
- If a fault condition occurs on full-bridge B, the EN/nFAULTB pin is forced low and both the half-bridges (1B and 2B) are disabled

This operation mode requires short-circuiting the following pins:

- OUT1A and OUT2A
- LSS1A and LSS2A
- OUT1B and OUT2B
- LSS1B and LSS2B

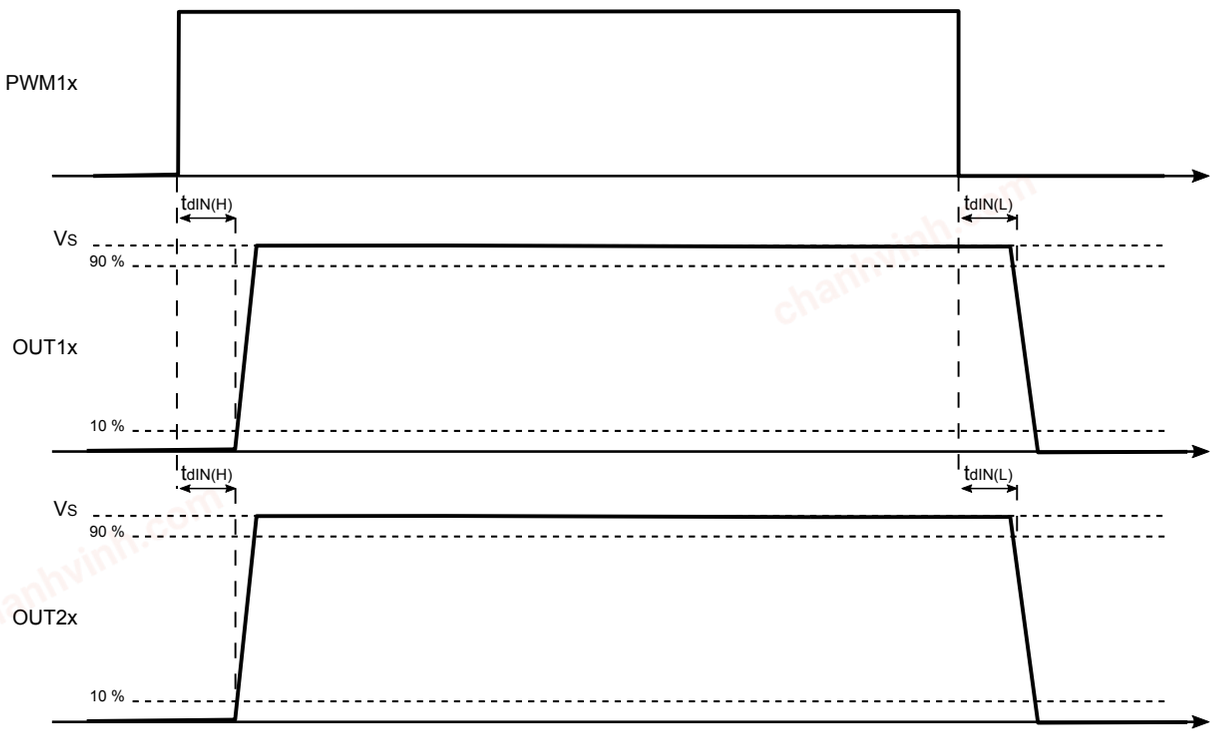
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Table 10. Truth table – dual half-bridge mode (parallel operation)

ENx	PWM1x	PHx	OUT1x/2x
0	X(1)	X(1)	High-Z(2)
1	0	See Section 5.6.1.2 and Section 5.6.2.2	LS on
1	1	See Section 5.6.1.2 and Section 5.6.2.2	HS on

1. *X: don't care.*
2. *High Z: high impedance.*

Figure 6. Driver time diagram - dual half-bridge mode (parallel operation)



5.4.3 Dual full-bridge mode – mixed decay operation

This mode is available only with the current limiter set in fixed OFF-time. The device is driven similarly to "Dual independent full-bridge mode" (see Section 5.4.1); however, when current limiter is triggered, a mixed decay is performed as described in Section 5.6.1.3.

5.5 Standby

The device provides a low consumption mode. In this condition, the charge pump circuitry is turned off.

The device enters the standby mode by forcing low the nSTBY input for at least t_{STBY}. As soon as the input is high, the device returns operative after t_{WAKE} + t_{BOOT}.

In low consumption mode, the EN/nFAULT pin should not be left floating at any times.

During the wake-up, the device is in Under Voltage Lock Out condition (UVLO) until the VBOOT supply voltage rises above the $V_{BOth(ON)}$ threshold. After t_{BOOT}, the charge-pump circuitry charges the bootstrap capacitor and the device becomes operative.

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5.6 PWM current control

The device integrates two independent current limiters internally connected to the V1A and V1B pins.

The input voltage of the amplifier (V_{SENSEx}), the voltage drop of an external shunt resistor connected between LSS1x and ground, is amplified by A_{CL} and output at V1A or V1B. These voltages are compared with the respective reference voltage (V_{REFA} or V_{REFB}). When $V_{1x} > V_{REFx}$ the comparator triggers and the device operates according to the selected decay strategy. The reference voltage value, V_{REFx}, must be selected according to the load current target value (peak value), the gain of the embedded amplifier (A_{CL}) and the sense resistors value.

Equation 1

$$V_{REFx} = R_{SENSE} \times A_{CL} + V_{AMPoffset} + V_{AMPoffset} \quad (1)$$

where $V_{AMPoffset}$ is equal to 0 (OFFSETx is low) or $V_{DD}/2$ (OFFSETx is high).

Two current limiter modes are available:

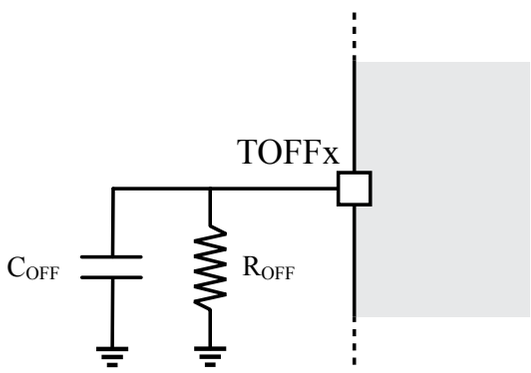
1. Fixed OFF-time
2. PWM trimming

5.6.1 Fixed OFF-time mode

When V_{1x} exceeds V_{REFx} the control circuitry sets the device in limiting status to reduce the current. During the t_{OFF} time, the commutation of the PWMx inputs are ignored.

The device returns to normal operation after a t_{off} time set according to the values of the R_{OFF} resistor and the C_{OFF} capacitor connected to TOFFx pin as shown in Figure 7.

Figure 7. OFF-time regulation circuit

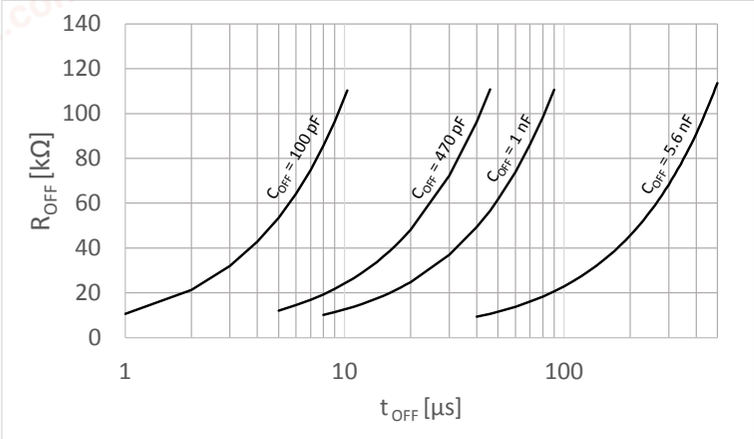


The recommended values for R_{OFF} and C_{OFF} are shown in Figure 8.

Short-circuiting TOFFx to ground disables the current limiter.

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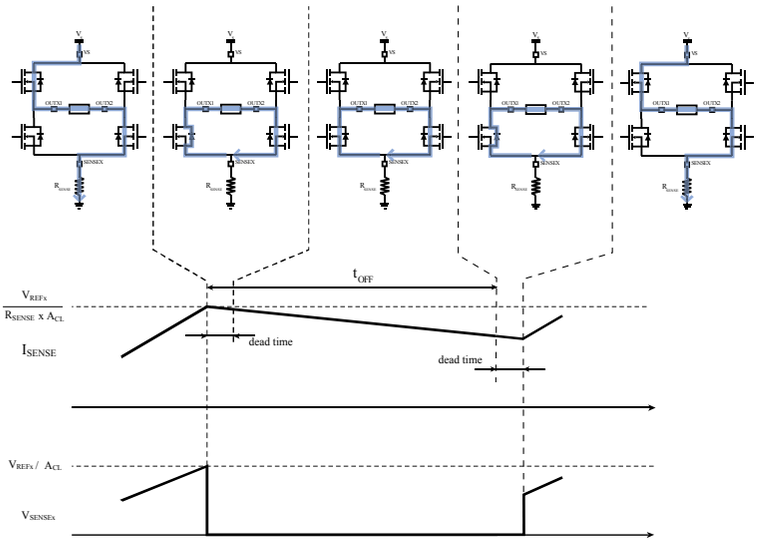
Figure 8. t_{OFF} vs. R_{OFF} and C_{OFF}



5.6.1.1 *Full-bridge operation mode (fixed OFF-time)*

In full-bridge operation mode, the current is limited turning on both the low-side MOS of the full-bridge (slow decay). As soon as the OFF-time expires the bridges return in the ON state (see Figure 9).

Figure 9. **Current control in full-bridge mode (fixed OFF-time)**



5.6.1.2 *Half-bridge parallel operation mode (fixed OFF-time)*

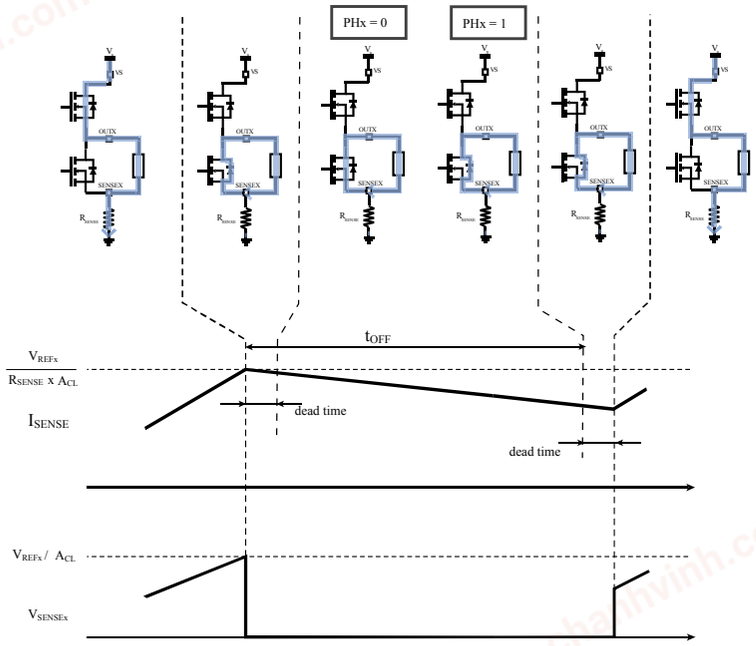
In half-bridge parallel operation mode, the decay strategy is determined by the status of PHx:

- PHx is low: the low-side MOS is switched on
- PHx is high: the output is in high impedance (current recirculates in the body diode)

As soon as the OFF-time expires the bridges return in the ON state (see Figure 10).

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Figure 10. **Current control in half-bridge parallel mode (fixed OFF-time)**

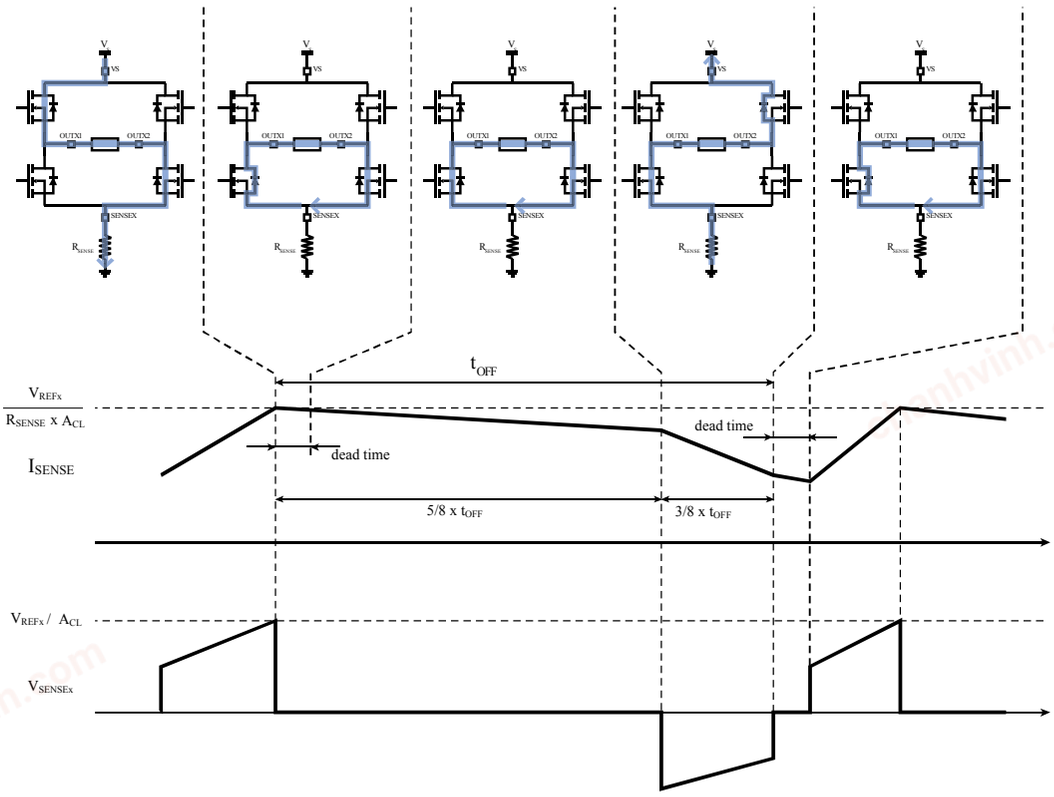


5.6.1.3 *Mixed decay operation mode (fixed OFF-time)*

In mixed decay operation mode, the current is limited turning on both the low-side MOS of the full-bridge (slow decay), the system switches from slow decay to quasi-synchronous fast decay (the sinking side of the bridge is put in high impedance) when the counter reaches a fixed threshold corresponding to a 5/8th of the total decay time (t_{OFF}).

As soon as the OFF-time expires the bridges return in the ON state (see Figure 11).

Figure 11. **Current control in mixed decay mode (fixed OFF-time)**



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5.6.2 PWM trimming mode

When V_{1x} exceeds V_{REFx} the control circuitry sets the device in limiting status to reduce the current. The decay strategy and the return to normal operation depends on the selected driving mode: full-bridge or parallel operation mode (mixed decay is not available with this current limiter mode).

In PWM trimming mode the TOFFx pin is a digital output and it is forced low during the current decay time.

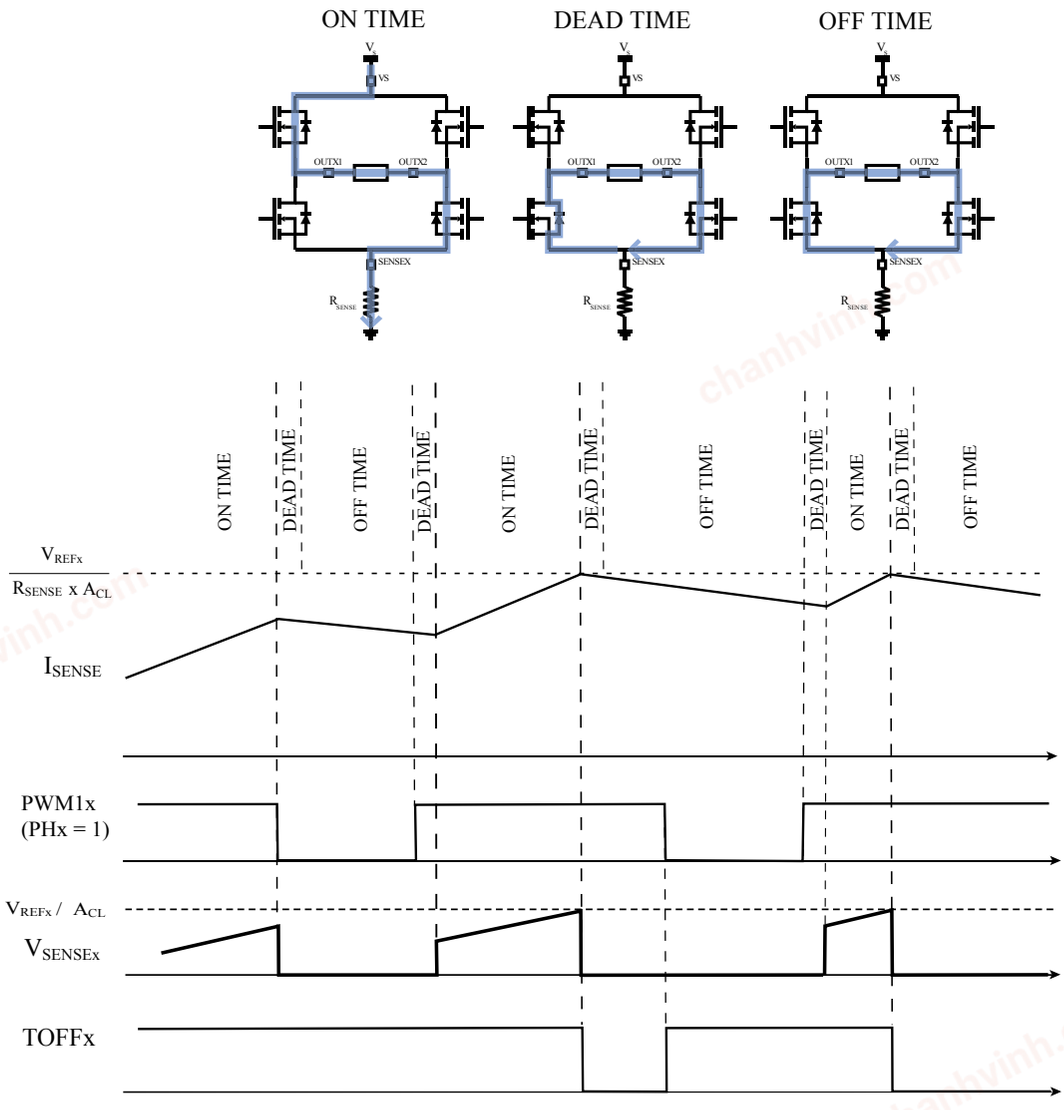
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5.6.2.1 *Full-bridge operation mode (PWM trimming)*

In full-bridge operation mode, the current is limited turning on both the low-side MOS of the full-bridge (slow decay, see Figure 12). The device returns to normal operation if one of the following conditions occurs:

- nSTDBY is set low
- EN/nFAULTx is set low
- PWM1x is set low

Figure 12. Current control in full-bridge mode (PWM trimming)



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5.6.2.2 *Half-bridge parallel operation mode (PWM trimming)*

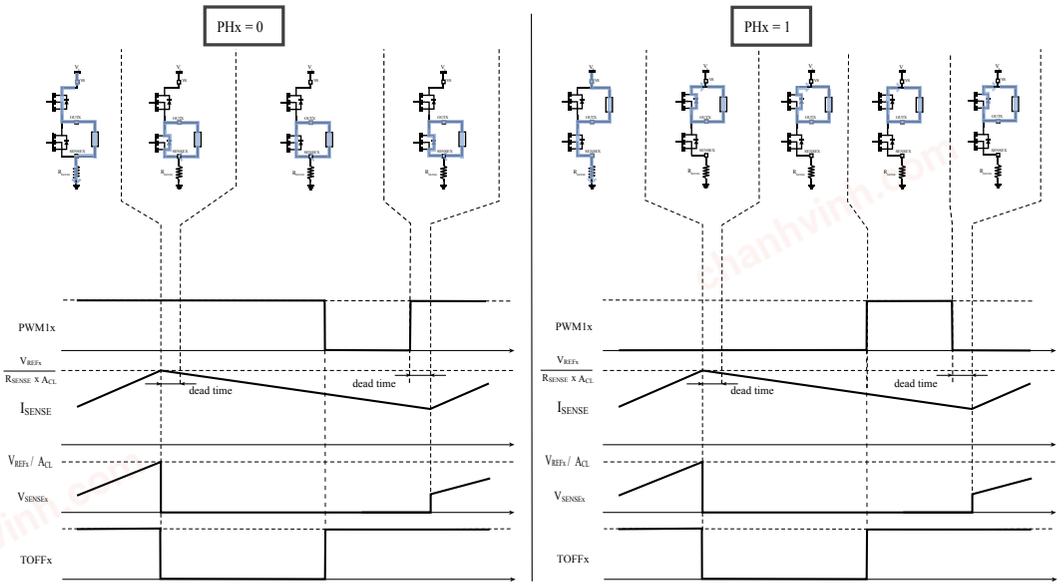
In half-bridge parallel operation mode, the decay strategy is determined by the status of PHx (see Figure 13):

- PHx is low: the low-side MOS is switched on
- PHx is high: the output is in high impedance (current recirculates in the body diode)

The device returns to normal operation if one of the following conditions occurs:

- nSTDBY is set low
- EN/nFAULTx is set low
- PWM1x is set low, if PHx = 0
- PWM1x is set high, if PHx = 1

Figure 13. Current control in half-bridge parallel mode (PWM trimming)



5.6.3 Blanking

In order to avoid spurious triggering of the current limiter's comparator due to both internal and external noise (ringing, diode's recovery currents, etc.), the device integrates a blanking circuitry.

Each full-bridge (A and B) has an independent blanking signal (no cross-blanking). The blanking signal is generated at each commutation of the full-bridge A or B.

When the bridge is in high impedance, blanking condition is always imposed.

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5.7 Overcurrent protection

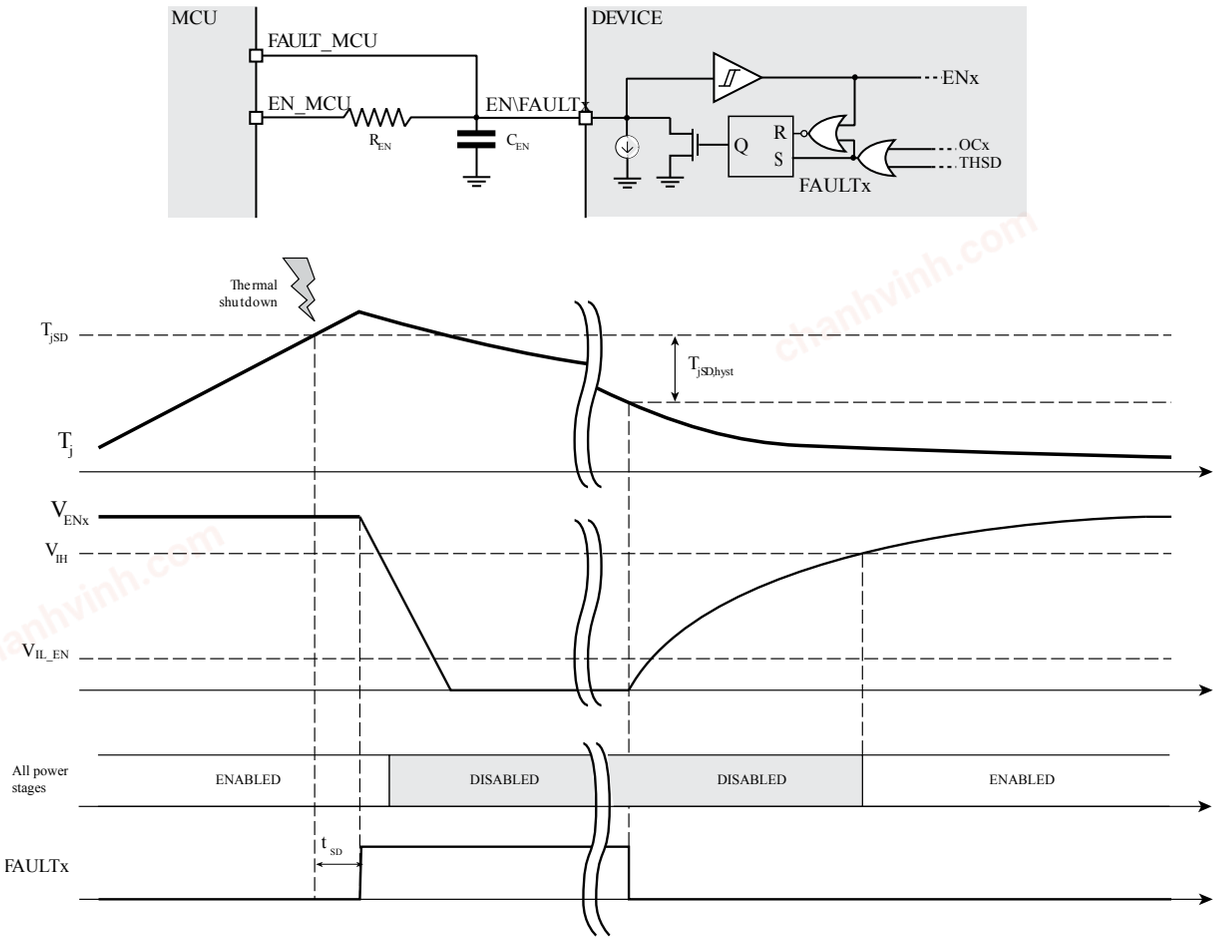
An integrated circuitry, independent from the current limiter, protects the power stage from overcurrent condition.

If the current flowing into one of the integrated MOSFETs exceeds the I_{OC} threshold, the OC protection turns off all the MOSFETs and forces low the EN/nFAULTx open drain output.

The device holds this condition until the nFAULT input voltage falls below the V_{IL_EN} threshold.

In order to avoid spurious triggering due to noise, a deglitch filter with t_{OCSD} (OC protection) period is implemented.

Figure 14. Overcurrent protection timings



The total disable time after an overcurrent event can be set properly sizing the external network connected to the EN\nFAULT pin.

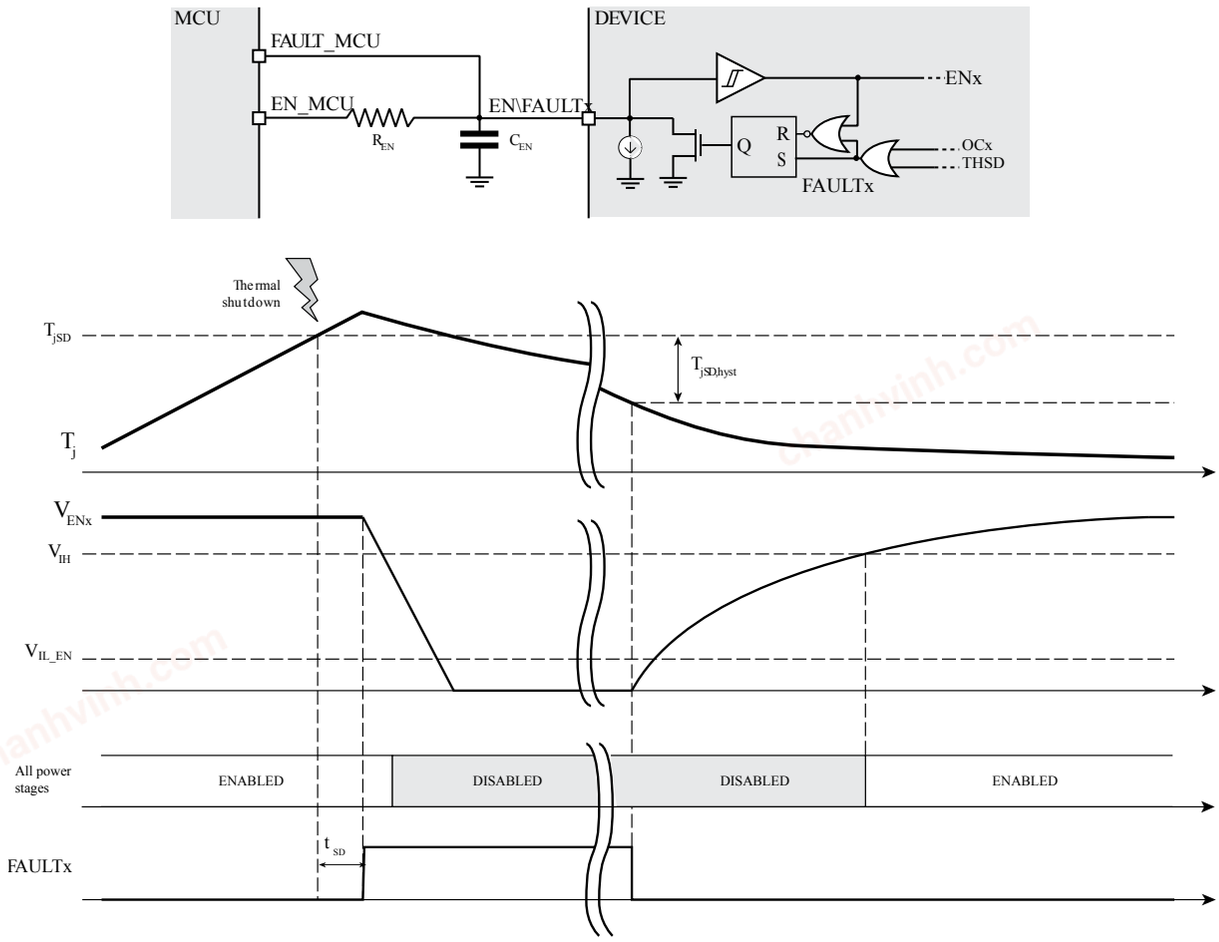
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5.8 Thermal shutdown

The device integrates a thermal shutdown protection. When the internal temperature exceeds the T_{SD} temperature, the power stage is disabled until the temperature returns below T_{SD} - $T_{SD(Hyst)}$.

When the device is in thermal shutdown, the nFAULTA and nFAULTB outputs are forced low (see Figure 15).

Figure 15. Thermal shutdown sequence



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6 Characterization graphs

Figure 16. Output slew rate vs. temperature (V_S = 58 V, normalized at T_J = 25 °C)

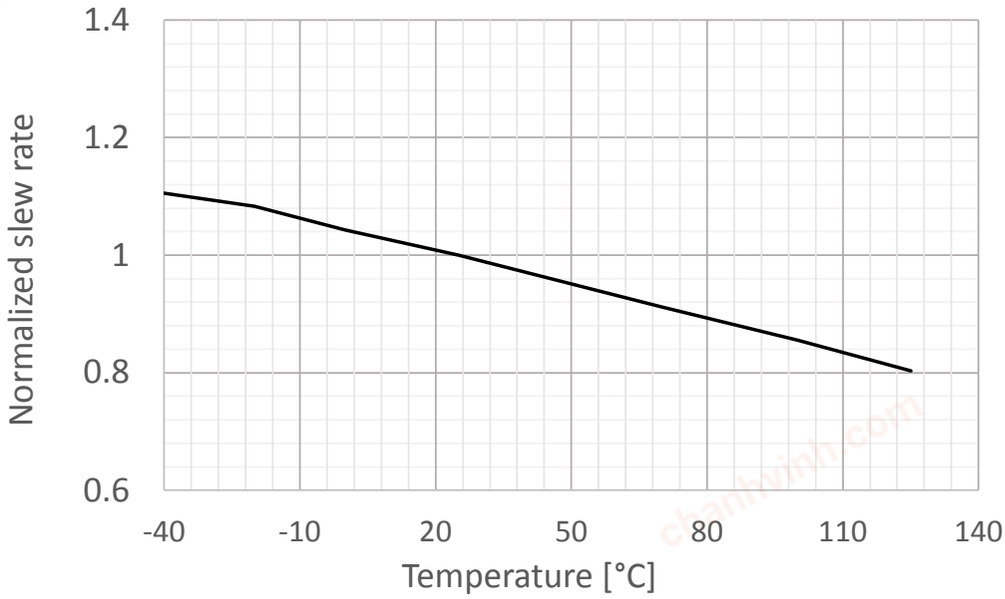
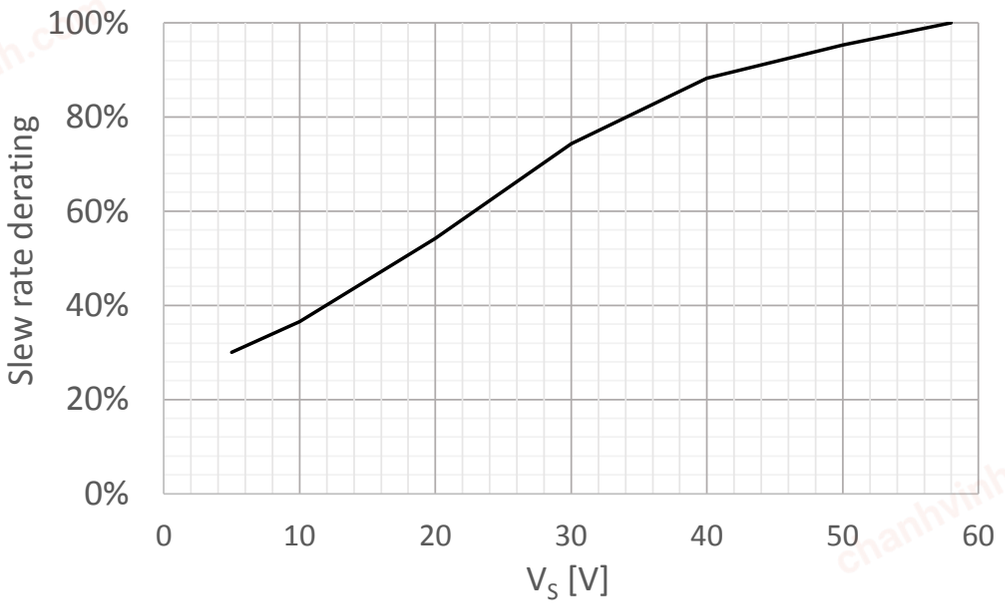


Figure 17. Output slew rate derating vs. supply voltage (T_J = 25 °C)



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Figure 18. **Overcurrent threshold vs. temperature (V_S = 58 V, normalized at T_J = 25 °C)**

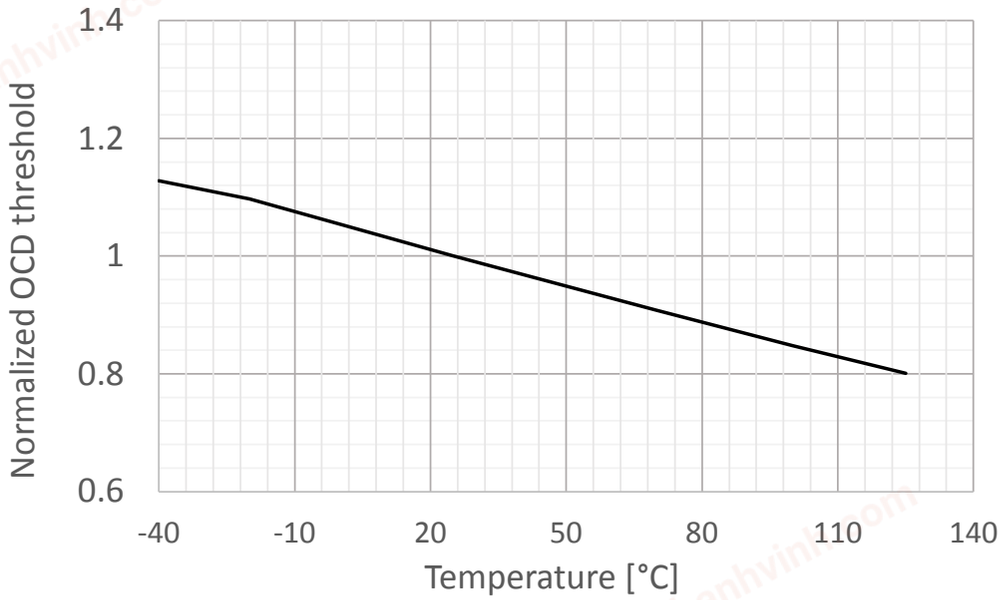
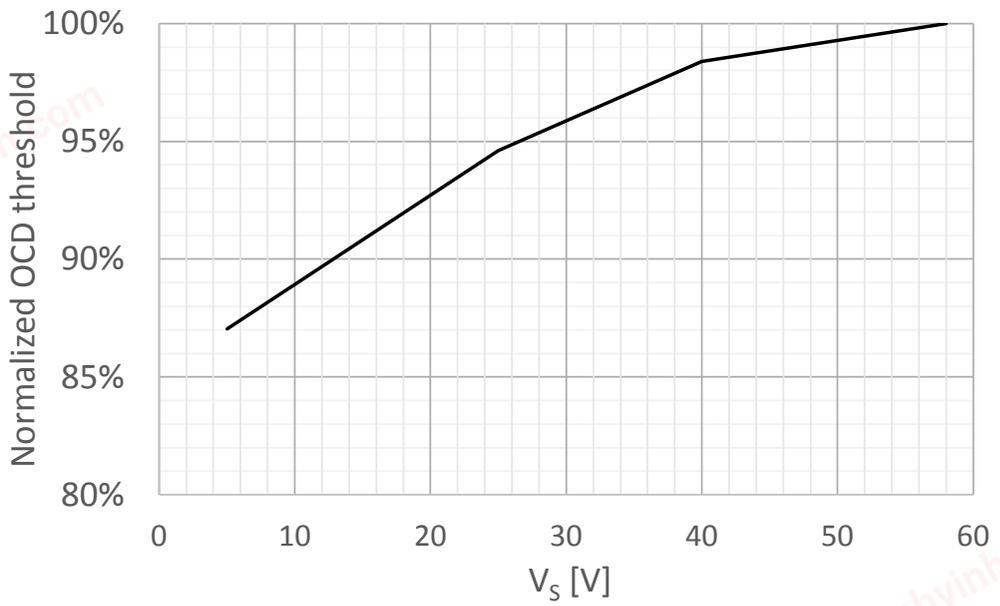
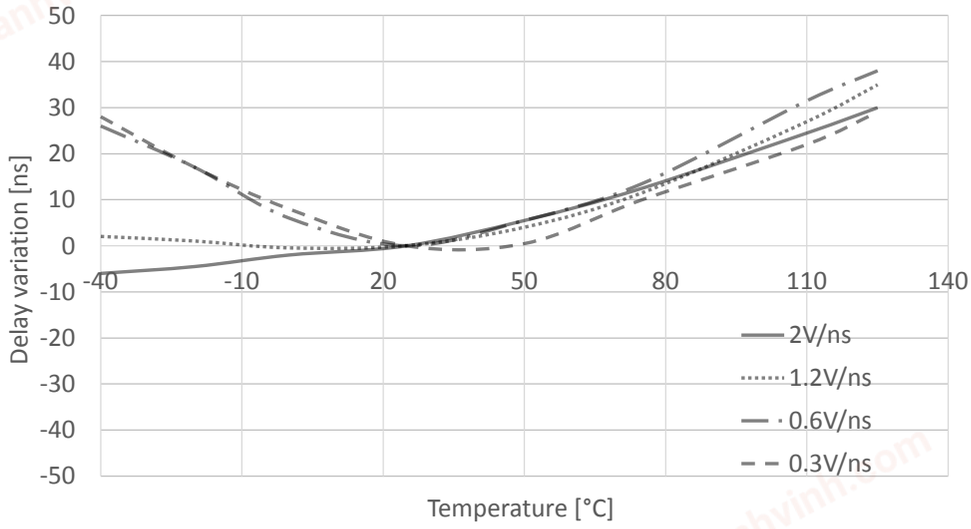


Figure 19. **Overcurrent threshold vs. supply voltage (T_J = 25 °C, normalized at V_S = 58 V)**



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Figure 20. **PWM input to output propagation delay vs. temperature (referenced to T_j = 25 °C) T**



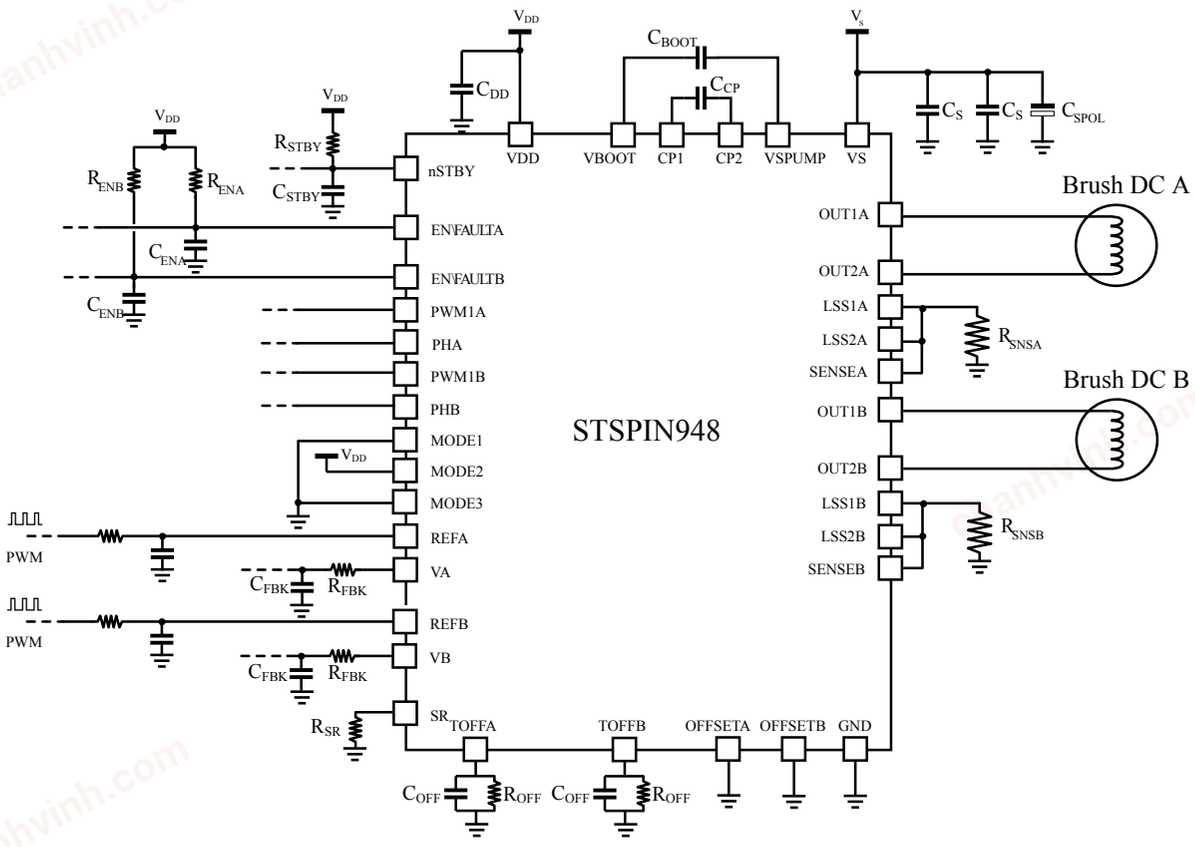
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7 Typical application

Table 11. **Typical application value**

Name	Value
C_S	470 nF
C_{BULK}	220 µF
C_{DD}	220 nF
C_{CP}	100 nF
C_{BOOT}	1 µF
R_{SNSA}, R_{SNSB}	50 mΩ / 3W
C_{ENA}, C_{ENB}	10 nF
R_{ENA},R_{ENB}	39 kΩ
C_{STBY}	1 nF
R_{STBY}	18 kΩ
R_{OFF}, C_{OFF}	22 kΩ, 1 nF (t_{OFF} = 18 µs)
C_{FBK}	100 pF
R_{FBK}	100 Ω
R_{SR}	5.6 kΩ (SR = 0.6 V/ns)

Figure 21. **Typical application schematic**



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8 Layout guidelines

Two 470 nF bypass capacitors must be connected between the VS supply voltage pins and ground and one 220 nF bypass capacitor must be connected between the VDD supply pin and ground.

These capacitors must be low-ESR ceramic technology and placed as close to the pins as possible (VS and VDD pins) with a thick ground plane connection to the device GND pin.

A bulk capacitor is required to bypass the high current path. One or more capacitors should be placed as to minimize the length of high current paths between VS and GND. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers.

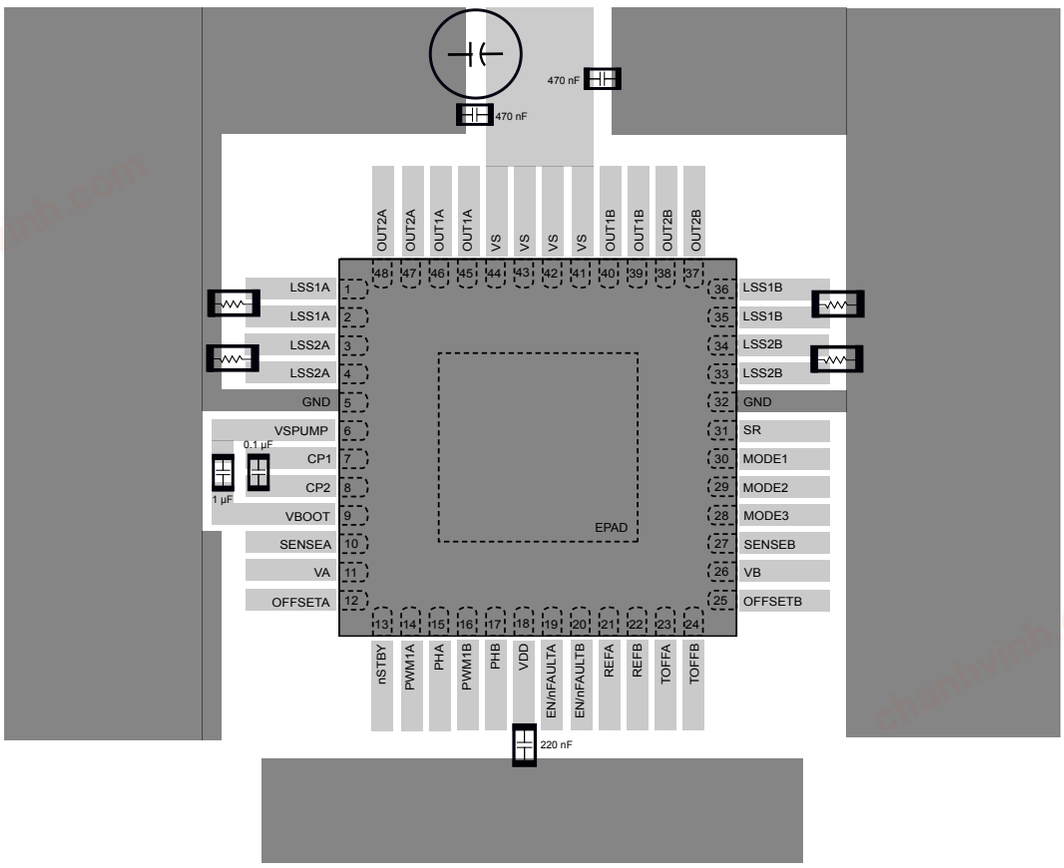
In application requiring the device switching at high slew rates or with high output currents, ground layers should be designed to separate digital and power ground. In this case, the exposed PAD must be connected to the power ground and the VDD bypass capacitor to the digital ground. The path between the ground of the shunt resistors and the ceramic bypass capacitor of the device is critical; for this reason it must be as short as possible minimizing parasitic inductances that can cause voltage spikes on the SENSE and OUT pins.

The current sense resistors should be placed as close as possible to the device pins to minimize trace inductance between the device pin and resistors avoiding, where possible, to place them on a different board layer.

A low-ESR ceramic capacitor must be placed between the CP1 and CP2 pins (100 nF, rated for 16V) and between the VBOOT and VSPUMP pins (1 µF, rated for 16 V).

A layout example is shown in Figure 22. Layout example.

Figure 22. Layout example



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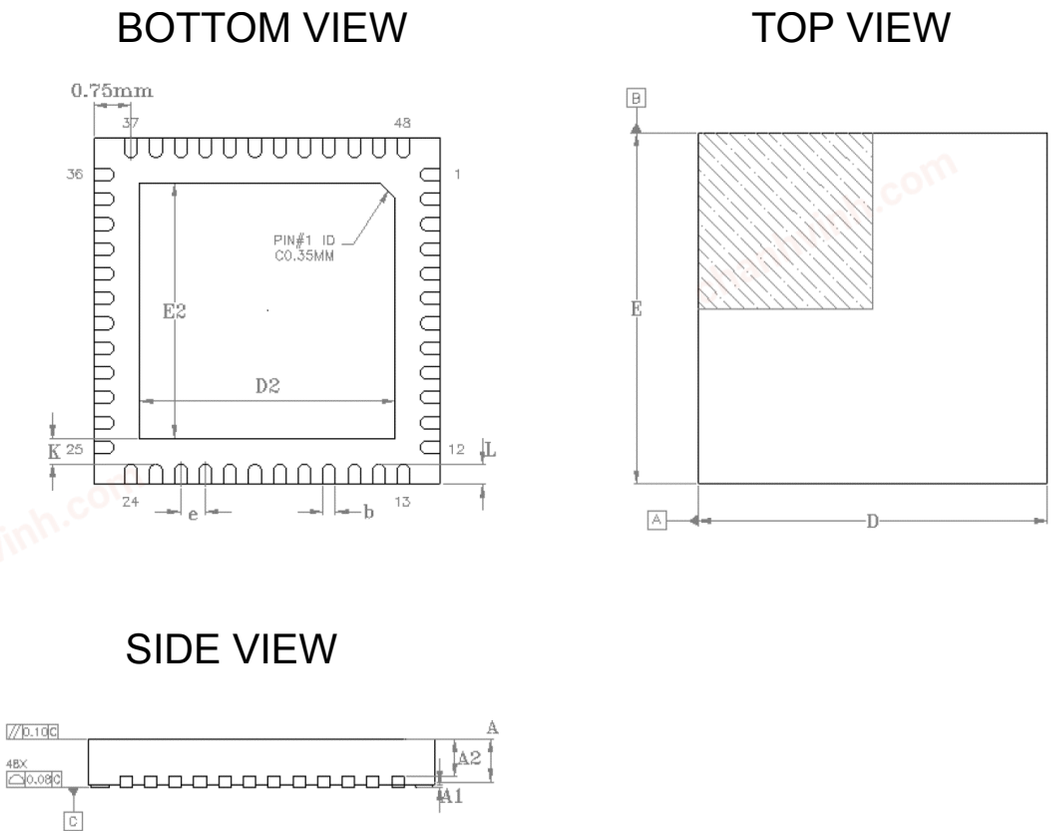
9 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at www.st.com. ECOPACK is an STMicroelectronics trademark.

A customized VFQFPN48 7 x 7 package is proposed. A smaller EPAD, internally connected to the ground pin, is desired to place through holes on the bottom of the package. Lead plating is Nickel/Palladium/Gold (Ni/Pd/Au).

9.1 VFQFPN48 7 x 7 package information

Figure 23. VFQFPN48 (7 x 7 x 1.0 mm) package outline

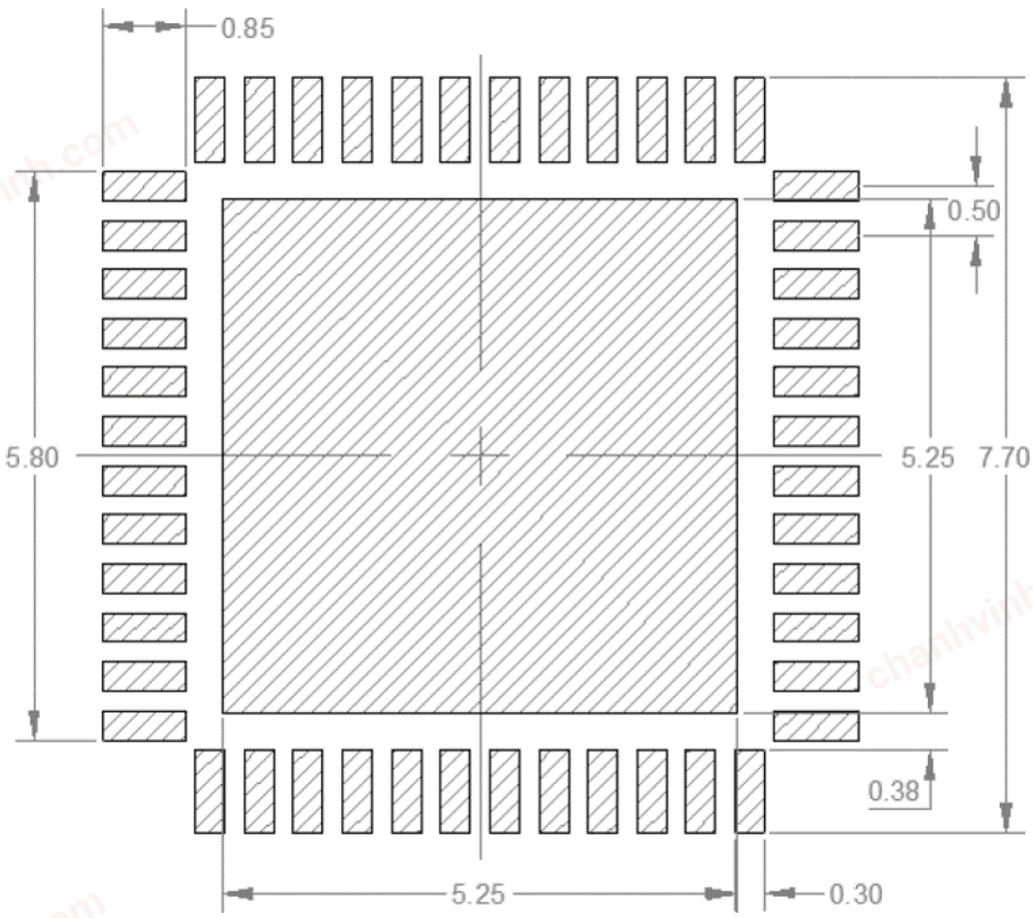


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Table 12. **VFQFPN48 (7 x 7 x 1.0 mm) package mechanical data**

Dim.	(mm)		
	Min.	Typ.	Max.
A	0.80	0.9	1.00
A1		0.02	0.05
A2		0.75	
A3		0.20	
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D2	5.05	5.15	5.25
E	6.85	7.00	7.15
E2	4.95	5.15	5.25
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 24. **VFQFPN48 (7 x 7 x 1.0 mm) recommended footprint**



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10 Ordering information

Table 13. **Device summary**

Order code	Package	Packaging
STSPIN948TR	VFQFPN 7 x 7 x 1 – 48 L	Tape and reel
STSPIN948	VFQFPN 7 x 7 x 1 – 48 L	Tray

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Revision history

Table 14. **Document revision history**

Date	Version	Changes
07-Jul-2023	1	Initial release.
25-Oct-2023	2	Added P/N in Table 13

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