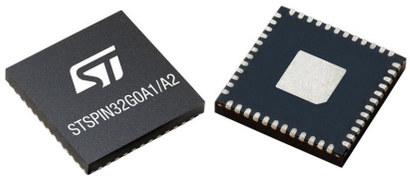
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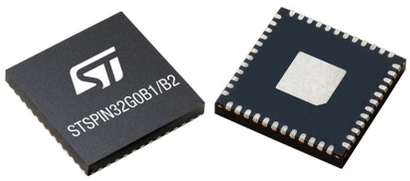
STSPIN32G0A1/A2/B1/B2

Datasheet

Advanced brushless motor controller with embedded STM32G0 MCU



VFQFPN 48L 7x7x1 mm



VFQFPN 48L 7x7x1 mm

STSPIN

Product status link
STSPIN32G0A1
STSPIN32G0A2
STSPIN32G0B1
STSPIN32G0B2

Product label
SUSTAINABLE TECHNOLOGY

Features

- Operating voltage from 6.7 to 45 V
- Three-phase gate drivers:
  - 600 mA sink/source
  - Integrated bootstrap diodes
  - Cross-conduction prevention
- 32-bit ARM® Cortex™-M0+ core:
  - Up to 64 MHz clock frequency
  - 8-kbyte SRAM with hardware parity check
  - 64-kbyte flash memory with protection and securable area
- 3.3. V DC-DC buck converter regulator with overcurrent, short-circuit, and thermal protection
- 12 V LDO linear regulator with thermal protection
- Up to 23 fast I/O ports (GPIO)
- 5-channel DMA controller with flexible mapping
- 12-bit ADC (up to 11 external channels) with 2.5 Msps conversion rate
- Advanced-control timer dedicated for motor control
- Up to 5 general purpose timers (1 x 32-bit + 4 x 16-bit)
- I^2C, USART, and SPI interfaces
- Up to 3 rail-to-rail operation amplifiers for signal conditioning
- Comparator for overcurrent protection
- Standby mode for low power consumption
- UVLO protection on each power supply:
  - V_M, V_{DD}, V_{REG}, and V_{BOOTx}
- On-chip debug support via SWD and embedded bootloader through UART and I^2C
- Extended temperature range: -40 to +125 °C

Applications

- Battery supplied power tools
- Portable vacuum cleaners
- Pumps and fans
- E-bike
- Lawn mover
- Industrial automation

Description

The STSPIN32G0 is a family of highly integrated system-in-package providing solution suitable for driving three-phase brushless motors using different driving modes extremely reducing the BOM and area.

It is composed by four part numbers, for full flexibility in balancing the resources among op-amp for current sensing, GPIOs and specifically dedicated features like a precise reference for the ADC.

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It embeds a triple half-bridge gate driver able to drive power MOSFETs with a current capability of 600 mA (sink and source). The high and low-side switches of the same half-bridge cannot be simultaneously driven high thanks to an integrated interlocking function.

An internal DC-DC buck converter provides the 3.3 V voltage suitable to supply both the MCU and external components. An internal LDO linear regulator provides the supply voltage for gate drivers.

The integrated operational amplifiers are available for the signal conditioning, for example, the current sensing across the shunt resistors.

A comparator is integrated to perform the overcurrent protection.

The integrated MCU (STM32G031x8) allows performing field oriented control, the 6-step sensorless, and other advanced driving algorithms including the speed control loop. It has the write-protection and read-protection feature for the embedded flash memory to protect against unwanted writing and/or reading.

The device also features overtemperature and undervoltage lockout protections and can be put into standby mode to reduce the power consumption. The device provides 23 general-purpose I/O ports (GPIO) , one 12-bit analog-to-digital converter with up to 11 channels performing conversions in a single-shot or scan modes, 5 synchronizable general-purpose timers and supports an easy-to-use debugging serial interface (SWD). The embedded bootloader allows flash and option byte management through UART and I^2C interfaces.

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1 Block diagrams

Figure 1. **STSPIN32G0A1 block diagram**

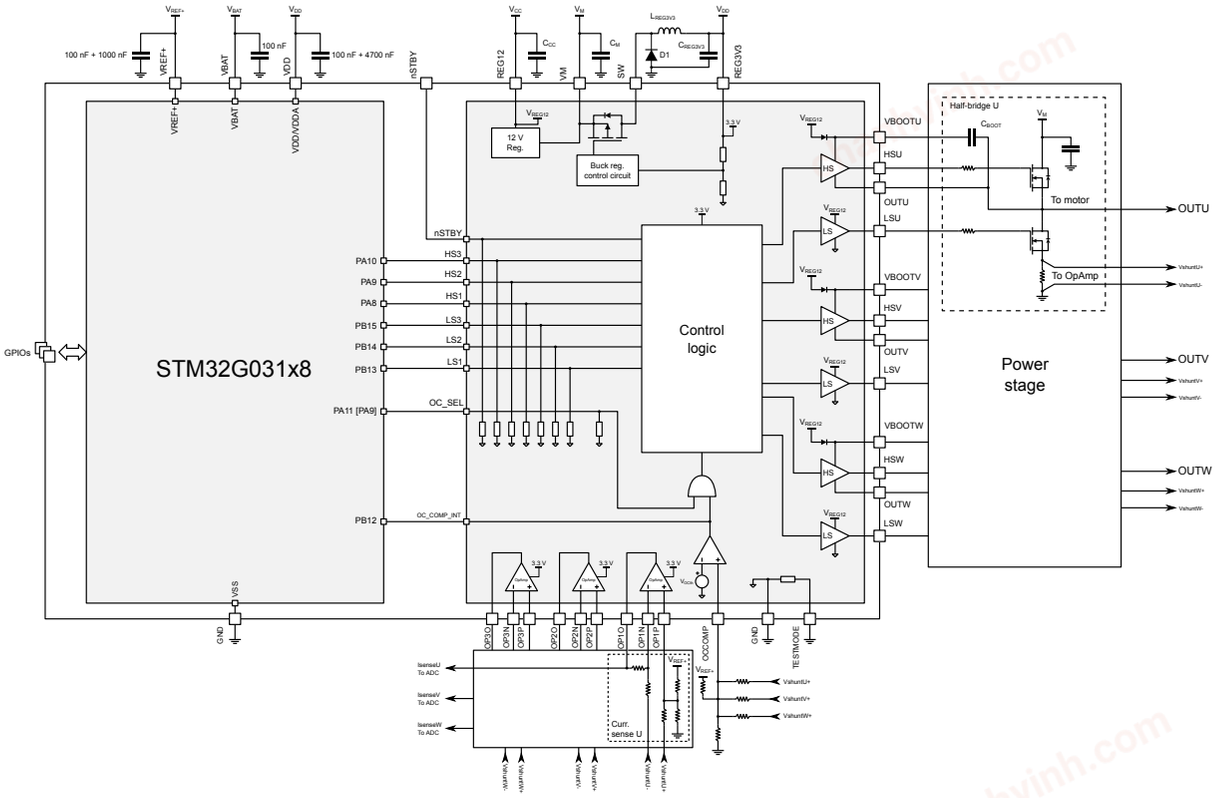
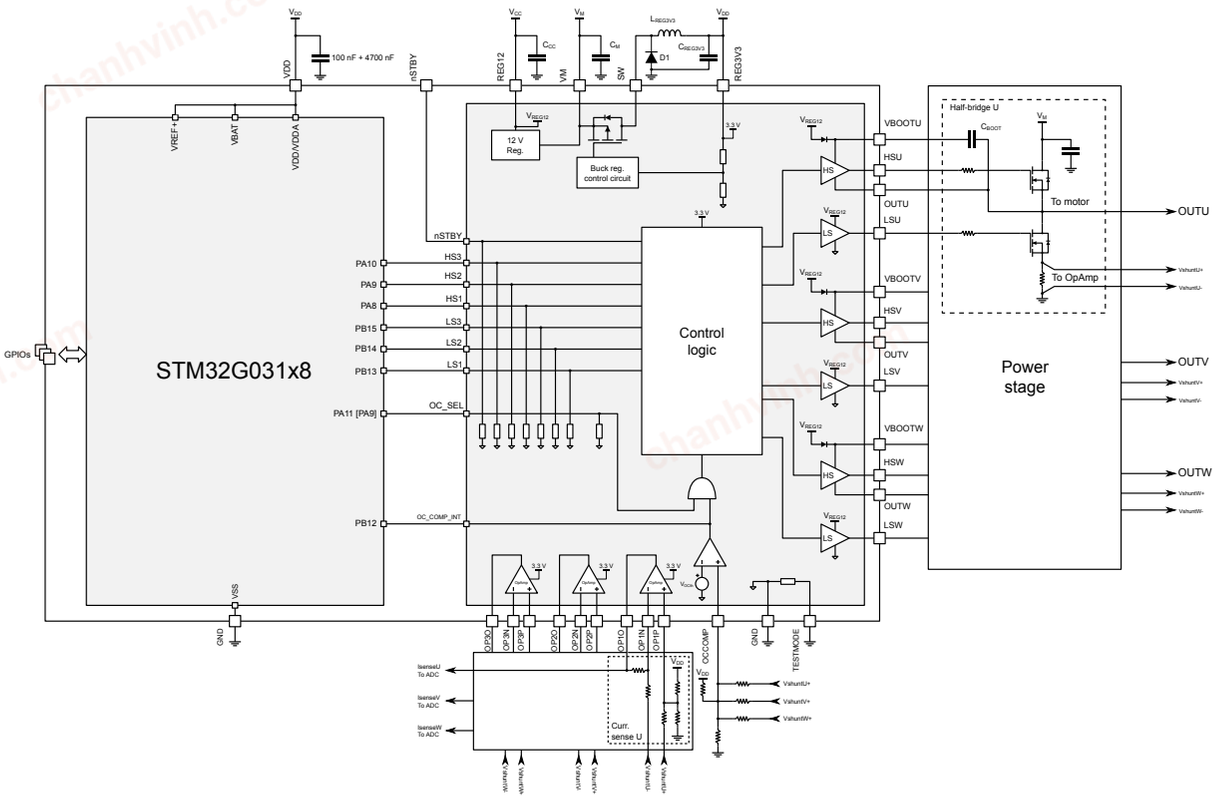


Figure 2. **STSPIN32G0A2 block diagram**



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Figure 3. **STSPIN32G0B1 block diagram**

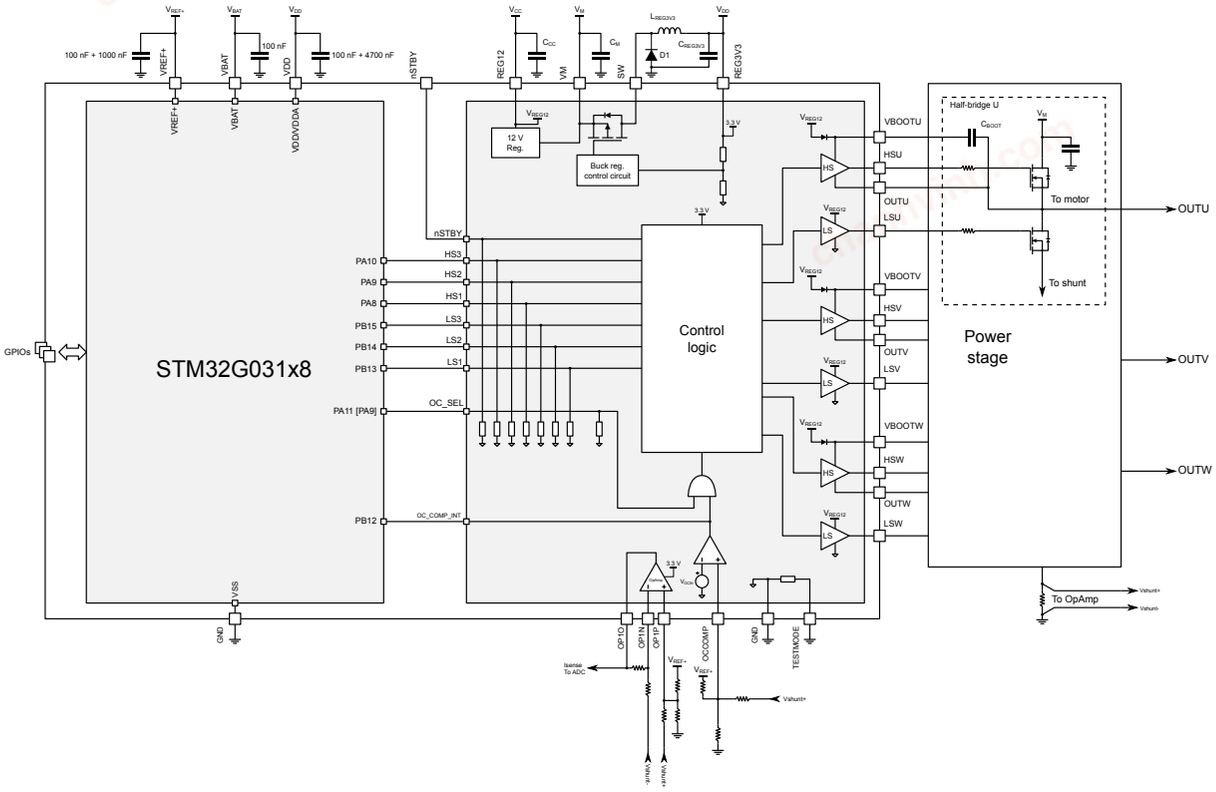
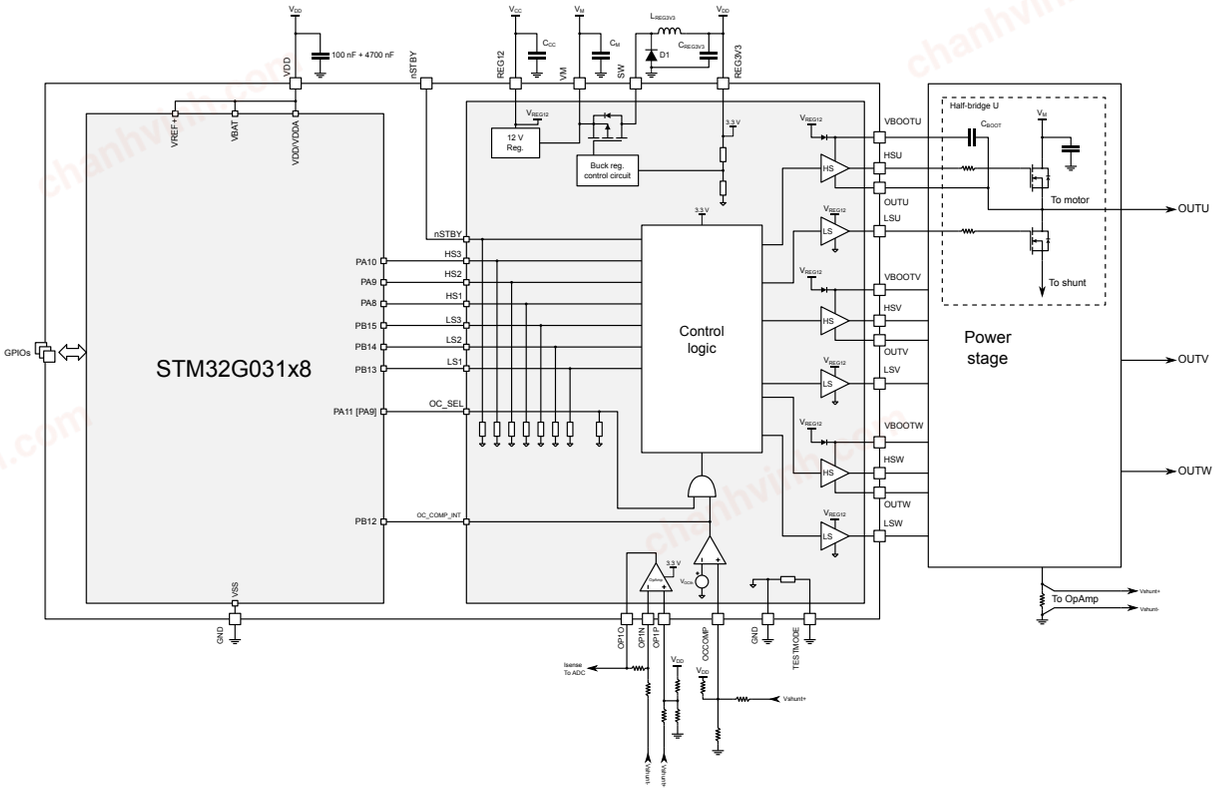


Figure 4. **STSPIN32G0B2 block diagram**



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Figure 5. **STSPIN32G0A1/A2 - analog IC block diagram**

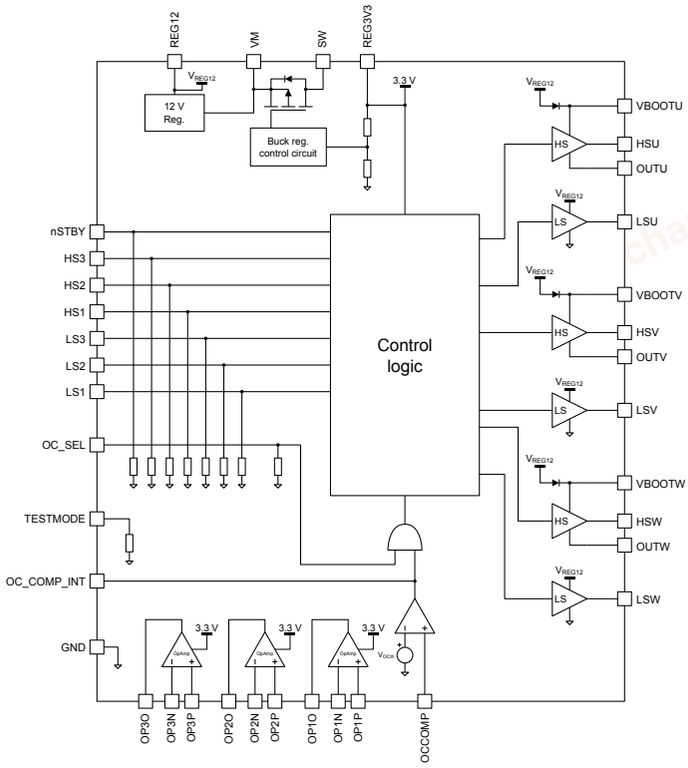
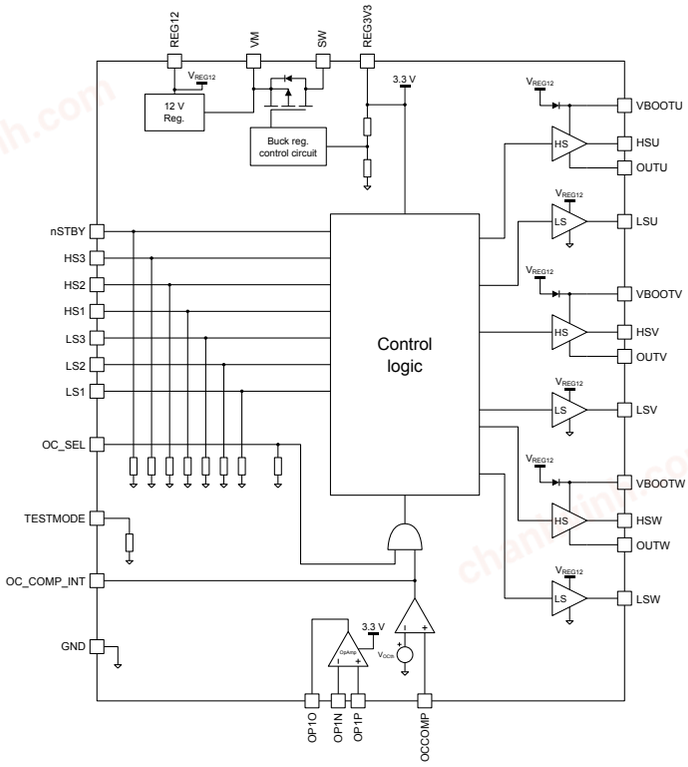


Figure 6. **STSPIN32G0B1/B2 - analog IC block diagram**



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2 Electrical data

2.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 1 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_M	Power supply voltage	-	-0.3 to 48	V
V_{REG12}	Linear regulator output and gate driver supply voltage	REG12 shorted to VM	15	V
V_{OPP}	Op amp positive input voltage	-	-0.2 to V_{DD} + 0.2	V
V_{OPN}	Op amp negative input voltage	-	-0.2 to V_{DD} + 0.2	V
V_{CP}	Comparator input voltage	-	-2 to 2	V
V_{HS}	High-side gate output voltage	-	V_{OUT} - 0.3 to V_{BOOT} + 0.3	V
V_{LS}	Low-side gate output voltage	-	-0.3 to V_{REG12} + 0.3	V
V_{BOOT}	Bootstrap voltage	-	-0.3 to 60	V
V_{OUT}	Output voltage (OUTU, OUTV, OUTW)	-	-2 to V_M + 2	V
dV_{OUT}/dt	Output slew rate	-	± 10	V/ns
V_{nSTBY}	nSTBY input voltage		-0.3 to min (V_{REG3V3} + 0.3, 4)	V
V_{IO}	MCU logic input voltage	FT_xx (1)	-0.3 to V_{DD} + 4 (2)	V
		Others (1)	-0.3 to 4	
I_{IO}	MCU I/O output current positive if sourced	FT_f (1)	-20 to 15	mA
		Others (1)	-15 to 15	
ΣI_{IO}	MCU I/O total output current	(1)	-80 to 80	mA
I_{INJ}	MCU I/O injected current	$V_{IN} < V_{SS}$ FT_xx (1)	-5	mA
		$V_{IN} > V_{DD}$ FT_xx (1)	NA (3)	
$\Sigma\lvert I_{INJ}\rvert$	MCU I/O total injected current	(1)	up to 25	mA
V_{DD}	MCU digital supply voltage	(1)	-0.3 to 4	V
I_{DD}	MCU supply current	(1)	up to 100	mA
V_{BAT}	MCU VBAT supply voltage	(1)	-0.3 to 4	V
V_{REF+}	MCU analog reference voltage	(1)	-0.3 to min (V_{DD} + 0.4, +4.0)	V
V_{REG3V3}	DC-DC regulator output voltage	(1)	-0.3 to 4	V
T_{stg}	Storage temperature	-	-55 to 150	°C
T_j	Operating junction temperature	-	-40 to 150	°C

1. *For details refer to the STM32G031x8 datasheet.*
2. *To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.*
3. *Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.*

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2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_M	Power supply voltage	-	6.7 (1)	-	45	V
dV_M/dt	Power supply voltage slope	V_M = 45 V	-	-	0.75	V/µs
V_{REG3V3}	DC-DC regulator output voltage	-	-	3.3	-	V
I_{REG3V3}	DC-DC regulator output current	-	-	-	70	mA
L_{SW}	Output inductance	-	-	22	-	µH
C_{REG3V3}	Output capacitance	-	47	-	-	µF
ESR_{REG3V3}	Output capacitor ESR	-	-	-	200	mΩ
V_{REG12}	Linear regulator output and gate driver supply voltage	13 < V_M < 45 V	-	12	-	V
		Shorted to VM	6.7 (1)	-	15	
C_{REG12}	Load capacitance	-	1	10	-	µF
ESR_{REG12}	ESR load capacitance	-	-	-	1.2	Ω
V_{BO}	Floating supply voltage (2)	-	-	V_{REG12} - 1	15	V
V_{CP}	Comparator input voltage	-	0	-	1	V
V_{DD}	MCU supply voltage (3)	-	1.7	-	3.6	V
		For VREFBUF operation	2.4	-	3.6	
		Any gate driver input high (see Table 7)	-	-	V_{REG3V3} + 0.3	
V_{BAT}	Backup operating voltage (3)	-	1.55	-	3.6	V
V_{REF+}	MCU ADC reference voltage (3)	V_{DD} ≥ 2 V	2	-	V_{DD}	V
		V_{DD} < 2 V	-	V_{DD}	-	
V_{IO}	MCU I/O input voltage (3)	V_{DD} = 3.3 V No internal pull-up or pull-down	-0.3	-	5.5	V
		With internal pull-up or pull-down	-0.3	-	V_{DD} + 0.3	
V_{nSTBY}	nSTBY input voltage	-	0	-	3.3	V
T_{amb}	Ambient temperature	-	-40		125 (4)	
T_j	Operating junction temperature	Analog IC	-40	-	130	°C
		MCU	-40	-	130	°C

1. *UVLO threshold V_{MOn_max}.*
2. *V_{BO} = V_{BOOT} - V_{OUT}.*
3. *See STM32G031x8 datasheet (suffix 3) for details.*
4. *Limited by the thermal performance of the application.*

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2.3 Thermal data

Table 3. **Thermal data**

Symbol	Parameter	Test condition	Value	Unit
$R_{th\ (JA)}$	Junction-to-ambient thermal resistance	Thermal values are calculated by simulation with the following boundary conditions: 2s2p board as per the std. JEDEC (JESD51-7) in natural convection, board dimensions: 114.3 x 76.2 x 1.6 mm, ambient temperature: 25 °C.	45.6	°C/W

2.4 Electrical sensitivity characteristics

Table 4. **ESD protection ratings**

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2017	2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS-002-2018	C3	1000	V

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3 Electrical characteristics

Testing conditions: V_M = 15 V; V_{DD} = V_{REG3V3} = 3.3 V, unless otherwise specified.

Typical values are tested at T_j = 25 °C, minimum and maximum values are guaranteed by thermal characterization in the temperature range of -40 to 125 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power supply and standby mode						
I_M	V_M current consumption	V_M = 45 V REG3V3 = 3.5 V externally supplied	-	2	2.6	mA
		nSTBY = 0 V_M = 45 VREG3V3 = 3.5 V externally supplied	-	880	1100	µA
V_{MOn}	V_M UVLO turn-on threshold	V_M rising from 0 V	6.0	6.3	6.6	V
V_{MOff}	V_M UVLO turn-off threshold	V_M falling from 8 V	5.8	6.1	6.4	V
V_{MHys}	V_M UVLO threshold hysteresis	-	-	0.2	-	V
I_{REG3V3}	V_{REG3V3} current consumption	V_M = 45 V REG3V3 = 3.5 V externally supplied	-	300	375	µA
		nSTBY = 0 V_M = 45 V REG3V3 = 3.5 V externally supplied	-	10	60	
$V_{REG3V3On}$	REG3V3 UVLO turn-on threshold	V_{DD} rising from 0 V	2.5	2.65	2.8	V
$V_{REG3V3Off}$	REG3V3 UVLO turn-off threshold	V_{DD} falling from 3.3 V	2.2	2.35	2.5	V
$V_{REG3V3Hys}$	REG3V3 UVLO threshold hysteresis	-	-	0.3	-	V
I_{REG12}	REG12 current consumption	V_M = 45 V REG12 = 13 V externally supplied No commutation	-	800	1200	µA
		nSTBY = 0 REG12 = 13 V externally supplied	-	800	1200	
$V_{REG12On}$	REG12 UVLO turn-on threshold	REG12 rising from 0 V	6.0	6.3	6.6	V
$V_{REG12Off}$	REG12 UVLO turn-off threshold	REG12 falling from 8 V	5.8	6.1	6.4	V
$V_{REG12Hys}$	REG12 UVLO threshold hysteresis	-	-	0.2	-	V
I_{BOOT}	V_{BOOT} current consumption	HS on V_{BO} = 13 V	-	200	290	µA
V_{BOOn}	V_{BO} UVLO turn-on threshold	V_{BO} rising from 0 V	5.5	5.8	6.1	V
V_{BOOff}	V_{BO}UVLO turn-off threshold	V_{BO} falling from 8 V	5.3	5.6	5.9	V
V_{BOHys}	V_{BO} UVLO threshold hysteresis	-	-	0.15	-	V
t_{sleep}	Standby set time	-	-	-	1	µs
DC-DC switching regulator						
V_{PWR_OK}	Power-good voltage	-	5.6	6	6.4	V
V_{REG3V3}	Average output voltage	(1)	3.09	3.3	3.5	V
f_{SW}	Switching frequency		-	200	330	kHz

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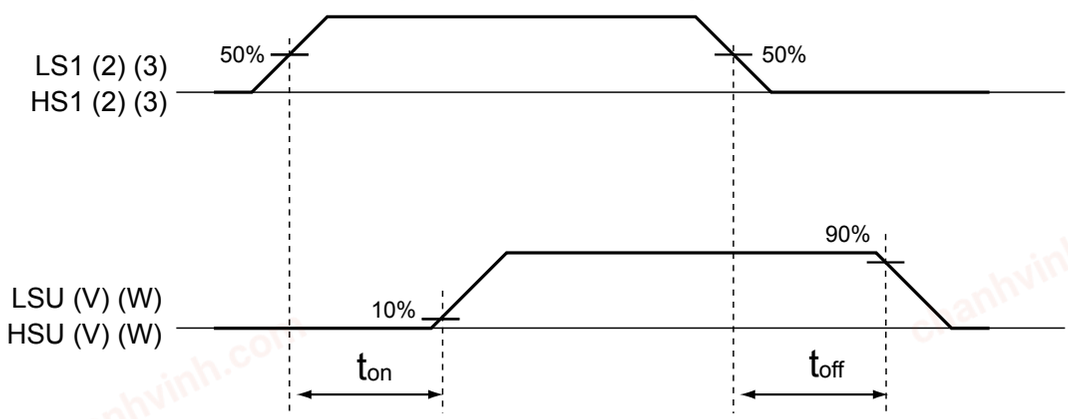
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{SWDS(ON)}$	Switch on-resistance	I_{SW} = 200 mA	-	1.4	-	Ω
η	Efficiency	V_M = 8 V; I_{REG3V3} = 70 mA (1) (2)	-	80	-	%
$I_{SW,peak}$	Peak current threshold	-	-	320	-	mA
I_{OVC}	Latched overcurrent threshold	-	-	1	-	A
t_{SS}	Soft-start time	-	2.5	5	7.5	ms
Linear regulator						
V_{REG12}	Linear regulator output and gate driver supply voltage	V_M > 13 V I_{REG12} = 10 mA	11.4	12	12.6	V
$V_{REG12,drop}$	Drop voltage	8 V ≤ V_M ≤ 11 V, I_{REG12} = 10 mA	-	200	400	mV
$I_{REG12,lim}$	Linear regulator current limit	V_M = 13 V, REG12 = 0 V	20	-	40	mA
Gate drivers						
I_{SI} I_{SO}	Maximum sink/source current capabilities	T_J = 25 °C	400	600	-	mA
		Full temperature range	350	-	-	mA
R_{PDin}	Input lines pull-down resistor	-	30	60	95	kΩ
t_{on} t_{off}	Input-to-output propagation delay	(3)	-	20	40	ns
MT	Delay matching, HS and LS turn-on/off	(4)	-	10	20	ns
R_{DS_diode}	Bootstrap diode on-resistance	-	-	120	240	Ω
Operational amplifiers						
V_{OPio}	Input offset voltage	V_{out} = 1.65; T_j = 25 °C	-	1	6	mV
		V_{out} = 1.65; full temperature range	-	-	7	mV
I_{OPio}	Input offset current	V_{out} = 1.65	-	-	100	pA
I_{OPib}	Input bias current	-	-	-	100	pA
CMRR	Common-mode rejection ratio	(2) 0 to 3.3 V; V_{out} = 1.65 V	-	80	-	dB
A_{OL}	Open loop gain	(2) R_L = 10 kΩ; V_{out} = 1.65	-	90	-	dB
V_{DD} - V_{OH}	High level output voltage	R_L = 10 kΩ	-	15	40	mV
V_{OL}	Low level output voltage	R_L = 10 kΩ	-	15	40	mV
I_{OUT}	Sink output current	V_{out} = 3.3 V; T_j = 25 °C	18	-	-	mA
		V_{out} = 3.3 V; full temperature range	16	-	-	
	Source output current	V_{out} = 0 V; T_j = 25 °C	18	-	-	mA
		V_{out} = 0 V; full temperature range	16	-	-	
GBP	Gain bandwidth product	(2) R_L = 2 kΩ; C_L = 100 pF V_{out} = 1.65	10	18	-	MHz
SR	Slew rate	R_L = 2 kΩ; C_L = 100 pF V_{in} 1 to 2 V step	-	10	-	V/µs

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Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
OC comparator						
V_{OCth}	Overcurrent threshold	-	235	255	275	mV
t_{CPD}	Comparator propagation delay	OCCOMP step from 0 to 1 V	-	80	120	ns
$t_{OCdeglitch}$	Comparator input deglitch filter time	(5)	35	50	-	ns
$t_{OCrelease}$	Minimum overcurrent latch release pulse width	(5)	-	-	20	ns
Thermal protection						
T_{SD}	Thermal shutdown temperature	-	130	140	150	°C
T_{hys}	Thermal shutdown hysteresis	-	20	30	40	°C

1. *Using the 47 µF capacitor (APXG250ARA470MF61G), 22 µH inductor (MLF1608C220KTA00), and diode 1N4448TR.*
2. *Guaranteed by characterization, not tested in production.*
3. *See Figure 7.*
4. *MT = max. ($|t_{on(LVG)} - t_{off(LVG)}|$, $|t_{on(HVG)} - t_{off(HVG)}|$, $|t_{off(LVG)} - t_{on(HVG)}|$, $|t_{off(HVG)} - t_{on(LVG)}|$).*
5. *See Figure 21.*

Figure 7. Gate drivers timing



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4 Pin description

Figure 8. **STSPIN32G0A1 pin connection (top view)**

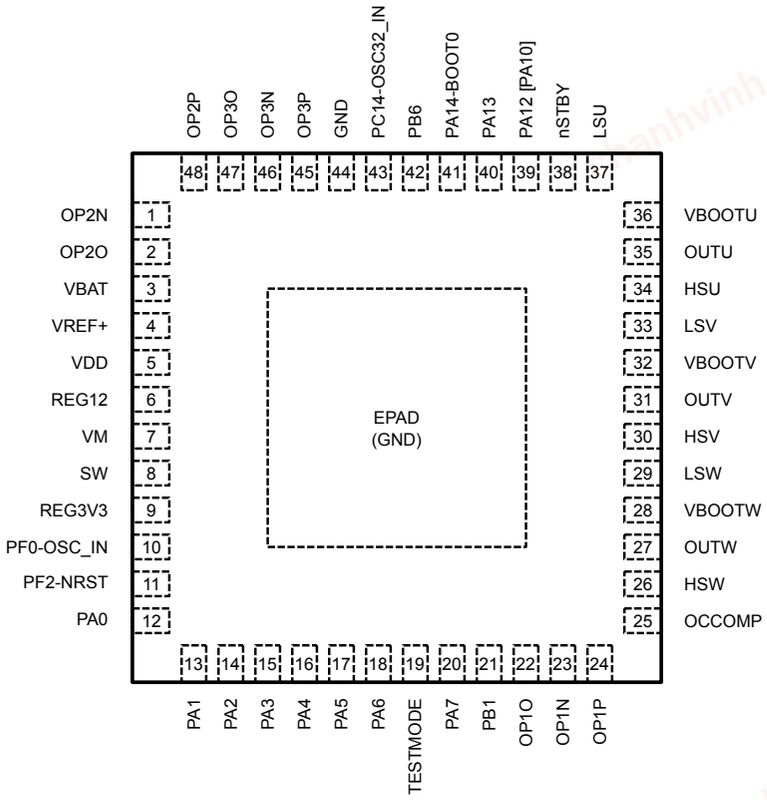
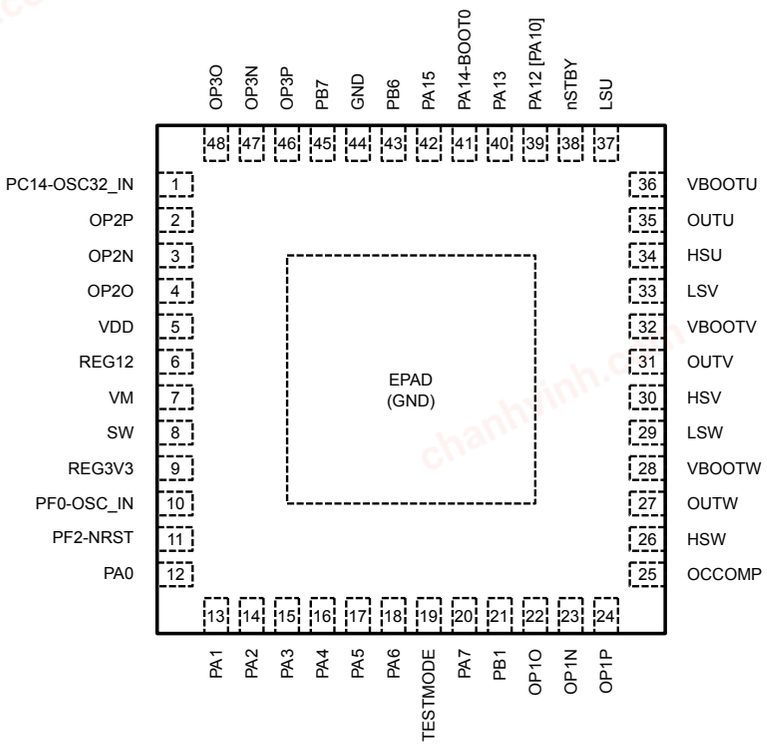


Figure 9. **STSPIN32G0A2 pin connection (top view)**



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Figure 10. **STSPIN32G0B1 pin connection (top view)**

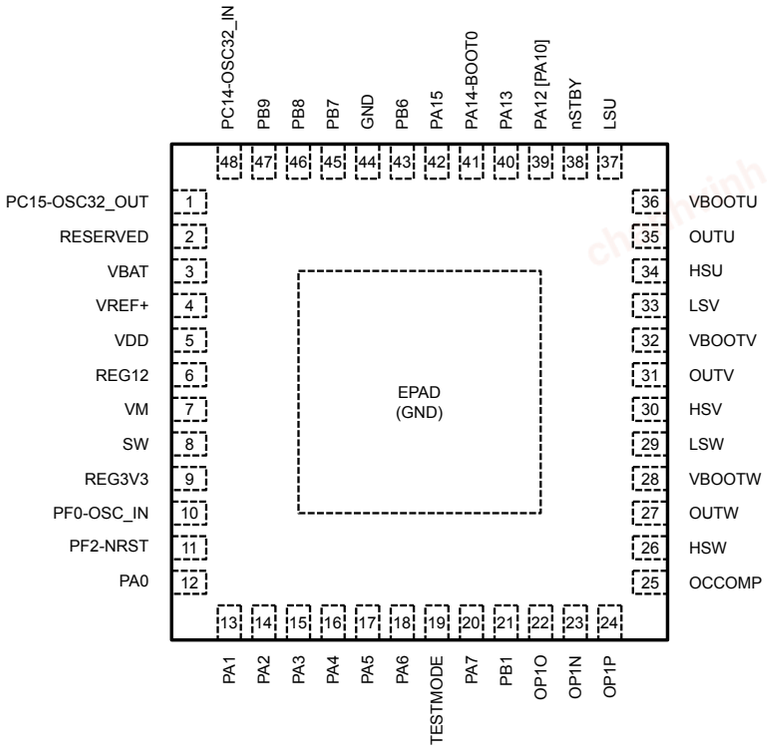
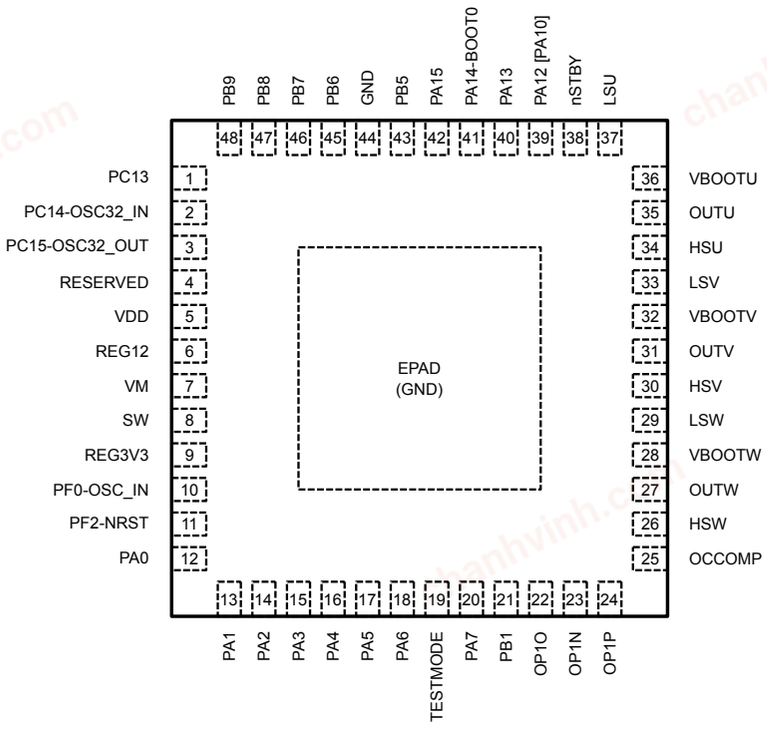


Figure 11. **STSPIN32G0B2 pin connection (top view)**



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Table 6. **STSPIN32G0A1/A2/B1/B2 pin list**

A1	A2	B1	B2	Name	Type	Function
24	24	24	24	OP1P	Analog In	Op amp 1 non inverting input
23	23	23	23	OP1N	Analog In	Op amp 1 inverting input
22	22	22	22	OP1O	Analog Out	Op amp 1 output
48	2			OP2P	Analog In	Op amp 2 non inverting input
1	3			OP2N	Analog In	Op amp 2 inverting input
2	4			OP2O	Analog Out	Op amp 2 output
45	46			OP3P	Analog In	Op amp 3 non inverting input
46	47			OP3N	Analog In	Op amp 3 inverting input
47	48			OP3O	Analog Out	Op amp 3 output
7	7	7	7	VM	Power	Power supply voltage (Bus voltage)
44	44	44	44	GND	Ground	Ground
6	6	6	6	REG12	Power	12 V linear regulator output
8	8	8	8	SW	Analog Out	3.3 V DC-DC buck regulator switching node
9	9	9	9	REG3V3	Power	3.3 V DC-DC buck regulator output
19	19	19	19	TESTMODE	Digital In	Test mode input
25	25	25	25	OCCOMP	Analog In	Overcurrent comparator input
26	26	26	26	HSW	Analog Out	W phase high-side driver output
27	27	27	27	OUTW	Power	W phase high-side (floating) common voltage
28	28	28	28	VBOOTW	Power	W phase bootstrap supply voltage
29	29	29	29	LSW	Analog Out	W phase low-side driver output
30	30	30	30	HSV	Analog Out	V phase high-side driver output
31	31	31	31	OUTV	Power	V phase high-side (floating) common voltage
32	32	32	32	VBOOTV	Power	V phase bootstrap supply voltage
33	33	33	33	LSV	Analog Out	V phase low-side driver output
34	34	34	34	HSU	Analog Out	U phase high-side driver output
35	35	35	35	OUTU	Power	U phase high-side (floating) common voltage
36	36	36	36	VBOOTU	Power	U phase bootstrap supply voltage
37	37	37	37	LSU	Analog Out	U phase low-side driver output
38	38	38	38	nSTBY	Digital In	Active low standby input
3		3		VBAT	Power	Backup supply voltage
5	5	5	5	VDD	Power	MCU supply voltage
4		4		VREF+	Analog	Reference voltage for MCU analog circuitry
			1	PC13	GPIO	MCU GPIO
43	1	48	2	PC14-OSC32_IN	GPIO	MCU GPIO
		1	3	PC15-OSC32_OUT	GPIO	MCU GPIO
10	10	10	10	PF0-OSC_IN	GPIO	MCU GPIO
11	11	11	11	PF2-NRST	GPIO	MCU GPIO
12	12	12	12	PA0	GPIO	MCU GPIO
13	13	13	13	PA1	GPIO	MCU GPIO
14	14	14	14	PA2	GPIO	MCU GPIO

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A1	A2	B1	B2	Name	Type	Function
15	15	15	15	PA3	GPIO	MCU GPIO
16	16	16	16	PA4	GPIO	MCU GPIO
17	17	17	17	PA5	GPIO	MCU GPIO
18	18	18	18	PA6	GPIO	MCU GPIO
20	20	20	20	PA7	GPIO	MCU GPIO
21	21	21	21	PB1	GPIO	MCU GPIO
39	39	39	39	PA12 [PA10]	GPIO	MCU GPIO
40	40	40	40	PA13	GPIO	MCU GPIO
41	41	41	41	PA14-BOOT0	GPIO	MCU GPIO
	42	42	42	PA15	GPIO	MCU GPIO
			43	PB5	GPIO	MCU GPIO
42	43	43	45	PB6	GPIO	MCU GPIO
	45	45	46	PB7	GPIO	MCU GPIO
		46	47	PB8	GPIO	MCU GPIO
		47	48	PB9	GPIO	MCU GPIO
		2	4	RESERVED	-	
				EPAD	Power	Internally connected to ground

Table 7. MCU to analog IC connections

MCU	Analog IC	Type	Function
PB12	OC_COMP_INT	Digital Out	OC comparator output
PA8	HS1	Digital In	High-side input driver U
PA9	HS2	Digital In	High-side input driver V
PA10	HS3	Digital In	High-side input driver W
PB13	LS1	Digital In	Low-side input driver U
PB14	LS2	Digital In	Low-side input driver V
PB15	LS3	Digital In	Low-side input driver W
PA11 [PA9]	OC_SEL	Digital In	OC protection selection

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5 Device description

The device is a system-in-package providing an integrated solution suitable for driving the three-phase brushless motor with Hall effect sensors.

5.1 UVLO and thermal protections

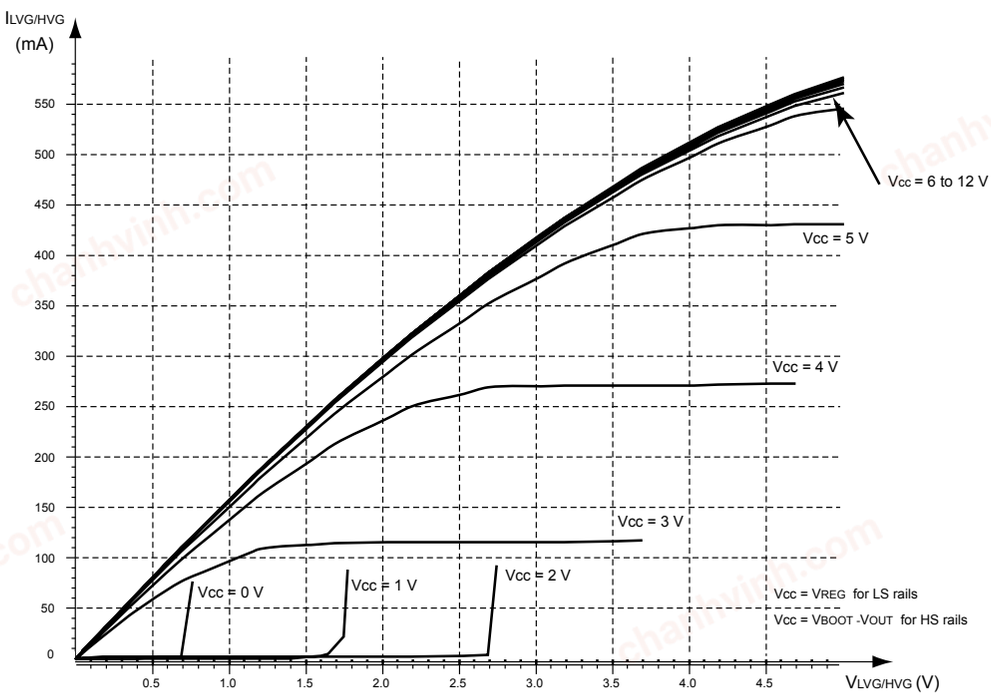
Table 8 summarizes the UVLO and OT protection management.

Table 8. UVLO and OT protection management

Block	V_M UVLO	V_{DD} UVLO	V_{REG12} UVLO	V_{BOOT} UVLO	Lin. Reg OT	DC-DC Reg OT
DC-DC regulator	-	-	-	-	-	OFF
Linear regulator	OFF	OFF	-	-	OFF	-
Op amps and OC comp	OFF	OFF	-	-	-	-
HSU, HSV, HSW output	LOW	LOW	LOW (1)	LOW (1) (2)	-	-
LSU, LSV, LSW output	LOW	LOW	LOW (1)	-	-	-

1. *The N-channel of the gate driver is turned ON with all the available supply voltage, refer to Figure 12.*
2. *Only the high-side gate driver in which the UVLO condition is detected (for example UVLO on VBOOTU causes the HSU to turn off).*

Figure 12. Gate driver output characteristics in UVLO conditions



5.1.1 UVLO on supply voltages

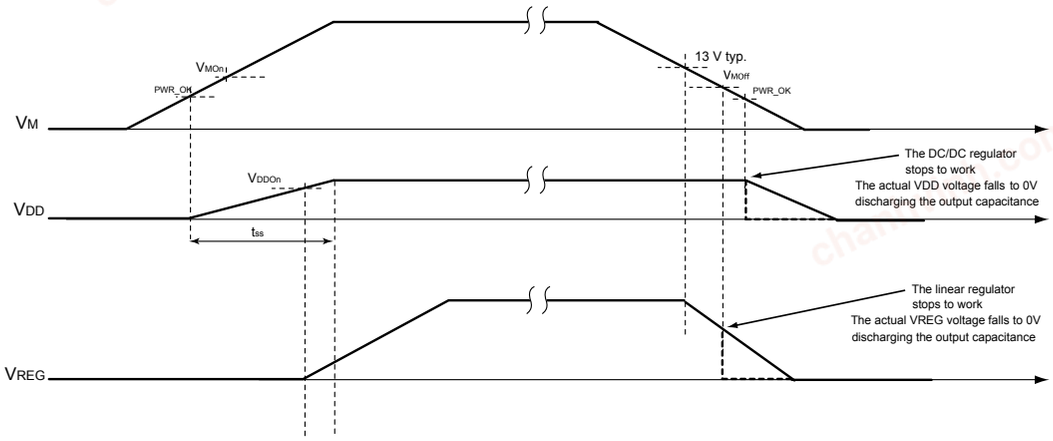
The device provides UVLO protections on each power supply.

The device enters into the undervoltage condition when the power supply voltage falls below the OFF threshold voltage and expires when the motor supply voltage goes over the ON threshold voltage.

Table 8 shows the UVLO protection management: which blocks are switched off after an UVLO event.

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Figure 13. **Power-up and power-down sequence**



5.1.2 Thermal protection

The device embeds an overtemperature shutdown protection. The thermal sensors are placed next to the DC-DC and linear regulator blocks.

When the OT protection is triggered, the correspondent block is switched off, the thermal shutdown condition only expires when the temperature goes below the "T_{SD} - T_{hys}" temperature (auto-restart).

Table 8 shows the thermal protection management: which blocks are switched off after an overtemperature event.

5.2 DC-DC buck regulator

The internal DC-DC buck converter provides the 3.3 V supply voltage suitable to supply the MCU and other external devices (for example, Hall effect sensors).

The regulator operates in the discontinuous current mode (DCM).

A soft-start function with fixed startup time is implemented to minimize the inrush current at the startup, refer to Figure 15.

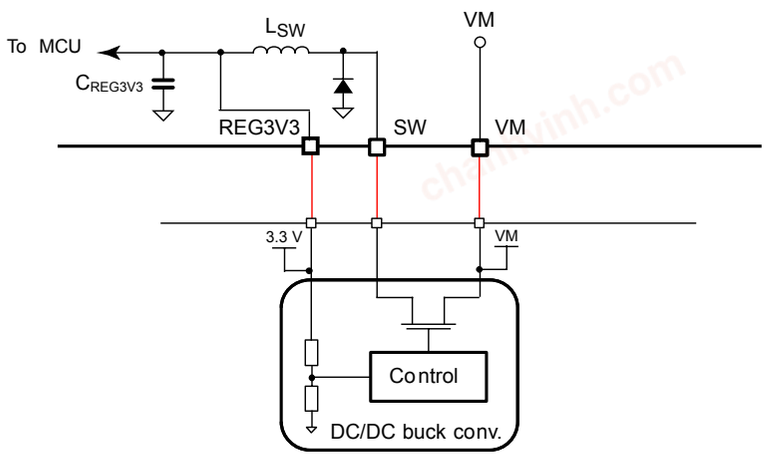
An overcurrent and short-circuit protection is provided.

If the failure event occurs on the SW pin and the I_{OVC} threshold is reached, the regulator is latched off. To restart the DC-DC regulator a power-down and power-up cycle of device supply voltage (V_M) is mandatory.

If the failure event occurs on the regulator output (REG3V3 pin) and the voltage goes below the UVLO threshold ($V_{REG3V3off}$), the regulator restarts with a new soft-start sequence until the OC condition is removed. In this case the current in the coil is limited by $I_{SW.peak}$.

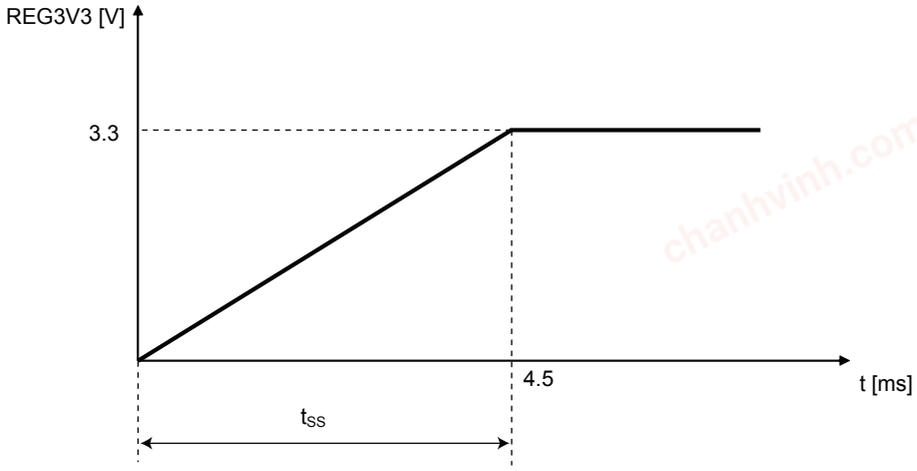
The DC-DC regulator embeds a thermal protection as described in Section 5.1.2.

Figure 14. **DC-DC buck regulator topology**



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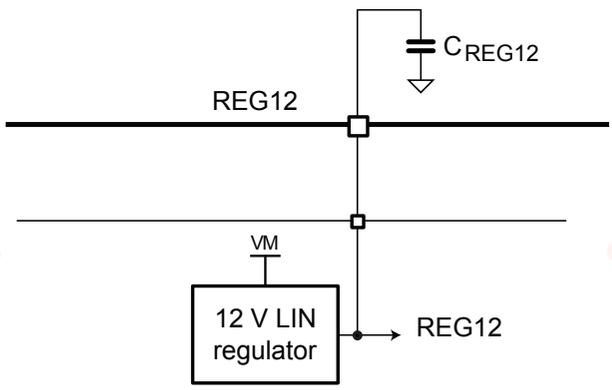
Figure 15. **Soft-start timing**



5.3 Linear regulator

The internal 12 V linear regulator is an LDO regulator providing the supply voltage for the gate drivers' section. An external capacitor connected to the REG12 pin is required.

Figure 16. **Linear regulator block diagram**

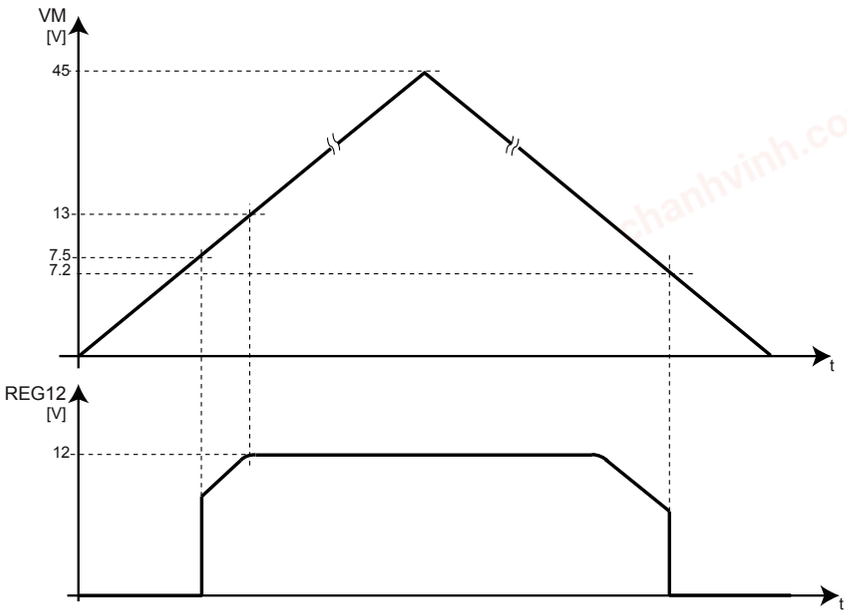


When the VM voltage is below 12 V, the VM pin and the linear regulator output can be shorted together providing the gate driver supply externally.

The linear regulator embeds a thermal protection as described in Section 5.1.2.

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Figure 17. **Linear regulator output characteristics**



Note: The linear regulator is designed to supply the internal circuitry only and must not be used to supply external components.

5.4 Standby mode

The device is forced into standby mode to reduce power consumption, forcing both the nSTBY inputs low.

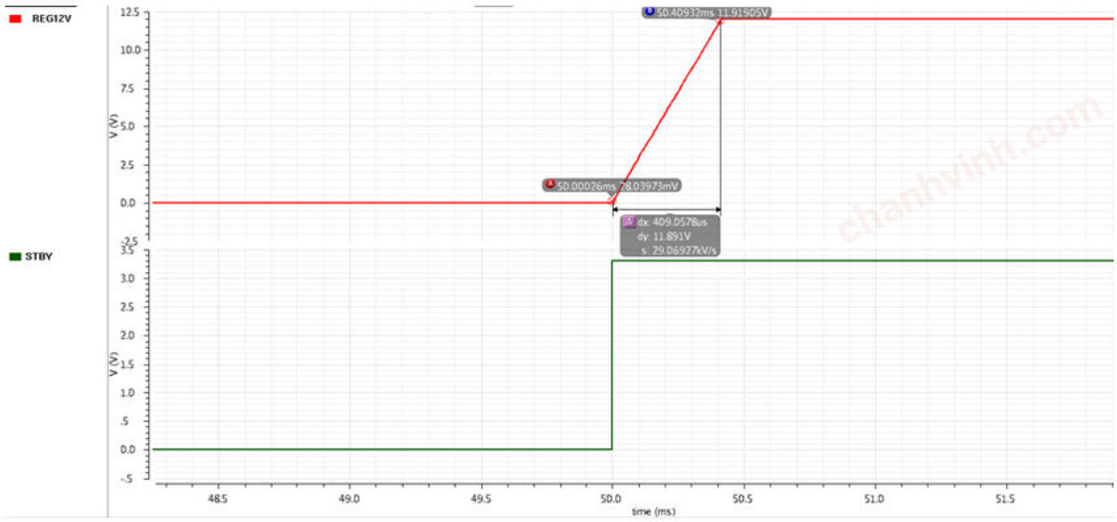
When standby mode is set, the analog IC is put into low consumption mode after a t_{sleep} time, in particular:

- The linear regulator is switched off
- All the output drivers are forced low (external power switches turned off)
- Op amps and comparators disabled
- The DC-DC regulator remains operative.

When the device exits standby mode, a set time is necessary to recover a proper value of the 12 V internal regulator. This set time is strictly dependent on the capacitor connected on the REG12 pin and can be calculated with Eq. (1).

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Figure 18. **"Standby to normal" operation timing (C_{REG} = 1 µF)**



Equation 1

$$t_{REG} = \frac{C_{REG} \cdot V_{REG12}}{I_{REG12,lim}} \quad (1)$$

5.5 Gate drivers

The device integrates a triple half-bridge gate driver able to drive N-channel power MOSFETs or IGBTs. The high-side section is supplied by a bootstrapped voltage technique with an integrated bootstrap diode.

All the input lines are connected to a pull-down resistor (60 kΩ typical value).

The high and low-side outputs of same half-bridge cannot be simultaneously driven high thanks to an integrated interlocking function.

Note: All the input lines of analog IC have an internal pull-down to guarantee the low logic level during device startup and when the MCU line is not present.

5.6 Microcontroller unit

The integrated MCU is the STM32G031x8 with the following main characteristics:

- Core: ARM® 32-bit Cortex™-M0+ CPU, frequency up to 64 MHz
- 64-kbyte of flash memory with protection and securable area
- 8-kbyte of SRAM with hardware parity check
- Up to 23 fast I/O ports (GPIO)
- 5-channel DMA controller with flexible mapping
- 12-bit ADC (up to 11 external channels) with 2.5 Msps conversion rate
- Advanced-control timer dedicated to motor control
- Up to 5 general purpose timers (1 x 32-bit + 4 x 16-bit)
- Communication interfaces: I^2C, USART, SPI
- Serial wire debug (SWD)
- Extended temperature range: -40 to 125 °C

For more details refer to the STM32G031x8 datasheet on www.st.com.

5.6.1 Memories and boot modes

The embedded MCU features up to 64 kbytes of embedded flash memory available for storing code and data. The whole non-volatile memory embeds the error correction code (ECC) feature supporting: single error correction, double error detection, and readout of the ECC fail address.

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Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection.
  - Level 1: memory readout protection. The flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected.
  - Level 2: chip readout protection. Debug features (Cortex-M0+ serial wire), boot in RAM and bootloader selection are disabled. This selection is irreversible.
- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU as instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. An additional option bit (PCROP_RDP) determines whether the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the flash memory cannot be read from or written to if either debug features are connected or the boot in the RAM is selected
- Level 2: chip readout protection. Debug features (Cortex-M0 serial wire) and the boot in the RAM selection is disabled.

A part of the flash memory can be hidden from the application once the code it contains is executed. As soon as the write-once SEC_PROT bit is set, the securable memory cannot be accessed until the system resets. The securable area generally contains the secure boot code to execute only once at boot. This helps to isolate secret code from untrusted application code.

The embedded MCU has 8 kbytes of embedded SRAM with parity. Hardware parity check allows memory data errors to be detected, which contributes to increasing functional safety of applications. The memory can be read/write-accessed at CPU clock speed, with 0 wait states.

At startup the boot pin and the boot selector option bit are used to select one of the three boot options:

- Boot from user flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot pin is shared with a standard GPIO and can be enabled through the boot selector option bit.

The boot loader is located in the system memory. It is used to reprogram the flash memory by using one of the following interfaces:

- USART on pins PA2/PA3
- I^2C-bus on pins PB6/PB7

5.6.2 MCU power supply management

The embedded MCU requires a 1.7 V to 3.6 V operating supply voltage (V_{DD}).

Other supplies are provided to specific peripherals:

The MCU supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wake-up sources:

- V_{DD} (1.7 to 3.6 V) is the external power supply for the internal regulator and the system analog such as reset, power management A/D converter, voltage reference buffer, and internal clocks. It is provided through the VDD pin and it can be generated by the embedded DC-DC buck regulator (see Section 5.2).
- V_{BAT} (1.55 V to 3.6 V) is the power supply (through a power switch) for RTC, TAMP, low-speed external 32.768 kHz oscillator, and backup registers when VDD is not present. VBAT is provided externally through the VBAT pin. In the STSPIN32A2 and STSPIN32B2 versions this pin is not available on the package, and it is internally bonded to the VDD pin.

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- V_{REF+} is the analog peripheral input reference voltage, or the output of the internal voltage reference buffer (when enabled). When V_{DD} < 2 V, V_{REF+} must be equal to V_{DD}. When V_{DD} ≥ 2 V, V_{REF+} must be between 2 V and V_{REG3V3}. It can be grounded when the analog peripherals using V_{REF+} are not active. In the STSPIN32A2 and STSPIN32B2 versions this pin is not available on the package, and it is internally connected with VDD. In this case, the internal voltage reference buffer must be kept disabled.

5.6.3 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted deadtimes.

This timer is used to generate the PWM signal for the three half-bridge gate drivers as shown in Table 9.

Table 9. TIM1 channel configuration

MCU I/O	Analog IC input	TIM1 channel
PB13	LS1	TIM1_CH1N
PB14	LS2	TIM1_CH2N
PB15	LS3	TIM1_CH3N
PA8	HS1	TIM1_CH1
PA9	HS2	TIM1_CH2
PA10	HS3	TIM1_CH3

5.6.4 Voltage reference buffer

When enabled, an embedded buffer provides the internal reference voltage to analog blocks (for example ADC) and to the VREF+ pin for external components.

The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is disabled.

Note: In STSPIN32G0A2 and STSPIN32G0B2, the VREF+ pin is not available, and the voltage reference buffer should not be enabled.

5.7 Test mode

A dedicated TESTMODE pin is available to enter test mode.

Note: ***In the application, the TESTMODE pin should be shorted to GND in order to not enter the test mode inadvertently.***

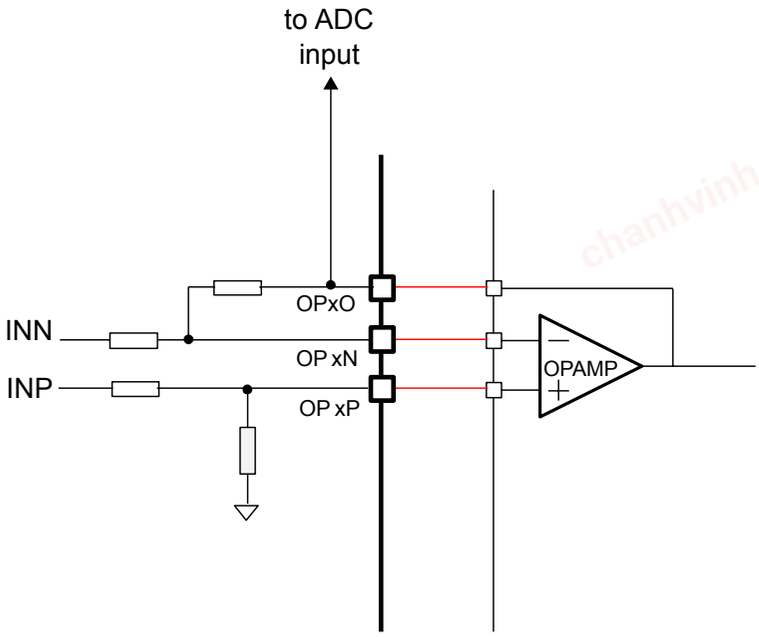
5.8 Operational amplifiers

The device integrates three rail-to-rail operational amplifiers suitable for signal conditioning, in particular for current sensing.

The operational amplifiers provide a rail-to-rail output stage with fast recovery in the saturation condition. The output stage saturation happens in linear applications when a high amplitude input signal occurs and causes the output of the operational amplifier to move outside its real capabilities.

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Figure 19. **Operational amplifiers**



5.9 Comparator

A comparator is available to perform an overcurrent protection. The OCCOMP pin can be connected to the shunt resistor to monitor the load current.

When an OC event is triggered, the OC comparator output signals the OC event to the PB12 input of MCU (TIM1_BKIN).

Depending on the status of the OC_SEL signal (see Table 10), the OC event is acting directly on the control logic of the gate driver switching off all high-side gate outputs, and consequently the external high-side power switches.

Figure 20. **Comparator**

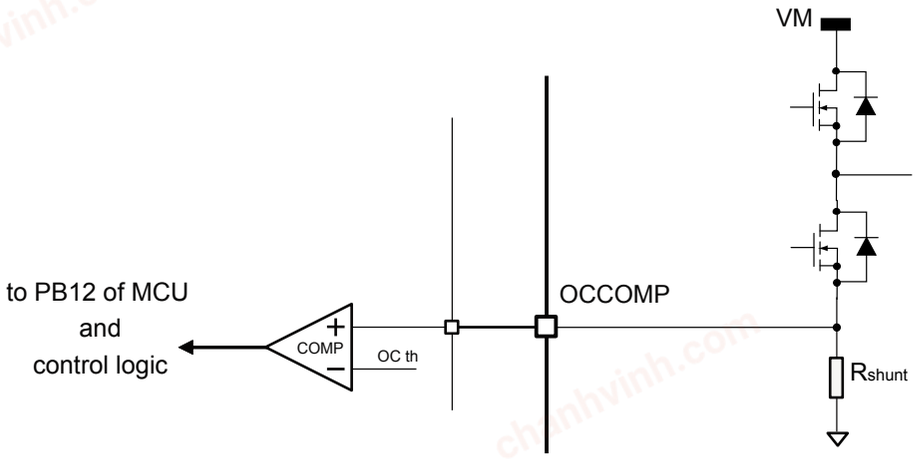


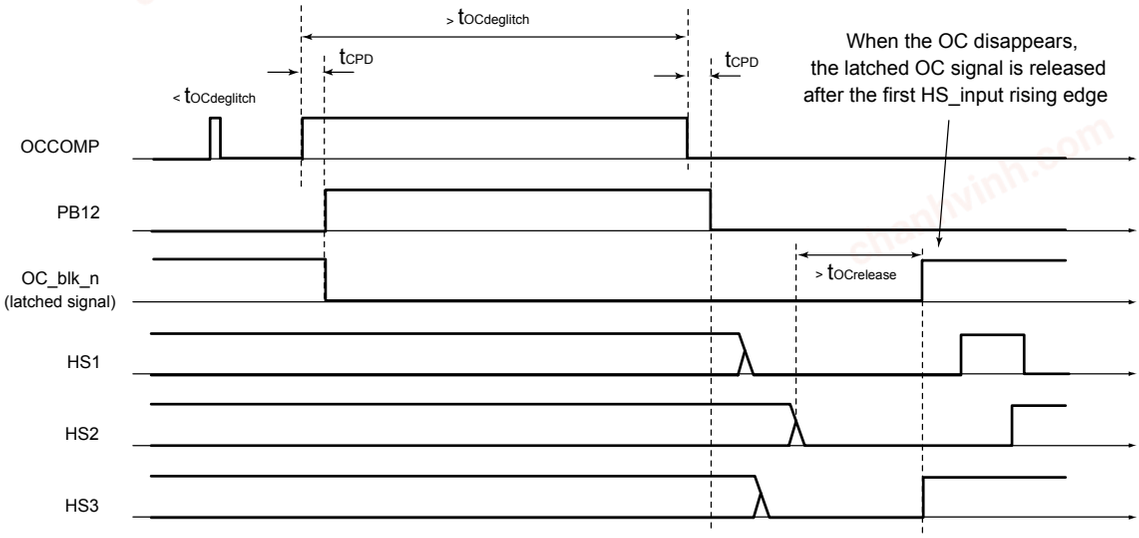
Table 10. **OC protection selection**

OC_SEL	Function
0	OC comparator output signal is visible only to MCU (default)
1	OC comparator output signal is visible to MCU and also acts on gate driver control logic

When the overcurrent condition expires, after all HS driving inputs are forced low, the latched overcurrent blanking signal is released after the first HS input rising edge occurrence (refer to Figure 21).

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Figure 21. **Driver logic overcurrent management signals**



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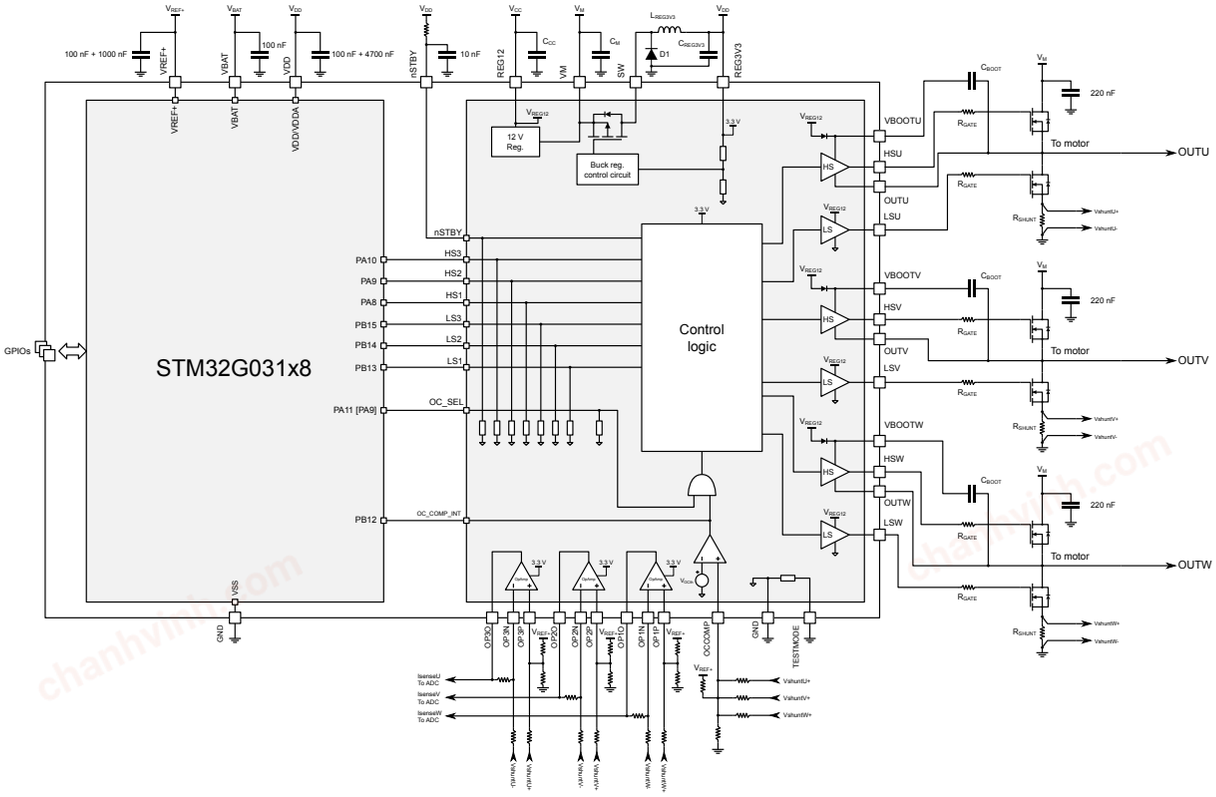
6 Application example

Figure 22, Figure 23, Figure 24, and Figure 25 show an application example using the device to drive a three-phase motor with triple or single shunt configuration.

The others features implemented are:

- V_{DD} (3.3 V) power supply internally generated via DC-DC regulator
- V_{REG12} (12 V) power supply internally generated via LDO linear regulator
- Overcurrent protection using internal comparator
- Current sensing using internal operational amplifiers and ADCs

Figure 22. STSPIN32G0A1 application example



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Figure 23. **STSPIN32G0A2 application example**

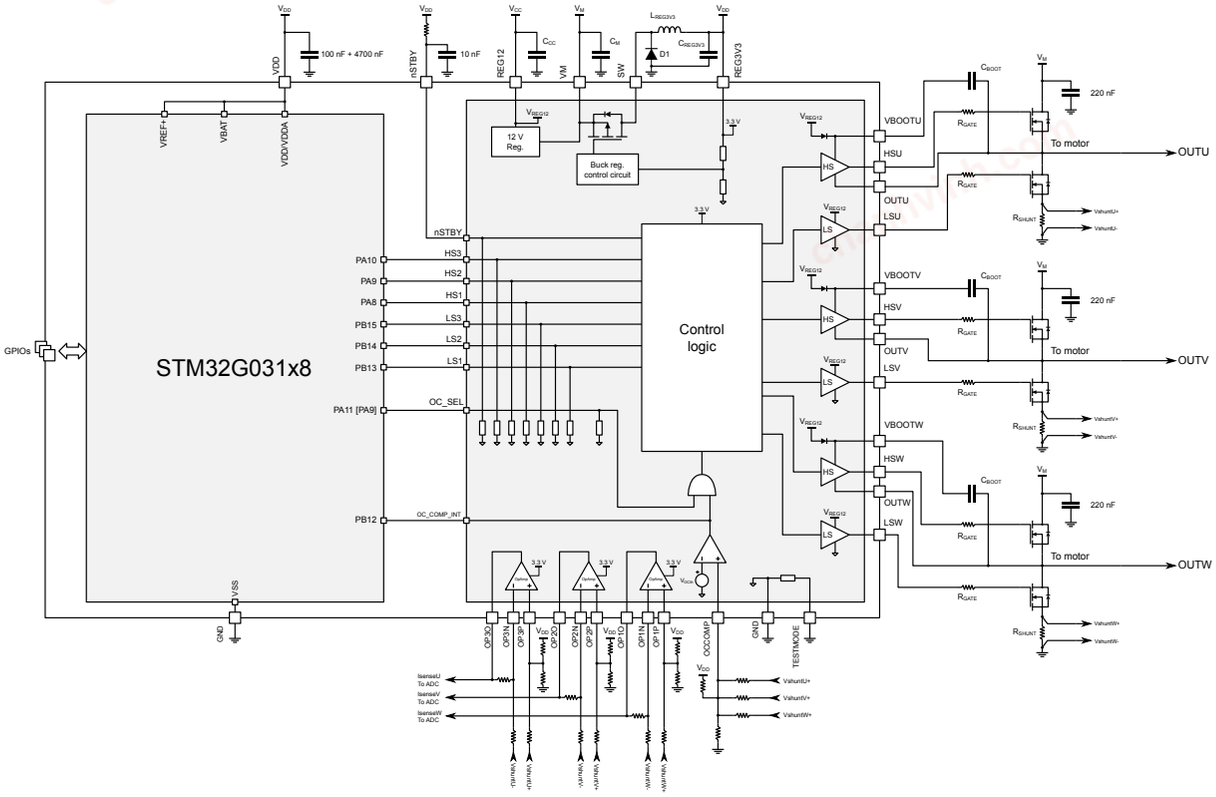
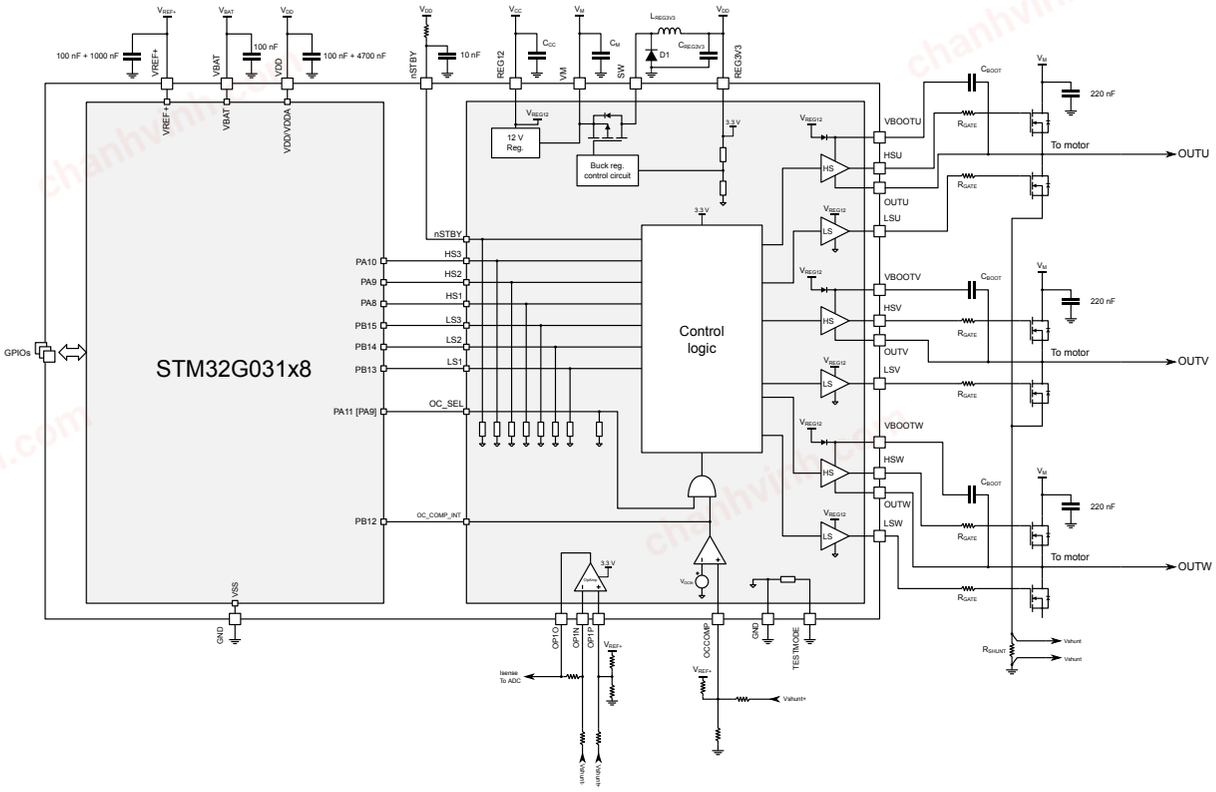
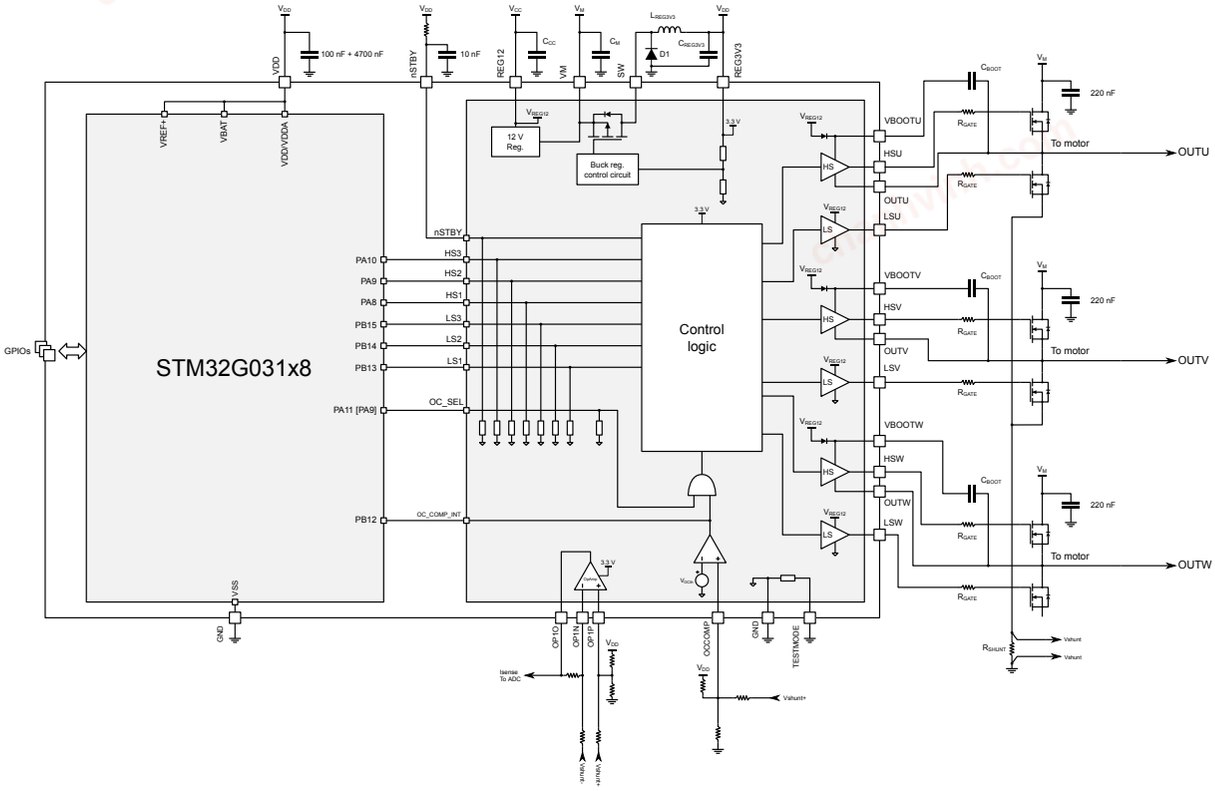


Figure 24. **STSPIN32G0B1 application example**



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Figure 25. **STSPIN32G0B2 application example**



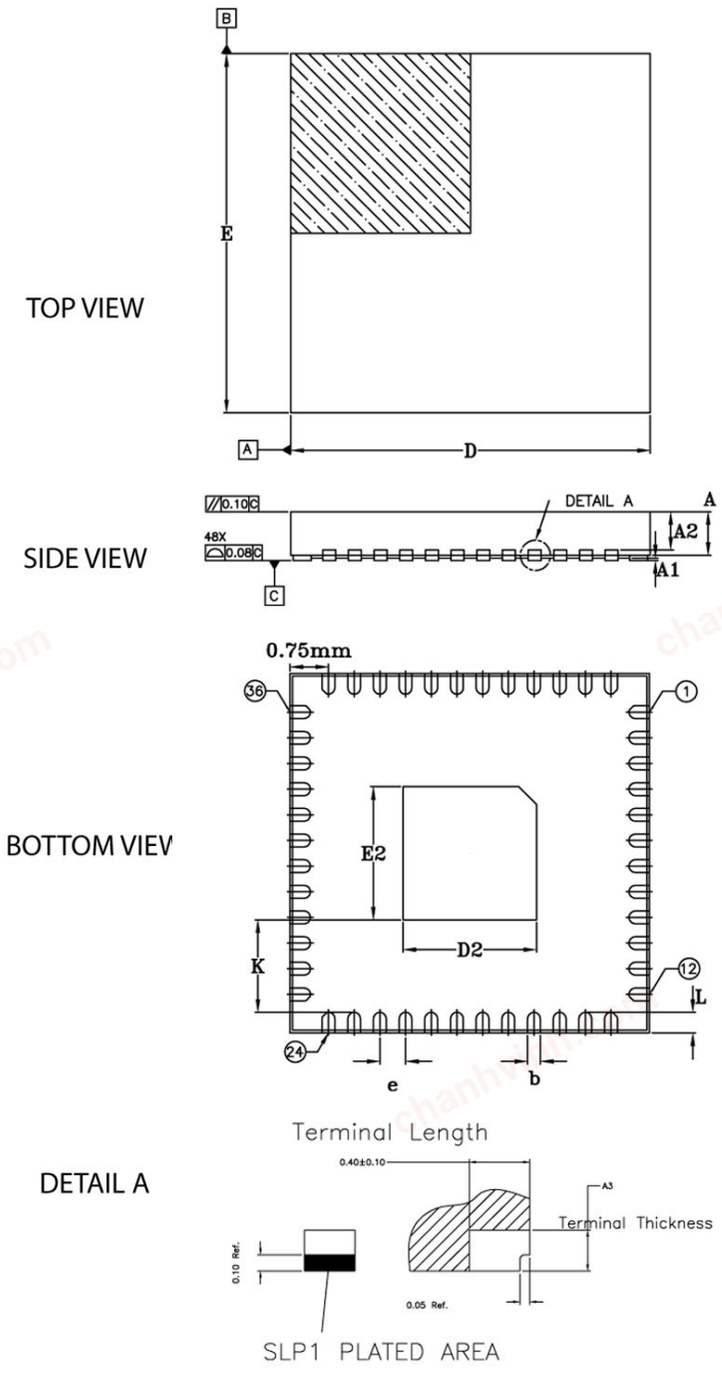
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7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 VFQFPN48 7 x 7 package information

Figure 26. VFQFPN48 7 x 7 x 1.0 - 48L, pitch 0.5 package outline

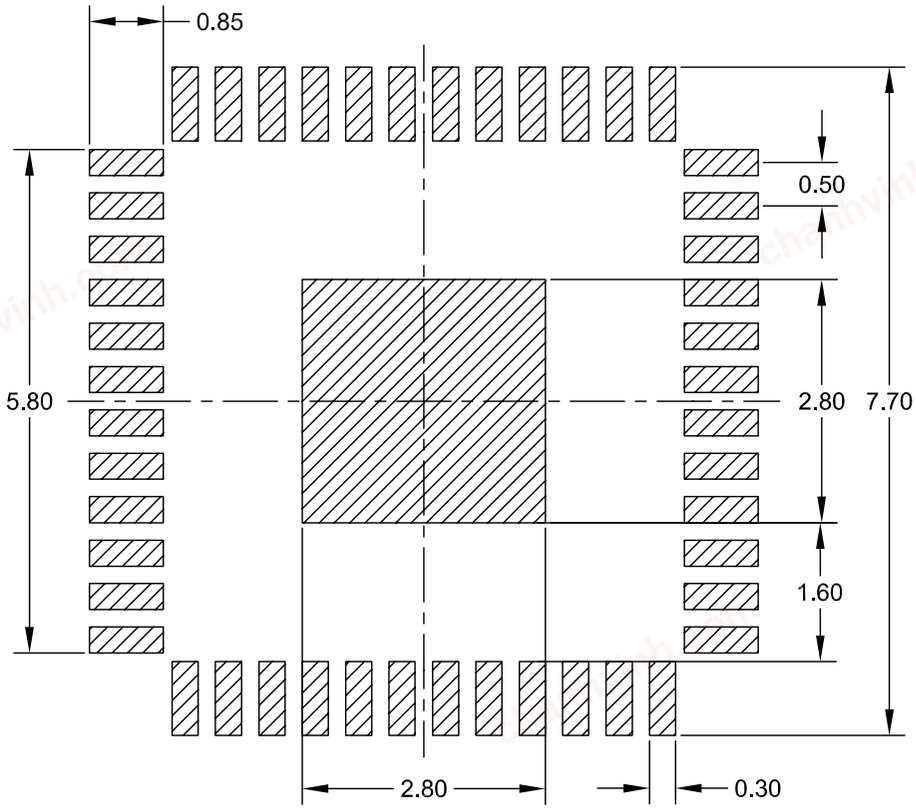


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Table 11. **VFQFPN48 7 x 7 x 1.0 - 48L, pitch 0.5 - package mechanical data**

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1	0.0	-	0.05
A2		0.75	
A3		0.203	
b	0.20	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
e		0.50	
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
K		1.80	
L	0.30	0.40	0.50

Figure 27. **VFQFPN48 7 x 7 x 1.0 - 48L, pitch 0.5 - suggested footprint**



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8 Ordering information

Table 12. **Order codes**

Order code	Package	Package marking	Packaging
STSPIN32G0A1	VFQFPN 7 x 7 x 1.0 - 48L	SPIN32G0A1	Tray
STSPIN32G0A1TR	VFQFPN 7 x 7 x 1.0 - 48L	SPIN32G0A1	Tape and reel
STSPIN32G0B1	VFQFPN 7 x 7 x 1.0 - 48L	SPIN32G0B1	Tray
STSPIN32G0B1TR	VFQFPN 7 x 7 x 1.0 - 48L	SPIN32G0B1	Tape and reel
STSPIN32G0A2	VFQFPN 7 x 7 x 1.0 - 48L	SPIN32G0A2	Tray
STSPIN32G0A2TR	VFQFPN 7 x 7 x 1.0 - 48L	SPIN32G0A2	Tape and reel
STSPIN32G0B2	VFQFPN 7 x 7 x 1.0 - 48L	SPIN32G0B2	Tray
STSPIN32G0B2TR	VFQFPN 7 x 7 x 1.0 - 48L	SPIN32G0B2	Tape and reel

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Revision history

Table 13. **Document revision history**

Date	Revision	Changes
03-Oct-2024	1	Initial release.

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