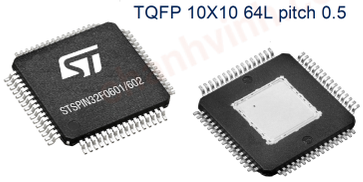
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# STSPIN32F0601, STSPIN32F0602

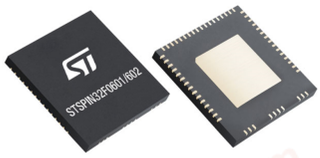
Datasheet

## Advanced 600 V three-phase BLDC controller with embedded STM32 MCU

TQFP 10X10 64L pitch 0.5



QFN 10X10 72L pitch 0.5



| Product status link |
|---|
| STSPIN32F0601 |
| STSPIN32F0601Q |
| STSPIN32F0602 |
| STSPIN32F0602Q |

| Product label |
|---|
| SUSTAINABLE TECHNOLOGY |

## Features

- Three-phase gate drivers
  - High voltage rail up to 600 V
  - dV/dt transient immunity ±50 V/ns
  - Gate driving voltage range from 9V to 20V
- Driver current capability:
  - STSPIN32F0601/Q: 200/350 mA source/sink current
  - STSPIN32F0602/Q: 1/0.85 A source/sink current
- 32-bit ARM® Cortex®-M0 core:
  - Up to 48 MHz clock frequency
  - 4-kByte SRAM with HW parity
  - 32-kByte Flash memory with option bytes
  - used for write/readout protection
- 21 general-purpose I/O ports (GPIO)
- 6 general-purpose timers
- 12-bit ADC converter (up to 10 channels)
- $I^2C$, USART and SPI interfaces
- Matched propagation delay for all channels
- Integrated bootstrap diodes
- Comparator for fast over current protection
- UVLO, Interlocking and deadtime functions
- Smart shutdown (smartSD) function
- Standby mode for low power consumption
- On-chip debug support via SWD
- Extended temperature range: -40 to +125 °C
- Package:
  - TQFP 10x10 64L pitch 0.5 Creepage 1.2 mm
  - QFN 10x10 72L pitch 0.5 Creepage 1.8 mm

## Applications

- Home and Industrial refrigerators compressors
- Industrial drives, pumps, fans
- Air conditioning compressors & fans
- Corded power tools, garden tools
- Home appliances
- Industrial automation

## Description

The STSPIN32F060x system-in-package is an extremely integrated solution for driving three-phase applications, helping designers to reduce PCB area and overall bill-of-material.

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It embeds an STM32F031x6x7 featuring an ARM® 32-bit Cortex®-M0 CPU and a 600 V triple half-bridge gate driver, able to drive N-channel power MOSFETs or IGBTs.

A comparator featuring advanced smartSD function is integrated, ensuring fast and effective protection against overload and overcurrent.

The high-voltage bootstrap diodes are also integrated, as well as anti cross-conduction, deadtime and UVLO protection on both the lower and upper driving sections, which prevents the power switches from operating in low efficiency or dangerous conditions. Matched delays between low and high-side sections guarantee no cycle distortion.

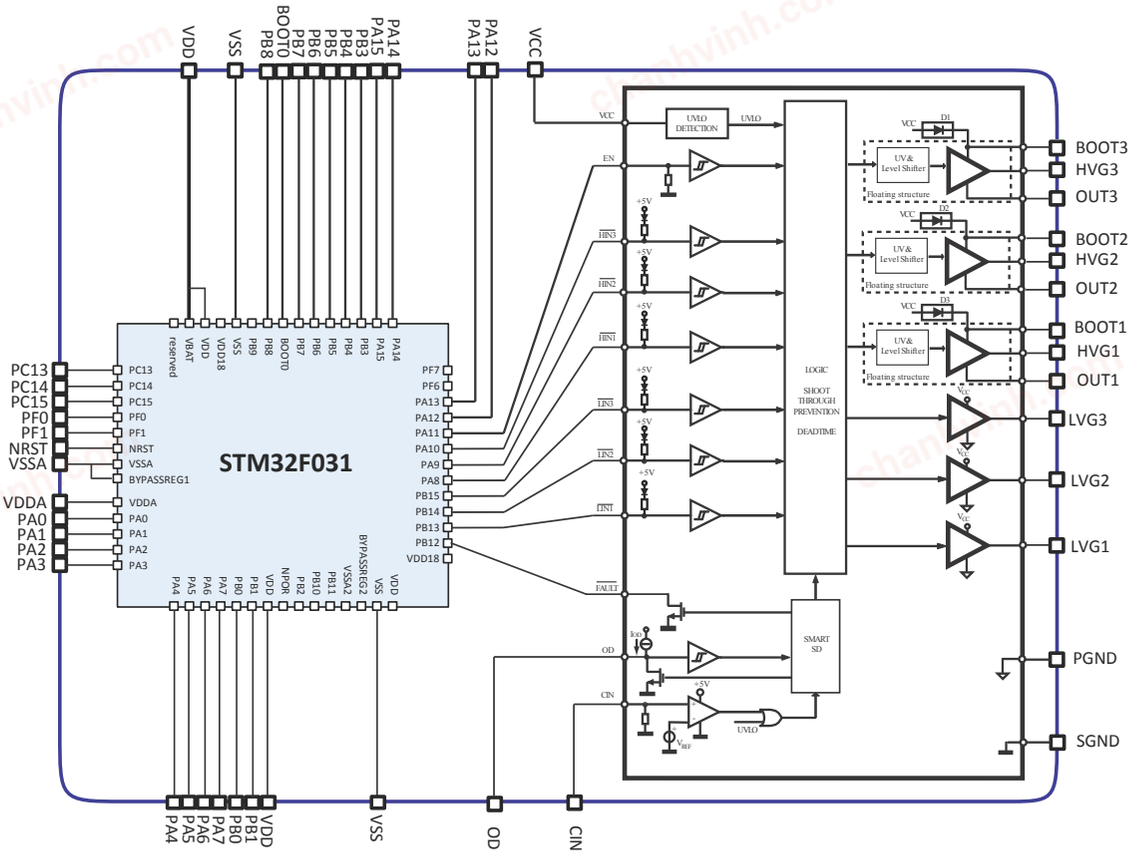
The integrated MCU allows performing FOC, 6-step sensorless and other advanced driving algorithms including the speed control loop.

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# 1 Block diagram

Figure 1. **STSPIN32F060x SiP block diagram**



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# 2 Pin description and connection diagram

Figure 2. **STSPIN32F060x pin connection (TQFP top view)**

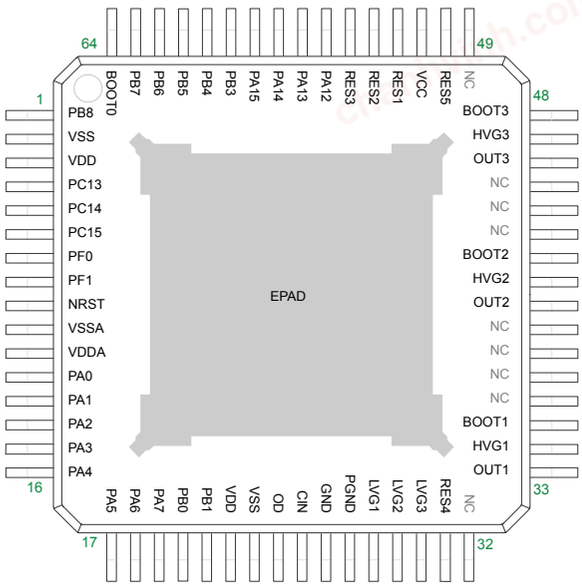
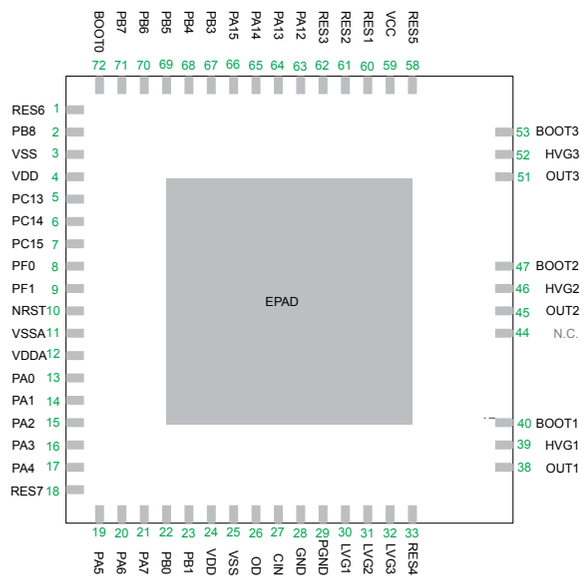



Figure 3. **STSPIN32F060x pin connection (QFN top view)**



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**Table 1. Legend/abbreviations used in the pin description table**

| Name | Abbreviation | |
|---|---|---|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | AO | Gate Driver Analog Output |
| | P | Gate Driver Supply\GND pin |
| | S | Supply pin |
| | I | Input-only pin |
| | I/O | Input / output pin |
| I/O structure | FT | 5 V-tolerant I/O |
| | FTf | 5 V-tolerant I/O, FM+ capable |
| | TTa | 3.3 V-tolerant I/O directly connected to ADC |
| | TC | Standard 3.3V I/O |
| | B | Dedicated BOOT0 pin |
| | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset | |
| Pin functions | Alternate Functions | Functions selected through GPIOx_AFR registers |
| | Additional functions | Functions directly selected/enabled through peripheral registers |

**Table 2. STSPIN32F060x MCU-Driver internal connections**

| MCU pad | Type | controller pad | Function |
|---|---|---|---|
| PB12 | I/O - FT | $\overline{\text{FAULT}}$ | Gate Driver Fault output |
| PB13 | I/O - FT | $\overline{\text{LIN1}}$ | Gate Driver Low Side input driver 1 |
| PB14 | I/O - FT | $\overline{\text{LIN2}}$ | Gate Driver Low Side input driver 2 |
| PB15 | I/O - FT | $\overline{\text{LIN3}}$ | Gate Driver Low Side input driver 3 |
| PA8 | I/O - FT | $\overline{\text{HIN1}}$ | Gate Driver High Side input driver 1 |
| PA9 | I/O - FTf | $\overline{\text{HIN2}}$ | Gate Driver High Side input driver 2 |
| PA10 | I/O - FTf | $\overline{\text{HIN3}}$ | Gate Driver High Side input driver 3 |
| PA11 | I/O - FT | EN | Gate Driver shut down input |

*Note: Each unused GPIO inside the SiP should be configured in OUTPUT mode low level after startup by software*

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# 3 Pin description table

Table 3. **Pin description**

| TQFP N. | QFN N. | Name | Type | Function |
|---|---|---|---|---|
| - | 1 | RES6 | Reserved | Pin must be left floating |
| 1 | 2 | PB8 | I/O - FTf | MCU PB8 |
| 2 | 3 | VSS | Supply | MCU digital ground |
| 3 | 4 | VDD | Supply | MCU digital power supply |
| 4 | 5 | PC13 | I/O - TC | MCU PC13 |
| 5 | 6 | PC14 | I/O - TC | MCU PC14 |
| 6 | 7 | PC15 | I/O - TC | MCU PC15 |
| 7 | 8 | PF0 | I/O - FT | MCU PF0 |
| 8 | 9 | PF1 | I/O - FT | MCU PF1 |
| 9 | 10 | NRST | I/O - RST | MCU Reset pin |
| 10 | 11 | VSSA | Supply | MCU analog ground |
| 11 | 12 | VDDA | Supply | MCU analog power supply |
| 12 | 13 | PA0 | I/O - TTa | MCU PA0 |
| 13 | 14 | PA1 | I/O - TTa | MCU PA1 |
| 14 | 15 | PA2 | I/O - TTa | MCU PA2 |
| 15 | 16 | PA3 | I/O - TTa | MCU PA3 |
| 16 | 17 | PA4 | I/O - TTa | MCU PA4 |
| - | 18 | RES7 | Reserved | Pin must be left floating |
| 17 | 19 | PA5 | I/O - TTa | MCU PA5 |
| 18 | 20 | PA6 | I/O - TTa | MCU PA6 |
| 19 | 21 | PA7 | I/O - TTa | MCU PA7 |
| 20 | 22 | PB0 | I/O - TTa | MCU PB0 |
| 21 | 23 | PB1 | I/O - TTa | MCU PB1 |
| 22 | 24 | VDD | Supply | MCU digital power supply |
| 23 | 25 | VSS | Supply | MCU digital ground |
| 24 | 26 | OD | Analog OD Output | Open Drain comparator output |
| 25 | 27 | CIN | Analog Input | Comparator positive input |
| 26 | 28 | SGND | Power | Driver signal ground |
| 27 | 29 | PGND | Power | Driver power ground |
| 28 | 30 | LVG1(1) | Analog Out | Phase 1 low-side driver output |
| 29 | 31 | LVG2(1) | Analog Out | Phase 2 low-side driver output |
| 30 | 32 | LVG3(1) | Analog Out | Phase 3 low-side driver output |
| 31 | 33 | RES4 | Reserved | Pin must be left floating |
| 33 | 38 | OUT1 | Power | Phase 1 high-side (floating) common voltage |
| 34 | 39 | HVG1(1) | Analog Out | Phase 1 high-side driver output |
| 35 | 40 | BOOT1 | Power | Phase 1 bootstrap supply voltage |

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| TQFP N. | QFN N. | Name | Type | Function |
|---|---|---|---|---|
| 40 | 45 | OUT2 | Power | Phase 2 high-side (floating) common voltage |
| 41 | 46 | HVG2(1) | Analog Out | Phase 2 high-side driver output |
| 42 | 47 | BOOT2 | Power | Phase 2 bootstrap supply voltage |
| 46 | 51 | OUT3 | Power | Phase 3 high-side (floating) common voltage |
| 47 | 52 | HVG3(1) | Analog Out | Phase 3 high-side driver output |
| 48 | 53 | BOOT3 | Power | Phase 3 bootstrap supply voltage |
| 50 | 58 | RES5 | Reserved | Pin must be left floating |
| 51 | 59 | VCC | Power | Driver low side and logic supply voltage |
| 52 | 60 | RES1 | Reserved | Pin must be left floating |
| 53 | 61 | RES2 | Reserved | Pin must be left floating |
| 54 | 62 | RES3 | Reserved | Pin must be left floating |
| 55 | 63 | PA12 | I/O - FT | MCU PA12 |
| 56 | 64 | PA13 | I/O - FT | MCU PA13/SWDIO (System debug data) |
| 57 | 65 | PA14 | I/O - FT | MCU PA14/SWDCLK (System debug clock) |
| 58 | 66 | PA15 | I/O - FT | MCU PA15 |
| 59 | 67 | PB3 | I/O - FT | MCU PB3 |
| 60 | 68 | PB4 | I/O - FT | MCU PB4 |
| 61 | 69 | PB5 | I/O - FT | MCU PB5 |
| 62 | 70 | PB6 | I/O - FTf | MCU PB6 |
| 63 | 71 | PB7 | I/O - FTf | MCU PB7 |
| 64 | 72 | BOOT0 | I - B | Boot memory selection |
| 32, 36, 37, 38, 39, 43, 44, 45, 49 | 44 | NC | | Not Connected |
| - | - | EPAD | Power | Exposed pad, internally connected to SGND |

1. *The circuit guarantees less than 1 V on the LVG and HVG pins (at $I_{sink}$ = 10 mA), with VCC > 3 V. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFETs normally used to hold the pin low. When the EN is set low, gate driver outputs are forced low and assure low impedance.*

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# 4 Electrical data

## 4.1 Absolute maximum ratings

**(Each voltage referred to SGND unless otherwise specified)**

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| VCC | Power supply voltage | | -0.3 | 21 | V |
| $V_{PGND}$ | Low-side driver ground | | VCC – 21 | VCC + 0.3 | V |
| $V_{PS}$ (1) | Low-side driver ground | | -21 | 21 | V |
| $V_{OUT}$ | Output voltage | | $V_{BOOT}$ – 21 | $V_{BOOT}$ + 0.3 | V |
| $V_{BOOT}$ | Bootstrap voltage | | -0.3 | 620 | V |
| $V_{HVG}$ | High side gate output voltage | | $V_{OUT}$ – 0.3 | $V_{BOOT}$ + 0.3 | V |
| $V_{LVG}$ | Low side gate output voltage | | $V_{PGND}$ – 0.3 | VCC + 0.3 | V |
| $V_{CIN}$ | Comparator input voltage | | -0.3 | 20 | V |
| $V_{OD}$ | Open-drain voltage (OD, FAULT) | | -0.3 | 21 | V |
| $dV_{OUT}/dt$ | Common mode transient Immunity | | | 50 | V/ns |
| $V_{IO}$ | MCU logic input voltage | TTa type(2) | -0.3 | 4 | V |
| | Logic input voltage | FT, FTf type(2) | -0.3 | VDD + 4 (3) | V |
| $I_{IO}$ | MCU I/O output current | (2) | -25 | 25 | mA |
| $\Sigma I_{IO}$ | MCU I/O total output current | (2) | -80 | 80 | mA |
| VDD | MCU digital supply voltage | (2) | -0.3 | 4 | V |
| VDDA | MCU analog supply voltage | (2) | -0.3 | 4 | V |
| $T_{stg}$ | Storage temperature | | -50 | 150 | °C |
| $T_J$ | Junction temperature | | -40 | 150 | °C |
| $P_{TOT}$ | Total power dissipation | | | 4.5 | W |
| ESD | Human Body Model | TQFP 10x10 64L package | 2(4) | | kV |
| | | QFN 10x10 72L package | 2 | | |

1. $V_{PS} = V_{PGND} - V_{SGND}$
2. *For details see Table 15 and 16 in the STM32F031x6x7 datasheet www.st.com*
3. *Valid only if the internal pull-up/pull-down resistors are disabled. If the internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.*
4. *Pins 33 to 48 have HBM ESD rating 1C conforming to ANSI/ESDA/JEDEC JS-001-2014.*

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## 4.2 Thermal data

Table 5. **Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th(JA)}$ | Thermal resistance junction to ambient(1) TQFP 10x10 64L package | 27.6 | °C/W |
| | Thermal resistance junction to ambient (1) QFN 10x10 72L package | 22.4 | |

1. *JEDEC 2s2p PCB in still air.*

## 4.3 Recommended operating conditions

Table 6. **Recommended operating conditions**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VCC | Power supply voltage | | $(V_{CCthON})_{MAX}$ | | 20 | V |
| $V_{LS}$ (1) | Low-side driver supply voltage | | 4 | | 20 | V |
| $V_{PS}$ (2) | Low-side driver ground | | -5 | | 5 | V |
| $V_{BO}$(3) | Floating supply voltage | | $(V_{BOthON})_{MAX}$ | | 20 | V |
| $V_{CIN}$ | Comparator input voltage | | 0 | | 15 | V |
| $V_{OUT}$ | DC Output voltage | | -10(4) | | 580 | V |
| $F_{SW}$ | Maximum switching frequency (5) | | | | 800 | kHz |
| VDD | Standard MCU operating voltage | | 3.0 | 3.3 | 3.6 | V |
| VDDA | MCU analog operating voltage (ADC not used) | Must have a potential equal to or higher than VDD | VDD | | 3.6 | V |
| | MCU analog operating voltage (ADC used) | | VDD | | 3.6 | V |
| $T_J$ | Operating junction temperature | | -40 | | 125 | °C |

1. $V_{LS} = VCC - V_{PGND}$
2. $V_{PS} = V_{PGND} - V_{SGND}$
3. $V_{BO} = V_{BOOT} - V_{OUT}$
4. *LVG off. VCC = 9 V. Logic is operational if* $V_{BOOT} > 5$ V
5. *Actual maximum* $F_{SW}$ *depends on power dissipation.*

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# 5 Electrical characteristics

(VCC=15 V; VDD=3.3 V; PGND = SGND; $T_J$ = +25 °C, unless otherwise specified)

**Table 7. Electrical characteristics**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power supply and standby mode** | | | | | | |
| $I_{QCCU}$ | VCC under-voltage quiescent supply current | VCC = 7 V;<br>EN = 5 V; CIN = SGND | | 430 | 744 | µA |
| $I_{QCC}$ | VCC quiescent supply current | EN = 5 V;<br>CIN = SGND<br>LVG & HVG: OFF | | 950 | 1450 | µA |
| $VCC_{thON}$ | VCC UVLO turn-on threshold | | 8 | 8.5 | 9 | V |
| $VCC_{thOFF}$ | VCC UVLO turn-off threshold | | 7.5 | 8 | 8.5 | V |
| $VCC_{hys}$ | VCC UVLO threshold hysteresis | | 0.4 | 0.5 | 0.6 | V |
| $I_{DD}$(1) | VDD current consumption<br>(Supply current in Run mode, code executing from Flash memory) | VDD = 3.6 V<br>HSE bypass, PLL off<br>$f_{HCLK}$ = 1 MHz | | 0.8 | | mA |
| | | VDD = 3.6 V<br>HSI clock, PLL on<br>$f_{HCLK}$ = 48 MHz | | 18.9 | | |
| $I_{DDA}$(1) | VDDA current consumption | VDD = 3.6 V<br>HSE bypass, PLL off<br>$f_{HCLK}$ = 1 MHz | | 2.0 | | µA |
| | | VDD = 3.6 V<br>HSI clock, PLL on<br>$f_{HCLK}$ = 48 MHz | | 220 | | |
| $V_{POR}$ | VDD Power on reset threshold | Rising edge | 1.84(2) | 1.92 | 2.00 | V |
| $V_{PDR}$ | VDD Power down reset threshold | Falling edge | 1.80 | 1.88 | 1.96(2) | V |
| $V_{PDRhyst}$ | VDD PDR hysteresis | | | 40 | | mV |
| **High-side floating section supply** | | | | | | |
| $I_{QBOU}$ | VBO under-voltage quiescent supply current | VCC = VBO = 6.5 V;<br>EN = 5 V; CIN = SGND | | 25 | 62 | µA |
| $I_{QBO}$ | VBO quiescent supply current | VBO = 15 V<br>EN = 5 V; CIN = SGND<br>LVG OFF; HVG = ON | | 84 | 150 | µA |
| $V_{BOthON}$ | VBO UVLO turn on threshold | | 7.5 | 8 | 8.5 | V |

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| Symbol | Parameter | Test condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{BOthOff}$ | VBO UVLO turn-off threshold | | | 7 | 7.5 | 8 | V |
| $V_{BOhys}$ | VBO UVLO threshold hysteresis | | | 0.4 | 0.5 | 0.6 | V |
| $I_{LK}$ | High voltage leakage current | BOOT = HVG = OUT = 620 V | | | | 15 | µA |
| $R_{Dboot}$ | Bootstrap diode on resistance | TJ = 25 °C | LVG ON | | 215 | 240 | Ω |
| | | | LVG OFF | | 215 | 250 | |
| **Output driving buffers** | | | | | | | |
| $I_{SO}$ | Source peak current | | | | | | |
| | STSPIN32F0601/Q | TJ = 25 °C | | 160 | 200 | 300 | mA |
| | | Full temperature range(3) | | 130 | | 350 | mA |
| | STSPIN32F0602/Q | TJ = 25 °C | | 0.88 | 1.0 | 1.33 | A |
| | | Full temperature range(3) | | 0.72 | | 1.48 | A |
| $I_{SI}$ | Sink peak current | | | | | | |
| | STSPIN32F0601/Q | TJ = 25 °C | | 230 | 350 | 430 | mA |
| | | Full temperature range(3) | | 200 | | 500 | mA |
| | STSPIN32F0602/Q | TJ = 25 °C | | 0.71 | 0.85 | 1.02 | A |
| | | Full temperature range(3) | | 0.51 | | 1.15 | A |
| $R_{DSonON}$ | Source $R_{DSon}$ | I = 10mA | | | | | |
| | STSPIN32F0601/Q | TJ = 25 °C | | 24 | 35 | 46 | Ω |
| | | Full temperature range(3) | | 20 | | 56 | Ω |
| | STSPIN32F0602/Q | TJ = 25 °C | | 5 | 6.4 | 7.6 | Ω |
| | | Full temperature range(3) | | 4.2 | | 10.3 | Ω |
| $R_{DSonOFF}$ | Sink $R_{DSon}$ | I = 10mA | | | | | |
| | STSPIN32F0601/Q | TJ = 25 °C | | 11 | 16 | 21 | Ω |
| | | Full temperature range(3) | | 8 | | 27 | Ω |
| | STSPIN32F0602/Q | TJ = 25 °C | | 5.5 | 6.7 | 8 | Ω |
| | | Full temperature range(3) | | 4.5 | | 11.2 | Ω |
| **Logic Inputs** | | | | | | | |
| $V_{il}$ | Low level logic threshold voltage | TTa type (4) | | | | 0.3·VDD+ 0.07 | V |
| | | FT, FTf type (4) | | | | 0.475 ·VDD –0.2 | V |
| $V_{ih}$ | High level logic threshold voltage | TTa type (4) | | 0.45 ·VDDIOx + 0.398 | | | V |
| | | FT, FTf type (4) | | 0.5 ·VDDIOx +0.2 | | | V |
| $V_{hyst}$ | Schmitt trigger hysteresis | TTa type (4) | | 200 | | | mV |
| | | FT, FTf type (4) | | 100 | | | mV |

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| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{lkg}$ | Input leakage current | TC, FT and FTf I/O TTa in digital mode<br>VSS ≤ VIN ≤ VDDIOx | | | ± 0.1 | µA |
| | | TTa in digital mode<br>VDDIOx ≤ VIN ≤ VDDA | | | 1 | |
| | | TTa in analog mode<br>VSS ≤ VIN ≤ VDDA | | | ± 0.1 | |
| | | FT and FTf I/O<br>VDDIOx ≤ VIN ≤ 5 V | | | 10 | |
| $V_{SSDh}$ | SmartSD restart threshold | | 3.5 | 4 | 4.3 | V |
| $V_{SSDl}$ | SmartSD unlatch threshold | | | 0.56 | 0.75 | V |
| **Sense Comparator and FAULT** | | | | | | |
| $V_{REF}$ | Internal voltage reference | | 410 | 460 | 510 | mV |
| $CIN_{hyst}$ | Comparator input hysteresis | | 40 | 70 | | mV |
| $CIN_{PD}$ | Comparator input pull-down current | VCIN = 1 V | 7 | 10 | 13 | µA |
| $I_{OD}$ | OD internal current source | | 2.5 | 5 | 7.5 | µA |
| $R_{ON_OD}$ | OD On resistance | IOD = 16 mA | 19 | 25 | 36 | W |
| $I_{SAT_OD}$ | OD saturation current | $V_{OD}$ = 5 V | | 95 | | mA |
| $V_{FLOAT_OD}$ | OD floating voltage level | OD connected only to an external capacitance | 4.4 | 4.8 | 5.2 | V |
| $I_{OL_OD}$ | OD low level sink current | $V_{OD}$ = 400 mV | 11 | 16 | 21 | mA |
| $R_{ON_F}$ | FAULT On resistance | $I_{FAULT}$ = 8 mA | | 50 | 100 | Ω |
| $I_{OL_F}$ | FAULT low level sink current | $V_{FAULT}$ = 400mV | 4 | 8 | 12 | mA |
| $t_{OD}$ | Comparator propagation delay | Rpu = 100 kΩ to 5 V;<br>0 to 3.3 V voltage step on CIN<br>50% CIN to 90% OD | | 350 | 500 | ns |
| $t_{CIN-F}$ | Comparator triggering to FAULT | 0 to 3.3 V voltage step on CIN;<br>50% CIN to 90% FAULT | | 350 | 500 | ns |
| $t_{CINoff}$ | Comparator triggering to high/low side driver propagation delay | 0 to 3.3 V voltage step on CIN<br>50% CIN to 90% LVG/HVG | | 360 | 510 | ns |
| $t_{FCIN}$ | Comparator input filter time | | 200 | 300 | 400 | ns |
| SR | Slew rate | CL = 1 nF; Rpu = 1 kΩ to 5 V;<br>90% to 10% OD | 4 | 7.7 | 10.3 | V/µs |

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| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Driver dynamic characteristics** | | | | | | |
| $t_{on}$ | High/Low-side driver turn-on propagation delay | OUT = 0 V<br>BOOT = VCC<br>CL = 1 nF<br>Vin = 0 to 3.3 Vsee Figure 4 | 45 | 85 | 120 | ns |
| $t_{off}$ | High/Low-side driver turn-off propagation delay | | 45 | 85 | 120 | ns |
| $t_{EN}$ | Enable to high/low side driver propagation delay | | 245 | 345 | 520 | ns |
| $t_r$ | Rise time | CL= 1 nF | | | | ns |
| | STSPIN32F0601/Q | | | 120 | | |
| | STSPIN32F0602/Q | | | 19 | | |
| $t_f$ | Fall time | CL= 1 nF | | | | ns |
| | STSPIN32F0601/Q | | | 50 | | |
| | STSPIN32F0602/Q | | | 17 | | |
| MT | Delay matching high/low side turn-on/off (6) | | | 0 | 30 | ns |
| DT | Deadtime | CL= 1 nF | 200 | 300 | 400 | ns |
| MDT | Matching deadtime (7) | CL= 1 nF | | 0 | 50 | ns |

1. *The current consumption depends on the firmware loaded in the microcontroller. See STM32F031x6x7 datasheet.www.st.com*
2. *Data based on characterization results, not tested in production.*
3. *Values provided by characterization, not tested*
4. *Data based on design simulation only. Not tested in production.*
5. *Comparator is disabled when VCC is in UVLO condition.*
6. *MT = max. ($|t_{on}(LVG) - t_{off}(LVG)|$, $|t_{on}(HVG) - t_{off(}HVG)|$, $|t_{off(}LVG) - t_{on}(HVG)|$, $|t_{off}(HVG) - t_{on}(LVG)|$)*
7. *MDT = | DTLH - DTHL |, refer to Figure 4.*

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Figure 4. **Propagation delay timing definition**

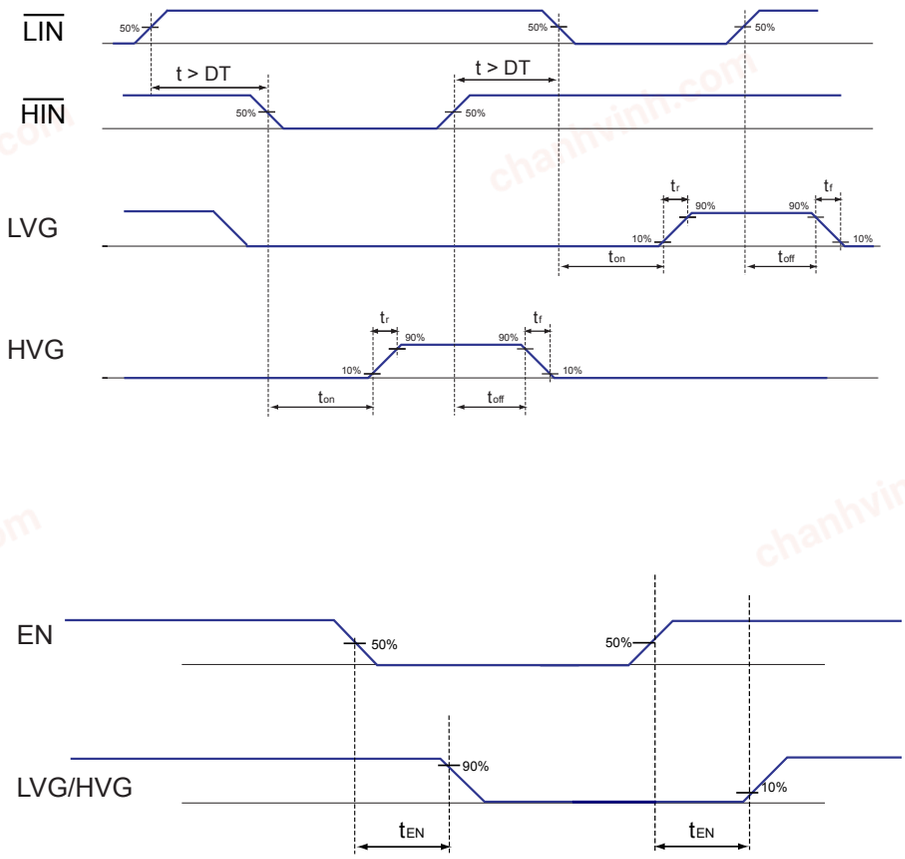
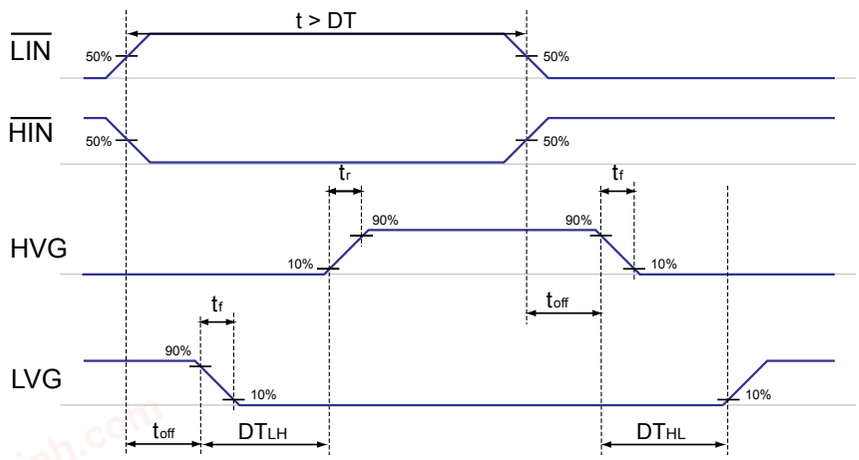






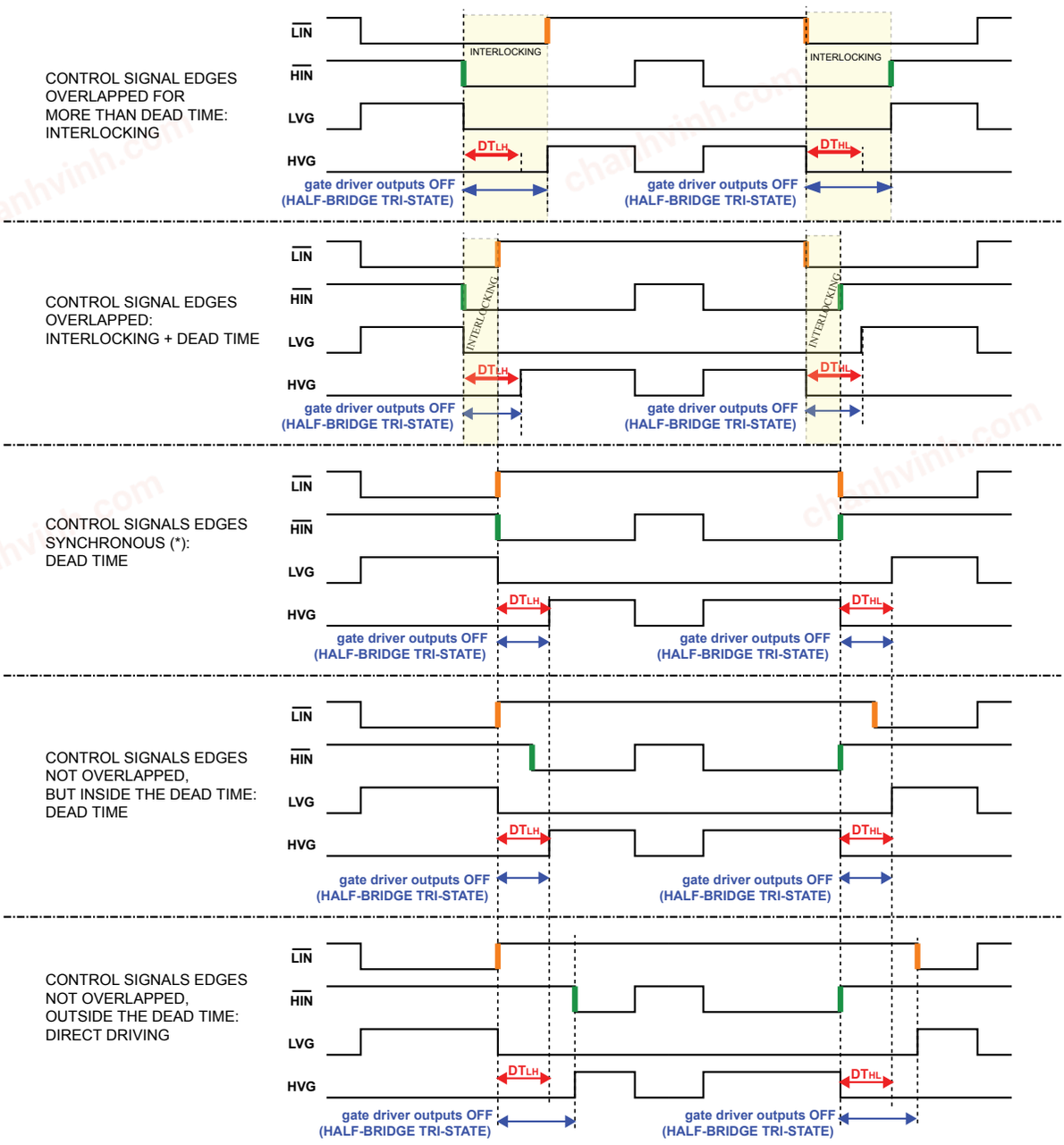
Figure 5. **Deadtime timing definitions**



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Figure 6. **Deadtime and interlocking waveforms definition**



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# 6 Device description

The STSPIN32F060x is a system-in-package providing an integrated solution suitable for driving high-voltage 3-phase applications.

## 6.1 Gate driver

The STSPIN32F060x integrates a triple half-bridge gate driver able to drive N-channel power MOSFETs or IGBTs. The high-side section is supplied by a bootstrapped voltage technique with integrated bootstrap diode.

All the inputs lines are connected to a pull-down resistor with typical value of 60 kΩ.

The high- and low-side outputs of same half-bridge cannot be simultaneously driven high thanks to an integrated interlocking function.

### 6.1.1 Inputs and outputs

The device is controlled through the following logic inputs:

- EN: enable input, active high;
- LIN: low-side driver inputs, active low;
- HIN: high-side driver inputs, active low.

**Table 8. Inputs truth table (applicable when device is not in UVLO or SmartSD protection)**

| | Input pins | | | Output pins | |
|---|---|---|---|---|---|
| | **EN** | **$\overline{\text{LIN}}$** | **$\overline{\text{HIN}}$** | **LVG** | **HVG** |
| | L | X | X | Low | Low |
| | H | H | H | Low | Low |
| | H | L | H | **HIGH** | Low |
| | H | H | L | Low | **HIGH** |
| **Interlocking** | H | L | L | Low | Low |

*Note: X : Don't care*

The FAULT and OD pins are open-drain outputs. The FAULT signal is set low in case VCC UVLO is detected, or in case the SmartShutDown comparator triggers an event. It is only used to signal a UVLO or SmartSD activation to external circuits, and its state does not affect the behavior of other functions or circuits inside the driver. The OD behavior is explained in Section 6.1.5 .

### 6.1.2 Deadtime

The deadtime feature, in companion with the interlocking feature, guarantees that driver outputs of the same channel are not high simultaneously and at least a DT time passes between the turn-off of one driver's output and the turn-on of the companion output of the same channel. If a deadtime longer than the internal DT is applied to LIN and HIN inputs by the external controller, the internal DT is ignored and the outputs follow the deadtime determined by the inputs. Refer to Figure 4 for the deadtime and interlocking waveforms.

### 6.1.3 VCC UVLO protection

Undervoltage protection is available on VCC and BOOT supply pins. In order to avoid intermittent operation, a hysteresis sets the turn-off threshold with respect to the turn-on threshold.

When VCC voltage goes below the $V_{CCthOFF}$ threshold all the outputs are switched off, both LVG and HVG. When VCC voltage reaches the $V_{CCthON}$ threshold the driver returns to normal operation and sets the LVG outputs according to actual input pins status; HVG is also set according to input pin status if the corresponding VBO section is not in UVLO condition. The FAULT output is kept low when VCC is in UVLO condition. The following figures show some examples of typical operation conditions.

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Figure 7. **VCC power ON and UVLO, LVG timing**

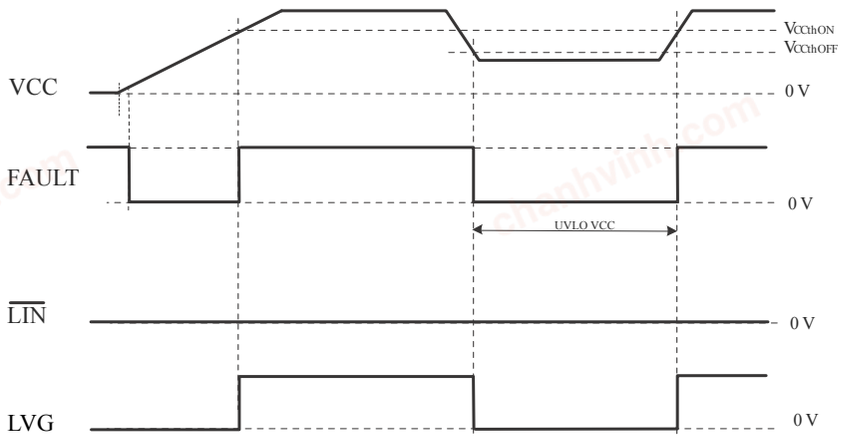
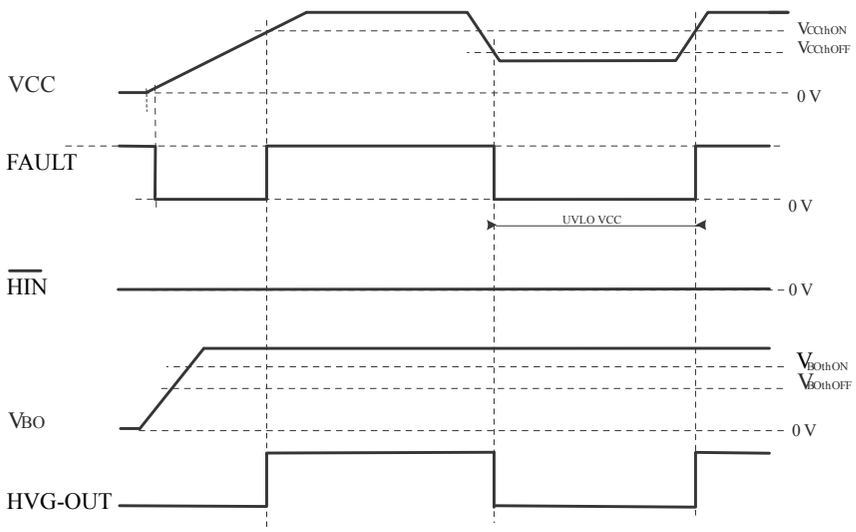



Figure 8. **VCC power ON and UVLO, HVG timing**




### 6.1.4 $V_{BO}$ UVLO protection

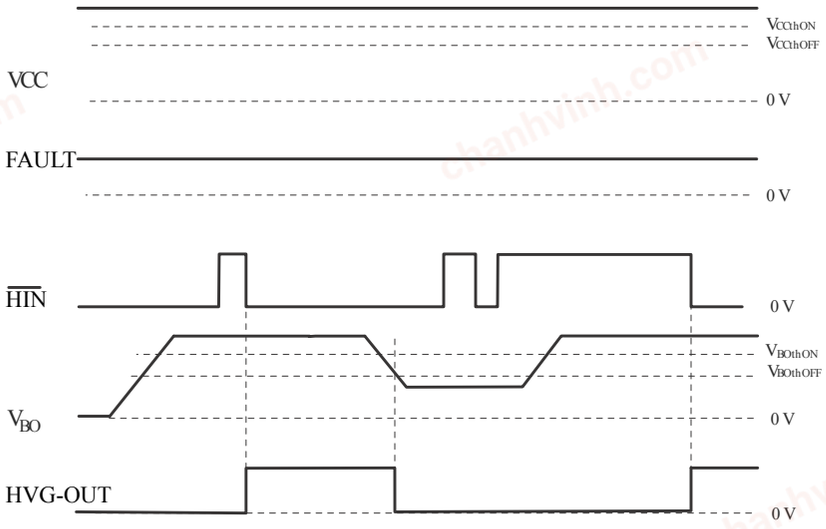
Dedicated undervoltage protection is available on each bootstrap section between BOOTx and OUTx supply pins. In order to avoid intermittent operation, a hysteresis sets the turn-off threshold with respect to the turn-on threshold.

When VBO voltage goes below the $V_{BOthOFF}$ threshold, the HVG output of the corresponding bootstrap section is switched off. When VBO voltage reaches the $V_{BOthON}$ threshold the device returns to normal operation and the output remains off up to the next input pins transition that requests HVG to turn on.

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Figure 9. **VBO Power-ON and UVLO timing**




### 6.1.5 Comparator and Smart shutdown

The STSPIN32F060x integrates a comparator committed to the fault protection function, thanks to the SmartShutDown (SmartSD) circuit.

The SmartSD architecture allows immediate turn-off of the gate driver outputs in the case of overload or overcurrent condition, by minimizing the propagation delay between the fault detection event and the actual output switch-off. In fact, the time delay between the fault detection and the output turn-off is not dependent on the value of the external components connected to the OD pin, which are only used to set the duration of disable time after the fault.

This provides the possibility to increase the duration of the output disable time after the fault event up to very large values without increasing the delay time of the protection. The duration of the disable time is determined by the values of the external capacitor $C_{OD}$ and of the optional pull-up resistor connected to the OD pin.

The comparator has an internal voltage reference $V_{REF}$ connected to the inverting input, while the non-inverting input is available on the CIN pin. The comparator's CIN input can be connected to an external shunt resistor in order to implement a fast and simple overcurrent protection function. The output signal of the comparator is filtered from glitches shorter than $t_{FCIN}$ and then fed to the SmartSD logic.

If the impulse on the CIN pin is higher than $V_{REF}$ and wider than $t_{FCIN}$, the SmartSD logic is triggered and immediately sets all of the driver outputs to low-level (OFF).

At the same time, FAULT is forced low to signal the event (for example to a MCU input) and OD starts to discharge the external $C_{OD}$ capacitor used to set the duration of the output disable time of the fault event.

The FAULT pin is released and driver outputs restart following the input pins as soon as the *output disable time* expires.

The overall disable time is composed of two phases:

- The OD *unlatch time* ($t_1$ in Figure 10), which is the time required to discharge the $C_{OD}$ capacitor down to the $V_{SSDl}$ threshold. The discharge starts as soon as the SSD comparator is triggered.
- The OD *Restart time* ($t_2$ in Figure 10), which is the time required to recharge the $C_{OD}$ capacitor up to the $V_{SSDh}$ threshold. The recharge of $C_{OD}$ starts when the OD internal MOSFET is turned-off, which happens when the fault condition has been removed (CIN < $V_{REF}$ - $C_{INhyst)}$ and the voltage on OD reaches the $V_{SSDl}$ threshold. This time normally covers most of the overall output disable time.

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If no external pull-up is connected to OD, the external $C_{OD}$ capacitor is discharged with a time constant defined by $C_{OD}$ and the internal MOSFET's characteristic (Equation 1), and the Restart time is determined by the internal current source $I_{OD}$ and by $C_{OD}$ (Equation 2 ).

**Equation 1**

$$t_1 \cong R_{ON_OD} \cdot C_{OD} \cdot \ln\left(\frac{V_{OD}}{V_{SSDl}}\right) \quad (1)$$

**Equation 2**

$$t_2 \cong \frac{C_{OD} \cdot V_{SSDh}}{I_{OD}} \cdot \ln\left(\frac{V_{SSDl} - V_{OD}}{V_{SSDh} - V_{OD}}\right) \quad (2)$$

Where $V_{OD} = V_{FLOAT_OD}$ In case the OD pin is connected to VCC by an external pull-up resistor $R_{OD_ext}$, the OD discharge time is determined by the external network $R_{OD_ext}$ $C_{OD}$ and by the internal MOSFET's $R_{ON_OD}$ (Equation 3), while the Restart time is determined by current in $R_{OD_ext}$ (Equation 4)

**Equation 3**

$$t_1 \cong C_{OD} \cdot \left(R_{OD_ext} // R_{ON_OD}\right) \cdot \ln\left(\frac{V_{OD} - V_{on}}{V_{SSDl} - V_{on}}\right) \quad (3)$$

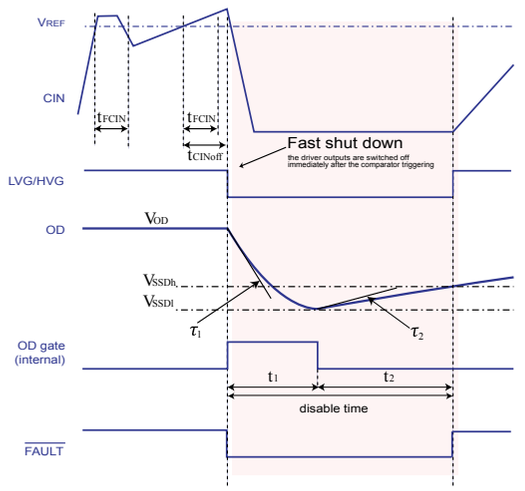
**Equation 4**

$$t_2 \cong C_{OD} \cdot R_{OD_ext} \cdot \ln\left(\frac{V_{SSDl} - V_{OD}}{V_{SSDh} - V_{OD}}\right) \quad (4)$$

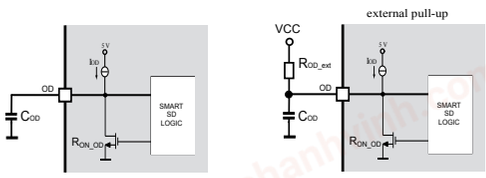
where

$$V_{on} = \frac{R_{ON_OD}}{R_{OD_ext} + R_{ON_OD}} \cdot V_{cc} \;\; ; \;\; V_{OD} = V_{cc}$$

**Figure 10. Smart shutdown timing waveforms**




**SMART SHUTDOWN CIRCUIT**



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## 6.2 Microcontroller unit

The integrated MCU is the STM32F031x6 with the following main characteristics:

- Core: ARM® 32-bit Cortex® -M0 CPU, frequency up to 48 MHz
- Memories: 4kB of SRAM, 32 kB of Flash Memory
- CRC calculation unit
- Up to 21 fast I/Os
- Advanced-control timer dedicated for PWM generation
- Up to 6 general purpose timers
- 12-bit ADC (up to 10 channels)
- Communication interfaces: $I^2C$, USART, SPI
- Serial Wire Debug (SWD)
- Extended temperature range: -40 to 125°C

*Note: For more details refer to the STM32F031x6 datasheet on www.st.com*

### 6.2.1 Memories and boot mode

The device has the following features:

- 4 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 32 Kbytes of embedded Flash memory for programs and data
  - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled.

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot loader is located in System Memory, programmed by ST during production. It is used to reprogram the Flash memory by using USART on pins PA14/PA15.

### 6.2.2 Power management

The VDD pin is the power supply for I/Os and the internal regulator.

The VDDA pin is power supply for ADC, Reset blocks, RCs and PLL. The VDDA voltage is provided externally through VDDA pin

*Note: The VDDA voltage level must be always greater or equal to the VDD voltage level and must be established first.*

The MCU has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, VPOR/PDR, without the need for an external reset circuit.

- The POR monitors only the VDD supply voltage. During the startup phase it is required that VDDA should arrive first and be greater than or equal to VDD.
- The PDR monitors both the VDD and VDDA supply voltages, however the VDDA power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that VDDA is higher than or equal to VDD.

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The device features an embedded programmable voltage detector (PVD) that monitors the VDD power supply and compares it to the VPVD threshold. An interrupt can be generated when VDD drops below the VPVD threshold and/or when VDD is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

The MCU supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines (one of the 16 external lines, the PVD output, RTC, $I^2C1$ or USART1).

- **Standby mode**

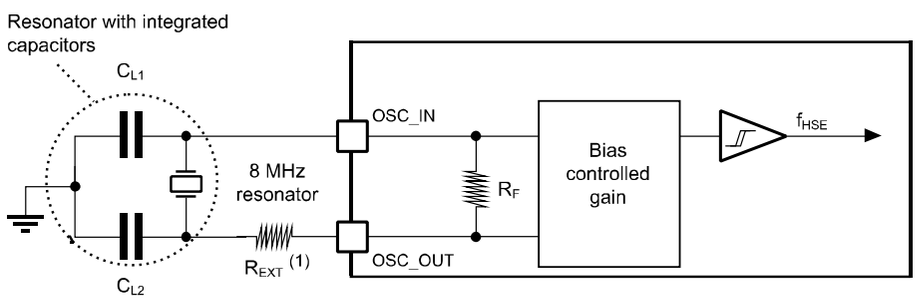
  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HIS RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

### 6.2.3 High-speed external clock source

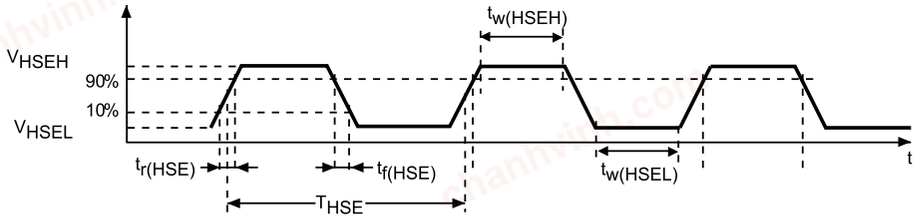
The high-speed external (HSE) clock can be generated from external clock signal or supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator (see Figure 11). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

**Figure 11. Typical application with 8 MHz crystal**




1. The REXT value depends on the crystal characteristics (refer to the crystal resonator manufacturer for more details on them).
2. The external clock signal has to respect the I/O characteristics and follows recommended clock input waveform (refer to Figure 12).

**Figure 12. HSE clock source timing diagram**



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## 6.3 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted deadtimes.

This timer is used to generate the PWM signal for the three half-bridge gate drivers as shown in Table 9.

**Table 9. TIM1 channel configuration**

| MCU I/O | ASIC input | TIM1 channel |
|---|---|---|
| PB13 | LIN1 | TIM1_CH1N |
| PB14 | LIN2 | TIM1_CH2N |
| PB15 | LIN3 | TIM1_CH3N |
| PA8 | HIN1 | TIM1_CH1 |
| PA9 | HIN2 | TIM1_CH2 |
| PA10 | HIN3 | TIM1_CH3 |

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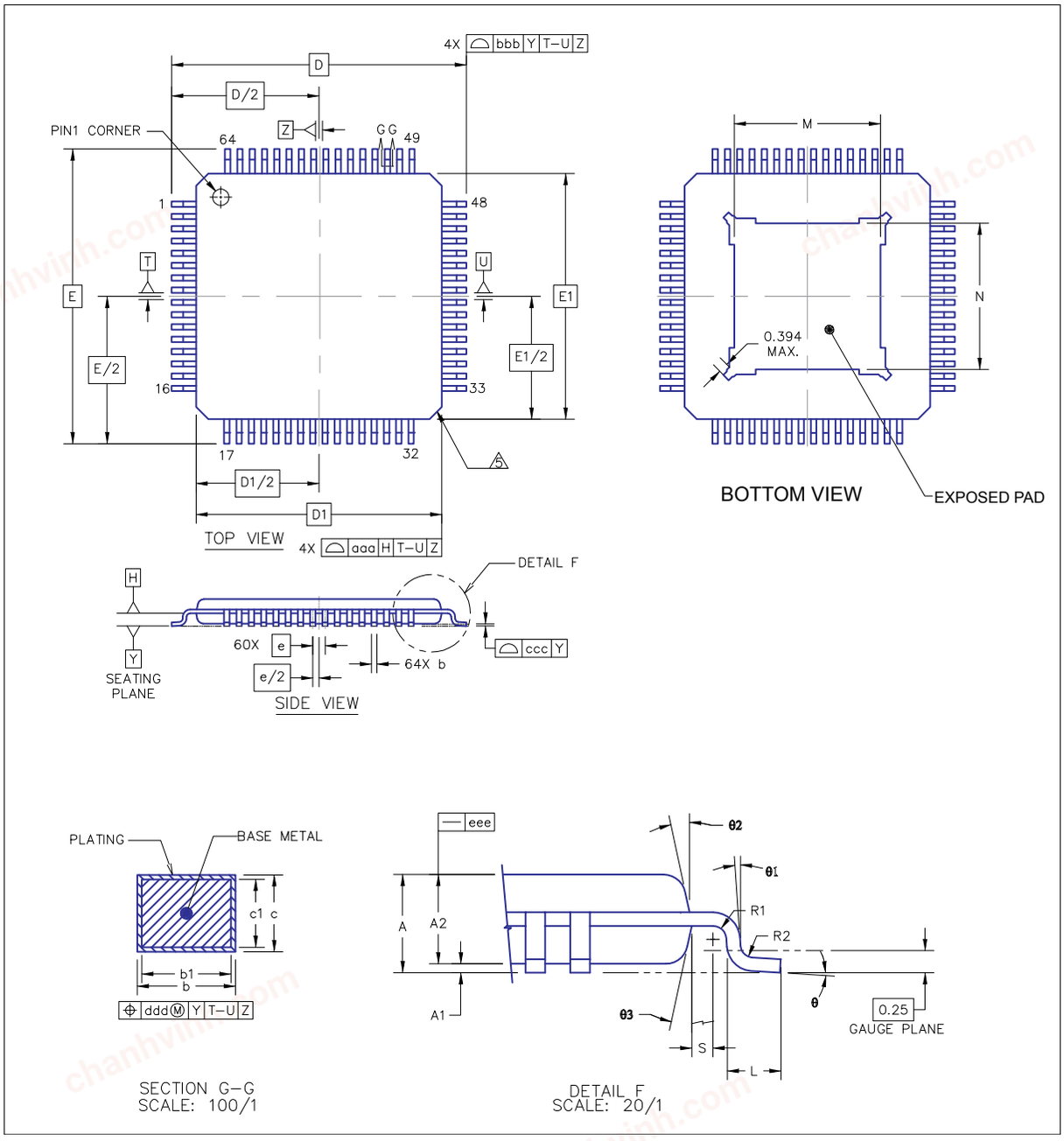


# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 7.1 TQFP 10x10 64L package information

**Figure 13. TQFP mechanical data**



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**Table 10. TQFP package dimensions**

| | | Symbol | Min | Nom | Max |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | - | - | 1.2 |
| STAND OFF | | A1 | 0.05 | - | 0.15 |
| MOLD THICKNESS | | A2 | 0.95 | - | 1.05 |
| LEAD WIDTH(PLATING) | | b | 0.17 | 0.22 | 0.27 |
| LEAD WIDTH | | b1 | 0.17 | 0.2 | 0.23 |
| L/F THICKNESS(PLATING) | | c | 0.09 | - | 0.2 |
| L/F THICKNESS | | c1 | 0.09 | - | 0.16 |
| | X | D | - | 12 | - |
| | Y | E | - | 12 | - |
| BODY SIZE | X | D1 | - | 10 | - |
| | Y | E1 | - | 10 | - |
| LEAD PITCH | | e | - | 0.5 | - |
| | | L | 0.45 | 0.6 | 0.75 |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | - | - |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | - | - |
| | | R2 | 0.08 | - | 0.2 |
| | | S | 0.2 | - | - |
| EP SIZE | X | M | 5.85 | 5.95 | 6.05 |
| | Y | N | 5.85 | 5.95 | 6.05 |
| PACKAGE LEAD TOLERANCE | | aaa | 0.2 | | |
| LEAD EDGE TOLERANCE | | bbb | 0.2 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.08 | | |
| MOLD FLATNESS | | eee | 0.05 | | |

*Note: All dimensions are mm unless otherwise specified*

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Figure 14. **QFN mechanical data**

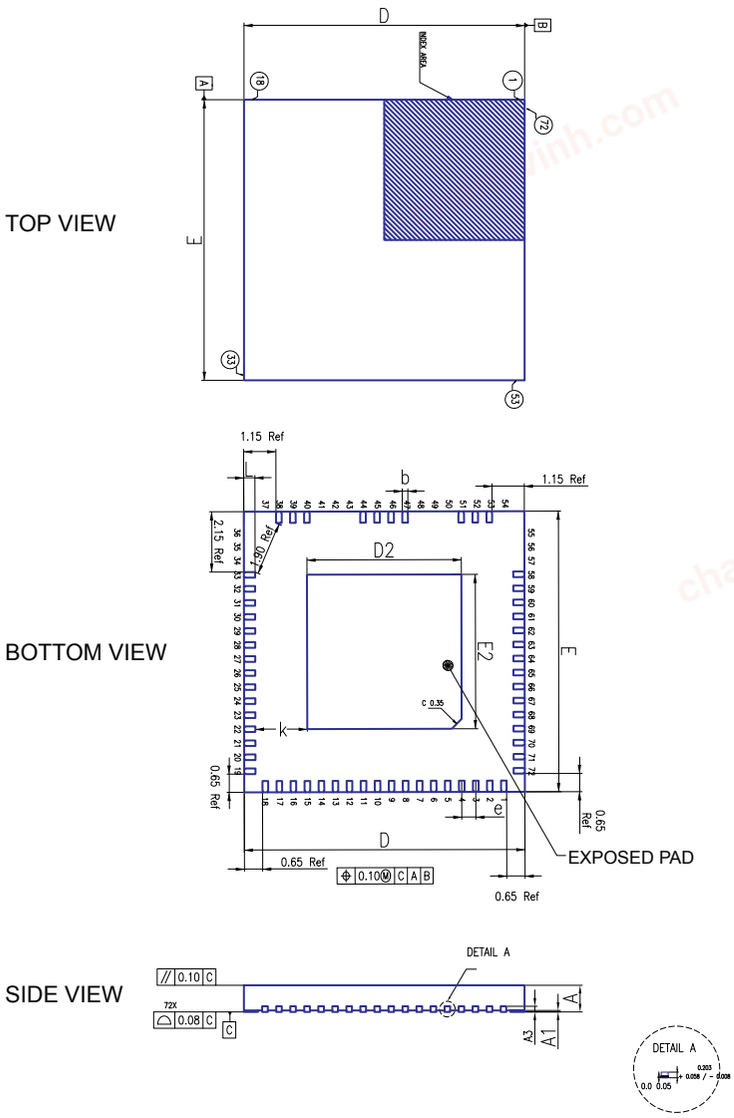



Table 11. **QFN package dimensions**

| | Symbol | Min | Non | Max |
|---|---|---|---|---|
| TOTAL THICKNESS | A | 0.90 | 0.95 | 1.00 |
| STAND OFF | A1 | 0 | | 0.05 |
| L/F THICKNESS | A3 | | 0.20 Ref. | |
| LEAD WIDTH | b | 0.15 | 0.20 | 0.25 |
| BODY LENGTH X | D | 9.90 | 10.00 | 10.10 |
| EP LENGTH X | D2 | 5.40 | 5.50 | 5.60 |
| LEAD PITCH | e | | 0.50 BSC | |
| BODY WIDTH Y | E | 9.90 | 10.00 | 10.10 |
| EP WIDTH Y | E2 | 5.40 | 5.50 | 5.60 |
| LEAD LENGTH | L | 0.30 | 0.40 | 0.50 |

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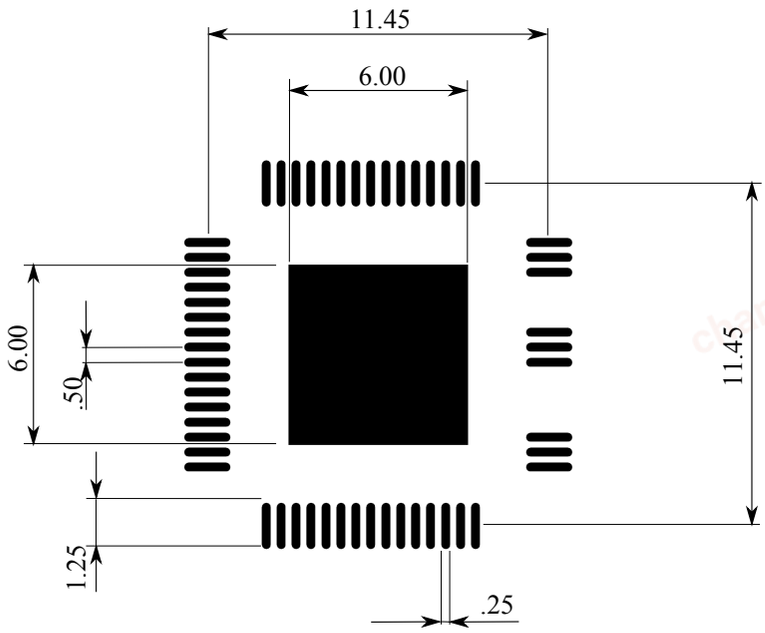


| | Symbol | Min | Non | Max |
|---|---|---|---|---|
| | K | | 1.85 Ref. | |

*Note: All dimensions are mm unless otherwise specified*

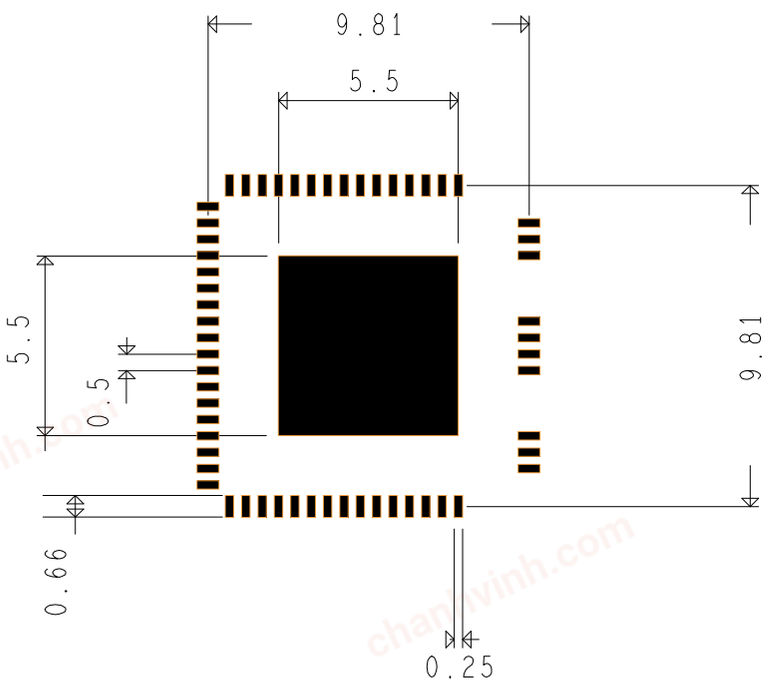
## 7.2 Suggested land pattern

**Figure 15. TQFP 10x10 64L suggested land pattern**




*Note: All dimensions are mm unless otherwise specified*

**Figure 16. QFN 10x10 72L suggested land pattern**



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# 8 Ordering information

Table 12. **Order codes**

| Order code | Package | Package marking | Packaging |
|---|---|---|---|
| STSPIN32F0601 | TQFP 10x10 64L | STSPIN32F0 601 | Tray |
| STSPIN32F0601TR | TQFP 10x10 64L | STSPIN32F0 601 | Tape and Reel |
| STSPIN32F0602 | TQFP 10x10 64L | STSPIN32F0 602 | Tray |
| STSPIN32F0602TR | TQFP 10x10 64L | STSPIN32F0 602 | Tape and Reel |
| STSPIN32F0601Q | QFN 10 x 10 72L | SPINF601Q | Tray |
| STSPIN32F0601QTR | QFN 10 x 10 72L | SPINF601Q | Tape and Reel |
| STSPIN32F0602Q | QFN 10 x 10 72L | SPINF602Q | Tray |
| STSPIN32F0602QTR | QFN 10 x 10 72L | SPINF602Q | Tape and Reel |

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## Revision history

Table 13. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 12-Jun-2019 | 1 | Initial release. |
| 29-Aug-2019 | 2 | Minor text changes |
| 04-Sept-2019 | 3 | Minor change to Table 10 |
| 28-Oct-2020 | 4 | Added QFN package version |
| 20-Feb-2021 | 5 | Updated Table 5, Table 7. Updated Figure 6, 7, 8, 9, and 10. |

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# Contents

1 Block diagram . . . 3
2 Pin description and connection diagram . . . 4
3 Pin description table . . . 6
4 Electrical data . . . 8
4.1 Absolute maximum ratings . . . 8
4.2 Thermal data . . . 9
4.3 Recommended operating conditions . . . 9
5 Electrical characteristics . . . 10
6 Device description . . . 16
6.1 Gate driver . . . 16
6.1.1 Inputs and outputs . . . 16
6.1.2 Deadtime . . . 16
6.1.3 VCC UVLO protection . . . 16
6.1.4 $V_{BO}$ UVLO protection . . . 17
6.1.5 Comparator and Smart shutdown . . . 18
6.2 Microcontroller unit . . . 20
6.2.1 Memories and boot mode . . . 20
6.2.2 Power management . . . 20
6.2.3 High-speed external clock source . . . 21
6.3 Advanced-control timer (TIM1) . . . 22
7 Package information . . . 23
7.1 [Package name] package information . . . 23
7.2 Suggested land pattern . . . 26
8 Ordering information . . . 27
Revision history . . . 28
Contents . . . 29
List of tables . . . 30
List of figures . . . 31

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# List of tables

Table 1. Legend/abbreviations used in the pin description table . . . 5
Table 2. STSPIN32F060x MCU-Driver internal connections . . . 5
Table 3. Pin description . . . 6
Table 4. Absolute maximum ratings . . . 8
Table 5. Thermal data . . . 9
Table 6. Recommended operating conditions . . . 9
Table 7. Electrical characteristics . . . 10
Table 8. Inputs truth table (applicable when device is not in UVLO or SmartSD protection) . . . 16
Table 9. TIM1 channel configuration . . . 22
Table 10. TQFP package dimensions . . . 24
Table 11. QFN package dimensions . . . 25
Table 12. Order codes . . . 27
Table 13. Document revision history . . . 28

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# List of figures

Figure 1. STSPIN32F060x SiP block diagram . . . 3
Figure 2. STSPIN32F060x pin connection (TQFP top view) . . . 4
Figure 3. STSPIN32F060x pin connection (QFN top view) . . . 4
Figure 4. Propagation delay timing definition . . . 14
Figure 5. Deadtime timing definitions . . . 14
Figure 6. Deadtime and interlocking waveforms definition . . . 15
Figure 7. VCC power ON and UVLO, LVG timing . . . 17
Figure 8. VCC power ON and UVLO, HVG timing . . . 17
Figure 9. VBO Power-ON and UVLO timing . . . 18
Figure 10. Smart shutdown timing waveforms . . . 19
Figure 11. Typical application with 8 MHz crystal . . . 21
Figure 12. HSE clock source timing diagram . . . 21
Figure 13. TQFP mechanical data . . . 23
Figure 14. QFN mechanical data . . . 25
Figure 15. TQFP 10x10 64L suggested land pattern . . . 26
Figure 16. QFN 10x10 72L suggested land pattern . . . 26

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