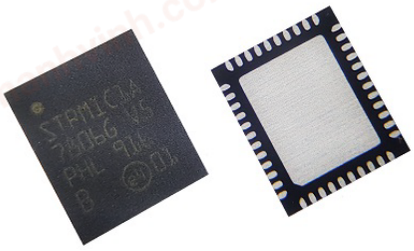
chanhvinh.com

life.augmented

STPMIC1

Datasheet

Highly integrated power management IC for micro processor units



Features

- Input voltage range from 2.8 V to 5.5 V
- 4 adjustable general purpose LDOs
- 1 LDO for DDR3 termination (sink-source), bypass mode for low power DDR or as general purpose LDO
- 1 LDO for USB PHY supply with automatic power source detection
- 1 reference voltage LDO for DDR memory
- 4 adjustable adaptive constant on-time (COT) buck SMPS converters
- 5.2 V / 1.1 A boost SMPS with bypass mode for 5 V input or battery input
- 1 power switch 500 mA USB OTG compliant
- 1 power switch 500 mA/1000 mA general purpose
- User programmable non-volatile memory (NVM), enabling scalability to support a wide range of applications
- I²C and digital IO control interface
- WFQFN 44L (5x6x0.8)

Applications

- Power management for embedded micro processor units
- Wearable and IoT
- Portable devices
- Man-machine interfaces
- Smart home
- Power management unit companion chip of the STM32MP1 MPU

Product status link
STPMIC1

Device summary	
Order code	STPMIC1APQR
	STPMIC1BPQR
	STPMIC1CPQR
	STPMIC1DPQR
	STPMIC1EPQR
Packing	WFQFN 44L (5x6x0.8)

Description

The STPMIC1 is a fully integrated power management IC designed for products based on high integrated application processor designs requiring low power and high efficiency.

The device integrates advanced low power features controlled by a host processor via I²C and IO interface.

The STPMIC1 regulators are designed to supply power to the application processor as well as to the external system peripherals such as: DDR, Flash memories and other system devices.

The boost converter can power up to 3 USB ports (two 500 mA host USB and one 100 mA USB OTG). Its advanced bypass architecture allows the smooth regulation of VBUS for USB ports from a battery as well as low-cost consumer 5 V AC-DC adapters.

4 buck SMPS are optimized to provide an excellent transient response and an output voltage precision for a wide range of operating conditions, high full range efficiency (η up to 90%) by implementing a low power mode with a smooth transition from PFM to PWM and also an advanced PWM synchronization technique with an integrated PLL for a better noise (EMI performance).

chanhvinh.com

1 Device configuration

The STPMIC1 has a non-volatile memory (NVM) that enables scalability to support a wide range of applications:

- Default output voltage, POWER_UP/POWER_DOWN sequence, protection behavior, auto turn-on functionality, I^2C slave address
- The STPMIC1A, STPMIC1B, STPMIC1D and STPMIC1E are pre-programmed devices to support the STM32MP1 series application processor versions
- The STPMIC1C is not a programmed device to support custom applications
- Straightforward NVM (re)programming via I^2C to facilitate mass production directly in target applications

Table 1. Default NVM configuration vs part number

	Default configuration table									
	STPMIC1A		STPMIC1B		STPMIC1C		STPMIC1D		STPMIC1E	
	Default output voltage	Rank	Default output voltage	Rank	Default output voltage	Rank	Default output voltage	Rank	Default output voltage	Rank
LDO1	1.8 V	0	1.8 V	0	1.8 V	0	1.8 V	0	1.8 V	0
LDO2	1.8 V	0	2.9 V	2	1.8 V	0	1.8 V	0	1.8 V	0
LDO3	1.8 V	0	1.8 V	0	1.8 V	0	1.8 V	0	1.8 V	0
LDO4	3.3 V	3	3.3 V	3	3.3 V	0	3.3 V	3	3.3 V	3
LDO5	2.9 V	2	2.9 V	2	1.8 V	0	3.3 V	2	2.9 V	2
LDO6	1.0 V	0	1.0 V	0	1.0 V	0	1.0 V	0	1.0 V	0
REFDDR	0.55 V	0	0.55 V	0	0.55 V	0	0.55 V	0	0.55 V	0
BOOST	5.2 V	N/A	5.2 V	N/A	5.2 V	N/A	5.2 V	N/A	5.2 V	N/A
BUCK1	1.2 V	2	1.2 V	2	1.1 V	0	1.2 V	3	1.2 V	3
BUCK2	1.1 V	0	1.1 V	0	1.1 V	0	1.1 V	0	1.1 V	0
BUCK3	3.3 V	1	1.8 V	1	1.2 V	0	3.3 V	1	1.8 V	1
BUCK4	3.3 V	2	3.3 V	2	1.15 V	0	1.2 V	2	1.2 V	2
	Default value									
VINOK_Rise	3.5 V		3.3 V		3.5 V		4.0 V		3.3 V	

The start-up sequence is split into four steps (Rank0 to Rank3).

Each BUCK converter or LDO regulator can be programmed to be automatically turned ON in one of these phases:

- Rank= 0: rail not turned ON automatically, no output voltage appears after POWER-UP
- Rank= 1: rail automatically turned ON after 7 ms following a Turn_ON condition
- Rank= 2: rail automatically turned ON after further 3 ms
- Rank= 3: rail automatically turned ON after further 3 ms

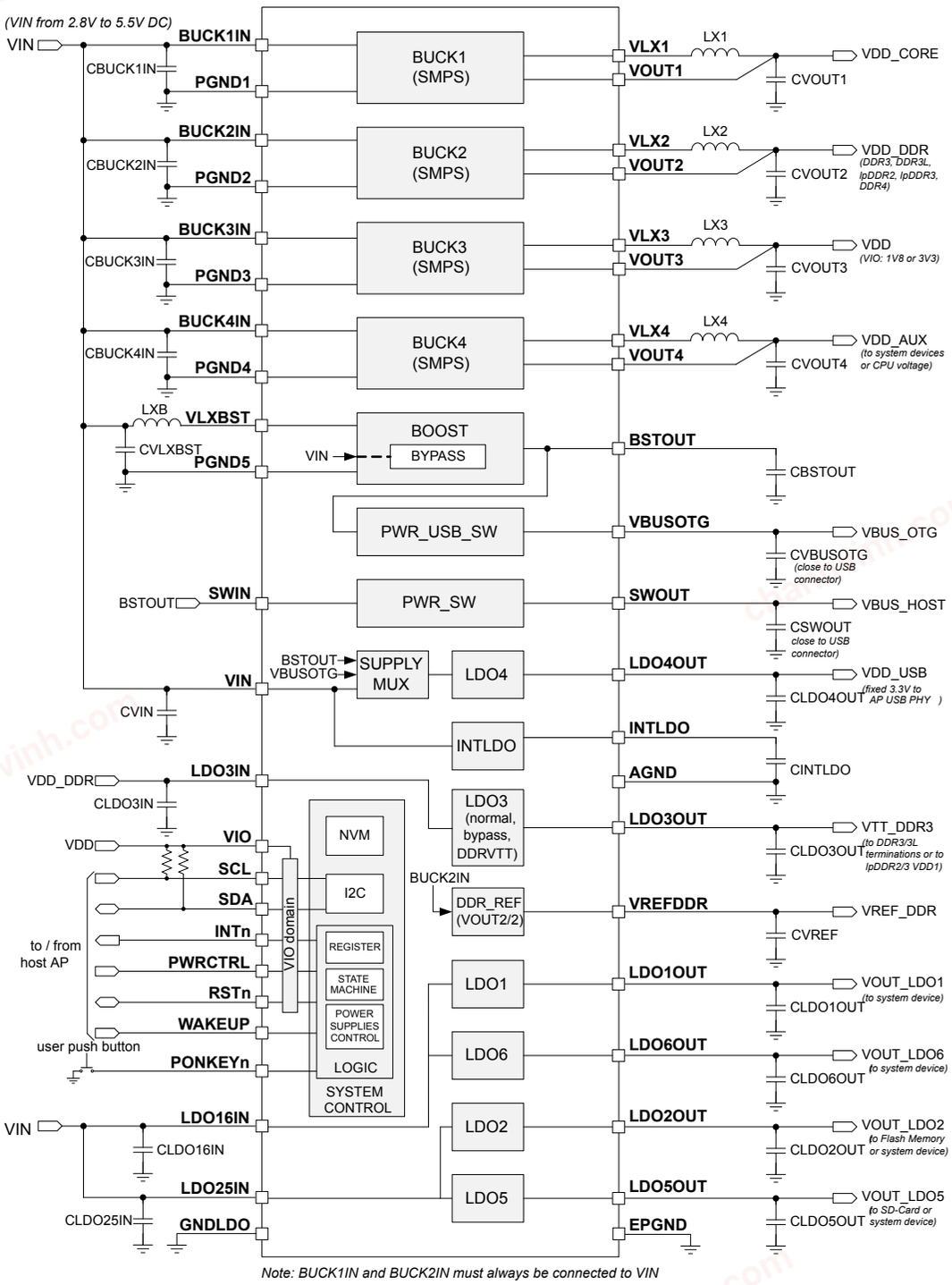
Whatever the STPMIC1 version:

- AUTO_TURN_ON option is set
- Boost and switches cannot be turned ON automatically

chanhvinh.com

2 Typical application schematic

Figure 1. **Typical application schematic**



Note: BUCK1IN and BUCK2IN must always be connected to VIN

chanhvinh.com

2.1 Recommended external components

Table 2. Passive components

Component	Manufacturer	Part number	Value	Size
CVIN, CLDO1OUT, CLDO2OUT, CLDO4OUT, CLDO5OUT, CLDO6OUT, CINTLDO	Murata	GRM155R60J475ME47#(1)	4.7 µF	0402
CVLXBST, CBUCK1IN, CBUCK2IN, CBUCK3IN, CBUCK4IN, CLDO3IN, CLDO3OUT(2)		GRM188R61A106KE69D	10 µF	0603
CLDO16IN, CLDO25IN, CVREF		GRM155R61E105KA12	1 µF	0402
CVBUSOTG		GRM188R61C475KE11#	4.7 µF	0603
CBSTOUT, CVOUT1, CVOUT2, CVOUT3, CVOUT4		GRM188R60J226MEA0	22 µF	0603
CSWOUT		GRM31CR60J227ME11L	220 µF	0603
LX1, LX2, LX3, LX4, LXB		DFE252012P-1R0M=P2	1 µH	1008

1. *# is the last P/N digit; it indicates a package specification code.*
2. *4.7 µF normal mode - 10 µF sink/source mode - no cap bypass mode.*

Note: All the components above refer to a typical application. Operation of the device is not limited to the choice of these external components.

chanhvinh.com

2.2 Pinout and pin description

Figure 2. **Pin configuration WFQFN 44L top view**

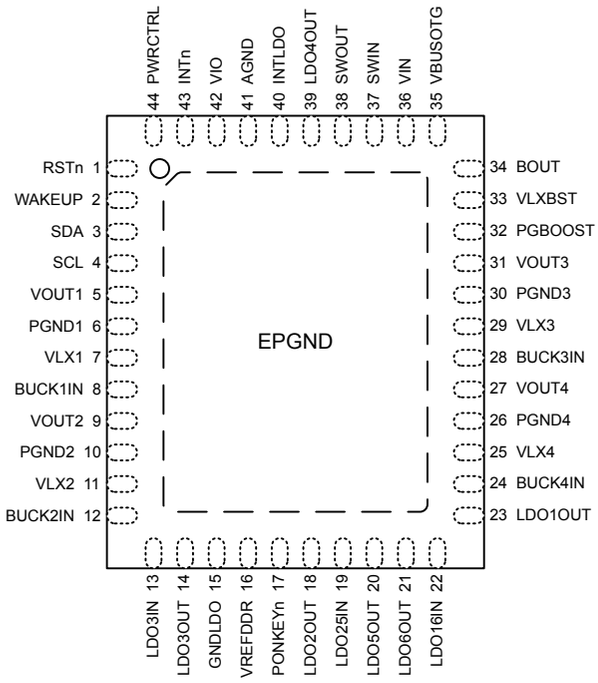


Table 3. **Pin description**

Pin name	A/D(1)	I/O	Location	Description (default configuration)
RSTn	D	I/O	1	Bi-directional reset (active low with internal pull-up)
WAKEUP	D	I	2	Power-ON from host processor (active high with internal pull-down)
SDA	D	I/O	3	I^2C serial data
SCL	D	I	4	I^2C serial clock
VOUT1	A	I	5	Input feedback signal buck converter 1
PGND1	A	-	6	Power ground buck converter 1
VLX1	A	O	7	LX node buck converter 1
BUCK1IN	A	I	8	Power input buck converter 1 must be connected to the same value of VIN pin
VOUT2	A	I	9	Input feedback signal buck converter 2
PGND2	A	-	10	Power ground buck converter 2
VLX2	A	O	11	LX node buck converter 2
BUCK2IN	A	I	12	Power input buck converter 2 must be connected to the same value of VIN pin
LDO3IN	A	I	13	Power input LDO3
LDO3OUT	A	O	14	Output voltage LDO3
GNDLDO	A	-	15	LDO GND
VREFDDR	A	O	16	DDR VREF output voltage
PONKEYn	D	I	17	User power ON key (active low with internal pullup)

chanhvinh.com

Pin name	A/D[1]	I/O	Location	Description (default configuration)
LDO2OUT	A	O	18	Output voltage LDO2
LDO25IN	A	I	19	Power input LDO2 and LDO5
LDO5OUT	A	O	20	Output voltage LDO5
LDO6OUT	A	O	21	Output voltage LDO6
LDO16IN	A	I	22	Power input LDO1 and LDO6
LDO1OUT	A	O	23	Output voltage LDO1
BUCK4IN	A	I	24	Power input buck converter 4 must be connected to the same value of VIN pin
VLX4	A	O	25	LX node buck converter 4
PGND4	A	-	26	Power ground buck converter 4
VOUT4	A	I	27	Input feedback signal buck converter 4
BUCK3IN	A	I	28	Power input buck converter 3 must be connected to the same value of VIN pin
VLX3	A	O	29	LX node buck converter 3
PGND3	A	-	30	Power ground buck converter 3
VOUT3	A	I	31	Input feedback signal buck converter 3
PGND5	A	-	32	Power ground boost converter
VLXBST	A	I	33	LX Node boost converter
BSTOUT	A	O	34	Output voltage boost converter
VBUSOTG	A	O	35	Power output switch powered by boost converter
VIN	A	I	36	Main power input - power input LDO4, VREF
SWIN	A	I	37	Power input switch
SWOUT	A	O	38	Power output switch
LDO4OUT	A	O	39	Output voltage LDO4
INTLDO	A	O	40	Internal LDO
AGND	A	-	41	Main analog ground
VIO	A	I	42	I/O voltage (for all digital signals except WAKEUP and PONKEYn)
INTn	D	O	43	Interrupt (active low with internal pull-up)
PWRCTRL	D	I	44	Power control mode (pull-up and pull-down inactive by default)
EPGND	A	-	ePad	Exposed pad to be connected to ground

1. *A: analog; D: digital*

chanhvinh.com

3 Electrical and timing characteristics

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Parameter	Min.	Unit
VIN, BUCKxIN, SWIN, LDO3IN, LDOxxIN, PONKEYn	-0.5 to 7	V
VIO, SDA, SCL, RSTn, PWRCTRL, INTn, WAKEUP	-0.5 to 4.2	V
INTLDO	-0.5 to 2	V
VLXx	-0.5 to 7	V
VOUT1, VOUT2	-0.5 to 3	V
VOUT3, VOUT4	-0.5 to 5	V
BSTOUT, VBUSOTG, VLXBST, SWOUT	-0.5 to 7	V
LDOxOUT, VREFDDR	-0.5 to 5	V
T_{STO} storage temperature	-65 to 150	°C
ESD human body model	±1000	V
ESD charge device model	±500	V

Note: Once the normal operating conditions are exceeded, the performance of the device may suffer. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

3.2 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Min.	Max.	Unit
T_J	Operating junction temperature	-40	125	°C
T_{JAMR}	Absolute maximum junction temperature	-40	160	°C
T_A	Operating ambient temperature	-40	105	°C
Θ_{JC}	Junction-case package thermal resistance JEDEC reference (JESD51-12.01)		7	°C/W
Θ_{JA}	Junction-ambient package thermal resistance on 2s2p std JEDEC board (JESD51-7)		29	

chanhvinh.com

3.3 Consumption in typical application scenarios

Table 6. Consumption in typical application scenarios

Application mode	Application description	Conditions	Min.	Typ.	Max.	Unit
STPMIC1 VIN input current consumption (all supply pins connected to VIN, V_{IN} = 3.6 V, V_{IO} = 1.8 V(from V_{OUT3}), T_A= +25 °C)						
OFF	Application is OFF, waiting for turn-on event to start	STPMIC1 in OFF-state Turn-on from PONKEYn, WAKEUP and VBUSOTG/SWOUT active No activity on I^2C VIO=0 V (BUCK3 is OFF)		50		µA
STANDBY	Application is in STANDBY,AP always ON power domain is present	STPMIC1 in POWER_ON state IRQ from PONKEYn, WAKEUP and VBUSOTG/SWOUT BUCK3 active in LP mode, V_{OUT3}=1.8 V All other regulators OFF All outputs without load No activity on I^2C		110		µA
STOP	Application is in STOP mode, AP core voltages are supplied, and DDR memory in self refresh	STPMIC1 in POWER_ON state IRQ from PONKEYn WAKEUP and VBUSOTG/SWOUT BUCK1 active in LP mode, V_{OUT}=1.2 V BUCK2 active in LP mode, V_{OUT}=1.2 V BUCK3 active in LP mode, V_{OUT}=1.8 V REF_DDR active LDO3 active All other regulators OFF All outputs without load No activity on I^2C		370		µA
RUN	Application is running	STPMIC1 in POWER_ON state IRQ from PONKEYn WAKEUP and VBUSOTG/SWOUT BUCK1 active in HP mode, V_{OUT}=1.2 V BUCK2 active in HP mode, V_{OUT}=1.2 V BUCK3 active in HP mode, V_{OUT}=1.8 V REF_DDR active LDO3 active, V_{OUT}=1.8 V All other regulators OFF All outputs without load No activity on I^2C		1.2		mA

chanhvinh.com

3.4 Electrical and timing parameters

Table 7. Electrical and timing parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{IN} = 3.6 V, V_{OUT1} = 1.2 V, V_{OUT2} = 1.2 V, V_{OUT3} = 1.8 V, V_{OUT4} = 3.3 V, $V_{LDO1OUT}$/$V_{LDO3OUT}$ = 1.8 V, $V_{LDO2OUT}$/$V_{LDO5OUT}$/$V_{LDO6OUT}$ = 2.9 V, V_{IO} = 1.8 V, recommended BOM, T_j = -40 °C to +125 °C, unless otherwise specified.						
V_{IN}	Input voltage range		2.8	3.6	5.5	V
$V_{IN_POR_Rise}$	VIN POR rising threshold		2.2	2.3	2.4	V
$V_{IN_POR_Fall}$	VIN POR falling threshold		2	2.1	2.2	V
V_{INOK_Rise}	VINOK rising threshold	Programmable value, defined in NVM register Table 65. NVM_MAIN_CTRL_SHR	3 3.2 3.4 3.9	3.1 3.3 3.5 4	3.2 3.4 3.6 4.1	V
V_{INOK_HYST}	VINOK hysteresis	Programmable value, defined in NVM register Table 65. NVM_MAIN_CTRL_SHR		200 300 400 500		mV
V_{INOK_Fall}	VINOK falling threshold	Defined indirectly by V_{INOK_Rise} and V_{INOK_HYST} settings		V_{INOK_Rise} - V_{INOK_HYST}		
V_{INLOW_Rise}	VINLOW rising threshold	Programmable value, defined in register Table 30. SW_VIN_CR	+30 +300	V_{INOK_Fall} +50 to V_{INOK_Fall} +400	+80 +500	mV
V_{INLOW_HYST}	VINLOW hysteresis	Programmable value, defined in register Table 30. SW_VIN_CR	90 180 270 360	100 200 300 400	110 220 330 440	mV
V_{INLOW_Fall}	VINLOW falling threshold	Defined indirectly by V_{INLOW_Rise} and V_{INLOW_HYST} settings		V_{INLOW_Rise} + V_{INLOW_HYST}		mV
T_{WRN_Rise}	Warning temperature rising		115	125	140	°C
T_{WRN_Fall}	Warning temperature falling		95	105	120	°C
T_{SHDN_Rise}	Shutdown temperature rising		140	150	160	°C
T_{SHDN_Fall}	Shutdown temperature falling		115	125	135	°C
t_{OCPDB_LDO}	LDO OCP turn-off delay			30		ms
t_{OCPDB_BUCK}	BUCK OCP turn-off delay			5		µs

chanhvinh.com

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{OVPDB_BST}	BOOST OVP turn-off delay				1		ms
t_{OCPDB_BST}	BOOST OCP turn-off delay				2		µs
t_{OCPDB_SW}	Switches OCP turn-off delay				30		ms
t_{WD}	Watchdog timer	Programmable value, defined in register Table 34. WDG_CR			1 to 256		s
		Timer programming step			1		
NVM_{END}	NVM write cycles endurance			1000			Cycle
LDO1, LDO2, LDO5							
V_{LDOIN} = 3.6 V, V_{IN} = 3.6 V, $V_{BUCK2IN}$ = 3.6 V, V_{LDOOUT} = 1.8 V, recommended BOM, T_j = -40 °C to +125 °C, unless otherwise specified,$V_{BUCK1IN}$ and $V_{BUCK2IN}$ must always be connected to V_{IN}							
V_{LDOIN}	Main input voltage range			2.8		5.5	V
V_{LDOOUT}	Output voltage	V_{LDOIN} >V_{LDOOUT} +$V_{LDODROP}$ Programmable value. Refer to Table 9. LDO output voltage settings	LDO1 LDO2		1.7 to 3.3		V
			LDO5		1.7 to 3.9		V
		Voltage programming step			100		mV
$V_{LDOOUT-ACC}$	Output voltage accuracy	V_{LDOIN} >V_{LDOOUT}+$V_{LDODROP}$ 1 mA<I_{LDOOUT}<350 mA		-2		2	%
I_{LDOOUT}	Continuous output current	V_{LDOIN} = 2.8 V to 5.5 V		350			mA
I_{LDOLIM}	Load current limitation	V_{LDOIN} = 2.8 V to 5.5 V		360	450	800	mA
I_{LDOQ}	Total quiescent current	I_{LDOOUT} = 0 mA, T_J = +105 °C total current from all LDO supply pins (VIN, LDOIN, BUCK2IN)			4	20	µA
I_{LDOIN_LKG}	Input leakage current	LDO OFF			0.5	2.5	µA
$V_{LDODROP}$	Dropout voltage (1)	V_{LDOOUT} = 2.8 V, I_{LDOOUT} = 350 mA			180	300	mV
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 5 to 180 mA, ΔV_{LDOIN} = 0, t_R = t_F ~1 µs			45		mV
$V_{LDOOUT-LI}$	Line transient regulation	V_{LDOIN} = 3.6 V to 3.0 V, $\Delta I_{LDO1OUT}$ = 0, t_R = t_F ~10 µs			10		mV
$PSRR_{LDO}$	Power supply rejection ratio	ΔV_{LDOIN} = 300 mVPP, f=[0.1:20] kHz			43		dB
		ΔV_{LDOIN} = 300 mVPP, f=[20:100] kHz			37		
t_{SSLDO}	Soft-start duration	2.8 V<V_{LDOIN}<5.5 V, 0<I_{LDOOUT}<1 mA C_{OUT}=4.7 µF			160		µs
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT}=1.8 V to V_{LDOOUT}=0.2 V, I_{LDOOUT}= no load				3	ms
LDO3 normal mode							
V_{LDO3IN} = 3.6 V, V_{IN} = 3.6 V, $V_{BUCK2IN}$ = 3.6 V, $V_{LDO3OUT}$ = 1.8 V, recommended BOM, T_j = -40 °C to +12 5 °C, unless otherwise specified							
V_{LDO3IN}	Main input voltage range			2.8		5.5	V

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{LDO3OUT}$	Output voltage	V_{LDO3IN} >$V_{LDO3OUT}$+$V_{LDO3DROP}$ programmable value. Refer to Table 9. LDO output voltage settings		1.8 to 3.3		V
		Voltage programming step		100		mV
$V_{LDO3OUT-ACC}$	Output voltage accuracy	V_{LDO3IN} >$V_{LDO3OUT}$+$V_{LDO3DROP}$ 1 mA<$I_{LDO3OUT}$<50 mA	-2		2	%
$I_{LDO3OUT}$	Continuous output current	V_{LDO3IN} = 2.8 V to 5.5 V	100			mA
$I_{LDO3LIM}$	Load current limitation	V_{LDO3IN} = 2.8 V to 5.5 V	120		150	mA
I_{QLDO3}	Total quiescent current	$I_{LDO3OUT}$ = 0 mA, T_J = +105 °C total current from all LDO supply pins (VIN, LDOIN, BUCK2IN)			20	µA
I_{LDO3IN_LKG}	Input leakage current	LDO OFF		1	3	µA
$V_{LDO3DROP}$	Dropout voltage	$V_{LDO3OUT}$ = 2.8 V, $I_{LDO3OUT}$ = 100 mA		120	200	mV
$V_{LDO3OUT-LO}$	Load transient regulation	$\Delta I_{LDO3OUT}$ = 5 mA to 55 mA, ΔV_{LDO3IN} = 0, t_R = t_F ~10 µs		30		mV
$V_{LDO3OUT-LI}$	Line transient regulation	V_{LDOIN} = 3.6 V to 3.0 V, $\Delta I_{LDO3OUT}$ = 0, t_R = t_F ~10 µs		5		mV
$PSRR_{LDO3}$	Power supply rejection ratio	ΔV_{LDO3IN} = 300 mVPP, f=[0.1:20] kHz		45		dB
		ΔV_{LDO3IN} = 300 mVPP, f=[20:100] kHz		40		
t_{SSLDO3}	Soft-start duration	2.8 V<V_{LDO3IN}<5.5 V, 0<$I_{LDO3OUT}$<1 mA		200		µs
t_{SDLDO3}	Shutdown duration (all modes)	Pull-down enabled, $V_{LDO3OUT}$=1.8 V to $V_{LDO3OUT}$ = 0.2 V, $I_{LDO3OUT}$ = no load, V_{IN}=3.6 V, C_{OUT}=4.7 µF			3	ms
LDO3 sink-source mode						
V_{LDO3IN} = V_{OUT2} = 1.35 V, V_{IN} = 5.0 V, $V_{BUCK2IN}$ = 5.0 V, $V_{LDO3OUT}$ = V_{REFDDR} = $V_{OUT2/2}$, T_j = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
$V_{LDO3IN-SS}$	Input voltage range		1.1	1.35	1.6	V
$I_{LDO3OUT-SS}$	Continuous output current				120	mA_{RMS}
$I_{LDO3LIM-SS}$	Overcurrent limit		±200			mA
I_{QLDO3_SS}	Total quiescent current	$I_{LDO3OUT}$ = 0 mA, T_J = +105 °C total current from all LDO supply pins (VIN, LDOIN, BUCK2IN)		2	20	µA
$V_{LDO3OUT-LO-SS}$	Load transient regulation	$\Delta I_{LDO3OUT}$ = +/- [0:50] mA, ΔV_{LDO3IN} = 0, t_R = t_F ~250 ns		30		mV
$V_{LDO3OUT-LI-SS}$	Line transient regulation	V_{LDO3IN} = V_{OUT2} = 1.35 V, $\Delta I_{LDO3OUT}$ = 0, t_R = t_F ~1 µs		5		mV
$t_{SSLDO3-SS}$	Soft-start duration	2.8 V <V_{LDO3IN} <5.5 V, 0< $I_{LDO3OUT}$ < 1 mA		21	40	µs
$t_{SDLDO3-SS}$	*Shutdown duration*	Pull-down enabled, $V_{LDO3OUT}$= $V_{OUT2/2}$ to $V_{LDO3OUT}$ < 0.2 V, $I_{LDO3OUT}$ = no load, V_{IN} = V_{OUT2}, C_{OUT}=4.7 µF			3	ms
LDO3 bypass mode						
V_{LDO3IN} = 1.8 V, $V_{LDO3OUT}$ = ~1.8 V, T_j = -40 °C to +125 °C, recommended BOM, unless otherwise specified						

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{LDO3IN-BP}$	Input voltage range		1.7		2	V
$I_{LDO3OUT-BP}$	Continuous output current	1.7 V<V_{LDO3IN}<2 V no overcurrent protection in bypass mode	50			mA
$R_{DSONLDO3-BP}$	Bypass transistor $R_{DS(on)}$	$I_{LDO3OUT}$=40 mA,T_j = 25 °C		0.45	0.6	Ω
$t_{SSLDO3-BP}$	Soft-start duration	1.7 V < V_{LDO3IN} < 2 V, 0 < $I_{LDO3OUT}$ < 1 mA		100		µs
$t_{SDLDO3-BP}$	Shutdown duration	Pull-down enabled, $V_{LDO3OUT}$=1.8 V to $V_{LDO3OUT}$ = 0.2 V, $I_{LDO3OUT}$ = no load, V_{IN}=3.6 V, C_{OUT}=4.7 µF			3	ms
LDO4						
VLDO4OUT = 3.3 V, T_j = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
V_{LDO4IN}	Input voltage range	V_{LDO4IN} = Max.(VIN; VBUSOTG; BSTOUT)	2.8(2)		5.5	V
$V_{LDO4OUT-ACC}$	Output voltage accuracy	3.6 V<V_{LDO4IN}<5.5 V, 1 mA<$I_{LDO4OUT}$<30 mA	3.23	3.3	3.34	V
$I_{LDO4OUT}$	Continuous output current	V_{LDO4IN} = 3.6 V to 5.5 V	50			mA
$I_{LDO4LIM}$	Load current limitation	V_{LDO4IN} = 3.6 V to 5.5 V	50	75	200	mA
I_{LDO4Q}	Quiescent current	$I_{LDO4OUT}$ = 0 mA, T_J = +105 °C		20	25	µA
$V_{LDO4DROP}$	Dropout voltage from VIN	$I_{LDO4OUT}$ = 30 mA		45	90	mV
$V_{LDO4OUT-LO}$	Load transient regulation VIN	$\Delta I_{LDO4OUT}$ = 1 to 30 mA, ΔV_{LDO4IN} = 0, t_R = t_F ~1 µs		40		mV
$V_{LDO4OUT-LI}$	Line transient regulation VIN	ΔV_{LDO4IN} = 600 mV, $\Delta I_{LDO4OUT}$ = 0, t_R = t_F ~10 µs		10		mV
$PSRR_{LDO4}$	Power supply rejection ratio	ΔV_{LDO4IN} = 300 mVPP, f=[0.1:10] kHz		40		dB
t_{SSLDO4}	Soft-start duration	3.5 V<V_{LDO4IN}<5.5 V, 0<$I_{LDO4OUT}$<1 mA		100		µs
t_{SDLDO4}	Shutdown duration	Pull-down enabled, $V_{LDO4OUT}$=3.3 V to $V_{LDO4OUT}$<0.2 V, $I_{LDO4OUT}$ = no load, V_{IN}=3.6 V, C_{OUT}=4.7 µF			3	ms
LDO6						
V_{LDO6IN} =3.6 V, $V_{LDO6OUT}$ = 1.0 V, T_j = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
V_{IN}	Main input voltage range	V_{LDO6IN}	2.8		5.5	V
$V_{LDO6OUT}$	Output voltage	V_{LDO6IN} >$V_{LDO6OUT}$ +$V_{LDO6DROP}$ Programmable value. Refer to Table 9. LDO output voltage settings		0.9 to 3.3		V
		Voltage programming step		100		mV
$V_{LDO6OUT-ACC}$	Output voltage accuracy	V_{LDO6IN} >$V_{LDO6OUT}$ +$V_{LDO6DROP}$, 0<$I_{LDO6OUT}$<150 mA	-2		2	%
$I_{LDO6OUT}$	Continuous output current	2.8 V<V_{LDO6IN}<5.5 V	150			mA
$I_{LDO6LIM}$	Load current limitation	2.8 V<V_{LDO6IN}<5.5 V	160	200	350	mA
I_{LDO6Q}	Quiescent current	$I_{LDO6OUT}$ = 0 mA, T_J = +105 °C		4	20	µA

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LDO6IN_LKG}	Input leakage current	LDO OFF		0.5	1	µA
$V_{LDO6DROP}$	Dropout voltage	$V_{LDO6OUT}$ = 2.9 V, $I_{LDO6OUT}$=150 mA		160	300	mV
$V_{LDO6OUT-LO}$	Load transient regulation	$\Delta I_{LDO6OUT}$ = 75 mA, ΔV_{LDO6IN} = 0, t_R = t_F ~1 µs		30		mV
$V_{LDO6OUT-LI}$	Line transient regulation	ΔV_{LDO6IN} = 600 mV, $\Delta I_{LDO6OUT}$ = 0, t_R = t_F ~10 µs		5		mV
$PSRR_{LDO6}$	Power supply rejection ratio	ΔV_{LDO6IN} = 300 mVPP, f=[0.1:20] kHz		55		dB
		ΔV_{LDO6IN} = 300 mVPP, f=[20:100] kHz		40		
t_{SSLDO6}	Soft-start duration	2.8 V<V_{LDO6IN}<5.5 V, 0<$I_{LDO6OUT}$<1 mA		100		µs
t_{SDLDO6}	Shutdown duration	PD on, $V_{LDO6OUT}$=1.8 V to $V_{LDO6OUT}$<0.2 V, $I_{LDO6OUT}$<1 mA, V_{IN}=3.6 V, C_{OUT}=4.7 µF			3	ms
REFDDR						
V_{REFOUT}= $V_{OUT2/2}$= 0.675 V, T_j = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
V_{REFOUT}	Output voltage	0.1 mA<I_{REFOUT}<5 mA		V_{OUT2}/2		V
$V_{REF-ACC}$	Output voltage accuracy	I_{REF} = 0.1 mA	-1		1	%
I_{REFOUT}	Output current capability		5			mA_{RMS}
I_{REFLIM}	Load current limitation		±10	±25	±50	mA
I_{REFQ}	Quiescent current	I_{REFOUT} = 0 mA, T_J = +25 °C		30		µA
t_{SSREF}	Soft-start duration	0.1 mA<I_{REF}<1 mA		100		µs
t_{SDREF}	Shutdown duration	PD on, V_{REFOUT}=0.6 V to V_{REFOUT}<0.2 V, I_{REFOUT}<0.1 mA, V_{IN}=3.6 V, C_{OUT}=1 µF			3	ms
Buck converter 1						
$V_{BUCK1IN}$ = 3.6 V, V_{OUT1} = 1.2 V, recommended BOM, T_j= -40 °C to +125 °C , unless otherwise specified						
$V_{BUCK1IN}$	Main input voltage range		2.8		5.5	V
V_{OUT1}	Output voltage	Programmable value, refer to Table 10. BUCK output settings		0.725 to 1.5		V
		Voltage programming step		25		mV
$V_{OUT1-ACC}$	Output voltage accuracy	$V_{BUCK1IN}$= 2.8 V to 5.5 V, V_{OUT1} = 0.725 V to 1.5 V				%
		HP mode I_{BK1OUT} = 0 to 1.5 A	-2		2	
		LP mode I_{BK1OUT} = 0 to 50 mA	-4		4	
$V_{OUT1-RIPP}$	Output voltage ripple	I_{BK1OUT} = 0 mA, HP mode, T_A = +25 °C		10		mV
		I_{BK1OUT} = 1500 mA, HP mode, T_A = +25 °C		5		
I_{OUT1}	Continuous output current	2.8<$V_{BUCK1IN}$<5.5 V, HP mode	1500			mA
		2.8< $V_{BUCK1IN}$<5.5 V, LP mode	50			
$I_{OUT1_LP_PEAK}$	Peak output current in LP mode	2.8< $V_{BUCK1IN}$<5.5 V, t_{PEAK} < 10 us	200			
I_{BK1LIM}	Inductor peak current limit			2		A

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{REFCLK}	Reference switching frequency			2		MHz
I_{Q_BK1}	Total quiescent current	$I_{BUCK1OUT}$ = 0 mA, HP mode		220	300	µA
		$I_{BUCK1OUT}$ = 0 mA, LP mode		50	80	
$I_{BUCK1IN_LKG}$	Input leakage current	BUCK OFF			1	µA
EFF_{BK1}	Efficiency	I_{BK1OUT}=150 mA, T_A = +25 °C		86		%
		I_{BK1OUT}=750 mA,T_A = +25 °C		83		
		I_{BK1OUT}=1500 mA,T_A = +25 °C		70		
$V_{OUT1-LO}$	Load transient regulation	HP mode; 0<I_{BK1OUT}<1.5 A, ΔI_{BK1OUT} = 450 mA, t_R = t_F ~250 ns		15	30	mV
		LP mode; 0<I_{BK1OUT}<50 mA, ΔI_{BK1OUT} = 50 mA t_R = t_F ~250 ns			5	
$V_{OUT1-LI}$	Line transient regulation	ΔV_{BK1IN} = 600 mV, ΔI_{BK1OUT} = 0, t_R = t_F ~10 µs, HP mode		1.5	5	mV
$V_{OUT1-OVR}$	Power-up overshoot	2.8 V<V_{BK1IN}<5.5 V, I_{BK1OUT}~1 mA, T_A = +25 °C, 0.725 V<V_{OUT1}<1.5 V			40	mV
$t_{LP-HP-BK1}$	Recovery time from LP to HP mode	V_{OUT1_LP} = VOUT1_HP			20	µs
t_{SU_BK1}	Start-up delay (delay before voltage starts to rise)	2.8 V<$V_{BUCK1IN}$<5.5 V, refer toFigure 46. BUCKx start-up/shutdown timings	0.05	0.5	1	ms
t_{SS_BK1}	Soft-start duration	2.8 V<$V_{BUCK1IN}$<5.5 V, 1 mA<I_{BK1OUT}<100 mA, V_{OUT1}=1.2 V, refer to Figure 16. Buck4 load transient in LP mode.		235	400	µs
S_{RBK1}	Output voltage slew rate	Slew rate during start-up		5.5		mV/µs
		DVS slew rate of a voltage programmed change low to high or high to low, from 0.8 V to 1.2 V	2.3	3.1		mV/µs
t_{SD_BK1}	Shutdown duration	From V_{OUT1}=1.2 V to V_{OUT1}<0.2 V, V_{IN}=3.6 V, C_{OUT}=22 µF				ms
		Slow PD, I_{BK1OUT}<1 mA			1.5	
		Fast PD, I_{BK1OUT}<1 mA			0.15	
Buck converter 2						
$V_{BUCK2IN}$ = 3.6 V, V_{OUT2} = 1.2 V, recommended BOM, T_j = -40 °C to +125 °C, unless otherwise specified						
$V_{BUCK2IN}$	Main input voltage range		2.8		5.5	V
V_{OUT2}	Output voltage	Programmable value, refer to Table 10. BUCK output settings		1.0 to 1.5		V
		Voltage programming step		50		mV
$V_{OUT2-ACC}$	Output voltage accuracy	$V_{BUCK2IN}$ = 2.8 V to 5.5 V, V_{OUT2} = 1.0 V to 1.5 V				%
		HP mode I_{BK2OUT} = 0 to 1.0 A	-2		2	

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OUT2-ACC}$	Output voltage accuracy	LP mode I_{BK2OUT} = 0 to 50 mA	-4		4	%
$V_{OUT2-RIPP}$	Output voltage ripple	I_{BK2OUT} = 0 mA, HP mode, T_A = +25 °C		10		mV
		I_{BK2OUT} = 1000 mA, HP mode, T_A = +25 °C		5		
I_{OUT2}	Continuous output current	2.8<$V_{BUCK2IN}$<5.5 V, HP mode	1000			mA
		2.8< $V_{BUCK2IN}$<5.5 V, LP mode	50			
$I_{OUT2_LP_PEAK}$	Peak output current in LP mode	2.8< $V_{BUCK2IN}$<5.5 V, LP mode, t_{PEAK} < 10 us	200			
I_{BK2LIM}	Inductor peak current limit			1.6		A
f_{REFCLK}	Reference switching frequency			2		MHz
I_{Q_BK2}	Total quiescent current	$I_{BUCK2OUT}$ = 0 mA, HP mode		220	300	µA
		$I_{BUCK2OUT}$ = 0 mA, LP mode		50	80	
$I_{BUCK2IN_LKG}$	Input leakage current	BUCK OFF			1	µA
EFF_{BK2}	Efficiency	I_{BK2OUT}=150 mA, T_A = +25 °C		87		%
		I_{BK2OUT}=750 mA, T_A = +25 °C		86		
		I_{BK2OUT}=1000 mA, T_A = +25 °C		84		
$V_{OUT2-LO}$	Load transient regulation	HP mode; 0<I_{BK2OUT}<1.0 A, ΔI_{BK2OUT} = 450 mA, t_R = t_F ~250 ns		15	30	mV
		LP mode; 0<I_{BK2OUT}<50 mA ΔI_{BK2OUT} = 50 mA, t_R = t_F ~250 ns			5	
$V_{OUT2-LI}$	Line transient regulation	ΔV_{BK2IN} = 600 mV, ΔI_{BK2OUT} = 0, t_R = t_F ~10 µs, HP mode		1.5	5	mV
$V_{OUT2-OVR}$	Power-up overshoot	2.8 V<V_{BK2IN}<5.5 V, I_{BK2OUT}~1 mA, T_A = +25 °C, 0.725 V<V_{OUT2}<1.5 V			40	mV
$t_{LP-HP-BK2}$	Recovery time from LP to HP mode	V_{OUT2_LP} = V_{OUT2_HP}			20	µs
t_{SU_BK2}	Start-up delay (delay before voltage starts to rise)	2.8 V<$V_{BUCK2IN}$<5.5 V, refer to Figure 46. BUCKx start-up/shutdown timings.	0.05	0.5	1	ms
t_{SS_BK2}	Soft-start duration	2.8 V<$V_{BUCK2IN}$<5.5 V, 1 mA<I_{BK2OUT}<100 mA, V_{OUT2}=1.2 V, refer to Figure 16. Buck4 load transient in LP mode		235	400	µs
S_{RBK2}	Output voltage slew rate	Slew rate during start-up		5.5		mV/µs
		DVS slew rate of a voltage programmed change low to high or high to low		3.1		mV/µs
t_{SD_BK2}	Shutdown duration	From V_{OUT2} = 1.2 V to V_{OUT2}<0.2 V, V_{IN}=3.6 V, C_{OUT}=22 µF				ms
		Slow PD, I_{BK2OUT}<1 mA			1.5	
		Fast PD, I_{BK2OUT}<1 mA			0.15	
Buck converter 3						

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BUCK3IN}$ = 3.6 V, V_{OUT3} = 1.8 V, recommended BOM, T_j = -40 °C to +125 °C, unless otherwise specified						
$V_{BUCK3IN}$	Main input voltage range		2.8[2]		5.5	V
V_{OUT3}	Output voltage	Programmable value, refer to Table 10. BUCK output settings		1.0 to 3.4		V
		Voltage programming step		100		mV
$V_{OUT3-ACC}$	Output voltage accuracy	$V_{BUCK3IN}$ = 2.8 V to 5.5 V				%
		HP mode I_{BK3OUT} = 0 to 500 mA, V_{OUT3} = 1.8 V to 3.3 V	-2.5		2.5	
		HP mode I_{BK3OUT} = 0 to 500 mA, V_{OUT3} = 1.0 V to 3.4 V	-3		3	
		LP mode I_{BK3OUT} = 0 to 50 mA, V_{OUT3} = 1.0 V to 3.4 V	-4		4	
$V_{OUT3-RIPP}$	Output voltage ripple	I_{BK3OUT} = 0 mA, HP mode, T_A = +25 °C		10		mV
		I_{BK3OUT} = 500 mA, HP mode, T_A = +25 °C		5		
I_{OUT3}	Continuous output current	2.8<$V_{BUCK3IN}$<5.5 V, HP mode	500			mA
		2.8< $V_{BUCK3IN}$<5.5 V, LP mode	50			
$I_{OUT3_LP_PEAK}$	Peak output current in LP mode	2.8< $V_{BUCK3IN}$<5.5 V, LP mode, t_{PEAK} < 10 µs	200			
I_{BK3LIM}	Inductor peak current limit			1		A
f_{REFCLK}	Reference switching frequency			2		MHz
I_{Q_BK3}	Total quiescent current	$I_{BUCK3OUT}$ = 0 mA, HP mode		220	300	µA
		$I_{BUCK3OUT}$ = 0 mA, LP mode		50	80	
$I_{BUCK3IN_LKG}$	Input leakage current	BUCK OFF			1	µA
EFF_{BK3}	Efficiency	I_{BK3OUT}=150 mA, T_A = +25 °C		90		%
		I_{BK3OUT}=350 mA,T_A = +25 °C		88		
		I_{BK3OUT}=500 mA,T_A = +2 5°C		91		
$V_{OUT3-LO}$	Load transient regulation	HP mode; 0<I_{BK3OUT}<0.5 A, ΔI_{BK3OUT} = 100 mA, t_R = t_F ~250 ns		15	30	mV
		LP mode; 0<I_{BK3OUT}<50 mA $\Delta_{IBK3OUT}$ = 50 mA, t_R = t_F ~250 ns			5	
$V_{OUT3-LI}$	Line transient regulation	Δ_{VBK3IN} = 600 mV, $\Delta_{IBK3OUT}$ = 0, t_R = t_F ~10 µs, HP mode		1.5	5	mV
$V_{OUT3-OVR}$	Power-up overshoot	2.8 V<V_{BK3IN}<5.5 V, I_{BK3OUT}~1 mA, T_A = +25 °C, 0.725 V<V_{OUT3}<1.5 V			40	mV
$t_{LP-HP-BK3}$	Recovery time from LP to HP mode	V_{OUT3_LP} = V_{OUT3_HP}			20	µs

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SU_BK3}	Start-up delay (delay before voltage starts to rise)	2.8 V<$V_{BUCK3IN}$<5.5 V, refer to Figure 46. BUCKx start-up/shutdown timings.	0.05	0.5	1	ms
t_{SS_BK3}	Soft-start duration	2.8 V<$V_{BUCK3IN}$<5.5 V, 1 mA<I_{BK3OUT}<100 mA, V_{OUT3}=1.2 V, refer to Figure 16. Buck4 load transient in LP mode		235	400	µs
S_{RBK3}	Output voltage slew rate	Slew rate during start-up		5.5		mV/µs
		DVS slew rate of a voltage programmed change low to high or high to low		3.1		mV/µs
t_{SD_BK3}	Shutdown duration	From V_{OUT3} = 1.2 V to V_{OUT3}<0.2 V, V_{IN}=3.6 V, C_{OUT}=22 µF				ms
		Slow PD, I_{BK3OUT}<1 mA			1.5	
		Fast PD, I_{BK3OUT}<1 mA			0.15	
Buck converter 4						
$V_{BUCK4IN}$ = 5.0 V, V_{OUT4} = 3.3 V, recommended BOM, T_j = -40 °C to +125 °C, unless otherwise specified						
$V_{BUCK4IN}$	Main input voltage range		2.8 (2)		5.5	V
V_{OUT4}	Output voltage	Programmable value, refer to Table 10. BUCK output settings		0.6 to 3.9		V
		Voltage programming step				
		0.6 V ≤ V_{BK4OUT}<1.3 V		25		mV
		1.3 V≤ V_{BK4OUT}<1.5 V		50		
		1.5 V ≤ V_{BK4OUT}<3.9 V		100		
$V_{OUT4-ACC}$	Output voltage accuracy	$V_{BUCK4IN}$ = 2.8 V to 5.5 V				%
		HP mode I_{BK4OUT} = 0 to 2.0 A, V_{OUT4} = 0.8 V to 1.4 V	-2.5		2.5	
		HP mode I_{BK4OUT} = 0 to 2.0 A, V_{OUT4} = 0.6 V to 3.9 V	-3.5		3.5	
		LP mode I_{BK4OUT} = 0 to 50 mA, V_{OUT4} = 0.6 V to 3.9 V	-4		4	
$V_{OUT4-RIPP}$	Output voltage ripple	I_{BK4OUT} = 0 mA, HP mode, T_A = +25 °C		10		mV
		I_{BK4OUT} = 2000 mA, HP mode, T_A = +25 °C		10		
I_{OUT4}	Continuous output current	2.8<$V_{BUCK4IN}$<5.5 V, HP mode	2000			mA
		2.8< $V_{BUCK4IN}$<5.5V, LP Mode	50			
$I_{OUT4_LP_PEAK}$	Peak output current in LP mode	2.8< $V_{BUCK4IN}$<5.5 V, LP mode, t_{PEAK} < 10 µs	200			
I_{BK4LIM}	Inductor peak current limit			3		A
f_{REFCLK}	Reference switching frequency			2		MHz
I_{Q_BK4}	Total quiescent current	$I_{BUCK4OUT}$ = 0 mA, HP mode		220	300	µA
		$I_{BUCK4OUT}$ = 0mA, LP mode		50	80	

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{BUCK4IN_LKG}$	Input leakage current	BUCK OFF			1	µA
EFF_{BK4}	Efficiency	I_{BK4OUT}=250 mA, T_A = +25 °C		90		%
		I_{BK4OUT}=1300 mA,T_A = +25 °C		85		
		I_{BK4OUT}=2000 mA,T_A = +25 °C		79		
$V_{OUT4-LO}$	Load transient regulation	HP mode; 0<I_{BK4OUT}<2.0 A, ΔI_{BK4OUT} = 500 mA, t_R = t_F ~250 ns		15	30	mV
		LP mode; 0<I_{BK4OUT}<50 mA ΔI_{BK4OUT} = 50 mA, tR = tF ~250 ns			5	
$V_{OUT4-LI}$	Line transient regulation	Δ_{VBK4IN} = 600 mV, $\Delta_{IBK4OUT}$ = 0, t_R = t_F ~10 µs, HP mode		1.5	5	mV
$V_{OUT4-OVR}$	Power-up overshoot	2.8 V<V_{BK4IN}<5.5 V, I_{BK4OUT}~1 mA, T_A = +25 °C, 0.725 V<V_{OUT4}<1.5 V			40	mV
$t_{LP-HP-BK4}$	Recovery time from LP to HP mode	V_{OUT4_LP} = V_{OUT4_HP}			20	µs
t_{SU_BK4}	Startup delay (delay before voltage starts to rise)	2.8 V<$V_{BUCK4IN}$<5.5 V, refer to Figure 16. Buck4 load transient in LP mode.	0.05	0.5	1	ms
t_{SS_BK4}	Soft-start duration	2.8 V<$V_{BUCK4IN}$<5.5 V, 1 mA<I_{BK4OUT}<100 mA, V_{OUT4} = 1.2 V, refer to Figure 46. BUCKx start-up/shutdown timings		235	400	µs
SR_{BK4}	Output voltage slew rate	Slew rate during start-up		5.5		mV/µs
		DVS slew rate of a voltage programmed change low to high or high to low, from 0.8 V to 1.2 V	1.9	3.1		mV/µs
t_{SD_BK4}	Shutdown duration	From V_{OUT4} = 1.2 V to V_{OUT4}<0.2 V, V_{IN}=3.6 V, C_{OUT} = 22 µF				ms
		Slow PD, I_{BK4OUT}<1 mA			1.5	
		Fast PD, I_{BK4OUT}<1 mA			0.15	
Boost converter						
V_{IN} = 3.6 V, V_{BSTOUT} = 5.2 V, T_A = 25 °C, T_j = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
V_{IN}	Main input voltage range		2.8		5.5	V
V_{OUT}	Output voltage range	2.8 V<V_{BSTOUT}<5.2 V, boost mode		5.2		V
		5.2 V<V_{BSTOUT}<5.5 V, bypass mode		~VBOOSTIN		
$V_{BST-ACC}$	Output voltage accuracy	2.8 V<V_{BSTIN}<3.3 V, 0<I_{BSTOUT}<0.5 A or 3.3 V<V_{BSTIN}<5.5 V, 0<I_{BSTOUT}<1.1 A	-3.5		3.5	%
V_{BSTOVP}	Overvoltage threshold		5.5	5.7	5.85	V
I_{BSTOUT_HI}	Continuous output current	3.3 V<V_{BSTIN}<5.5 V	1.1			A
I_{BSTOUT_LO}	Continuous output current	2.8 V<V_{BSTIN}<3.3 V	0.5			A
I_{BSTOUT_LKG}	Output leakage current	B_{STOUT}, boost OFF, pull-down disabled			1	µA

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{BSTLIM}	Inductor peak current limit LS			3.3		A
I_{BSTSH}	Short-circuit threshold HS			4		A
I_Q	Quiescent current	I_{BSTOUT}=0 mA		600	900	µA
EFF_{BST}	Efficiency	I_{BSTOUT}=2.5 mA, T_A = 25 °C		76		%
		I_{BSTOUT}=100 mA, T_A = 25 °C		89		
		I_{BSTOUT}=500 mA, T_A = 25 °C		89		
		I_{BSTOUT}=1100 mA, T_A = 25 °C		82		
V_{BST-LO}	Load transient regulation	I_{BSTOUT}= 0 A to 0.5 A, Δ_{VIN} = 0, t_R = t_F ~5 µs V_{IN}={3.6 V;5 V}			300	mV
		I_{BSTOUT}= 0.5 A to 1.0 A, ΔVIN = 0, t_R = t_F ~5 µs VIN={3.6 V;5 V}		130	200	
V_{BST-LI}	Line transient regulation	Δ_{VIN} = 5 V+/-250 mV, I_{BSTOUT} = 500 mA, t_R = t_F ~1 µs		40		mV
$V_{BST-OVR}$	Power-up overshoot	3.0 V<V_{BSTIN}<5.2 V, I_{BSTOUT}=0 mA			300	mV
I_{PRECH_BST}	Precharge current			220		mA
t_{PRECH_BST}	Maximum precharge duration	I_{BSTOUT}=0 mA		1		ms
t_{SS_BST}	Soft-start duration	I_{BSTOUT}=0 mA		500		µs
$R_{DSON-BYP}$	Bypass switch ON-resistance	I_{BSTOUT}=300 mA, V_{IN} = 5.3 V		115		mΩ
PWR_USB_SW switch						
VBSTOUT=5.2 V, T_j = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
$R_{DSON-VBUSOTG}$	Switch ON-resistance	$I_{VBUSOTG}$=300 mA		145	250	mΩ
$I_{VBUSOTG}$	Continuous output current		0.5			mA
$I_{VBUSOTGOCP}$	Overcurrent limit		0.55			A
$I_{VBUSOTG_SH}$	Short-circuit threshold			1.1		A
$t_{SS_VBUSOTG}$	Soft-on/off duration			3		ms
$t_{VBUSOTGDB}$	V_{BUSOTG} det. debounce time			30		ms
$V_{VBUSOTG_Rise}$	V_{BUSOTG} rise threshold		3.6	3.8	4.0	V
$V_{VBUSOTG_Fall}$	V_{BUSOTG} fall threshold		2.0	2.2	2.4	V
PWR_SW switch						
VSWIN = 5.2 V, T_j = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
$R_{DSON-SWOUT}$	Switch ON-resistance	I_{SWOUT}=300 mA		100	200	mΩ
I_{SWOUT}	Continuous output current		1			A

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SWOUTOCP}$	Overcurrent limit	OCP_SWOUT_LIM = 0	0.6			A
		OCP_SWOUT_LIM = 1	1.1			A
I_{SWOUT_SH}	Short-circuit threshold			1.1		A
t_{SS_SWOUT}	Soft-on/off duration			3		ms
V_{SWOUT_Rise}	SWOUT rise threshold		40	50	60	% VIN
V_{SWOUT_Fall}	SWOUT fall threshold		30	40	50	% VIN
$t_{SWOUTDB}$	SWOUT det. debounce time			30		ms
V_{SWIN_Rise}	SWIN rise threshold		2.75	2.92	3.00	V
V_{SWIN_Fall}	SWIN fall threshold		2.5	2.65	2.8	V
t_{SWINDB}	SWIN det. debounce time			30		ms
$t_{OCPDBSW}$	SWIN OCP debounce time			2		µs
Digital interface						
V_{IO}	VIO input voltage for IO signal		1.7	1.8	3.6	V
V_{IL}	PONKEYn input low voltage	internal VIN pull-up on pin	0		0.3x VIN	V
	WAKEUP input low voltage	internal VIO pull-down on pin	0.3	0.8		
	PWRCTRL input low voltage	internal VIO pull-up on pin	0		0.3x VIO	
		internal VIO pull-down on pin	0		0.3x VIO	
	RSTn input low voltage	internal VIO pull-up on pin	0		0.3x VIO	
	SDA, SCL input low voltage	I^2C NXP UM10204 revision 5 compliant (October 2012)				
V_{IH}	PONKEYn input high voltage	internal VIN pull-up on pin	0.7 x VIN		VIN	V
	WAKEUP input high voltage	Internal VIO pull-down on pin		1	1.2	
	PWRCTRL input high voltage	Internal VIO pull-up pin	0.7 x VIO		VIO	
		Internal VIO pull-down pin	0.7 x VIO		VIO	
	RSTn input high voltage	Internal VIO pull-up on pin	0.7 x VIO		VIO	
	SDA, SCL input high voltage	I^2C NXP UM10204 revision 5 compliant (October 2012)				
V_{OL}	INTn output low voltage	80 kΩ internal VIO pull-up on pin	0		0.3 x VIO	V
	SDA, SCL output low voltage	I^2C NXP UM10204 revision 5 compliant (October 2012)				

chanhvinh.com

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	INTn output high voltage	80 kΩ internal VIO pull-up on pin		VIO		V
	SDA, SCL output high voltage	I²C NXP UM10204 revision 5 compliant (October 2012)				
R_{PD}	WAKEUP pin pull-down resistor	Internally connected to GND	45	60	80	kΩ
	PWRCTRL pin pull-down resistor	Internally connected to GND	60	90	140	
R_{PU}	PONKEYn pin pull-up resistor	Internally connected to V_{IN}	90	120	140	
	PWRCTRL pin pull-up resistor	Internally connected to V_{io}	50	80	120	
	RSTn pin pull-up resistor	Internally connected to V_{io}	50	80	120	
	INTn pin pull-up resistor	Internally connected to V_{io}	50	80	120	
$PONKEYn_{DB}$	PONKEYn debounce time			30		ms
$WAKEUP_{DB}$	WAKEUP debounce time			2		µs
$RSTn_{DB}$	RSTn assertion time		20			µs

1. *Dropout is the smallest difference between a regulator's input and its output voltage, which is required to maintain regulation and enable the regulator to provide rated voltage and current*
2. *V_{IN} is intended to be higher than VOUT*

chanhvinh.com

3.5 Application board curves

Unless otherwise specified, all typical curves are given as design guidelines.

Figure 3. BUCK1 efficiency

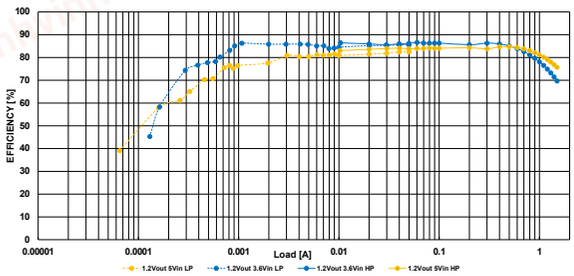


Figure 4. BUCK2 efficiency

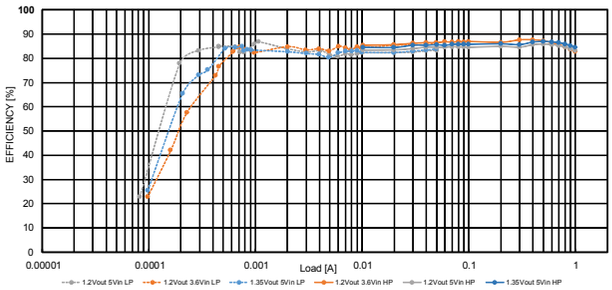


Figure 5. BUCK3 efficiency

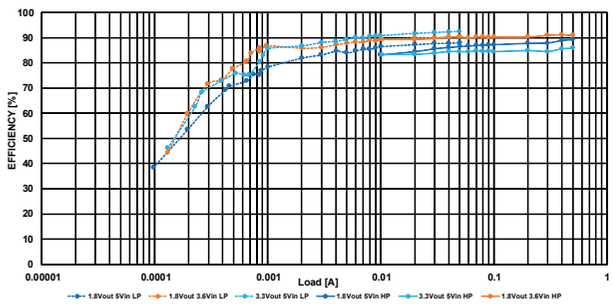


Figure 6. BUCK4 efficiency

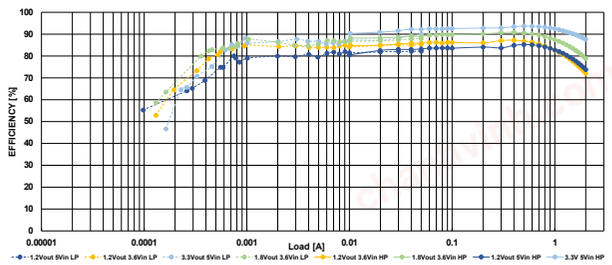


Figure 7. Boost efficiency

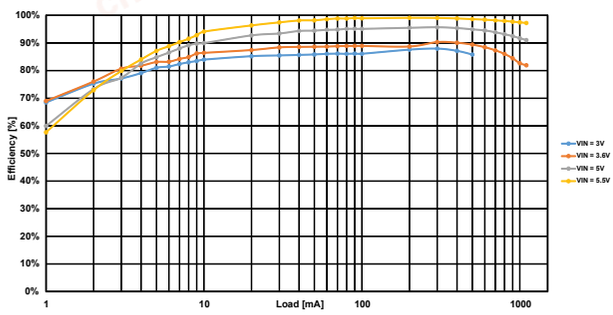
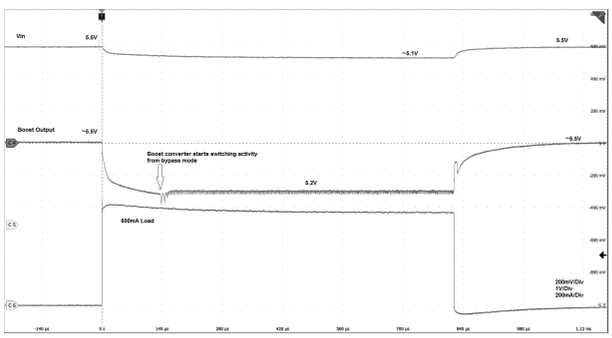


Figure 8. Boost powered by 5 V supply having poor performance



chanhvinh.com

Figure 9. **BUCK1 load transient in HP mode**

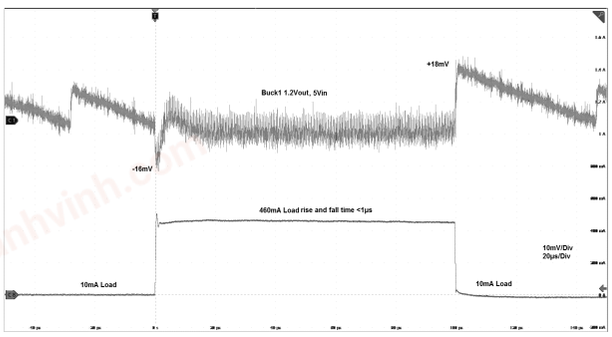


Figure 10. **Buck1 load transient in LP mode**

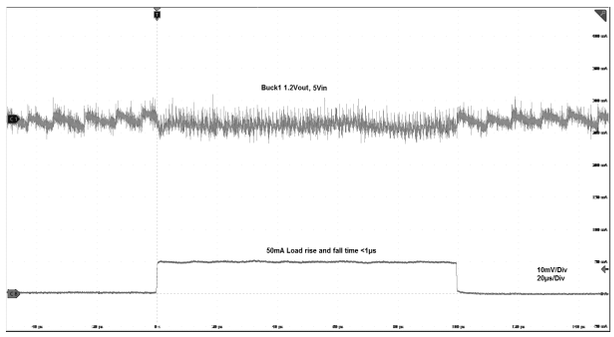


Figure 11. **BUCK2 load transient in HP mode**

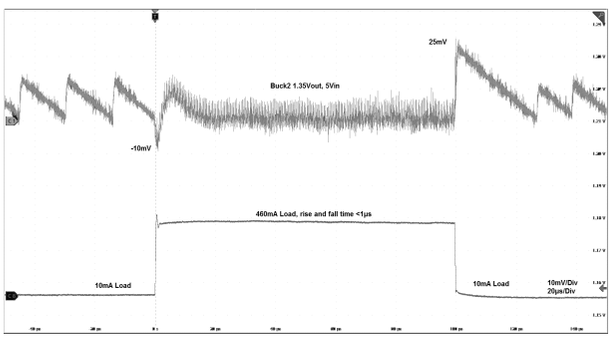


Figure 12. **Buck2 load transient in LP mode**

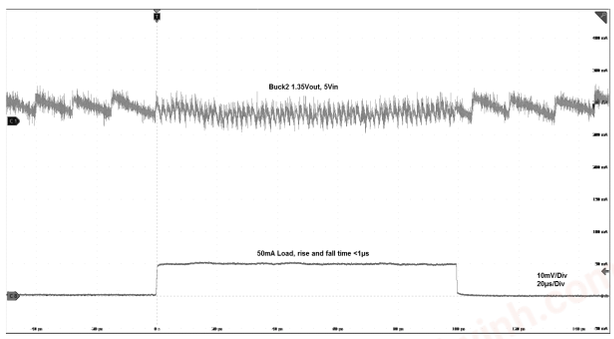


Figure 13. **Buck3 load transient in HP mode**

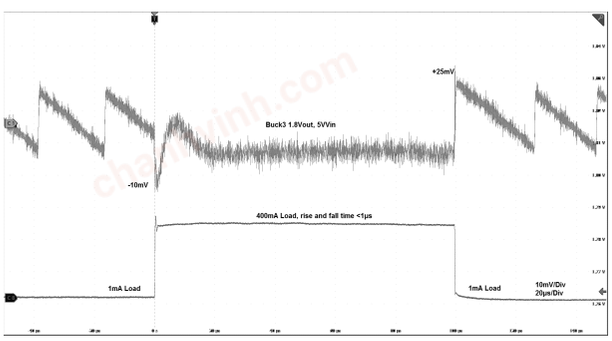


Figure 14. **Buck3 load transient in LP mode**

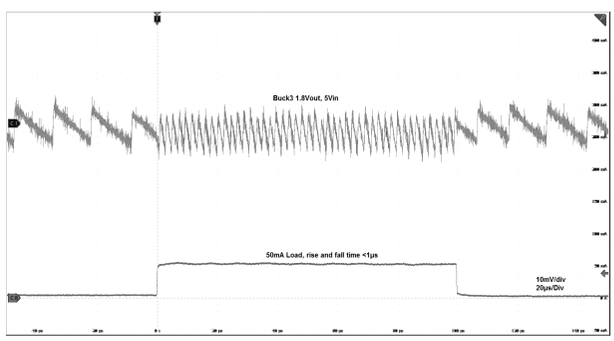


Figure 15. **Buck4 load transient in HP mode**

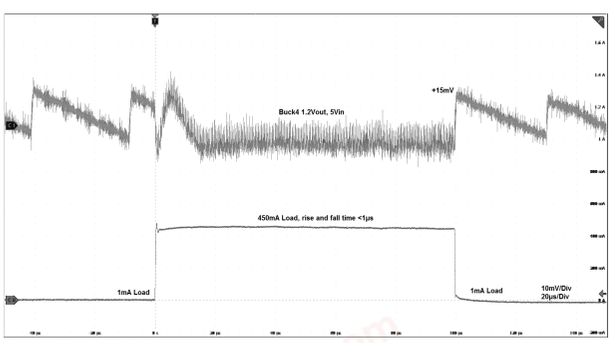
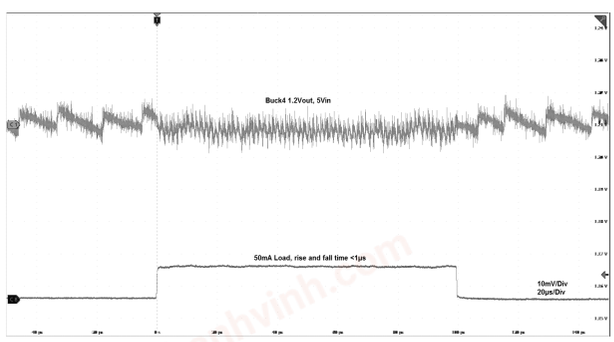


Figure 16. **Buck4 load transient in LP mode**



chanhvinh.com

Figure 17. LDO1 load transient

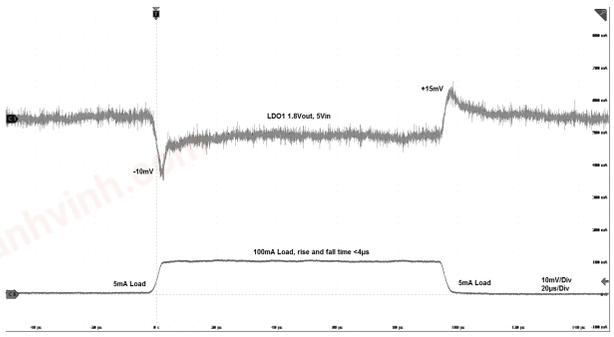


Figure 18. LDO2 load transient

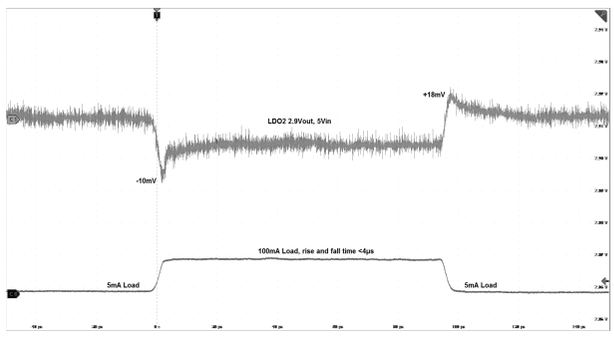


Figure 19. LDO3 load transient

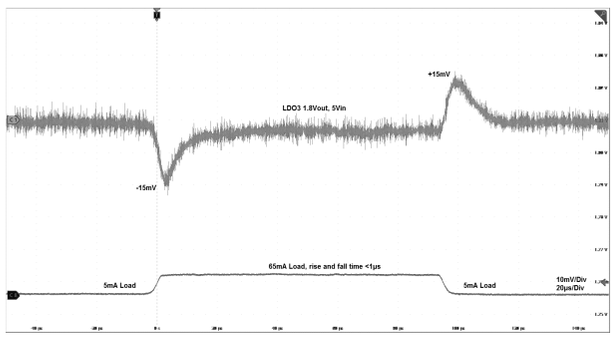


Figure 20. LDO4 load transient

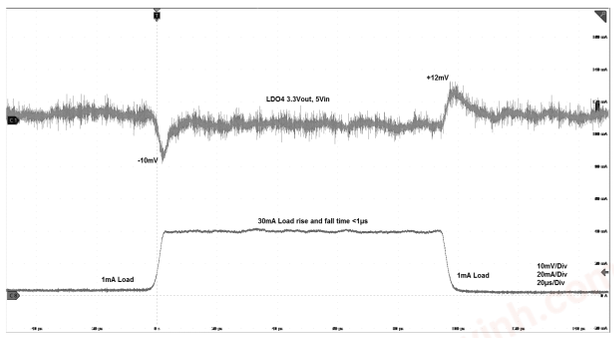


Figure 21. LDO5 load transient

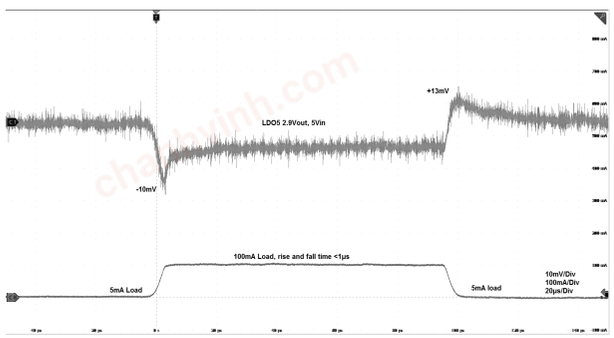


Figure 22. LDO6 load transient

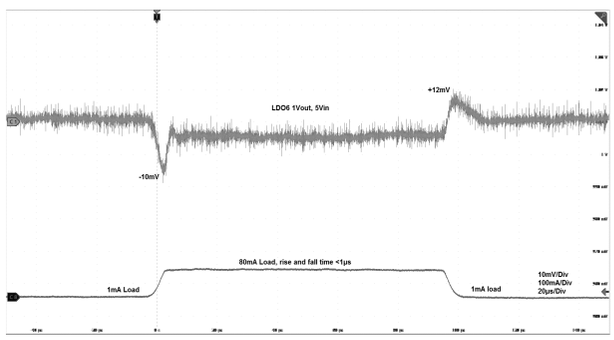


Figure 23. LDO4 line transient

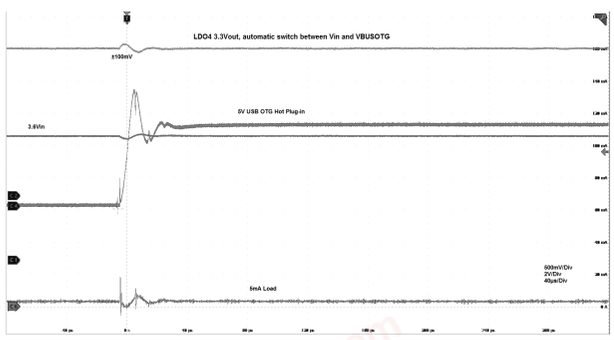
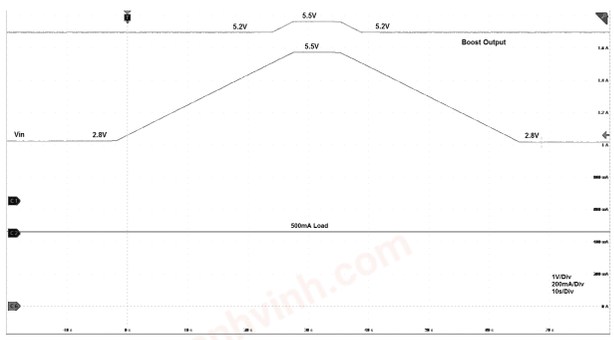


Figure 24. Boost output vs. input voltage



chanhvinh.com

Figure 25. Boost load regulation 5 V_{IN}

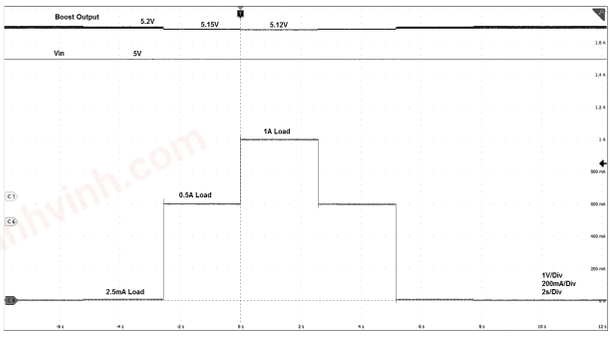


Figure 26. Boost load regulation 3.6 V_{IN}

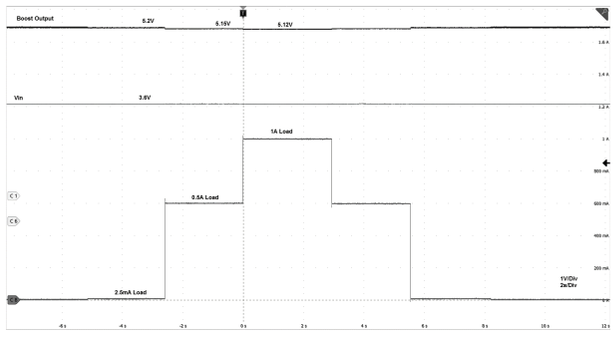


Figure 27. LDO1 line transient, no load

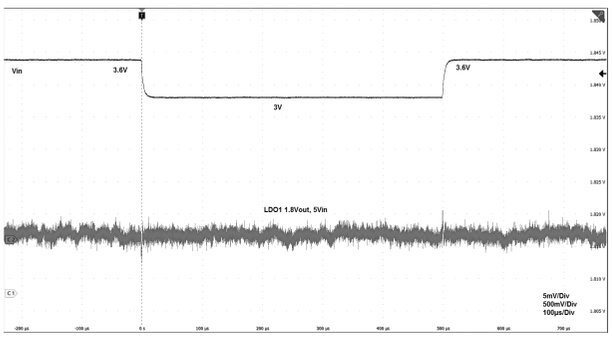


Figure 28. LDO2 line transient, no load

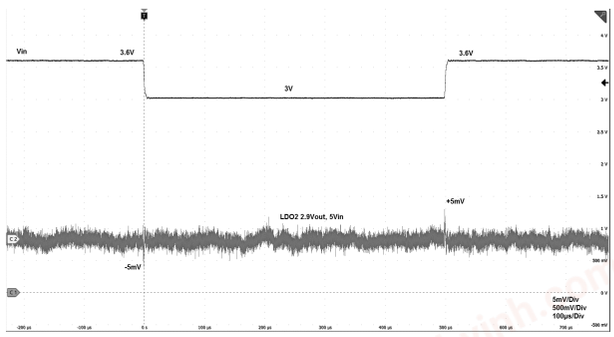


Figure 29. LDO3 line transient, no load

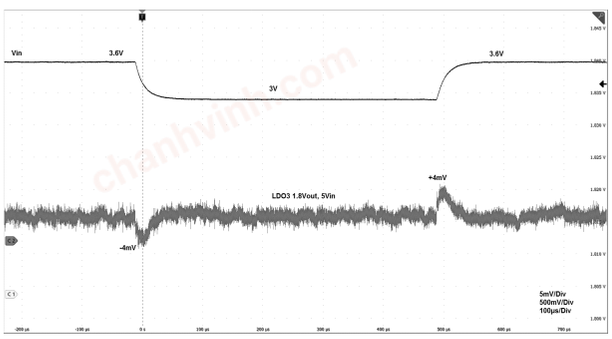


Figure 30. LDO5 line transient, no load

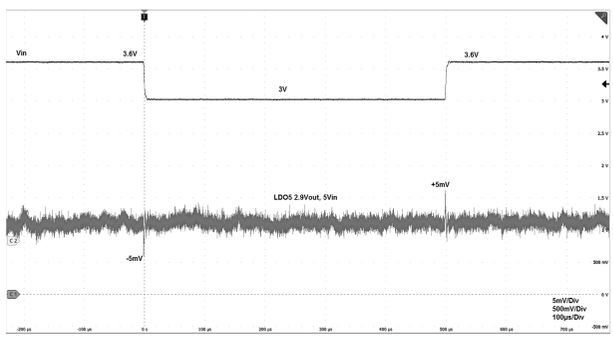


Figure 31. LDO6 line transient, no load

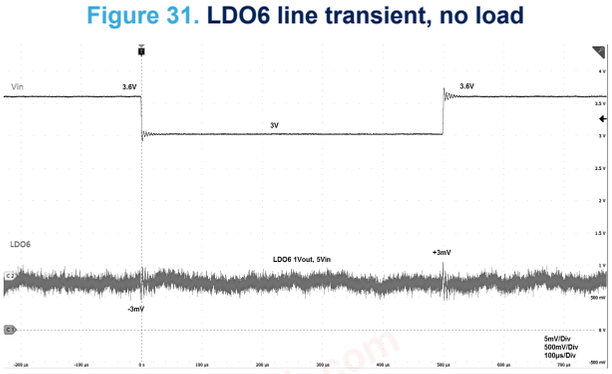
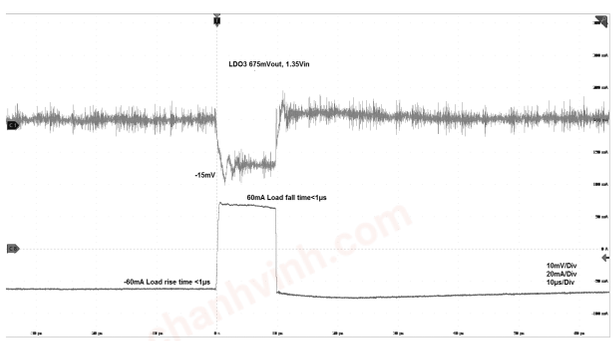


Figure 32. LDO3 sink/source mode load transient response



chanhvinh.com

Figure 33. **Buck1 turn-ON waveform**

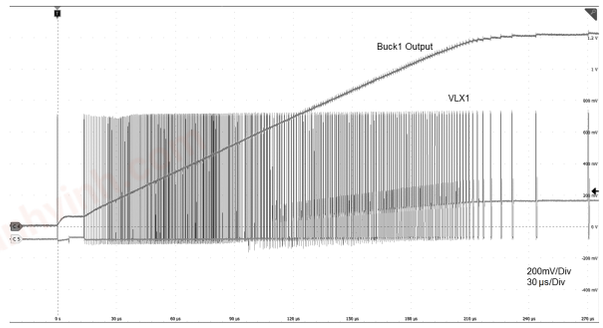


Figure 34. **STPMIC1A POWER_UP sequencing**

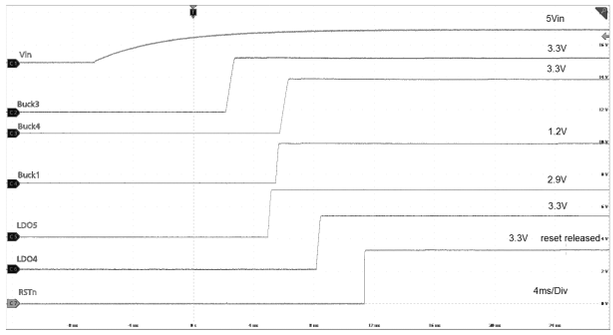


Figure 35. **STPMIC1A POWER_UP sequencing PONKEYn**

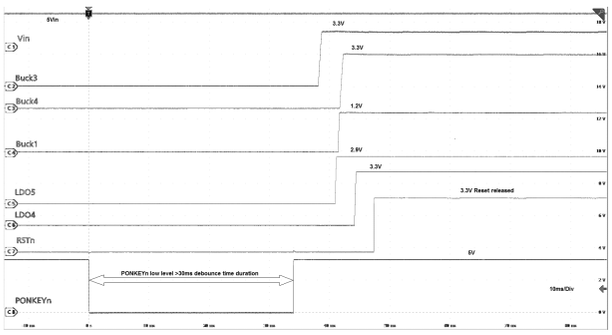


Figure 36. **STPMIC1A POWER_DOWN sequencing**

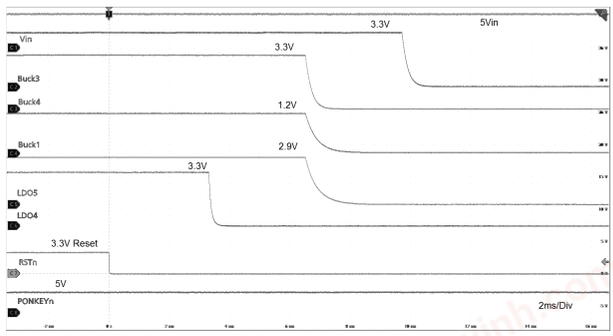
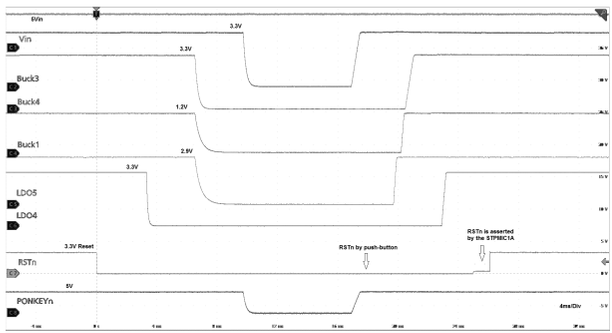


Figure 37. **STPMIC1A reset sequencing**



chanhvinh.com

4 Power regulators and switch description

4.1 Overview

The STPMIC1 has a large input voltage range from 2.8 V to 5.5 V to supply applications from typically 5 V DC wall-adaptor or from 1-cell 3.6 V Li-Ion / Li-PO battery or from USB port (bus-powered).

The STPMIC1 provides all regulators needed to power supply a complete application:

- 6 LDOs + 1 reference voltage LDO for DDR memories
- 4 step-down (buck) converters
- 1 step-up (boost) converter with a bypass to supply USB sub-system
- 2 power switches to supply USB sub-system

Table 8. General description

Regulator	Output voltage (V)	Programming step(mV)	Rated output current (mA)	Application use (example)
LDO1	1.7 to 3.3	100	350	GP
LDO2	1.7 to 3.3	100	350	SD-card or GP
LDO3 normal mode	1.7 to 3.3	100	100	lpDDR_1V8 or GP
LDO3 sink/source mode	VOUT2 / 2 (BUCK2)	-	+/-120 (+/-200 peak)	DDR3 VTT (termination)
LDO3 bypass mode	LDO3IN-V_{DROP_LDO3}	-	50	lpDDR_1V8
LDO4	3.3 (fixed)	-	50	USB PHY
LDO5	1.7 to 3.9	100	350	Application FlashMem or GP
LDO6	0.9 to 3.3	100	150	GP
REFDDR	VOUT2 / 2 (BUCK2)	-	+/-5	Vref DDR
BUCK1	0.725 to 1.5	25	1500	Application CORE
BUCK2	1 to 1.5	50	1000	lpDDR2/3/4, DDR3/L, DDR4
BUCK3	1 to 3.4	100	500	Application VIO
BUCK4	0.6 to 3.9	25 (0.6 V to 1.3 V) 50 (1.3 V to 1.5 V) 100 (1.5 to 3.9 V)	2000	Application CPU or GP
BOOST	5.2 V (fixed)	-	1100	USB ports
PWR_USB_SW	~BSTOUT	-	500	USB OTG/DRD
PWR_SW	~SWIN	-	1000	USB or GP

LDO1, LDO2, LDO5, LDO6 are general purpose (GP) LDO (low-dropout) linear regulators and can be used to supply application peripherals.

LDO3 is a multipurpose linear regulator that supports 3 modes:

- **Normal mode**: operates as standard LDO with 1.7 to 3.3 V output voltage range (for general purpose use)
- **Sink/source mode**: LDO3 operates in sink/source regulation mode to supply termination resistors of DDR3/DDR3L memory interface (VTT voltage)
- **Bypass mode**: LDO3 operates as a simple power switch to supply lpDDR2/3 VDD1 (1.8 V) power domain. In that case, LDO3IN is supplied by 1.8 V. This is a preferred mode versus normal mode in term of power efficiency to power supply lpDDR2/3 VDD1

chanhvinh.com

LDO4 is a fixed output voltage (3.3 V) LDO and it is dedicated to power supply host processor USB PHY. It is able to automatically switch among 3 power inputs (VIN, VBUSOTG and BSTOUT) to provide a valid output voltage in all application use cases, for example to support a discharged battery for Li-Ion/Li-PO battery-powered device.

DDR REF is sink/source reference voltage LDO dedicated to power VREF of lpDDR/DDR.

BUCK1 to BUCK4 are 2 MHz synchronous step-down converters optimized for high efficiency. To improve transient response, converters use an adaptive constant on-time (COT) controller with a nominal switching frequency of 2 MHz.

In low power (LP) mode, converters operate in hysteretic mode to minimize quiescent current and improve efficiency while an excellent transient response is being kept.

Buck controller also supports a dynamic voltage scaling (DVS) capability with an active discharge (voltage tracking) and a switching phase shifting pi/2 mutual synchronization between converters to reduce switching EMI radiations.

BOOST is a fixed output voltage 5.2 V synchronous step-up converter dedicated to power supply USB ports (PWR_USB_SW and/or PWR_SW power switches). In addition to support a step-up conversion for battery applications (to convert VBAT=3.6 V to VBUS= 5.2 V), this boost converter has been enhanced with a special bypass circuitry with smooth output voltage transitions to comply USB VBUS tolerance when the application is powered by a 5 V wall adaptors. This is to compensate voltage tolerance of the voltage source (wall adaptor) and voltage drop through the PCB from input supply of device to USB port.

PWR_USB_SW is a 500 mA power switch suitable for USB OTG port or USB Type-C DRD. Input is internally connected to BOOST output. It supports VBUS detection, OCP and the reverse current protection.

PWR_SW is a 1000 mA power switch, that can supply max. 2 USB STD HOST port.

4.2 LDO regulators

4.2.1 LDO regulators - common features

The STPMIC1 has 7 LDO regulators with the following meaning:

- LDO1, LDO2, LDO5 and LDO6 are general purpose LDOs
- LDO3 serves for DDR2, DDR3 memory termination (sink-source mode) or for lpDDR2 or lpDDR3 memory (bypass mode) or for general purpose. For more details refer to Section 4.3 DDR memory sub-system examples.
- LDO4 is LDO dedicated to supply 3V3 USB PHY circuit of AP
- REFDDR – sink/source LDO dedicated to provide a voltage reference for lpDDR/DDR memory

Enable/Disable - LDO can be enabled or disabled:

1. Automatically during POWER_UP/POWER_DOWN state as described in Section 5.3 POWER_UP, POWER_DOWN sequence
2. Manually by setting ENA bit in corresponding Table 40. LDOx_MAIN_CR or Table 45. LDOx_ALT_CR registers.

VOUT setting – LDO output voltage can be set:

1. Automatically during POWER_UP/POWER_DOWN state as described in section Section 5.3 POWER_UP, POWER_DOWN sequence. Default voltage is selected in *LDOx_VOUT[1:0]* bits of Table 70. NVM_LDOS_VOUT_SHR1 and Table 71. NVM_LDOS_VOUT_SHR2 registers.
2. Automatically during MAIN/ALTERNATE mode change by toggling PWRCTRL pin as defined in *VOUT[4:0]* field in corresponding Table 40. LDOx_MAIN_CR or Table 45. LDOx_ALT_CR registers.
3. Manually by setting *VOUT[4:0]* field of Table 38. BUCKx_MAIN_CR or Table 43. BUCKx_ALT_CR registers. Refer to Table 9. LDO output voltage settings

chanhvinh.com

LDOs contain the following functions:

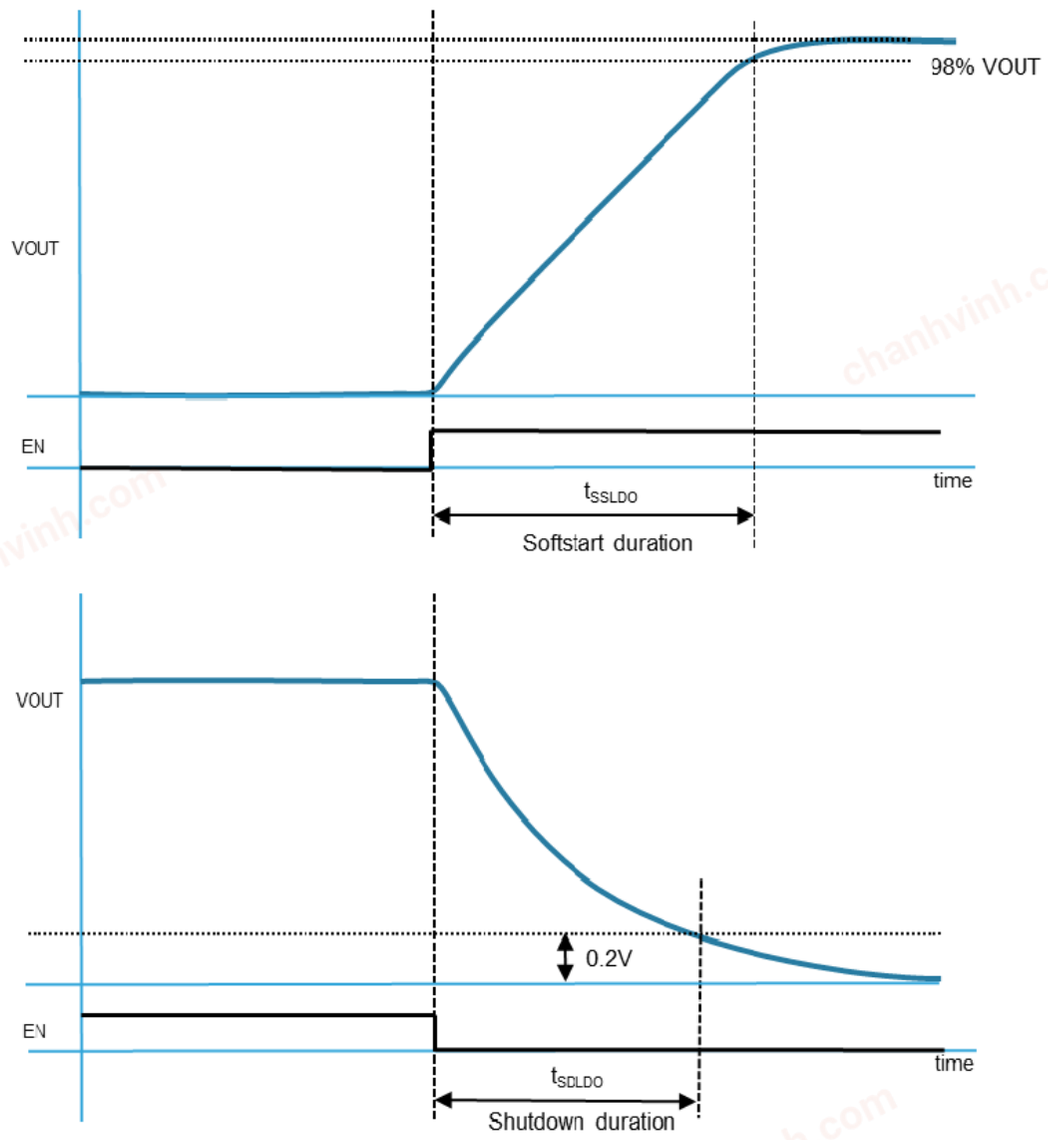
1. ***Soft-start circuit*** is implemented to limit input inrush current when LDO starts. LDO soft-start duration is defined by t_{SSLDO} parameter. For more details, Figure 38. LDO start-up/shutdown timings
2. ***Overcurrent limit circuit*** - When the load on the output of the LDO exceeds overcurrent limit threshold I_{LDOLIM}, LDO starts decreasing the output voltage limiting the output current. When the overcurrent condition on LDO lasts for more than t_{OCPDB_LDO}, *LDOx_OCP* interrupt is generated. For a detailed behavior of the device on OCP event refer to Section 5.4.7 Overcurrent protection (OCP)
3. ***Output discharge circuit*** (passive), to discharge LDO output decoupling capacitor energy. In power down sequence, it allows LDO voltage to be down before disabling next regulators in next ranking slot.

   Output discharge is by default active when LDO is disabled.

   Different behavior can be programmed in Table 28. LDO14_PD_CR and Table 29. LDO56_VREF_PD_CR registers.

Note: To ensure the LDO functionality, BUCK2IN input must be always connected to VIN power supply.

Figure 38. LDO start-up/shutdown timings



4.2.2 LDO regulators - special features

LDO3

chanhvinh.com

LDO3 is a multipurpose LDO with 3 operating modes:

1. ***Normal mode*** – LDO works as general purpose LDOs to regulate VOUT only, such as the common LDO1,2,5 and 6.
2. ***Bypass mode*** – LDO operates as a power switch providing output without any regulation. Note, that in this mode there is no overcurrent limitation available, and LDO is only protected by its input source capability; that is typically BUCK3 powering application processor VIO domain at 1.8 V.

   This mode can be set by writing to bit *BYPASS* in Table 41. LDO3_MAIN_CR or Table 46. LDO3_ALT_CR register. Bypass mode can be activated by default at startup by setting LDO3_BYPASS bit in Table 68. NVM_LDOS_RANK_SHR2.

   Important : enabling BYPASS bit in Table 41. LDO3_MAIN_CR or Table 46. LDO3_ALT_CR overrides normal and sink/source mode
3. ***Sink/source mode*** – LDO is able to regulate voltage in source and sink mode allowing current to flow to/from output; up to maximum rated current. This mode is dedicated to supply termination of DDR3/DDR3L memories with fixed output voltage. If LDO3 is used in this mode, LDO3IN should be powered from the output of BUCK2.

   When LDO3 is enabled in this mode, output voltage is fixed and follows VOUT2/2; even during BUCK2 ramp-up and ramp-down phase. Overcurrent limitation works the same way as for the other LDOs, and it is active for both load current polarities.

   This mode can be enabled by setting *VOUT[6:2]* of Table 41. LDO3_MAIN_CR or Table 46. LDO3_ALT_CR to 0x1F.

Note: LDO requires the output capacitor with a low value of ESR and care must be taken during PCB design to minimize parasitic inductance of the track between this capacitor and the device.

LDO4

It is primarily dedicated to supply 3.3 V circuit of USB analog PHY in AP.

VOUT setting – VOUT is fixed to 3.3 V

Automatic input switching - To guarantee the output voltage for various application scenarios (for example to support discharged battery for Li-Ion/Li-PO battery powered device) LDO4 can be supplied from 3 power sources: VIN, VBUSOTG and BSTOUT. The selection among these 3 power inputs is fully automatic, no user intervention is needed. Internal circuit continuously monitors voltage levels on these pins and selects the input source having the highest input voltage.

Active input source of LDO4 can be read out from *LDO4_SRC[1:0]* in Section 6.2.5 Restart status register (RESTART_SR) status register.

REFDDR LDO (DDR reference voltage)

DDR_REF is sink/source LDO similar to LDO3 sink/source mode LDO but with lower current capability primarily dedicated to supply VREF pin of lpDDR/DDR memories.

VOUT setting - Output voltage is fixed at $V_{OUT2}/2$ at any time. Input of REFDDR is internally connected to BUCK2IN.

In case BUCK2 is enabled/disabled when REFDDR is enabled, output of the REFDDR follows BUCK2 startup/shutdown waveforms always keeping $V_{OUT2}/2$.

Overcurrent limit circuit - When short-circuit event occurs, output of the LDO is current-limited and output voltage decreases, however this LDO cannot trigger interrupt or shutdown the device.

4.2.3 LDO output voltage settings

Table 9. LDO output voltage settings

	VOUT[4:0] LDOx_MAIN/ ALT_CR[6:2]	V_{OUT}[V] LDO1	V_{OUT}[V] LDO2	V_{OUT}[V] LDO3	V_{OUT}[V] LDO5	V_{OUT}[V] LDO6
Step 100 mV	0	1.7	1.7	1.7	1.7	0.9
	1	1.7	1.7	1.7	1.7	1
	2	1.7	1.7	1.7	1.7	1.1
	3	1.7	1.7	1.7	1.7	1.2

chanhvinh.com

	VOUT[4:0] LDOx_MAIN/ ALT_CR[6:2]	V_{OUT}[V] LDO1	V_{OUT}[V] LDO2	V_{OUT}[V] LDO3	V_{OUT}[V] LDO5	V_{OUT}[V] LDO6
Step 100 mV	4	1.7	1.7	1.7	1.7	1.3
	5	1.7	1.7	1.7	1.7	1.4
	6	1.7	1.7	1.7	1.7	1.5
	7	1.7	1.7	1.7	1.7	1.6
	8	1.7	1.7	1.7	1.7	1.7
	9	1.8	1.8	1.8	1.8	1.8
	10	1.9	1.9	1.9	1.9	1.9
	11	2.0	2.0	2.0	2.0	2.0
	12	2.1	2.1	2.1	2.1	2.1
	13	2.2	2.2	2.2	2.2	2.2
	14	2.3	2.3	2.3	2.3	2.3
	15	2.4	2.4	2.4	2.4	2.4
	16	2.5	2.5	2.5	2.5	2.5
	17	2.6	2.6	2.6	2.6	2.6
	18	2.7	2.7	2.7	2.7	2.7
	19	2.8	2.8	2.8	2.8	2.8
	20	2.9	2.9	2.9	2.9	2.9
	21	3.0	3.0	3.0	3.0	3.0
	22	3.1	3.1	3.1	3.1	3.1
	23	3.2	3.2	3.2	3.2	3.2
	24	3.3	3.3	3.3	3.3	3.3
	25	3.3	3.3	3.3	3.4	3.3
	26	3.3	3.3	3.3	3.5	3.3
	27	3.3	3.3	3.3	3.6	3.3
	28	3.3	3.3	3.3	3.7	3.3
	29	3.3	3.3	3.3	3.8	3.3
	30	3.3	3.3	3.3	3.9	3.3
	31	3.3	3.3	**VOUT2/2 (sink/source)**	3.9	3.3

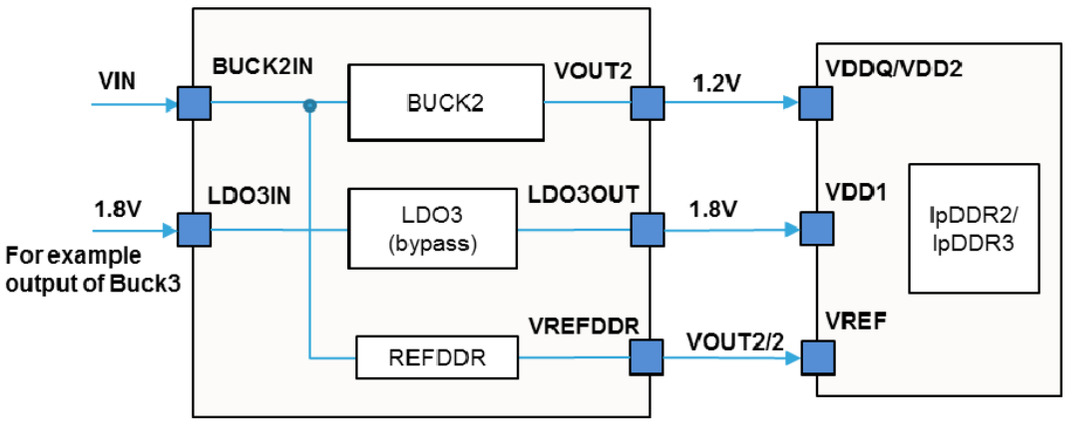
chanhvinh.com

4.3 DDR memory sub-system examples

BUCK2, LDO3 and REFDDR regulators can be used in several possible configurations, to supply various types of DDR memories.

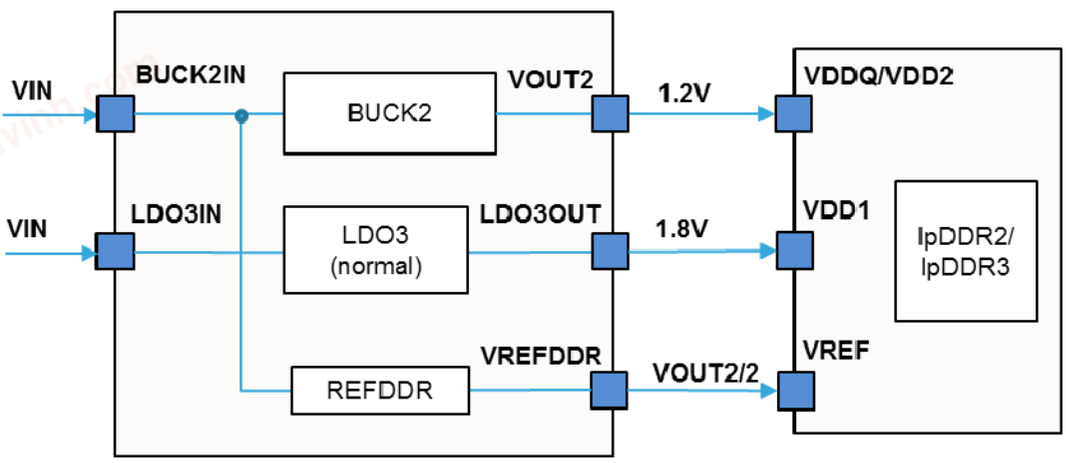
4.3.1 Powering lpDDR2/lpDDR3 memory

Figure 39. Powering lpDDR2/lpDDR3 memory (LDO3 in bypass mode)



The example in Figure 39. Powering lpDDR2/lpDDR3 memory (LDO3 in bypass mode) shows how to use LDO3 in bypass mode to power supply lpDDR2/3 VDD1 (1.8 V) power domain. LDO3IN is supplied by 1.8 V power source that is usually from BUCK3 output when BUCK3 is set at 1.8 V to power supply the application processor VIO power domain. This topology reaches better power efficiency than next example in Figure 40. Powering lpDDR2/lpDDR3 memory (LDO3 normal mode supplied from VIN).

Figure 40. Powering lpDDR2/lpDDR3 memory (LDO3 normal mode supplied from VIN)

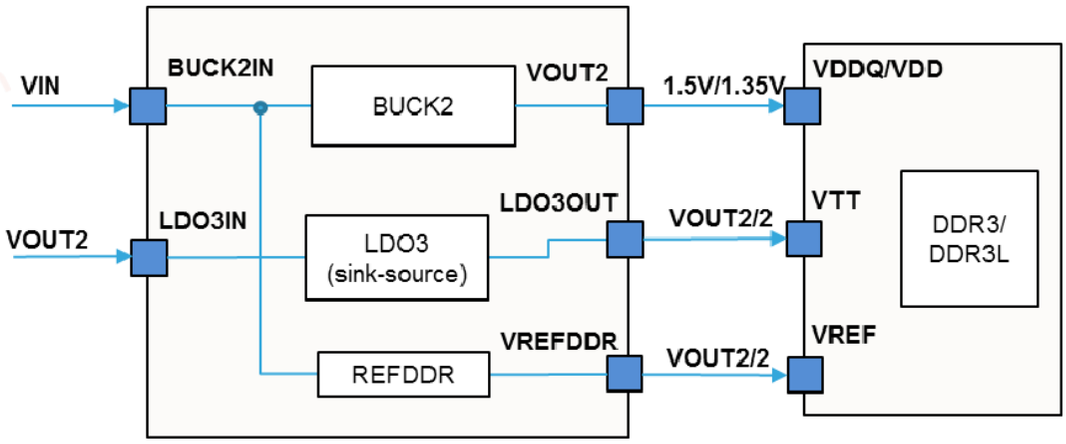


The example in Figure 40. Powering lpDDR2/lpDDR3 memory (LDO3 normal mode supplied from VIN) shows how to use LDO3 in normal mode to power supply lpDDR2/3 VDD1 (1.8V) power domain. LDO3IN is supplied by a power source having higher voltage than LDO3OUT (VIN in this example). This topology is suitable for those applications which do not have 1.8 V power source available from a buck converter.

chanhvinh.com

4.3.2 Powering DDR3/DDR3L memory

Figure 41. **Powering DDR3/DDR3L memory (LDO3 in sink/source mode)**



The example in Figure 41. Powering DDR3/DDR3L memory (LDO3 in sink/source mode) shows how to use LDO3 in sink/source mode to power supply termination resistor network of DDR3/DDR3L memory (aka VTT). LDO3IN is a power supply from BUCK2 output (VOUT2) and LDO3 output regulate at Vout2/2 voltage.

4.4 Buck converters

4.4.1 BUCK general description

There are 4 buck converters in the STPMIC1 optimised to supply circuits with high current consumption and fast transient response requirement.

BUCK1 is primarily dedicated to power supply CORE power domain of application processors.

BUCK2 is primarily dedicated to power supply DDR memory.

BUCK3 is primarily dedicated to VIO domain and analog subsystem.

BUCK4 is for general purpose, it can be used to supply CPU power domain of application processors having CORE and CPU power domain splitted.

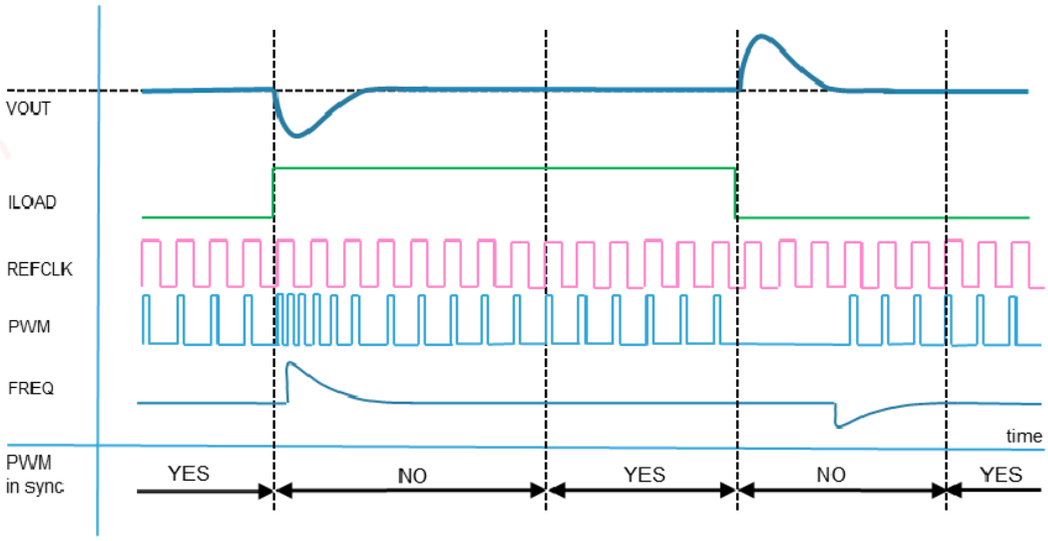
All converters are based on an adaptive constant-on-time controller (COT), that guarantees an excellent transient response and high efficiency across a wide range of operating conditions.

Each converter can work in 2 power modes – HP mode, and LP mode. These modes differ both in performance and quiescent current consumption. In HP mode the highest performance can be reached, while in LP mode the performance is lower with a much lower consumption.

Switching frequency of converter is 2 MHz in steady-state CCM condition. During load transient, switching frequency can be temporarily increased/decreased to provide accurate amount of energy needed and minimize voltage error. Refer to the figure below.

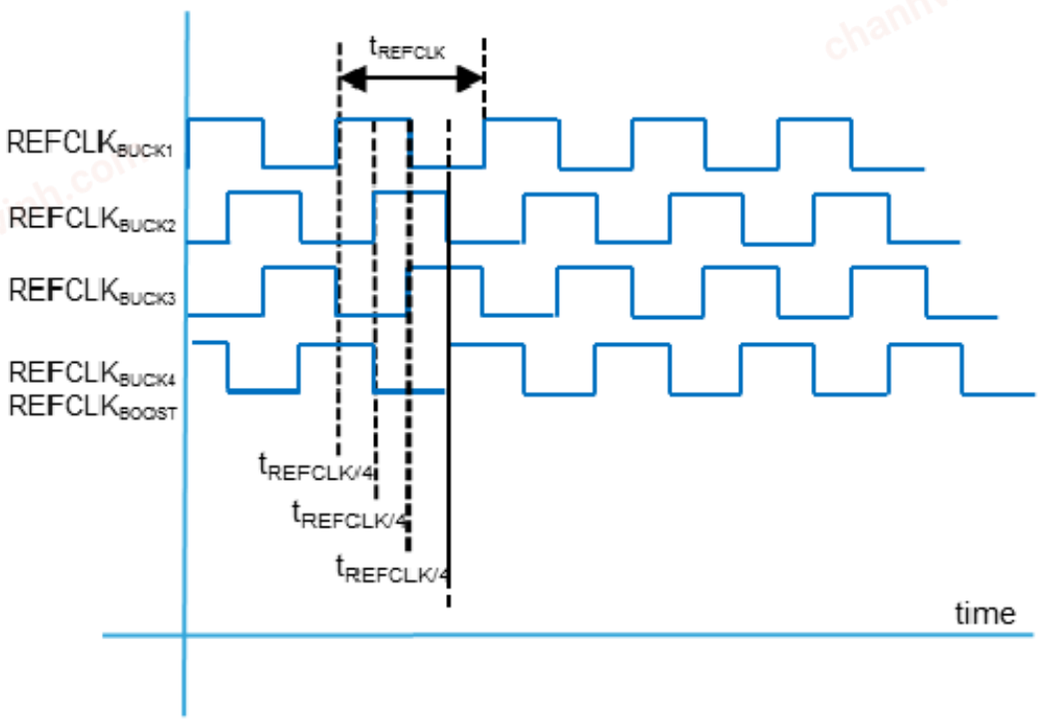
chanhvinh.com

Figure 42. **PWM clock generation**



Clock synchronization (HP mode)– buck controller integrates phase locked loop (PLL) circuit, that maintains steady-state frequency in CCM phase-locked to reference 2 MHz clock generated by internal oscillator. Each buck has its own reference clock that is shifted from master clock by 90 degree, which minimizes the chance of multiple controllers switching at the same time, and improving EMI performance. Refer to Figure 43. PWM clock synchronisation .

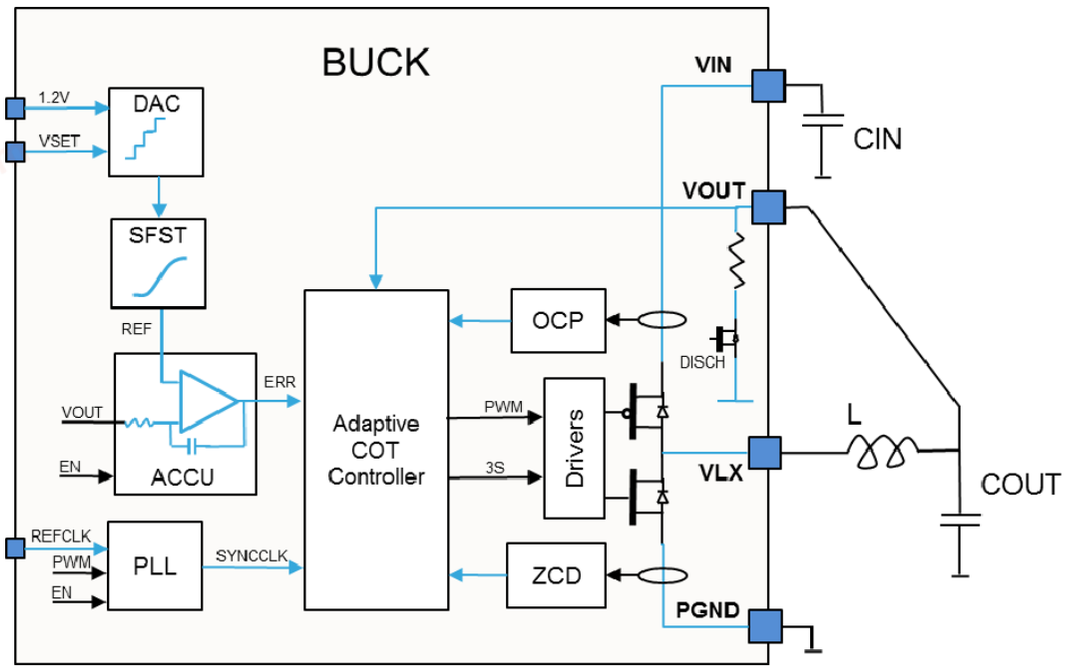
Figure 43. **PWM clock synchronisation**



Voltage accuracy (HP mode)- COT controllers are well-known for their excellent transient response but standard implementations usually suffer from a high output load regulation error. To cope with this problem, the STPMIC1 adaptive COT controller also integrates an ACCU loop circuit that fixes the parameters of controller in order to reach the maximum possible accuracy of output voltage for all operating conditions. Refer to Figure 44. Buck block diagram.

chanhvinh.com

Figure 44. **Buck block diagram**



Light low power consumption (HP mode)– To minimize power consumption in low load conditions PFM mode is implemented. Switching between PFM and PWM mode is smooth, fully automatic, and requires no user intervention.

Low power mode (LP mode) – If the application remains in low load conditions for longer time, the converter can be switched to LP mode and minimize quiescent consumption to $I_{Q_BK_LP}$. In LP mode, the controller works in hysteretic PFM mode, and has the following features:

1. Maximum DC current capability is lower, specified by I_{OUT}. However, also in LP mode, converter is able to handle peak current load of up to $I_{OUT_LP_PEAK}$ but transient response and accuracy are not guaranteed.
2. ACCU loop is disabled, which results in a lower V_{OUT} accuracy specified by $V_{OUT1-ACC}$
3. PLL is disabled. Converter is in PFM mode, which means pulses are not synced to reference clock

To guarantee the best performance, it is recommended LP mode to be entered only when output load is below I_{OUTMAX_LP}, LP mode can be entered by setting *PREG_MODE* bit Table 38. BUCKx_MAIN_CR or Table 43. BUCKx_ALT_CR registers.

Exit from LP mode - It is recommended that application processor switches from LP mode to HP mode before it applies full rated load exceeding maximum LP current I_{OUT_LP}. This time is defined as minimum LP to HP recovery time $t_{LP-HP-BK}$If load is increased before this time, buck converter stays in regulation but transient or accuracy specification may not be guaranteed. Refer to Figure 45. BUCKx LP to HP mode recovery time.

Note: During POWER_UP sequence, buck is always started in HP mode, with default VOUT configuration defined in NVM_BUCKx_VOUT[1:0] bits of Table 69. NVM_BUCKS_VOUT_SHR register.

Enable/disable - BUCK can be enabled or disabled:

1. Automatically during POWER_UP/POWER_DOWN state as described in Section 5.3 POWER_UP, POWER_DOWN sequence
2. Manually by setting ENA bit in corresponding Table 38. BUCKx_MAIN_CR or Table 43. BUCKx_ALT_CR registers

VOUT setting – BUCK output voltage can be set:

1. Automatically during POWER_UP/POWER_DOWN state as described in Section 5.3 POWER_UP, POWER_DOWN sequence

   Default voltage is selected in *BUCKx_VOUT[1:0]* bits of Table 69. NVM_BUCKS_VOUT_SHR register.
2. Automatically during MAIN/ALTERNATE mode change by toggling PWRCTRL pin as defined in *VOUT[5:0]* field in corresponding Table 38. BUCKx_MAIN_CR or Table 43. BUCKx_ALT_CR registers.

chanhvinh.com

3. Manually by setting *VOUT[5:0]* field of Table 38. BUCKx_MAIN_CR or Table 43. BUCKx_ALT_CR registers. Refer to Section 4.2.3 LDO output voltage settings.

Dynamic voltage scaling (DVS) – When Buck voltage is changed by writing to *VOUT[5:0]* bits in POWER_ON state, Buck reference is digitally stepped up/down in order to keep VOUT slew rate defined by parameter SR_{BK}.

When a lower VOUT is requested, Buck operates in “boost reverse” mode to discharge the output capacitor with the same slew rate SR_{BK}, providing current back to the input supply capacitor. This improves efficiency because energy stored in the output capacitor is not lost but “recycled” into input capacitor. For more details refer to Figure 47. BUCKx dynamic voltage scaling (DVS) .

Bypass capability – BUCK3 and BUCK4 switch to bypass mode with 100% duty cycle when V_{IN} voltage is below target VOUT setting. Transition to bypass mode is fully automatic and requires no user intervention.

Overcurrent protection – When inductor current exceeds peak current limit threshold I_{BK1_LIM}, PWM pulse is immediately stopped, and buck starts to decrease output voltage limiting the output current. When this condition lasts for more than t_{OCPDB_BUCK}, *BUCKx_OCP* interrupt is generated.

For a detailed behavior of the device on OCP event refer to Section 5.4.7 Overcurrent protection (OCP).

VOUT Protection – BUCK4 VOUT value digital setting can be limited to 1.3 V by writing *BUCK4_CLAMP* bit in Table 68. NVM_LDOS_RANK_SHR2 register.

This feature can be used to prevent destruction of low-voltage circuit connected to VOUT4, in case of erroneous/unwanted software access to Table 38. BUCKx_MAIN_CR or Table 43. BUCKx_ALT_CR.

Start-up sequence – After the Buck is enabled, variable calibration delay is present before the output voltage starts rising. This delay is specified as start-up delay t_{SU_BUCKx}. For details about start-up/shutdown timings refer to Figure 46. BUCKx start-up/shutdown timings.

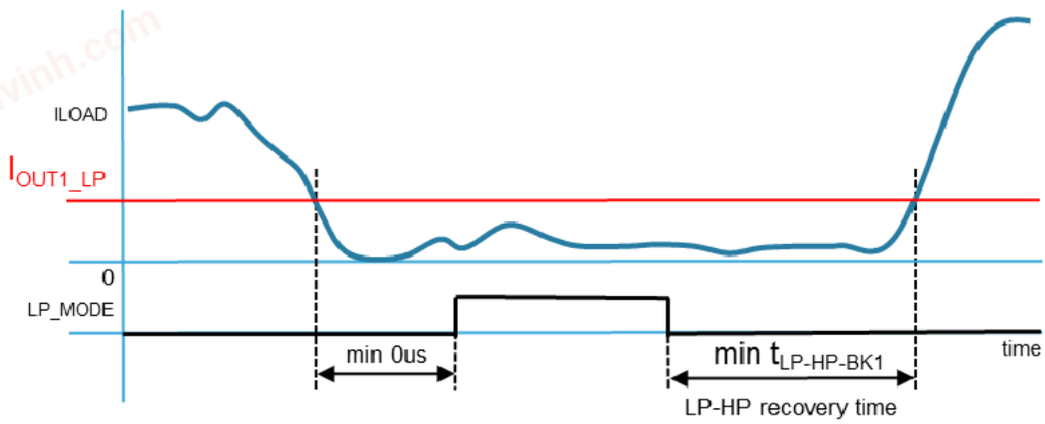
Output discharge – Buck has configurable passive output discharge circuit to guarantee that shutdown time is shorter than single ranking slot in POWER_DOWN sequence.

Discharge circuit can be configured to **Slow PD** (pull-down) for longer discharge time or **Fast PD** for faster discharge time. Discharge duration is defined accordingly by t_{SD_BKx}.

Slow output discharge circuit is active by default when buck is disabled.

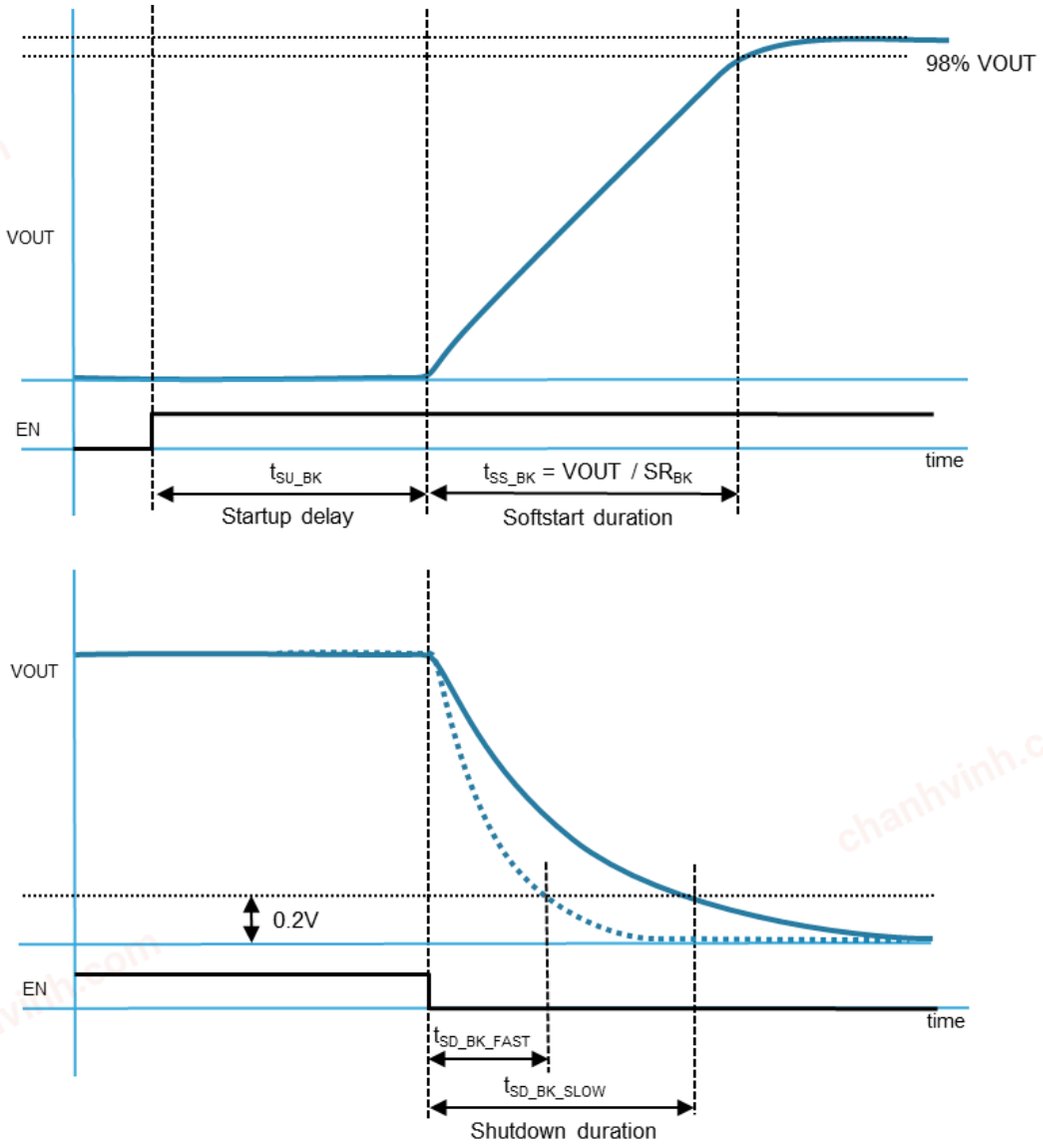
Different behavior can be programmed in *BUCKx_PD[1:0]* bits of *BUCKS_PD_CR* register.

Figure 45. BUCKx LP to HP mode recovery time



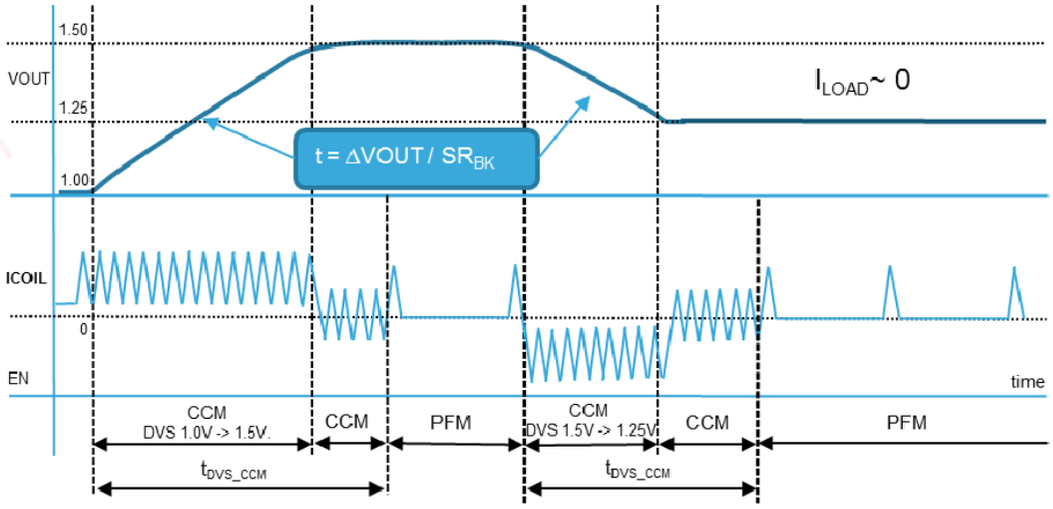
chanhvinh.com

Figure 46. **BUCKx start-up/shutdown timings**



chanhvinh.com

Figure 47. **BUCKx dynamic voltage scaling (DVS)**



chanhvinh.com

4.4.2 BUCK output voltage settings

Table 10. BUCK output settings

VOUT[5:0] BUCKx_MAIN/ALT_CR[7:2]	V_{OUT}[V] BUCK1	V_{OUT}[V] BUCK2	V_{OUT}[V] BUCK3	V_{OUT}[V] BUCK4
0	0.725	1	1	0.6(1)
1	0.725	1	1	0.625(1)
2	0.725	1	1	0.65(1)
3	0.725	1	1	0.675(1)
4	0.725	1	1	0.7(1)
5	0.725(1)	1	1	0.725(1)
6	0.75(1)	1	1	0.75(1)
7	0.775(1)	1	1	0.775(1)
8	0.8(1)	1	1	0.8(1)
9	0.825(1)	1	1	0.825(1)
10	0.85(1)	1	1	0.85(1)
11	0.875(1)	1	1	0.875(1)
12	0.9(1)	1	1	0.9(1)
13	0.925(1)	1	1	0.925(1)
14	0.95(1)	1	1	0.95(1)
15	0.975(1)	1	1	0.975(1)
16	1(1)	1	1	1(1)
17	1.025(1)	1 (2)	1	1.025(1)
18	1.05(1)	1.05(2)	1	1.05(1)
19	1.075(1)	1.05(2)	1 (3)	1.075(1)
20	1.1(1)	1.1(2)	1.1(3)	1.1(1)
21	1.125(1)	1.1(2)	1.1(3)	1.125(1)
22	1.15(1)	1.15(2)	1.1(3)	1.15(1)
23	1.175(1)	1.15(2)	1.1(3)	1.175(1)
24	1.2(1)	1.2(2)	1.2(3)	1.2(1)
25	1.225(1)	1.2(2)	1.2(3)	1.225(1)
26	1.25(1)	1.25(2)	1.2(3)	1.25(1)
27	1.275(1)	1.25(2)	1.2(3)	1.275(1)
28	1.3(1)	1.3(2)	1.3(3)	1.3(1)
29	1.325(1)	1.3(2)	1.3(3)	1.3(2)
30	1.35(1)	1.35(2)	1.3(3)	1.35(2)
31	1.375(1)	1.35(2)	1.3(3)	1.35(2)
32	1.4(1)	1.4(2)	1.4(3)	1.4(2)
33	1.425(1)	1.4(2)	1.4(3)	1.4(2)

chanhvinh.com

VOUT[5:0] BUCKx_MAIN/ALT_CR[7:2]	V_{OUT}[V] BUCK1	V_{OUT}[V] BUCK2	V_{OUT}[V] BUCK3	V_{OUT}[V] BUCK4
34	1.45(1)	1.45(2)	1.4(3)	1.45(2)
35	1.475(1)	1.45(2)	1.4(3)	1.45(2)
36	1.5(1)	1.5(2)	1.5(3)	1.5(2)
37	1.5	1.5	1.6(3)	1.6(3)
38	1.5	1.5	1.7(3)	1.7(3)
39	1.5	1.5	1.8(3)	1.8(3)
40	1.5	1.5	1.9(3)	1.9(3)
41	1.5	1.5	2(3)	2(3)
42	1.5	1.5	2.1(3)	2.1(3)
43	1.5	1.5	2.2(3)	2.2(3)
44	1.5	1.5	2.3(3)	2.3(3)
45	1.5	1.5	2.4(3)	2.4(3)
46	1.5	1.5	2.5(3)	2.5(3)
47	1.5	1.5	2.6(3)	2.6(3)
48	1.5	1.5	2.7(3)	2.7(3)
49	1.5	1.5	2.8(3)	2.8(3)
50	1.5	1.5	2.9(3)	2.9(3)
51	1.5	1.5	3(3)	3(3)
52	1.5	1.5	3.1(3)	3.1(3)
53	1.5	1.5	3.2(3)	3.2(3)
54	1.5	1.5	3.3(3)	3.3(3)
55	1.5	1.5	3.4(3)	3.4(3)
56	1.5	1.5	3.4	3.5(3)
57	1.5	1.5	3.4	3.6(3)
58	1.5	1.5	3.4	3.7(3)
59	1.5	1.5	3.4	3.8(3)
60	1.5	1.5	3.4	3.9(3)
61	1.5	1.5	3.4	3.9
62	1.5	1.5	3.4	3.9
63	1.5	1.5	3.4	3.9

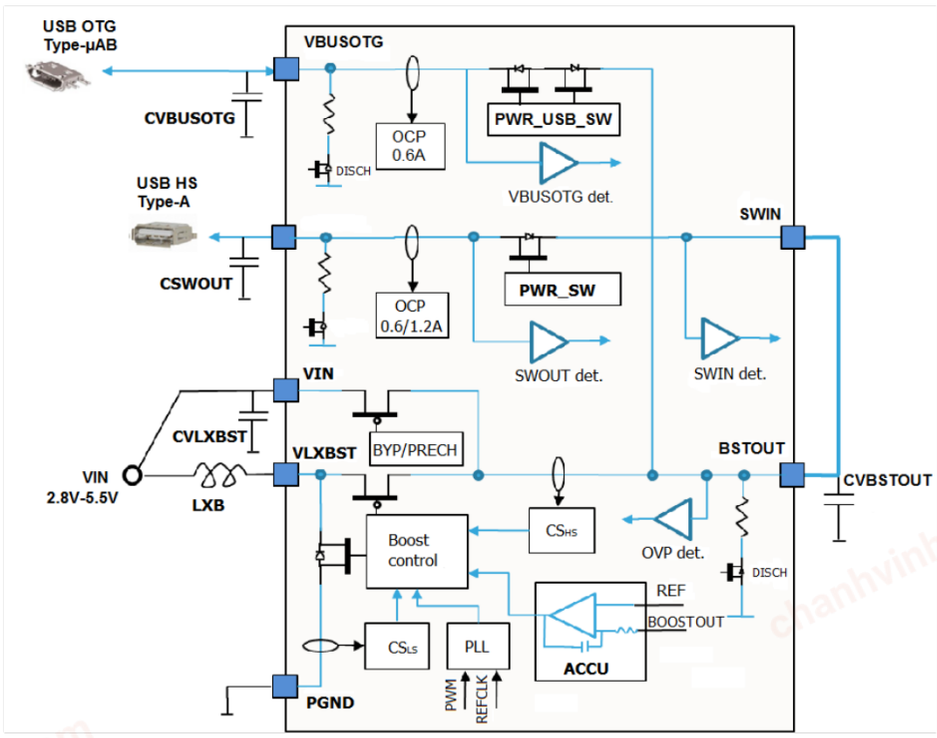
1. *Step 25 mV*
2. *Step 50 mV*
3. *Step 100 mV*

chanhvinh.com

4.5 Boost converter and power switches

The STPMIC1 integrates boost converter and two power switches, primarily dedicated to supply USB sub-system: PWR_USB_SW with 500 mA capability PWR_SW with 1 A capability.
For application examples refer to USB sub-system examples.

Figure 48. Boost and switch block diagram



4.5.1 Boost converter

Boost is a synchronous constant on-time step-up converter with fixed 5.2 V output. It is dedicated to power supply USB sub-system (VBUS) with 1.1 A rated output current to supply up to 3 USB ports: x2 USB host port @500 mA + 1 USB OTG port @100 mA.

Boost requires 3 small external components only to operate (1 coil LXB, 2 capacitors CVLXBST and CBSTOUT) – there is no external diode required. Refer to: Table 2. Passive components.

Input voltage range Converter is capable to supply 0.5 A starting from as low as 2.8 V input, and full rated current from 3.3 V input. This allows a wide range of applications to be supported embedding USB host port like Li-Ion/Li-Po battery powered applications or 5 V DC wall adaptor applications.

Bypass feature Boost integrates an advanced bypass circuitry that allows fast and smooth transition to be performed from boost to bypass operation and reciprocally to keep VBUS in USB compliant tolerance [4.75 V;5.5 V]. This allows USB subsystems to be supplied with standard 5 V DC wall adaptors.

- When the wall adaptor voltage is below ~5.2 V (due to its nominal tolerance, load regulation or voltage loss between adaptor and device), the converter works in boost mode
- When the wall adaptor voltage is between ~5.2 V to 5.5 V (due to its nominal tolerance or light device load), the converter works in bypass mode

Switching frequency of converter is 2 MHz in steady-state CCM condition for VIN below ~5 V. During load transient, switching frequency can be temporarily increased/decreased to provide accurate amount of energy needed and minimize the voltage error. For VIN above ~5.2 V or for low load conditions, 2 MHz frequency decreases to optimum.

chanhvinh.com

Clock synchronization - The controller integrates PLL circuit, that maintains steady-state frequency in CCM locked in phase to reference 2 MHz clock generated by the internal oscillator. Boost clock is shifted in phase to Buck reference clocks, which minimizes the chance of multiple controllers switching at the same time, and improving EMI performance.

Enable/disable – Boost can be enabled in POWER_ON state only by I^2C setting of *BST_ON* bit in *BST_SW_CR* register.

Boost can be disabled by I^2C clearing *BST_ON* bit.

Boost is also disabled during POWER_DOWN sequence in RANK0 slot and when overcurrent or overvoltage condition is present for defined time.

Output discharge – When boost is switched off (*BST_ON* bit = '0'), switching stops immediately and a passive discharge, enabled on BSTOUT by default, occurs.

Output discharge can be disabled by setting *BST_PD*bit in Table 29. LDO56_VREF_PD_CR register.

Overvoltage protection – Boost converter has an overvoltage protection. If voltage on BSTOUT pin exceeds V_{BSTOVP} threshold, LXB pin stops switching immediately, and remains in high impedance state. If the overvoltage condition lasts for more than t_{OVPDB_BST}, boost is disabled, and *BST_OVP* interrupt is generated.

OVP event on BSTOUT also disables switches PWR_USB_SW and PWR_SW (if *NVM_SWOUT_BOOST_OVP* is set in Table 70. NVM_LDOS_VOUT_SHR1).

Overcurrent protection – Boost implements low-side current sensor with peak current detector (I_{BSTLIM}), and high-side current sensor with short-circuit detector, (I_{BSTSH}). If the overcurrent condition during HS phase lasts for more than t_{OCPDB_BST}, boost is disabled, and *BST_OCP* interrupt is generated.

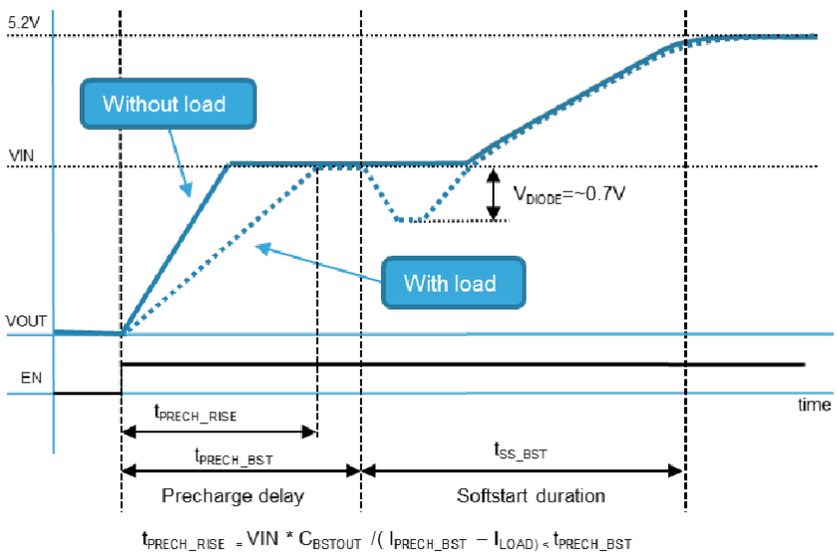
Start-up sequence Boost start-up sequence consists of 2 phases:

- ***Precharge phase -*** in this phase, bypass switch operates in "constant current source" mode and charges boost output capacitor with constant I_{PRECH_BST} current for t_{PRECH_BST} duration. After this time, boost output voltage is checked. If $V_{BSTOUT} > V_{PRECH} =\sim (V_{IN} – 0.7\ V)$, boost starts switching and proceeds to soft-start phase, besides boost is immediately turned off and BST_OCP interrupt is generated

Note: Boost load during precharge phase must be minimized, from this reason it is necessary to enable PWR_USB_SW and PWR_SW after the boost soft-start is finished.

- ***Soft-start phase –*** in this phase boost switches, the inrush current minimizes. Soft-start duration is t_{SS_BST}

Figure 49. Boost start-up sequence



$$t_{PRECH_RISE} = VIN * C_{BSTOUT} / (I_{PRECH_BST} - I_{LOAD}) < t_{PRECH_BST}$$

4.5.2 PWR_USB_SW and PWR_SW power switches

PWR_USB_SW is a 500 mA power switch dedicated to supply a USB port (VBUS voltage) and it is compatible with USB OTG specifications. PWR_USB_SW input is internally connected to boost converter output (BSTOUT). See Figure 48. Boost and switch block diagram.

chanhvinh.com

Reverse current protection - VBUSOTG pin is a switch with a reverse current protection to prevent leakage from VBUSOTG pin to BSTOUT or VIN when switch is OFF.

Enable/disable – PWR_USB_SW can be enabled in POWER_ON state by I²C setting of *VBUSOTG_ON* bit in Table 48. BST_SW_CR register. PWR_USB_SW switch cannot be enabled automatically during power-up sequence. During power-down sequence, switch is turned OFF in RANK0 phase.

It is recommended that PWR_USB_SW is enabled only after boost converter works in steady-state (after boost start-up sequence). This is typically ~2 ms after boost is enabled. Nevertheless, if PWR_USB_SW is enabled earlier than Boost, it turns ON only when both boost is enabled by BST_ON bit and BSTOUT voltage is higher than ~V_{IN}.

Boost OVP – When boost OVP is detected PWR_USB_SW is disabled automatically.

VBUSOTG pin monitoring – When PWR_USB_SW is OFF, VBUSOTG voltage is monitored by VBUSOTG det. to detect VBUS voltage rising/falling from USB OTG connector due to USB cable insertion/removal.

When voltage on $V_{VBUSOTG}$ pin goes higher than $V_{VBUSOTG_Rise}$ threshold, the interrupt and/or turn-ON condition is generated. When voltage on VBUSOTG pin goes below than $V_{VBUSOTG_Fall}$ threshold, the interrupt is generated. VBUSOTG pin monitoring is filtered by $t_{VBUSOTGDB}$ debounce timer for both rising and falling voltage. VBUSOTG detector is enabled by default and can be disabled by setting *VBUSOTG_DET_DIS* bit Table 48. BST_SW_CR register.

Soft-on/off –Switch implements soft-on, soft-off circuit. After the switch is enabled, switch starts operating in “current limiting” mode, gradually increasing the output current limit until the switch is fully turned ON. This soft-on phase has a duration defined by $t_{SS_VBUSOTG}$.

The same mechanism is also applied during switch soft-off phase during turn-off to prevent quick unloading of BSTOUT and excessive voltage overshoot.

Overcurrent limitation – Switch implements 2 levels of overcurrent protection:

1. When load on the output exceeds overcurrent limit threshold $I_{VBUSOTGOCP}$, switch starts limiting the output voltage to decrease output current. If the switch stays in this condition for more than $t_{OCPDBSW}$, switch is automatically turned OFF, and *VBUSOTG_OCP* interrupt generated.
2. In case the output load exceeds $I_{VBUSOTG_SH}$ threshold, switch turns OFF immediately to prevent boost overload, and *VBUSOTG_SH* interrupt is generated. Shortly after this action, switch is re-enabled automatically with standard soft-on current limiting procedure. In case the overload condition is still present, the switch continues operation in current limiting mode, and is finally switched OFF after $t_{OCPDBSW}$. In case overload condition is removed before $t_{OCPDBSW}$, switch continues its normal operation.

For detailed behavior of the device on OCP event refer to Section 5.4.7 Overcurrent protection (OCP).

Output discharge – Switch implements passive discharge circuit (by default disabled) that can be enabled by setting *VBUSOTG_PD* bit in Table 48. BST_SW_CR.

PWR_SW is a configurable 500 mA/1000 mA power switch that can be used to power supply one or two USB host ports or for general purpose.

It has dedicated the input SWIN and the output SWOUT pin.

Minimum SWIN voltage to enable the switch is V_{SWIN_Rise}.

PWR_SW pin is a switch without reverse current protection. If voltage on SWOUT is higher than SWIN-0.7 V, a leakage from SWOUT to SWIN occurs even if the switch is OFF.

Enable/disable – PWR_SW can be enabled in POWER_ON state by I²C setting of *SWOUT_ON* bit in Table 48. BST_SW_CR. PWR_SW switch cannot be enabled automatically during power-up sequence. During power-down sequence, switch is automatically turned OFF in RANK0 phase.

PWR_SW turns ON only when SWIN voltage is higher than V_{SWIN_Rise} threshold.

If the switch is supplied by boost, it is recommended to enable the switch after boost is already in steady-state with 5.2 V output. This is typically ~2 ms after boost is enabled.

Boost OVP – When boost OVP is detected, switch is ON by default. It is disabled automatically only if *NVM_SWOUT_BOOST_OVP* bit is set.

SWOUT pin monitoring – When PWR_SW is OFF, SWOUT voltage is monitored by SWOUT detector.

When $V_{SWOUT} > V_{SWOUT_Rise}$, interrupt and turn-ON condition is generated. SWOUT detector is enabled by default and can be disabled by setting *SWOUT_DET_DIS* bit in Table 30. SW_VIN_CR.

$t_{SWOUTDB}$ debounce timer is on SWOUT detector output.

chanhvinh.com

SWIN pin monitoring – SWIN detector is disabled by default and can be enabled to monitor the voltage on SWIN pin by setting *SWIN_DET_EN* bit in Table 48. BST_SW_CR.

When $V_{SWIN} > V_{SWIN_Rise}$, interrupt is generated.

t_{SWINDB} debounce timer is on SWIN detector output.

Note: Regardless SWIN detector is enabled or not, PWR_SW is enabled only if $V_{SWIN} > V_{SWIN_Rise}$.

Soft-on/off – Switch implements soft-on, soft-off circuit. After the switch is enabled, switch starts operating in “current limiting” mode, gradually increasing the output current limit until the switch is fully turned ON. This soft-on phase has a duration defined by t_{SS_SWOUT}.

The same mechanism is also applied during switch soft-off phase during turn-off to prevent quick unloading of SWIN and excessive voltage overshoot.

Overcurrent limitation – Switch implements 2 levelsof overcurrent protection:

1. When load on the output exceeds overcurrent limit threshold $I_{SWOUTOCP}$, switch starts limiting the output voltage to decrease the output current. If the switch is in this condition for more than $t_{OCPDBSW}$, switch is automatically turned OFF, and *SWOUT_OCP* interrupt is generated.
2. In case output load exceeds I_{SWOUT_SH} threshold, switch turns OFF immediately to prevent boost overload, and *SWOUT_SH* interrupt is generated. Shortly after this action switch is re-enabled automatically with standard soft-on current limiting procedure. In case overload condition is still present, switch continues the operation in current limiting mode, and is finally switched OFF after $t_{OCPDBSW}$. In case overload condition is removed before $t_{OCPDBSW}$ switch continues its normal operation.

For a detailed behavior of the device on OCP event refer to Section 5.4.7 Overcurrent protection (OCP).

Output discharge – Switch implements a passive discharge circuit (by default disabled) that can be enabled by setting *SWOUT_PD* bit in Table 48. BST_SW_CR register.

SWOUT pin is bidirectional but does not support reverse current protection:

- Output: PWR_SW is turned ON (using *SW_ON* bit = ‘1’) only if SWIN voltage is higher than S_{WIN_Rise} threshold; else, PWR_SW keeps OFF. The SWIN rising and falling edge voltage (respectively V_{SWIN_Rise} / V_{SWIN_Fall} thresholds) can be monitored by sending interrupt to host processor.
- Input:
  - When PWR_SW is turned OFF (*SW_ON* bit = ‘0’), SWOUT pin monitors output voltage rising/falling by sending interrupts to host processor. See V_{SWOUT_Rise} / V_{SWOUT_Fall} thresholds
  - When the STPMIC1 is in OFF (PWR_SW is implicitely turned OFF), SWOUT pin monitors a rising voltage (*SWOUT_Rise threshold)* to generate power-up event. Refer to Section 5.4.2 Turn-ON conditions.
- PWR_SW has no reverse current protection voltage: SWIN should always be higher or equal to SWOUT voltage to avoid reverse current flowing from SWOUT to SWIN

If PWR_SW switch is used to supply USB port from Boost converter (SWIN pin connected to BSTOUT pin), then SWOUT_BOOST_OVP bit should be set in Table 70. NVM_LDOS_VOUT_SHR1 in order to automatically turn OFF PWR_SW and clear SW_ON *bit* in case of boost OVP event occur. Reciprocally, if PWR_SW is used as general-purpose power switch, SWOUT_BOOST_OVP bit should be clear in Table 70. NVM_LDOS_VOUT_SHR1 in order to ignore boost OVP event. Reference to Section 5.4.8 BOOST overvoltage protection.

Both of switches are controlled by *VBUSOTG_ON* / *SWOUT_ON* bit in Table 48. BST_SW_CR only. They are always turned OFF when the STPMIC1 goes to POWER_ON (no NVM bit option to turn ON switches at power-up) and are automatically turned OFF if the STPMIC1 POWER_DOWN.

Both of switches have a Pull_Down (PD) discharge resistor that is automatically enabled when switches are turned OFF. PD discharge resistor can be disabled on PWR_USB_SW and PWR_SW by setting respectively VBUSOTG_PD and SWOUT_PD bit in Table 48. BST_SW_CR register.

Both switches have overcurrent protection:

- Safety features, see Section 5.4.7 Overcurrent protection (OCP).
- An overcurrent detection can also be set as a turn-off condition – Section 5.4.7 Overcurrent protection (OCP).
- PWR_SW is selectable 500 mA/1000 mA power switch: overcurrent protection threshold is set by *SW_OCP* bit in Table 48. BST_SW_CR.

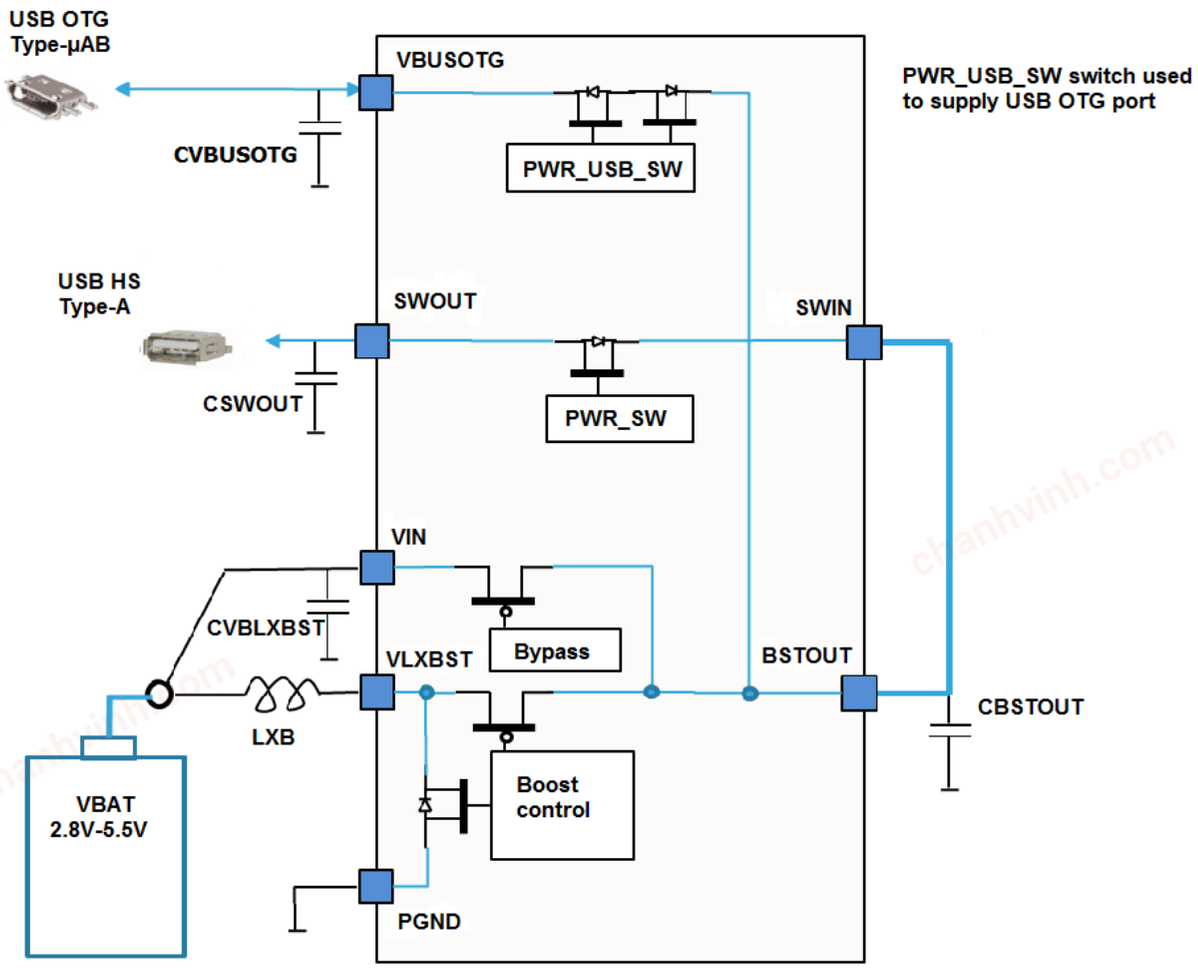
chanhvinh.com

PWR_USB_SW and PWR_SW switches (if *SW_BOOST_OVP* bit in Table 70. NVM_LDOS_VOUT_SHR1 is set) are also disabled and their enable bits are cleared in case of boost OVP event.

4.6 USB sub-system examples

The following Figure 50. Battery powered application with a USB OTG port and a USB host port, Figure 51. Battery powered application with a single USB OTG port , and Figure 52. 5 V DC powered application with a USB OTG port and two USB host ports show some typical USB sub-system configuration examples:

Figure 50. Battery powered application with a USB OTG port and a USB host port



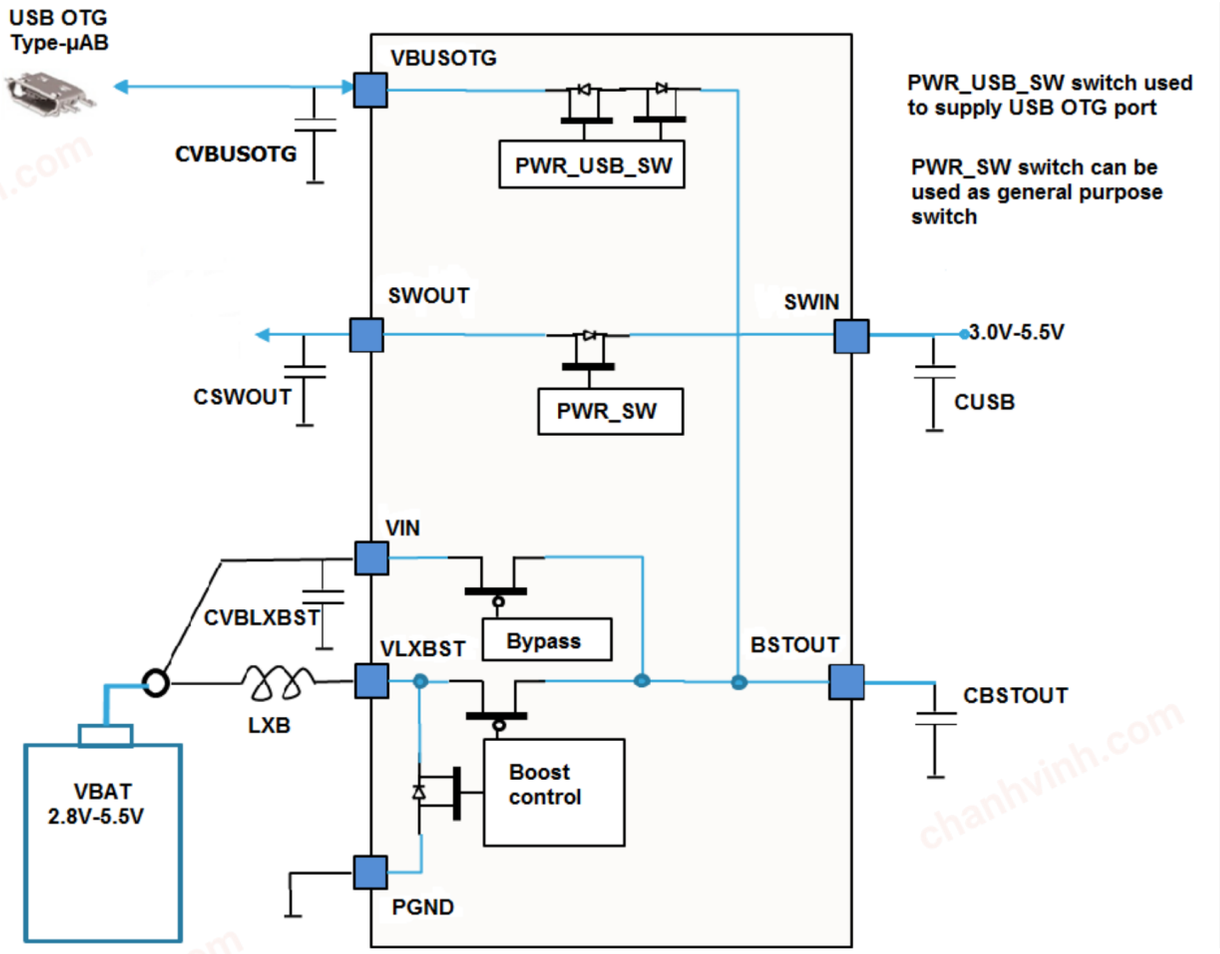
On this example, a battery supplies the boost converter. When enabled, the boost converter generates a 5.2 V on BSTOUT.

PWR_USB_SW output (VBUSOTG) is connected, in this example, to a USB Type-µAB connector (OTG). It can alternatively be connected to a USB Type-C connector.

PWR_SW output (SWOUT) is connected, in this example, to a USB Type-A connector (USB host only). PWR_SW input (SWIN) is connected to the output of boost converter (BSTOUT).

chanhvinh.com

Figure 51. **Battery powered application with a single USB OTG port**



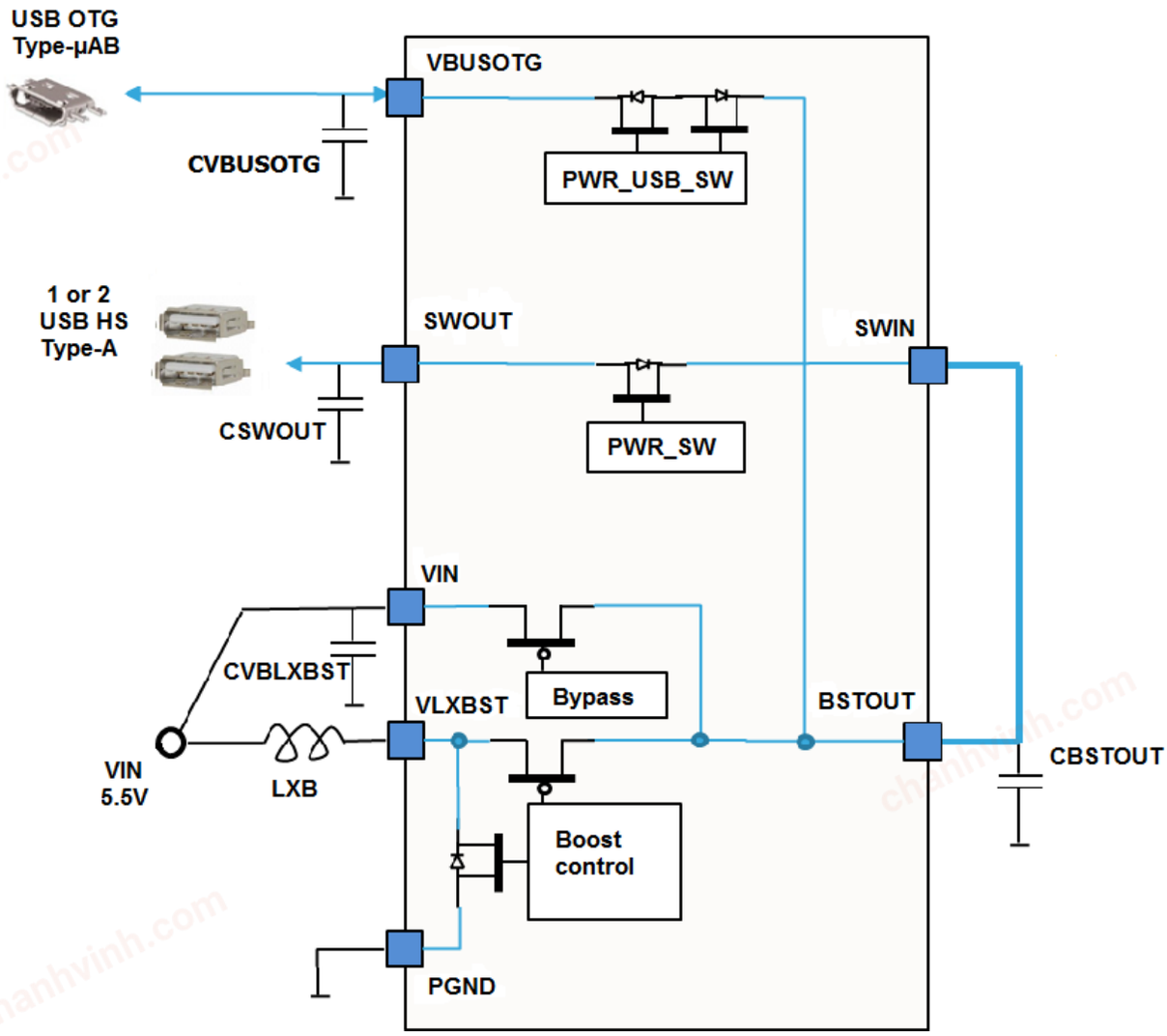
On this example, a battery supplies a boost converter. When enabled, the boost converter generates a 5.2 V on BSTOUT.

PWR_USB_SW output (VBUSOTG) is connected, in this example, to a USB Type-µAB connector (OTG). It can alternatively be connected to a USB Type-C connector.

PWR_SW can be used as general purpose power switch in the application. Note that PWR_SW is functional when SWIN is powered by VSWIN_Rise to 5.5 V.

chanhvinh.com

Figure 52. **5 V DC powered application with a USB OTG port and two USB host ports**



In this example, the application is powered by a 5 V DC power source (eg: from 5 V AC/DC wall adaptor) and it supplies a boost converter. When enabled, the boost converter generates a 5.2 V on BSTOUT.

PWR_USB_SW output (VBUSOTG) is connected, in this example, to a USB Type-µAB connector (OTG). It can alternatively be connected to a USB Type-C connector.

PWR_SW output (SWOUT) is connected, in this example, to one or two USB Type-A connectors (USB host only).

PWR_SW input (SWIN) is connected to the output of the boost converter (BSTOUT).

In this example, the boost is used to regulate VBUS voltage at 5.2 V (to be compatible with USB specification voltage range [4.75 V;5.5 V]) to compensate the power supply voltage losses (power supply voltage tolerance and load regulation lose on the printed circuit board).

chanhvinh.com

5 Functional description

5.1 Overview

The STPMIC1 integrates advanced low power features controlled by the application processor through I²C, 4 digital control pins (PONKEYn, WAKEUP, PWRCTRL and RSTn) and one interrupt output line (INTn).

The main parameter settings can be programmed in a non-volatile memory (NVM) as default values at start-up time.

See Section 5.5.2 Non-volatile memory (NVM)

The STPMIC1 offers 2 independent POWER_ON modes called MAIN and ALTERNATE. Switching between these modes is driven by the application processor through PWRCTRL pin.

This allow a flexible configuration and fast transition between two different power strategies at application level, typically RUN and STANDBY (LowPower).

Other features are provided to fulfill high-end application processors and advanced operating system needs:

- Multiple turn-on/turn-off conditions
- mask_default and restart_request options
- Overcurrent and overvoltage protection
- Thermal protection
- Watchdog
- Interrupt controller

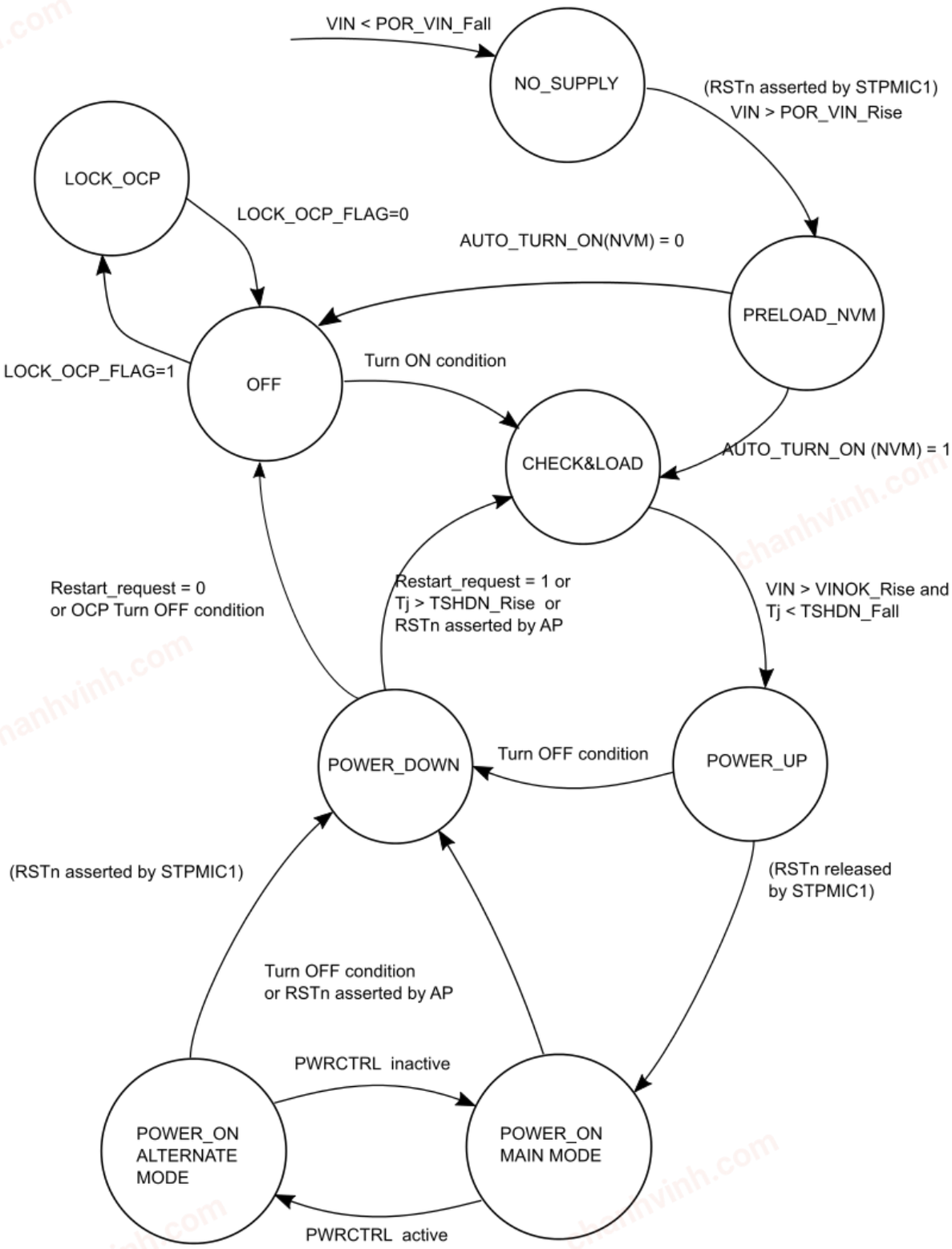
5.2 Functional state machine

The behavior of the STPMIC1 circuit is controlled by a state machine described in this section.

chanhvinh.com

5.2.1 Main state machine diagram

Figure 53. **STPMIC1 state machine**



chanhvinh.com

5.2.2 State explanations

NO_SUPPLY

VIN is below $V_{IN_POR_Fall}$ - see Section 5.4.1 VIN conditions and monitoring. No output state can be guaranteed in this state.

PRELOAD_NVM

State is immediately reached after VIN transition above $V_{IN_POR_Rise}$.

NVM download is performed in this state. (see Section 5.5.2 Non-volatile memory (NVM))

If automatic turn-on condition is set in NVM, AUTO_TURN_ON bit in Table 65. NVM_MAIN_CTRL_SHR, transition is made to CHECK&LOAD, else to OFF-state. Refer to Section 5.4.2 Turn-ON conditions.

RSTn is asserted by the STPMIC1 and all regulators are off.

OFF

State is entered after PRELOAD_NVM from POR_VIN, or when a turn-OFF condition occurs from POWER_ON.

Transition to CHECK&LOAD state is made of any turn-ON condition. Refer to Section 5.4.3 Turn-OFF conditions and restart_request.

RSTn is asserted by the STPMIC1 and all regulators are OFF.

LOCK_OCP

This state is an alternative to OFF-state in the context of overcurrent protection safety feature.

This state occurs if an overcurrent has been detected and LOCK_OCP bit has been set in Table 65. NVM_MAIN_CTRL_SHR register.

As soon as an overcurrent is detected from any regulator, the STPMIC1 immediately performs a POWER_DOWN sequence and goes permanently to LOCK_OCP state (passing through OFF-state). LOCK_OCP_FLAG internal bit is set to prevent state machine from leaving LOCK_OCP state.

LOCK_OCP_FLAG bit can only been reset by $V_{IN_POR_Fall}$ (removing application power supply source) and optionally by a PONKEYn long key press if PKEY_CLEAR_OCP_FLAG bit has been set in Table 31. PKEY_TURNOFF_CR.

Refer to Section 5.4.7 Overcurrent protection (OCP) for further details.

RSTn is assert by the STPMIC1 and all regulators are off.

CHECK&LOAD

This state is a combination of three initialization steps in this order:

- **CHECK_TEMP:** The STPMIC1 starts a thermal monitoring and control that junction temperature (T_j) is in functional range before going to next state. Refer to Section 5.4.6 Thermal protection.
- **LOAD_NVM:** The STPMIC1 performs a load of the NVM, initializing related registers to their default state.
- **CHECK_VIN:** The STPMIC1 starts VIN monitoring and control that the applied VIN is in functional range before going to next state. Refer to Section 5.4.1 VIN conditions and monitoring for details. RSTn is asserted by the STPMIC1 and all regulators are off.

POWER_UP

The STPMIC1 sequentially starts regulators following a rank procedure. Refer to Section 5.3 POWER_UP, POWER_DOWN sequence for detailed description. RSTn is asserted by the STPMIC1.

POWER_ON

RSTn is released and monitored (digital input) by the STPMIC1. RSTn signal can be driven externally by the application processor or a reset push-button.

The STPMIC1 delivers by default the power as per configuration in main mode, through Section 6.3.1 Main control register (MAIN_CR) registers of each regulator.

The STPMIC1 can optionally switch to ALTERNATE mode, controlled by the application processor through PWRCTRL pin. As described in Section 5.4.5 Power control modes (MAIN / ALTERNATE) for details.

The STPMIC1 exits POWER_ON state if:

- A turn-OFF condition occurs. See Section 5.4.3 Turn-OFF conditions and restart_request
- RSTn is asserted by the application processor. See Section 5.4.4 Reset and mask_reset option

POWER_DOWN

The STPMIC1 sequentially stops regulators following the rank procedure in reverse order than POWER_UP. Refer to Section 5.3 POWER_UP, POWER_DOWN sequence for a more detailed description.

chanhvinh.com

5.3 POWER_UP, POWER_DOWN sequence

The STPMIC1 starts and stops regulators following sequential rank procedures called respectively POWER_UP and POWER_DOWN.

During POWER_UP each regulator is started at one of the 4-rank phase programmed in NVM.

RANK0 means that the regulator is not started.

Default rank is defined:

For BUCKs: Section 6.7.2 NVM BUCK rank shadow register (NVM_BUCKS_RANK_SHR)

For LDO1, 2, 3, 4: Section 6.7.3 NVM LDOs rank shadow register 1 (NVM_LDOS_RANK_SHR1)

For LDO5, 6, REFDDR: Section 6.7.4 NVM LDOs rank shadow register 2 (NVM_LDOS_RANK_SHR2)

Default voltage is defined:

For BUCKs: Section 6.7.5 NVM BUCKs voltage output shadow register (NVM_BUCKS_VOUT_SHR)

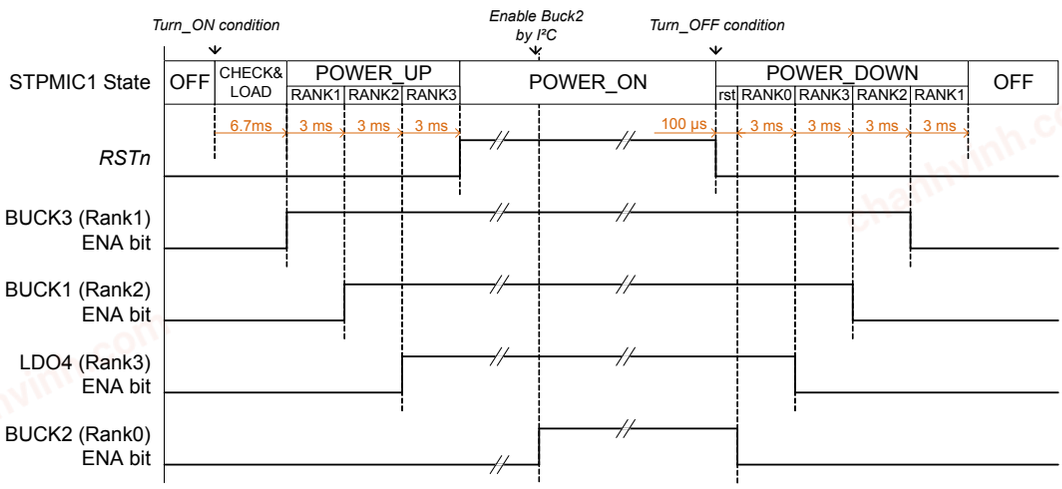
For LDO1, 2, 3, 4: Section 6.7.6 NVM LDOs voltage output shadow register 1 (NVM_LDOS_VOUT_SHR1

For LDO5, 6, REFDDR: Section 6.7.7 NVM LDOs voltage output shadow register 2 (NVM_LDOS_VOUT_SHR2)

During POWER_DOWN regulators are shutdown in reverse order than POWER_UP.

Figure 54. STPMIC1 POWER_UP and POWER_DOWN sequence example shows an example of power cycle.

Figure 54. STPMIC1 POWER_UP and POWER_DOWN sequence example



POWER_UP

The STPMIC1 enables regulators sequentially by 3 ms slots:

RANK1 (BUCK3) -> RANK2 (BUCK1) -> RANK3 (LDO4) regulators, this sequence example is related to the STPMIC1.

RANK0 regulators (eg BUCK2) are not started.

RSTn is asserted by the STPMIC1 until all regulators on. Then it deasserts RSTn and switches to POWER_ON as soon as RSTn is deasserted by the application processor (RSTn signal goes high).

POWER_ON:

Regulator state and output voltage are driven by settings to registers MAIN or ALTERNATE control registers.

Those registers are by default initialized with values programmed in NVM and can then be changed through I²C.

In the example, BUCK2 (RANK0) is enabled by I²C.

POWER_DOWN:

The STPMIC1 asserts RSTn and immediately shutdowns RANK0 regulators which may have been started by software. (BUCK2 in upon example).

Then it disables regulators sequentially in rank reverse order by 3 ms slots:

RANK3 (LDO4) -> RANK2 (BUCK1) -> RANK1 (BUCK3)

chanhvinh.com

The example above shows POWER_UP and POWER_DOWN procedure from digital point of view (ENA bit of each regulators); but not their respective output voltage (analog).

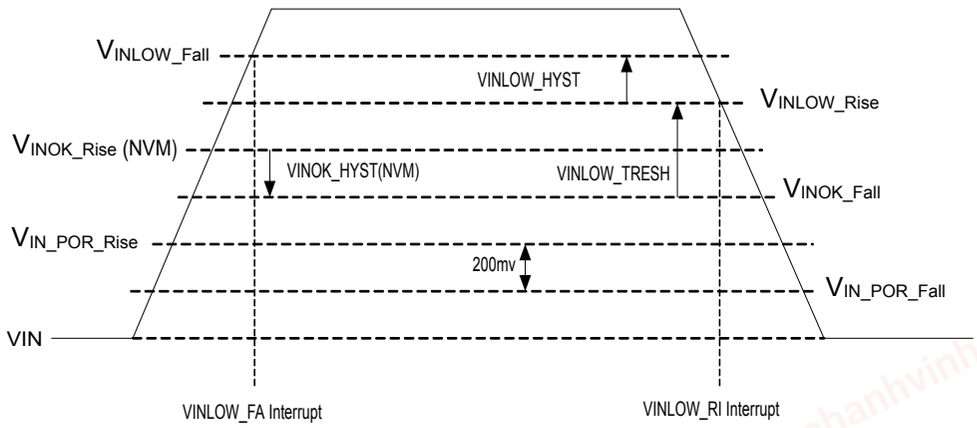
Regarding to analog behavior of each regulator, please refer to Section 4 Power regulators and switch description.

5.4 Feature description

5.4.1 VIN conditions and monitoring

Main input supply named VIN is monitored permanently by the STPMIC1 state machine. There are different threshold triggers on VIN. The lowest to the highest thresholds are: *POR_VIN, VINOK, VINLOW* as presented in the Figure 55. VIN monitoring thresholds.

Figure 55. VIN monitoring thresholds



POR_VIN

POR_VIN is the minimum voltage required to supply the STPMIC1 internal circuitry. It is specified by two hardcoded thresholds with 200 mv hysteresis:

- Below $V_{IN_POR_Fall}$ STPMIC1 is considered as not supplied
- Above $V_{IN_POR_Rise}$ STPMIC1 internal circuitry is functional

Refer to Section 3.4 Electrical and timing parameters for threshold value.

VIN_OK

VIN_OK is the minimal voltage required to allow the STPMIC1 to work in POWER_ON state.

It is specified by V_{INOK_Rise} threshold and V_{INOK_HYST} hysteresis values that can be adjusted in NVM, respectively by VINOK_TRESH[1:0] and VINOK_HYS[1:0] bits in Table 65. NVM_MAIN_CTRL_SHR.

- If VIN falls below V_{INOK_Fall} ($V_{INOK_Fall} = V_{INOK_Rise} – V_{INOK_HYST}$) then it is considered as a turn-OFF condition and the STPMIC1 immediately starts POWER_DOWN sequence. Refer to Section 5.4.3 Turn-OFF conditions and restart_request.
- If VIN rises above V_{INOK_Rise} then the STPMIC1 is allowed to go to POWER_ON state after a turn-ON condition has occurred. Refer to Section 5.4.2 Turn-ON conditions

VINLOW

VINLOW is an optional and configurable software threshold that can be setup to notify the application processor through interrupt, that a power shutdown, due to VIN going low, is a possible risk.

VINLOW can be enabled and configured by programming register Section 6.3.6 PWR_SWOUT and VIN control register (SW_VIN_CR).

VINLOW rising and falling thresholds are defined by a logical signal point of view. VINLOW signal goes to ‘1’ (rising edge) when VIN decreases V_{INLOW_Rise} threshold. VINLOW falling edge occurs when VIN goes above V_{INLOW_Fall} threshold.

chanhvinh.com

V_{INLOW_Rise} and V_{INLOW_Fall} detection generate respectively VINLOW_RI and VINLOW_FA interrupt in INT_PENDING_R4, allowing application processor to take relevant actions. They can be unmasked independently.

Refer to Section 6.5 Interrupt registers.

5.4.2 Turn-ON conditions

Turn-ON means the STPMIC1 reaches POWER_ON state from NO_SUPPLY or OFF-state.

The STPMIC1 is turned ON on four conditions.

Three conditions are triggered by an external stimulation:

- PONKEYn pin detection
- VBUS detection (voltage rising on VBUSOTG or SWOUT pins)
- WAKEUP pin detection

Last condition is triggered by AUTO turn-ON feature (see below).

When in POWER_ON, the last turn-ON condition is stored and can be read in Section 6.2.1 Turn-ON status register (TURN_ON_SR) register.

AUTO turn-ON

AUTO turn-ON feature allows the STPMIC1 to be turned ON automatically as soon as VIN rises above a valid voltage. See Section 5.4.1 VIN conditions and monitoring .

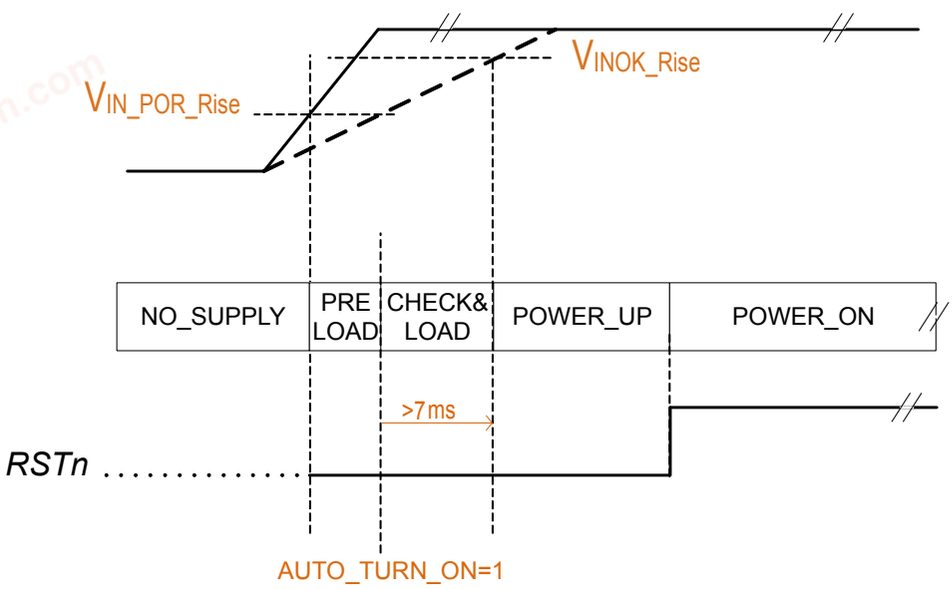
After VIN rises above V_{INOK_Rise}, the STPMIC1 goes to PRELOAD_NVM state and load AUTO_TURN_ON bit from NVM. If AUTO_TURN_ON is set, the STPMIC1 goes directly into CHECK&LOAD then goes to POWER_UP and to POWER_ON.

AUTO turn-ON event is triggered only by NO_SUPPLY state transition.

AUTO turn-ON is enabled by default in NVM and can be disabled by resetting AUTO_TURN_ON bit in Table 65. NVM_MAIN_CTRL_SHR register.

Details of the sequence are described in the Figure 56. Auto turn-on condition sequence.

Figure 56. Auto turn-on condition sequence



PONKEY/VBUS/WAKEUP detection

Those 3 conditions depend on stimulation on the specific STPMIC1 pins. The source and electrical characteristics of each condition are described in Table 11. Turn-on description.

chanhvinh.com

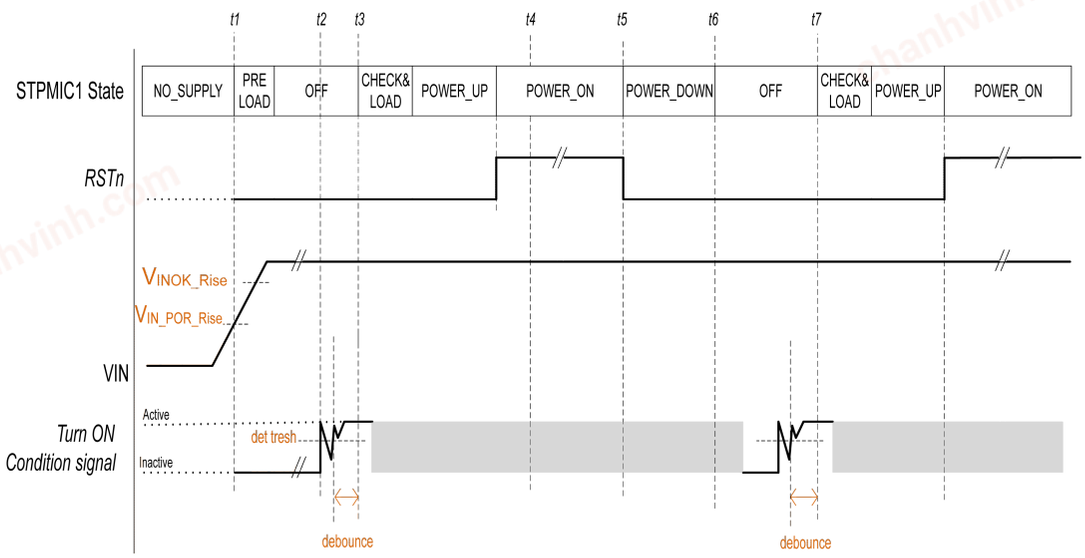
Table 11. Turn-on description

Name	Turn-ON condition source	Configuration	Active condition description	Debounce	Interrupt
PONKEY	PONKEYn pin	N/A	Active low	30 ms	PKEY_RI/PKEY_FA in INT_PENDING_R1
VBUS (VBUSOTG)	VBUSOTG pin	Can be disable by settingVBUSOTG_DET_DIS bit in Table 48. BST_SW_CR	VBUSOTG > VBUSOTG_Rise	30 ms	VBUSOTG_RI/ VBUSOTG_FA in INT_PENDING_R1
VBUS (SWOUT)	SWOUT pin	Can be disable by setting SWOUT_DET_DIS bit in Table 30. SW_VIN_CR	SWOUT > SWOUT_Rise	30 ms	SWOUT_RI/ SWOUT_FA in INT_PENDING_R1
WAKEUP	WAKEUP pin	N/A	Active high	No debounce	WKP_RI/WKP_FA in INT_PENDING_R1

The STPMIC1 manages 2 different scenarios depending if the turn-ON condition is active before or after VIN rises above $V_{IN_POR_Rise}$.

Active Turn-ON condition after VIN rises above $V_{IN_POR_Rise}$ sequence is presented in Figure 57. Turn-on condition after $V_{IN_POR_RISE}$.

Figure 57. Turn-on condition after $V_{IN_POR_RISE}$



t1: VIN rises above $V_{IN_POR_Rise}$ while no turn-ON condition is detected active. The STPMIC1 performs the PRELOAD_NVM and swiches to OFF-state.

t2: the STPMIC1 starts detecting the activity on turn-ON condition but the detection threshold above is not stable.

t3: turn-ON signal has been detected stable longer than debounce time. Turn-ON event triggered. Switch to CHECK&LOAD then POWER_UP as VIN > V_{INOK_Rise}.

t3 to t4: turn-ON conditions are ignored from CHECK&LOAD to POWER_ON.

t4: turn-ON condition is ignored and does not affect the usual STPMIC1 behavior in POWER_ON. (Except PONKEY long key press. See Section 5.4.3 Turn-OFF conditions and restart_request). Active turn-ON signal does not prevent from POWER_DOWN.

t5: active turn-OFF condition event occurs from a valid source. Switch to POWER_DOWN.

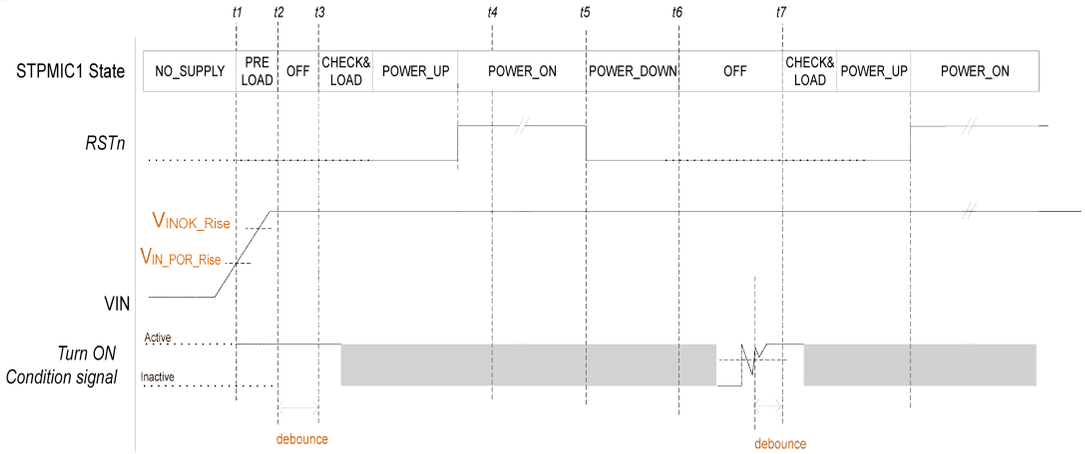
t5 to t6: active turn-ON during POWER_DOWN is ignored.

chanhvinh.com

t7: New turn-ON signal rising edge has been detected after debounce time. A valid turn-ON condition is detected. The STPMIC1 switches to POWER_UP.

Active turn-ON condition before VIN rises above $V_{IN_POR_Rise}$ sequence is presented in Figure 58. Turn-on condition before $V_{IN_POR_Rise}$.

Figure 58. Turn-on condition before $V_{IN_POR_Rise}$



t1: VIN rises above $V_{IN_POR_RISE}$ while a turn-ON condition is detected active. The STPMIC1 performs the PRELOAD_NVM and swiches to OFF-state.

t2: the STPMIC1 starts debounce as soon as it is entered OFF-state.

t3: turn-ON condition is confirmed after debounce time. Switch to CHECK&LOAD then POWER_UP as VIN > V_{INOK_Rise}.

t3 to t4: turn-ON conditions are ignored from CHECK&LOAD to POWER_ON.

t4: turn-ON condition is ignored and does not affect usual STPMIC1 behavior in POWER_ON. (Except PONKEY long key press. See Section 5.4.3 Turn-OFF conditions and restart_request)

Active turn-ON signal does not prevent from POWER_DOWN.

t5: active turn-OFF condition event occurs from a valid source. Switch to POWER_DOWN.

t5 to t6: Active turn-ON during POWER_DOWN is ignored.

t7: New turn-ON signal rising edge has been detected after debounce time. Valid turn-ON condition detected. The STPMIC1 switches to POWER_UP.

5.4.3 Turn-OFF conditions and restart_request

Turn-OFF conditions are events or stimulus leading the STPMIC1 to go to OFF-state from a POWER_ON state, by switching through a POWER_DOWN sequence.

The STPMIC1 is turned OFF by six conditions presented in Table 12. Turn-off conditions.

Some turn-OFF conditions support *restart_request* option that allows the STPMIC1 to perform a power cycle back to POWER_ON instead of going to off-state (POWER_DOWN/CHECK&LOAD/POWER_UP) without waiting for a valid turn-ON condition restarts.

Turn-OFF condition with restart_request option has a similar behavior as a reset power cycle except that mask_reset option is ignored. Refer to Section 5.4.4 Reset and mask_reset option

restart_request option can be enabled by setting RREQ_EN bit in Table 25. MAIN_CR register, prior to turn-OFF condition occurrence.

Table 12. Turn-off conditions

Name	Conditions	Power cycle if RREQ_EN=1
Software switch-OFF	Writing 1 to SWOFF bit in Table 25. MAIN_CR register	YES

chanhvinh.com

Name	Conditions	Power cycle if RREQ_EN=1
PONKEYn long key press	PKEYLKP bit set in Table 31. PKEY_TURNOFF_CR Default value loaded by PKEYLKP_OFF bit in Table 65. NVM_MAIN_CTRL_SHR Request duration for the long key press defined in PKEY_LKP_TMR[3:0] in Table 31. PKEY_TURNOFF_CR PONKEYn signal is asserted for a duration > PKEY_LKP_TMR[3:0]	YES
Thermal shutdown	STPMIC1 functional temperature is exceeded. Refer to Section 5.4.6 Thermal protection	STPMIC1 always restart automatically whatever restart_request option.
Overcurrent protection	STPMIC1 detects overcurrent on a regulator. Refer to Section 5.4.7 Overcurrent protection (OCP)	NO
Watchdog	Watchdog feature active and downcounter reach 0. Refer to Section 5.4.9 Watchdog feature	YES
VIN_OK_Fall	VIN falls down under VIN_OK_Fall threshold. Depending on VIN decrease speed, proper execution of POWER_DOWN operation is not guaranteed	YES only if VIN remains above POR_VIN_Fall

Last turn-OFF condition is stored in Table 20. TURN_OFF_SR.

If *restart_request* is set, power cycle source is stored in Table 23. RESTART_SR register.

5.4.4 Reset and mask_reset option

RSTn is bidirectional reset pin both for the STPMIC1 and the application processor. It is digital input / open drain output topology with internal pull-up resistor.

- When the STPMIC1 asserts RSTn, it drives RSTn signal low (open drain internal transistor). Application processor is forced in reset state
- When the STPMIC1 does not assert RSTn, RSTn pin is in high impedance and RSTn signal goes high (thanks to pull-up resistor) if RSTn signal is not asserted low externally (eg: by a reset push button or from application processor asserting the reset signal low). In that case, the STPMIC1 RSTn pin becomes digital input and it monitors RSTn signal

In POWER_ON state, RSTn pin can be driven by the application processor or a reset push-button.

If the application processor asserts RSTn low more than RSTnDB duration, it triggers immediately a reset sequence of the STPMIC1 by performing a non-interruptible power cycle:

1. The STPMIC1 asserts RSTn low (forcing AP to keep it in case reset is deasserted by AP)
2. POWER_DOWN sequence
3. LOAD&CHECK
4. POWER_UP sequence
5. STPMIC1 deasserts RSTn and monitor RSTn
6. STPMIC1 waits for RSTn signal going high before entering POWER_ON. (To prevent infinite loop of reset sequence)

LDOs and Bucks follow POWER_DOWN / POWER_UP power cycle from leave state to default one, except if mask_reset option is specified.

mask_reset option can be defined for each regulator by setting the corresponding MRST bit in corresponding MRST_CR register.

Eg for BUCK3 : MRST_BUCK3 in Table 32. BUCKS_MRST_CR.

When mask_reset option is set by a regulator, it means that MAIN and ALTERNATE related register do not change during and after the reset power cycle:

- POWER_DOWN is not performed
- MAIN and ALTERNATE register values are not reloaded by NVM and are not reset

The STPMIC1 always ends the power cycle in POWER_ON MAIN mode. (PWRCTRL pin configuration reset).

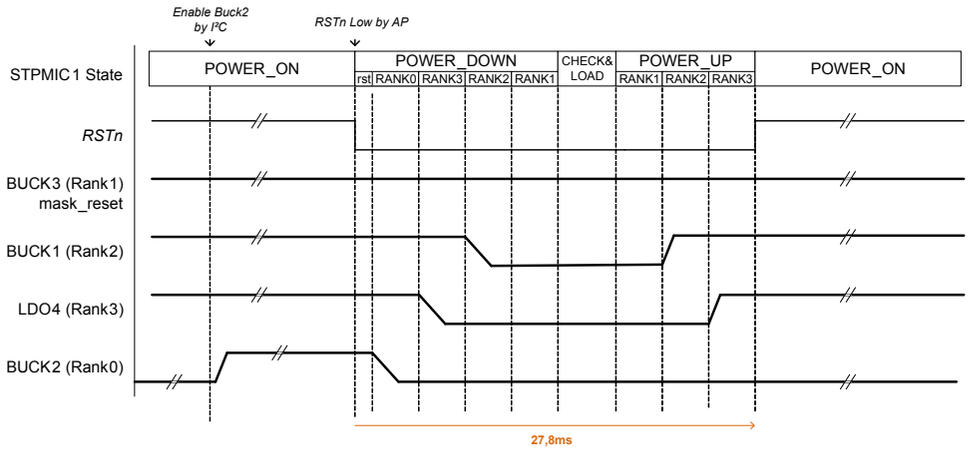
chanhvinh.com

If reset happens in MAIN mode, the regulator is not impacted at all, keeping VOUT, ENA and PREG_MODE unchanged.

In case reset happens in ALTERNATE mode, VOUT, ENA and PREG_MODE switch to content of the [regulator]_MAIN_CR register values.

Figure 59. Reset power-cycle sequence below shows an example of a reset power-cycle on the STPMIC1.

Figure 59. Reset power-cycle sequence



mask_reset is a single shot option, cleared by Turn-OFF, POR_VIN and reset.

BUCK3 with mask_reset option set, is not impacted by reset power-cycle.

BUCK1 and LDO4 are powered down and up at their respective rank defined in NVM.

BUCK2, enabled by I^2C is power down but not restarted.

5.4.5 Power control modes (MAIN / ALTERNATE)

In order to address implementation of low power platform, the STPMIC1 supports two independent and configurable modes for POWER_ON state. For all regulators, settings enable (ENA), output voltage (VOUT) and regulation mode (PREG_MODE) can be defined for each mode. With the following exceptions due to some regulator specificities:

- REFDDR provides ENA only
- LDO3 also provides BYPASS mode bit
- LDO4 also provides input source selector bits

Default MAIN mode has to be applied to full load applications, typically RUN mode of application processor. ALTERNATE mode has to be used when the application processor enters low power mode, typically STANDBY mode. Switch between MAIN and ALTERNATE, can be controlled by the application processor through PWRCTRL pin.

- MAIN mode corresponds to “inactive state” of PWRCTRL pin
- ALTERNATE mode corresponds to “active state” of PWRCTRL pin

PWRCTRL pin detection can be enabled and its polarity configured through respectively PWRCTRL_EN and PWRCTRL_POL bits in Table 25. MAIN_CR register.

PWRCTRL pin detection is always disabled by default (PWRCTRL_EN bit clear by turn-OFF and reset), as a consequence POWER_ON mode is always MAIN by default.

In each mode, MAIN or ALTERNATE, the STPMIC1 applies the settings indicated in the regulator (Rx) related register, [Rx]_MAIN_CR for MAIN and [Rx]_ALT_CR, for ALTERNATE.

If Buck converter has different output voltage settings between MAIN and ALTERNATE register, a smooth voltage transition is applied during MAIN to ALTERNATE (and reciprocally) as described in Figure 47. BUCKx dynamic voltage scaling (DVS).

Please refer to Section 4 Power regulators and switch description for details on voltage scale up and down procedure for each regulator and switche.

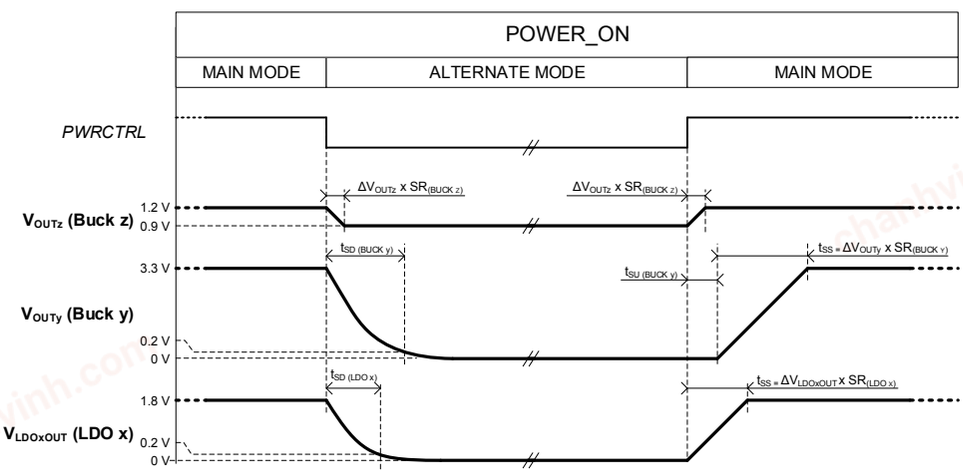
chanhvinh.com

Figure 60. Power mode switch sequence example is an example of the STPMIC1 transition with settings available in Table 13. MAIN/ALTERNATE switch example configuration and where PWRCTRL is set as active low.

Table 13. MAIN/ALTERNATE switch example configuration

Regulator	MAIN setting	ALTERNATE setting	Register value
BUCKz(z=1..4)	ENA=1 VOUT=1.2 V, PREG_MODE=HP	ENA=1 VOUT=0.9 V PREG_MODE=LP	BUCKx_MAIN_CR=0x61 BUCKx_ALT_CR=0x33
BUCKy(y=1..4)	ENA=1 VOUT=3.3 V PREG_MODE=HP	ENA=0, VOUT=3.3 V PREG_MODE=HP	BUCKy_MAIN_CR=0xD9 BUCKy_ALT_CR=0xD8(or 0x00)
LDOx(x=1,2,5,6)	ENA=1 VOUT=1.8	ENA=0 VOUT=1.8	LDOx_MAIN_CR=0x27 LDOx_ALT_CR=0x26 (or 0x00)

Figure 60. Power mode switch sequence example



5.4.6 Thermal protection

The STPMIC1 implements a thermal protection to prevent over heating damage.

Junction temperature is permanently monitored thanks to an embed cell.

Protection consists of 2 thresholds :

- Thermal shutdown threshold (T_{SHDN}), which turns off the STPMIC1
- Thermal warning threshold (T_{WRN}), which generates an interrupt to be handled by the application processor

Figure 61. Thermal protection thresholds represents the distribution of those thresholds along the temperature curve.

When the temperature rises above T_{SHDN_Rise}, the STPMIC1 starts a rank down and goes to CHECK&LOAD state.

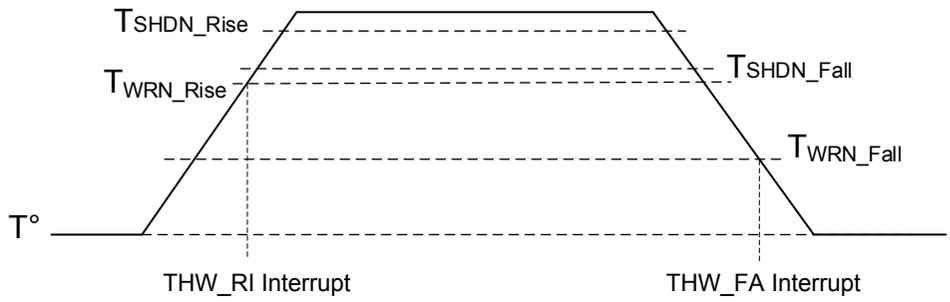
If temperature decreases and comes back lower than T_{SHDN_Fall}, the STPMIC1 restarts automatically with POWER_UP sequence.

In order to allow the application processor to anticipate T_{SHDN_Rise} shutdown and take relevant actions, interrupts THW_RI and THW_FA are generated when the temperature rises above T_{WRN_Rise} and falls down T_{WRN_Fall}.

Refer to Section 6.5 Interrupt registers about the interruption management.

chanhvinh.com

Figure 61. **Thermal protection thresholds**



5.4.7 Overcurrent protection (OCP)

The STPMIC1 implements protection against short-circuit (SC) or overcurrent (OC) on all regulators output.
The STPMIC1 supports 3 levels of protection described in Table 14. OCP levels below.

Table 14. **OCP levels**

Protection level	LOCK_OCP (NVM)	OCPOFF [Rx] bit	STPMIC1 behavior
Level 0	0	0	This is the default mode. When SC/OC occurs on regulator *Rx* : • **For LDOs and bucks**: if current rises above defined tresholds, an automatic current limitation is activated. Refer to Section 4.2 LDO regulators and Section 4.4.1 BUCK general description for details • **For BOOST** refer to Section 4.5.1 Boost converter • **For switches**: Refer to PWR_USB_SW and PWR_SW power switches *Note:* In case of a sharp increase of the current, the boost overcurrent protection may react earlier than switch. • **For all**: all interrupts are generated by setting corresponding [Rx]_OCP bit of INT_PENDING_R2 or INT_PENDING_R3. (see Section 6.5 Interrupt registers) The STPMIC1 is in **POWER_ON state**.
Level 1	0	1	By setting OCPOFF[Rx] bit Section 6.3.12 Bucks OCP turn-OFF control register (BUCKS_OCPOFF_CR) or Section 6.3.13 LDO OCP turn-OFF control register (LDOS_OCPOFF_CR) registers, an OC on related *Rx* becomes a turn-OFF condition. (see Section 5.4.3 Turn-OFF conditions and restart_request The STPMIC1 starts a **POWER_DOWN** sequence. RREQ_EN bit is ignored in case OCP turn-OFF. The STPMIC1 is in OFF-state until a valid turn-ON condition. Regulator that caused the OCP turn-OFF can be identified with a corresponding bit set in overcurrent protection LDO turn-OFF status register (Section 6.2.3 Overcurrent protection LDO turn-OFF status register (OCP_LDOS_SR)) or Section 6.2.4 Overcurrent protection buck turn-OFF status register (OCP_BUCKS_BSW_SR)
Level 2	1	x	NVM_LOCK_OCP (Section 6.7.1 NVM main control shadow register (NVM_MAIN_CTRL_SHR) bit 0) is set. This level 2 concerns all regulators. OCPOFF[Rx] bits are ignored. If SC/OC occurs on any regulators, the STPMIC1 enters POWER_DOWN to finally goes into **LOCK_OCP state**

chanhvinh.com

Protection level	LOCK_OCP (NVM)	OCPOFF [Rx] bit	STPMIC1 behavior
			The STPMIC1 is kept forced in LOCK_OCP state (see Figure 53. STPMIC1 state machine) until internal LOCK_OCP_FLAG is released by $V_{IN_POR_Fall}$ or optionally by PONKEYn long key press, if enabled by setting PKEY_CLEAR_OCP_FLAG bit in Table 31. PKEY_TURNOFF_CR register

5.4.8 BOOST overvoltage protection

See Section 4.5.1 Boost converter.

5.4.9 Watchdog feature

The STPMIC1 offers a watchdog mechanism that triggers a turn-OFF condition when the watchdog down counter elapses.

Watchdog is disabled by default and it is enabled if WDG_ENA bit is set in Section 6.3.10 Watchdog control register (WDG_CR).

The watchdog timer downcounter can be set in a range from 1 s to 256 s by 1 s step in Section 6.3.11 Watchdog timer control register (WDG_TMR_CR).

Watchdog counter is reset by setting WDG_RST bit in Section 6.3.10 Watchdog control register (WDG_CR) and when setting WDG_ENA from 0 to 1.

When enabled the watchdog timer remains active regardless MAIN or ALTERNATE mode. Watchdog is disabled by reset, $V_{IN_POR_Fall}$ and turn-OFF.

5.5 Programming

5.5.1 I²C interface

I²C interface works in slave mode. It supports both standard and fast mode with data rate up to 400Kb/s. It supports also fast mode plus (FM+) with data rate up to 1Mb/s that is suitable frequency for DVS operations. Please refer to NXP UM10204 revision 5 for specifications.

SCL pin is the input clock used to shift data. SDA pin is the input/output bi-directional data.

Device ID

There is a device ID system to address the STPMIC1.

The address is stored into NVM_I2C_ADDR[6:0] bits in Section 6.7.8 NVM device address shadow register (I2C_ADDR_SHR). Default address is 0x33.

Table 15. Device ID format

b7	b6	b5	b4	b3	b2	b1	b0
AdrID6	AdrID5	AdrID4	AdrID3	AdrID2	AdrID1	AdrID0	R/W

Read/write operation

Each transaction is composed of a start condition followed by a number of packet number (8-bit long) representing either a device ID plus R/W command or register address or register data coming to/from slave Table 15. Device ID format. An acknowledgment is needed after each packet. This acknowledgment is given by the receiver of the packet. Transaction examples are given in Table 16. Register address format and Table 17. Register data format. Multi read and multi write operations are supported.

Table 16. Register address format

b7	b6	b5	b4	b3	b2	b1	b0
RegADR7	RegADR6	RegADR5	RegADR4	RegADR3	RegADR2	RegADR1	RegADR0

chanhvinh.com

Table 17. **Register data format**

b7	b6	b5	b4	b3	b2	b1	b0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 62. **I²C read operation**

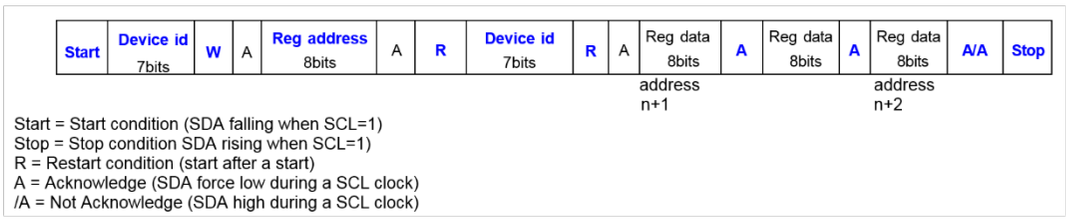
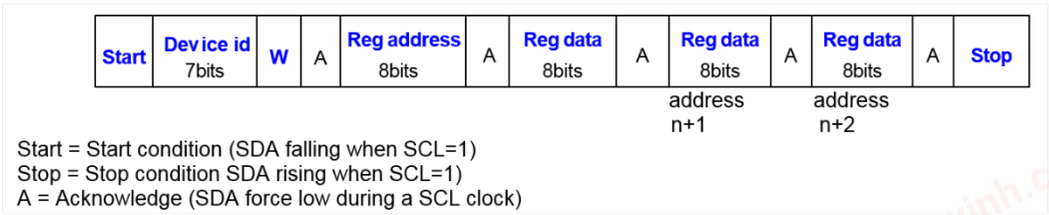


Figure 63. **I²C write operation**



5.5.2 Non-volatile memory (NVM)

General description

The STPMIC1 built-in non-volatile memory provides a high flexibility to support a wide range of applications:

Its straightforward write management through I²C allows customizing the STPMIC1 directly in final applications during the product development and mass production.

The NVM is composed of 64 bits customizable parameters (accessible from shadow registers):

- BUCKs and LDOs regulators:
  - Output voltage: to set the default output voltage at POWER-UP
  - POWER-UP sequence order: RANK regulator starts
- General:
  - AUTO_TURN_ON: to power up the STPMIC1 automatically when the input voltage rises
  - V_{INOK_RISE} threshold voltage: to select right power-up voltage
  - V_{INOK_HYST} hysteresis voltage: to trigger power-down in case of VIN drop
  - LOCK_OCP: overcurrent protection bit that blocks the STPMIC1 in LOCK_OCP state in case of short-circuit or overload detection
  - PONKEY long key press functionality – can be configured to reset device
  - I²C slave address

NVM read operation is performed automatically before each POWER_UP sequence to set control registers with default values and configure POWER_UP and POWER_DOWN sequence.

NVM write operation can be performed several times at product level to:

1. Customize a pre-programmed device directly from application host processor via I²C interface (STPMIC1A,STPMIC1B, STPMIC1D and STPMIC1E)
2. To program a non-programmed device (STPMIC1C) into a final application by connecting a I²C host programmer to the product via JIG tester

chanhvinh.com

NVM macrocell is designed to provide high reliability: it is composed of complementary memory approach with two cells per bit (one direct cell and one complementary cell) and during each read operation, NVM controller check NVM content integrity. If integrity check fails, the STPMIC1 does not start up.

NVM read operation

NVM read operation is fully managed by the STPMIC1.

For each read operation, the STPMIC1 automatically loads the 64-bit NVM content into NVM shadow registers (see Table 64. NVM shadow register map). It means that shadow register content is a copy of NVM content.

When the STPMIC1 power supply is connected (V_{IN} > $V_{POR_VIN_Rise}$), the STPMIC1 state machine goes to PRELOAD_NVM state (see Section 5.2 Functional state machine). In this state, a NVM read operation is performed to check if the STPMIC1 should start up automatically depending on AUTO_TURN_ON NVM bit value. If AUTO_TURN_ON bit is not set, the STPMIC1 goes to OFF-state; else the STPMIC1 continues automatically by power-up procedure.

Before each POWER_UP procedure, NVM read operation is performed in CHECK&LOAD state. NVM content is loaded into shadow registers. Additionally, the STPMIC1 initializes BUCK and LDO control registers with values pre-defined in NVM (see Table 64. NVM shadow register map) and configure POWER_UP and POWER_DOWN sequence of regulators.

NVM write operation (STPMIC1 customization)

NVM write operation can be performed multiple times (see NVM_{END}) by I^2C interface.

NVM write operation generic sequence:

1. Apply VIN to the application: STPMIC1 goes to POWER_ON state(1)
2. Write NVM shadow registers with expected customization values
3. Initiate a “NVM program operation” command - write NVM_CMD[1:0] = ‘01’ in Section 6.6.2 NVM control register (NVM_CR)
4. Wait for NVM write operation to be completed: wait for NVM_BUSY becomes 0 in Table 62. NVM_SR
5. (Optional): check new NVM content by initiating a NVM read operation: write NVM_CMD[1:0] = ‘10’ and wait for NVM_BUSY becomes 0

1. *The STPMIC1 has AUTO_TURN_ON bit set by default to power up automatically. This is to allow NVM write operation without generating turn-ON conditions.*

The following conditions should be fulfilled to allow NVM write operation:

- VIN must be minimum 3.8 V
- The STPMIC1 must be in POWER_ON state (NVM write operation is ignored in OFF-state)

Writing into NVM shadow registers does not affect NVM content until NVM write operation is executed.

WARNING: If V_{IN} goes below 3.8 V during write operation, NVM content integrity may be corrupted and the STPMIC1 may not start up anymore.

Change of I^2C address

Special attention must be given when new I^2C address needs to be programmed.

When different I^2C address is written in Section 6.7.8 NVM device address shadow register (I2C_ADDR_SHR), this new address becomes effective immediately and next I^2C transaction must already use this new device address.

If a “NVM write operation” is not performed following I^2C address change in shadow register, previously programmed I^2C address is loaded from NVM during next POWER_UP sequence.

chanhvinh.com

6 Register description

6.1 User register map

Registers are all default down to 0 at $V_{IN_POR_Fall}$.

Default value in the table below represents values at POWER_ON when application processor can access I^2C registers.

Value ‘x’ represents:

- Read/write bits loaded by NVM
- Read bit status depending on previous operation or event

It is important to highlight that all bits marked "reserved" (-) must be written 0 (reset value). So a read / modify / write operation into a register is allowed if "reserved" bits are not modified.

Table 18. Register map

@HEX	Register name	R/W	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
01	TURN_ON_SR	R	8'b000x_xxxx	-	-	-	AUTO	SWOUT	VBUS	WKUP	PKEY
				0	0	0	x	x	x	x	x
02	TURN_OFF_SR	R	8'b000x_xxxx	-	-	PKEYLKP	WDG	OCP	THSD	VINOK_FA	SWOFF
				0	0	x	x	x	x	x	x
03	OCP_LDOS_SR	R	8'b00xx_xxxx	-	-	OCP_LDO6	OCP_LDO5	OCP_LDO4	OCP_LDO3	OCP_LDO2	OCP_LDO1
				0	0	x	x	x	x	x	x
04	OCP_BUCKS_BSW_SR	R	8'b00xx_xxxx	-	OCP_BOOST	OCP_SWOUT	OCP_VBUSOTG	OCP_BUCK4	OCP_BUCK3	OCP_BUCK2	OCP_BUCK1
				0	0	x	x	x	x	x	x
05	RESTART_SR	R	8'b000x_xxxx	OP_MODE	LDO4_IS[1:0]		VINOK_FA	PKEYLKP	WDG	SWOFF	RST
				0	0	0	x	x	x	x	x
06	VERSION_SR	R	8'b0010_0000	MAJOR_VERSION[3:0]				MINOR_VERSION[3:0]			
				0	0	1	0	0	0	0	1
10	MAIN_CR	R/W	8'b0000_0000	-	-	-	OCP_OFF_DBG	PWRCTRL_POL	PWRCTRL_EN	RREQ_EN	SWOFF
				0	0	0	0	0	0	0	0
11	PADS_PULL_CR	R/W	8'b0000_0000	-	-	-	WKUP_EN	PWRCTRL_PD	PWRCTRL_PU	WKUP_PD	PKEY_PU
				0	0	0	0	0	0	0	0
12	BUCKS_PD_CR	R/W	8'b0000_0000	BUCK4_PD[1:0]		BUCK3_PD[1:0]		BUCK2_PD[1:0]		BUCK1_PD[1:0]	
				0	0	0	0	0	0	0	0
13	LDO14_PD_CR	R/W	8'b0000_0000	LDO4_PD[1:0]		LDO3_PD[1:0]		LDO2_PD[1:0]		LDO1_PD[1:0]	
				0	0	0	0	0	0	0	0
14	LDO56_VREF_PD_CR	R/W	8'b0000_0000	-	BST_PD	VREF_PD[1:0]		LDO6_PD[1:0]		LDO5_PD[1:0]	
				0	0	0	0	0	0	0	0
15	SW_VIN_CR	R/W	8'b0000_0000	SWIN_DET_EN	SWOUT_DET_DIS	VINLOW_HYST[1:0]		VINLOW_TRESH[2:0]			VINLOW_MON
				0	0	0	0	0	0	0	0
16	PKEY_TURNOFF_CR	R/W	8'bx000_0000	PKEY_LKP_OFF	PKEY_CLEAR_OCP	-	-	PKEY_LKP_TMR[3:0]			
				x	0	0	0	0	0	0	0

chanhvinh.com

@HEX	Register name	R/W	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
18	BUCKS_MRST_CR	R/W	8'b0000_0000	-	-	-	-	MRST_BUCK4	MRST_BUCK3	MRST_BUCK2	MRST_BUCK1
				0	0	0	0	0	0	0	0
1A	LDOS_MRST_CR	R/W	8'b0000_0000	-	MRST_REFDDR	MRST_LDO6	MRST_LDO5	MRST_LDO4	MRST_LDO3	MRST_LDO2	MRST_LDO1
				0	0	0	0	0	0	0	0
1B	WDG_CR	R/W	8'b0000_0000	-	-	-	-	-	-	WDG_RST	WDG_ENA
				0	0	0	0	0	0	0	0
1C	WDG_TMR_CR	R/W	8'b0000_0000	WDG_TMR[7:0]							
				0	0	0	0	0	0	0	0
1D	BUCKS_OCPOFF_CR	R/W	8'b0000_0000	-	OCPOFFBOOST	OCPOFFSWOUT	OCPOFFVBUSOTG	OCPOFFBUCK4	OCPOFFBUCK3	OCPOFFBUCK2	OCPOFFBUCK1
				0	0	0	0	0	0	0	0
1E	LDOS_OCPOFF_CR	R/W	8'b0000_0000	-	-	OCPOFFLDO6	OCPOFFLDO5	OCPOFFLDO4	OCPOFFLDO3	OCPOFFLDO2	OCPOFFLDO1
				0	0	0	0	0	0	0	0
20	BUCK1_MAIN_CR	R/W	8'bxxxx_xx0x	VOUT[5:0]						PREG_MODE	ENA
				x	x	x	x	x	x	0	x
21	BUCK2_MAIN_CR	R/W	8'bxxxx_xx0x	VOUT[5:0]						PREG_MODE	ENA
				x	x	x	x	x	x	0	x
22	BUCK3_MAIN_CR	R/W	8'bxxxx_xx0x	VOUT[5:0]						PREG_MODE	ENA
				x	x	x	x	x	x	0	x
23	BUCK4_MAIN_CR	R/W	8'bxxxx_xx0x	VOUT[5:0]						PREG_MODE	ENA
				x	x	x	x	x	x	0	x
24	REFDDR_MAIN_CR	R/W	8'b0000_000x	-	-	-	-	-	-	-	ENA
				0	0	0	0	0	0	0	x
25	LDO1_MAIN_CR	R/W	8'b0xxx_xx0x	-	VOUT[4:0]					-	ENA
				0	x	x	x	x	x	0	x
26	LDO2_MAIN_CR	R/W	8'b0xxx_xx0x	-	VOUT[4:0]					-	ENA

chanhvinh.com

@HEX	Register name	R/W	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
26	LDO2_MAIN_CR	R/W	8'b0xxx_xx0x	0	0	0	0	0	0	0	x
27	LDO3_MAIN_CR	R/W	8'b0xxx_xx0x	BYPASS	VOUT[4:0]					-	ENA
				0	0	0	0	0	0	0	x
28	LDO4_MAIN_CR	R/W	8'b0000_000x	-	-	-	SRC_VBUSOTG	SRC_BOOST	SRC_VIN	-	ENA
				0	0	0	0	0	0	0	x
29	LDO5_MAIN_CR	R/W	8'b0xxx_xx0x	-	VOUT[4:0]					-	ENA
				0	x	x	x	x	x	0	x
2A	LDO6_MAIN_CR	R/W	8'b0xxx_xx0x	-	VOUT[4:0]					-	ENA
				0	x	x	x	x	x	0	x
30	BUCK1_ALT_CR	R/W	8'bxxxx_xx0x	VOUT[5:0]						PREG_MODE	ENA
				x	x	x	x	x	x	0	x
31	BUCK2_ALT_CR	R/W	8'bxxxx_xx0x	VOUT[5:0]						PREG_MODE	ENA
				x	x	x	x	x	x	0	x
32	BUCK3_ALT_CR	R/W	8'bxxxx_xx0x	VOUT[5:0]						PREG_MODE	ENA
				x	x	x	x	x	x	0	x
33	BUCK4_ALT_CR	R/W	8'bxxxx_xx0x	VOUT[5:0]						PREG_MODE	ENA
				x	x	x	x	x	x	0	x
34	REFDDR_ALT_CR	R/W	8'b0000_000x	-	-	-	-	-	-	-	ENA
				0	0	0	0	0	0	0	x
35	LDO1_ALT_CR	R/W	8'b0xxx_xx0x	-	VOUT[4:0]					-	ENA
				0	x	x	x	x	x	0	x
36	LDO2_ALT_CR	R/W	8'b0xxx_xx0x	-	VOUT[4:0]					-	ENA
				0	x	x	x	x	x	0	x
37	LDO3_ALT_CR	R/W	8'b0xxx_xx0x	BYPASS	VOUT[4:0]					-	ENA
				0	x	x	x	x	x	0	x
38	LDO4_ALT_CR	R/W	8'b0000_000x	-	-	-	SRC_VBUSOTG	SRC_BOOST	SRC_VIN	-	ENA

chanhvinh.com

@HEX	Register name	R/W	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
38	LDO4_ALT_CR	R/W	8'b0000_000x	0	0	0	0	0	0	0	x
39	LDO5_MAIN_CR	R/W	8'b0xxx_xx0x	-	VOUT[4:0]					-	ENA
				0	x	x	x	x	x	0	x
3A	LDO6_MAIN_CR	R/W	8'b0xxx_xx0x	-	VOUT[4:0]					-	ENA
				0	x	x	x	x	x	0	x
40	BST_SW_CR	R/W	8'b0000_000x	BST_OVP_DIS	VBUSOTG_DET_DIS	SWOUT_PD	VBUSOTG_PD	OCP_SWOUT_LIM	SWOUT_ON	VBUSOTG_ON	BST_ON
				0	0	0	0	0	0	0	0
50	INT_PENDING_R1	R	8'b0000_0000	SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
				0	0	0	0	0	0	0	0
51	INT_PENDING_R2	R	8'b0000_0000	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
				0	0	0	0	0	0	0	0
52	INT_PENDING_R3	R	8'b0000_0000	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
				0	0	0	0	0	0	0	0
53	INT_PENDING_R4	R	8'b0000_0000	SWIN_RI	SWIN_FA	-	-	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA
				0	0	0	0	0	0	0	0
60	INT_DBG_LATCH_R1	W/R 0	8'b0000_0000	SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
				0	0	0	0	0	0	0	0
61	INT_DBG_LATCH_R2	W/R 0	8'b0000_0000	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
				0	0	0	0	0	0	0	0
62	INT_DBG_LATCH_R3	W/R 0	8'b0000_0000	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
				0	0	0	0	0	0	0	0
63	INT_DBG_LATCH_R4	W/R 0	8'b0000_0000	SWIN_RI	SWIN_FA	-	-	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA
				0	0	0	0	0	0	0	0
70	INT_CLEAR_R1	W/R 0	8'b0000_0000	SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
				0	0	0	0	0	0	0	0

chanhvinh.com

@HEX	Register name	R/W	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
71	INT_ CLEAR _R2	W/R 0	8'b0000_0000	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
				0	0	0	0	0	0	0	0
72	INT_ CLEAR _R3	W/R 0	8'b0000_0000	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
				0	0	0	0	0	0	0	0
73	INT_ CLEAR _R4	W/R 0	8'b0000_0000	SWIN_RI	SWIN_FA	-	-	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA
				0	0	0	0	0	0	0	0
80	INT_MASK_R1	W/R 0	8'b1111_1111	SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
				1	1	1	1	1	1	1	1
81	INT_MASK_R2	W/R 0	8'b1111_1111	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
				1	1	1	1	1	1	1	1
82	INT_MASK_R3	W/R 0	8'b1111_1111	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
				1	1	1	1	1	1	1	1
83	INT_MASK_R4	W/R 0	8'b1111_1111	SWIN_RI	SWIN_FA	-	-	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA
				1	1	1	1	1	1	1	1
90	INT_SET_MASK_R1	W/R 0	8'b0000_0000	SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
				0	0	0	0	0	0	0	0
91	INT_SET_MASK_R2	W/R 0	8'b0000_0000	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
				0	0	0	0	0	0	0	0
92	INT_SET_MASK_R3	W/R 0	8'b0000_0000	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
				0	0	0	0	0	0	0	0
93	INT_SET_MASK_R4	W/R 0	8'b0000_0000	SWIN_RI	SWIN_FA	-	-	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA
				0	0	0	0	0	0	0	0
A0	INT_CLEAR_MASK_R1	W/R 0	8'b0000_0000	SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
				0	0	0	0	0	0	0	0

chanhvinh.com

@HEX	Register name	R/W	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
A1	INT_CLEAR_MASK _R2	W/R 0	8'b0000_0000	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
				0	0	0	0	0	0	0	0
A2	INT_CLEAR_MASK _R3	W/R 0	8'b0000_0000	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
				0	0	0	0	0	0	0	0
A3	INT_CLEAR_MASK _R4	W/R 0	8'b0000_0000	SWIN_RI	SWIN_FA	-	-	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA
				0	0	0	0	0	0	0	0
B0	INT_SRC_R1	R	8'b0000_0000	SWOUT	-	VBUSOTG	-	WKP	-	PKEY	-
				0	0	0	0	0	0	0	0
B1	INT_SRC_R2	R	8'b0000_0000	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
				0	0	0	0	0	0	0	0
B2	INT_SRC_R3	R	8'b0000_0000	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
				0	0	0	0	0	0	0	0
B3	INT_SRC_R4	R	8'b0000_0000	SWIN	-	-	-	VINLOW	-	THW	-
				0	0	0	0	0	0	0	0
B8	NVM_SR	R	8'b0000_0000	-	-	-	-	-	-	-	NVM_BUSY
				0	0	0	0	0	0	0	0
B9	NVM_CR	R/W	8'b0000_0000	-	-	-	-	-	-	NVM_CMD[1:0]	
				0	0	0	0	0	0	0	0

chanhvinh.com

chanhvinh.com

6.2 Status registers

6.2.1 Turn-ON status register (TURN_ON_SR)

Table 19. **TURN_ON_SR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	AUTO	SWOUT	VBUS	WKUP	PKEY
R	R	R	R	R	R	R	R

Address: 0x01
Type: read register only
Default: b000x_xxxx where x depends on turn-ON condition
Description: turn-ON status register. This register stores last condition, which has turned ON the STPMIC1.
Register is set during CHECK&LOAD state following the turn-ON condition.
It is not refreshed or default by restart and default power cycle.

[7 :5]	Reserved
[4]	**AUTO**: STPMIC1 has automatically turned ON on VIN rising. 0: False 1: True
[3]	**SWOUT**: last Turn-ON condition was VBUS detection on SWOUT pin. 0: False 1: True
[2]	**VBUS**: last Turn-ON condition was VBUS detection on VBUSOTG pin 0: False 1: True
[1]	**WKUP**: last Turn-ON condition was WAKEUP pin detection 0: False 1: True
[0]	**PKEY**: last Turn-ON condition was PONKEYn detection 0: False 1: True

chanhvinh.com

6.2.2 Turn-OFF status register (TURN_OFF_SR)

Table 20. **TURN_OFF_SR**

7	6	5	4	3	2	1	0
reserved	reserved	PKEYLKP	WDG	OCP	THSD	VINOK_FA	SWOFF
R	R	R	R	R	R	R	R

Address: 0x02
Type: read register only
Default : b000x_xxxx where x depends on previous turn-OFF condition
Description: Turn-OFF status register. This register stores the last condition, which turns OFF the STPMIC1. It is set during POWER_DOWN state following turn-OFF condition.

[7 :6]	Reserved
[5]	**PKEYLKP**: Last turn-OFF condition was due to PONKEYn long key 0: False 1: True
[4]	**WDG**: Last turn-OFF condition was due to watchdog 0: False 1: True
[3]	**OCP**: Last turn-ON condition was due to overcurrent protection 0: False 1: True
[2]	**THSD**: Last turn-OFF condition was due to thermal shutdown 0: False 1: True
[1]	**VINOK_FA**: Last turn-OFF condition was due to VIN below V_{INOK_Fall} (when VIN is crossing VIN_POR_Rise threshold, this bit value is not valid) 0: False 1: True
[0]	**SWOFF**: Last turn-OFF condition was due to software switch OFF 0: False 1: True

chanhvinh.com

6.2.3 Overcurrent protection LDO turn-OFF status register (OCP_LDOS_SR)

Table 21. **OCP_LDOS_SR**

7	6	5	4	3	2	1	0
reserved	reserved	OCP_LDO6	OCP_LDO5	OCP_LDO4	OCP_LDO3	OCP_LDO2	OCP_LDO1
R	R	R	R	R	R	R	R

Address: 0x03

Type: read register only

Default: b00xx_xxxx where x depends on possible OCP event during previous POWER_ON

Description: OCP LDO turn-OFF status register. This register stores the identification of the LDO source of the last OCP turn-OFF.

It is set during POWER_DOWN state.

[7 :6]	Reserved
[5]	**OCP_LDO6**: Last turn-OFF was due to overcurrent protection on LDO6 0: False 1: True
[4]	**OCP_LDO5**: Last turn-OFF was due to overcurrent protection on LDO5 0: False 1: True
[3]	**OCP_LDO4**: Last turn-OFF was due to overcurrent protection on LDO4 0: False 1: True
[2]	**OCP_LDO3**: Last turn-OFF was due to overcurrent protection on LDO3 0: False 1: True
[1]	**OCP_LDO2**: Last turn-OFF was due to overcurrent protection on LDO2 0: False 1: True
[0]	**OCP_LDO1**: Last turn-OFF was due to overcurrent protection on LDO1 0: False 1: True

chanhvinh.com

6.2.4 Overcurrent protection buck turn-OFF status register (OCP_BUCKS_BSW_SR)

Table 22. **OCP_BUCKS_BSW_SR**

7	6	5	4	3	2	1	0
reserved	OCP_BOOST	OCP_SWOUT	OCP_VBUSOTG	OCP_BUCK4	OCP_BUCK3	OCP_BUCK2	OCP_BUCK1
R	R	R	R	R	R	R	R

Address: 0x04

Type: read register only

Default: b00xx_xxxx where x depends on possible OCP event during previous POWER_ON

Description: OCP buck turn-OFF status register. This register stores the identification of the BUCK, BOOST or power switch source of the last OCP turn-OFF.

It is set during POWER_DOWN state.

[7]	Reserved
[6]	**OCP_BOOST**: Last turn-OFF was due to overcurrent protection on BOOST 0: False 1: True
[5]	**OCP_SWOUT**: Last turn-OFF was due to overcurrent protection on SWOUT pin (PWR_SW out) 0: False 1: True
[4]	**OCP_VBUSOTG**: Last turn-OFF was due to overcurrent protection on VBUSTOTG pin (PWR_USB_SW out) 0: False 1: True
[3]	**OCP_BUCK4**: Last turn-OFF was due to overcurrent protection on BUCK4 0: False 1: True
[2]	**OCP_BUCK3**: Last turn-OFF was due to overcurrent protection on BUCK3 0: False 1: True
[1]	**OCP_BUCK2**: Last turn-OFF was due to overcurrent protection on BUCK2 0: False 1: True
[0]	**OCP_BUCK1**: Last turn-OFF was due to overcurrent protection on BUCK1 0: False 1: True

chanhvinh.com

6.2.5 Restart status register (RESTART_SR)

Table 23. **RESTART_SR**

7	6	5	4	3	2	1	0
OP_MODE	LDO4_SRC[1:0]		R_VINOK_FA	R_PKEYLKP	R_WDG	R_SWOFF	R_RST
R	R	R	R	R	R	R	R

Address: 0x05

Type: read register only

Default: b000x_xxxx where x depends on last restart condition

Description: Restart status register. This register mainly contains identification of the last restart condition. Either turn-OFF condition with restart_request option set, or from RSTn assertion from application processor. (Refer to Section 5.4.3 Turn-OFF conditions and restart_request) and Section 5.4.4 Reset and mask_reset option.

Bits prefixed with R_ are set during transition from POWER_DOWN to CHECK&LOAD.

This register also contains active operating mode (MAIN or ALTERNATE) and current LDO4 input source. (Refer to Section 4.2.2 LDO regulators - special features).

[7]	**OP_MODE**: Operating mode. Signal if the STPMIC1 is in MAIN mode or ALTERNATE mode. 0: STPMIC1 is in MAIN mode 1: STPMIC1 is in ALTERNATE mode
[6 :5]	**LDO4_SRC[1:0]**: LDO4 input source. Provides status of LDO4 input switch selection. 00: LDO4 is OFF 01: VIN supply selected 10: VBUSOTG supply selected 11: BSTOUT supply selected
[4]	**R_VINOK_FA**: Restart is due to VINOK_Fall turn-OFF condition while RREQ_EN bit is set 0: False 1: True
[3]	**R_PKEYLKP**: Restart is due to PONKEYn long key press turn- OFF condition while *RREQ_EN* bit is set 0: False 1: True
[2]	**R_WDG**: Restart is due to watchdog turn-OFF condition while *RREQ_EN* bit is set 0: False 1: True
[1]	**R_SWOFF**: Restart is due to *SWOFF* turn-OFF condition while *RREQ_EN* bit is set 0: False 1: True
[0]	**R_RST**: Restart is due to RSTn signal asserted by application processor 0: False 1: True

chanhvinh.com

6.2.6 Version status register (VERSION_SR)

Table 24. **VERSION_SR**

7	6	5	4	3	2	1	0
MAJOR_VERSION[3:0]				MINOR_VERSION[3:0]			
R	R	R	R	R	R	R	R

Address: 0x06
Type: read register only
Default: 0x21
Description: version status register. Chip ID version.

[7 :4]	**MAJOR_VERSION[3:0]**
[3 :0]	**MINOR_VERSION[3:0]**

Reading x21 means that the STPMIC1 has a silicon version 2.1; regardless the STPMIC1A, STPMIC1B, STPMIC1C, STPMIC1D and STPMIC1E.

chanhvinh.com

6.3 Control registers

6.3.1 Main control register (MAIN_CR)

Table 25. **MAIN_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	OCP_OFF_DBG	PWRCTRL_POL	PWRCTRL_EN	RREQ_EN	SWOFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x10
Type: read/write register
Default: 0x00
Description: main control register. This register is initialized to default values during CHECK&LOAD state.

[7 :5]	Reserved
[4]	**OCP_OFF_DBG**: Used as software debug bit to emulate OCP turn-OFF event generation. OCP flags coming from any regulators are bypassed when this bit is set. 0: OCP event is generated based on flags from regulators. 1: OCP turn-OFF event is generated.
[3]	**PWRCTRL_POL**: specifies PWRCTRL pin polarity 0: PWRCTRL active low 1: PWRCTRL active high
[2]	**PWRCTRL_EN**: enable PWRCTRL functionality 0: PWRCTRL enable 1: PWRCTRL disable
[1]	**RREQ_EN**: allows power cycling on turn-OFF condition 0: power cycling is performed only on RSTn assertion by the application processor 1: Power cycling is performed on turn-OFF condition and on RSTn assertion by the application processor
[0]	**SWOFF**: Software switch OFF bit 0: no effect 1: switch-OFF requested (POWER_DOWN starts immediately)

chanhvinh.com

6.3.2 Pads pull control register (PADS_PULL_CR)

Table 26. **PADS_PULL_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	WKUP_EN	PWRCTRL_PD	PWRCTRL_PU	WKUP_PD	PKEY_PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x11
Type: read/write register
Default: 0x00
Description: pads pull control register. This register is initialized to default values upon entering CHECK&LOAD state.

[7 :5]	Reserved
[4]	**WKUP_EN**: Enable WAKEUP detector 0: WAKEUP detector is enabled 1: WAKEUP detector is disabled
[3]	**PWRCTRL_PD**: PWRCTRL pull-down control 0: PD inactive 1: PD active Note: this bit has higher priority than *PWRCTRL_PU*.
[2]	**PWRCTRL_PU**: PWRCTRL pull-up control 0: PU inactive 1: PU active
[1]	**WKUP_PD**: WAKEUP pull-down control (reverse logic) 0: PD active 1: PD not active
[0]	**PKEY_PU**: PONKEY pull-up control (reverse logic) 0: PU active 1: PU not active

chanhvinh.com

6.3.3 Bucks pull-down control register (BUCKS_PD_CR)

Table 27. **BUCKS_PD_CR**

7	6	5	4	3	2	1	0
BUCK4_PD[1:0]		BUCK3_PD[1:0]		BUCK2_PD[1:0]		BUCK1_PD[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x12

Type: read/write register

Default: 0x00

Description: Bucks pull-down control register. This register is initialized to default values upon entering to CHECK&LOAD state

[7:6]	**BUCK4_PD[1:0]**: 00: light PD active when *ENA* of Buck4 = 0 01: high PD active when *ENA* of Buck4 = 0 10: light and high PD forced inactive 11: light PD forced active
[5:4]	**BUCK3_PD[1:0]**: 00: light PD active when *ENA* of Buck3 = 0 01: high PD active when *ENA* of Buck3 = 0 10: light and high PD forced inactive 11: light PD forced active
[3:2]	**BUCK2_PD[1:0]**: 00: light PD active when *ENA* of Buck2 = 0 01: high PD active when *ENA* of Buck2 = 0 10: light and high PD forced inactive 11: light PD forced active
[1:0]	**BUCK1_PD[1:0]**: 00: light PD active when *ENA* of Buck1 = 0 01: high PD active when *ENA* of Buck1 = 0 10: light and high PD forced inactive 11: light PD forced active

chanhvinh.com

6.3.4 LDO1-4 pull-down control register (LDO14_PD_CR)

Table 28. **LDO14_PD_CR**

7	6	5	4	3	2	1	0
LDO4_PD[1:0]		LDO3_PD[1:0]		LDO2_PD[1:0]		LDO1_PD[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x13

Type: read/write register

Default: 0x00

Description: LDO1-4 pull-down control register. This register is initialized to default values upon entering to CHECK&LOAD state.

[7:6]	**LDO4_PD[1:0]**: 00: PD active when *ENA* of LDO4 = 0 01: PD forced inactive 10: PD forced inactive 11: PD forced active
[5:4]	**LDO3_PD[1:0]**: 00: PD active when *ENA* of LDO3 = 0 01: PD forced inactive 10: PD forced inactive 11: PD forced active
[3:2]	**LDO2_PD[1:0]**: 00: PD active when *ENA* of LDO2 = 0 01: PD forced inactive 10: PD forced inactive 11: PD forced active
[1:0]	**LDO1_PD[1:0]**: 00: PD active when *ENA* of LDO1 = 0 01: PD forced inactive 10: PD forced inactive 11: PD forced active

chanhvinh.com

6.3.5 LDO5/6 pull-down control register (LDO56_VREF_PD_CR)

Table 29. **LDO56_VREF_PD_CR**

7	6	5	4	3	2	1	0
reserved	BST_PD	REFDDR_PD[1:0]		LDO6_PD[1:0]		LDO5_PD[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x14

Type: read/write register

Default: 0x00

Description: LDO5 and LDO6 pull-down control register. This register is initialized to default values upon entering to CHECK&LOAD state.

[7]	Reserved
[6]	BST_PD: Boost pull-down activation (reverse logic) 0: PD active when *BST_ON* = 0 1: PD inactive when *BST_ON* = 0
[5:4]	**REFDDR_PD[1:0]:** 00: PD active only when REFDDR disabled 01: PD forced inactive 10: PD forced inactive 11: PD forced active
[3:2]	**LDO6_PD[1:0]:** 00: PD active only when LDO6 disabled 01: PD forced inactive 10: PD forced inactive 11: PD forced active
[1:0]	**LDO5_PD[1:0]:** 00: PD active only when LDO5 disabled 01: PD forced inactive 10: PD forced inactive 11: PD forced active

chanhvinh.com

6.3.6 PWR_SWOUT and VIN control register (SW_VIN_CR)

Table 30. **SW_VIN_CR**

7	6	5	4	3	2	1	0
SWIN_DET_EN	SWOUT_DET_DIS	VINLOW_HYST[1:0]		VINLOW_TRESH[2:0]			VINLOW_MON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x15

Type: read/write register

Default: 0x00

Description: switch and VIN control register. This register is initialized to default values upon entering to CHECK&LOAD state.

[7]	**SWIN_DET_EN**: SWIN detection enable control bit 0: SW_IN detector is enabled only when SW_OUT switch is enabled else SW_IN detector is off 1: SW_IN detector is enabled
[6]	**SWOUT_DET_DIS**: SWOUT detection disable control bit 0: SWOUT detector is enabled 1 : SWOUT detector is disabled
[5 :4]	**VINLOW_HYST[1:0]**: VINLOW threshold hysteresis 00: 100 mV 01 : 200 mV 10 : 300 mV 11: 400 mV
[3 :1]	**VINLOW_TRESH[2:0]**: VINLOW threshold offset 000 : VINOK_Fall + 50 mV 001 : VINOK_Fall + 100 mV 010 : VINOK_Fall + 150 mV 011 : VINOK_Fall + 200 mV 100 : VINOK_Fall + 250 mV 101 : VINOK_Fall + 300 mV 110 : VINOK_Fall + 350 mV 111 : VINOK_Fall + 400 mV
[0]	**VINLOW_MON**: VINLOW monitoring enable bit 0: VINLOW monitoring is disabled 1: VINLOW monitoring is enabled

chanhvinh.com

6.3.7 PONKEYn turn-OFF control register (PKEY_TURNOFF_CR)

Table 31. **PKEY_TURNOFF_CR**

7	6	5	4	3	2	1	0
PKEY_LKP_OFF	PKEY_CLEAR_OCP_FLAG	reserved	reserved	PKEY_LKP_TMR[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x16

Type: read/write register

Default: 0bX0000000 where X depends on the value programmed in NVM

Description: PONKEYn turn-OFF control register. This register is initialized to default values during CHECK&LOAD state.

[7]	**PKEY_LKP_OFF**: 0: Turn OFF on long key press inactive 1: Turn OFF on long key press active Default value is defined by PKEYLKP_OFF bit in Table 65. NVM_MAIN_CTRL_SHR
[6]	**PKEY_CLEAR_OCP_FLAG**: 0: only VIN_POR_Fall can reset LOCK_OCP_FLAG internal signal 1: if PONKEYn pin is pressed for more than *PKEY_LKP_TMR[3:0]* then LOCK_OCP_FLAG is cleared. This also results as turn-ON condition for the STPMIC1
[5 :4]	reserved
[3 :0]	**PKEY_LKP_TMR[3:0]**: PONKEYn long key press duration 0000 : 16 s 0001 : 15 s 0010 : 14 s 0011 : 13 s 0100 : 12 s 0101 : 11 s 0110 : 10 s 0111 : 9 s 1000 : 8 s 1001 : 7 s 1010: 6 s 1011 : 5 s 1100 : 4 s 1101 : 3 s 1110 : 2 s 1111 : 1 s

chanhvinh.com

6.3.8 Mask reset Buck control register (BUCKS_MRST_CR)

Table 32. **BUCKS_MRST_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	MRST_BUCK4	MRST_BUCK3	MRST_BUCK2	MRST_BUCK1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x18

Type: read/write register

Default: 0x00

Description: mask reset Buck control register. Set bit to 1 active Mask reset option for selected Bucks for the next NRST power cycle. It is a single shot option. Register is reset to default in CHECK&LOAD state.

Refer to Section 5.4.4 Reset and mask_reset option.

[7 :4]	Reserved
[3]	**MRST_BUCK4**: Buck 4 mask reset option 0: inactive 1: Mask default active for Buck4
[2]	**MRST_BUCK3**: Buck3 mask reset option 0: inactive 1: Mask default active for Buck3
[1]	**MRST_BUCK2**: Buck2 mask reset option 0: inactive 1: Mask default active for Buck2
[0]	**MRST_BUCK1**: Buck1 mask reset option 0: inactive 1: Mask default active for Buck1

chanhvinh.com

6.3.9 Mask reset LDO control register (LDOS_MRST_CR)

Table 33. **LDOS_MRST_CR**

7	6	5	4	3	2	1	0
reserved	MRST_REFDDR	MRST_LDO6	MRST_LDO5	MRST_LDO4	MRST_LDO3	MRST_LDO2	MRST_LDO1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x1A

Type: read/write register

Default: 0x00

Description: mask reset LDO control register. Set bit to 1 active mask reset option for selected LDO for next reset power-cycle. It is a single shot option. Register is reset to default in CHECK&LOAD state. Refer to Section 5.4.4 Reset and mask_reset option.

[7]	Reserved
[6]	**MRST_REFDDR**: REFDDR LDO mask reset option 0: inactive 1: Mask reset active for REFDDR
[5]	**MRST_LDO6**: LDO6 mask default option 0: inactive 1: mask reset active for LDO6
[4]	**MRST_LDO5**: LDO5 mask default option 0: inactive 1: mask reset active for LDO5
[3]	**MRST_LDO4**: LDO4 mask default option 0: inactive 1: mask reset active for LDO4
[2]	**MRST_LDO3**: LDO3 mask default option 0: inactive 1: mask reset active for LDO3
[1]	**MRST_LDO2**: LDO2 mask default option 0: inactive 1: mask default active for LDO2
[0]	**MRST_LDO1**: LDO1 mask default option 0: inactive 1: mask default active for LDO1

chanhvinh.com

6.3.10 Watchdog control register (WDG_CR)

Table 34. **WDG_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	WDG_RST	WDG_ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x1B
Type: read/write register
Default: 0x00
Description: watchdog control register

[7 :2]	Reserved
[1]	**WDG_RST**: watchdog counter reset 0: NA 1: Watchdog downcounter is reloaded with a value in WDG_TIMER_CR (self-cleared bit)
[0]	**WDG_ENA**: watchdog enable bit 0: watchdog is disabled 1: watchdog is enabled

chanhvinh.com

6.3.11 Watchdog timer control register (WDG_TMR_CR)

Table 35. **WDG_TMR_CR**

7	6	5	4	3	2	1	0
WDG_TMR [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x1C

Type: read/write register

Default: 0x00

Description: watchdog timer control register. This register is initialized to default value upon entering CHECK&LOAD state.

[7 :0]	**WDG_TMR[7:0]**: watchdog downcounter period value Value in second. 0x00 = 1 s … 0xFF=256 s

chanhvinh.com

6.3.12 Bucks OCP turn-OFF control register (BUCKS_OCPOFF_CR)

Table 36. **BUCKS_OCPOFF_CR**

7	6	5	4	3	2	1	0
reserved	OCPOFF BOOST	OCPOFF SWOUT	OCPOFF VBUSOTG	OCPOFF BUCK4	OCPOFF BUCK3	OCPOFF BUCK2	OCPOFF BUCK1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x1D
Type: read/write register
Default: 0x00
Description: Buck OCP turn-OFF control register. This register is initialized to default value during CHECK&LOAD state.

[7]	reserved
[6]	**OCPOFFBOOST**: STPMIC1 turn-OFF in case OCP on BOOST 0: False 1: True
[5]	**OCPOFFSWOUT**: STPMIC1 turn-OFF in case OCP on SWOUT 0: False 1: True
[4]	**OCPOFFVBUSOTG**: STPMIC1 turn-OFF in case OCP on VBUSOTG 0: False 1: True
[3]	**OCPOFFBUCK4**: STPMIC1 turn-OFF in case OCP on BUCK4 0: False 1: True
[2]	**OCPOFFBUCK3**: STPMIC1 turn-OFF in case OCP on BUCK3 0: False 1: True
[1]	**OCPOFFBUCK2**: STPMIC1 turn-OFF in case OCP on BUCK2 0: False 1: True
[0]	**OCPOFFBUCK1**: STPMIC1 turn-OFF in case OCP on BUCK1 0: False 1: True

chanhvinh.com

6.3.13 LDO OCP turn-OFF control register (LDOS_OCPOFF_CR)

Table 37. **LDOS_OCPOFF_CR**

7	6	5	4	3	2	1	0
reserved	reserved	OCPOFFLDO6	OCPOFFLDO5	OCPOFFLDO4	OCPOFFLDO3	OCPOFFLDO2	OCPOFFLDO1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x1E

Type: read/write register

Default: 0x00

Description: LDO OCP turn-OFF control register. This register is initialized to default value upon entering CHECK&LOAD state.

[7 :6]	Reserved
[5]	**OCPOFFLDO6**: STPMIC1 Turn-OFF in case OCP on LDO6 0: False 1: True
[4]	**OCPOFFLDO5**: STPMIC1 Turn-OFF in case OCP on LDO5 0: False 1: True
[3]	**OCPOFFLDO4**: STPMIC1 Turn OFF in case OCP on LDO4 0: False 1: True
[2]	**OCPOFFLDO3**: STPMIC1 Turn-OFF in case OCP on LDO3 0: False 1: True
[1]	**OCPOFFLDO2**: STPMIC1 Turn-OFF in case OCP on LDO2 0: False 1: True
[0]	**OCPOFFLDO1**: STPMIC1 Turn-OFF in case OCP on LDO1 0: False 1: True

chanhvinh.com

6.4 Power supplies control registers

6.4.1 BUCKx MAIN mode control registers (BUCKx_MAIN_CR) (x=1…4)

Table 38. BUCKx_MAIN_CR

7	6	5	4	3	2	1	0
VOUT[5:0]						PREG_MODE	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x20 to 0x23

Type: Read/write register

Default: 0bXXXXXX0X where X depends on the value programmed in NVM

Description: BUCKx MAIN mode control registers. Registers are initialized in CHECK&LOAD state. User can write to these registers to control enable, regulation mode and voltage setting of BUCKx that are applied to MAIN mode.

[7:2]	**VOUT[5:0]**: Buck output voltage setting. Refer to Table 10. BUCK output settings
[1]	**PREG_MODE**: select high power or low power regulation mode 0: High power mode (HP) 1: Low power mode (LP)
[0]	**ENA**: Buck enable bit 0: Buck is disabled 1: Buck is enabled

chanhvinh.com

6.4.2 REFDDR MAIN mode control register (REFDDR_MAIN_CR)

Table 39. **REFDDR_MAIN_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x24
Type: read/write register
Default: 0x0000000X where X depends on NVM settings
Description: REFDDR, MAIN mode control register. Register is initialized in CHECK&LOAD mode.
User can write to this register to control the enable of REFDDR applied to MAIN mode.

[7 :1]	Reserved
[0]	**ENA**: VREF_DDR enable bit 0: VREF_DDR is disabled 1: VREF_DDR is enabled

chanhvinh.com

6.4.3 LDOx MAIN mode control registers (LDOx_MAIN_CR) (x=1, 2, 5, 6)

Table 40. **LDOx_MAIN_CR**

7	6	5	4	3	2	1	0
reserved	VOUT[4:0]					Reserved	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x25, 0x26, 0x29, 0x2A
Type: read/write register
Default: 0b0XXXXX00 where X depends on the value programmed in NVM
Description: LDOx (x=1,2,5,6) MAIN mode control register. The register is set to default value in CHECK&LOAD. User can write to this register to control both enable and voltage settings of LDOx that are applied to MAIN mode.

[7]	Reserved
[6:2]	**VOUT[4:0]**: refer to Table 9. LDO output voltage settings
[1]	reserved
[0]	**ENA**: LDOx enable bit 0: LDOx is disabled 1: LDOx is enabled

chanhvinh.com

6.4.4 LDO3 MAIN mode control register (LDO3_MAIN_CR)

Table 41. **LDO3_MAIN_CR**

7	6	5	4	3	2	1	0
BYPASS	VOUT[4:0]					reserved	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x27

Type: read/write register

Default: 0bXXXXXX00 where X depends on the value programmed in NVM

Description: LDO3 MAIN mode control register. The register is set to a default value in CHECK&LOAD.

User can write to this register to control bypass, enable and voltage settings of LDO3 that is applied to MAIN mode.

[7]	**BYPASS**: force bypass mode of LDO3 0: LDO3 is in normal mode 1: LDO3 is in bypass mode. *VOUT[4:0]* bits have no effect
[6:2]	**VOUT[4:0]**: refer to Table 9. LDO output voltage settings
[1]	reserved
[0]	**ENA**: LDO3 enable bit 0: LDO3 is disabled 1: LDO3 is enabled

chanhvinh.com

6.4.5 LDO4 MAIN mode control register (LDO4_MAIN_CR)

Table 42. **LDO4_MAIN_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	SRC_VBUSOTG	SRC_BOOST	SRC_VIN	reserved	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x28

Type: read/write register

Default: 0x0000000X

Description: LDO4 MAIN mode control register. Register is set to a default value in CHECK&LOAD. User can write to this register to enable and force the input source of LDO4 that is applied to MAIN mode. If more than one SRC_ bit is set, it is taken into account following this priority order: VIN, VBUSOTG, BSTOUT.

[7 :5]	reserved
[4]	**SRC_VBUSOTG**: Force VBUSOTG as input source. 0: automatic 1: supply switch is set to VBUSOTG
[3]	**SRC_BSTOUT**: Force BSTOUT has input source. 0: automatic 1: supply switch is set to BSTOUT
[2]	**SRC_VIN**: Force VIN has an input source. 0: automatic 1: supply switch is set to VIN
[1]	reserved
[0]	**ENA**: LDO4 enable bit 0: LDO4 is disabled 1: LDO4 is enabled

chanhvinh.com

6.4.6 BUCKx ALTERNATE mode control registers (BUCKx_ALT_CR)(x=1..4)

Table 43. **BUCKx_ALT_CR**

7	6	5	4	3	2	1	0
VOUT[5:0]						PREG_MODE	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x30 to 0x33

Type: read/write register

Default: 0bXXXXXX00 where X depends on the value programmed in NVM

Description: BUCKx ALTERNATE mode control registers. The register is set to a default value in CHECK&LOAD.

User can write to these registers to control enable, regulation mode and voltage settings of BUCKx that is applied to ALTERNATE mode.

[7:2]	**VOUT[5:0]**: refer to Table 10. BUCK output settings
[1]	**PREG_MODE**: Force high power - low power mode of buck 0: high power mode (HP) 1: low power mode (LP)
[0]	**ENA**: buck enable bit 0: buck is disabled 1: buck is enabled

chanhvinh.com

6.4.7 REFDDR ALTERNATE mode control register (REFDDR_ALT_CR)

Table 44. **REFDDR_ALT_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x34

Type: read/write register

Default: 0x00

Description: REFDDR ALTERNATE mode control register. The register is initialized in CHECK&LOAD mode. User can write to this register to control enable of REFDDR that is applied to ALTERNATE mode.

[7 :1]	Reserved
[0]	**ENA**: REFDDR enable bit 0: REFDDR is disabled 1: REFDDR is enabled

chanhvinh.com

6.4.8 LDOx ALTERNATE mode control registers (LDOx_ALT_CR) (x=1, 2, 5, 6)

Table 45. LDOx_ALT_CR

7	6	5	4	3	2	1	0
reserved	VOUT[4:0]					reserved	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x35, 0x36, 0x39, 0x3A

Type: read/write register

Default: 0b0XXXXX0X where X depends on the value programmed in NVM

Description: LDOx ALTERNATE mode control registers. Register is set to a default value in CHECK&LOAD.

User can write to these registers to control enable and voltage settings of LDOx that are applied to ALTERNATE mode.

[7]	Reserved
[6 :2]	**VOUT[4:0]**: refer to Table 9. LDO output voltage settings
[1]	reserved
[0]	**ENA**: LDOx enable bit 0: LDOx is disabled 1: LDOx is enabled

chanhvinh.com

6.4.9 LDO3 ALTERNATE mode control register (LDO3_ALT_CR)

Table 46. LDO3_ALT_CR

7	6	5	4	3	2	1	0
BYPASS	VOUT[4:0]					reserved	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x37

Type: read/write register

Default: 0bXXXXXX00 where X depends on the value programmed in NVM

Description: LDO3 ALTERNATE mode control register. Register is set to a default value in CHECK&LOAD.

User can write to this register to control bypass, enable and voltage settings of LDO3 that is applied to ALTERNATE mode.

[7]	**BYPASS**: force bypass mode of LDO3 0: LDO3 is in normal mode 1: LDO3 is in bypass mode. *VOUT[4:0]* bits have no effect. Default value of BYPASS is NVM_LDO3_BYPASS.
[6:2]	**VOUT[4:0]**: refer to Table 9. LDO output voltage settings
[1]	reserved
[0]	**ENA**: LDO3 enable bit 0: LDO3 is disabled 1: LDO3 is enabled

chanhvinh.com

6.4.10 LDO4 ALTERNATE mode control register (LDO4_ALT_CR)

Table 47. **LDO4_ALT_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	ENA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x38
Type: read/write register
Default: 0x00
Description: LDO4 ALTERNATE mode control register. Register is set to a default value in CHECK&LOAD. User can write to this register to control enable LDO4 that is applied to ALTERNATE mode.

[7 :1]	Reserved
[0]	**ENA**: LDO4 enable bit 0: LDO4 is disabled 1: LDO4 is enabled

chanhvinh.com

6.4.11 Boost/switch control register (BST_SW_CR)

Table 48. **BST_SW_CR**

7	6	5	4	3	2	1	0
RESERVED	VBUSOTG_DET_DIS	SWOUT_PD	VBUSOTG_PD	OCP_SWOUT_LIM	SWOUT_ON	VBUSOTG_ON	BST_ON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x40
Type: read/write register
Default: 0x00
Description: boost and power switch control register. Register is set to a default value in CHECK&LOAD.

[7]	RESERVED
[6]	**VBUSOTG_DET_DIS**: PWR_USB_SW detection circuit disable 0: detection circuit is enabled 1: detection circuit is disabled
[5]	**SWOUT_PD**: SWOUT (PWR_SW) pull-down activation 0: PD inactive 1: PD active when PWR_SW is disabled (SW_ON bit = 0)
[4]	**VBUSOTG_PD**: PWR_USB_SW pull-down activation 0: PD inactive 1: PD active when PWR_USB_SW is disabled (VBUSOTG_ON bit = 0)
[3]	**OCP_SWOUT_LIM**: Overcurrent limit protection of PWR_SW switch 0: limit max. output current to 600 mA 1: limit max. output current to 1.1 A
[2]	**SWOUT_ON**: PWR_SW switch enable bit 0: PWR_SW disabled 1: PWR_SW enabled
[1]	**VBUSOTG_ON**: PWR_USB_SW switch enable 0: PWR_USB_SW disabled 1: PWR_USB_SW enabled
[0]	**BST_ON**: BOOST enable bit 0: BOOST disabled 1: BOOST enabled

chanhvinh.com

6.5 Interrupt registers

6.5.1 Overall interrupt register behavior

No interrupts are stored before RSTn is released. Interrupt registers are all cleared and masked on default and turn-OFF conditions.

Section 6.5.2 Interrupt pending register 1 (INT_PENDING_R1), Section 6.5.3 Interrupt pending register 2 (INT_PENDING_R2), Section 6.5.4 Interrupt pending register 3 (INT_PENDING_R3) and Section 6.5.5 Interrupt pending register 4 (INT_PENDING_R4) store information about masked and not masked events.

Section 6.5.10 Interrupt clear mask registers (INT_CLEAR_MASK_Rx) or Section 6.5.6 Interrupt debug latch registers (INT_DBG_LATCH_Rx) is a write register. Any read on this address provides x00 as data. Writing ‘1’ in a bit forces INT_PENDING corresponding bit to ‘1’. Writing ‘0’ has no effect.

Section 6.5.8 Interrupt mask registers (INT_MASK_Rx) is a read/write register.

INTn pin is forced low as long as a bit is set in INT_PENDING_Rx and no mask in its corresponding Section 6.5.8 Interrupt mask registers (INT_MASK_Rx). Section 6.5.11 Interrupt source register 1 (INT_SRC_R1), Section 6.5.12 Interrupt source register 2 (INT_SRC_R2), Section 6.5.13 Interrupt source register 3 (INT_SRC_R3) and Section 6.5.14 Interrupt source register 4 (INT_SRC_R4) reflects a ‘real time’ status of the event while INT_PENDING_Rx stores events and not levels.

chanhvinh.com

6.5.2 Interrupt pending register 1 (INT_PENDING_R1)

Table 49. **INT_PENDING_R1**

7	6	5	4	3	2	1	0
SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
R	R	R	R	R	R	R	R

Address: 0x50
Type: read register only
Default: 0x00
Description: interrupt pending register 1. Register is set to default on RSTn assertion.
For all bits:
0: IT not pending
1: IT pending

[7]	**SWOUT_RI**: VBUS on SWOUT pin (PWR_SW out) rises above SWOUT_Rise treshold
[6]	**SWOUT_FA**: VBUS on SWOUT pin (PWR_SW out) falls below above SWOUT_Fall treshold
[5]	**VBUSOTG_RI**: VBUS on VBUSOTG pin (PWR_USB_SW out) rises above VBUSOTG_Rise threshold
[4]	**VBUSOTG_FA**: VBUS on VBUSOTG pin (PWR_USB_SW out) falls below VBUSOTG_Fall threshold
[3]	**WKP_RI**: WAKEUP rising edge
[2]	**WKP_FA**: WAKEUP falling edge
[1]	**PKEY_RI**: PONKEYn rising edge
[0]	**PKEY_FA**: PONKEYn falling edge detected

chanhvinh.com

6.5.3 Interrupt pending register 2 (INT_PENDING_R2)

Table 50. **INT_PENDING_R2**

7	6	5	4	3	2	1	0
BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
R	R	R	R	R	R	R	R

Address: 0x51
Type: read register only
Default: 0x00
Description: interrupt pending register 2. Register is set to default on RSTn assertion
For all bits:
0: IT not pending
1: IT pending

[7]	**BST_OVP**: Overvoltage detected on Boost BSTOUT pin
[6]	**BST_OCP**: Overcurrent detected on Boost BSTOUT pin
[5]	**SWOUT_OCP**: Current limitation detected on SWOUT pin
[4]	**VBUSOTG_OCP**: Overcurrent detected on VBUSOTG pin
[3]	**BUCK4_OCP**: Overcurrent detected on Buck4
[2]	**BUCK3_OCP**: Overcurrent detected on Buck3
[1]	**BUCK2_OCP**: Overcurrent detected on Buck2
[0]	**BUCK1_OCP**: Overcurrent detected on Buck1

chanhvinh.com

6.5.4 Interrupt pending register 3 (INT_PENDING_R3)

Table 51. **INT_PENDING_R3**

7	6	5	4	3	2	1	0
SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
R	R	R	R	R	R	R	R

Address: 0x52
Type: read register only
Default: 0x00
Description: interrupt pending register 3. Register is set to default on RSTn assertion
For all bits:
0: IT not pending
1: IT pending

[7]	**SWOUT_SH**: A short event has been detected on SWOUT pin. Refer to Section 4.5.2 PWR_USB_SW and PWR_SW power switches
[6]	**VBUSOTG_SH**: A short event has been detected on VBUSOTG pin. Refer to Section 4.5.2 PWR_USB_SW and PWR_SW power switches
[5]	**LDO6_OCP**: Current limitation detected on LDO6
[4]	**LDO5_OCP**: Current limitation detected on LDO5
[3]	**LDO4_OCP**: Current limitation detected on LDO4
[2]	**LDO3_OCP**: Current limitation detected on LDO3
[1]	**LDO2_OCP**: Current limitation detected on LDO2
[0]	**LDO1_OCP**: Current limitation detected on LDO1

chanhvinh.com

6.5.5 Interrupt pending register 4 (INT_PENDING_R4)

Table 52. **INT_PENDING_R4**

7	6	5	4	3	2	1	0
SWIN_RI	SWIN_FA	reserved	reserved	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA
R	R	R	R	R	R	R	R

Address: 0x53
Type: read register only
Default: 0x00
Description: interrupt pending register 4. Register is set to default on RSTn assertion
For all bits:
0: IT not pending
1: IT pending

[7]	**SWIN_RI**: Voltage on SWIN pin (PWR_SW input) rises above SWIN_Rise threshold
[6]	**SWIN_FA**: Voltage on SWIN pin (PWR_SW input) falls below SWIN_Fall threshold
[5 :4]	reserved
[3]	**VINLOW_RI**: VIN drops below VINLOW_Rise threshold
[2]	**VINLOW_FA**: VIN rises above VINLOW_Fall threshold
[1]	**THW_RI**: Temperature rises above Twrn_Rise threshold
[0]	**THW_FA**: Temperature drops below Twrn_Fall threshold

chanhvinh.com

6.5.6 Interrupt debug latch registers (INT_DBG_LATCH_Rx)

Table 53. **INT_DBG_LATCH_Rx**

Name	Address	7	6	5	4	3	2	1	0
INT_DBG_ LATCH_R1	0x60	SWOUT _RI	SWOUT _FA	VBUS OTG_RI	VBUS OTG_FA	WKP _RI	WKP _FA	PKEY _RI	PKEY _FA
INT_DBG_ LATCH_R2	0x61	BST _OVP	BST _OCP	SWOUT _OCP	VBUSOTG _OCP	BUCK4_ OCP	BUCK3_ OCP	BUCK2_ OCP	BUCK1_ OCP
INT_DBG_ LATCH_R3	0x62	SWOUT_ SH	VBUS OTG_SH	LDO6_ OCP	LDO5_ OCP	LDO4_ OCP	LDO3_ OCP	LDO2_ OCP	LDO1_ OCP
INT_DBG_ LATCH_R4	0x63	SWIN _RI	SWIN _FA	reserved	reserved	VINLOW _RI	VINLOW _FA	THW_RI	THW _FA

Address: 0x60-0x63

Type: write register - read x00

Default: 0x00

Description: interrupt debug latch registers. Write registers only. Read always return 0x00.

Writing 1 in the bit forces the corresponding interrupt event in INT_PENDING_Rx

Refer to Section 6.5.2 Interrupt pending register 1 (INT_PENDING_R1), Section 6.5.3 Interrupt pending register 2 (INT_PENDING_R2), Section 6.5.4 Interrupt pending register 3 (INT_PENDING_R3) and Section 6.5.5 Interrupt pending register 4 (INT_PENDING_R4) about the interrupt description.

chanhvinh.com

6.5.7 Interrupt clear registers (INT_CLEAR_Rx)

Table 54. **INT_CLEAR_Rx**

Name	Address	7	6	5	4	3	2	1	0
INT_CLEAR_R1	0x70	SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
INT_CLEAR_R2	0x71	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
INT_CLEAR_R3	0x72	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
INT_CLEAR_R4	0x73	SWIN_RI	SWIN_FA	reserved	reserved	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA

Address: 0x70-0x73

Type: write register - read x00

Default: 0x00

Description: Interrupt clear registers. Write registers only. Read always return 0x00.

Writing 1 clears the corresponding interrupt event in INT_PENDING_Rx

Refer to Section 6.5.2 Interrupt pending register 1 (INT_PENDING_R1), Section 6.5.3 Interrupt pending register 2 (INT_PENDING_R2), Section 6.5.4 Interrupt pending register 3 (INT_PENDING_R3) and Section 6.5.5 Interrupt pending register 4 (INT_PENDING_R4) about the interrupt description.

chanhvinh.com

6.5.8 Interrupt mask registers (INT_MASK_Rx)

Table 55. **INT_MASK_Rx**

Name	Address	7	6	5	4	3	2	1	0
INT_MASK_R1	0x80	SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
INT_MASK_R2	0x81	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
INT_MASK_R3	0x82	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
INT_MASK_R4	0x83	SWIN_RI	SWIN_FA	reserved	reserved	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA

Address: 0x80 – 0x83
Type: read/write register
Default: 0xFF
0x83
Description: interrupt mask registers. Registers are default on RSTn assertion.
Reading 1 from the bit means the corresponding interrupt event is masked
Refer to Section 6.5.2 Interrupt pending register 1 (INT_PENDING_R1), Section 6.5.3 Interrupt pending register 2 (INT_PENDING_R2), Section 6.5.4 Interrupt pending register 3 (INT_PENDING_R3) and Section 6.5.5 Interrupt pending register 4 (INT_PENDING_R4) about the interrupt description.

chanhvinh.com

6.5.9 Interrupt set mask registers (INT_SET_MASK_Rx)

Table 56. **INT_SET_MASK_Rx**

Name	Address	7	6	5	4	3	2	1	0
INT_SET_MASK_R1	0x90	SWOUT_RI	SWOUT_FA	VBUSOTG_RI	VBUSOTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
INT_SET_MASK_R2	0x91	BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
INT_SET_MASK_R3	0x92	SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
INT_SET_MASK_R4	0x93	SWIN_RI	SWIN_FA	reserved	reserved	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA

Address: 0x90 – 0x93

Type: write registers - read x00

Default: 0x00

Description: interrupt set mask registers. Registers are default on RSTn assertion

Writing 1 in the bit forces the mask of the corresponding interrupt event in INT_MASK_Rx

Refer to Section 6.5.2 Interrupt pending register 1 (INT_PENDING_R1), Section 6.5.3 Interrupt pending register 2 (INT_PENDING_R2), Section 6.5.4 Interrupt pending register 3 (INT_PENDING_R3) and Section 6.5.5 Interrupt pending register 4 (INT_PENDING_R4) about the interrupt description.

chanhvinh.com

6.5.10 Interrupt clear mask registers (INT_CLEAR_MASK_Rx)

Table 57. **INT_CLEAR_MASK_Rx**

Name	Address	7	6	5	4	3	2	1	0
INT_CLEAR_MASK_R1	0xA0	SWOUT_RI	SWOUT_FA	VBUS OTG_RI	VBUS OTG_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
INT_CLEAR_MASK_R2	0xA1	BST_OVP	BST_OCP	SWOUT_OCP	VBUS OTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
INT_CLEAR_MASK_R3	0xA2	SWOUT_SH	VBUS OTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
INT_CLEAR_MASK_R4	0xA3	SWIN_RI	SWIN_FA	reserved	reserved	VINLOW_RI	VINLOW_FA	THW_RI	THW_FA

Address: 0xA0 – 0xA3

Type: write register - read x00

Default: 0x00

Description: interrupt clear registers. Registers are default on RSTn assertion.

Writing 1 in the bit clears the mask of the corresponding interrupt in INT_MASK_Rx.

Refer to Section 6.5.2 Interrupt pending register 1 (INT_PENDING_R1), Section 6.5.3 Interrupt pending register 2 (INT_PENDING_R2), Section 6.5.4 Interrupt pending register 3 (INT_PENDING_R3) and Section 6.5.5 Interrupt pending register 4 (INT_PENDING_R4) about the interrupt description.

chanhvinh.com

6.5.11 Interrupt source register 1 (INT_SRC_R1)

Table 58. **INT_SRC_R1**

7	6	5	4	3	2	1	0
SWOUT	reserved	VBUSOTG	reserved	WKP	reserved	PKEY	reserved
R	R	R	R	R	R	R	R

Address: 0xB0
Type: read register
Default: 0x00
Description: interrupt source register 1. Register is reset on RSTn assertion.
State bit is 1 as long as event source is active.

[7]	**SWOUT**: SWOUT event source state 0: inactive 1: active
[6]	reserved
[5]	**VBUSOTG**: VBUSOTG event source state 0: inactive 1: active
[4]	reserved
[3]	**WKP**: WAKEUP event source state 0: inactive 1: active
[2]	reserved
[1]	**PKEY**: PONKEYn event source state 0: inactive 1: active
[0]	reserved

chanhvinh.com

6.5.12 Interrupt source register 2 (INT_SRC_R2)

Table 59. **INT_SRC_R2**

7	6	5	4	3	2	1	0
BST_OVP	BST_OCP	SWOUT_OCP	VBUSOTG_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
R	R	R	R	R	R	R	R

Address: 0xB1
Type: read register
Default: 0x00
Description: interrupt source register 2. Register is set to default on RSTn assertion. State bit is 1 as long as event source is active.

[7]	**BST_OVP**: overvoltage detection on Boost output 0: inactive 1: active
[6]	**BST_OCP**: Current limitation detection on Boost output 0: inactive 1: active
[5]	**SWOUT_OCP**: Current limitation detection on SWOUT 0: inactive 1: active
[4]	**VBUSOTG_OCP**: Current limitation detection on VBUSOTG 0: inactive 1: active
[3]	**BUCK4_OCP**: Current limitation detection on Buck4 0: inactive 1: active
[2]	**BUCK3_OCP**: Current limitation detection on Buck3 0: inactive 1: active
[1]	**BUCK2_OCP**: Current limitation detection on Buck2 0: inactive 1: active
[0]	**BUCK1_OCP**: Current limitation detection on Buck1 0: inactive 1: active

chanhvinh.com

6.5.13 Interrupt source register 3 (INT_SRC_R3)

Table 60. **INT_SRC_R3**

7	6	5	4	3	2	1	0
SWOUT_SH	VBUSOTG_SH	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
R	R	R	R	R	R	R	R

Address: 0xB2

Type: read register

Default: 0x00

Description: interrupt source register 3. Register is default on RSTn assertion. State bit is 1 as long as event source is active.

[7]	**SWOUT_SH**: Current limitation detection on SWOUT 0: inactive 1: active
[6]	**VBUSOTG_SH**: Current limitation detection on VBUSOTG 0: inactive 1: active
[5]	**LDO6_OCP**: Current limitation detection on LDO6 0: inactive 1: active
[4]	**LDO5_OCP**: Current limitation detection on LDO5 0: inactive 1: active
[3]	**LDO4_OCP**: Current limitation detection on LDO4 0: inactive 1: active
[2]	**LDO3_OCP**: Current limitation detection on LDO3 0: inactive 1: active
[1]	**LDO2_OCP**: Current limitation detection on LDO2 0: inactive 1: active
[0]	**LDO1_OCP**: Current Limitation detection on LDO1 0: inactive 1: active

chanhvinh.com

6.5.14 Interrupt source register 4 (INT_SRC_R4)

Table 61. **INT_SRC_R4**

7	6	5	4	3	2	1	0
SWIN	reserved	reserved	reserved	VINLOW	reserved	THW	reserved
R	R	R	R	R	R	R	R

Address: 0xB3

Type: read register

Default: 0x00

Description: interrupt source register 4. Register is default on RSTn assertion. State bit is 1 as long as event source is active.

[7]	**SWIN**: SWIN event source state 0: inactive 1: active
[6 :4]	reserved
[3]	**VINLOW**: VINLOW event source state 0: inactive 1: active
[2]	reserved
[1]	**THW**: Temperature event source state 0: inactive 1: active
[0]	reserved

chanhvinh.com

6.6 NVM registers

6.6.1 NVM status register (NVM_SR)

Table 62. **NVM_SR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	NVM_BUSY
R	R	R	R	R	R	R	R

Address: 0xB8
Type: read only register
Default: 0x00
Description: NVM status register.

[7 :1]	reserved
[0]	**NVM_BUSY**: NVM controller status 0: NVM controller is in idle state 1: NVM controller is in busy state Self-cleared when the operation is completed

chanhvinh.com

6.6.2 NVM control register (NVM_CR)

Table 63. **NVM_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	NVM_CMD[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xB9
Type: read/write register
Default: 0x00
Description: NVM control register

[7 :2]	reserved
[1:0]	**NVM_CMD[1:0]**: NVM controller command bits to control NVM operation on NVM shadow register bits. 00: No operation 01: Program (write shadow register to NVM) 10: Read (load NVM content into shadow registers) 11: No operation

chanhvinh.com

6.7 NVM shadow registers

chanhvinh.com

Table 64. NVM shadow register map

				BITS[7:0]							
@HEX	Register name	R/W	Default	7	6	5	4	3	2	1	0
F8	NVM_MAIN_CTRL_SHR	R/W	A:8'b1110_1110	VINOK_HYST[1:0]		VIN_OK_THRES[1:0]		FORCE_LDO4	PKEYLKP_OFF	AUTO_TURN_ON	LOCK_OCP
				1	1	1	0	1	1	1	0
			B:8'b1101_1110	1	1	0	1	1	1	1	0
			C:8'b1110_1010	1	1	0	1	1	0	1	0
F9	NVM_BUCKS_RANK_SHR	R/W	A:8'b1001_0010	BUCK4_RANK [1:0]		BUCK3_RANK [1:0]		BUCK2_RANK|1:0]		BUCK1_RANK [1:0]	
				1	0	0	1	0	0	1	0
			B:8'b1001_0010	1	0	0	1	0	0	1	0
			C:8'b0000_0000	0	0	0	0	0	0	0	0
FA	NVM_LDOS_RANK_SHR1	R/W	A:8'b1100_0000	LDO4_RANK [1:0]		LDO3_RANK [1:0]		LDO2_RANK|1:0]		LDO1_RANK [1:0]	
				1	1	0	0	0	0	0	0
			B:8'b1100_1000	1s	1	0	0	1	0	0	0
			C:8'b0000_0000	0	0	0	0	0	0	0	0
FB	NVM_LDOS_RANK_SHR2	R/W	A:8'b0000_0010	BUCK4_CLAMP	LDO3_BYPASS	REFDDR_RANK[1:0]		LDO6_RANK[1:0]		LDO5_RANK[1:0]	
				0	0	0	0	0	0	1	0
			B:8'b0000_0010	0s	0	0	0	0	0	1	0
			C:8'b0000_0000	0	0	0	0	0	0	0	0
FC	NVM_BUCKS_VOUT_SHR	R/W	A:8'b1111_0010	BUCK4_VOUT[1:0]		BUCK3_VOUT[1:0]		BUCK2_VOUT[1:0]		BUCK1_VOUT[1:0]	
				1	1	1	1	0	0	1	0
			B:8'b1101_0010	1s	1	0	1	0	0	1	0
			C:8'b0000_0000	0	0	0	0	0	0	0	0

chanhvinh.com

				BITS[7:0]							
@HEX	Register Name	R/W	Default	7	6	5	4	3	2	1	0
FD	NVM_LDOS_VOUT_SHR1	R/W	A:8'b1000_0000	SWOUT_BOOST_OVP	-	LDO3_VOUT[1:0]		LDO2_VOUT[1:0]		LDO1_VOUT[1:0]	
				1	0	0	0	0	0	0	0
			B:8'b1000_1000	1	0	0	0	1	0	0	0
			C:8'b1000 0000	1	0	0	1	1	0	1	0
FE	NVM_LDOS_VOUT_SHR2	R/W	A:8'b0000_0010	-	-	-	-	LDO6_VOUT[1:0]		LDO5_VOUT[1:0]	
				0	0	0	0	0	0	1	0
			B:8'b0000_0010	0	0	0	0	0	0	1	0
			C:8'b0000 0000	0	0	0	0	0	0	0	0
FF	NVM_I2C_ADDR_SHR	R/W	A:8'b0011_0011	-	I2C_ADDR[6:0						
				0	0	1	1	0	0	1	1
			B:8'b0011_0011	0	0	1	1	0	0	1	1
			C:8'b0011_0011	0	0	1	1	0	0	1	1

chanhvinh.com

chanhvinh.com

6.7.1 NVM main control shadow register (NVM_MAIN_CTRL_SHR)

Table 65. NVM_MAIN_CTRL_SHR

7	6	5	4	3	2	1	0
VINOK_HYS[1:0]		VINOK_THRES[1:0]		FORCE_LDO4	PEKYLKP_OFF	AUTO_TURN_ON	LOCK_OCP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xF8
Type: read write register
Default: depends on the part number, refer to Table 64. NVM shadow register map
Description: NVM main control shadow register.

[7:6]	**VINOK_HYS[1:0]**: VINOK threshold hysteresis 00 : 200 mV 01 : 300 mV 10: 400 mV 11: 500 mV
[5:4]	**VINOK_THRES[1:0]**: VINOK_Rise threshold voltage 00 : 3.1 V 01 : 3.3 V 10: 3.5 V 11: 4.0 V
[3]	**FORCE_LDO4**: 0: LDO4 starts with rank LDO4_RANK[1:0] **only** if VBUS_det turn-ON condition occurs 1: LDO4 starts with rank LDO4_RANK[1:0] every turn-ON condition
[2]	**PKEYLKP_OFF**: 0: Turn-OFF on long key press inactive 1: Turn-OFF on long key press active
[1]	**AUTO_TURN_ON**: 0: STPMIC1 does not start automatically on VIN rising 1: STPMIC1 starts automatically on VIN rising
[0]	**LOCK_OCP**: 0: STPMIC1 is turned OFF only if regulator related OCPOFF bit is set in Section 6.3.12 Bucks OCP turn-OFF control register (BUCKS_OCPOFF_CR) or Section 6.3.13 LDO OCP turn-OFF control register (LDOS_OCPOFF_CR) . 1: short-circuit turn-OFF STPMIC1 and keep it in LOCK_OCP state until LOCK_OCP_FLAG is reset Refer to Section 5.4.7 Overcurrent protection (OCP)

chanhvinh.com

6.7.2 NVM BUCK rank shadow register (NVM_BUCKS_RANK_SHR)

Table 66. NVM_BUCKS_RANK_SHR

7	6	5	4	3	2	1	0
BUCK4_RANK[1:0]		BUCK3_RANK[1:0]		BUCK2_RANK[1:0]		BUCK1_RANK [1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xF9
Type: read write register
Default: Depends on part number refer to Table 64. NVM shadow register map
Description: NVM buck rank shadow register.

[7:6]	**BUCK4_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3
[5:4]	**BUCK3_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3
[3:2]	**BUCK2_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3
[1:0]	**BUCK1_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3

chanhvinh.com

6.7.3 NVM LDOs rank shadow register 1 (NVM_LDOS_RANK_SHR1)

Table 67. **NVM_LDOS_RANK_SHR1**

7	6	5	4	3	2	1	0
LDO4_RANK[1:0]		LDO3_RANK[1:0]		LDO2_RANK[1:0]		LDO1_RANK[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFA
Type: read write register
Default: Depends on part number refer to Table 64. NVM shadow register map
Description: NVM LDOs rank shadow register 1.

[7:6]	**LDO4_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3
[5:4]	**LDO3_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3
[3:2]	**LDO2_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3
[1:0]	**LDO1_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3

chanhvinh.com

6.7.4 NVM LDOs rank shadow register 2 (NVM_LDOS_RANK_SHR2)

Table 68. NVM_LDOS_RANK_SHR2

7	6	5	4	3	2	1	0
BUCK4_CLAMP	LDO3_BYPASS	REFDDR_RANK[1:0]		LDO6_RANK[1:0]		LDO5_RANK[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFB
Type: read write register
Default: depends on part number refer to Table 64. NVM shadow register map
Description: NVM LDOs rank shadow register 2

[7]	**BUCK4_CLAMP**: Clamp Buck4 output value to 1.3 V max. 0: *VOUT[5:0]* of Buck4 is not clamped 1: *VOUT[5:0]* of Buck4 is clamped to b011100 (1.3 V)
[6]	**LDO3_BYPASS**: LDO3 forced bypass mode 0: LDO3 not in bypass mode 1: LDO3 in bypass mode
[5:4]	**REFDDR_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3
[3:2]	**LDO6_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3
[1:0]	**LDO5_RANK[1:0]**: 00: rank0 01: rank1 10: rank2 11: rank3

chanhvinh.com

6.7.5 NVM BUCKs voltage output shadow register (NVM_BUCKS_VOUT_SHR)

Table 69. **NVM_BUCKS_VOUT_SHR**

7	6	5	4	3	2	1	0
BUCK4_VOUT[1:0]		BUCK3_VOUT[1:0]		BUCK2_VOUT[1:0]		BUCK1_VOUT[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFC
Type: read write register
Default: depends on part number refer to Table 64. NVM shadow register map
Description: NVM Bucks VOUT register.

[7:6]	**BUCK4_VOUT[1:0]**: Buck4 default output selection 00: 1.15 V 01: 1.2 V 10: 1.8 V 11: 3.3 V
[5:4]	**BUCK3_VOUT[1:0]**: Buck3 default output selection 00: 1.2 V 01: 1.8 V 10: 3.0 V 11: 3.3 V
[3:2]	**BUCK2_VOUT[1:0]**: Buck2 default output selection 00: 1.1 V 01: 1.2 V 10: 1.35 V 11: 1.5 V
[1:0]	**BUCK1_VOUT[1:0]**: Buck1 default output selection 00: 1.1 V 01: 1.15 V 10: 1.2 V 11: 1.5 V

chanhvinh.com

6.7.6 NVM LDOs voltage output shadow register 1 (NVM_LDOS_VOUT_SHR1

Table 70. **NVM_LDOS_VOUT_SHR1**

7	6	5	4	3	2	1	0
SWOUT_BOOST_OVP	reserved	LDO3_VOUT[1:0]		LDO2_VOUT[1:0]		LDO1_VOUT[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFD
Type: read write register
Default: depends on part number refer to Table 64. NVM shadow register map
Description: NVM LDO1 to LDO3 default voltage output setting shadow register.

[7]	**SWOUT_BOOST_OVP**: 0: PWR_SW does not turn OFF if boost OVP occurs 1: PWR_SW is turned OFF automatically if Boost OVP occurs
[6]	reserved
[5:4]	**LDO3_VOUT[1:0]**: LDO3 default output selection 00: 1.8 V 01: 2.5 V 10: 3.3 V 11: *VOUT[5:0]* of Buck2 divided by 2
[3:2]	**LDO2_VOUT[1:0]**: LDO2 default output selection 00: 1.8 V 01: 2.5 V 10: 2.9 V 11: 3.3 V
[1:0]	**LDO1_VOUT[1:0]**: LDO1 default output selection 00: 1.8 V 01: 2.5 V 10: 2.9 V 11: 3.3 V

chanhvinh.com

6.7.7 NVM LDOs voltage output shadow register 2 (NVM_LDOS_VOUT_SHR2)

Table 71. **NVM_LDOS_VOUT_SHR2**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	LDO6_VOUT[1:0]		LDO5_VOUT[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFE
Type: read write register
Default: depends on part number refer to Table 64. NVM shadow register map
Description: NVM LDO5-6 voltage output shadow register.

[7:4]	reserved
[3:2]	**LDO6_VOUT[1:0]**: LDO6 default output selection 00: 1.0 V 01: 1.2 V 10: 1.8 V 11: 3.3 V
[1:0]	**LDO5_VOUT[1:0]**: LDO5 default output selection 00: 1.8 V 01: 2.5 V 10: 2.9 V 11 : 3.3 V

chanhvinh.com

6.7.8 NVM device address shadow register (I2C_ADDR_SHR)

Table 72. NVM_I2C_ADDR_AHR

7	6	5	4	3	2	1	0
reserved	I2C_ADDR[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFF
Type: read write register
Default: depends on part number refer to Table 64. NVM shadow register map
Description: NVM device address shadow register.

[7]	Reserved
[6:0]	**I2C_ADDR[6:0]**: I^2C device address. Warning: applied immediately, next access should use new address

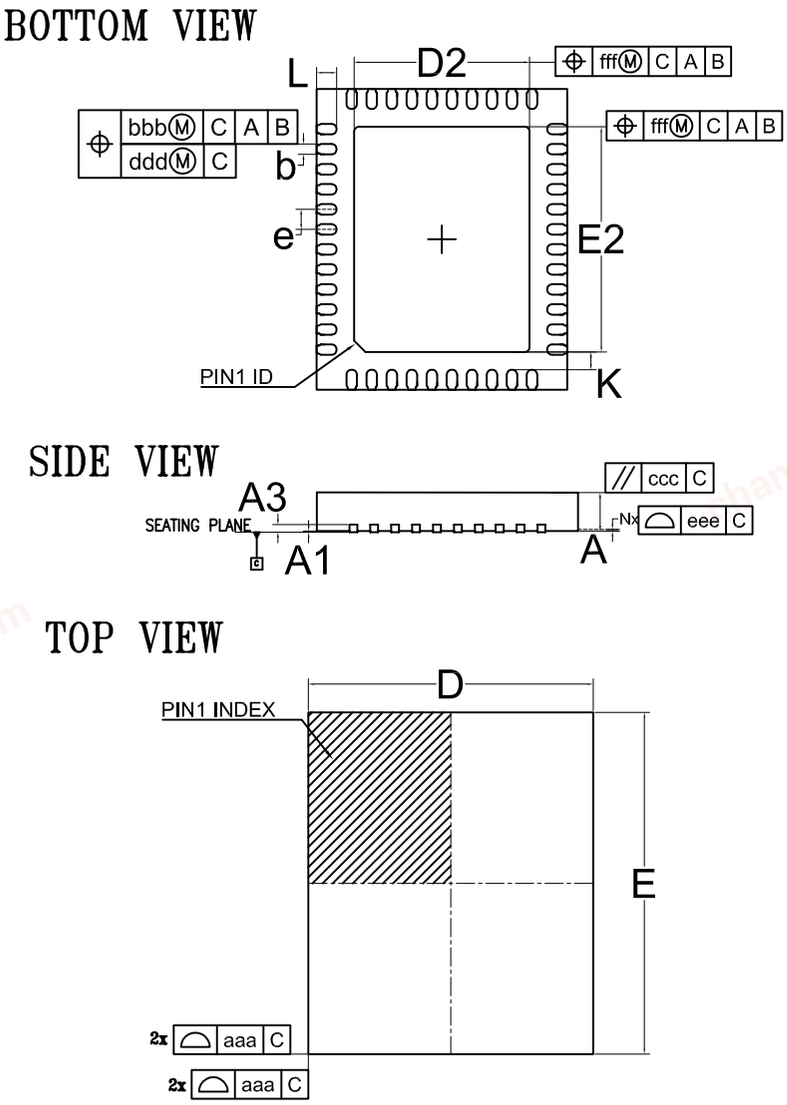
chanhvinh.com

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 WFQFN 44L (5X6X0.8) package information

Figure 64. WFQFN 44L (5X6X0.8) package outline

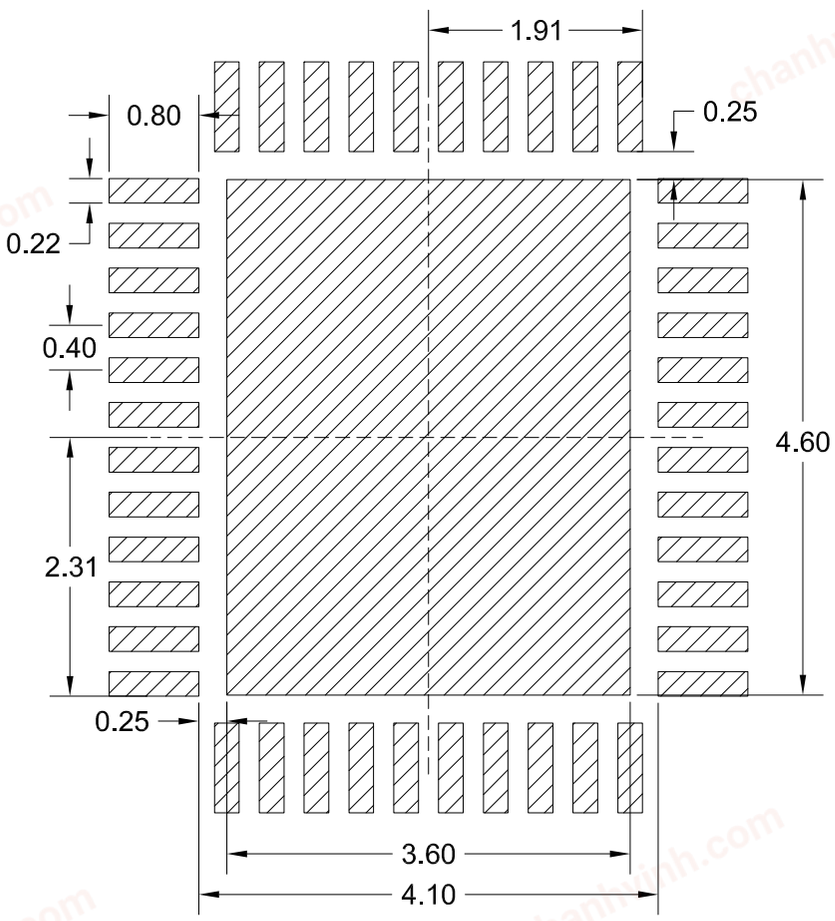


chanhvinh.com

Table 73. **WFQFN 44L (5X6X0.8) mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	0.65	0.75	0.80
A1	0.00	0.02	0.05
A3		0.2 REF	
b	0.16	0.21	0.26
D		5.00 BSC	
D2	3.40	3.50	3.60
e		0.40 BSC	
E		6.00 BSC	
E2	4.40	4.50	4.60
L	0.30	0.40	0.50
k	0.20		
N		44	

Figure 65. **WFQFN 44L (5X6X0.8) recommended footprint**



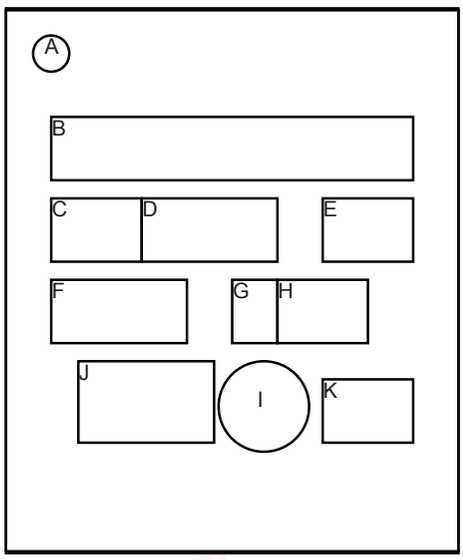
chanhvinh.com

8 Marking composition

Figure 66. **Marking composition**

MARKING COMPOSITION : VFQFPN 5.0 X 6.0 X 1 44L PITCH 0.4

PACKAGE FACE : TOP



LEGEND

Unmarkable surface

Marking composition field

A - 85256 - DOT
B - 85264 - MARKING AREA
C - 85263 - Assy Plant (PP)
D - 85262 - BE Sequence (LLL)
E - 85261 - Diffusion Traceability Plant (WX)
F - 85260 - COUNTRY OF ORIGIN (MAX CHAR ALLOWED = 3)
G - 85259 - Assy Year (Y)
H - 85258 - Assy Week (WW)
I - 85265 - Second_lvl_intct
J - 85255 - MARKING AREA
K - 85257 - ADDITIONAL INFORMATION (MAX CHAR ALLOWED = 2)

chanhvinh.com

9 Ordering information

Table 74. Ordering information

Order code	Part number	Marking	VIO (BUCK3) programming	Packing
STPMIC1APQR(1)	STPMIC1A	STPMIC1A	3.3 V(2)	WFQFN 44L (5x6x0.8)
STPMIC1BPQR(1)	STPMIC1B	STPMIC1B	1.8 V(2)	
STPMIC1CPQR(1)	STPMIC1C	STPMIC1C	Not programmed	
STPMIC1DPQR(1)	STPMIC1D	STPMIC1D	3.3 V(2)	
STPMIC1EPQR(1)	STPMIC1E	STPMIC1E	3.3 V(2)	

1. *xR= tape and reel packing*
2. *Refer to Table 1. Default NVM configuration vs part number for all default output voltages in NVM configuration.*

chanhvinh.com

Revision history

Table 75. **Document revision history**

Date	Version	Changes
26-Jun-2019	1	Initial release.
17-Oct-2019	2	Updated Table 4. Absolute maximum ratings, Table 7. Electrical and timing parameters and Table 11. Turn-on description. Updated Figure 66. Marking composition. Updated Section 4.5 Boost converter and power switches and Section 5.4.2 Turn-ON conditions.
30-Jan-2020	3	Updated Section 1 Device configuration, Section 5.5.2 Non-volatile memory (NVM) and Section 6.7.8 NVM device address shadow register (I2C_ADDR_SHR).
22-Jun-2020	4	Updated Table 3. Pin description, Table 4. Absolute maximum ratings, Table 7. Electrical and timing parameters and Table 18. Register map.
23-Sep-2020	5	Updated , Table 1. Default NVM configuration vs part number and Table 74. Ordering information. Updated Section 5.5.2 Non-volatile memory (NVM) and Section 6.2.6 Version status register (VERSION_SR).

chanhvinh.com

Contents

1 **Device configuration** . . . 2
2 **Typical application schematic** . . . 3
2.1 Recommended external components . . . 4
2.2 Pinout and pin description . . . 5
3 **Electrical and timing characteristics** . . . 7
3.1 Absolute maximum ratings . . . 7
3.2 Thermal characteristics . . . 7
3.3 Consumption in typical application scenarios . . . 8
3.4 Electrical and timing parameters . . . 9
3.5 Application board curves . . . 22
4 **Power regulators and switch description** . . . 27
4.1 Overview . . . 27
4.2 LDO regulators . . . 28
4.2.1 LDO regulators - common features . . . 28
4.2.2 LDO regulators - special features . . . 29
4.2.3 LDO output voltage settings . . . 30
4.3 DDR memory sub-system examples . . . 32
4.3.1 Powering lpDDR2/lpDDR3 memory . . . 32
4.3.2 Powering DDR3/DDR3L memory . . . 33
4.4 Buck converters . . . 33
4.4.1 BUCK general description . . . 33
4.4.2 BUCK output voltage settings . . . 39
4.5 Boost converter and power switches . . . 41
4.5.1 Boost converter . . . 41
4.5.2 PWR_USB_SW and PWR_SW power switches . . . 42
4.6 USB sub-system examples . . . 45
5 **Functional description** . . . 48
5.1 Overview . . . 48
5.2 Functional state machine . . . 48

chanhvinh.com

5.2.1 Main state machine diagram . . . 49
5.2.2 State explanations . . . 50
5.3 POWER_UP, POWER_DOWN sequence . . . 51
5.4 Feature description . . . 52
5.4.1 VIN conditions and monitoring . . . 52
5.4.2 Turn-ON conditions . . . 53
5.4.3 Turn-OFF conditions and restart_request . . . 55
5.4.4 Reset and mask_reset option . . . 56
5.4.5 Power control modes (MAIN / ALTERNATE) . . . 57
5.4.6 Thermal protection . . . 58
5.4.7 Overcurrent protection (OCP) . . . 59
5.4.8 BOOST overvoltage protection . . . 60
5.4.9 Watchdog feature . . . 60
5.5 Programming . . . 60
5.5.1 I^2C interface . . . 60
5.5.2 Non-volatile memory (NVM) . . . 61
6 Register description . . . 63
6.1 User register map . . . 63
6.2 Status registers . . . 70
6.2.1 Turn-ON status register (TURN_ON_SR) . . . 70
6.2.2 Turn-OFF status register (TURN_OFF_SR) . . . 71
6.2.3 Overcurrent protection LDO turn-OFF status register (OCP_LDOS_SR) . . . 72
6.2.4 Overcurrent protection buck turn-OFF status register (OCP_BUCKS_BSW_SR) . . . 73
6.2.5 Restart status register (RESTART_SR) . . . 74
6.2.6 Version status register (VERSION_SR) . . . 75
6.3 Control registers . . . 76
6.3.1 Main control register (MAIN_CR) . . . 76
6.3.2 Pads pull control register (PADS_PULL_CR) . . . 77
6.3.3 Bucks pull-down control register (BUCKS_PD_CR) . . . 78
6.3.4 LDO1-4 pull-down control register (LDO14_PD_CR) . . . 79
6.3.5 LDO5/6 pull-down control register (LDO56_VREF_PD_CR) . . . 80
6.3.6 PWR_SWOUT and VIN control register (SW_VIN_CR) . . . 81

chanhvinh.com

6.3.7 PONKEYn turn-OFF control register (PKEY_TURNOFF_CR) . . . 82
6.3.8 Mask reset Buck control register (BUCKS_MRST_CR) . . . 83
6.3.9 Mask reset LDO control register (LDOS_MRST_CR) . . . 84
6.3.10 Watchdog control register (WDG_CR) . . . 85
6.3.11 Watchdog timer control register (WDG_TMR_CR) . . . 86
6.3.12 Bucks OCP turn-OFF control register (BUCKS_OCPOFF_CR) . . . 87
6.3.13 LDO OCP turn-OFF control register (LDOS_OCPOFF_CR) . . . 88
6.4 Power supplies control registers . . . 89
6.4.1 BUCKx MAIN mode control registers (BUCKx_MAIN_CR) (x=1...4) . . . 89
6.4.2 REFDDR MAIN mode control register (REFDDR_MAIN_CR) . . . 90
6.4.3 LDOx MAIN mode control registers (LDOx_MAIN_CR) (x=1, 2, 5, 6) . . . 91
6.4.4 LDO3 MAIN mode control register (LDO3_MAIN_CR) . . . 92
6.4.5 LDO4 MAIN mode control register (LDO4_MAIN_CR) . . . 93
6.4.6 BUCKx ALTERNATE mode control registers (BUCKx_ALT_CR)(x=1..4) . . . 94
6.4.7 REFDDR ALTERNATE mode control register (REFDDR_ALT_CR) . . . 95
6.4.8 LDOx ALTERNATE mode control registers (LDOx_ALT_CR) (x=1, 2, 5, 6) . . . 96
6.4.9 LDO3 ALTERNATE mode control register (LDO3_ALT_CR) . . . 97
6.4.10 LDO4 ALTERNATE mode control register (LDO4_ALT_CR) . . . 98
6.4.11 Boost/switch control register (BST_SW_CR) . . . 99
6.5 Interrupt registers . . . 100
6.5.1 Overall interrupt register behavior . . . 100
6.5.2 Interrupt pending register 1 (INT_PENDING_R1) . . . 101
6.5.3 Interrupt pending register 2 (INT_PENDING_R2) . . . 102
6.5.4 Interrupt pending register 3 (INT_PENDING_R3) . . . 103
6.5.5 Interrupt pending register 4 (INT_PENDING_R4) . . . 104
6.5.6 Interrupt debug latch registers (INT_DBG_LATCH_Rx) . . . 105
6.5.7 Interrupt clear registers (INT_CLEAR_Rx) . . . 106
6.5.8 Interrupt mask registers (INT_MASK_Rx) . . . 107
6.5.9 Interrupt set mask registers (INT_SET_MASK_Rx) . . . 108
6.5.10 Interrupt clear mask registers (INT_CLEAR_MASK_Rx) . . . 109
6.5.11 Interrupt source register 1 (INT_SRC_R1) . . . 110
6.5.12 Interrupt source register 2 (INT_SRC_R2) . . . 111

chanhvinh.com

6.5.13 Interrupt source register 3 (INT_SRC_R3) . . . 112
6.5.14 Interrupt source register 4 (INT_SRC_R4) . . . 113
6.6 NVM registers . . . 114
6.6.1 NVM status register (NVM_SR) . . . 114
6.6.2 NVM control register (NVM_CR) . . . 115
6.7 NVM shadow registers . . . 116
6.7.1 NVM main control shadow register (NVM_MAIN_CTRL_SHR) . . . 119
6.7.2 NVM BUCK rank shadow register (NVM_BUCKS_RANK_SHR) . . . 120
6.7.3 NVM LDOs rank shadow register 1 (NVM_LDOS_RANK_SHR1) . . . 121
6.7.4 NVM LDOs rank shadow register 2 (NVM_LDOS_RANK_SHR2) . . . 122
6.7.5 NVM BUCKs voltage output shadow register (NVM_BUCKS_VOUT_SHR) . . . 123
6.7.6 NVM LDOs voltage output shadow register 1 (NVM_LDOS_VOUT_SHR1 . . . 124
6.7.7 NVM LDOs voltage output shadow register 2 (NVM_LDOS_VOUT_SHR2) . . . 125
6.7.8 NVM device address shadow register (I2C_ADDR_SHR) . . . 126
7 Package information . . . 127
7.1 WFQFN 44L (5x6x0.8) package information . . . 127
8 Marking composition . . . 129
9 Ordering information . . . 130
Revision history . . . 131

chanhvinh.com

List of tables

Table 1. Default NVM configuration vs part number . . . 2
Table 2. Passive components . . . 4
Table 3. Pin description . . . 5
Table 4. Absolute maximum ratings . . . 7
Table 5. Thermal characteristics . . . 7
Table 6. Consumption in typical application scenarios . . . 8
Table 7. Electrical and timing parameters . . . 9
Table 8. General description . . . 27
Table 9. LDO output voltage settings . . . 30
Table 10. BUCK output settings . . . 39
Table 11. Turn-on description . . . 54
Table 12. Turn-off conditions . . . 55
Table 13. MAIN/ALTERNATE switch example configuration . . . 58
Table 14. OCP levels . . . 59
Table 15. Device ID format . . . 60
Table 16. Register address format . . . 60
Table 17. Register data format . . . 61
Table 18. Register map . . . 64
Table 19. TURN_ON_SR . . . 70
Table 20. TURN_OFF_SR . . . 71
Table 21. OCP_LDOS_SR . . . 72
Table 22. OCP_BUCKS_BSW_SR . . . 73
Table 23. RESTART_SR . . . 74
Table 24. VERSION_SR . . . 75
Table 25. MAIN_CR . . . 76
Table 26. PADS_PULL_CR . . . 77
Table 27. BUCKS_PD_CR . . . 78
Table 28. LDO14_PD_CR . . . 79
Table 29. LDO56_VREF_PD_CR . . . 80
Table 30. SW_VIN_CR . . . 81
Table 31. PKEY_TURNOFF_CR . . . 82
Table 32. BUCKS_MRST_CR . . . 83
Table 33. LDOS_MRST_CR . . . 84
Table 34. WDG_CR . . . 85
Table 35. WDG_TMR_CR . . . 86
Table 36. BUCKS_OCPOFF_CR . . . 87
Table 37. LDOS_OCPOFF_CR . . . 88
Table 38. BUCKx_MAIN_CR . . . 89
Table 39. REFDDR_MAIN_CR . . . 90
Table 40. LDOx_MAIN_CR . . . 91
Table 41. LDO3_MAIN_CR . . . 92
Table 42. LDO4_MAIN_CR . . . 93
Table 43. BUCKx_ALT_CR . . . 94
Table 44. REFDDR_ALT_CR . . . 95
Table 45. LDOx_ALT_CR . . . 96
Table 46. LDO3_ALT_CR . . . 97
Table 47. LDO4_ALT_CR . . . 98
Table 48. BST_SW_CR . . . 99
Table 49. INT_PENDING_R1 . . . 101
Table 50. INT_PENDING_R2 . . . 102
Table 51. INT_PENDING_R3 . . . 103
Table 52. INT_PENDING_R4 . . . 104

chanhvinh.com

Table 53. INT_DBG_LATCH_Rx . . . 105
Table 54. INT_CLEAR_Rx . . . 106
Table 55. INT_MASK_Rx . . . 107
Table 56. INT_SET_MASK_Rx . . . 108
Table 57. INT_CLEAR_MASK_Rx . . . 109
Table 58. INT_SRC_R1 . . . 110
Table 59. INT_SRC_R2 . . . 111
Table 60. INT_SRC_R3 . . . 112
Table 61. INT_SRC_R4 . . . 113
Table 62. NVM_SR . . . 114
Table 63. NVM_CR . . . 115
Table 64. NVM shadow register map . . . 117
Table 65. NVM_MAIN_CTRL_SHR . . . 119
Table 66. NVM_BUCKS_RANK_SHR . . . 120
Table 67. NVM_LDOS_RANK_SHR1 . . . 121
Table 68. NVM_LDOS_RANK_SHR2 . . . 122
Table 69. NVM_BUCKS_VOUT_SHR . . . 123
Table 70. NVM_LDOS_VOUT_SHR1 . . . 124
Table 71. NVM_LDOS_VOUT_SHR2 . . . 125
Table 72. NVM_I2C_ADDR_AHR . . . 126
Table 73. WFQFN 44L (5X6X0.8) mechanical data . . . 128
Table 74. Ordering information . . . 130
Table 75. Document revision history . . . 131

chanhvinh.com

List of figures

Figure 1. Typical application schematic . . . 3
Figure 2. Pin configuration WFQFN 44L top view . . . 5
Figure 3. BUCK1 efficiency . . . 22
Figure 4. BUCK2 efficiency . . . 22
Figure 5. BUCK3 efficiency . . . 22
Figure 6. BUCK4 efficiency . . . 22
Figure 7. Boost efficiency . . . 22
Figure 8. Boost powered by 5 V supply having poor performance . . . 22
Figure 9. BUCK1 load transient in HP mode . . . 23
Figure 10. Buck1 load transient in LP mode . . . 23
Figure 11. BUCK2 load transient in HP mode . . . 23
Figure 12. Buck2 load transient in LP mode . . . 23
Figure 13. Buck3 load transient in HP mode . . . 23
Figure 14. Buck3 load transient in LP mode . . . 23
Figure 15. Buck4 load transient in HP mode . . . 23
Figure 16. Buck4 load transient in LP mode . . . 23
Figure 17. LDO1 load transient . . . 24
Figure 18. LDO2 load transient . . . 24
Figure 19. LDO3 load transient . . . 24
Figure 20. LDO4 load transient . . . 24
Figure 21. LDO5 load transient . . . 24
Figure 22. LDO6 load transient . . . 24
Figure 23. LDO4 line transient . . . 24
Figure 24. Boost output vs. input voltage . . . 24
Figure 25. Boost load regulation 5 V_{IN} . . . 25
Figure 26. Boost load regulation 3.6 V_{IN} . . . 25
Figure 27. LDO1 line transient, no load . . . 25
Figure 28. LDO2 line transient, no load . . . 25
Figure 29. LDO3 line transient, no load . . . 25
Figure 30. LDO5 line transient, no load . . . 25
Figure 31. LDO6 line transient, no load . . . 25
Figure 32. LDO3 sink/source mode load transient response . . . 25
Figure 33. Buck1 turn-ON waveform . . . 26
Figure 34. STPMIC1A POWER_UP sequencing . . . 26
Figure 35. STPMIC1A POWER_UP sequencing PONKEYn . . . 26
Figure 36. STPMIC1A POWER_DOWN sequencing . . . 26
Figure 37. STPMIC1A reset sequencing . . . 26
Figure 38. LDO start-up/shutdown timings . . . 29
Figure 39. Powering lpDDR2/lpDDR3 memory (LDO3 in bypass mode) . . . 32
Figure 40. Powering lpDDR2/lpDDR3 memory (LDO3 normal mode supplied from VIN) . . . 32
Figure 41. Powering DDR3/DDR3L memory (LDO3 in sink/source mode) . . . 33
Figure 42. PWM clock generation . . . 34
Figure 43. PWM clock synchronisation . . . 34
Figure 44. Buck block diagram . . . 35
Figure 45. BUCKx LP to HP mode recovery time . . . 36
Figure 46. BUCKx start-up/shutdown timings . . . 37
Figure 47. BUCKx dynamic voltage scaling (DVS) . . . 38
Figure 48. Boost and switch block diagram . . . 41
Figure 49. Boost start-up sequence . . . 42
Figure 50. Battery powered application with a USB OTG port and a USB host port . . . 45
Figure 51. Battery powered application with a single USB OTG port . . . 46

chanhvinh.com

Figure 52. 5 V DC powered application with a USB OTG port and two USB host ports 47
Figure 53. STPMIC1 state machine 49
Figure 54. STPMIC1 POWER_UP and POWER_DOWN sequence example 51
Figure 55. VIN monitoring thresholds 52
Figure 56. Auto turn-on condition sequence 53
Figure 57. Turn-on condition after $V_{IN_POR_RISE}$ 54
Figure 58. Turn-on condition before $V_{IN_POR_Rise}$ 55
Figure 59. Reset power-cycle sequence 57
Figure 60. Power mode switch sequence example 58
Figure 61. Thermal protection thresholds 59
Figure 62. I^2C read operation. 61
Figure 63. I^2C write operation 61
Figure 64. WFQFN 44L (5X6X0.8) package outline 127
Figure 65. WFQFN 44L (5X6X0.8) recommended footprint 128
Figure 66. Marking composition 129

chanhvinh.com

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved