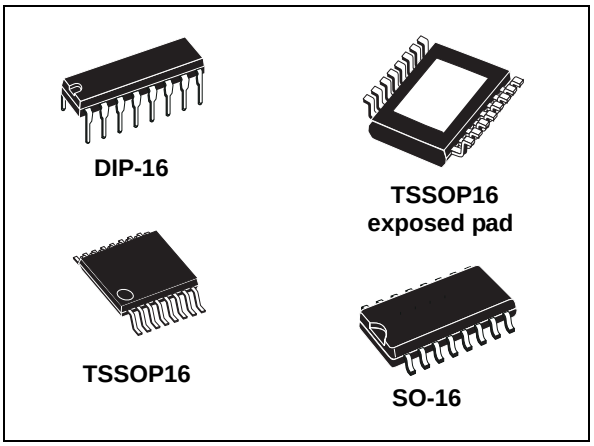
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# STP08CP05

## Low voltage, low current power 8-bit shift register

**Datasheet - production data**




## Features

- Low voltage power supply down to 3 V
- 8 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- 3.3 V micro driver-able
- Output current: 5-100 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection 2.5 kV HBM, 200 V MM

## Description

The STP08CP05 is a monolithic, low voltage, low current, power 8-bit shift register designed for LED panel displays. The STP08CP05 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. In the output stage, eight regulated current sources were designed to provide 5-100 mA constant current to drive the LEDs, the output current setup time is 11 ns (typ), thus improving the system performance.

The STP08CP05 is backward compatible in functionality and footprint with STP8C/L596. Through an external resistor, users can adjust the STP08CP05 output current, controlling in this way the light intensity of LEDs, in addition, user can adjust LED's brightness intensity from 0% to 100% via $\overline{OE}$ pin.

The STP08CP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, also satisfies the system requirement of high volume data transmission. The 3.3 V of voltage supply is useful for applications that interface with any micro from 3.3 V. Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a 2.5 factor.

**Table 1. Device summary**

| Order codes | Package | Packaging |
|---|---|---|
| STP08CP05B1R | DIP-16 | 25 parts per tube |
| STP08CP05MTR | SO-16 (Tape and reel) | 2500 parts per reel |
| STP08CP05TTR | TSSOP16 (Tape and reel) | 2500 parts per reel |
| STP08CP05XTTR | TSSOP16 exposed pad (Tape and reel) | 2500 parts per reel |



This is information on a product in full production. www.st.com

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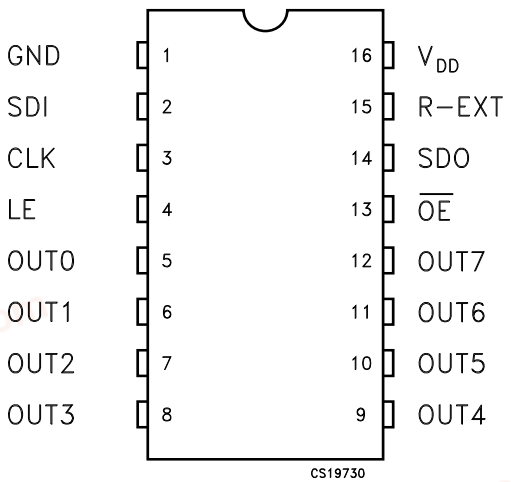
# 1 Summary description

**Table 2. Typical current accuracy**

| Output voltage | Current accuracy | | Output current |
|---|---|---|---|
| | Between bits | Between ICs | |
| ≥ 1.3 V | ± 1.5% | ± 3% | 20 to 100 mA |

## 1.1 Pin connection and description

**Figure 1. Connections diagram**




*Note: The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.*

**Table 3. Pin description**

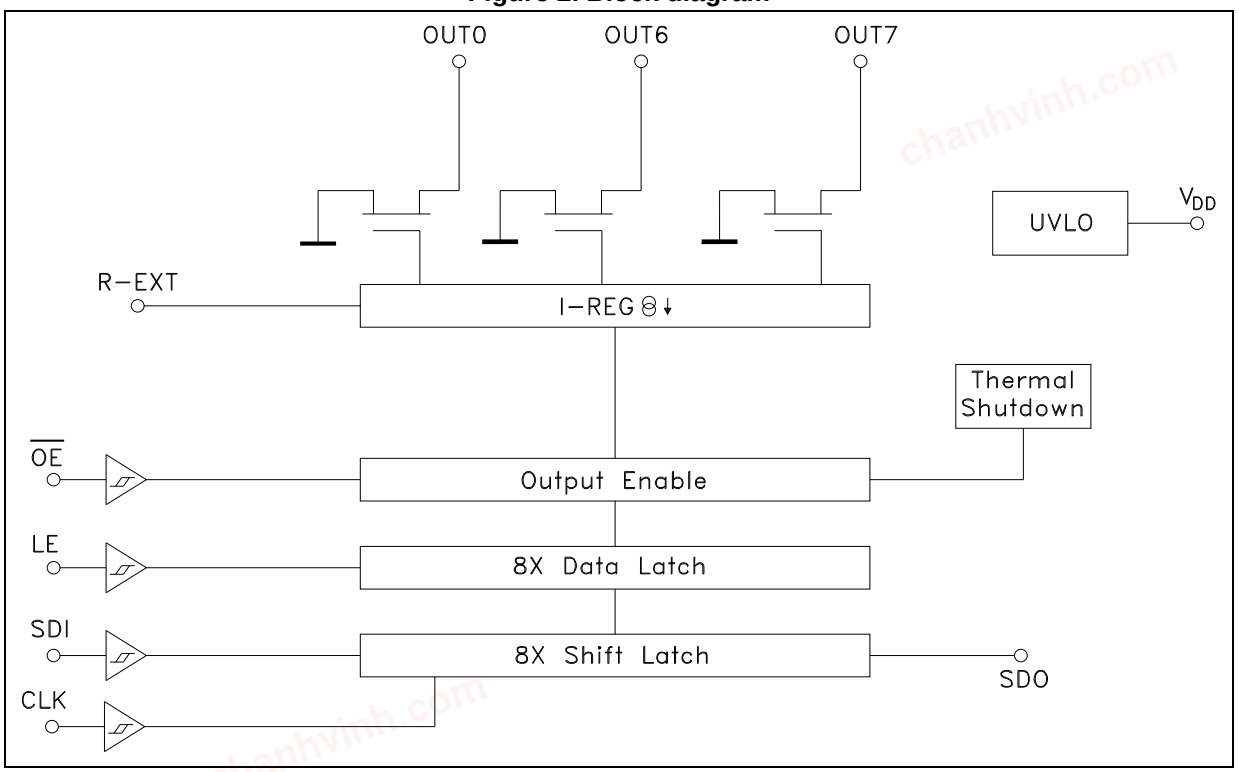
| Pin N° | Symbol | Name and function |
|---|---|---|
| 1 | GND | Ground terminal |
| 2 | SDI | Serial data input terminal |
| 3 | CLK | Clock input terminal |
| 4 | LE | Latch input terminal |
| 5-12 | OUT 0-7 | Output terminal |
| 13 | $\overline{OE}$ | Output enable input terminal (active low) |
| 14 | SDO | Serial data out terminal |
| 15 | R-EXT | Constant current programming |
| 16 | $V_{DD}$ | 5 V supply voltage terminal |

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# 2 Block diagram

**Figure 2. Block diagram**



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# 3 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. these are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 3.1 Absolute maximum ratings

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply voltage $I_{GND}$ | 0 to 7 | V |
| $V_O$ | Output voltage | -0.5 to 20 | V |
| $I_O$ | Output current | 100 | mA |
| $I_{GND}$ | GND terminal current | 800 | mA |
| $f_{CLK}$ | Clock frequency | 50 | MHz |
| $T_{OPR}$ | Operating temperature range | -40 to +125 | °C |
| $T_{STG}$ | Storage temperature range | -55 to +150 | °C |

## 3.2 Thermal data

**Table 5. Thermal data**

| Symbol | Parameter | DIP-16 | SO-16 | TSSOP16 | TSSOP16 (1) exposed pad | Unit |
|---|---|---|---|---|---|---|
| $R_{thJA}$ | Thermal resistance junction-ambient | 90 | 125 | 140 | 37.5 | °C/W |

1. The exposed-pad should be soldered to the PBC to realize the thermal benefits

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## 3.3 Recommended operating conditions

**Table 6. Recommended operating conditions**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 3.0 | | 5.5 | V |
| $V_O$ | Output voltage | | | | 20 | V |
| $I_O$ | Output current | OUTn | 5 | | 100 | mA |
| $I_{OH}$ | Output current | SERIAL-OUT | | | +1 | mA |
| $I_{OL}$ | Output current | SERIAL-OUT | | | -1 | mA |
| $V_{IH}$ | Input voltage | | 0.7 $V_{DD}$ | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input voltage | | -0.3 | | 0.3 $V_{DD}$ | V |
| $t_{wLAT}$ | LE pulse width | $V_{DD}$ = 3.0 to 5.0 V | 20 | | | ns |
| $t_{wCLK}$ | CLK pulse width | | 20 | | | ns |
| $t_{wEN}$ | $\overline{OE}$ pulse width | | 200 | | | ns |
| $t_{SETUP(D)}$ | Setup time for DATA | | 7 | | | ns |
| $t_{HOLD(D)}$ | Hold time for DATA | | 4 | | | ns |
| $t_{SETUP(L)}$ | Setup time for LATCH | | 15 | | | ns |
| $f_{CLK}$ | Clock frequency | Cascade operation (1) | | | 30 | MHz |

1. In order to achieve high cascade data transfer, please consider $t_r/t_f$ timings carefully.

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# 4 Electrical characteristics

$V_{DD}$ = 3.3 V to 5 V, T = 25 °C, unless otherwise specified.

**Table 7. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage high level | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Input voltage low level | | GND | | 0.3$V_{DD}$ | V |
| $I_{OH}$ | Output leakage current | $V_{OH}$ = 20 V | | 0.5 | 10 | µA |
| $V_{OL}$ | Output voltage (Serial-OUT) | $I_{OL}$ = 1 mA | | 0.03 | 0.4 | V |
| $V_{OH}$ | Output voltage (Serial-OUT) | $I_{OH}$ = -1 mA | $V_{OH}$ - $V_{DD}$ =- 0.4 V | | | V |
| $I_{OL1}$ | Output current | $V_O$ = 0.3 V, $R_{ext}$ = 3.9 kΩ | 4.25 | 5 | 5.75 | mA |
| $I_{OL2}$ | | $V_O$ = 0.3 V, $R_{ext}$ = 970 Ω | 19.4 | 20 | 20.6 | |
| $I_{OL3}$ | | $V_O$ = 1.3 V, $R_{ext}$ = 190 Ω | 97 | 100 | 103 | |
| $\Delta I_{OL1}$ | Output current error between bit (All Output ON) | $V_O$ = 0.3 $VR_{EXT}$ = 3.9 kΩ | | ± 5 | ± 8 | % |
| $\Delta I_{OL2}$ | | $V_O$ = 0.3 $VR_{EXT}$ = 970 Ω | | ± 1.5 | ± 2.75 | |
| $\Delta I_{OL3}$ | | $V_O$ = 1.3 $VR_{EXT}$ =190 Ω | | ± 1.2 | ± 2.5 | |
| $R_{SIN(up)}$ | Pull-up resistor | | 150 | 300 | 600 | KΩ |
| $R_{SIN(down)}$ | Pull-down resistor | | 100 | 200 | 400 | KΩ |
| $I_{DD(OFF1)}$ | Supply current (OFF) | $R_{EXT}$ = 980 OUT 0 to 7 = OFF | | 4 | 5 | mA |
| $I_{DD(OFF2)}$ | | $R_{EXT}$ = 250 OUT 0 to 7 = OFF | | 11.2 | 13.5 | |
| $I_{DD(ON1)}$ | Supply current (ON) | $R_{EXT}$ = 980 OUT 0 to 7 = ON | | 4.5 | 5 | |
| $I_{DD(ON2)}$ | | $R_{EXT}$ = 250 OUT 0 to 7 = ON | | 11.7 | 13.5 | |
| Thermal | Thermal protection (1) | | | 170 | | °C |

1. Guaranteed by design (not tested)
The thermal protection switches OFF only the outputs

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# 5 Switching characteristics

$V_{DD}$ = 5 V, T = 25 °C, unless otherwise specified.

**Table 8. Switching characteristics**

| Symbol | Parameter | Test conditions | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH1}$ | Propagation delay time, CLK-OUTn, LE = H, OE = L | $V_{DD}$ = 3.3 V<br>$V_{IL}$ = GND<br>$I_O$ = 20 mA<br>$R_{EXT}$ = 1 KΩ | $V_{IH}$ = $V_{DD}$<br>$C_L$ = 10 pF<br>$V_L$ = 3.0 V<br>$R_L$ = 60 Ω | $V_{DD}$ = 3.3 V | | 35 | 50 | ns |
| | | | | $V_{DD}$ = 5 V | | 18 | 28 | |
| $t_{PLH2}$ | Propagation delay time, LE -OUTn, OE = L | | | $V_{DD}$ = 3.3 V | | 48 | 74 | ns |
| | | | | $V_{DD}$ = 5 V | | 30 | 50 | |
| $t_{PLH3}$ | Propagation delay time, OE -OUTn, LE = H | | | $V_{DD}$ = 3.3 V | | 55 | 82 | ns |
| | | | | $V_{DD}$ = 5 V | | 37 | 58 | |
| $t_{PLH}$ | Propagation delay time, CLK-SDO | | | $V_{DD}$ = 3.3 V | | 21 | 28 | ns |
| | | | | $V_{DD}$ = 5 V | | 17 | 22 | |
| $t_{PHL1}$ | Propagation delay time, CLK-OUTn, LE = H, OE = L | | | $V_{DD}$ = 3.3 V | | 11 | 17 | ns |
| | | | | $V_{DD}$ = 5 V | | 7 | 11 | |
| $t_{PHL2}$ | Propagation delay time, LE -OUTn, OE = L | | | $V_{DD}$ = 3.3 V | | 24 | 40 | ns |
| | | | | $V_{DD}$ = 5 V | | 21 | 31 | |
| $t_{PHL3}$ | Propagation delay time, OE -OUTn, LE = H | | | $V_{DD}$ = 3.3 V | | 20 | 35 | ns |
| | | | | $V_{DD}$ = 5 V | | 18 | 28 | |
| $t_{PHL}$ | Propagation delay time, CLK-SDO | | | $V_{DD}$ = 3.3 V | | 24 | 32 | ns |
| | | | | $V_{DD}$ = 5 V | | 19 | 25 | |
| $t_{ON}$ | Output fall time 10~90% of voltage waveform | | | $V_{DD}$ = 3.3 V | | 26 | 40 | ns |
| | | | | $V_{DD}$ = 5 V | | 11 | 17 | |
| $t_{OFF}$ | Output rise time 90~10% of voltage waveform | | | $V_{DD}$ = 3.3 V | | 5 | 10 | ns |
| | | | | $V_{DD}$ = 5 V | | 4 | 8 | |
| $t_r$ | CLK rise time (1) | | | | | | 5000 | ns |
| $t_f$ | CLK fall time (1) | | | | | | 5000 | ns |

1. In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

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# 6 Equivalent circuit and outputs

**Figure 3. $\overline{OE}$ terminal**

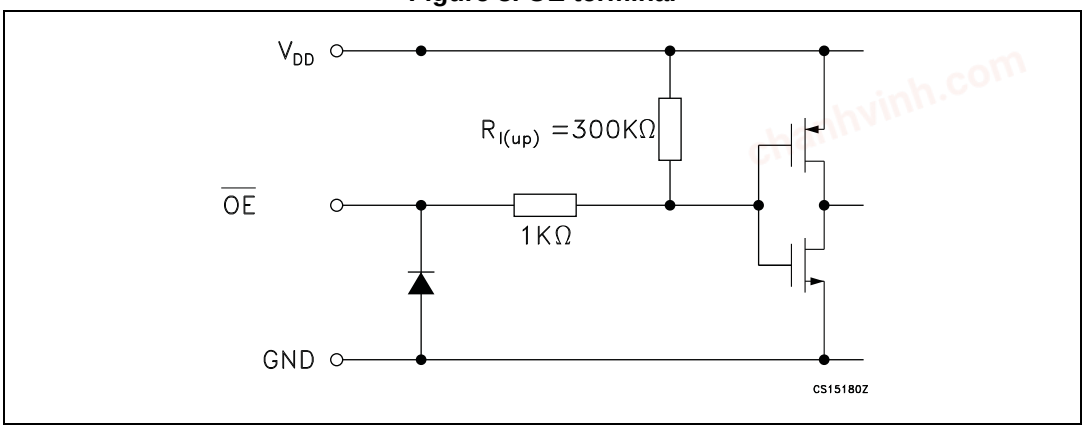



**Figure 4. LE terminal**

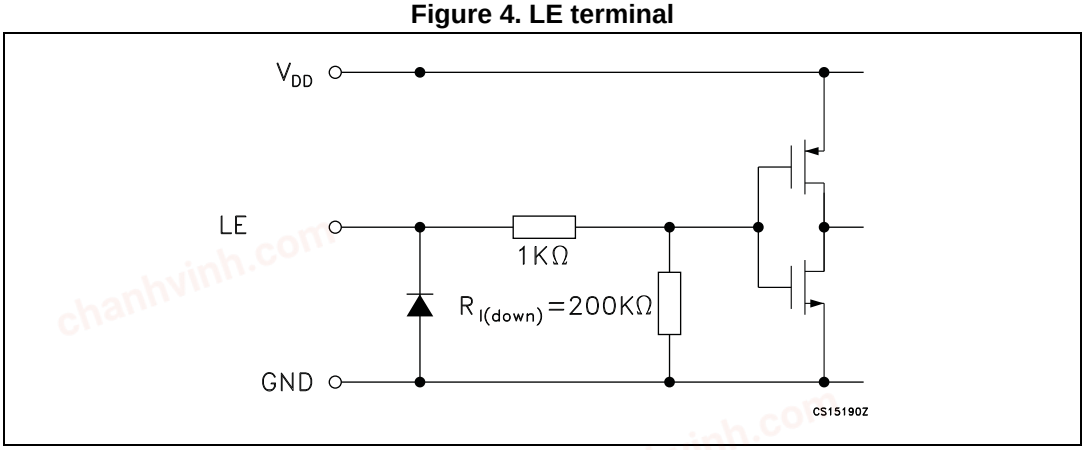
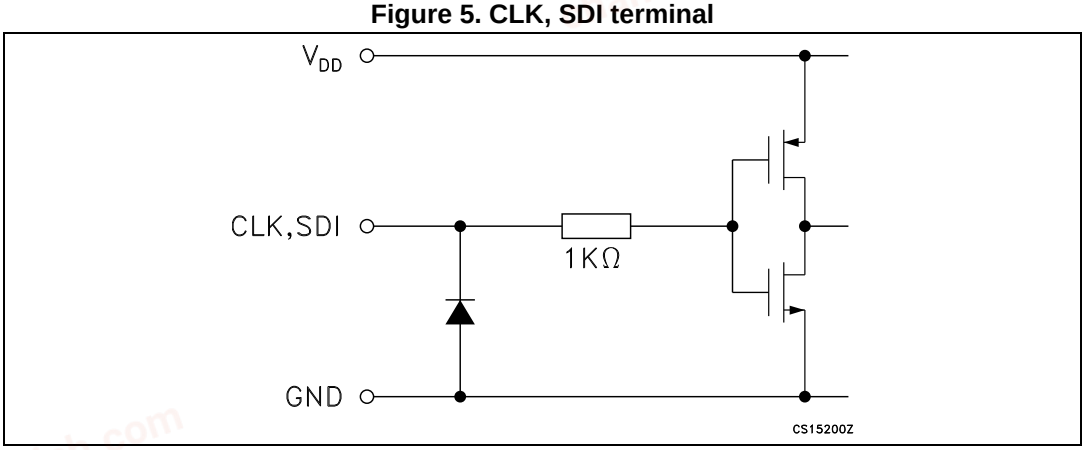


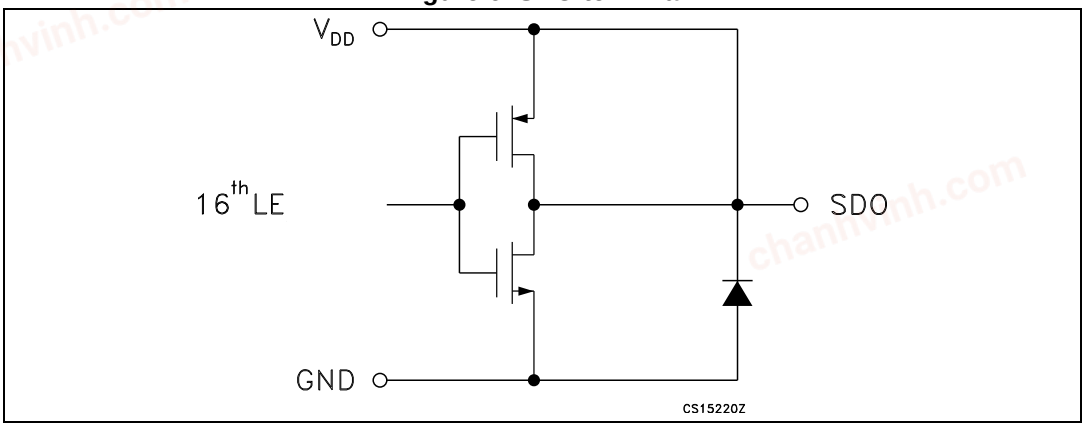

**Figure 5. CLK, SDI terminal**



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Figure 6. SDO terminal



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# 7 Truth table and timing diagram

## 7.1 Truth table

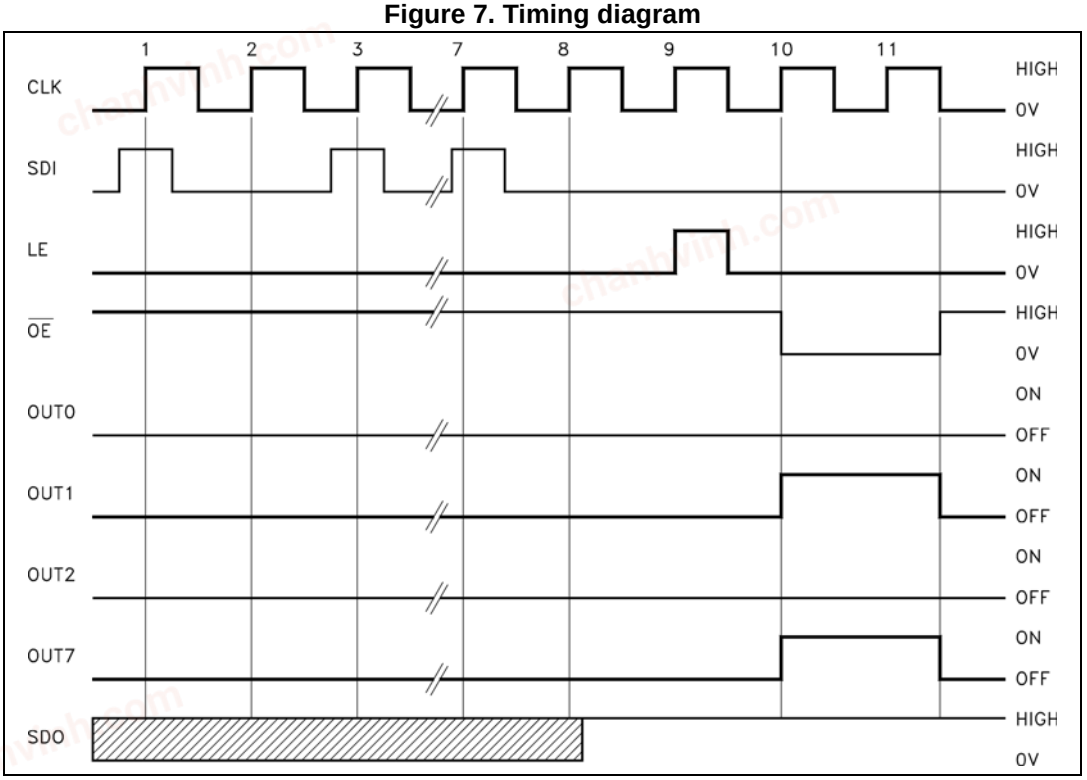
**Table 9. Truth table**

| Clock | $\overline{LE}$ | $\overline{OE}$ | SDI | $\overline{OUT0}$ ..... $\overline{OUT0}$ ..... $\overline{OUT7}$ | SDO |
|---|---|---|---|---|---|
| ↑ | H | L | Dn | Dn ..... Dn -5 ..... Dn -7 | Dn -7 |
| ↑ | L | L | Dn + 1 | No change | Dn -7 |
| ↑ | H | L | Dn + 2 | $\overline{Dn+2}$ ..... $\overline{Dn-3}$ ..... $\overline{Dn-5}$ | Dn -5 |
| ↓ | X | L | Dn + 3 | $\overline{Dn+2}$ ..... $\overline{Dn-3}$ ..... $\overline{Dn-5}$ | Dn -5 |
| ↓ | X | H | Dn + 3 | OFF | Dn -5 |

*Note: OUT0 to OUT7 = ON when Dn = H; OUT0 to OUT7 = OFF when Dn = L.*

## 7.2 Timing diagram

**Figure 7. Timing diagram**



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Figure 8. Clock, serial-in, serial-out

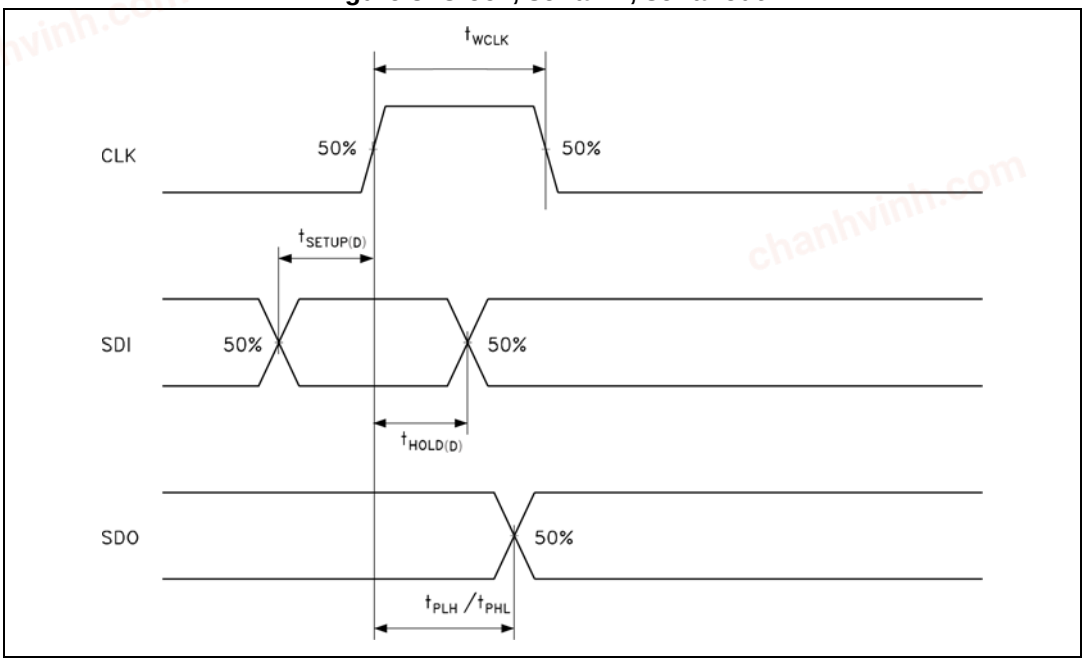
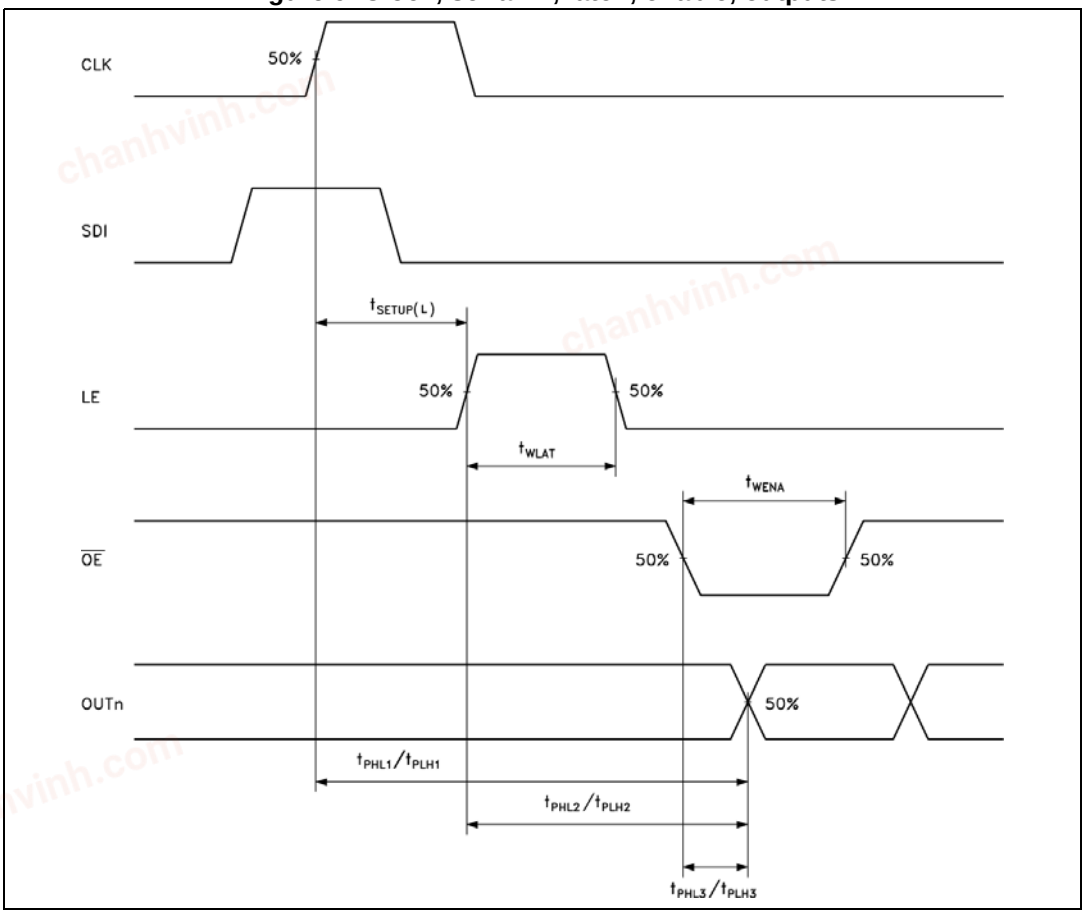


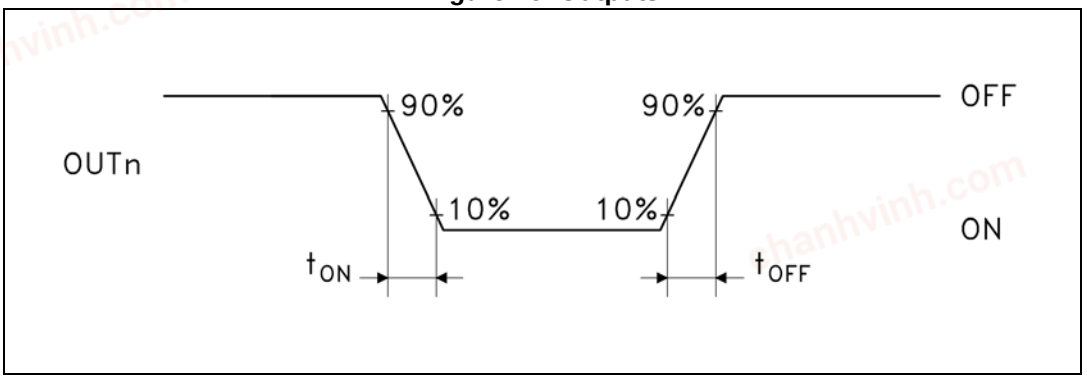

Figure 9. Clock, serial-in, latch, enable, outputs



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**Figure 10. Outputs**

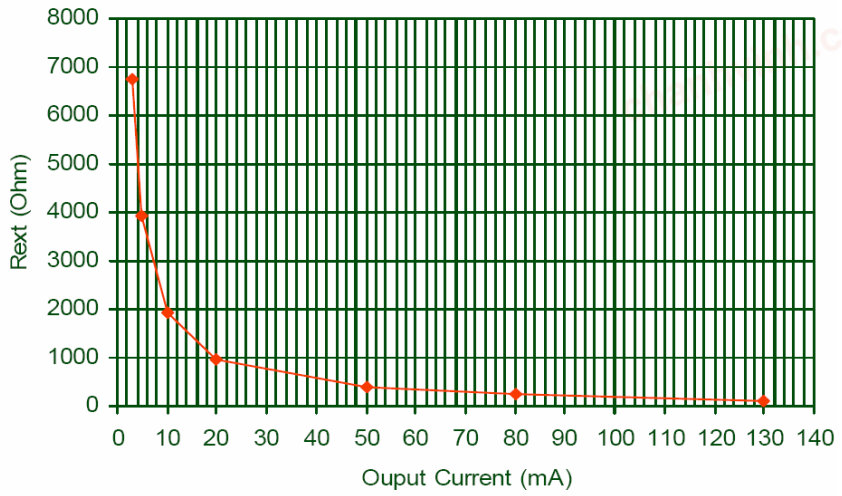


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# 8 Typical characteristics

**Figure 11. Output current-$R_{EXT}$ resistor**




$T_A$ = 25 °C, Iset = 3 mA; 5 mA; 10 mA; 20 mA; 50 mA; 80 mA; Max

**Table 10. Output current-$R_{EXT}$ resistor**

| Output current (mA) | 3 | 5 | 10 | 20 | 50 | 80 | 130 |
|---|---|---|---|---|---|---|---|
| Rext (Ω) | 6740 | 3930 | 1913 | 963 | 386 | 241 | 124 |

*Note: Maximum output current capabilities setting was 130 mA applying an Rext = 124 Ω.*

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Figure 12. $I_{SET}$ vs. drop out voltage ($V_{DROP}$)

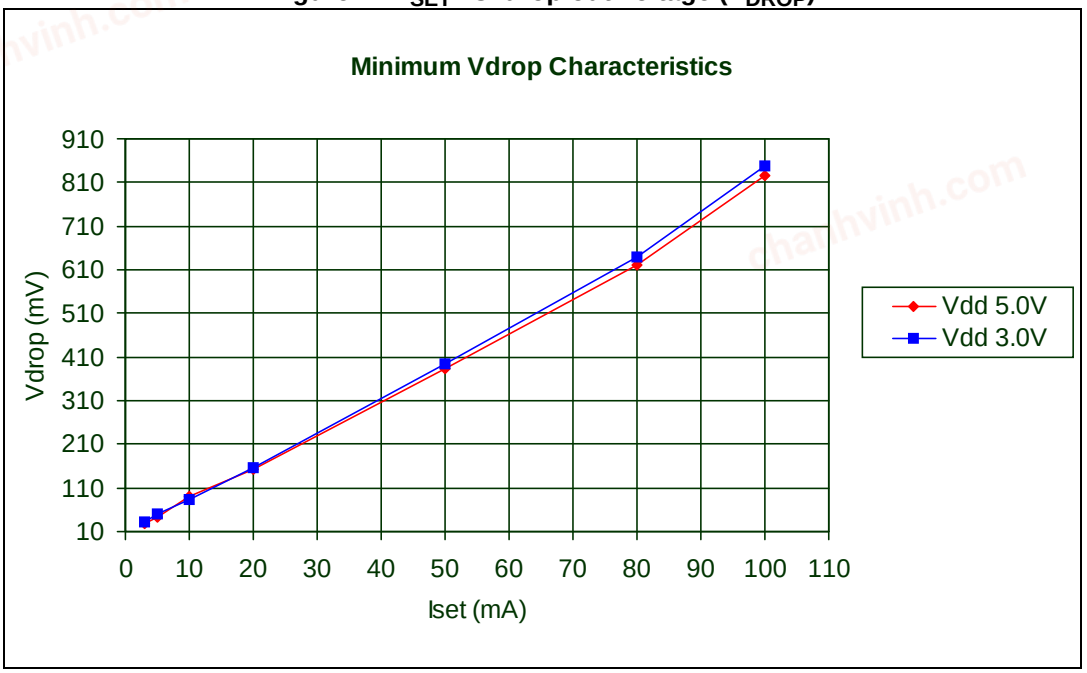


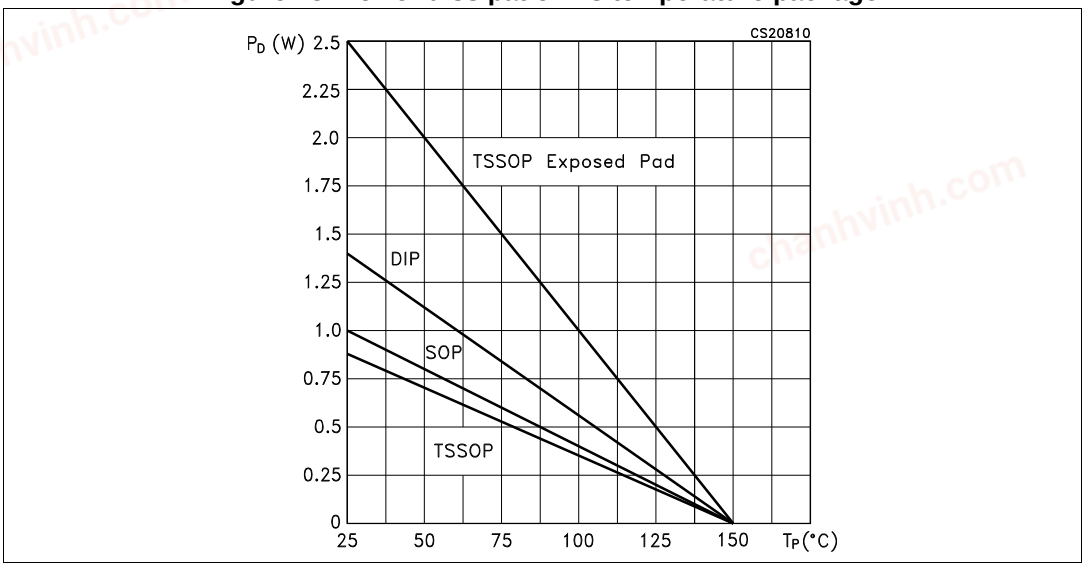

Table 11. $I_{SET}$ vs drop out voltage ($V_{DROP}$)

| Vdd (V) | Iset (mA) | Rext (Ω) | Vdrop min (mV) | Vdrop max (mV) | Vdrop AVG (mV) |
|---|---|---|---|---|---|
| 3 | 3 | 6470 | 30.6 | 31.2 | 30.93 |
| | 5 | 3930 | 46.5 | 52.9 | 48.63 |
| | 10 | 1910 | 80.9 | 100 | 82.26 |
| | 20 | 963 | 150 | 161 | 157 |
| | 50 | 386 | 392 | 396 | 394.3 |
| | 80 | 241 | 636 | 646 | 640.3 |
| | 100 | 192 | 846 | 850 | 848 |
| 5 | 3 | 6470 | 25.6 | 29 | 26.96 |
| | 5 | 3930 | 40.8 | 41.7 | 41.16 |
| | 10 | 1910 | 80.1 | 105 | 89.2 |
| | 20 | 963 | 153 | 154 | 154 |
| | 50 | 386 | 379 | 386 | 382 |
| | 80 | 241 | 618 | 626 | 621 |
| | 100 | 192 | 825 | 830 | 827 |

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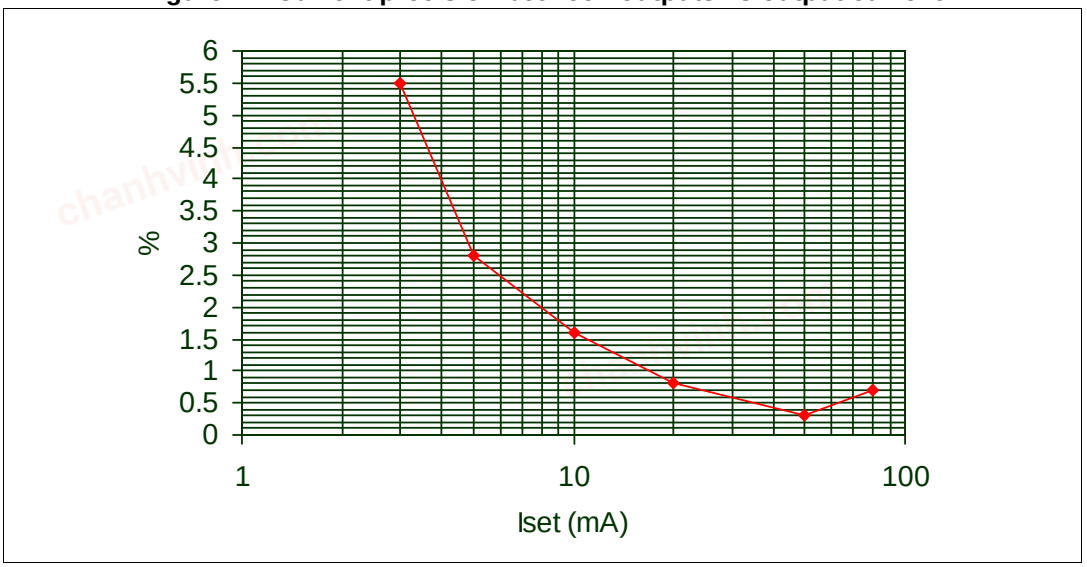


**Figure 13. Power dissipation vs temperature package**




*Note: The exposed-pad should be soldered to the PBC to realize the thermal benefits.*

**Figure 14. Current precision between outputs vs output current**



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# 9 Test circuit

Figure 15. DC characteristics

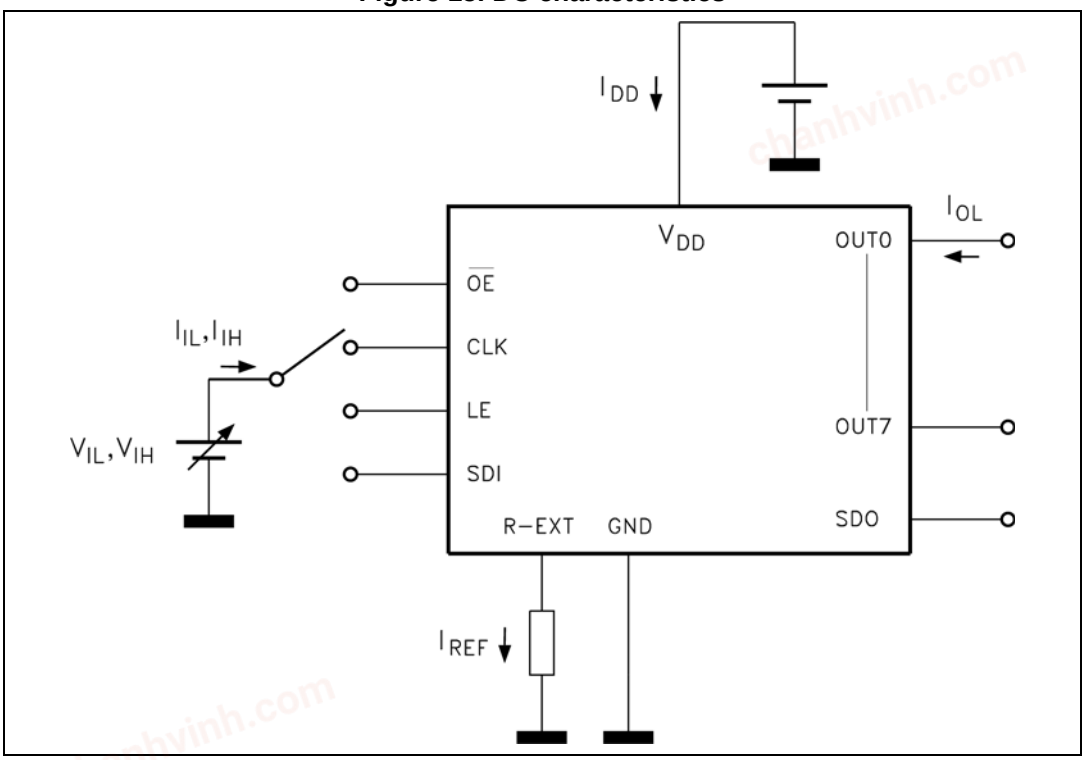
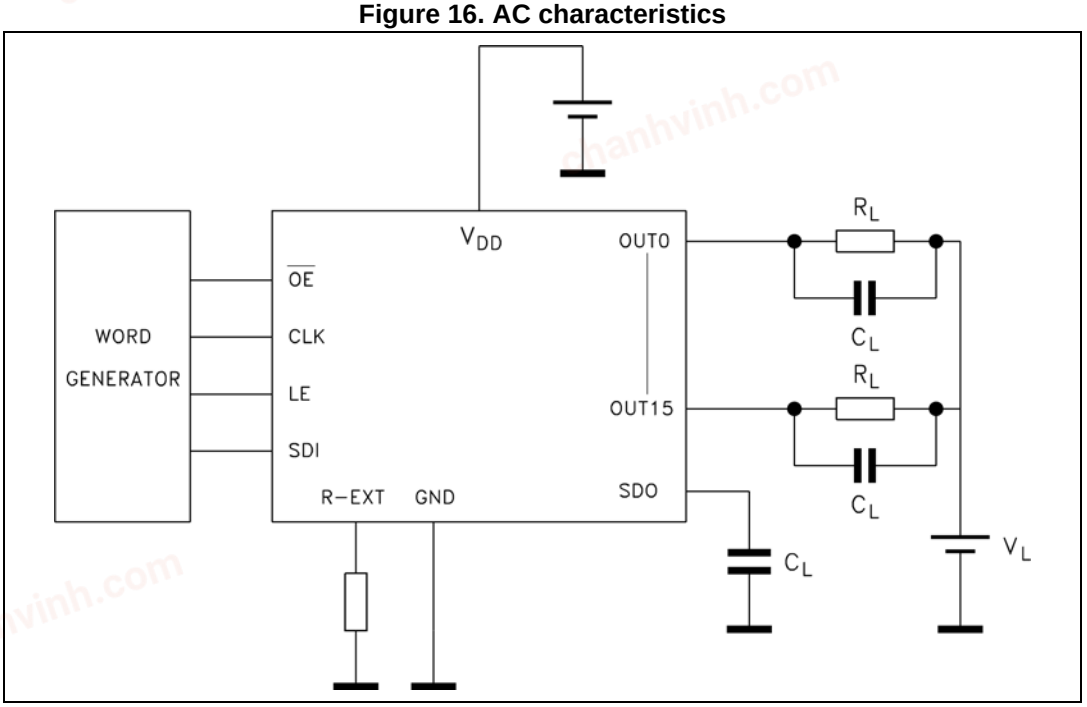



Figure 16. AC characteristics



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# 10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

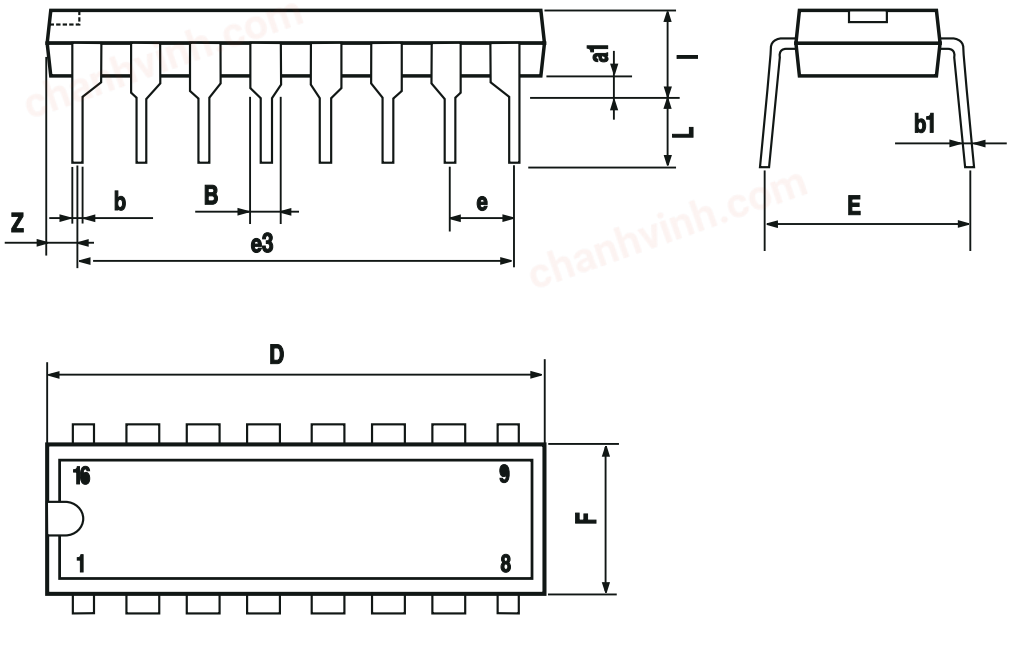
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Table 12. DIP-16 mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| a1 | 0.51 | | |
| B | 0.77 | | 1.65 |
| b | | 0.5 | |
| b1 | | 0.25 | |
| D | | | 20 |
| E | | 8.5 | |
| e | | 2.54 | |
| e3 | | 17.78 | |
| F | | | 7.1 |
| I | | | 5.1 |
| L | | 3.3 | |
| Z | | | 1.27 |

Figure 17. DIP-16 drawing



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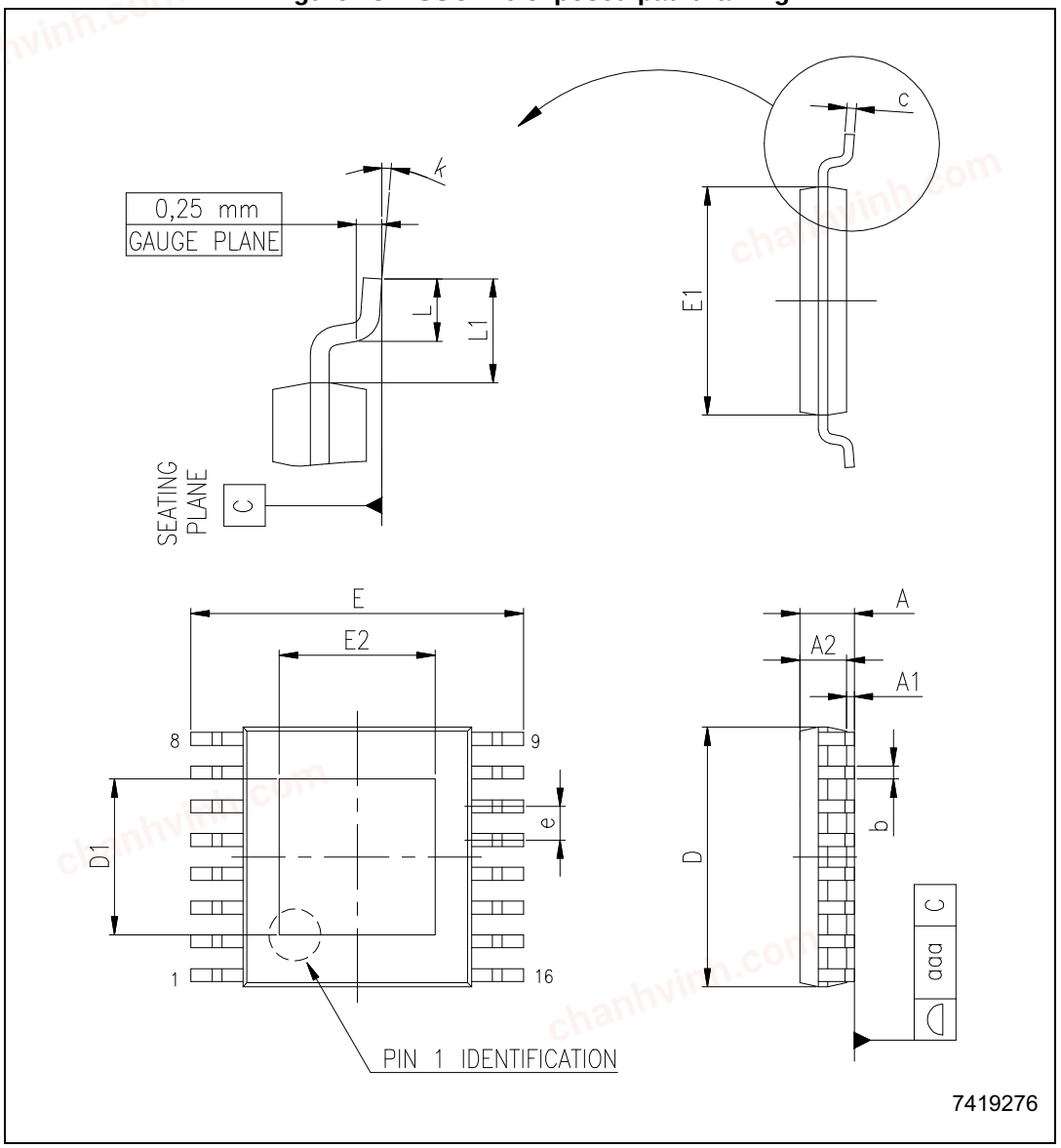
Table 13. TSSOP16 exposed pad mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.20 |
| A1 | | | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| D1 | | 3.00 | |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| E2 | | 3.00 | |
| e | | 0.65 | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 | |
| k | 0.00 | | 8.00 |
| aaa | | | 0.10 |

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**Figure 18. TSSOP16 exposed pad drawing**



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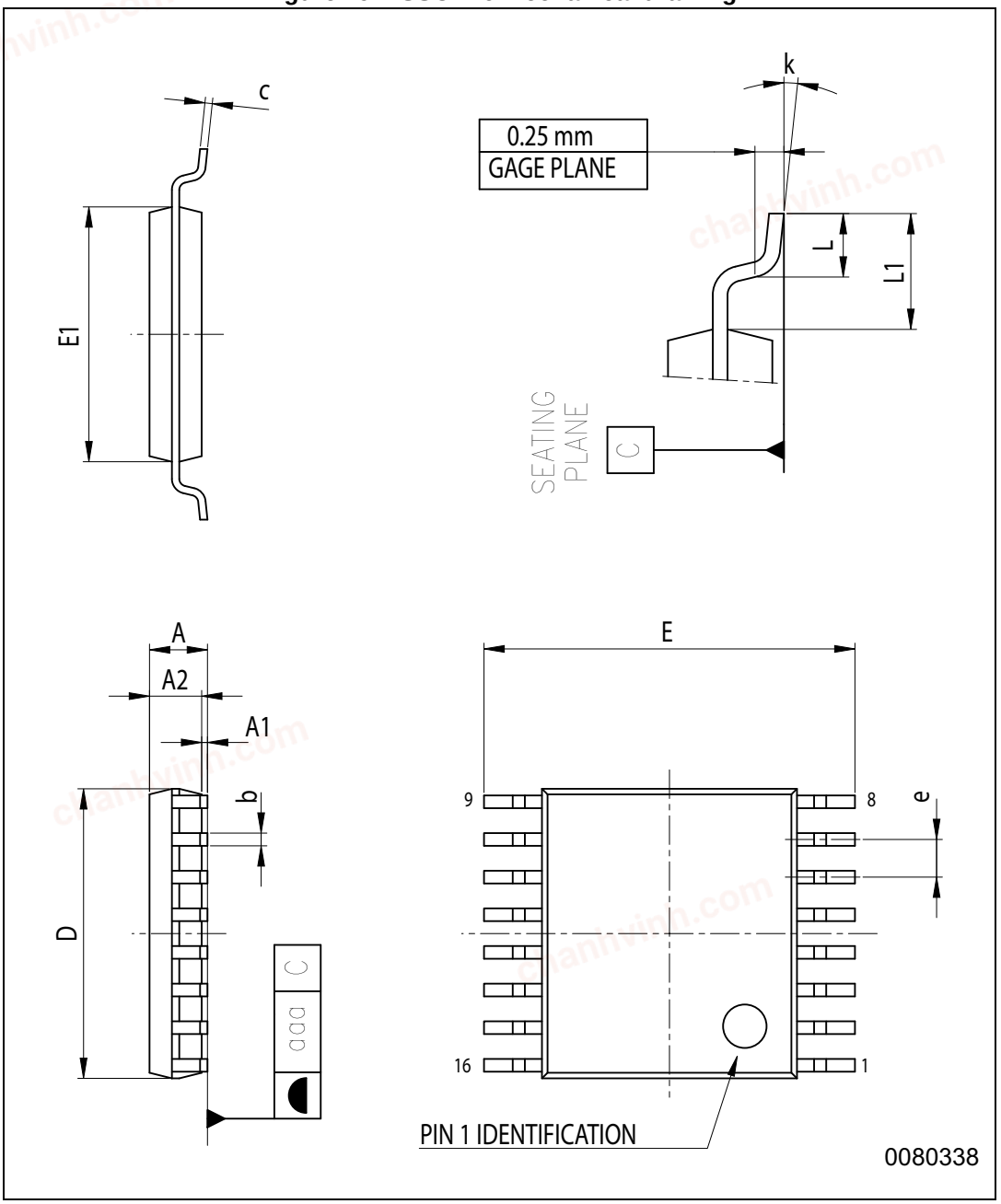
Table 14. TSSOP16 mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | | 0.65 | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 | |
| k | 0 | | 8 |
| aaa | | | 0.10 |

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Figure 19. TSSOP16 mechanical drawing



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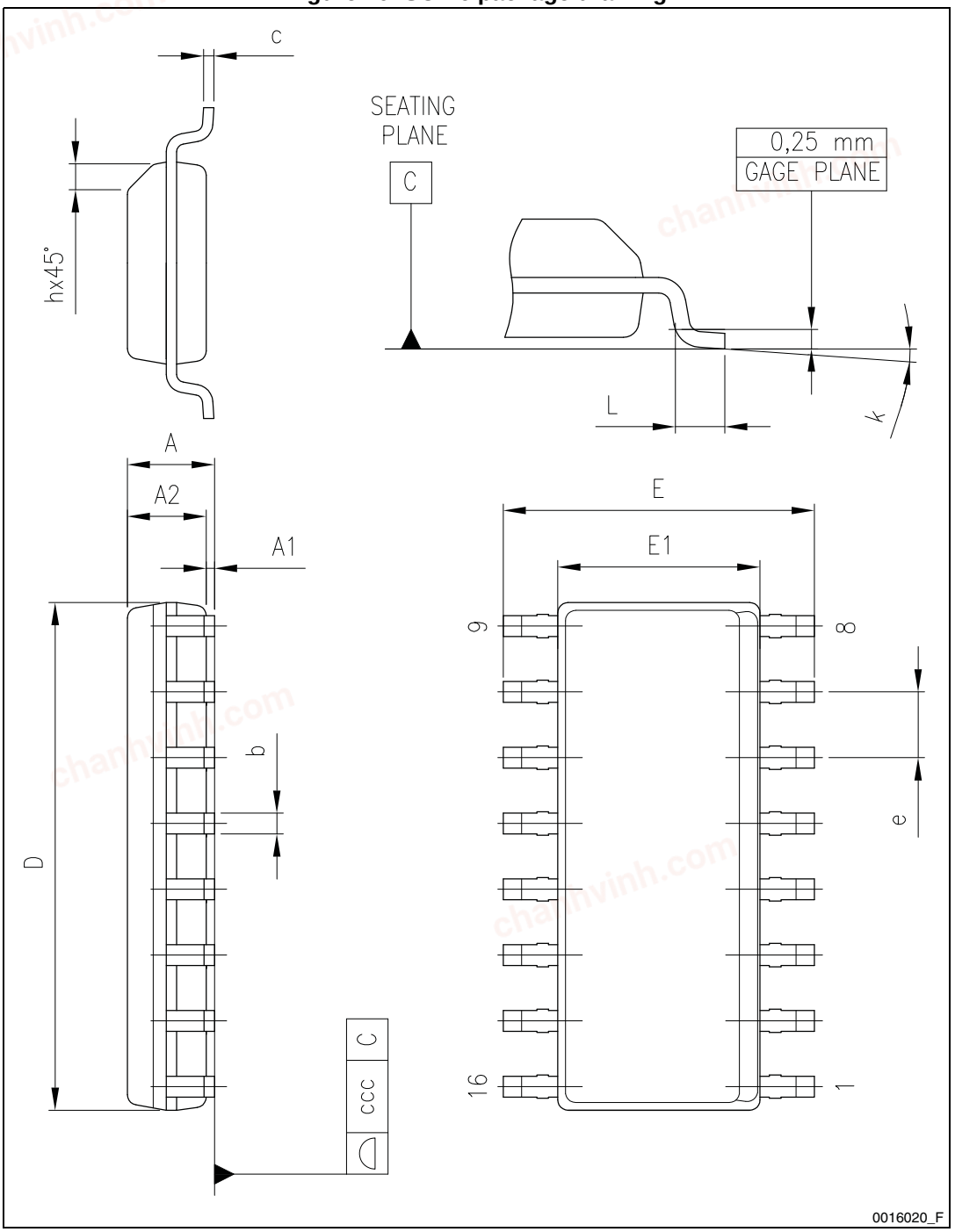
Table 15. SO-16 dimensions

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.31 | | 0.51 |
| c | 0.17 | | 0.25 |
| D | 9.80 | 9.90 | 10.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| k | 0 | | 8° |
| ccc | | | 0.10 |

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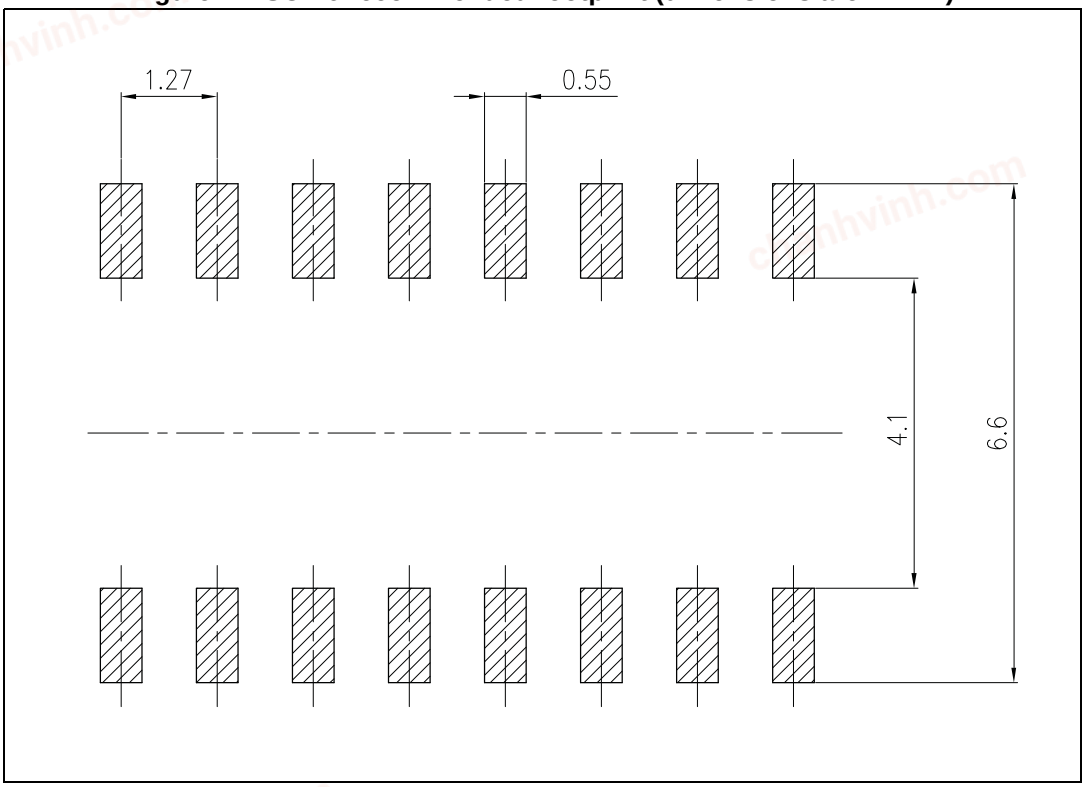
**Figure 20. SO-16 package drawing**



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Figure 21. SO-16 recommended footprint (dimensions are in mm)



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# 11 Packaging mechanical data

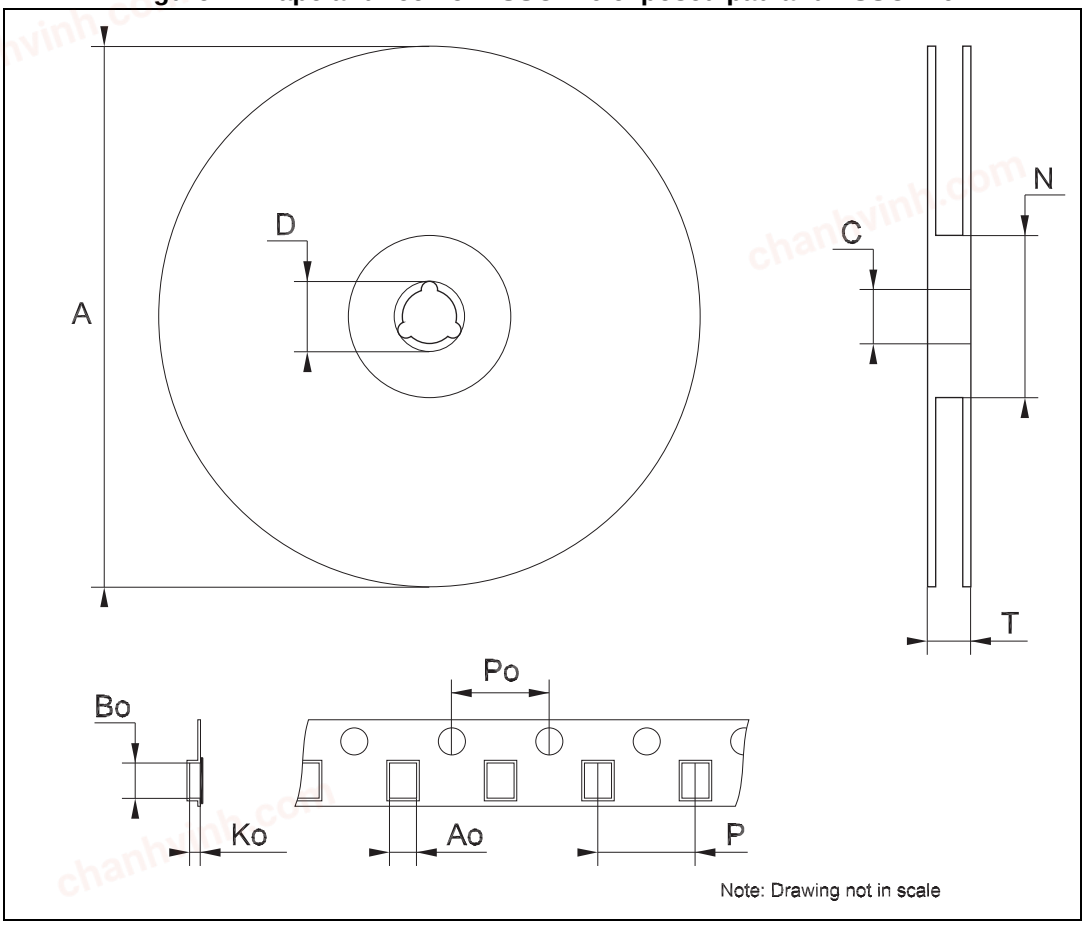
**Table 16. TSSOP16 exposed pad and TSSOP16 tape and reel mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 330 |
| C | 12.8 | | 13.2 |
| D | 20.2 | | |
| N | 60 | | |
| T | | | 22.4 |
| Ao | 6.7 | | 6.9 |
| Bo | 5.3 | | 5.5 |
| Ko | 1.6 | | 1.8 |
| Po | 3.9 | | 4.1 |
| P | 7.9 | | 8.1 |

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**Figure 22. Tape and reel for TSSOP16 exposed pad and TSSOP16**



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# 12 Revision history

**Table 17. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 23-May-2007 | 1 | First release |
| 28-Jun-2007 | 2 | Updated Table 7 on page 7 |
| 12-Mar-2008 | 3 | Updated Table 8 on page 8 and added Figure 11 and Figure 12 on page 15 |
| 07-Aug-2008 | 4 | Updated Section 8: Typical characteristics on page 14 |
| 27-Aug-2010 | 5 | Updated Note: on page 3 |
| 10-Jul-2013 | 6 | Updated Section 10: Package mechanical data, Figure 3: OE terminal and Figure 4: LE terminal<br>Added Section 11: Packaging mechanical data |
| 28-Jun-2018 | 7 | Updated: Table 14: TSSOP16 mechanical data and Figure 20: TSSOP16 mechanical drawing |
| 29-Aug-2018 | 8 | Updated: *Figure 7: Timing diagram*, *Figure 8: Clock, serial-in, serial-out*, *Figure 9: Clock, serial-in, latch, enable, outputs*, *Figure 10: Outputs*, *Figure 15: DC characteristics* and *Figure 16: AC characteristics*.<br>Minor text changes. |

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