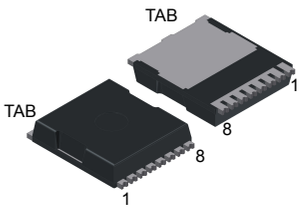
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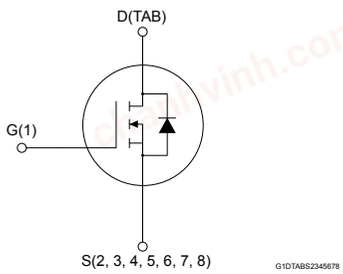
STO450N6F7

Datasheet

N-channel 60 V, 0.85 mΩ max., 545 A STripFET F7 Power MOSFET in a TO-LL package



TO-LL



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STO450N6F7	60 V	0.85 mΩ	545 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Application

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status link
STO450N6F7

Product summary	
Order code	STO450N6F7
Marking	450N6F7
Package	TO-LL
Packing	Tape and reel

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1 Electrical ratings

Table 1. Absolute maximum ratings (at T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D[1]	Drain current (continuous) at T_C = 25 °C[2]	545	A
	Drain current (continuous) at T_C = 100 °C[2]	385	
	Drain current (continuous) at T_C = 25 °C[3]	300	
I_{DM}[1][2][4]	Drain current (pulsed), t_P = 10 µs	2180	A
P_{TOT}	Total power dissipation at T_C = 25 °C	454	W
I_{AS}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	90	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = 90 A, R_{Gmin} = 25 Ω)	1772	mJ
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		°C

1. *Specified by design, not tested in production.*
2. *This is the theoretical current value only related to the silicon.*
3. *This current value is limited by package.*
4. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}[1]	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	11.7	°C/W
R_{thJC}[2]	Thermal resistance, junction-to-case	0.33	°C/W

1. *Measured on 4 layer PCB according to Jedec 51.2 in natural convection (still air).*
2. *Measured according to Jedec 51.14.*

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2 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	60			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 90 A		0.75	0.85	mΩ
R_G(1)	Gate resistance			1.2		Ω

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}(1)	Input capacitance	V_{DS} = 30 V, f = 1 MHz, V_{GS} = 0 V	-	16500	-	pF
C_{oss}(1)	Output capacitance		-	7500	-	pF
C_{rss}(1)	Reverse transfer capacitance		-	400	-	pF
Q_g(1)	Total gate charge	V_{DD} = 30 V, I_D = 90 A, V_{GS} = 0 to 10 V	-	300	-	nC
Q_{gs}(1)	Gate-source charge		-	80	-	nC
Q_{gd}(1)	Gate-drain charge		-	95	-	nC
$Q_{g(sync)}$	Total gate charge, sync. MOSFET	I_D = 90 A, V_{GS} = 0 to 10 V	-	220	-	nC
Q_{oss}	Output charge	V_{DD} = 30 V, V_{GS} = 0 V	-	340	-	nC

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(1)	Turn-on delay time	V_{DD} = 30 V, I_D = 90 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	55	-	ns
t_r(1)	Rise time		-	100	-	ns
$t_{d(off)}$(1)	Turn-off delay time		-	140	-	ns
t_f(1)	Fall time		-	90	-	ns

1. *Specified by design and evaluated by characterization, not tested in production.*

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Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)(2)	Forward on current (continuous)	T_C = 25 °C	-	-	286	A
V_{SD}	Forward on voltage	I_{SD} = 90 A, V_{GS} = 0 V	-	-	1.2	V
t_{rr} (1)	Reverse recovery time	I_D = 90 A, di/dt = 100 A/µs, V_{DD} = 48 V	-	95	-	ns
Q_{rr} (1)	Reverse recovery charge		-	175	-	nC
I_{RRM} (1)	Reverse recovery current		-	3.8	-	A

1. *Specified by design and evaluated by characterization, not tested in production.*
2. *This is the theoretical current value only related to the silicon.*

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2.1 Electrical characteristics (curves)

Figure 1. Total power dissipation

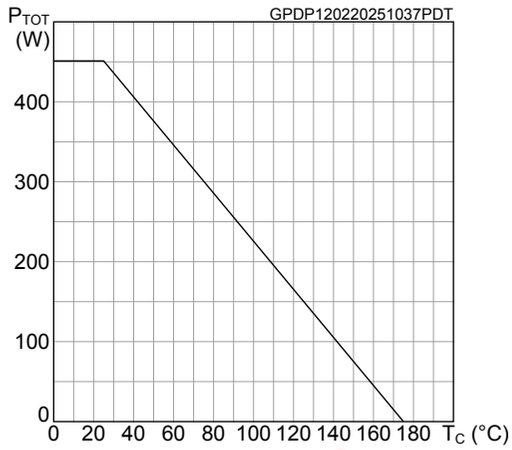


Figure 2. Drain current vs case temperature

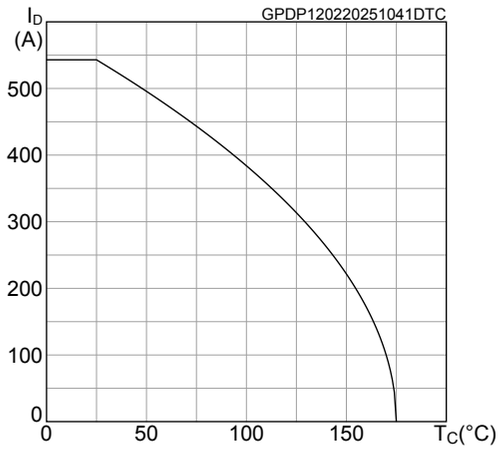


Figure 3. Safe operating area

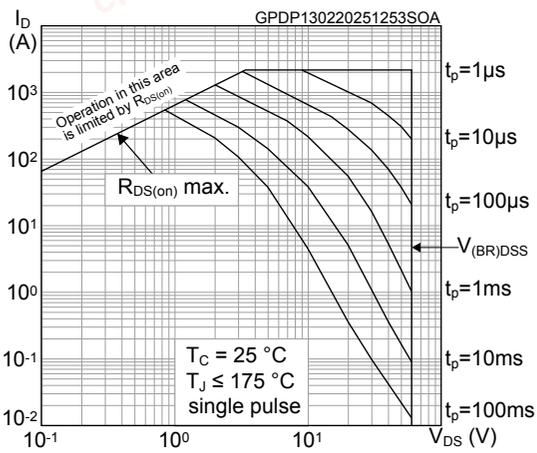


Figure 4. Normalized transient thermal impedance

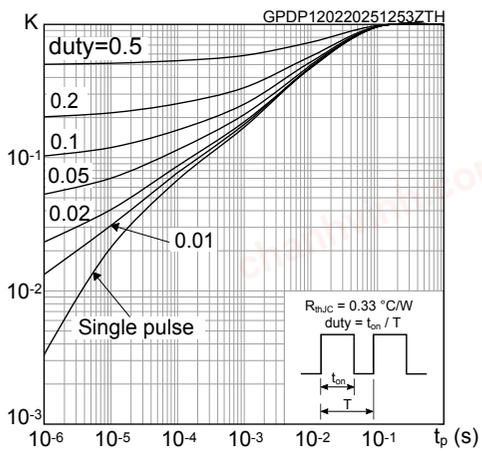


Figure 5. Avalanche characteristics

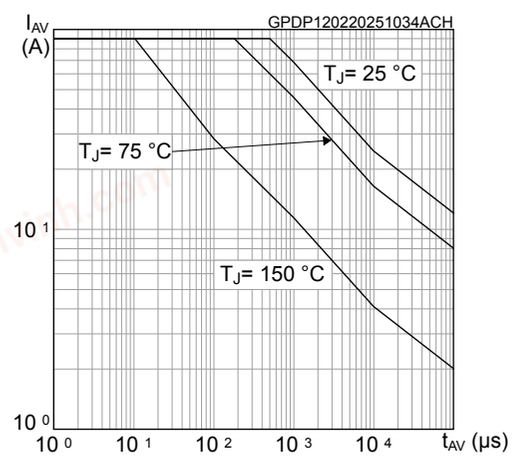
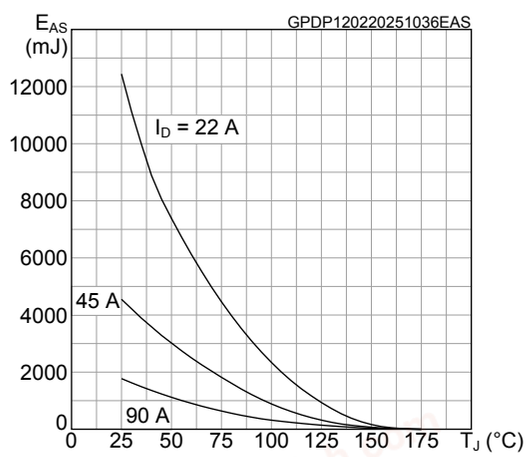


Figure 6. Avalanche energy



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Figure 7. Normalized on-resistance vs temperature

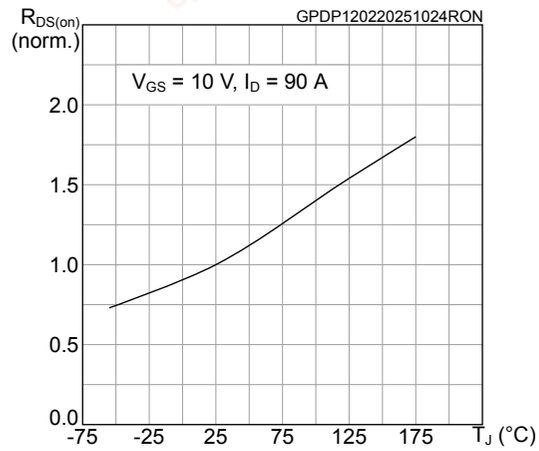


Figure 8. Normalized gate threshold vs temperature

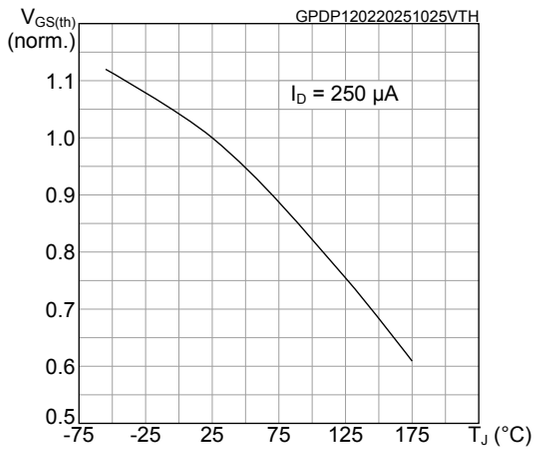


Figure 9. Typical reverse diode forward characteristics

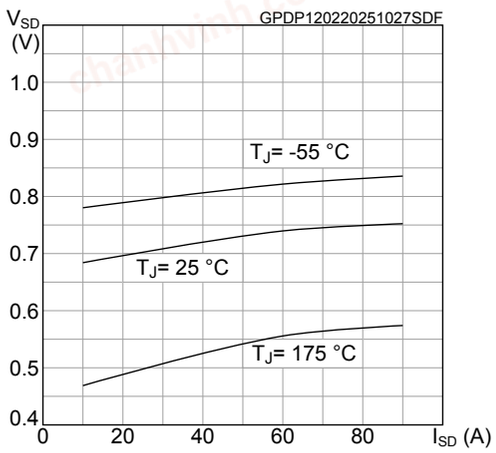


Figure 10. Normalized breakdown voltage vs temperature

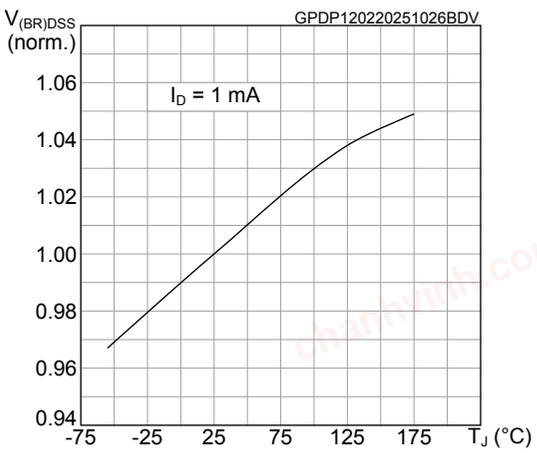


Figure 11. Typical output characteristics

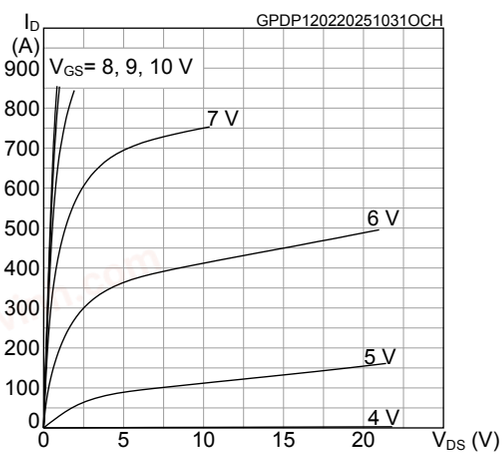
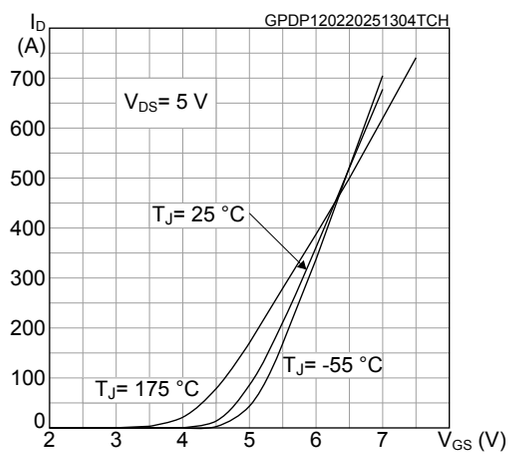


Figure 12. Typical transfer characteristics



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Figure 13. Typical drain-source on-resistance

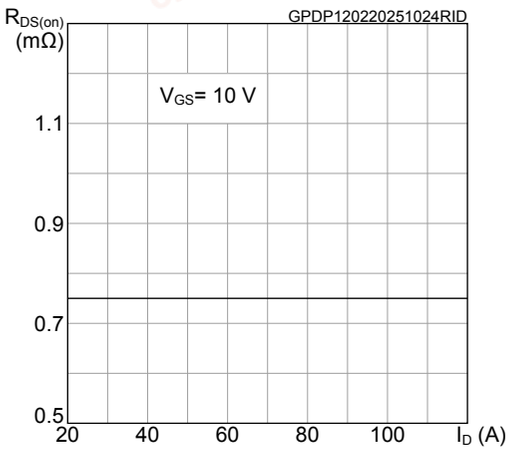


Figure 14. Typical on-resistance vs gate-source voltage

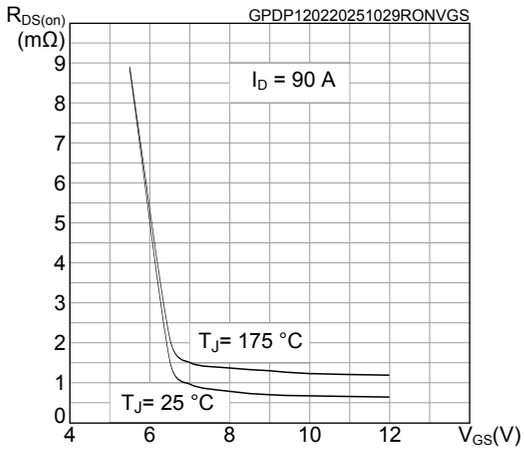


Figure 15. Typical gate charge characteristics

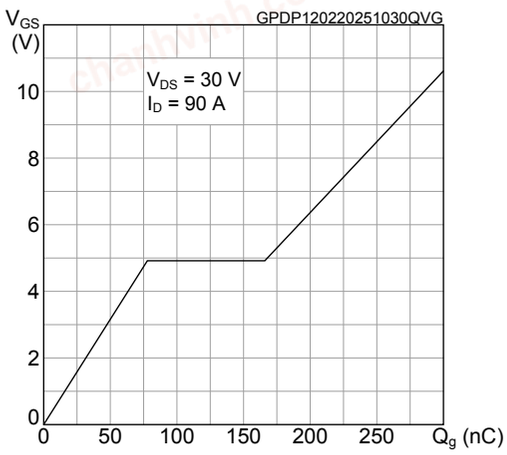
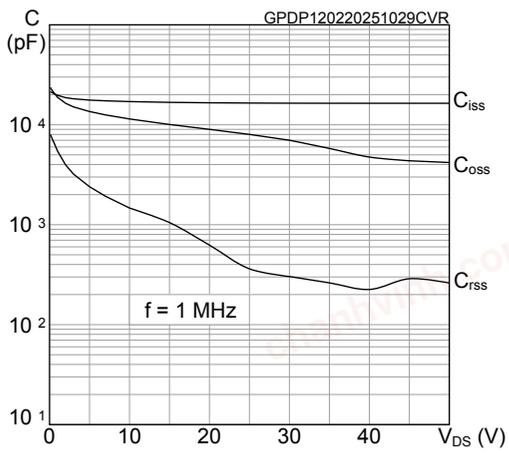


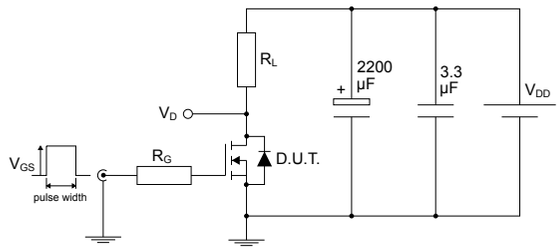
Figure 16. Typical capacitance characteristics



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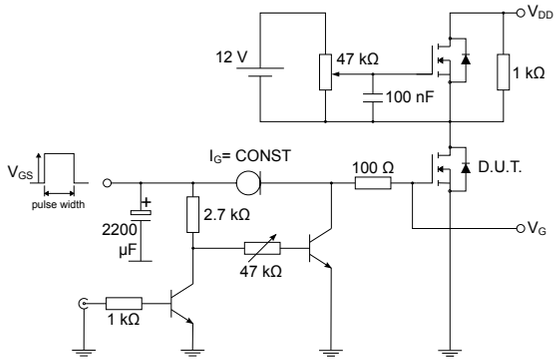
3 Test circuits

Figure 17. Test circuit for resistive load switching times



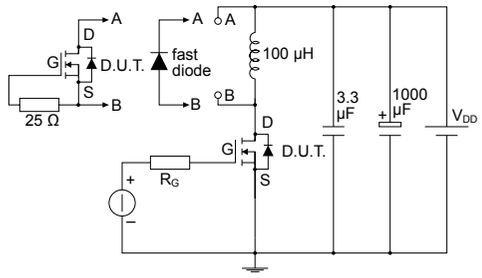
AM01468v1

Figure 18. Test circuit for gate charge behavior



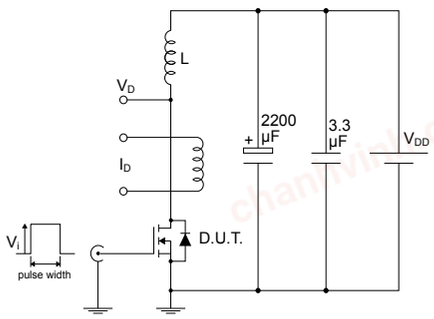
AM01469v1

Figure 19. Test circuit for inductive load switching and diode recovery times



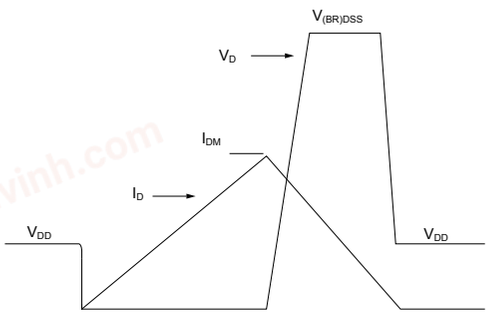
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Figure 20. Unclamped inductive load test circuit



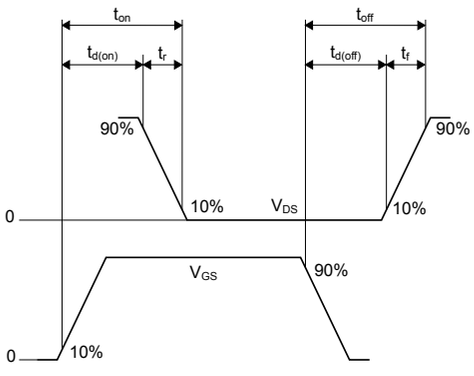
AM01471v1

Figure 21. Unclamped inductive waveform



AM01472v1

Figure 22. Switching time waveform



AM01473v1

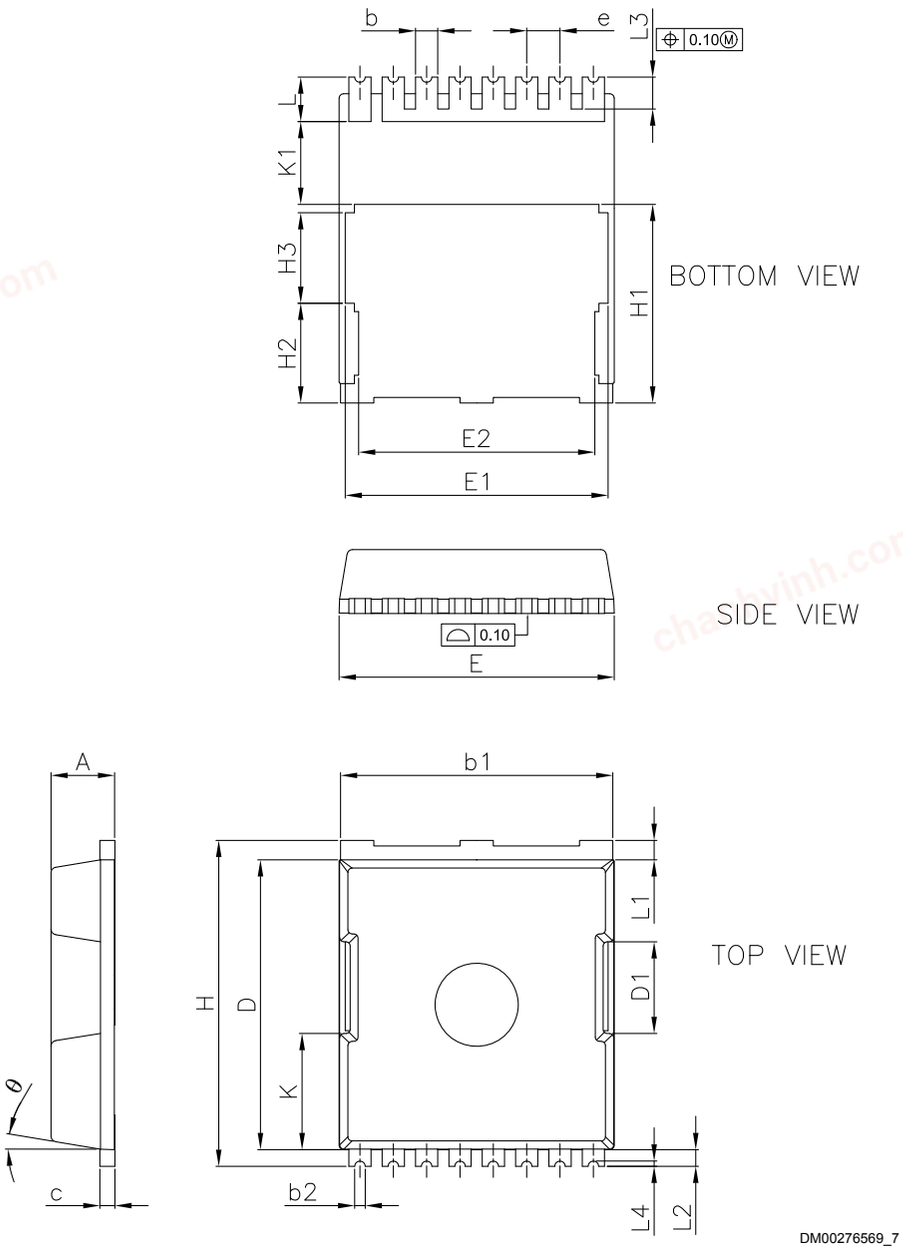
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL package information

Figure 23. TO-LL package outline



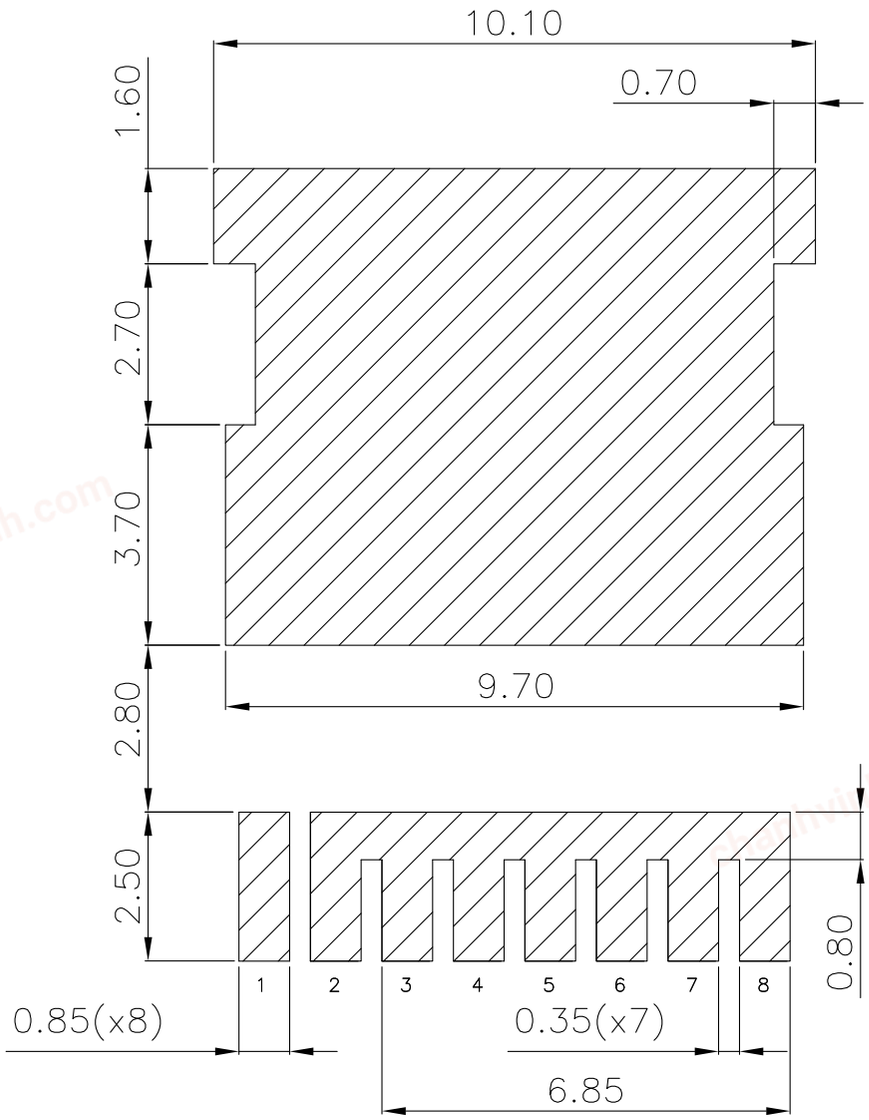
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Table 7. **TO-LL package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
b	0.60	0.80	0.90
b1	9.70	9.80	9.90
b2	0.20		0.50
c	0.40	0.50	0.60
D	10.28	10.43	10.58
D1	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	9.31	9.46	9.61
E2	8.35	8.50	8.65
e	1.10	1.20	1.30
H	11.48	11.73	11.88
H1	7.00	7.15	7.30
H2	3.34	3.59	3.84
H3	3.11	3.26	3.41
K	4.03	4.18	4.33
K1	2.70		
L	1.45	1.60	1.75
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
L4	0.05		0.40

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Figure 24. **TO-LL recommended footprint (dimensions are in mm)**

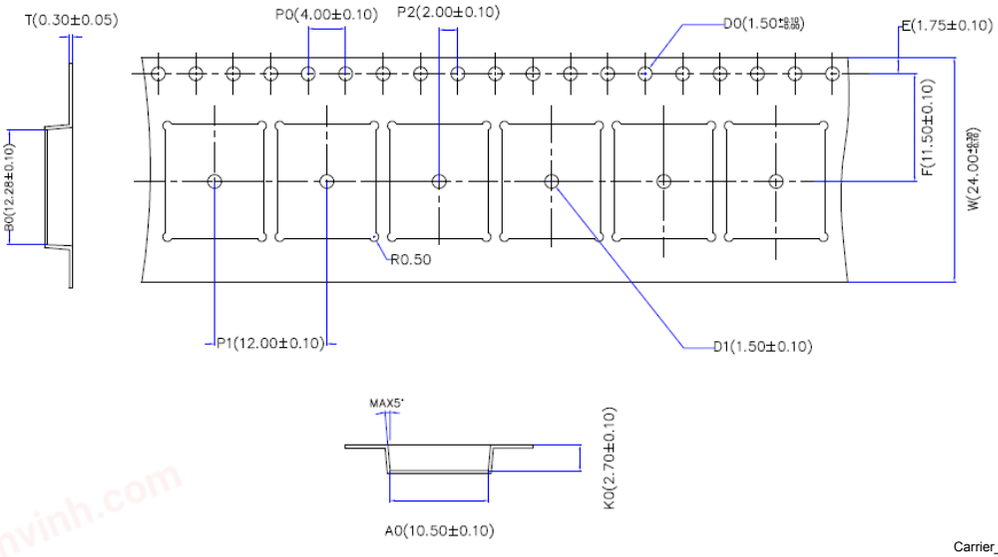


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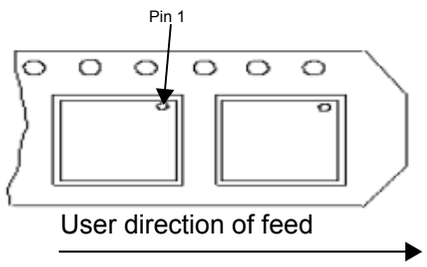
4.2 TO-LL packing information

Figure 25. **Carrier tape outline and dimensions**



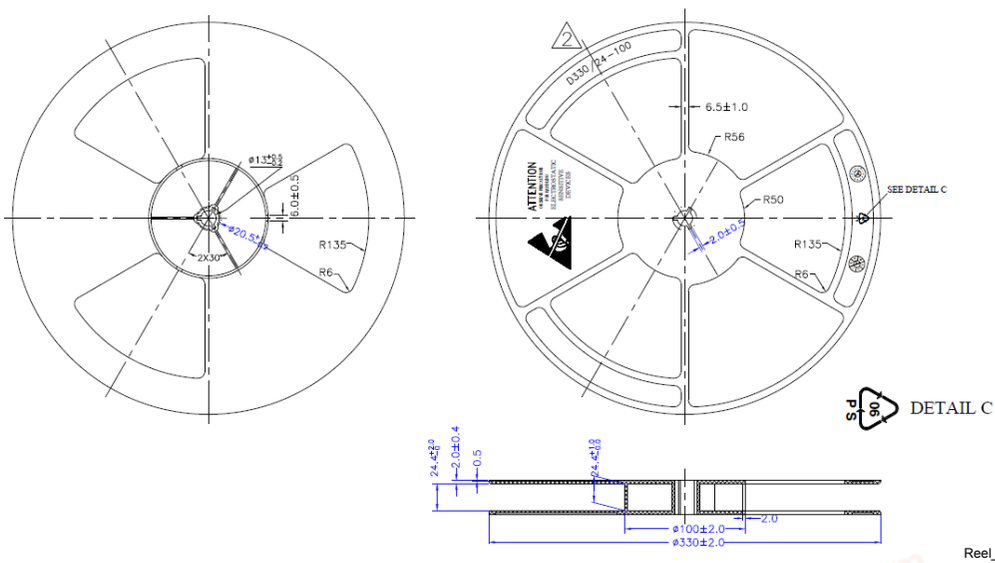
Carrier_DM00282027_5

Figure 26. **TO-LL orientation in carrier tape**



orientation_carrier_tape_0031932_65

Figure 27. **Reel outline and dimensions**

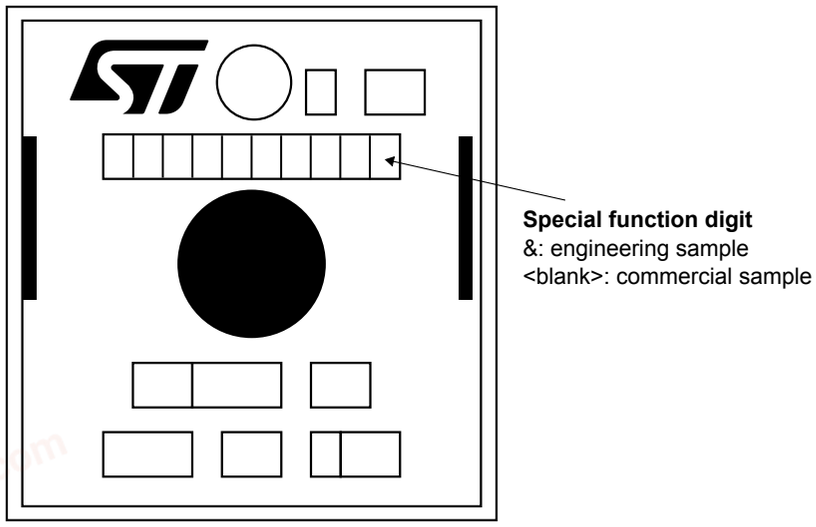


Reel_DM00282027_5

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4.3 TO-LL marking information

Figure 28. **TO-LL marking information**



Note: Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

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Revision history

Table 8. **Document revision history**

Date	Version	Changes
02-Aug-2024	1	Initial release.
17-Mar-2025	2	Updated *Section 1: Electrical ratings* and *Section 2: Electrical characteristics*. Added *Section 2.1: Electrical characteristics (curves)*. Updated *Section 4.2: TO-LL packing information*. Minor text changes.
07-Apr-2025	3	Updated Section 2.1: Electrical characteristics (curves). Minor text changes.

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Contents

1 **Electrical ratings** 2
2 **Electrical characteristics** 3
2.1 Electrical characteristics (curves) 5
3 **Test circuits** 8
4 **Package information** 9
4.1 TO-LL package information 9
4.2 TO-LL packing information 12
4.3 TO-LL marking information 13
Revision history 14

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