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STM32WBA50KG

Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M33 with FPU, Bluetooth® 5.4 radio solution

Datasheet - production data

Features

- Includes ST state-of-the-art patented technology
- Ultra-low power radio
  - 2.4 GHz radio
  - RF transceiver supporting Bluetooth® Low Energy specification 5.4
  - RX sensitivity: -96 dBm (Bluetooth® Low Energy at 1 Mbps)
  - Programmable output power, +4 dBm with 1 dB steps
  - Integrated balun to reduce BOM
  - Single crystal operation
  - Suitable for systems requiring compliance with radio frequency regulations ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T66
- Operating conditions:
  - 1.71 to 3.6 V power supply
  - -40 to 85 °C temperature range
- Ultra-low power platform with FlexPowerControl
  - Autonomous peripherals with DMA, functional down to Stop 1 mode
  - 160 nA Standby mode (8 wake-up pins)
  - 2.25 µA Standby mode with 16-Kbyte SRAM
  - 20.2 µA Stop mode with 16-Kbyte SRAM
  - 41.8 µA/MHz Run mode at 3.3 V
  - Radio: Rx 7.91 mA / Tx at 0 dBm 10.51 mA
  - Embedded regulator LDO
- Core: Arm® 32-bit Cortex®-M33 CPU with MPU, DSP, and FPU
- ART Accelerator: 8-Kbyte instruction cache allowing 0-wait-state execution from flash memory (frequency up to 100 MHz, 150 DMIPS)



UFQFPN32 (5 x 5 mm)

- Benchmarks
  - 1.5 DMIPS/MHz (Drystone 2.1)
  - 410 CoreMark® (4.10 CoreMark/MHz)
- Real time clock (RTC) with hardware calendar, alarms, and calibration
- Clock sources
  - 32 MHz crystal oscillator
  - 32 kHz crystal oscillator (LSE)
  - Internal low-power 32 kHz (±5%) RC
  - Internal 16 MHz factory trimmed RC (±1%)
  - PLL for system clock and ADC
- Memories
  - 1 Mbyte flash memory with ECC, including 256 Kbytes with 100k cycles
  - 64-Kbyte SRAM, including 48 KB with parity check
  - 512-byte (32 rows) OTP
- Rich analog peripherals (independent supply)
  - 12-bit ADC 2.5 Msps, with hardware oversampling
- Communication peripherals
  - Two UARTs (ISO 7816, IrDA, modem)
  - SPI
  - I2C Fm+ (1 Mbit/s), SMBus/PMBus®

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- System peripherals
  - Touch sensing controller, up to 12 sensors, supporting touch key, linear, and rotary touch sensors
  - One 16-bit, advanced motor control timer
  - One 16-bit timer
  - One 32-bit timer
  - One low-power 16-bit timer (available in Stop mode)
  - One Systick timer
  - Two watchdogs
  - 8-channel DMA controller, functional in Stop mode
- Security and cryptography
  - Flexible life cycle scheme with RDP and password protected debug
  - AES co-processor
  - Public key accelerator
  - HASH hardware accelerator
  - True random number generator, NIST SP800-90B compliant
  - 96-bit unique ID
  - Active tampers
  - CRC calculation unit
- General purpose input/output:
  - 20 I/Os (most of them 5 V-tolerant) with interrupt capability
- Development support
  - Serial wire debug (SWD), JTAG
- ECOPACK2 compliant packages

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32WBA50KG microcontrollers, based on Arm® cores[a]. It must be read in conjunction with the reference manual (RM0493).

Throughout the whole document TBD indicates a value to be defined.

For information on the device errata with respect to the datasheet and reference manual refer to the STM32WBA50KG errata sheet (ES0637).

For information on the Arm® Cortex®-M33 core, refer to the Cortex®-M33 Technical Reference Manual, available on the www.arm.com website.

For information on Bluetooth®, refer to www.bluetooth.com.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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2 Description

The STM32WBA50KG multiprotocol wireless and ultra-low power devices embed a powerful and ultra-low power radio compliant with the Bluetooth® SIG Low Energy specification 5.4. They operate at a frequency of up to 100 MHz.

The devices integrate a 2.4 GHz RADIO supporting Bluetooth Low Energy, and make possible to use proprietary protocols.

The STM32WBA50KG are based on a high-performance Arm Cortex-M33 32-bit RISC core, featuring a single-precision floating-point unit (FPU), supporting all the Arm single-precision data-processing instructions and all the data types. This core also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (1 Mbyte of flash memory and 64 Kbytes of SRAM), an extensive range of enhanced I/Os and peripherals connected to AHB and APB buses on the 32-bit multi-AHB bus matrix.

A flexible life cycle is managed thanks to multiple levels readout protection and debug unlock with password.

Several protection mechanisms are available for embedded flash memory and SRAM, namely readout and write protection.

The devices embed several peripherals reinforcing security: a fast AES coprocessor, a PKA (public key accelerator), a HASH hardware accelerator, and a true random number generator.

Active tamper detection and protection against transient perturbation attacks, is achieved thanks to several internal monitoring generating secret data erase in case of attack. This helps to fit the PCI requirements for point of sales applications.

Hardware semaphores enable the synchronization between software processes.

The devices offer one 12-bit ADC (2.5 Msps), a low-power RTC, one 32-bit general-purpose timer, one 16-bit PWM timer for motor control, one 16-bit general-purpose timer, and one 16-bit low-power timer. They also feature standard and advanced communication interfaces, namely one I2C, one SPI, one USART, and one low-power UART.

The STM32WBA50KG operate in the -40 to 85 °C (105 °C junction) temperature range from a 1.71 to 3.6 V power supply.

The design of low-power applications is enabled by a comprehensive set of power-saving modes.

Many peripherals (including radio, communication, analog, and timer peripherals) can be functional and autonomous in Stop mode with direct memory access thanks to BAM (background autonomous mode) support.

Some independent power supplies are supported, like an analog independent supply input for ADC, and radio dedicated supply inputs for the 2.4 GHz RADIO.

The STM32WBA50KG devices are available in an UFQFPN32 package.

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Table 2. Device features and peripheral counts

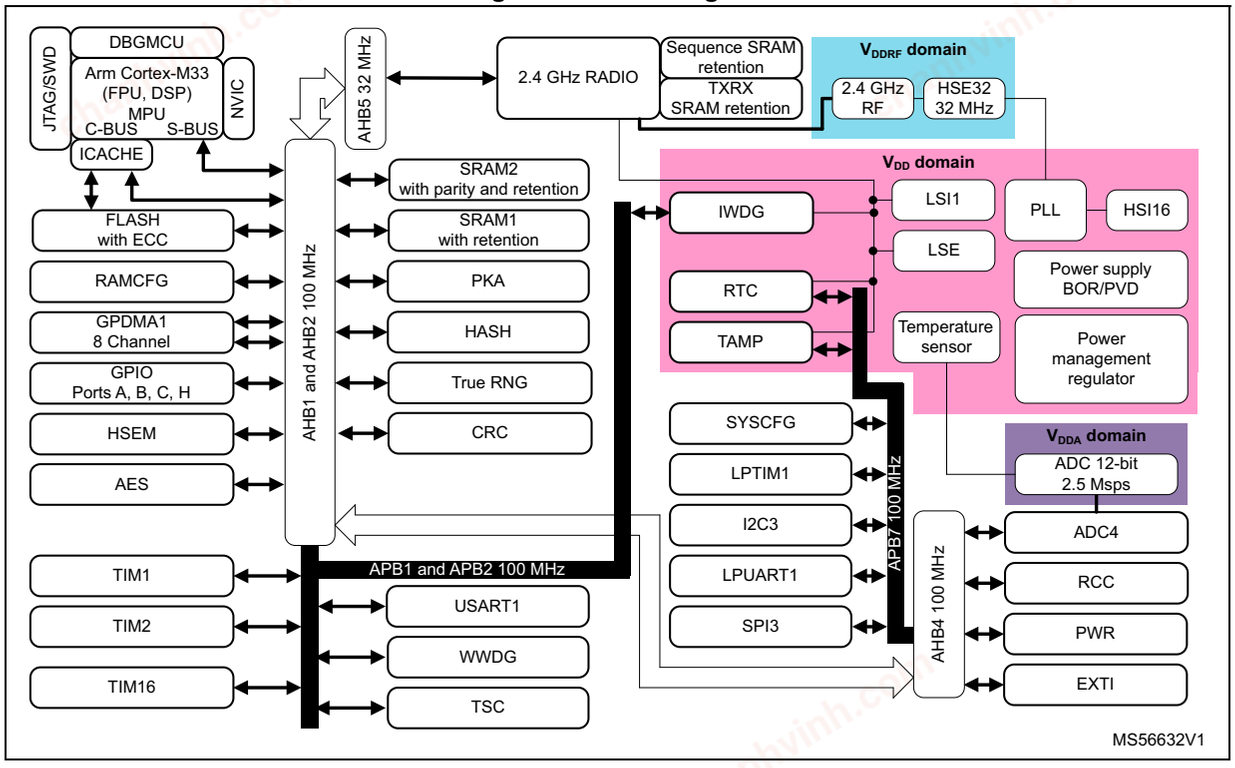
Feature		STM32WBA50KG
Flash memory density		1024 Kbytes
SRAM density	SRAM1	16 Kbytes
	SRAM2	48 Kbytes
Backup registers		32 x 32 bits
Bluetooth Low Energy		Yes
Real time clock (RTC)		Yes
Timers	Advanced control	1 (16-bit)
	General purpose	1 (32-bit) + 1 (16-bit)
	Low power	1 (16-bit)
	SysTick	1
	Watchdog (independent, window)	2
Communication interfaces	SPI	1
	I2C	1
	USART	1
	LPUART	1
Tamper pins (active tampers)(1)		3 (2)
Wake-up pins		8
GPIOs		20
Capacitive sensing (channels)		12
12-bit ADC		1 (8 channels)
True random number generator		Yes
Analog comparators		No
AES		Yes
Public key accelerator (PKA)		Yes
HASH		Yes
Maximum CPU frequency		100 MHz
Operating temperature		Ambient: -40 to 85 °C Junction: -40 to 105 °C
Operating voltage		1.71 to 3.6 V
Package		UFQFPN32

1. Active tampers in output sharing mode (one output shared by all inputs).

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Figure 1 shows the general block diagram of the devices.

Figure 1. Block diagram



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3 Functional overview

3.1 Arm Cortex-M33 core with MPU, DSP, and FPU

The Cortex-M33 with MPU, DSP and FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications.

The Cortex-M33 processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. It features:

- MPUs (memory protection units), supporting up to 8 regions for applications
- Floating-point arithmetic functionality, with support for single precision arithmetic

The processor supports a set of DSP instructions for efficient signal processing and complex algorithm execution.

The Cortex-M33 processor supports the following bus interfaces:

- System AHB (S-AHB) bus: used for instruction fetch and data access to the memory-mapped SRAM, peripheral, and Vendor_SYS regions of the Armv8-M memory map.
- Code AHB (C-AHB) bus: used for instruction fetch and data access to the code region of the Armv8-M memory map.

3.2 ART Accelerator (ICACHE)

The ICACHE (instruction cache) is introduced on C-AHB code bus of Cortex-M33 processor to improve performance when fetching instruction (or data) from internal memories.

ICACHE offers the following features:

- Multi-bus interface:
  - Slave port receiving the memory requests from the Cortex-M33 C-AHB code execution port
  - Master1 port performing refill requests to internal flash memory
  - Master2 port performing refill requests to internal SRAMs
  - Second slave port dedicated to ICACHE registers access
- Close to 0 wait-states instructions/data access performance:
  - 0 wait-state on cache hit
  - Hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - Critical-word-first refill policy, minimizing processor stalls on cache miss
  - Hit ratio improved by two-ways set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - Dual master ports to decouple internal flash memory and SRAM traffic, on fast and slow buses, respectively; also minimizing impact on interrupt latency
  - Optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - Performance monitoring by means of a hit counter and a miss counter
- Extension of cacheable region beyond the code memory space, by means of address remapping logic enabling the definition of four regions

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- Power consumption intrinsically reduced (more accesses to cache memory rather than to bigger main memories), even improved by configuring ICACHE as direct mapped (rather than the default two-ways set-associative mode)
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

3.3 Memory protection unit

The MPU is used to manage the CPU accesses to the memory and to prevent tasks to accidentally corrupt the memory or the resources used by other active tasks. This memory area is organized into up to 8 protected areas.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to execute.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all the masters (CPU, GPDMA1) and the slaves (flash memory, SRAMs, AHB, and APB) peripherals. It also ensures a seamless and efficient operation even when several peripherals work simultaneously.

3.5 Embedded flash memory

The devices feature 1 Mbyte of embedded flash memory, available to store programs and data. This memory supports 10000 cycles, and up to 100000 cycles on 32 pages (256 Kbytes).

A 128-bit instruction prefetch is implemented and can optionally be enabled.

The flash memory contains 128 pages of 8 Kbytes, and embeds a 512-byte OTP (one time programmable) for user data.

The configuration of flexible protections is possible thanks to the option bytes:

- RDP (readout protection) to protect the whole memory, has four levels of protection available (see *Table 3*):
  - Level 0: no readout protection
  - Level 1: memory readout protection

    The flash memory cannot be read from or written to if either the debug features are connected or the boot in SRAM or bootloader are selected. Regressions from Level 1 to lower levels can be protected by password authentication.
  - Level 2: chip readout protection

    The debug features, the boot in RAM and the bootloader selection are disabled. A secret key can be configured to allow the regression capability from Level 2 to Level 1. By default (key not configured), this Level 2 selection is irreversible and

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JTAG/SWD interfaces are disabled. If the secret key was previously configured in lower RDP levels, the device enables the RDP regression from Level 2 to Level 1 after password authentication through JTAG/SWD interface.

- Write protection (WRP) to protect areas against erasing and programming. Two areas can be selected with 8-Kbyte granularity.

Table 3. Access status versus protection level and execution modes

Area	RDP level	User execution (boot from flash memory)			Debug/boot from RAM/bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Flash main memory	1	Yes	Yes	Yes	No	No	No(4)
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory (2)	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes(3)	1	Yes	Yes(4)	N/A	Yes	Yes(4)	N/A
	2	Yes	No	N/A	N/A	N/A	N/A
OTP	1	Yes	Yes(5)	N/A	Yes	Yes(5)	N/A
	2	Yes	Yes(5)	N/A	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A	No	No	N/A(6)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	N/A	No	No	N/A(7)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. When the protection level 2 is active, the debug port, the boot from RAM, and the boot from system memory are disabled.
2. The system memory is only read-accessible, whatever the protection level (0, 1 or 2) and execution mode.
3. Option bytes are accessible only through the flash memory interface registers and OPSTRT bit.
4. The flash main memory is erased when the RDP option byte changes from level 1 to level 0.
5. OTP can be written only once.
6. The backup registers are erased when RDP changes from level 1 to level 0.
7. All SRAMs are erased when RDP changes from level 1 to level 0.

The whole nonvolatile memory embeds the ECC (error correction code) feature supporting:

- single-error detection and correction
- double-error detection
- ECC fail address report

3.6 Embedded SRAMs

SRAM1 and SRAM2 are the main SRAMs embedded in the devices, each with specific features. Both can be used for peripherals background autonomous mode (BAM).

These SRAMs can be powered down in Stop mode to reduce consumption:

- SRAM1: one 16-Kbyte block, can be retained in Standby mode
- SRAM2: one 48-Kbyte block with parity, can be retained in Standby mode.

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3.7 Boot modes

At startup, a BOOT0 pin, nBOOT0 and NSBOOTADDx[24:0] (x = 0, 1) option bytes are used to select the boot memory address. This includes:

- Boot from any address in user flash memory
- Boot from system memory bootloader
- Boot from any address in embedded SRAM

The BOOT0 value comes from the PH3-BOOT0 pin or from an option bit, depending upon the value of a user option bit to free the GPIO pad if needed.

The bootloader is located in the system memory, programmed by ST during production. It is used to program the flash memory by using USART, I^2C or SPI in device mode.

The bootloader is available on all devices. Refer to AN2606 *STM32 microcontroller system memory boot mode*, available on *www.st.com*, for more details.

Refer to *Table 4* for boot modes.

Table 4. Boot modes

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option-bytes selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x08000 000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF8 8000
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF8 8000

The boot address option bytes allow any boot memory address to be programmed. The allowed address space depends on the flash memory RDP level.

If the programmed boot memory address is out of the allowed memory mapped area when RDP level is 1 or higher, the default boot address is forced in flash memory, as detailed in *Table 5*.

Table 5. Boot space versus RDP protection

RDP	Description
0	Any boot address
1	Any boot address
2	Boot address only in flash memory: 0x0800 0000 - 0x080F FFFF. Otherwise, forced boot address is 0x0800 0000

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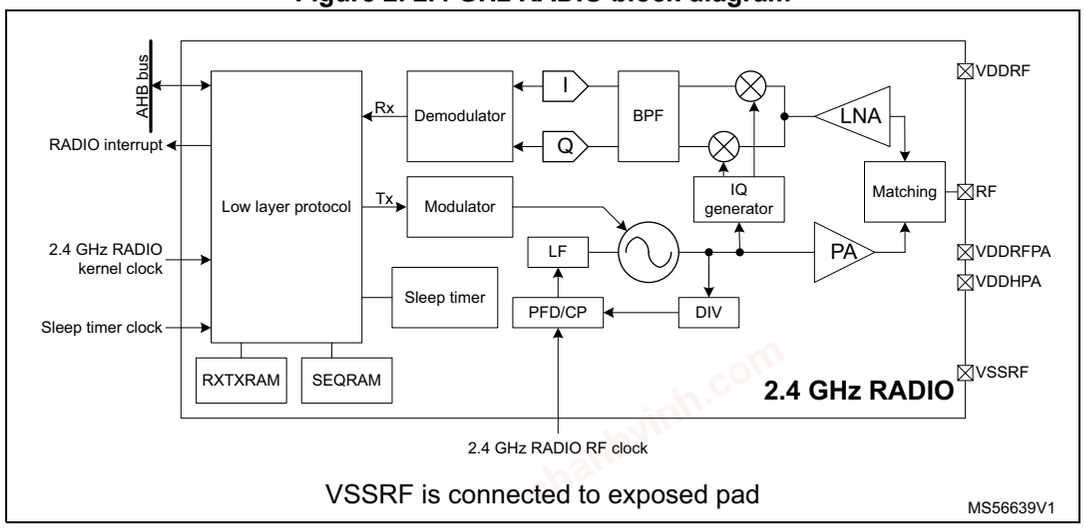
3.8 2.4 GHz RADIO

The 2.4 GHz RADIO is ultra-low power, operating in the 2.4 GHz ISM band. It provides Bluetooth LE 1 Mbps coded, 1 Mbps and 2 Mbps non-coded GFSK. It is compliant with the Bluetooth 5.4 specification and radio regulations including ETSI EN 300 328, EN 300 440, EN 301 489-17, ARIB STD-T66, FCC CFR47 part 15 section 15.205, 15.209, 15.247 and 15.249, IC RSS-139 and RSS-210.

The 2.4 GHz RADIO supports the following features:

- Radio protocol:
  - Bluetooth Low Energy

Figure 2. 2.4 GHz RADIO block diagram



3.9 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domain (V_{CORE})
  - V_{DD} and backup domain
  - Analog domain (V_{DDA})
  - V_{DDRF} for 2.4 GHz RADIO
- System supply voltage regulation
  - Voltage regulator (LDO)
- Power supply supervision
  - BOR monitor
  - PVD monitor
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes

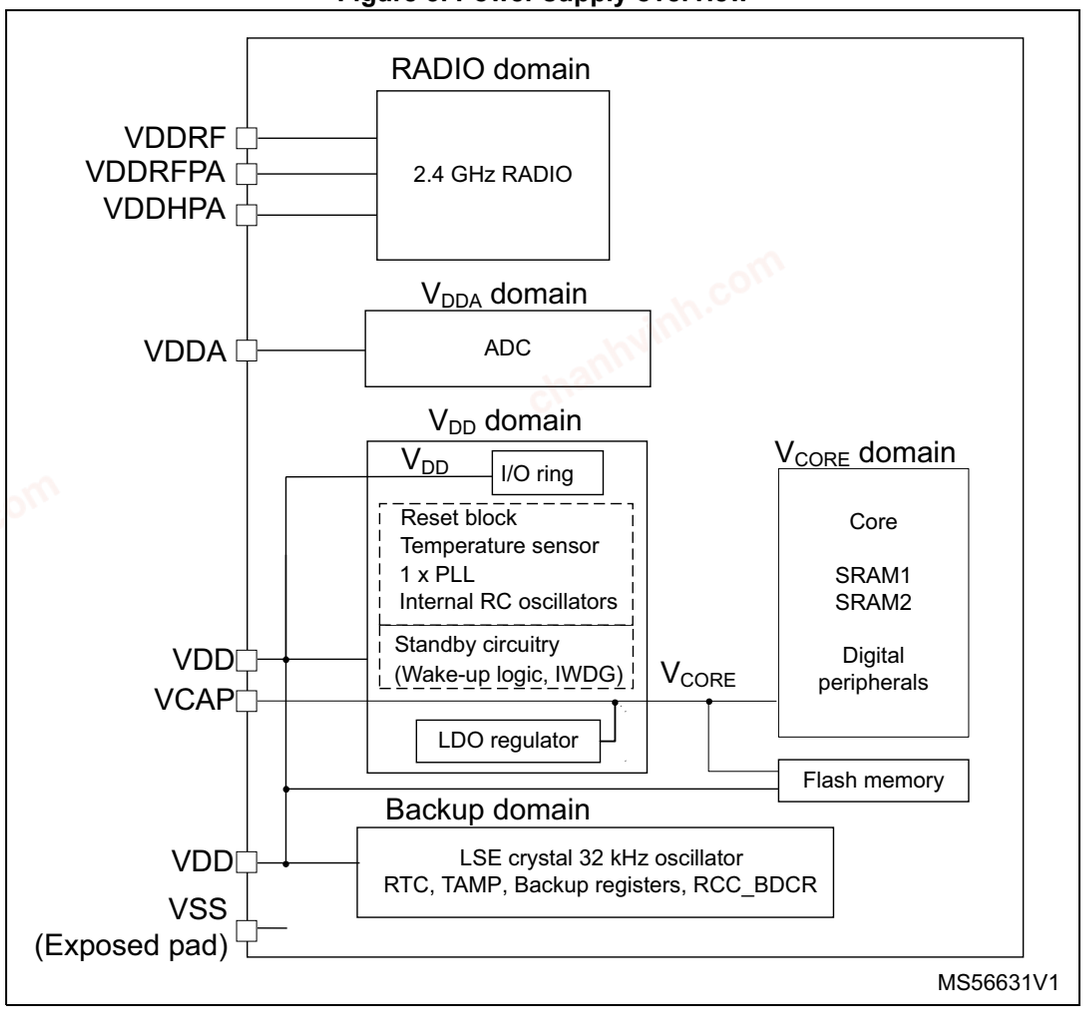
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3.9.1 Power supply schemes

The devices require a 1.71 to 3.6 V V_{DD} operating voltage supply. Independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 to 3.6 V (functionality guaranteed down to V_{BORx} minimum value)
  External power supply for the I/Os, the internal regulator, the system analog such as reset, power management, and internal clocks and the backup domain. It is provided externally through the VDD pins. VDDRF must be connected to the same supply used for VDD.
- V_{DDA} = 1.62 to 3.6 V
  External analog power supply for ADC. The voltage level is independent from the V_{DD} voltage and must be connected to VDD (preferably) or to VSS pin when this peripheral is not used.

Figure 3. Power supply overview

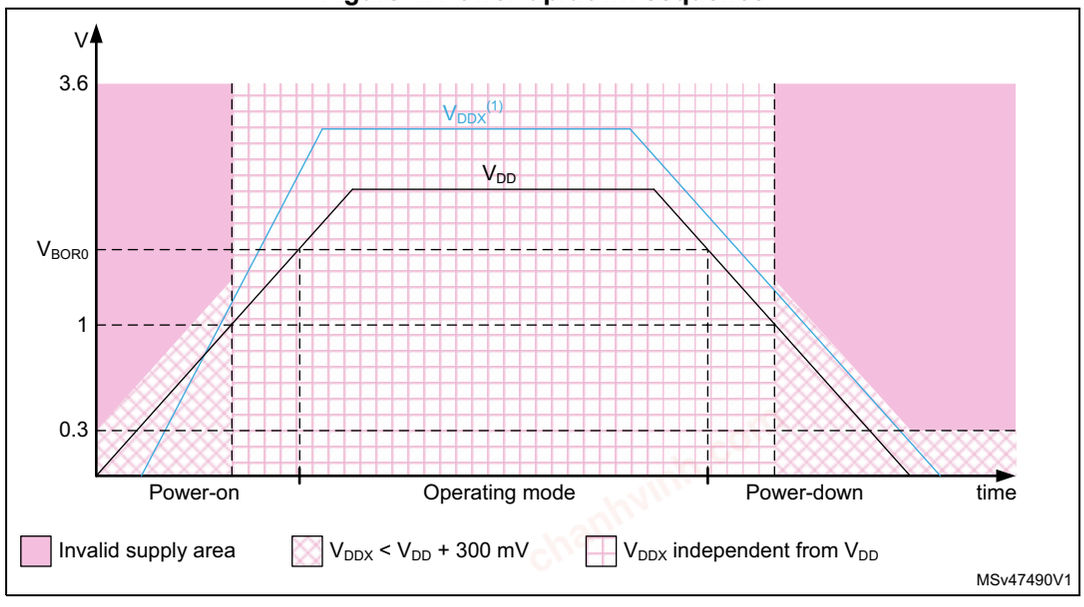


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During power-up and power-down phases, respect the following requirements:

- When V_{DD} is below 1 V, other power supplies (namely V_{DDA}) must remain below V_{DD} + 300 mV.
- When V_{DD} is equal to or above 1 V, other power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 4. Power-up/down sequence



1. V_{DDX} refers to power supply V_{DDA}.

3.9.2 Power supply supervisor

The devices have an integrated ultra-low power BOR (brownout reset) active in all modes. The BOR ensures proper operation after power-on and during power-down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded PVD (programmable voltage detector) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold.

An interrupt can be generated when V_{DD} drops below and/or rises above the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

The devices support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the main regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating frequency.

The main regulator operates in the following ranges:

- Range 1 (V_{CORE} = 1.2 V) with CPU and peripherals running at up to 100 MHz
- Range 2 (V_{CORE} = 0.9 V) with CPU and peripherals running at up to 16 MHz

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Low-power modes

The devices support different low-power modes to achieve the best compromise between low-power consumption, startup time, available peripherals, and available wake-up sources.

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Table 6. Operating modes overview

Mode	Regulator[1]	CPU	Flash memory	SRAM	Clocks	DMA and peripherals[2]	Wake-up source
Run	Range 1	Yes	ON[3]	ON	Any	All	N/A
	Range 2					All except 2.4 GHz RADIO	
Sleep	Range 1	No	ON	ON[4]	Any	All	Any interrupt or event
	Range 2					All except 2.4 GHz RADIO	
Stop 0	Range 1	No	OFF	ON[5]	LSE LSI (6)	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4[7] (temperature sensor), USART1[8], LPUART1, SPI3[9], I2C3[10], LPTIM1[11], GPIO, GPDMA1[12], 2.4 GHz RADIO All other peripherals are frozen.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 (temperature sensor), USART1, LPUART1, SPI3, I2C3, LPTIM1, GPDMA1, 2.4 GHz RADIO
	Range 2					All from Stop 0 Range 1 except 2.4 GHz RADIO	
Stop 1[13]	LPR	No	OFF	ON[5]	LSE LSI	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 and temperature sensor), USART1, LPUART1, SPI3, I2C3, LPTIM1, GPIO All other peripherals are frozen.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 and temperature sensor, USART1, LPUART1, SPI3, I2C3, LPTIM1

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Table 6. Operating modes overview (continued)

Mode	Regulator[1]	CPU	Flash memory	SRAM	Clocks	DMA and peripherals[2]	Wake-up source
Standby retention	LPR	Powered off	OFF	ON[5]	LSE LSI	BOR, RTC, TAMP, IWDG, SLEEP_TIMER All other peripherals are powered off. I/O configuration can be retained, floating, pull-up or pull-down.	Reset pin, WKUPx (x = 1, 3, 4, 6, 7, 8), BOR, RTC, TAMP, IWDG, SLEEP_TIMER
Standby	OFF			Powered off		All from mode Standby retention, except SLEEP_TIMER	

1. LPR means that the main regulator is OFF and the low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. The flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
4. The SRAM1 and SRAM2 clocks can be gated on or off independently.
5. The SRAM can be individually powered off to save power consumption.
6. HSI16 can be temporary enabled upon peripheral request, for autonomous functions with DMA or wake-up from Stop event detections.
7. The ADC conversion is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on conversion events.
8. U(S)ART and LPUART transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
9. SPI transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
10. I2C transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
11. LPTIM is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on all events.
12. GPDMA is functional and autonomous in Stop 0 mode, and can generate a wake-up interrupt on events.
13. Active peripherals ADC, U(S)ART, LPUART, SPI, I2C and LPTIM, can generate bus clock request and/or a wake-up interrupt on event.

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By default, the microcontroller is in Run mode after a system or a power on reset. It is up to the user to select one of the low-power modes described below:

- **Sleep**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt or event occurs.

- **Stop 0 and Stop 1**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the V_{CORE} domain are stopped, the PLL, the HSI16, and the HSE32 crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC, TAMP, IWDG and SLEEP_TIMER can remain active.

  Some peripherals are autonomous and can operate in Stop mode by requesting their kernel clock and their bus clock when needed, in order to transfer data with DMA Stop 0 modes will be entered. Refer to *Background autonomous mode (BAM)* for more details. In Stop modes the bus clocks when requested use HSI16.

  Stop 0 offer the largest number of active peripherals, with or without DMA, and wake-up sources, a smaller wake-up time but a higher consumption than Stop 1.

  In Stop 0 mode, the main regulator remains ON, allowing a very fast wake-up time, but with much higher power consumption.

  Stop 1 is the lowest power mode with full retention, but the functional peripherals and sources of wake-up are reduced.

  The BOR can be configured in ultra-low power mode to further reduce power consumption during Stop 1 mode.

  The system clock when exiting from Stop 0 or Stop 1 modes is HSI16.

- **Standby retention and Standby**

  The Standby mode is used to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16 and the HSE32 crystal oscillators are also switched off. The LSE or LSI is still running.

  The RTC and IWDG can remain active.

  The BOR always remains active in Standby mode.

  The BOR can be configured in ultra-low power mode to further reduce power consumption during Standby mode.

  The state of each I/O during Standby mode can be retained with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAMs and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, the full SRAM1 and/or SRAM2 can be retained in Standby mode, supplied by the low-power regulator (Standby with RAM retention mode). Also optionally the 2.4 GHz RADIO can be retained in Standby mode, supplied by the low-power regulator (Standby with 2.4 GHz RADIO retention mode).

  The device exits Standby modes when an external reset (NRST pin), an IWDG event or reset, WKUP pin event (configurable rising or falling edge), an RTC event occurs (alarm, periodic wake-up, timestamp), or a tamper detection. The tamper detection can be raised either due to external pins or due to an internal failure detection.

  When in Standby with 2.4 GHz RADIO retention mode also the SLEEP_TIMER can exit the device from Standby mode.

  The system clock after wake-up is HSI16.

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Background autonomous mode (BAM)

The devices support BAM (background autonomous mode), that allows peripherals to be functional and autonomous in Stop mode (Stop 0 and Stop 1 modes), so without any software running.

In Stop 0 modes, the autonomous peripherals are the following: ADC4, LPTIM1, USART1, LPUART1, SPI3, I2C3, 2.4 GHz RADIO, and GPDMA1. In this mode the GPDMA1 can be used to transfer data or control peripherals and access SRAM1 and SRAM2. The ADC4 can also be used to measure temperature. The 2.4 GHz RADIO is autonomous only in Stop 0 range 1.

In Stop 1 mode, the autonomous peripherals are the following: ADC4, LPTIM1, USART1, LPUART1, SPI3, I2C3. These peripherals can request a transition to Stop 0 mode allowing then data transfers with GPDMA1.

Those peripherals support the features detailed below:

- Functionality in Stop mode thanks to its own independent clock (named kernel clock) request capability: the peripheral kernel clock is automatically switched on when requested by a peripheral, and automatically switched off when no peripheral requests it.
- DMA transfers supported in Stop 0 mode thanks to system clock request capability: the system clock (HSI16) automatically switched on when requested by a peripheral, and automatically switched off when no peripheral requests it. When the system clock is requested by an autonomous peripheral, Stop 0 mode is automatically entered and the system clock is woken up and distributed to all peripherals enabled in the RCC. This allows the DMA to access the enabled SRAM, and any enabled peripheral register (for instance GPIO registers). When no peripheral requests its bus clock Stop 1 mode is automatically re-entered when Stop 1 mode selected as low-power mode.
- Automatic start of the peripheral thanks to hardware synchronous or asynchronous triggers (such as I/Os edge detection and low-power timer event).
- Wake-up from Stop mode with peripheral interrupt.

The GPDMA is fully functional and the linked-list is updated in Stop 0 mode, allowing the different DMA transfers to be linked without any CPU wake-up. This can be used to chain different peripherals transfers, or to write peripherals registers, to change their configuration while remaining in Stop 0 mode.

The DMA transfers from memory to memory can be started by hardware synchronous or asynchronous triggers, and the DMA transfers between peripherals and memories can also be gated by those triggers.

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Here below some use-cases that can be done while remaining in Stop mode:

- A/D conversion triggered by a low-power timer (or any other trigger)
  - wake-up from Stop mode on analog watchdog if the A/D conversion result is out of programmed thresholds
  - wake-up from Stop mode on DMA buffer event
- I^2C slave reception or transmission, SPI reception, UART/LPUART reception
  - wake-up at the end of peripheral transfer or on DMA buffer event
- I^2C master transfer, SPI transmission, UART/LPUART transmission, triggered by a low-power timer (or any other trigger):
  - example: sensor periodic read
  - wake-up at the end of peripheral transfer or on DMA buffer event
- Bridges between peripherals
  - example: ADC converted data transferred by communication peripherals
- Data transfer from/to GPIO to/from SRAM for:
  - controlling external components
  - implementing data transmission and reception protocols

Table 7. Functionalities depending on the working mode(1)

Peripheral	Run		Sleep		Stop 0			Stop 1		Standby retention		Standby	
	Range 1	Range 2	Range 1	Range 2	Range 1	Range 2	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability
CPU	Y		R		R		-	R	-	-	-	-	-
Flash memory	O(2)		O(2)		R		-	R	-	R	-	R	-
SRAM1	O		O		O(3)		-	O(3)	-	O(3)	-	O(3)	-
SRAM2	O		O		O(3)		O(4)	O(3)		O(3)	-	O(3)	-
Backup registers	O		O		O		-	R	-	R	-	R	-
ICACHE	O		R		R		-	R	-	-	-	-	-
2.4 GHz RADIO	O	R	O	R	O	R	O	R	-	-	-	-	-
2.4 GHz RADIO SRAM	O	R	O	R	O	R	-	R	-	R	-	-	-
SLEEP_TIMER	O		O		O		O	O	O	O	O	-	-
BOR	Y		Y		Y		Y	Y	Y	Y	Y	Y	Y
PVD	O		O		O		O	O	O	-	-	-	-
HSI16	O		O		O(5)		-	O(5)	-	-	-	-	-
HSE32	O		O		O(6)	-	-	-	-	-	-	-	-
LSI	O		O		O		-	O	-	O	-	O	-
LSE	O		O		O		-	O	-	O	-	O	-
HSECSS	O		O		O	-	O	-	-	-	-	-	-

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Table 7. Functionalities depending on the working mode(1) (continued)

Peripheral	Run		Sleep		Stop 0			Stop 1		Standby retention		Standby	
	Range 1	Range 2	Range 1	Range 2	Range 1	Range 2	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability
LSECSS	O		O		O		O	O	O	O	O	O	O
IWDG	O		O		O		O	O	O	O	O	O	O
RTC	O		O		O		O	O	O	O	O	O	O
TAMP tamper pins	3		3		3		O	3	O	3	O	3	O
GPIO pins	O		O		O		O	O	O	O/R(7)	O(8)	O/R(7)	O(8)
U(S)ART1	O		O		O		O(9)	O	O(9)	-	-	-	-
LPUART1	O		O		O		O(9)	O	O(9)	-	-	-	-
I2C3	O		O		O		O(10)	O	O(10)	-	-	-	-
SPI3	O		O		O		O(11)	O	O(11)	-	-	-	-
ADC4	O		O		O		O(12)	O	O(12)	-	-	-	-
LPTIM1	O		O		O		O(13)	O	O(13)	-	-	-	-
GPDMA1	O		O		O		O(14)	R	-	-	-	-	-
TIMx (x = 1, 2, 16)	O		O		R		-	R	-	-	-	-	-
TSC	O		O		R		-	R	-	-	-	-	-
RNG	O		O		R		-	R	-	-	-	-	-
AES	O		O		R		-	R	-	-	-	-	-
PKA	O		O		R		-	R	-	-	-	-	-
HASH	O		O		R		-	R	-	-	-	-	-
CRC	O		O		R		-	R	-	-	-	-	-
WWDG	O		O		R		-	R	-	-	-	-	-
SysTick timer	O		O		R		-	R	-	-	-	-	-
HSEM	O		R		R		-	R	-	-	-	-	-
DBGMCU	O		O		O(15)		-	O(15)	-	O(16)	-	O(16)	-

1. Legend: Y = yes (enabled). O = optional (disabled by default, can be enabled by software).R = retained, - = not available. Gray cells highlight the wake-up capability in each mode.
2. The flash memory can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAMs can be powered on or off independently.
4. Parity error interrupt or NMI wake-up from Stop mode.
5. Some peripherals with autonomous mode and wake-up from Stop capability can request HSI16 to be enabled. In this case, the oscillator is woken up by the peripheral, and is automatically put off when no peripheral needs it.
6. The 2.4 GHz RADIO peripheral in autonomous mode request HSE32 to be enabled. In this case, the oscillator is kept active by the peripheral, and is automatically put off when it no longer needs it.
7. I/O levels can be retained with pull-up, pull-down, or floating.
8. There are 8 wake-up pins available.

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9. U(S)ART and LPUART reception and transmission are functional and autonomous in Stop mode in asynchronous and in SPI master modes, and generate a wake-up interrupt on transfer events.
10. I2C reception and transmission is functional and autonomous in Stop mode and generates a wake-up interrupt on transfer events.
11. SPI reception and transmission is functional and autonomous in Stop mode and generates a wake-up interrupt on transfer events.
12. A/D conversion is functional and autonomous in Stop mode, and generates a wake-up interrupt on conversion events.
13. LPTIM is functional and autonomous in Stop mode, and generates a wake-up interrupt on events.
14. GPDMA transfers are functional and autonomous in Stop 0 mode, and generates a wake-up interrupt on transfer events.
15. DBGMCU remains accessible trough AP0.
16. DBGMCU remains accessible through AP0 when CDBGPWRUPREQ is set.

3.9.3 Reset mode

To improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.10 Reset and clock controller (RCC)

The RCC (reset and clock controller) manages device and peripheral reset and distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- Device reset source monitoring.
- Individual peripheral reset control.
- Clock prescaler: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- Clock selection system: clock sources can be changed safely on-the-fly in Run mode through a configuration register.
- Clock management: to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory.
- System clock source: different clock sources can be used to drive the system clock SYSCLK:
  - HSE32 (32 MHz high-speed external crystal oscillator), trimmable by software. The HSE32 can also be used with an external clock.
  - HSI16 (16 MHz high-speed internal RC oscillator), trimmable by software.
  - System PLL that can be fed by HSE32 or HSI16 with a maximum output frequency at 100 MHz.
- Auxiliary clock source: three ultra-low power clock sources that can be used to drive, for instance, the real-time clock:
  - LSE (32.000 kHz or 32.768 kHz low-speed external crystal oscillator), supporting programmable drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - LSI (32 kHz low-speed internal RC oscillators), also used to drive the independent watchdog. The LSI1 clock absolute accuracy is ±5%, it can be divided by 128 to output a 250 Hz as source clock.

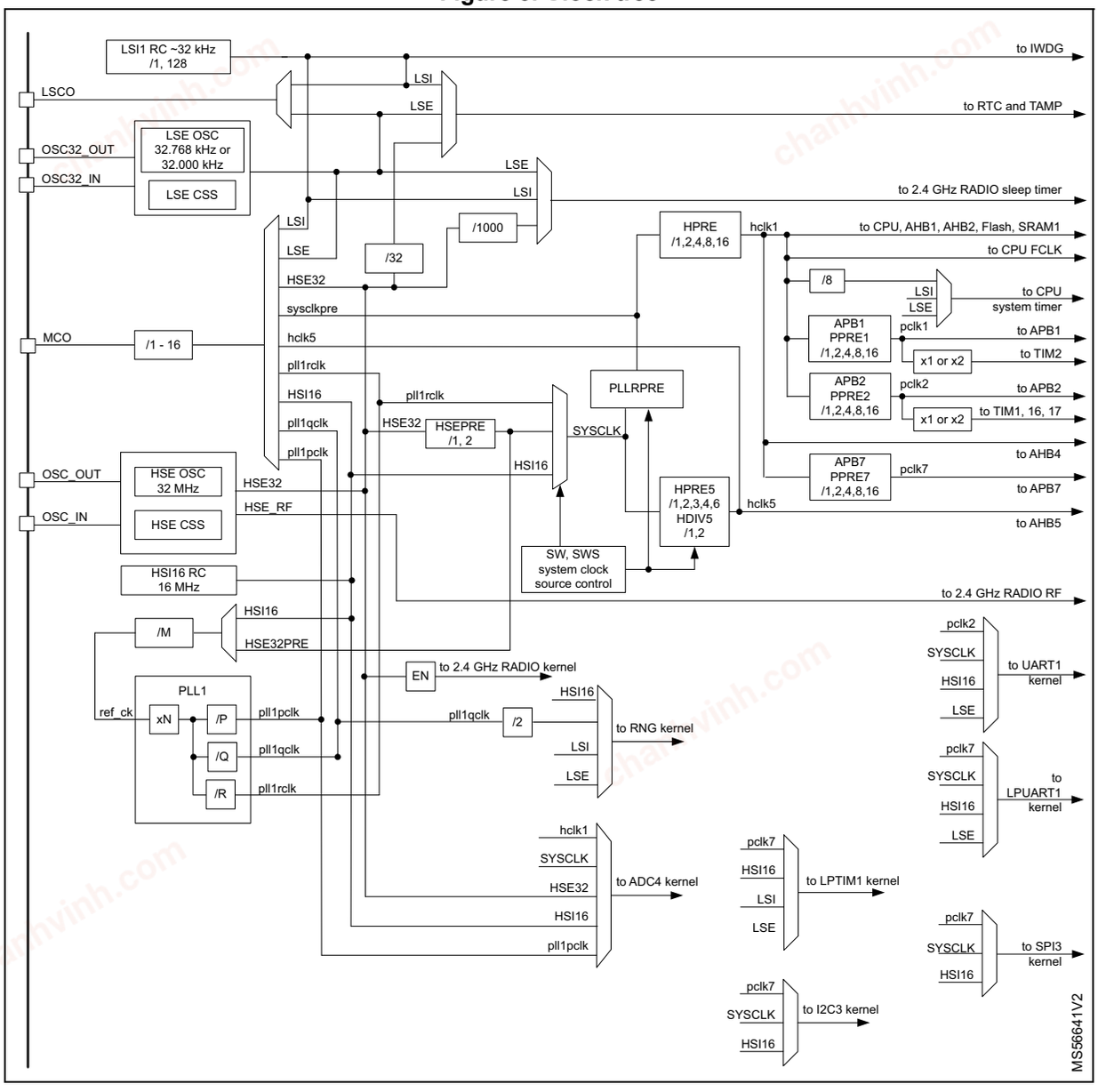
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- Peripheral clock sources: several peripherals have their own independent kernel clock whatever the system clock. The PLL has three independent outputs allowing the highest flexibility and can generate clocks for the ADC and the RNG.
- Startup clock: after reset, the microcontroller restarts by default with the HSI16. The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- CSS (Clock security systems): these features can be enabled by software.
  - If a HSE32 clock failure occurs, the system clock automatically switches to HSI16 and a software interrupt is generated if enabled.
  - LSE failure can also be detected and generates an interrupt, in this case the clock switches to LSI.
- Clock-out capability:
  - MCO (microcontroller clock output): outputs one of the internal clocks for external use by the application. (only available in Run, Sleep and Stop mode)
  - LSCO (low-speed clock output): outputs LSI or LSE in all operating modes.

Several prescalers allow AHB and APB frequencies configuration. The maximum frequency of the AHB and the APB clock domains is 100 MHz, except for AHB5 domain, limited to 32 MHz.

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Figure 5. Clock tree



3.11 General-purpose input/output (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked, if needed, following a specific sequence in order to avoid spurious writing to the I/Os registers.

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The GPIO allows dynamic I/O control in Stop 0 mode thanks to GPDMA1. All I/Os can be configured and controlled as input or output (open-drain or push-pull depending on GPIO configuration).

When enabled in the PWR, latest I/Os output level can be retained by pulling the I/Os high or low before entering Standby mode. I/O levels are retained after exit from Standby mode, until they are reconfigured by software.

3.12 System configuration controller (SYSCFG)

The main purpose of the SYSCFG (system configuration controller) are the following:

- Managing robustness features
- Configuring FPU interrupts
- Enabling/disabling the I^2C fast-mode plus high-drive mode of some I/Os and booster for I/Os analog switches
- Managing the I/O compensation
- Provides memory erase status

3.13 Peripheral interconnect matrix

Several peripherals have direct connections between them, to have autonomous communication between them and to support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep and Stop modes.

3.14 General purpose direct memory access controller (GPDMA)

This controller is a bus master and system peripheral.

The GPDMA is used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

The GPDMA main features are:

- Dual bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Run, Sleep and Stop 0 modes
- Transfers arbitration based on a four-grade programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)

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- Per channel event generation, on any of the following events: transfer complete or half transfer complete or data transfer error or user setting error, and/or update linked-list item error or completed suspension
- Per channel interrupt generation, with separately programmed interrupt enable per event
- Eight concurrent DMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intra-channel DMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intra-channel and inter-channel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - Programmable DMA request and trigger selection
  - Programmable DMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting including FIFO level and event flags

Table 8. GPDMA1 channels implementation and usage

Channel x	Hardware parameters		Features
	dma_fifo_ size[x]	dma_ addressing[x]	
x = 0 to 5	2	0	Channel x is implemented with: – a FIFO of 8 bytes, 2 words – fixed/contiguously incremented addressing These channels may be also used for GPDMA transfers, between an APB or AHB peripheral and SRAM.
x = 6 to 7	4	0	Channel x is implemented with: – a FIFO of 32 bytes, 8 words – fixed/contiguously incremented addressing These channels may be also used for GPDMA transfers, between a demanding AHB or APB peripheral and SRAM.

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Table 9. GPDMA1 autonomous mode and wake-up in low-power modes

Feature	Low-power modes
Autonomous mode and wake-up	Sleep, Stop 0 modes

3.15 Interrupts and events

3.15.1 Nested vectored interrupt controller (NVIC)

The devices embed a NVIC (nested vectored interrupt controller) that is able to manage 16 priority levels and to handle up to 72 maskable interrupt vectors plus the 16 interrupt vectors of the Cortex-M33.

The NVIC benefits are the following:

- closely coupled NVIC giving low-latency interrupt processing
- interrupt entry vector table address passed directly to the core
- early processing of interrupts
- processing of late arriving higher priority interrupts
- support for tail chaining
- processor state automatically saved
- interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.15.2 Extended interrupt/event controller (EXTI)

The EXTI (extended interrupts and event controller) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run and Sleep modes. The EXTI also includes the peripheral interconnect EXTI multiplexer I/O port selection.

The EXTI main features are the following:

- All event inputs allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Selectable active trigger edge
  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt and event generation
  - Software trigger possibility
- EXTI I/O port selection for peripheral interconnect use.

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3.16 Cyclic redundancy check calculation unit (CRC)

The CRC is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, that can be ulteriorly compared with a reference signature generated at link-time and that can be stored at a given memory location.

3.17 Analog-to-digital converter (ADC4)

The devices embed one successive approximation analog-to-digital converter.

Table 10. ADC features

ADC modes/features[1]	ADC4
Resolution	12 bits
Maximum sampling speed for 12-bit resolution	2.5 Msps
Hardware offset calibration	X
Hardware linearity calibration	-
Single-ended inputs	X
Differential inputs	-
Injected channel conversion	-
Oversampling	Up to x256
Data register	16 bits
DMA support	X
Autonomous mode	X
Offset compensation	-
Gain compensation	-
Number of analog watchdogs	3
Wake-up from Stop mode	X

1. X = supported.

3.17.1 Analog-to-digital converter (ADC4)

The 12-bit ADC4 is a successive approximation analog-to-digital converter. It has up to 19 multiplexed channels allowing it to measure signals from 8 external and 3 internal sources (the other channels are reserved). ADC conversion of the various channels can be performed in Single, Continuous, Scan or Discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

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The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

An efficient low-power mode is implemented to allow very low consumption at low frequency. The ADC4 is autonomous in low-power modes down to Stop modes.

A built-in hardware oversampler allows analog performances to be improved while off-loading the related computational burden from the CPU.

The ADC4 main features are:

- High performance
  - 12-, 10-, 8- or 6-bit configurable resolution
  - ADC conversion time: 0.4 µs for 12-bit resolution (2.5 MHz), faster conversion times obtained by lowering resolution
  - Self-calibration
  - Programmable sampling time
  - Data alignment with built-in data coherency
  - DMA support
- Low-power
  - PCLK frequency reduced for low-power operation while still keeping optimum ADC performance
  - Wait mode: ADC overrun prevented in applications with low frequency PCLK
  - Auto-off mode: ADC automatically powered off except during the active conversion phase, dramatically reducing the ADC power consumption
  - Autonomous mode: In low-power modes down to Stop 1 mode, the ADC4 is automatically switched on when a trigger occurs to start conversion, and it is automatically switched off after conversion. Data are transfered to SRAM with DMA.
  - ADC4 interrupts wake up the device from Stop modes.
- Analog input channels
  - Eight external analog inputs
  - One channel for the internal temperature sensor (V_{SENSE})
  - One channel for the internal reference voltage (V_{REFINT})
  - One channel for the internal digital core voltage (V_{CORE})
- Start-of-conversion can be initiated:
  - By software
  - By hardware triggers with configurable polarity (timer events or GPIO input events)
- Conversion modes
  - Conversion of a single channel or scan of a sequence of channels
  - Selected inputs converted once per trigger in Single mode
  - Selected inputs converted continuously in Continuous mode
  - Discontinuous mode
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion, and in case of analog watchdog or overrun events, with wake-up from Stop capability
- Three analog watchdogs

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- ADC supply requirements: 1.62 to 3.6 V
- ADC input range: $V_{SSA} < V_{IN} < V_{DDA}$

Note: The ADC4 analog block clock frequency after the ADC4 prescaler must be between 140 kHz and 55 MHz.

Note: V_{SSA} is connected to package pin VSS.

3.17.2 Temperature sensor (V_{SENSE})

The temperature sensor generates a voltage V_{SENSE} that varies linearly with temperature. The temperature sensor is internally connected to ADC4 input channel that is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by STMicroelectronics in the system memory area, accessible in read-only mode.

Table 11. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	Temperature sensor ADC4 12-bit raw data acquired at (30 ± 5) °C, V_{DDA} = 3.0 V (± 10 mV)	0x0BF9 0710 - 0x0BF9 0711
TS_CAL2	Temperature sensor ADC4 12-bit raw data acquired at (130 ± 5) °C, V_{DDA} = 3.0 V (± 10 mV)	0x0BF9 0742 - 0x0BF9 0743

3.17.3 Internal voltage reference (V_{REFINT})

The internal voltage reference voltage V_{REFINT} provides a stable (bandgap) voltage for the ADC. The V_{REFINT} is internally connected to ADC4 input channel that is used to convert the voltage into a digital value.

The precise voltage of VREFINT is individually measured for each part by STMicroelectronics during production test and stored in the system memory area. It is accessible in read-only mode.

Table 12. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Internal voltage reference ADC4 12-bit raw data acquired at (30 ± 5) °C, V_{DDA} = 3.0 V (± 10 mV)	0x0BF9 07A5 - 0x0BF9 07A6

3.18 Touch sensing controller (TSC)

The TSC (touch sensing controller) provides a simple solution to add capacitive sensing functionality to any application. A capacitive sensing technology is able to detect finger

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presence near an electrode that is protected from direct touch by a dielectric (glass, plastic or other). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The TSC is fully supported by the STMTouch touch sensing firmware library that is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The TSC main features are the following:

- Proven and robust surface charge transfer acquisition principle
- Support of up to 12 capacitive sensing channels
- Up to three capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to three capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the packages and subject to I/O availability.

3.19 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a non-deterministic random bit generator (NDRBG).

The true random generator:

- Delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage
- Can be used as entropy source to construct a non-deterministic random bit generator (NDRBG)
- Produces four 32-bit random samples every 412 AHB clock cycles if f_{AHB} < 77 MHz (256 RNG clock cycles otherwise)
- Embeds start-up and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- Can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration)

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- Has an AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored)

3.20 Advanced encryption standard hardware accelerator (AES)

The devices embed one AES accelerator (AES).

The AES can be used to encrypt and decrypt data using the AES algorithm. It is a fully compliant implementation of the advanced encryption standard (AES) as defined by Federal Information Processing Standards Publication (FIPS PUB 197, Nov 2001).

Multiple chaining modes are supported for key sizes of 128 or 256 bits. ECB, CBC, CTR, CCM, GCM and GMAC chaining are supported.

The AES supports DMA single transfers for incoming and outgoing data (two DMA channels required).

The AES supports the selection of the 256-bit software key, written by the application in the key registers (write only).

Note: 128-bit key size can also be selected.

The peripheral supports:

- Compliant implementation of standard NIST *Special Publication 197, Advanced Encryption Standard (AES)* and *Special Publication 800-38A, Recommendation for Block Cipher Modes of Operation*
- 128-bit data block processing
- Support for cipher keys length of 128-bit and 256-bit
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- 51 or 75 clock cycle latency in ECB encryption mode for AES processing one 128-bit block of data with, respectively, 128- or 256-bit key
- Integrated round key scheduler to compute the last round key for AES ECB/CBC decryption
- 256-bit register for storing the cryptographic key (four 32-bit registers), with key atomicity enforcement
- 128-bit registers for storing initialization vectors (four 32-bit registers)
- One 32-bit input buffer and one 32-bit output buffer
- Automatic data flow control with support of single-transfer direct memory access (DMA) using two channels (one for incoming data, one for processed data)
- Data swapping logic to support 1-, 8-, 16- or 32-bit data
- Possibility for software to suspend a message if the AES needs to process another message with a higher priority (suspend/resume operation)

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Table 13. AES features

AES modes/features(1)	AES
ECB, CBC chaining	X
CTR, CCM, GCM chaining	X
AES 128-bit ECB encryption in cycles	51

1. X = supported.

3.21 HASH hardware accelerator (HASH)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA2-224, SHA-256), the MD5 (message-digest algorithm 5) hash algorithm and the keyed-hash message authentication code (HMAC) algorithm. HMAC is suitable for applications requiring message authentication.

The HASH computes Federal information processing standards (FIPS) approved digests of length of 160, 224, 256 bits, for messages of up to (2^{64} – 1) bits. It also computes 128 bits digests for the MD5 algorithm.

The HASH main features are:

- Suitable for data authentication applications, compliant with:
  - Federal Information Processing Standards Publication FIPS PUB 180-4, *Secure Hash Standard* (SHA-1 and SHA-2 family)
  - Federal Information Processing Standards Publication FIPS PUB 186-4, *Digital* Signature Standard (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 1321, *MD5* Message-Digest Algorithm
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, *HMAC: Keyed-Hashing for Message Authentication* and Federal Information Processing Standards Publication FIPS PUB 198-1, *The Keyed-Hash Message* Authentication Code (HMAC)
- Fast computation of SHA-1, SHA2-224, SHA-256, and MD5
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
  - 66 clock cycles for processing one 512-bit block of data using MD5 algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit string
  - Word swapping supported: bits, bytes, half-words and 32-bit words
- Automatic padding to complete the input bit string to fit digest minimum block size of 512 bits (16 × 32 bits)
- Single 32-bit input register associated to an internal input FIFO of sixteen 32-bit words, corresponding to one block size
- AHB slave peripheral, accessible through 32-bit word accesses only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H7) for output message digest

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- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of 4 supported.
- Interruptible message digest computation, on a per-32-bit word basis
  - Re-loadable digest registers
  - Hashing computation suspend/resume mechanism, including using DMA

3.22 Public key accelerator (PKA)

The PKA is intended for the computation of cryptographic public key primitives, specifically those related to RSA, DU (Diffie-Hellmann) or (ECC) elliptic curve cryptography over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

The PKA main features are:

- Acceleration of RSA, DH and ECC over GF(p) operations, based on the Montgomery method for fast modular multiplications. More specifically:
  - RSA modular exponentiation, RSA CRT (Chinese remainder theorem) exponentiation
  - ECC scalar multiplication, point on curve check, complete addition, double base ladder, projective to affine
  - ECDSA signature generation and verification
- Capability to handle operands up to 4160 bits for RSA/DH and 640 bits for ECC
- Arithmetic and modular operations such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication
- Built-in Montgomery domain inward and outward transformations

3.23 Timers and watchdogs

The devices include one advanced control timer, two general-purpose timers, one low-power timer, two watchdog timers, and two SysTick timers.

Table 14 compares the features of the advanced control and general-purpose timers.

Table 14. Timers comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16 bits	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2	32 bits	Up, down, up/down			4	No
	TIM16	16 bits	Up			1	1

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3.23.1 Advanced-control timers (TIM1)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes) with full modulation capability (0 - 100%)
- One-pulse mode output

In Debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in the next section) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the *Timer Link* feature for synchronization or event chaining.

3.23.2 General-purpose timers (TIM2, TIM16)

There are two synchronizable general-purpose timers embedded in the device (see *Table 14* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2
  - Full-featured general-purpose timer with 32-bit auto-reload up/downcounter, with 16-bit prescaler.
  - Feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.
  - The counters can be frozen in Debug mode.
  - Independent DMA request generation, support of quadrature encoders.
- TIM16
  - General-purpose timers with mid-range features.
  - 16-bit auto-reload upcounters and 16-bit prescalers. and one channel and one complementary channel.
  - All channels can be used for input capture/output compare, PWM or one-pulse mode output.
  - The counters can be frozen in Debug mode.
  - Independent DMA request generation.

3.23.3 Low-power timer (LPTIM1)

The devices embed one low-power timer, with an independent clock, running in Stop mode if clocked by HSI16, LSE, LSI, or an external clock. This timer is able to wake up the system from Stop mode.

LPTIM1 is active in Stop modes.

The low-power timer supports the following features:

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- 16-bit up counter with 16-bit autoreload register
- 3-bit prescaler with following possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working with no LP oscillator running, used by *Pulse Counter* application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
  - Update event
  - Input capture

3.23.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and a 10-bit prescaler. It is clocked from the independent LSI and, as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software enabled through the option bytes. The counter can be frozen in low-power and Debug mode.

3.23.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

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3.23.6 SysTick timer

The Cortex-M33 embeds one SysTick timer.

This timer is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.24 Real-time clock (RTC)

The real-time clock (RTC) is an independent BCD timer/counter. The RTC provides a time-of-day clock/calendar with programmable alarm interrupts.

As long as the V_{DD} supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode or under reset).

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in binary-coded decimal (BCD) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a reference clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period

The RTC is supplied from the V_{DD} supply.

The RTC clock sources can be one of the following:

- LSE, used as 32.768 kHz external crystal oscillator
- LSE, with external resonator or oscillator
- LSI, internal low-power RC oscillator (with typical frequency of 32 kHz)
- HSE32, high-speed external clock divided by a prescaler in the RCC.

The RTC is functional in all low-power modes when it is clocked by the LSE or LSI.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes.

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3.25 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 32-bit backup registers are retained in all low-power modes. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with tamper pins and nine internal tampers. The external tamper pins can be configured for level detection with or without filtering, or active tamper that increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- A tamper detection can erase the backup registers, SRAM2, ICACHE and cryptographic peripherals.
- 32 32-bit backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the Backup domain that remains powered-on by V_{DD} power.
- Up to three tamper pins for external tamper detection events:
  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks
  - Flexible active tamper I/O management: from one (input associated to its own exclusive output) to two meshes (single output shared for up to two tamper inputs)
  - Passive tampers: ultra-low power edge or level detection with internal pull-up hardware management
  - Configurable digital filter
- Nine internal tamper events to protect against transient or environmental perturbation attacks:
  - LSE monitoring
  - RTC calendar overflow
  - JTAG/SWD access if RDP different from 0
  - Monotonic counter overflow
  - Cryptographic peripherals fault (RNG, AES, PKA)
  - Independent watchdog reset when tamper flag is already set
  - Three ADC4 watchdogs
- Each tamper can be configured in two modes:
  - Hardware mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Software mode: erase of secrets following a tamper detection launched by software
- Any tamper detection can generate an RTC time stamp event.
- Monotonic counter

3.26 Inter-integrated circuit interface (I2C)

The device embeds one I2C, refer to *Table 15* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

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The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
  - Slave and Master modes, multi-master capability
  - Standard-mode (Sm), with a bit rate up to 100 Kbit/s
  - Fast-mode (Fm), with a bit rate up to 400 Kbit/s
  - Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 3.0 compatibility:
  - Hardware packet error checking (PEC) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming
- Autonomous functionality in Stop modes with wake-up from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 15. I2C implementation

I2C features[1]	I2C3
Standard-mode (up to 100 Kbit/s)	X
Fast-mode (up to 400 Kbit/s)	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X
Programmable analog and digital noise filters	X
SMBus/PMBus hardware support	X
Independent clock	X
Autonomous in Stop modes with wake-up capability	X

1. X: supported

3.27 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices have one embedded universal synchronous receiver transmitter (USART1) and one low-power universal asynchronous receiver transmitter (LPUART1).

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Table 16. U(S)ART and LPUART features

USART modes/features(1)	USART1	LPUART1
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (master/slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual-clock domain and wake-up from Stop modes	X	X
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto-baud rate detection	X	-
Driver enable	X	X
USART data length	7, 8, and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	8 bytes	
Autonomous mode	X	X

1. X = supported.

3.27.1 USART/UART

The U(S)ART offers a flexible means to perform full-duplex data exchange with external equipments requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The U(S)ART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications up to 20 Mbauds are possible by using the direct memory access (DMA) for multibuffer configuration.

The U(S)ART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data, each of them can be enabled/disabled by software and come with a status flag
- A common programmable transmit and receive baud rate

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- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection
- Programmable data word length (7, 8, or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous Master/Slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from stop capability
- LIN master synchronous break send capability and LIN slave break detection capability
  - 13-bit break generation and 10/11-bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16-bit duration for Normal mode
- Smartcard mode
  - Supports the T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

3.27.2 LPUART

The LPUART supports bidirectional asynchronous serial communication with minimum power consumption. It also supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher-speed clock can be used to reach higher baudrates.

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The LPUART interface can be served by the DMA controller.

The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data, each of them can be enabled/disabled by software and come with status flags for FIFOs states
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7, 8, or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from Stop capability

3.28 Serial peripheral interface (SPI)

The devices embed one SPI (serial peripheral interfaces) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices.

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The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to setup communication with concrete slave and to assure it handles the data flow properly. The Motorola data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4-bit to 32-bit data size selection or fixed to 8-bit and 16-bit only
- Multi master or multi slave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO and MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can secure communication at the end of transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 16 x or 8 x 8-bit embedded Rx and TxFIFOs with DMA capability
- Programmable number of data in transaction
- Configurable FIFO thresholds (data packing)
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Autonomous functionality in Stop modes (handling of the transaction flow and required clock distribution) with wake-up from stop capability
- Optional status pin RDY signalizing the slave device ready to handle the data flow.

Table 17. SPI features

SPI feature[1]	SPI3 (limited feature set instance)
Data size	8- and 16-bit
CRC computation	CRC polynomial length, configurable from 9- to 17-bit
Size of FIFOs	8 x 8-bit

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Table 17. SPI features (continued)

SPI feature[1]	SPI3 (limited feature set instance)
Number of transfered data	Up to 1024, no data counter
Autonomous in Stop modes with wake-up capability	X

1. X: supported

3.29 Development support

3.29.1 Serial-wire/JTAG debug port (SWJ-DP)

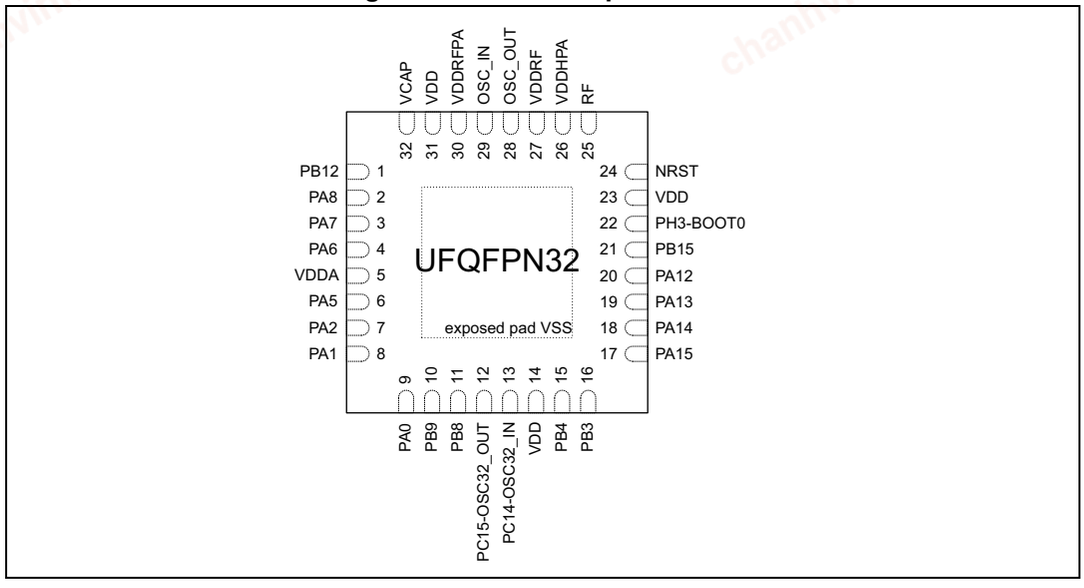
The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

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4 Pinouts and pin description

Figure 6. UFQFPN32 pinout(1) (2)



1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

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Table 18. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V-tolerant I/O
		TT	3.6 V-tolerant I/O
		RF	RF I/O
		RST	Bidirectional reset pin with weak pull-up resistor
		Option for TT or FT I/Os(1)	
		_f	I/O, Fm+ capable
		_a	I/O, with analog switch function supplied by V_{DDA}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 19* are a concatenation of various options. Examples: FT_a, FT_fa, FT_f.

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Table 19. Device pin definitions

Pin			I/O structure	Notes	Alternate functions	Additional functions
Number	Name (function after reset)	Type				
UFQFPN32						
1	PB12	I/O	FT_	-	TIM2_CH1, TIM2_ETR, USART1_TX, TSC_SYNC, EVENTOUT	-
2	PA8	I/O	FT_a	-	MCO, TIM2_CH2, LPTIM1_CH2, SPI3_RDY, USART1_RX, TSC_G1_IO1, EVENTOUT	ADC4_IN1
3	PA7	I/O	FT_fa	-	TIM2_CH3, I2C3_SDA, USART1_CTS, TSC_G1_IO2, EVENTOUT	ADC4_IN2, WKUP8, TAMP_IN1/TAMP_OUT2
4	PA6	I/O	FT_fa	-	CSTOP, TIM2_CH4, I2C3_SCL, SPI3_RDY, USART1_RTS_DE, TSC_G1_IO3, EVENTOUT	ADC4_IN3, WKUP7
5	VDDA	S	-	-	-	-
6	PA5	I/O	FT_a	-	CSLEEP, TIM2_CH1, TIM2_ETR, SPI3_NSS, USART1_CK, TSC_G1_IO4, EVENTOUT	ADC4_IN4, WKUP6
7	PA2	I/O	FT_a	-	TIM1_BKIN, USART1_RTS_DE, LPUART1_TX, TIM16_CH1, EVENTOUT	ADC4_IN7, WKUP4, LSCO
8	PA1	I/O	FT_a	-	TIM1_CH1N, USART1_CK, LPUART1_RX, TSC_G2_IO1, EVENTOUT	ADC4_IN8, WKUP3
9	PA0	I/O	FT_a	-	LPTIM1_IN1, TIM1_CH2N, SPI3_SCK, LPUART1_CTS, TSC_G2_IO2, EVENTOUT	ADC4_IN9, WKUP1
10	PB9	I/O	FT_a	-	TIM1_CH3N, SPI3_MISO, LPUART1_RTS_DE, TSC_G2_IO3, TIM16_CH1, EVENTOUT	ADC4_IN10, WKUP8
11	PB8	I/O	FT_a	-	LPTIM1_ETR, TIM1_CH1, SPI3_MOSI, TSC_G2_IO4, TIM16_CH1N, EVENTOUT	PVD_IN
12	PC15-OSC32_OUT	I/O	FT_	-	EVENTOUT	OSC32_OUT
13	PC14-OSC32_IN	I/O	FT_	-	EVENTOUT	OSC32_IN
14	VDD	S	-	-	-	-
15	PB4	I/O	FT_a	-	NJTRST, TIM1_CH3, TSC_G3_IO1, EVENTOUT	-
16	PB3	I/O	FT_fa	-	JTDO/TRACESWO, TIM1_CH4, LPTIM1_IN2, TSC_G3_IO2, EVENTOUT	-
17	PA15	I/O	FT_fa	-	JTDI, TIM1_ETR, LPTIM1_CH2, TSC_G3_IO3, EVENTOUT	-
18	PA14	I/O	FT_	-	JTCK/SWCLK, EVENTOUT	TAMP_IN3/TAMP_OUT6
19	PA13	I/O	FT_	-	JTMS/SWDIO, EVENTOUT	-
20	PA12	I/O	FT_a	-	TIM1_CH2, TSC_G3_IO4, EVENTOUT	WKUP6
21	PB15	I/O	TT_	-	TIM1_BKIN2, I2C3_SMBA, LPUART1_CTS, TIM16_BKIN, EVENTOUT	-
22	PH3-BOOT0	I/O	TT_	-	EVENTOUT	TAMP_IN2/TAMP_OUT1
23	VDD	S	-	-	-	-

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Table 19. Device pin definitions (continued)

Pin			I/O structure	Notes	Alternate functions	Additional functions
Number	Name (function after reset)	Type				
UFQFPN32						
24	NRST	I/O	RST	-	-	-
25	RF	I/O	RF	-	-	-
26	VDDHPA	S	-	-	-	-
27	VDDRF	S	-	-	-	-
28	OSC_OUT	O	RF	-	-	-
29	OSC_IN	I	RF	-	-	-
30	VDDRFPA	S	-	-	-	-
31	VDD	S	-	-	-	-
32	VCAP	S	-	-	-	-
33	VSS (exposed pad)	S	-	-	-	-

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4.1 Alternate functions

Table 20. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS_AF	TIM1/2	LPTIM1/TIM1/2	-	I2C3	-	I2C3/SPI3	USART1
A	PA0	LPTIM1_IN1	TIM1_CH2N	-	-	-	-	SPI3_SCK	-
	PA1	-	TIM1_CH1N	-	-	-	-	-	USART1_CK
	PA2	-	TIM1_BKIN	-	-	-	-	-	USART1_RTS_DE
	PA5	CSLEEP	TIM2_CH1	TIM2_ETR	-	-	-	SPI3_NSS	USART1_CK
	PA6	CSTOP	TIM2_CH4	-	-	I2C3_SCL	-	SPI3_RDY	USART1_RTS_DE
	PA7	-	TIM2_CH3	-	-	I2C3_SDA	-		USART1_CTS
	PA8	MCO	TIM2_CH2	LPTIM1_CH2	-	-	-	SPI3_RDY	USART1_RX
	PA12	-	TIM1_CH2	-	-	-	-	-	-
	PA13	JTMS/SWDIO	-	-	-	-	-	-	-
	PA14	JTCK/SWCLK	-	-	-	-	-	-	-
	PA15	JTDI	TIM1_ETR	LPTIM1_CH2	-	-	-	-	-
B	PB3	JTDO/TRACESWO	TIM1_CH4	LPTIM1_IN2	-	-	-	-	-
	PB4	NJTRST	TIM1_CH3	-	-	-	-	-	-
	PB8	LPTIM1_ETR	TIM1_CH1	-	-	-	-	SPI3_MOSI	-
	PB9	-	TIM1_CH3N	-	-	-	-	SPI3_MISO	-
	PB12	-	TIM2_CH1	TIM2_ETR	-	-	-	-	USART1_TX
	PB15	-	TIM1_BKIN2	-	-	-	-	I2C3_SMBA	-
C	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-
H	PH3	-	-	-	-	-	-	-	-

1. For AF8 to AF15 refer to *Table 21*.

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Table 21. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	TSC	-	-	-	-	TIM16	EVENTOUT
A	PA0	LPUART1_CTS	TSC_G2_IO2	-	-	-	-	-	EVENTOUT
	PA1	LPUART1_RX	TSC_G2_IO1	-	-	-	-	-	EVENTOUT
	PA2	LPUART1_TX	-	-	-	-	-	TIM16_CH1	EVENTOUT
	PA5	-	TSC_G1_IO4	-	-	-	-	-	EVENTOUT
	PA6	-	TSC_G1_IO3	-	-	-	-	-	EVENTOUT
	PA7	-	TSC_G1_IO2	-	-	-	-	-	EVENTOUT
	PA8	-	TSC_G1_IO1	-	-	-	-	-	EVENTOUT
	PA12	-	TSC_G3_IO4	-	-	-	-	-	EVENTOUT
	PA13	-	-	-	-	-	-	-	EVENTOUT
	PA14	-	-	-	-	-	-	-	EVENTOUT
	PA15	-	TSC_G3_IO3	-	-	-	-	-	EVENTOUT
B	PB3	-	TSC_G3_IO2	-	-	-	-	-	EVENTOUT
	PB4	-	TSC_G3_IO1	-	-	-	-	-	EVENTOUT
	PB8	-	TSC_G2_IO4	-	-	-	-	TIM16_CH1N	EVENTOUT
	PB9	LPUART1_RTS_DE	TSC_G2_IO3	-	-	-	-	TIM16_CH1	EVENTOUT
	PB12	-	TSC_SYNC	-	-	-	-	-	EVENTOUT
	PB15	LPUART1_CTS	-	-	-	-	-	TIM16_BKIN	EVENTOUT
C	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT
H	PH3	-	-	-	-	-	-	-	EVENTOUT

1. For AF0 to AF7 refer to *Table 20*.

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5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C and supply voltage V_{DD} = V_{DDA} = V_{DDRF} = 3 V. They are only given as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error lower than or equal to the value indicated (mean ± 2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines, and are not tested.

5.1.4 Loading capacitor

Unless otherwise specified, the loading conditions used for pin parameter measurement are shown in *Figure 7*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

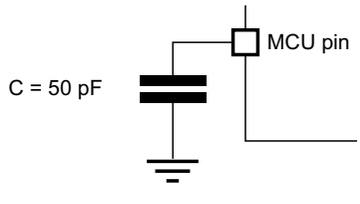
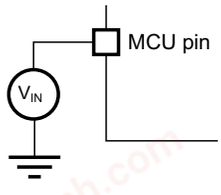


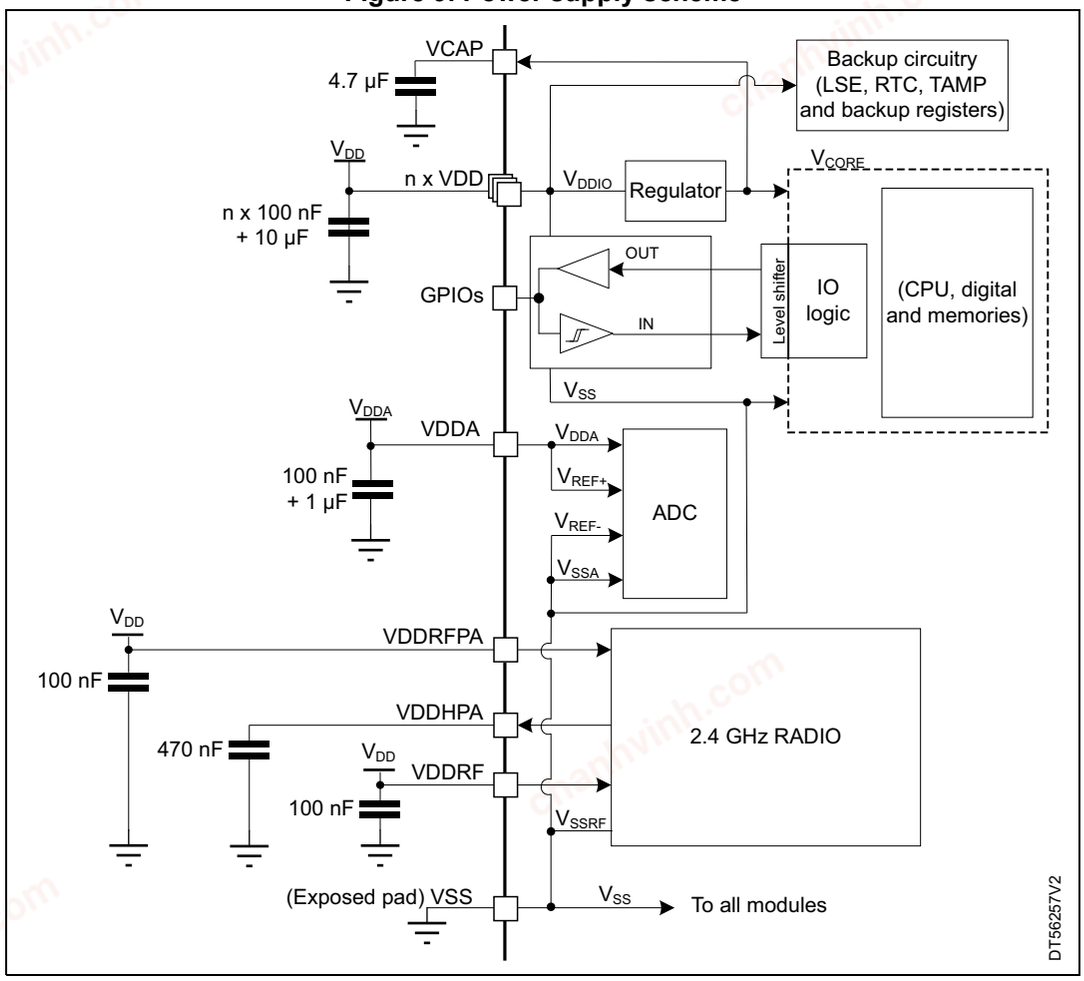
Figure 8. Pin input voltage



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5.1.6 Power supply scheme

Figure 9. Power supply scheme



Caution: Each power supply pair (V_{DD} / V_{SS}, V_{DDA} / V_{SS}, V_{DDRFPA} / V_{SS}, V_{DDRF} / V_{SS}) must be decoupled with filtering ceramic capacitors as shown. These capacitors must be placed as close as possible to (or below) the appropriate pins to ensure correct device functionality.

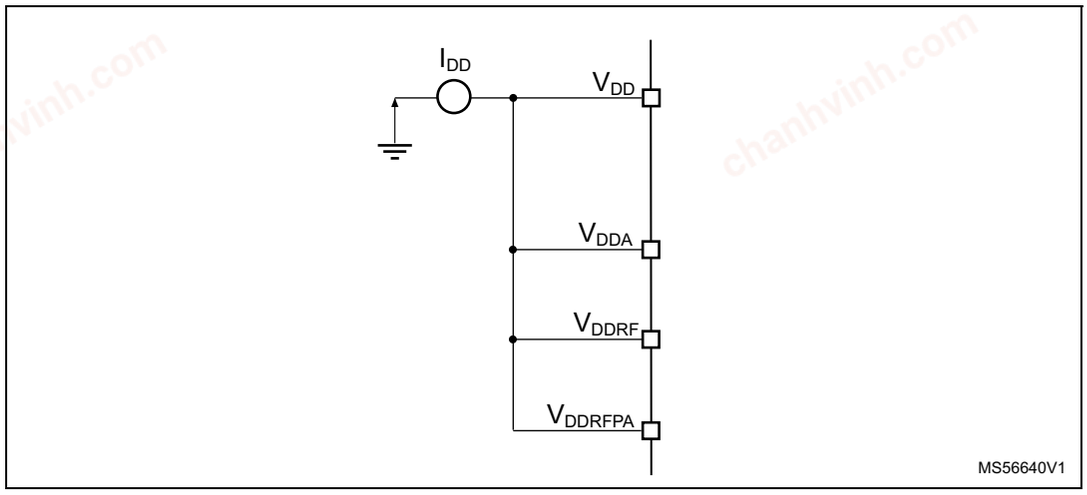
Caution: V_{DD} and V_{DDRF} must be connected to the same supply.

5.1.7 Current consumption measurement

The I_{DD} parameters in the tables in the next sections represent the total MCU consumption, including the current supplying V_{DD}, V_{DDA}, V_{DDRF}, V_{DDRFPA}, or the total 2.4 GHz RADIO current supplying V_{DDRF} and V_{DDRFPA}.

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Figure 10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 22*, *Table 23*, and *Table 24* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 22. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDRF}, V_{DDRFPA})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_ (any option) pins	V_{SS} - 0.3	min (min (V_{DD}, V_{DDA}) + 4.0, 6.0)(3)(4)	
	Input voltage on any other pin		4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different VDDX power pins of the same domain	-	50.0	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50.0	

1. All main power (VDD, VDDA, VDDRF, VDDRFPA) and ground (VSS) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 23* for the maximum allowed injected current values.
3. To sustain a voltage higher than 4 V, the internal pull-up/pull-down resistors must be disabled.
4. This formula applies only to power supplies related to the I/O structure described by the pin definition table. The maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}) + 4.0 V, and 6.0 V.

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Table 23. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	200	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	200	
$IV_{DD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\sum I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	120	
	Total output current sourced by sum of all I/Os and control pins(2)	120	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST pins	–5/+0	
$\sum\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (VDD, VDDA, VDDRF, VDDRFPA) and ground (VSS) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 22* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 24. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_{JMAX}	Maximum junction temperature	140	

5.3 Operating conditions

5.3.1 Summary of main performance

Table 25. Main performance at V_{DD} = 3.3 V

Parameter		Test conditions	Typ	Unit
I_{DD}	Core current consumption	Standby (16 Kbytes RAM retention)	2.58	µA
		Stop 1	22.6	
		Sleep (V_{DD} = 3.0 V, 16 MHz)	0.34	mA
		Run (100 MHz)	6.16	
		Radio BLE Rx 1 Mbps(1)	7.91	
		Radio BLE Tx 0 dBm output power(1)	10.51	

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Table 25. Main performance at V_{DD} = 3.3 V (continued)

Parameter			Test conditions	Typ	Unit
I_{DD}	Peripheral current consumption	BLE	Advertising using Standby mode(2) (Tx = 0 dBm; Period 1.28 s; 31 bytes, 3 channels)	20.3	µA
			Advertising using Standby mode(2) (Tx = 0 dBm, 6 bytes; period 10.24 s, 3 channels)	4.9	

1. Power consumption including RF subsystem and digital processing.
2. Power consumption integrated over 100 s, including Cortex-M33, 2.4 GHz RADIO subsystem and digital processing.

5.3.2 General operating conditions

Table 26. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	1.71(1)	-	3.6	V
V_{DDA}	Analog supply voltage	ADC used	1.62	-	3.6	V
		ADC not used	0	-		
V_{DDRF}	RF operating voltage	-	1.71	-	3.6	V
V_{DDRFPA}	RF power amplifier operating voltage	-	1.15(2)	-	3.6	V
V_{IN}	I/O input voltage	All I/Os FT_ (any option) pins	–0.3	-	Min (min (V_{DD}, V_{DDA}) + 3.6 , 5.5)(3)(4)	V
V_{CORE}	Internal regulator ON	Range 1	1.15	1.21	1.27	V
		Range 2	0.81	0.90	0.99	
f_{HCLK}	Internal AHB1, AHB2, and AHB4 clock frequency	Range 1	-	-	100	MHz
		Range 2	-	-	16	
f_{PCLK}	Internal APB1, APB2, and APB7 clock frequency	Range 1	-	-	100	
		Range 2	-	-	16	
f_{HCLK5}	Internal AHB5 clock frequency	Range 1	-	-	32	
		Range 2	-	-	12	
Δf_{HCLK1}	Internal AHB1, AHB2 and AHB4 clock incremental frequency step(5)	-	-	-	84	MHz
P_D	Power dissipation at T_A = 85 °C (suffix 6 version)	UFQFPN32	See *Section 6.3* for appropriate thermal resistance and package. Power dissipation is calculated according to ambient temperature (T_A), maximum junction temperature (T_J), and selected thermal resistance.			mW
T_A	Ambient temperature (suffix 6 version)	Max power dissipation	–40	-	85	°C
		Low-power dissipation(6)			105	

1. When RESET is released functionality is guaranteed down to V_{BORx} min.
2. When the 2.4 GHz RADIO is active, when inactive supply can go down to 0 V.

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3. This formula applies only to power supplies related to the I/O structure described by the pin definition table. The maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}) + 3.6 V and 5.5 V.
4. For operation with voltages higher than min (V_{DD}, V_{DDA}) + 0.3 V, the internal pull-up/pull-down resistors must be disabled.
5. Without system clock frequency step limiting.
6. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_J max (see *Section 6.3*).

5.3.3 RF characteristics

Table 27. Generic RF transmitter characteristics(1)

Symbol	Parameter		Test conditions	Standard	Min	Typ	Max	Unit
P_{txmax}	Maximum output power		-	-	-	4.0	-	dBm
P_{txmin}	Minimum output power		-	-	-	-20	-	dBm
ΔP_{tx}	Output power step		-	-	-	1	-	dB
$P_{freqband}$	Output power ± variation over the frequency band		P_{txmax} max setting	-	-	0.4	-	
P_{temp}	Output power ± variation over the temperature		P_{txmax} max setting -40 °C ≤ T_J ≤ +105 °C	-	-	2.9	-	
$P_{2ndHARM}$	Second harmonic		P_{txmax} max setting	-	-	-69.5	-	dBm
$P_{3rdHARM}$	Third harmonic		P_{txmax} max setting	-	-	-70.5	-	
$OBSE_{1Mbps}$	Out of band spurious emission 1 Mbps	< 1 GHz	P_{txmax} max setting	(2)	-	-51	-	
		≥ 1 GHz	P_{txmax} max setting		-	-43	-	
$OBSE_{2Mbps}$	Out of band spurious emission 2 Mbps	< 1 GHz	P_{txmax} max setting	(2)	-	-54	-	
		≥ 1 GHz	P_{txmax} max setting		-	-45	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

Table 28. Generic RF receiver characteristics(1)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
$Rssi_{max}$	RSSI maximum value	-	-	-	-32	-	dBm
$Rssi_{min}$	RSSI minimum value	-	-	-	-75	-	
$Rssi_{accu}$	RSSI accuracy	-	-	-	±6	-	dB

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

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Table 29. RF Bluetooth Low Energy characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{op}	Frequency channel operating band	-	2402	-	2480	MHz
ΔF	Delta frequency	-	-	250	-	kHz
Rgfsk	On air data rate	-	0.125	-	2	Mbps
PLLres	RF channel spacing	-	-	2	-	MHz

Table 30. RF transmitter Bluetooth Low Energy characteristics(1)

Symbol	Parameter		Test conditions	Standard	Min	Typ	Max	Unit
$BW6dB_{1Mbps}$	6 dB signal bandwidth		P_{txmax} max setting	-	-	665	-	kHz
$BW6dB_{2Mbps}$	6 dB signal bandwidth		P_{txmax} max setting	-	-	1142	-	
$IBSE_{1Mbps}$	In band spurious emission	2 MHz	-	-20	-	-41	-20	dBm
		≥ 3 MHz	-	-30	-	-47.5	-30	
$IBSE_{2Mbps}$	In band spurious emission	4 MHz	-	-20	-	-42.5	-20	dBm
		5 MHz	-	-20	-	-44	-20	
		≥ 6 MHz	-	-30		-45	-30	
f_d	Frequency drift		-	±50	-50	-	+50	kHz
dr_{max}	Maximum drift rate	Uncoded	-	±20	-20	-	+20	kHz/ 50 µs
		Coded	-	±19.2	-19.2	-	+19.2	
f_o	Frequency offset		-	±150	-150	-	+150	kHz
$Δf1_{1Mbps}$	Frequency deviation average 1 Mbps		-	225 - 275	225	-	275	kHz
$Δf1_{2Mbps}$	Frequency deviation average 2 Mbps		-	450 - 550	450	-	550	
$Δf1_{CodedS8}$	Frequency deviation average Coded S = 8		-	225 - 275	225	-	275	kHz
$Δf2_{1Mbps}$	Frequency deviation 99.9% 1 Mbps			185	185	-	-	kHz
$Δf2_{2Mbps}$	Frequency deviation 99.9% 2 Mbps			370	370	-	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 31. RF receiver Bluetooth Low Energy characteristics (1)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
P_{rxmax}	Maximum input signal	PER ≤ 30.8%	-10	-	6	-	dBm

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Table 31. RF receiver Bluetooth Low Energy characteristics (1) (continued)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
$P_{sens2Mbps}$ (2)	Sensitivity 2 Mbps	-	-70	-	-93	-	dBm
$P_{sens1Mbps}$ (2)	Sensitivity 1 Mbps	-	-70	-	-96	-	
$P_{sens500kbps}$ (2)	Sensitivity 500 kbps	-	-75	-	-99	-	
$P_{sens125kbps}$ (2)	Sensitivity 125 kbps	-	-82	-	-102	-	
$P_{IMD1Mbps}$	Intermodulation 1Mbps	|f2 - f1| = 3 MHz	-50	-50	-37	-	dBm
		|f2 - f1| = 4 MHz		-50	-27	-	
		|f2 - f1| = 5 MHz		-50	-28	-	
$P_{OBB1Mbps}$	Out of band blocking (for desired signal at -67 dBm and 1 Mbps)	30 to 2000 MHz	-30	-30	-10	-	
		2000 to 2399 MHz	-35	-35	-22	-	
		2484 to 2999 MHz	-35	-35	-15	-	
		3 to 12.75 GHz	-30	-30	-10	-	
$P_{IMD2Mbps}$	Intermodulation 2Mbps	|f2 - f1| = 3 MHz	-50	-50	-37	-	dBm
		|f2 - f1| = 4 MHz		-50	-30	-	
		|f2 - f1| = 5 MHz		-50	-30	-	
$P_{OBB2Mbps}$	Out of band blocking (for desired signal at -67 dBm and 2 Mbps)	30 to 2000 MHz	-30	-30	-10	-	
		2000 to 2399 MHz	-35	-35	-33	-	
		2484 to 2999 MHz	-35	-35	-19	-	
		3 to 12.75 GHz	-30	-30	-10	-	
$C/Ico_{125kbps}$	Co-channel rejection 125 kbps	-	12	-	3	-	dB
$C/I_{125kbps}$	Adjacent channel interference 125 kbps	Adj = ±1 MHz	6	-	-2	6	
		Adj = 2 MHz	-26	-	-38	-26	
		Adj-Image = -2 MHz	-18	-	-27	-18	
		Adj ≥ 3 MHz	-36	-	-43	-36	
		Adj = -3 MHz	-24	-	-28	-24	
		Adj ≤ -4 MHz	-36	-	-43	-36	
$C/Ico_{250kbps}$	Co-channel rejection 250 kbps	-	17	-	5	17	
$C/I_{500kbps}$	Adjacent channel interference 500 kbps	Adj = ±1 MHz	11	-	-2	11	
		Adj = 2 MHz	-21	-	-34	-21	
		Adj-Image = -2 MHz	-13	-	-26	-13	
		Adj ≥ 3 MHz	-31	-	-39	-31	
		Adj = -3 MHz	-19	-	-27	-19	
		Adj ≤ -4 MHz	-31	-	-37	-31	

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Table 31. RF receiver Bluetooth Low Energy characteristics (1) (continued)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
C/Ico_{1Mbps}	Co-channel rejection 1 Mbps	-	21	-	8	21	dB
C/I_{1Mbps}	Adjacent channel interference 1 Mbps	Adj = ±1 MHz	15	-	0	15	
		Adj = 2 MHz	-17	-	-38	-17	
		Adj-Image = -2 MHz	-9	-	-23	-9	
		Adj ≥ 3 MHz	-27	-	-36	-27	
		Adj = -3 MHz	-15	-	-27	-15	
		Adj ≤ -4 MHz	-27	-	-38	-27	
C/Ico_{2Mbps}	Co-channel rejection 2 Mbps	-	21	-	8	21	
C/I_{2Mbps}	Adjacent channel interference 2 Mbps	Adj = ±2 MHz	15	-	0	15	
		Adj = 4 MHz	-17	-	-35	-17	
		Adj-Image = -4 MHz	-9	-	-23	-9	
		Adj = ≥ 6 MHz	-27	-	-33	-27	
		Adj = -6 MHz	-15	-	-26	-15	
		Adj = ≤ -8 MHz	-27	-	-34	-27	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. With ideal transmitter.

Table 32. RF Bluetooth Low Energy power consumption for V_{DD} = 3.3 V(1)(2)

Symbol	Parameter	Typ	Unit
I_{tx}	Tx 0 dBm output power consumption	10.51	mA
I_{rx}	Rx consumption 1 Mbps	7.91	
	Rx consumption 2 Mbps	TBD	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Power consumption including 2.4 GHz RADIO subsystem and digital processing.

5.3.4 Operating conditions at power-up/down

The parameters in *Table 33* are evaluated by characterization under ambient temperature and supply voltage conditions summarized in *Table 26*.

Table 33. Operating conditions at power-up/down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate	ULPMEN = 0	20	∞	µs/V
		Standby mode with ULPMEN = 1	250	∞	ms/V

1. Evaluated by characterization, not tested in production, unless otherwise specified.

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5.3.5 Embedded reset and power control block characteristics

The parameters in *Table 34* are derived under ambient temperature and supply voltage conditions summarized in *Table 26*.

Table 34. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after V_{BOR0} threshold detection	V_{DD} rising	-	-	900	µs
V_{BOR0}(2)	Brown-out reset threshold 0	V_{DD} rising	1.60	1.66	1.71	V
		V_{DD} falling	1.58	1.64	1.69	
V_{BOR1}(2)	Brown-out reset threshold 1	V_{DD} rising	1.98	2.08	2.17	
		V_{DD} falling	1.90	2.00	2.10	
V_{BOR2}(2)	Brown-out reset threshold 2	V_{DD} rising	2.18	2.29	2.39	
		V_{DD} falling	2.08	2.18	2.25	
V_{BOR3}(2)	Brown-out reset threshold 3	V_{DD} rising	2.48	2.59	2.70	
		V_{DD} falling	2.39	2.50	2.61	
V_{BOR4}(2)	Brown-out reset threshold 4	V_{DD} rising	2.76	2.88	3.00	
		V_{DD} falling	2.67	2.79	2.90	
V_{PVD0}(2)	Programmable voltage detector threshold 0	V_{DD} rising	2.03	2.13	2.23	V
		V_{DD} falling	1.93	2.03	2.12	
V_{PVD1}(2)	PVD threshold 1	V_{DD} rising	2.18	2.29	2.39	
		V_{DD} falling	2.08	2.18	2.28	
V_{PVD2}(2)	PVD threshold 2	V_{DD} rising	2.33	2.44	2.55	
		V_{DD} falling	2.23	2.34	2.44	
V_{PVD3}(2)	PVD threshold 3	V_{DD} rising	2.47	2.59	2.70	
		V_{DD} falling	2.39	2.50	2.61	
V_{PVD4}(2)	PVD threshold 4	V_{DD} rising	2.60	2.72	2.83	
		V_{DD} falling	2.50	2.62	2.73	
V_{PVD5}(2)	PVD threshold 5	V_{DD} rising	2.76	2.88	3.00	
		V_{DD} falling	2.66	2.78	2.90	
V_{PVD6}(2)	PVD threshold 6	V_{DD} rising	2.83	2.96	3.08	
		V_{DD} falling	2.76	2.88	3.00	
V_{hyst_BOR0}(2)	BOR0 hysteresis voltage	-	-	20	-	mV
$V_{hyst_BOR_PVD}$(2)	BOR1, 2, 3, 4 and PVD hysteresis voltage	-	-	80	-	
$t_{sampling_BOR0}$(2)	BOR0 ultra-low power sampling monitoring period	ULPEN = 1	-	12	30	ms
$I_{DD_BOR_PVD}$(1)	BOR1, 2, 3, 4 and PVD consumption from V_{DD}, and additional BOR0 consumption for ULPMEN = 0 vs. ULPMEN = 1 (3)	-	-	1.7	2.5	µA

1. Specified by design, not tested in production.

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2. Evaluated by characterization, not tested in production.
3. BOR0 is enabled in all modes, its consumption is therefore included in the supply current characteristics tables.

5.3.6 Embedded voltage reference

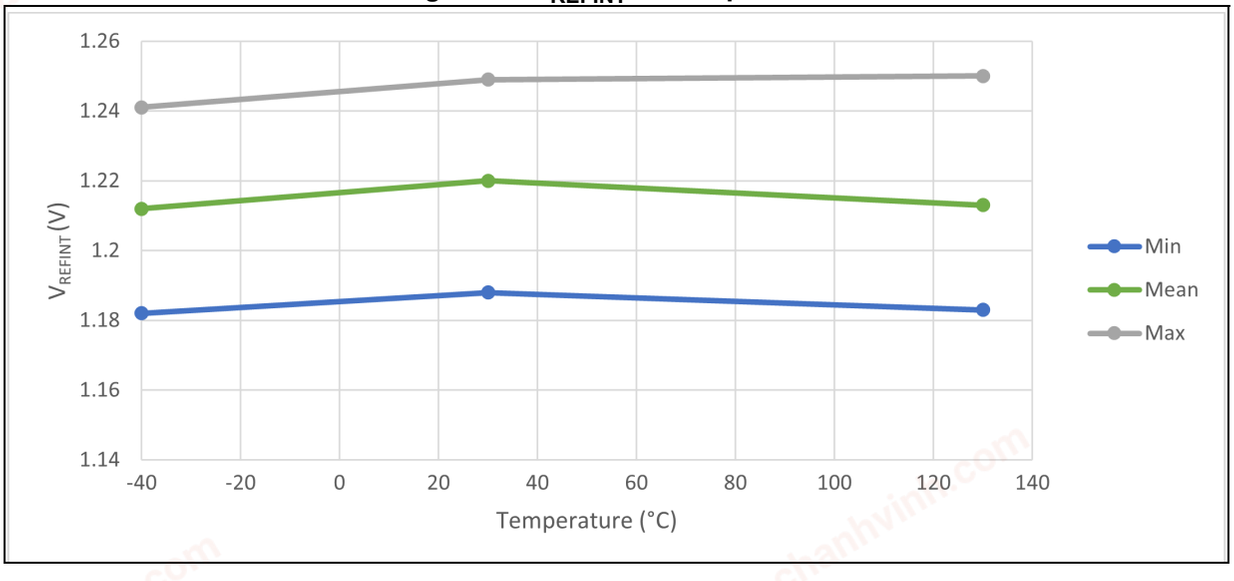
The parameters in *Table 35* are derived under ambient temperature and supply voltage conditions summarized in *Table 26*.

Table 35. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltage	Range 1	1.175	1.209	1.243	V
		Range 2 and low power modes	1.170	1.206	1.248	
$t_{S_vrefint}$(2)	ADC sampling time when reading the internal reference voltage(3)	-	11.25	-	-	µs
$t_{start_vrefint}$(2)	Start time of reference voltage buffer when ADC is enabled	-	-	4	6	
ΔV_{REFINT}(4)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V, –40 °C ≤ T_J ≤ +130 °C	-	8.2	-	mV
T_{Coeff}(4)	Temperature coefficient	–40 °C ≤ T_J ≤ +130 °C	-	40	-	ppm/°C
A_{Coeff}(2)	Long term stability	1000 hours, T = 25 °C	-	400	-	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	3.0 V ≤ V_{DD} ≤ 3.6 V	-	500	-	ppm/V

1. V_{REFINT} does not take into account package and soldering effects.
2. Specified by design, not tested in production.
3. The shortest sampling time can be determined in the application by multiple iterations.
4. Evaluated by characterization, not tested in production.

Figure 11. V_{REFINT} vs. temperature



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5.3.7 Supply current characteristics

The current consumption is measured as described in *Section 5.1.7*. It depends upon several parameters, such as operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequency, I/O pin switching rate, program location in memory, and executed binary code.

Typical and maximum current consumption

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled, except when otherwise mentioned
- The flash memory and SRAM access time is adjusted with the minimum wait states number, depending upon the f_{HCLK} frequency (refer to tables in the reference manual).
- When the peripherals are enabled $f_{PCLKx} = f_{HCLK1}$
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Voltage range 1 for 16 MHz < f_{HCLK1} ≤ 100 MHz and 12 MHz < f_{HCLK5} ≤ 32 MHz
  - Voltage range 2 for f_{HCLK1} ≤ 16 MHz and f_{HCLK5} ≤ 12 MHz

The parameters given in tables *36* to *38* are evaluated by characterization under ambient temperature and supply voltage conditions summarized in *Table 26*.

Table 36. Current consumption in Run modes, code with data processing running from flash memory, Cache ON (1-way), prefetch OFF, V_{DD} = 3.3 V(1)(2)(3)

Symbol	Parameter	Conditions			Typ			Unit
		-	Voltage scaling	f_{HCLK1}	25 °C	55 °C	85 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK1} = f_{HSI16}$ = 16 MHz	Range 2	16 MHz	0.91	0.95	1.10	mA
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz	Range 1	32 MHz	2.29	2.41	2.73	
		f_{HCLK1} = HSE32 + PLL > 32 MHz		100 MHz	6.16	6.30	6.63	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Reduced code used for characterization.
3. All peripherals disabled, SRAM1 and SRAM2 enabled.

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Table 37. Current consumption in Run mode, with different codes running from flash memory, Cache ON (2-way), Prefetch OFF(1)

Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
					25 °C				25 °C			
		-	Voltage scaling	Code	1.8 V	3.0 V	3.3 V		1.8 V	3.0 V	3.3 V	
I_{DD} (Run)	Supply current in Run mode	All peripherals disabled, SRAM1 and SRAM2 enabled	Range 2, $f_{HCLK1} = f_{HSI16}$ = 16 MHz	Reduced code	0.96	0.96	0.96	mA	59.7	59.7	59.8	µA/MHz
				Coremark®	0.96	0.96	0.96		60.2	60.2	60.2	
				SecureMark	1.00	1.00	1.01		62.8	62.8	62.8	
				Dhrystone 2.1	1.03	1.03	1.03		64.1	64.1	64.2	
				Fibonacci	0.86	0.86	0.86		53.7	53.7	53.7	
				While(1)	0.67	0.67	0.67		41.8	41.8	41.8	
			Range 1, $f_{HCLK1} = f_{HSE32}$ = 32 MHz	Reduced code	2.25	2.37	2.41		70.3	74.2	75.2	
				Coremark®	2.26	2.39	2.42		70.6	74.6	75.6	
				SecureMark	2.40	2.52	2.56		74.9	78.8	79.8	
				Dhrystone 2.1	2.42	2.55	2.58		75.7	79.6	80.7	
				Fibonacci	2.06	2.18	2.22		64.3	68.2	69.2	
				While(1)	1.64	1.77	1.80		51.3	55.3	56.3	
			Range 1, f_{HCLK1} = HSE32 + PLL at 100 MHz	Reduced code	6.37	6.49	6.52		63.7	64.9	65.2	
				Coremark®	6.41	6.53	6.56		64.1	65.3	65.6	
				SecureMark	6.73	6.86	6.89		67.3	68.6	68.9	
				Dhrystone 2.1	6.92	7.04	7.07		69.2	70.4	70.7	
				Fibonacci	5.85	5.97	6.01		58.5	59.7	60.1	
				While(1)	4.45	4.58	4.61		44.5	45.8	46.1	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

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Table 38. Current consumption in Sleep mode, flash memory in power-down(1)(2)

Symbol	Parameter	Conditions			Typ			Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	
I_{DD} (Sleep)	Supply current in Sleep mode	$f_{HCLK1} = f_{HSI16}$ = 16 MHz	Range 2	16 MHz	0.34	0.38	0.52	mA
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz	Range 1	32 MHz	0.95	1.06	1.36	
		f_{HCLK1} = HSE32 + PLL > 32 MHz		100 MHz	2.14	2.25	2.56	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. All peripherals disabled.

Table 39. Flash memory static power consumption(1)

Symbol	Parameter	Conditions	Typ			Unit
			25 °C	55 °C	85 °C	
I_{DD} (Flash)	Static consumption in normal mode	PD = 1 versus PD = 0	44.6	48.5	59.0	µA
I_{DD} (Flash_LPM)	Additional static consumption in normal versus low-power mode	LPM = 1 versus LPM = 0	25.2	26.2	28.7	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 40. Current consumption in Stop 0 mode(1)

Symbol	Parameter	Conditions		Typ			Unit
		-	V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Stop\ 0)}$	Supply current in Stop 0 mode, SRAM2 + CACHE retained	Range 2	1.8 V	48	79	181	µA
			2.4 V	48	79	180	
			3.0 V	49	80	182	
			3.3 V	49	82	186	
			3.6 V	50	82	197	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 41. Current consumption in Stop 1 mode(1)

Symbol	Parameter	Condition	Typ			Unit
		V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Stop\ 1)}$	Supply current in Stop 1 mode, SRAM1 retained, ULPMEN = 1	1.8 V	20.2	49.0	134.5	µA
		2.4 V	22.1	50.3	133.9	
		3.0 V	20.5	51.3	135.7	
		3.3 V	22.6	53.7	136.0	
		3.6 V	20.9	56.0	152.5	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

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Table 42. Current consumption in Standby retention mode(1)

Symbol	Parameter		Condition	Typ			Unit
			V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Standby)}$	Supply current in Standby mode, SRAM1 retained, ULPMEN = 1	Standby retention mode	1.8 V	2.25	4.85	14.8	µA
			2.4 V	2.40	5.41	15.1	
			3.0 V	2.39	5.66	15.5	
			3.3 V	2.58	5.51	16.2	
			3.6 V	2.76	8.52	17.6	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 43. Current consumption in Standby mode(1)

Symbol	Parameter	Conditions		Typ			Unit
		-	V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Standby)}$	Supply current in Standby mode, all peripherals disabled	ULPMEN = 1	1.8 V	0.16	0.58	3.02	µA
			2.4 V	0.18	0.64	3.29	
			3.0 V	0.24	0.79	3.81	
			3.3 V	0.37	1.06	4.50	
			3.6 V	0.71	1.69	5.93	
		ULPMEN = 0	1.8 V	1.26	1.71	4.05	
			2.4 V	1.61	2.07	4.57	
			3.0 V	2.00	2.54	5.34	
			3.3 V	2.29	2.96	6.18	
			3.6 V	2.81	3.77	7.71	
	Supply current in Standby mode, IWDG enabled	Clocked by LSI1, ULPMEN = 0	1.8 V	1.44	1.82	3.74	
			2.4 V	1.81	2.22	4.25	
			3.0 V	2.24	2.71	4.99	
			3.3 V	2.55	3.14	5.78	
			3.6 V	3.07	3.91	7.18	
		Clocked by LSI1 / 128, ULPMEN = 0	1.8 V	1.37	1.74	3.67	
			2.4 V	1.71	2.12	4.13	
			3.0 V	2.10	2.58	4.85	
			3.3 V	2.40	2.98	5.61	
			3.6 V	2.89	3.73	7.01	

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Table 43. Current consumption in Standby mode(1) (continued)

Symbol	Parameter	Conditions		Typ			Unit
		-	V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Standby with RTC)}$	Supply current in Standby mode, no IWDG, RTC enabled	Clocked by LSI1, ULPMEN = 0	1.8 V	1.48	1.85	3.78	µA
			2.4 V	1.87	2.27	4.30	
			3.0 V	2.31	2.78	5.06	
			3.3 V	2.64	3.22	5.86	
			3.6 V	3.17	4.02	7.27	
		Clocked by LSI1 / 128, ULPMEN = 0	1.8 V	1.36	1.74	3.67	
			2.4 V	1.71	2.12	4.15	
			3.0 V	2.11	2.58	4.85	
			3.3 V	2.40	2.98	5.61	
			3.6 V	2.90	3.75	7.02	
		Clocked by LSE bypass 32.768 kHz, ULPMEN = 0	1.8 V	1.51	1.89	4.03	
			2.4 V	1.91	2.32	4.55	
			3.0 V	2.36	2.84	5.36	
			3.3 V	2.70	3.28	6.16	
			3.6 V	3.24	4.06	7.61	
		Clocked by LSE crystal 32.768 kHz in medium low-drive, ULPMEN = 0	1.8 V	1.66	1.98	3.43	
			2.4 V	2.03	2.37	3.90	
			3.0 V	2.45	2.89	4.77	
			3.3 V	2.76	3.32	5.54	
			3.6 V	3.29	4.06	6.84	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up or pull-down generate current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Section 5.3.16*.

For the output pins, any internal or external pull-up or pull-down and external load must also be considered to estimate the current consumption.

An additional current consumption is due to I/Os configured as inputs when an intermediate voltage level is applied externally. This is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is the case of ADC input pins, which must be configured as analog inputs.

Caution: Any floating input pin can settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must be configured in analog mode, or forced internally to a definite digital value. This can be done by using pull-up/down resistors, or by configuring the pins in output mode.

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I/O dynamic current consumption

The I/Os used in application increase the consumption measured previously (see *Table 44*). When an I/O pin switches, it uses the current from the I/O supply voltage to supply the pin circuitry, and to charge/discharge the capacitive load (internal and external) connected to it:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where:

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the I/O supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$
  - C_{INT} is the I/O pin capacitance
  - C_{EXT} is any connected external device pin capacitance
  - C_S is the PCB board capacitance

The pin is configured in push-pull output mode, and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The power consumption of the digital part of the peripherals is given in *Table 44*of the analog part (when applicable) is indicated in the related sections.

The MCU is put under the following conditions:

- All I/O pins are in analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- The ambient operating temperature and supply voltage conditions summarized in *Table 26*

Table 44. Peripheral typical dynamic current consumption(1)

Bus	Peripheral	Range 1	Range 2	Unit
AHB1	AHB1 bus	0.27	0.19	µA/MHz
	SRAM1	0.29	0.22	
	TSC	1.25	0.92	
	CRC	0.30	0.22	
	RAMCFG	0.22	0.17	
	GPDMA1	1.48	1.10	
	ICACHE	0.46	0.34	
	FLASH interface	1.70	1.26	

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Table 44. Peripheral typical dynamic current consumption(1) (continued)

Bus	Peripheral	Range 1	Range 2	Unit
AHB2	AHB2 bus(2)	0.27	0.18	µA/MHz
	SRAM2	0.34	0.26	
	PKA	4.91	3.63	
	HSEM	0.08	0.07	
	RNG	0.88	0.69	
	HASH	1.47	1.11	
	AES	1.77	1.34	
	GPIOA	0.05	0.06	
	GPIOB	0.06	0.06	
	GPIOC	0.03	0.05	
	GPIOH	0.02	0.05	
AHB4	AHB4 bus	0.00	0.03	µA/MHz
	ADC4 kernel clock domain	1.60	1.17	
	ADC4 bus clock domain	2.76	2.03	
	PWR	0.04	0.02	
AHB5	AHB5 bus + peripherals(3)	0.07	0.05	µA/MHz
APB1	AHB to APB1(4)	0.00	0.00	µA/MHz
	TIM2	3.00	2.22	
	WWDG	0.21	0.16	
APB2	AHB to APB2(4)	0.62	0.46	µA/MHz
	TIM1	4.67	3.45	
	TIM16	1.63	1.22	
	USART1 kernel clock domain	3.21	2.39	
	USART1 bus clock domain	4.66	3.45	
APB7	AHB to APB7(4)	0.27	0.22	µA/MHz
	SYSCFG	0.32	0.24	
	SPI3 kernel clock domain	1.01	0.74	
	SPI3 bus clock domain	2.32	1.71	
	LPUART1 kernel clock domain	2.79	2.05	
	LPUART1 bus clock domain	3.97	2.94	
	I2C3 kernel clock domain	1.78	1.32	
	I2C3 bus clock domain	2.52	1.86	
	LPTIM1 kernel clock domain	4.40	3.26	
	LPTIM1 bus clock domain	5.33	3.96	
	RTC/TAMP	1.81	1.34	

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1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. The AHB bus is automatically active when at least one peripheral is ON on the AHB or associated APB.
3. RADIO inactive.
4. The AHB to APB bridge is automatically active when at least one peripheral is ON on the APB.

5.3.8 Wake-up time from low-power modes and voltage scaling transition times

The times given in *Table 45* are the latency between the event and the execution of the first user instruction (FSTEN = 1 in PWR_CR3 if not mentioned differently).

The device goes in Low-power mode after the WFE (Wait For Event) instruction.

Table 45. Low-power mode wake-up timings(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WU(Sleep)}$	Wake-up time from Sleep to Run mode	SLEEP_PD = 0	14	17	CPU clock cycles
$t_{WU(Stop\ 0)}$	Wake-up time from Stop 0 to Run mode in flash memory	FLASHFWU = 0	9.98	-	µs
	Wake-up time from Stop 0 to Run mode in SRAM2		10.36	-	
$t_{WU(Stop\ 1)}$	Wake-up time from Stop 1 to Run mode in flash memory	FLASHFWU = 0	24.10	-	
	Wake-up time from Stop 1 to Run mode in SRAM2		24.66	-	
$t_{WU(Standby\ with\ Retention)}$	Wake-up time from Standby retention to Run mode in flash memory	FLASHFWU = 0	48.5	-	
	Wake-up time from Standby retention to Run mode in SRAM2		48.5	-	
$t_{WU(Standby)}$	Wake-up time from Standby to Run mode in flash memory	FSTEN = 1	101.6	-	
		FSTEN = 0	553.4	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 46. Wake-up time using USART/LPUART(1)

Symbol	Parameter	Typ	Max	Unit
,$t_{WUUSART}$ $t_{WULPUART}$	Wake-up time needed to calculate the maximum USART/LPUART baudrate needed to wake up from Stop mode when USART/LPUART kernel clock source is HSI16	-	$t_{su(HSI16)}$ max	µs

1. Specified by design, not tested in production.

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5.3.9 External clock source characteristics

High-speed external clock

The high-speed external (HSE32) clock can be supplied with a 32 MHz crystal or a clock source.

The devices include internal programmable capacitances that can be used to trim the crystal frequency, to compensate the PCB parasitic one.

Table 47. HSE32 crystal requirements(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSE}	Oscillator frequency(2)	-		-	32	-	MHz
f_{TOL}	Frequency tolerance(3)	Includes initial accuracy, stability over temperature, aging, and frequency pulling due to incorrect load capacitance	Bluetooth Low Energy	-50	-	50	ppm
C_L	Load capacitance	-		8	-	18	pF
C_O	Shunt capacitance	-		-	-	4	
ESR	Equivalent series resistance	-		60	-	150	Ω
C_{bank}	Capacitor bank range	-		6.6	-	23.6	pF
$C_{bank-step}$	Capacitor bank step size	-		215	270	325	fF
t_{STAB}	Oscillator stabilization time	-		-	100	160	µs
$I_{DDRF(HSE32)}$	Current consumption	-		-	205	-	µA

1. Specified by design, not tested in production.
2. 32 MHz XTAL is specified for two specific references: NX2016SA and NX1612SA.
3. After capacitor bank trimming.

Table 48. HSE32 clock source requirements(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE32}	External clock source frequency(2)	-	-	32	-	MHz
V_{HSE32}	Clock input voltage limits	Input level	0	-	0.9	V
		Amplitude(3)	200	-	900	mV_{PP}
$DuCy_{HSE32}$	Duty cycle	-	45	-	55	%
$\varphi_{n(HSE32)}$	Phase noise for 32 MHz	Offset = 10 kHz	-	-	-127	dBc/Hz
		Offset = 100 kHz	-	-	-135	
		Offset = 1 MHz	-	-	-138	

1. Specified by design, not tested in production.
2. $f_{HSE} = 1 / t_{HSE}$.
3. AC coupling is supported (capacitor 470 pF to 100 nF).

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Note: For information about oscillator trimming, refer to AN5042 "Precise HSE frequency and startup time tuning for STM32 wireless MCUs", available on www.st.com.

Low-speed external clock

The low-speed external (LSE) clock can be supplied with a crystal or a clock source. The information provided in this section is based on design simulation results, obtained with the typical external components specified in *Table 49*. In the application, the crystal and the load capacitors must be placed as close as possible to the oscillator pins, to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

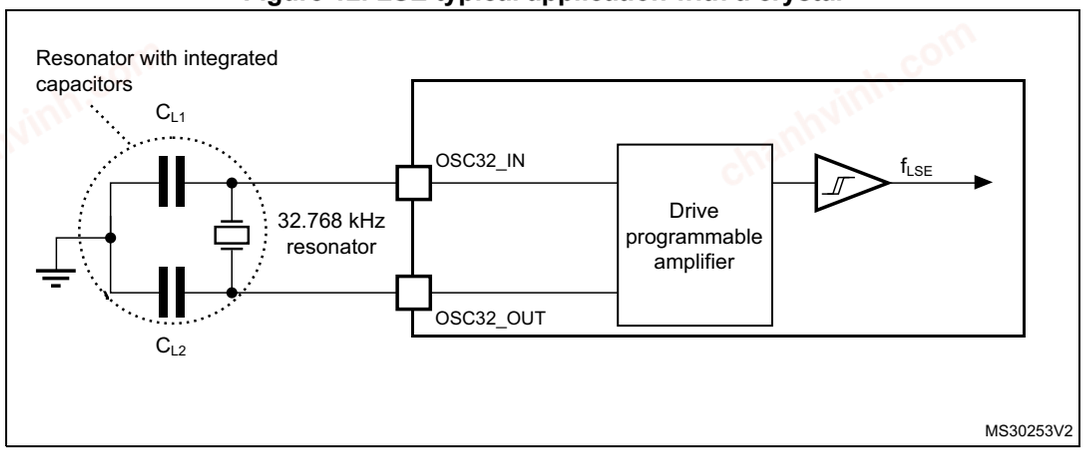
Table 49. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{LSE}	Oscillator frequency(2)	-		-	32.000 or 32.768	-	kHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance	Bluetooth Low Energy	-500	-	500	ppm
$I_{DD(LSE)}$	LSE current consumption	LSEDRV = medium-low drive capability		-	450	-	nA
		LSEDRV = medium-high drive capability		-	590	-	
		LSEDRV = high drive capability		-	700	-	
$Gm_{critmax}$	Maximum critical crystal Gm	LSEDRV = medium-low drive capability		-	-	0.75	µA/V
		LSEDRV = medium-high drive capability		-	-	1.70	
		LSEDRV = high drive capability		-	-	2.70	
C_{S_PARA}	Internal stray parasitic capacitance(3)	-		-	3	-	pF
$t_{SU(LSE)}$	Startup time(4)	V_{DD} is stabilized		-	2	-	s

1. Specified by design, not tested in production.
2. For information on selecting the crystal, refer to AN2867 '*Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs*".
3. CS_PARA is the equivalent capacitance seen by the crystal due to OSC32_IN and OSC32_OUT internal parasitic capacitances.
4. Time measured from when the LSE is enabled by software, until a stable LSE oscillation is reached. This value is measured for a standard crystal, and can vary significantly with the crystal used.

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Figure 12. LSE typical application with a crystal



Note: No external resistors are required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

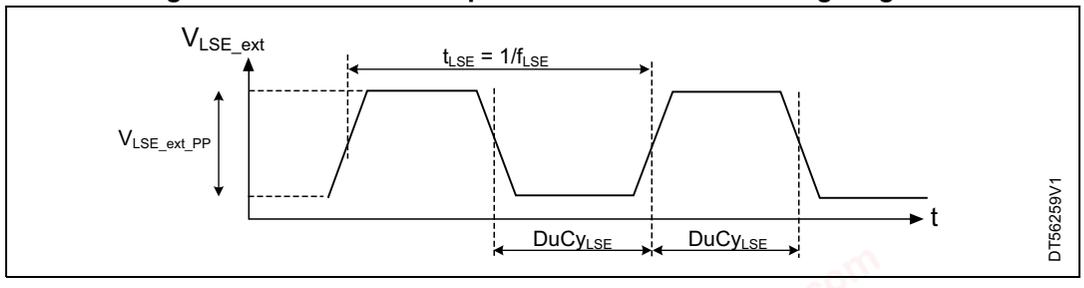
Table 50. LSE clock source requirements(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{LSE}	External clock source frequency(2)	-		32.000	32.768	-	kHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, and aging	Bluetooth Low Energy	-500	-	500	ppm
V_{LSE_ext}	Clock input voltage range	-		0	-	V_{DD}	V
$V_{LSE_ext_PP}$	Clock input peak-to-peak amplitude(3)	-		0.3	-	V_{DD}	V
$DuCy_{LSE}$	Duty cycle	-		40	-	60	%

1. Specified by design, not tested in production.
2. $f_{LSE} = 1/t_{LSE}$.
3. AC coupled is supported (10 pF capacitor).

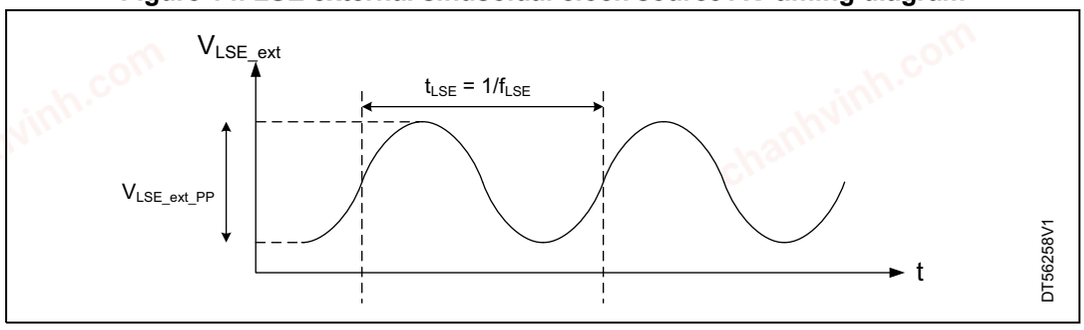
The clock input waveforms are shown in *Figure 13* and *Figure 14*.

Figure 13. LSE external square clock source AC timing diagram



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Figure 14. LSE external sinusoidal clock source AC timing diagram



In bypass mode the LSE oscillator is switched off, and the input pin OSC32_IN is a standard GPIO.

Table 51. LSE external clock bypass mode characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(2)	-		32.000	32.768	-	kHz
f_{TOL}	Frequency tolerance	Includes initial accuracy and stability over temperature	Bluetooth Low Energy	-500	-	500	ppm
V_{IL}	OSC32_IN input low level voltage	-		-	-	0.3 x V_{DD}	V
V_{IH}	OSC32_IN input high level voltage	-		0.7 x V_{DD}	-	-	V
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN input high or low time for square signal	-		10	-	-	µs

1. Specified by design, not tested in production.
2. $f_{LSE} = 1/t_{LSE}$.

5.3.10 Internal clock source characteristics

The parameters given in the following tables are derived under ambient operating temperature and supply voltage conditions summarized in *Table 26*.

High-speed internal (HSI16) RC oscillator

Table 52. HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency after factory calibration	V_{DD} = 3.0 V, T_J = 30 °C calibrated during production	15.92	16	16.08	MHz
		1.71 V ≤ V_{DD} ≤ 3.6 V, T_J = -10 to 100 °C(1)	15.84	16	16.16	
		1.71 V ≤ V_{DD} ≤ 3.6 V, T_J = -40 to 130 °C (1)	15.65	16	16.35	

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Table 52. HSI16 oscillator characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TRIM(2)	User trimming step	-	18	29	40	kHz
$DuCy_{HSI16}$(2)	Duty cycle	-	45	-	55	%
$t_{su(HSI16)}$(2)	Startup time	-	-	2.5	3.6	µs
$t_{stab(HSI16)}$(2)	Stabilization time	-	-	4	6	
$I_{DD(HSI16)}$(2)	Power consumption	-	-	150	210	µA

1. Evaluated by characterization, not tested in production, unless otherwise specified. It does not take into account package and soldering effects.
2. Specified by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 53. LSI1 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI1}	Frequency	V_{DD} = 3.0 V, T_J = 30 °C, LSIPREDIV = 1	0.245	0.25	0.255	kHz
		V_{DD} = 3.0 V, T_J = 30 °C, LSIPREDIV = 0	31.4	32.0	32.6	
		1.71 V ≤ V_{DD} ≤ 3.6 V, T_J = -40 to 85 °C, LSIPREDIV = 0 (1)	30.4	32.0	33.6	
$DuCy_{LSI1}$	Duty cycle	LSIPREDIV = 1	-	50	-	%
$t_{SU(LSI1)}$(2)	Startup time	-	-	230	260	µs
$t_{STAB(LSI1)}$(2)	Stabilization time	5% of final frequency	-	230	260	
$I_{DD(LSI1)}$(2)	Power consumption	LSIPREDIV = 0	-	140	255	nA
		LSIPREDIV = 1	-	130	240	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Specified by design, not tested in production.

5.3.11 PLL characteristics

The parameters given in *Table 54* are derived from tests performed at ambient temperature and under the supply voltage conditions summarized in *Table 26*.

Table 54. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}(1)	PLL input clock	-	4	-	16	MHz
$DuCy_{PLL_IN}$(1)	PLL input clock duty cycle	-	10	-	90	%
f_{PLL_OUT}(1)	PLL output clock P, Q, and R	-	1	-	100	MHz
$DuCy_{PLL_OUT}$(1)	PLL output clock duty cycle	Division 1	40	-	60	%
f_{VCO_OUT}(1)	PLL VCO output	-	128	-	544	MHz

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Table 54. PLL characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LOCK}(2)	PLL lock time(3)	Integer mode	-	25	54	µs
		Fractional mode	-	40	65	
Jitter(1)	RMS cycle-to-cycle jitter	Integer mode, VCO = 544 MHz	-	±20	-	ps
		Fractional mode, VCO = 544 MHz	-	±70	-	
	RMS period jitter	Integer mode, VCO = 544 MHz	-	±35	-	
		Fractional mode, VCO = 544 MHz	-	±45	-	
	Long-term jitter(4) f_{PLL_IN} = 8 MHz	Integer mode, VCO = 544 MHz	-	±160	-	
		Fractional mode, VCO = 544 MHz	-	±170	-	
$I_{DD(PLL)}$(1)	PLL power consumption on V_{DD}	VCO freq = 100 MHz	-	370	-	µA
		VCO freq = 200 MHz	-	460	-	
		VCO freq = 336 MHz	-	710	-	
		VCO freq = 544 MHz	-	1100	-	

1. Specified by design, not tested in production.
2. Evaluated by characterization, not tested in production, unless otherwise specified.
3. Lock time is the duration until PLL1RDY flag (2% of final frequency).
4. Measured on 5000 cycles.

5.3.12 Flash memory characteristics

Table 55. Flash memory characteristics

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}(2)	128-bit programming time	Normal mode	118	118	µs
		Burst mode	48	48	
t_{prog_page}(2)	One 8-Kbyte page programming time	f_{AHB} = 100 MHz, normal mode	62.0	-	ms
		f_{AHB} = 100 MHz, burst mode	24.9	-	
t_{prog_flash}(2)	1-Mbyte programming time	f_{AHB} = 100 MHz, normal mode	7926	-	
		f_{AHB} = 100 MHz, burst mode	3184	-	
t_{ERASE}(2)	One 8-Kbyte page erase time	10 k endurance cycles	1.5	2.4	
		100 k endurance cycles(3)	1.7	3.4	
t_{ME}(2)	Mass erase time	10 k endurance cycles	195	308	
I_{DD}(4)	Average consumption from V_{DD}	Write mode	2.1	-	mA
		Erase mode	1.3	-	
	Maximum current (peak) from V_{DD}	Write mode	2.6	-	
		Erase mode	3.0	-	

1. Evaluated by characterization after cycling, not tested in production.
2. Specified by design, not tested in production, unless otherwise specified.

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3. Erase time applies to all pages in user area in flash main memory (only 32 pages can be cycled more than 10 k times)
4. Evaluated by characterization, not tested in production, unless otherwise specified.

5.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs as follows:

- ESD (electrostatic discharge), positive and negative: applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB (fast transient voltage burst), positive and negative: applied to V_{DD} and V_{SS} pins through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 56*. They are based on the EMS levels and classes defined in AN1709 "*EMC design guide for STM8, STM32 and legacy MCUs*".

Table 56. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to apply on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK1} = 100 MHz, UFQFPN48 conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to apply through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK1} = 100 MHz, UFQFPN48 conforming to IEC 61000-4-4	5A

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software.

Good EMC performance is highly dependent on the user application, and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the requested EMC level.

Software recommendations

The software flow must include the management of runaway conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers)

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Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or on the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specified values. When an unexpected behavior is detected, the software can be hardened to prevent the occurrence of unrecoverable errors. See AN1015 "*Software techniques for improving microcontrollers EMC performance*" for more details.

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with the IEC 61967-2 standard, which specifies the test board and the pin loading.

Table 57. EMI characteristics for f_{HSE} = 32 MHz and f_{HCLK} = 100 MHz(1)

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak level(2)	V_{DD} = 3.6 V, T_A = 25 °C, UFQFPN48 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	23	dBµV
			30 MHz to 130 MHz	11	
			130 MHz to 1 GHz	13	
			1 GHz to 2 GHz	15	
	Level(3)		EMI level	3.5	-

1. Evaluated by characterization, not tested in production.
2. Refer to AN1709, "EMI radiated test" section.
3. Refer to AN1709, "EMI level classification" section.

5.3.14 Electrical sensitivity characteristics

Based on three different tests (ESD, latch-up) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 58. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions	Package	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to ANSI/ESDA/JEDEC JS-001	UFQFPN32	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to ANSI/ESDA/JEDEC JS-002		C2A	500	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

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Static latch-up

The following complementary static tests are required on three parts to assess the latch-up performance:

- a supply overvoltage is applied to each power supply pin
- a current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 59. Electrical sensitivity(1)

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_J = 130 °C conforming to JESD78E	2

1. Evaluated by characterization, not tested in production, unless otherwise specified.

5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller if abnormal injection accidentally happens, some susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter, such as an ADC error above a certain limit (higher than 5 LSB ET), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA / 0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 60*. The negative/positive induced leakage current is caused by the negative/positive injection.

Table 60. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins	5	N/A	mA

1. Evaluated by characterization, not tested in production, unless otherwise specified.

5.3.16 I/O port characteristics

General input/output characteristics

The parameters given in *Table 61* are derived from tests performed at ambient temperature and under the supply voltage conditions summarized in *Table 26*. All I/Os are designed as CMOS- and TTL-compliant.

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Note: For information on I/O configuration, refer to AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption”.

Table 61. I/O static characteristics

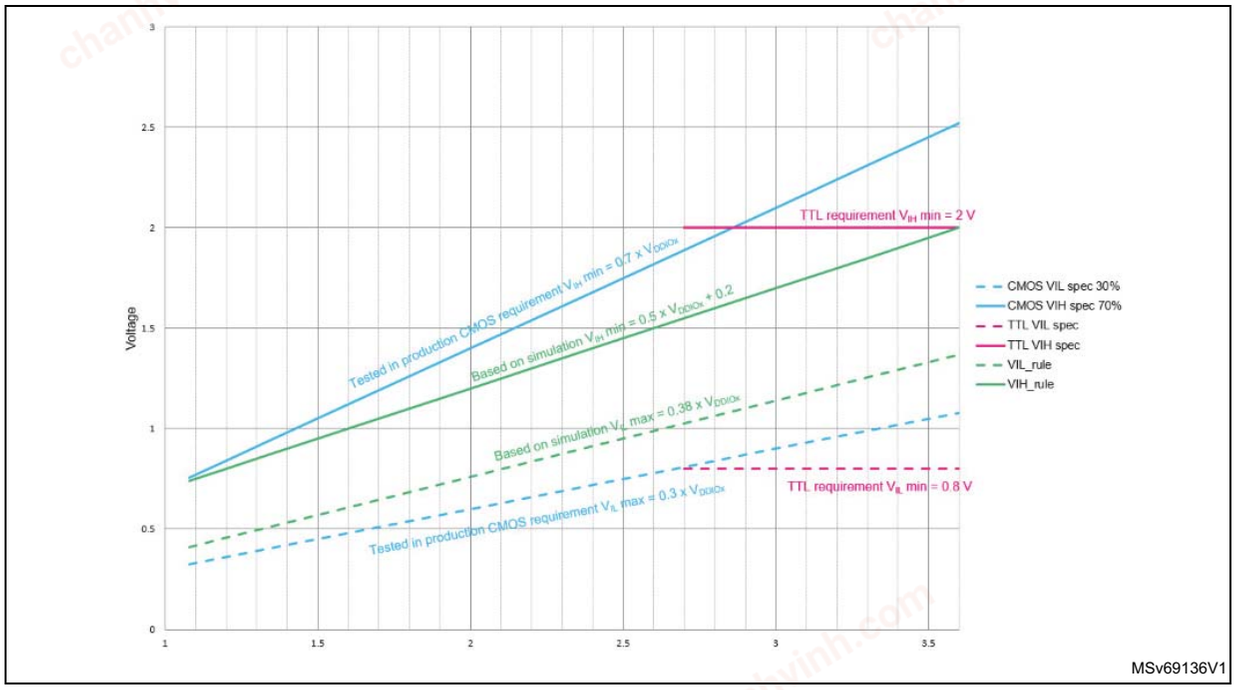
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage	1.58 V ≤ V_{DD} ≤ 3.6 V	-	-	0.3 x V_{DD}	V
V_{IH}	I/O input high level voltage		0.7 x V_{DD}	-	-	
V_{hys}(1)	Input hysteresis	-	-	250	-	mV
I_{lkg}(1)	I/O input leakage current(2)(3)	V_{IN} ≤ Max(V_{DD}, V_{DDA})	-	-	150	nA
		Max(V_{DD}, V_{DDA}) < V_{IN} ≤ Max(V_{DD}, V_{DDA}) + 1 V	-	-	2000	
		Max(V_{DD}, V_{DDA}) + 1 V < V_{IN} ≤ 5.5 V	-	-	500	
R_{PU}	Weak pull-up equivalent resistor(4)	-	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	-	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Specified by design, not tested in production.
2. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_Ileak_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x I_{lkg} max.
3. To sustain a voltage higher than Min (V_{DD}, V_{DDA}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled.
4. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10%).

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All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 15*.

Figure 15. I/O input characteristics (all I/Os except PH3)



Output driving current

The I/Os can sink or source up to ±8 mA, up to ±20 mA with a relaxed V_{OL} / V_{OH}.

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*.

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 23*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 23*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 62* are at ambient temperature and under the supply voltage conditions summarized in *Table 26*. All I/Os are CMOS- and TTL-compliant.

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Table 62. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage	$\|I_{IO}\|$ = 8 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage		V_{DD} - 0.4	-	
V_{OL}(2)	Output low level voltage	$\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}(2)	Output high level voltage		V_{DD} - 1.3	-	
V_{OL}(2)	Output low level voltage	$\|I_{IO}\|$ = 4 mA, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(2)	Output high level voltage		V_{DD} - 0.4	-	
V_{OLFM+}(2)	Output low level voltage for an I/O pin in Fm+ mode	$\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		$\|I_{IO}\|$ = 10 mA, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 22*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\Sigma I_{(PIN)}$.
2. Specified by design, not tested in production.

Output AC characteristics

Unless otherwise specified, the parameters given in *Table 63* are at ambient temperature and under the supply voltage conditions summarized in *Table 26*.

The definition and values of output AC characteristics are given, respectively, in *Figure 16* and in *Table 63*.

Table 63. Output AC characteristics(1)(2)

Speed(3)	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C_L = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.5	MHz
			C_L = 50 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	5	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.5	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	5	
	t_r/t_f	Output rise and fall time	C_L = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17	ns
			C_L = 50 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	33	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.5	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	25	
01	Fmax	Maximum frequency	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	MHz
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	12.5	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	12.5	
	t_r/t_f	Output rise and fall time	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.8	ns
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	10	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.2	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	7.5	

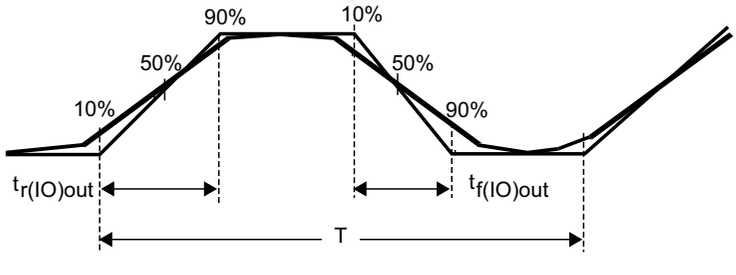
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Table 63. Output AC characteristics(1)(2) (continued)

Speed(3)	Symbol	Parameter	Conditions	Min	Max	Unit
10(4)	Fmax	Maximum frequency	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	MHz
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	33	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	40	
	t_r/t_f	Output rise and fall time	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	6.0	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.0	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	4.1	
Fm+	Fmax	Maximum frequency	C_L = 550 pF, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	1	MHz
	t_f	Output fall time(5)	C_L = 550 pF, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	100	ns
			C_L = 100 pF, 1.58 V ≤ V_{DD} < 3.6 V	-	50	

1. Specified by design, not tested in production.
2. PB15 and PH3 output and input frequency must not exceed 16 kHz, PC14 and PC15 output and input frequency must not exceed 250 kHz, for these IOs OSPEED must be kept at low speed.
3. The I/O speed is configured using the OSPEED bits, Fm+ is configured in SYSCFG. Refer to the product reference manual for the description.
4. I/O compensation system enabled.
5. The fall time is defined between 70% and 30% of the output waveform according to the I^2C specification.

Figure 16. Output AC characteristics definition



Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

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5.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in *Table 64* are at ambient temperature and under the supply voltage conditions summarized in *Table 26*.

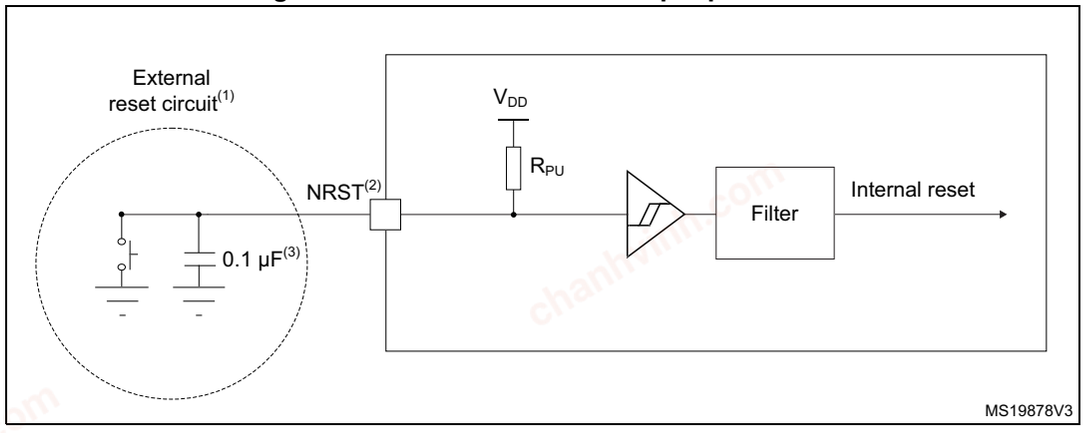
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Table 64. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	Input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	Input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(NRST)}$	Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$t_{F(NRST)}$	Input filtered pulse	-	-	-	50	ns
$t_{NF(NRST)}$	Input not-filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	330	-	-	
		1.58 V ≤ V_{DD} < 1.71 V	1000	-	-	

1. Specified by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS, whose contribution to the series resistance is minimal (~10%).

Figure 17. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ maximum level specified in *Table 64*, or the reset is not taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.18 Extended interrupt and event controller input (EXTI) characteristics

Pulses on the extended interrupt and event controller inputs must have a minimal length, to guarantee they are detected.

Table 65. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(EXTI)}$	Pulse length to event controller	-	20	-	-	ns

1. Specified by design, not tested in production.

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5.3.19 Wake-up pin (WKUP) characteristics

Pulses on the wake-up pin inputs must have a minimal length, to ensure their detection.

Table 66. WKUP input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(WKUP)}$	Pulse length to wake up	-	20	-	-	ns

1. Specified by design, not tested in production.

5.3.20 Analog switch booster

Table 67. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.6	1.8	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	-	-	125	µA

1. Specified by design, not tested in production.

5.3.21 12-bit Analog-to-Digital converter (ADC4) characteristics

Unless otherwise specified, the parameters given in the following tables are derived at ambient temperature, and under the f_{HCLK} frequency and supply voltage conditions summarized in *Table 26*.

Note: It is recommended to perform a calibration after each power-up.

Table 68. 12-bit ADC4 characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
f_{ADC}	ADC clock frequency	-	0.14	-	55	MHz
$DuCy_{ADC}$	ADC clock duty cycle	-	45	-	55	%
f_s	Sampling rate	Resolution 12 bits	0.01	-	2.75	Msps
		Resolution 10 bits	0.0120	-	3.05	
		Resolution 8 bits	0.0140	-	3.43	
		Resolution 6 bits	0.0175	-	3.92	
t_{TRIG}	External trigger period	Resolution 12 bits	16	-	-	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(4)	External input impedance	Resolution 12 bits, T_j = 130 °C	-	-	2.2	kΩ
		Resolution 10 bits, T_j = 130 °C	-	-	6.8	
		Resolution 8 bits, T_j = 130 °C	-	-	33.0	
		Resolution 6 bits, T_j = 130 °C	-	-	47.0	

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Table 68. 12-bit ADC4 characteristics (1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
$t_{ADCVREG_STUP}$	ADC voltage regulator startup time	-	-	-	25	µs
t_{STAB}	ADC power-up time	-	(3 x 1/f_{ADC}) + 1 conversion			cycle
t_{OFF_CAL}	Offset calibration time	-	82			1/f_{ADC}
t_{LATR}	Trigger conversion latency	WAIT = 0, AUTOFF = 0, DPD = 0, f_{ADC} = HCLK	4			
		WAIT = 0, AUTOFF = 1, DPD = 0, f_{ADC} = HCLK/2	4			
		WAIT = 0, AUTOFF = 1, DPD = 1, f_{ADC} = HCLK/4	3.75			
t_s	Sampling time	-	1.5	-	814.5	
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits, VREFPROTEN = 0	t_s + N + 0.5			
		Resolution = N bits, VREFPROTEN = 1, VREFSECSMP = 0	t_s + N + 0.5	-	t_s + N + 1.5	
		Resolution = N bits, VREFPROTEN = 1, VREFSECSMP = 1	t_s + N + 0.5	-	t_s + N + 2.5	
$I_{DDA(ADC)}$	ADC consumption on V_{DDA}	fs = 2.5 Msps	-	378	-	µA
		fs = 1 Msps	-	190	-	
		fs = 10 ksps	-	10	-	
		AUTOFF = 1, DPD = 0, no conversion	-	9	-	
		AUTOFF = 1, DPD = 1, no conversion	-	0.11	-	

1. Specified by design, not tested in production.
2. The voltage booster on the ADC switches must be used when V_{DDA} < 2.4 V (embedded I/O switches).
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. The tolerance is two LSBs.

Table 69. Maximum R_{AIN} for 12-bit ADC4(1) (2) (3)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
12 bits	47	276	12.5	19.5
	68	288		
	100	306		
	150	336		

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Table 69. Maximum R_{AIN} for 12-bit ADC4[1] [2] [3] (continued)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
12 bits (continued)	220	377	19.5	39.5
	330	442		
	470	526		
	680	650	39.5	
	1000	840		79.5
	1500	1134		
	2200	1643	79.5	814.5
	3300	2395	814.5	
	4700	3342		
	6800	4754		
	10000	6840		
	15000	9967		
	22000	14068		
	33000	19933		N/A
10 bits	47	86	3.5	7.5
	68	90		
	100	95		
	150	108	7.5	
	220	116		
	330	136		
	470	161		12.5
	680	212		
	1000	276	12.5	19.5
	1500	376	19.5	39.5
	2200	516		79.5
	3300	735	39.5	
	4700	1012		
	6800	1423	79.5	814.5
	10000	2040	814.5	814.5
	15000	2978		
	22000	4356		
	33000	6443		
	47000	8925		

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Table 69. Maximum R_{AIN} for 12-bit ADC4[1] [2] [3] (continued)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
8 bits	47	45	3.5	3.5
	68	46		
	100	48		
	150	53		
	220	59		
	330	69		7.5
	470	81		
	680	101	7.5	
	1000	130		
	1500	177		12.5
	2200	242	12.5	19.5
	3300	345		
	4700	475	19.5	39.5
	6800	670	39.5	
	10000	963		79.5
	15000	1417	79.5	
	22000	2040		814.5
	33000	2995	814.5	
	47000	4158		
6 bits	47	32	1.5	3.5
	68	32		
	100	33		
	150	35		
	220	37		
	330	41		
	470	49	3.5	
	680	61		
	1000	79		7.5
	1500	106	7.5	
	2200	146		12.5
	3300	207		
	4700	286	12.5	19.5
	6800	404	19.5	39.5
	10000	584	39.5	

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Table 69. Maximum R_{AIN} for 12-bit ADC4(1) (2) (3) (continued)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
6 bits (continued)	22000	1250	79.5	79.5
	33000	1853		814.5
	47000	2607	814.5	

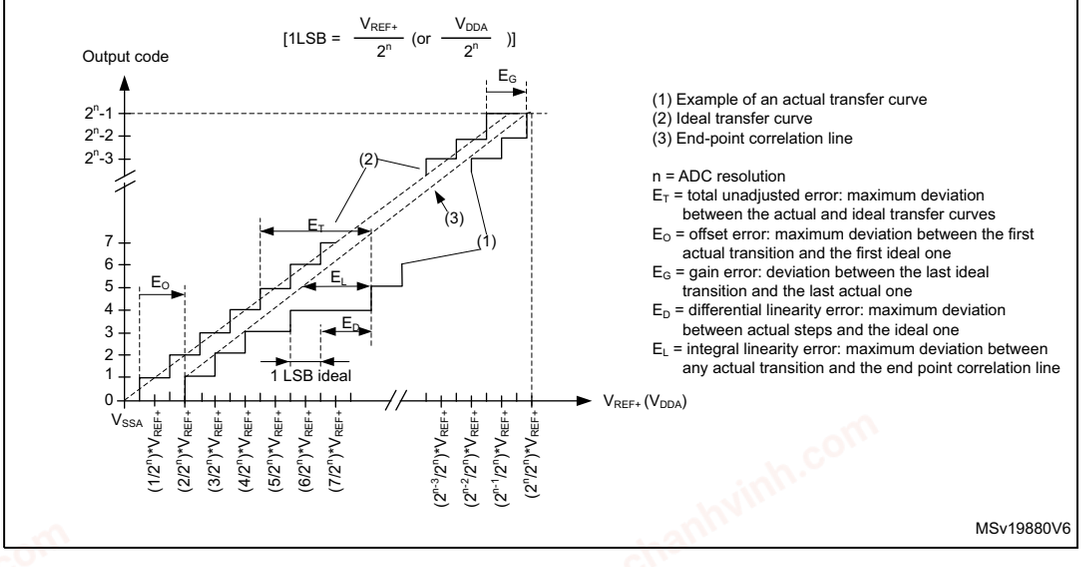
1. Specified by design, not tested in production.
2. BOOSTEN and ANASWVDD configured according to V_{DD} and V_{DDA} levels.
3. Values without external capacitance.

Table 70. 12-bit ADC4 accuracy(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	-	-	±3	±7.5	LSB
EO	Offset error		-	±2	±5.5	
EG	Gain error		-	±2	±6.5	
ED	Differential linearity error		-	-0.9/+1.0	-0.9/+1.5	
EL	Integral linearity error		-	±2	±3.5	
ENOB	Effective number of bits		9.9	10.9	-	bits
SINAD	Signal-to-noise and distortion ratio		61.4	67.4	-	dB
SNR	Signal-to-noise ratio		61.6	67.5	-	
THD	Total harmonic distortion		-	-74	-70	

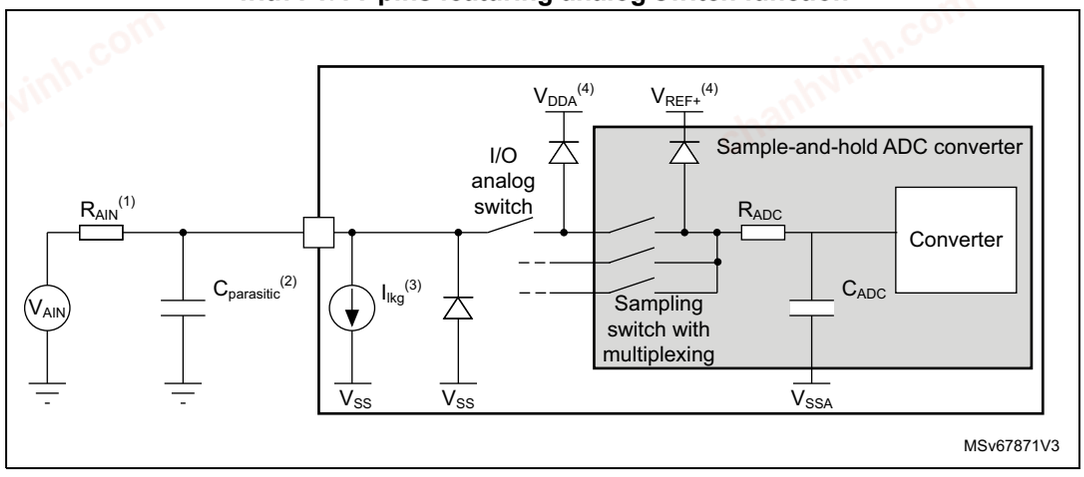
1. Evaluated by characterization, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (resolution = 12 bits, no oversampling).

Figure 18. ADC accuracy characteristics



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Figure 19. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



1. Refer to *Table 68* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the PCB capacitance (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 61* for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades the conversion accuracy. As a remedy, reduce f_{ADC}.
3. Refer to *Table 61* for the values of I_{lkg}.
4. Refer to *Figure 9*.

5.3.22 Temperature sensor characteristics

Table 71. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)(2)	V_{SENSE} linearity with temperature	-	-	1.3	°C
Avg_Slope(3)	Average slope	2	2.5	3.0	mV/ °C
$V_{SENSE30}$(4)	V_{SENSE} voltage at V_{DDA} = 3.0 V (±10 mV) and 30 °C (±1 °C)	700	742	800	mV
($V_{continous0}$ - $V_{sampling}$)(2)	Voltage difference between continuous and sampling modes(5)	-10	-	+4	mV
$t_{START(TS_BUF)}$(2)	Sensor buffer startup time	-	1	10	µs
t_{S_temp}(2)	ADC sampling time when reading the temperature	13	-	-	µs
$I_{DD(TS)}$(2)	Consumption from V_{DD}, when selected by ADC	-	14	20	µA

1. V_{SENSE} linearity depends upon calibration points. When using TS_CALx calibration points, linearity within the calibration limits is degraded by ±5 °C. Linearity outside the calibration limits is degraded more, due to the extrapolation.
2. Specified by design, not tested in production.
3. Evaluated by characterization, not tested in production, unless otherwise specified.
4. The $V_{SENSE30}$ ADC4 conversion result is stored in the TS_CAL1 field.
5. The temperature sensor is in continuous mode when the regulator is in range 1, in sampling mode when the regulator is in range 2 or the device is in Stop 1 mode.

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5.3.23 V_{CORE} monitoring characteristics

Table 72. V_{CORE} monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_{S_VCORE}	ADC sampling time when reading the V_{CORE} voltage	1	-	-	µs

1. Specified by design, not tested in production.

5.3.24 Timer characteristics

The parameters given in the following tables are specified by design. Refer to *Section 5.3.16* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 73. TIMx(1) characteristics(2)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 100 MHz	10	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 100 MHz	0	50	
Res_{TIM}	Timer resolution	TIM1, TIM16	-	16	bit
		TIM2	-	32	
$t_{COUNTER16}$	16-bit counter period	-	1	2^{16}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 100 MHz	0.01	655.36	µs
$t_{COUNTER32}$	32-bit counter period	-	1	2^{32}	$t_{TIMxCLK}$
		$f_{TIM2CLK}$ = 100 MHz	0,01	42.94	s

1. TIMx is used as a general term, where x stands for 1, 2, 3, 16, or 17.
2. Specified by design, not tested in production.

Table 74. IWDG min/max timeout period at 32 kHz(1)(2)

Prescaler divider	PR[3:0] bits	Min timeout RL[11:0] = 0x002	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.325	512	ms
/8	1	0.750	1024	
/16	2	1.500	2048	
/32	3	3.0	4096	
/64	4	6.0	8192	
/128	5	12.0	16384	
/256	6	24.0	32768	
/512	7	48.0	65536	
/1024	Others	96.0	131072	

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1. The exact timings depend upon the phasing of the APB interface clock vs. the IWDG kernel clock, hence there is always a full kernel clock period of uncertainty.
2. Specified by design, not tested in production.

Table 75. WWDG min/max timeout value at 100 MHz (PCLK)

Prescaler divider	WDGTB[2:0]	Min timeout value	Max timeout value	Unit
/1	0	0.040	1.621	ms
/2	1	0.081	5.242	
/4	2	0.163	10.485	
/8	3	0.327	20.971	
/16	4	0.655	41.943	
/32	5	1.310	83.886	
/64	6	2.621	167.772	
/128	7	5.242	335.544	

5.3.25 I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): bit rate up to 1 Mbit/s.

The I²C timings are valid when the I2C peripheral is properly configured (see the reference manual).

The SDA and SCL I/O requirements are met with the following restriction: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. I²C SDA and SCL use I/O FT structure with _f option supporting Fm+ low-level output-current maximum requirement. Refer to *Section 5.3.16* for I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter, refer to *Table 76* for its characteristics.

Table 76. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes suppressed by the analog filter	50(2)	190(3)	ns

1. Specified by design, not tested in production.
2. Spikes with widths below t_{AF} min are filtered.
3. Spikes with widths above t_{AF} max are not filtered.

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5.3.26 USART characteristics

Unless otherwise specified, the parameters given in *Table 77* are derived under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 26*, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30pF
- Measurement points are done at 0.5 x V_{DD}
- I/O compensation cell activated
- Voltage scaling range 1

Refer to *Section 5.3.16* for more details on the I/O input/output characteristics (NSS, CK, TX, RX for USART).

Table 77. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	12.5	MHz
		Slave receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	33.0	
		Slave transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	35.5	
		Slave transmitter, 1.71 V ≤ V_{DD} < 2.7 V	-	-	25.0	
$t_{su(NSS)}$	NSS setup time	Slave mode(2)	t_{ker} + 2	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	4	-	-	
$t_{w(CKH)}$ $t_{w(CKL)}$	SCK high and low time	Master mode	(1 / f_{CK}) / 2 - 1	(1 / f_{CK}) / 2	(1 / f_{CK}) / 2 + 1	
$t_{su(RX)}$	Data input setup time	Master mode	18.5	-	-	
		Slave mode	1.5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0.5	-	-	
		Slave mode	2	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	14	
		Slave mode, 1.71 V ≤ V_{DD} < 2.7 V	-	12	20	
		Master mode	-	0.5	1.0	
$t_{h(TX)}$	Data output hold time	Slave mode	10	-	-	
		Master mode	0	-	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. T_{ker} is the usart_ker_ck_pres clock period.

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Figure 20. USART timing diagram in master mode

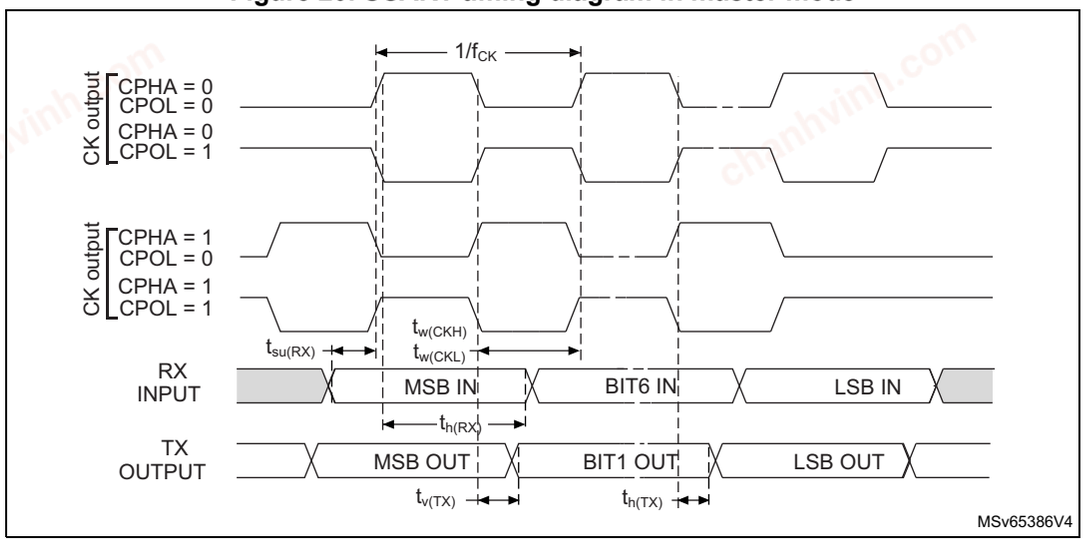
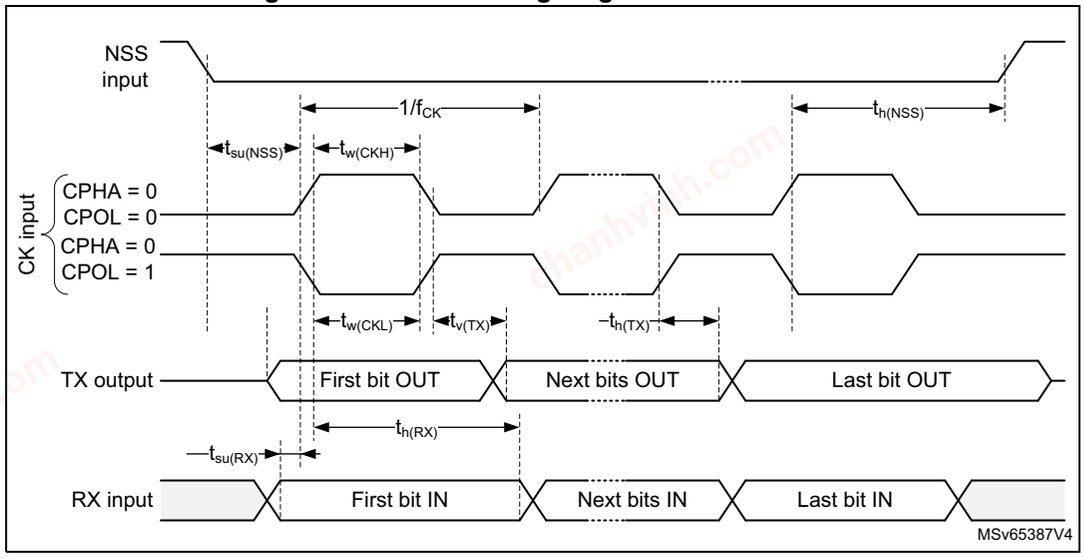


Figure 21. USART timing diagram in slave mode



5.3.27 SPI characteristics

Unless otherwise specified, the parameters given in *Table 78* are under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 26*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at 0.5 x V_{DD}
- I/O compensation cell activated

Refer to *Section 5.3.16* for more details on the I/O input/output characteristics (NSS, SCK, MOSI, MISO for SPI).

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Table 78. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{SCK}$	Clock frequency	Master receiver mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	50	MHz
		Master receiver mode 1.71 V ≤ V_{DD} < 2.7 V			33	
		Master transmitter mode 2.7 V ≤ V_{DD} < 3.6 V			50	
		Master transmitter mode 1.71 V ≤ V_{DD} < 2.7 V			33	
		Slave receiver mode 1.71 V ≤ V_{DD} ≤ 3.6 V			100	
		Slave transmitter mode 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 1			35.5(2)	
		Slave transmitter mode 1.71 V ≤ V_{DD} < 2.7 V, voltage range 1			24(2)	
		Slave transmitter mode 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 2			16	
$t_{su(NSS)}$	NSS setup time	Slave mode	$4*T_{pclk}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2*T_{pclk}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode(3)	$t_{SCK}/2 - 1$	$t_{SCK}/2$	$t_{SCK}/2 + 1$	
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	ns
$t_{su(SI)}$		Slave mode	2.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2.0	-	-	
$t_{h(SI)}$		Slave mode	1.0	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	10.5	21.0	
$t_{dis(SO)}$	Data output disable time		10.5	13.0	21.0	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 1	-	10.5	14.0	ns
		Slave mode (after enable edge) 1.71 V ≤ V_{DD} < 2.7 V, voltage range 1	-	16.5	20.5	
		Slave mode (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 2	-	14.0	18.5	
		Slave mode (after enable edge) 1.71 V ≤ V_{DD} < 2.7 V, voltage range 2	-	21.0	25.5	
$t_{v(MO)}$		Master mode	-	0.5	2.0	
$t_{h(SO)}$	Data output hold time	Slave mode	7.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Evaluated by characterization, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$, which must fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

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3. $t_{SCK} = t_{spi_ker_ck}$ x baudrate prescaler

Figure 22. SPI timing diagram - Slave mode and CPHA = 0

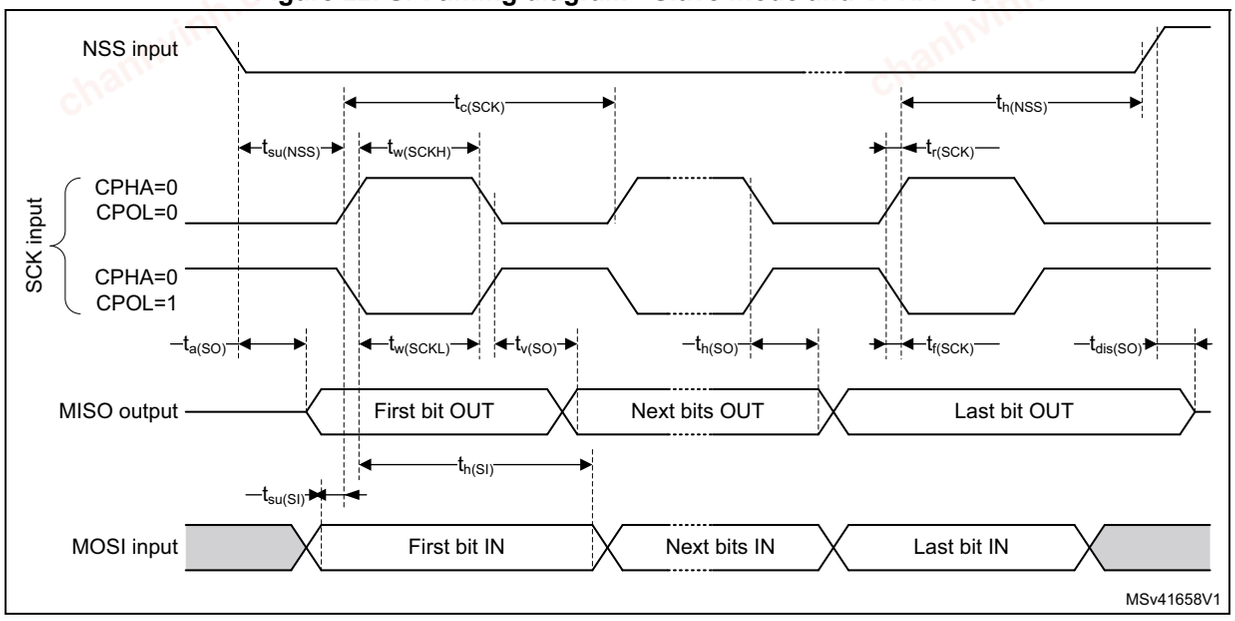
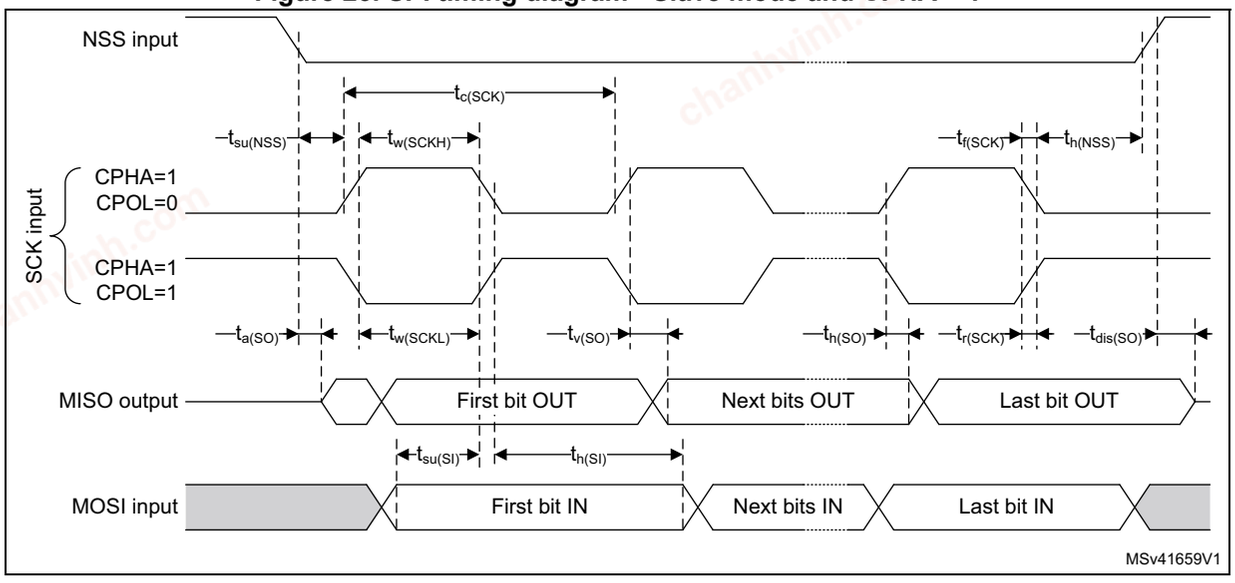
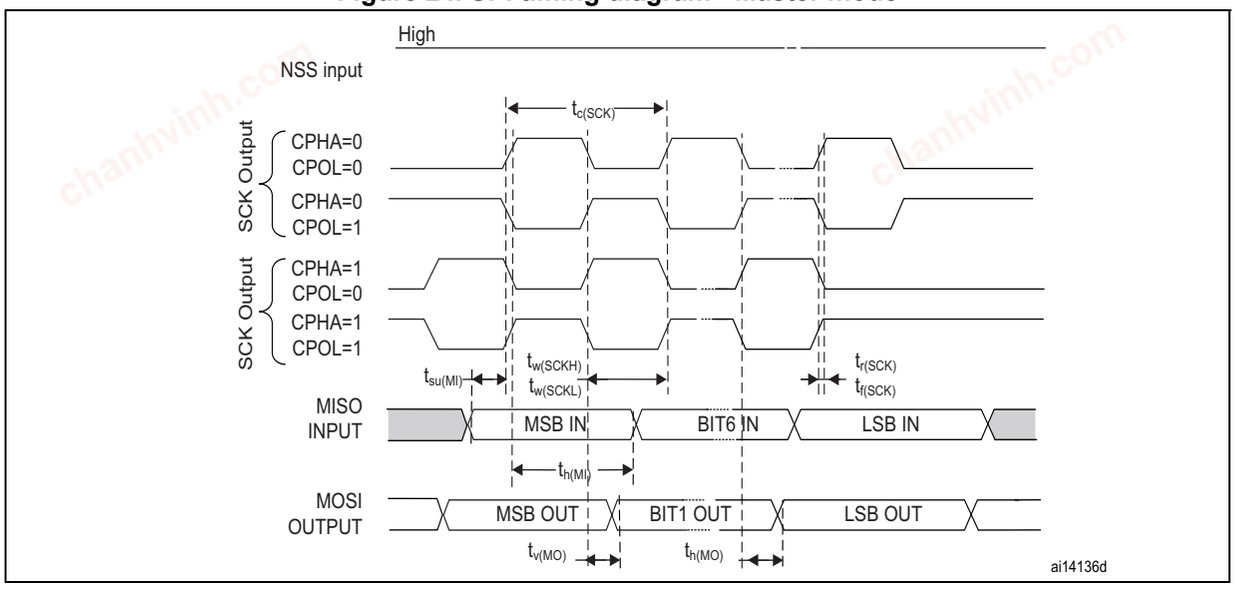


Figure 23. SPI timing diagram - Slave mode and CPHA = 1



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Figure 24. SPI timing diagram - Master mode



5.3.28 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in the tables below are with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 00
- Capacitive load C = 30 pF
- Measurement points are done at 0.5 x V_{DD}
- I/O compensation cell disabled

Table 79. JTAG characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TCK} $1/t_{c(TCK)}$	TCK clock frequency	2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	30	MHz
		1.71 V ≤ V_{DD} < 2.7 V	-	-	20.5	
$t_{isu(TMS)}$	TMS input setup time	-	1.5	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	3	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	9	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	0	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7 V ≤ V_{DD} ≤ 3.6 V	-	13	16.5	
		1.71 V ≤ V_{DD} < 2.7 V	-	13	24	
$t_{oh(TDO)}$	TDO output hold time	-	10	-	-	

1. Evaluated by characterization, not tested in production.

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Table 80. SWD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SWCLK} $1/t_{c(SWCLK)}$	SWCLK clock frequency	2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	62.5	MHz
		1.71 V ≤ V_{DD} < 2.7 V	-	-	34	
$t_{isu(SWDIO)}$	SWDIO input setup time	-	1	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	-	2.5	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	16	
		1.71 V ≤ V_{DD} < 2.7 V	-	12	29	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8.5	-	-	

1. Evaluated by characterization, not tested in production.

Figure 25. JTAG timing diagram

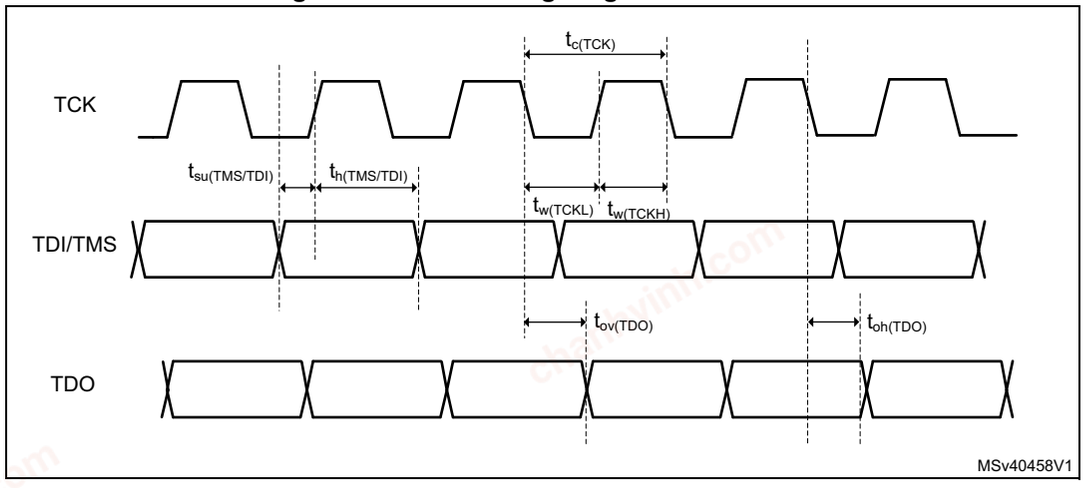
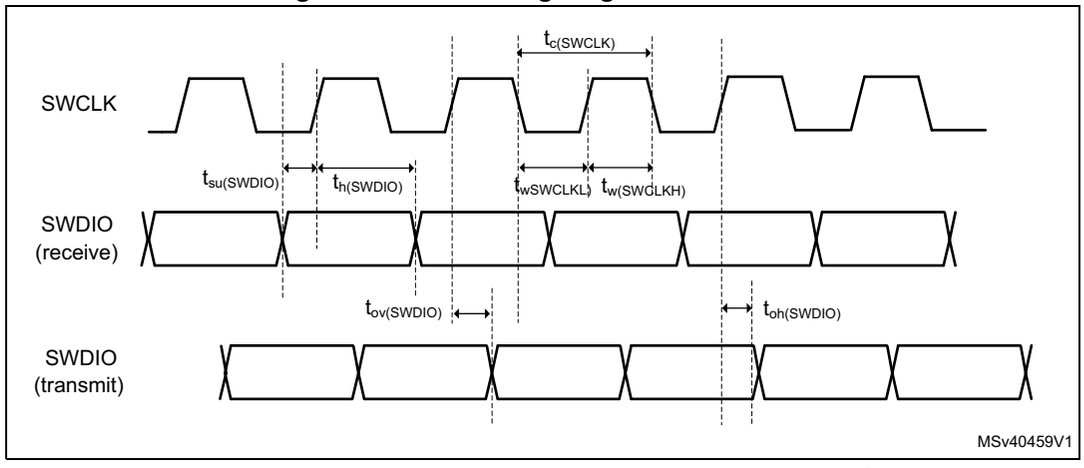


Figure 26. SWD timing diagram



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6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 Device marking

Refer to “*Reference device marking schematics for STM32 microcontrollers and microprocessors*” (TN1433), available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

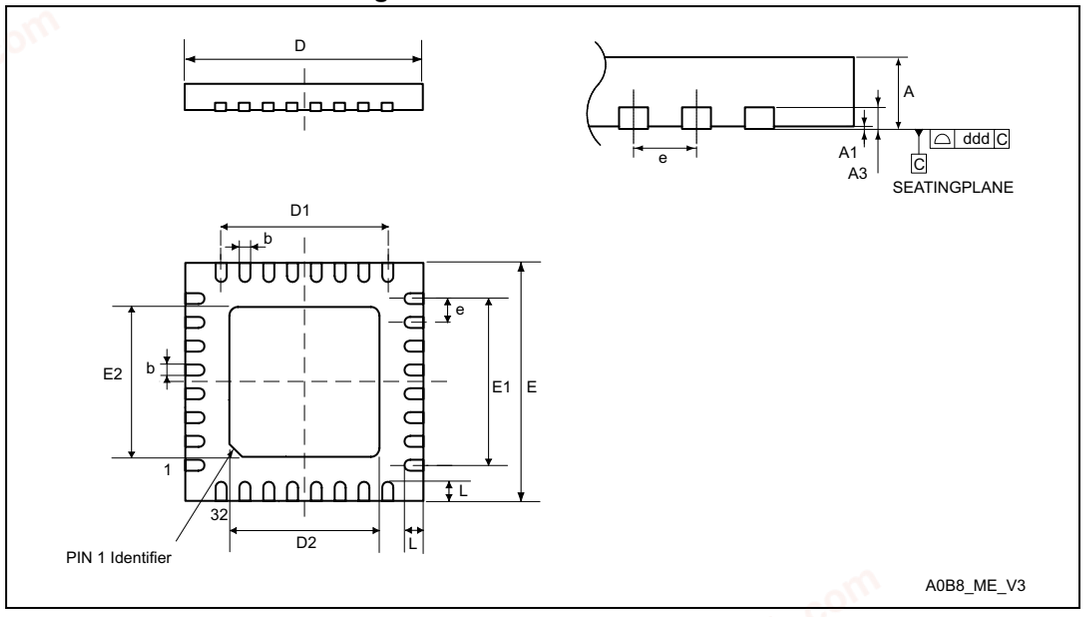
Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

6.2 UFQFPN32 package information (A0B8)

This UFQFPN is a 32-pin, 5 x 5 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 27. UFQFPN32 - Outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is mandatory to connect and

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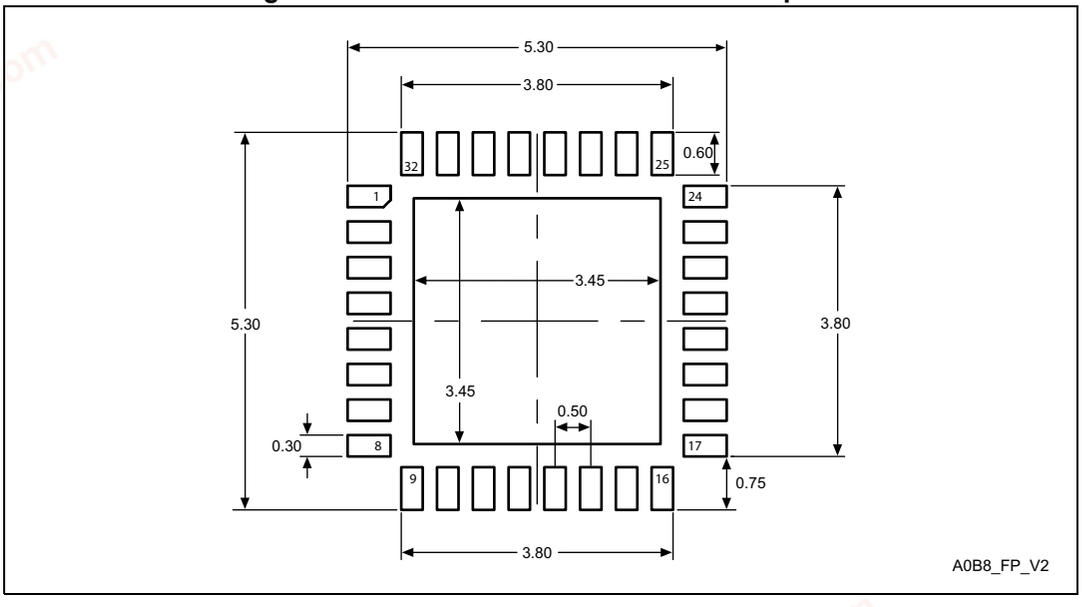
solder this back-side pad to PCB ground.

Table 81. UFQFPN32 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	-	0.300	0.0071	-	0.0118
D[2]	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	-	3.700	0.1339	-	0.1457
D2	3.400	-	3.600	0.1339	-	0.1417
E[2]	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	-	3.700	0.1339	-	0.1457
E2	3.400	-	3.700	0.1339	-	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimensions D and E do not include mold protrusion, not to exceed 0,15 mm.

Figure 28. UFQFPN32 - Recommended footprint



1. Dimensions are expressed in millimeters.

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6.3 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the specified values.

T_J max (in Celsius degrees), can be calculated using the equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

where:

- T_A max is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max)
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watt (this is the maximum chip internal power)

$P_{I/O}$ max represents the maximum power dissipation on output pins:

- $P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH})$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 82. Package thermal characteristics

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient**	UFQFPN32 - 5 mm x 5 mm	36.6	°C/W
Θ_{JB}	**Thermal resistance junction-board**	UFQFPN32 - 5 mm x 5 mm	18.3	
Θ_{JC}	**Thermal resistance junction-case**	UFQFPN32 - 5 mm x 5 mm	14.3	

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7 Ordering information

Example: STM32 WB A50 K G U 6 TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

WB = Wireless Bluetooth®

Device subfamily

A50 = Full set of features

Pin count

K = 32 pins

Flash memory size

G = 1 Mbyte

Package

U = UFQFPN

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

Packing

TR = Tape and reel

xxx = Programmed parts

For a list of available options (memory, package, and so on), or for further information on any aspect of this device, contact your nearest ST sales office.

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9 Revision history

Table 83. Document revision history

Date	Revision	Changes
12-Sep-2024	1	Initial release.

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