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STM32WB50CG
STM32WB30CE

Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5.4 or 802.15.4 radio solution

Datasheet - production data

Features

- Include ST state-of-the-art patented technology
- Radio
  - 2.4 GHz
  - RF transceiver supporting Bluetooth® 5.4 specification or IEEE 802.15.4-2011 PHY and MAC, supporting Thread 1.3 and Zigbee® 3.0
  - RX sensitivity: -96 dBm (Bluetooth® Low Energy at 1 Mbps), -100 dBm (802.15.4)
  - Programmable output power up to +4 dBm with 1 dB steps
  - Integrated balun to reduce BOM
  - Support for 1 Mbps
  - Support GATT caching
  - Support EATT (enhanced ATT)
  - Support advertising extension
  - Dedicated Arm® 32-bit Cortex® M0+ CPU for real-time Radio layer
  - Accurate RSSI to enable power control
  - Suitable for systems requiring compliance with radio frequency regulations ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T66
  - Support for external PA
  - Available integrated passive device (IPD) companion chip for optimized matching solution (MLPF-WB-01E3)
- Ultra-low-power platform
  - 2.0 to 3.6 V power supply
  - – 10 °C to +85 °C temperature range
  - 14 nA shutdown mode
  - 700 nA Standby mode + RTC + 32 KB RAM
  - 2.25 µA Stop mode + RTC + 128 KB RAM
  - Radio: Rx 7.9 mA / Tx at 0 dBm 8.8 mA



UFQFPN48
7 x 7 mm
solder pad

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, adaptive real-time accelerator (ART™ Accelerator) allowing 0-wait-state execution from flash memory, frequency up to 64 MHz, MPU, 80 DMIPS and DSP instructions
- Performance benchmark
  - 1.25 DMIPS/MHz (Drystone 2.1)
  - 219.48 CoreMark® (3.43 CoreMark/MHz at 64 MHz)
- Energy benckmark
  - 303 ULPMark™ CP score
- Supply and reset management
  - Ultra-safe, low-power BOR (brownout reset) with five selectable thresholds
  - Ultra-low-power POR/PDR
  - Programmable voltage detector (PVD)
  - V_{BAT} mode with RTC and backup registers
- Clock sources
  - 32 MHz crystal oscillator with integrated trimming capacitors (Radio and CPU clock)
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal low-power 32 kHz (±5%) RC (LSI1)
  - Internal low-power 32 kHz (stability ±500 ppm) RC (LSI2)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25% accuracy)
  - High speed internal 16 MHz factory trimmed RC (±1%)
  - 1x PLL for system clock, ADC

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- Memories
  - 1 MB flash memory with sector protection (PCROP) against R/W operations, enabling radio stack and application
  - 128 KB SRAM, including 64 KB with hardware parity check
  - 20x 32-bit backup register
  - Boot loader supporting USART, SPI, I2C interfaces
  - OTA (over the air) Bluetooth® Low Energy and 802.15.4 update
  - 1 Kbyte (128 double words) OTP
- Rich analog peripherals (down to 2.0 V)
  - 12-bit ADC 2.13 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
- System peripherals
  - Inter processor communication controller (IPCC) for communication with Bluetooth® Low Energy and 802.15.4
  - HW semaphores for resources sharing between CPUs
  - 1x DMA controller (7x channels) supporting ADC, SPI, I2C, USART, AES, timers
  - 1x USART (ISO 7816, IrDA, SPI Master, Modbus and Smartcard mode)
  - 1x SPI 32 Mbit/s
  - 1x I2C (SMBus/PMBus®)
  - 1x 16-bit, four channels advanced timer
  - 2x 16-bit, two channels timer
  - 1x 32-bit, four channels timer
  - 2x 16-bit ultra low power timer
  - 1x independent Systick
  - 1x independent watchdog
  - 1x window watchdog
- Security and ID
  - Secure firmware installation (SFI) for Bluetooth® Low Energy and 802.15.4 SW stack
  - 2x hardware encryption AES maximum 256-bit for the application, the Bluetooth® Low Energy and IEEE802.15.4
  - HW public key authority (PKA)
  - Cryptographic algorithms: RSA, Diffie-Helman, ECC over GF(p)
  - True random number generator (RNG)
  - Sector protection against R/W operation (PCROP)
  - CRC calculation unit
  - Die information: 96-bit unique ID
  - IEEE 64-bit unique ID, possibility to derive 802.15.4 64-bit and Bluetooth® Low Energy 48-bit EUI
- Up to 30 fast I/Os, 28 of them 5 V-tolerant
- Development support
  - Serial wire debug (SWD), JTAG for the application processor
  - Application cross trigger
- ECOPACK2 compliant package

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32WB50CG and STM32WB30CE microcontrollers, based on Arm® cores[a].

This document must be read with the reference manual (RM0471), available from the STMicroelectronics website *www.st.com*.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32WB50CG and STM32WB30CE errata sheet (ES0492), available from the STMicroelectronics website *www.st.com*.

For information on the Arm® Cortex®-M4 and Cortex®-M0+ cores, refer, respectively, to the Cortex®-M4 Technical Reference Manual and to the Cortex®-M0+ Technical Reference Manual, both available on the www.arm.com website.

For information on 802.15.4 refer to the IEEE website (www.ieee.org).

For information on Bluetooth® refer to www.bluetooth.com.

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2 Description

The STM32WB50CG and STM32WB30CE multiprotocol wireless and ultra-low-power device embeds a powerful and ultra-low-power radio compliant with the Bluetooth® Low Energy SIG specification 5.4 or with IEEE 802.15.4-2011. It contains a dedicated Arm® Cortex®-M0+ for performing all the real-time low layer operation.

The devices are designed to be extremely low-power and are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 64 MHz. This core features a Floating point unit (FPU) single precision that supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) that enhances application security.

Enhanced inter-processor communication is provided by the IPCC with six bidirectional channels. The HSEM provides hardware semaphores used to share common resources between the two processors.

The devices embed high-speed memories (1 Mbyte of flash memory for STM32WB50xx, 512 Kbytes for STM32WB30xx, 128 Kbytes of SRAM for STM32WB50xx, 96 Kbytes for STM32WB30xx) and an extensive range of enhanced I/Os and peripherals.

Direct data transfer between memory and peripherals and from memory to memory is supported by seven DMA channels with a full flexible channel mapping by the DMAMUX peripheral.

The devices feature several mechanisms for embedded flash memory and SRAM: readout protection, write protection and proprietary code readout protection. Portions of the memory can be secured for Cortex® -M0+ exclusive access.

The AES encryption engine, PKA, and RNG enable lower layer MAC and upper layer cryptography.

The devices offer a fast 16-bit ADC.

These devices embed a low-power RTC, one advanced 16-bit timer, one general-purpose 32-bit timer, two general-purpose 16-bit timers, and two 16-bit low-power timers.

The STM32WB50CG and STM32WB30CE also feature standard and advanced communication interfaces, namely one USART (ISO 7816, IrDA, Modbus, and Smartcard mode), one I2C (SMBus/PMBus), one SPI up to 32 MHz.

The STM32WB50CG and STM32WB30CE operate in the -10 to +85 °C (+105 °C junction) temperature range from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes enables the design of low-power applications.

The devices include independent power supplies for analog input for ADC.

A V_{BAT} dedicated supply allows the device to back up the LSE 32.768 kHz oscillator, the RTC and the backup registers, thus enabling the STM32WB50CG and STM32WB30CE to supply these functions even if the main V_{DD} is not present through a CR2032-like battery, a Supercap or a small rechargeable battery.

The STM32WB50CG and STM32WB30CE are available in a 48-pin UFQFPN package.

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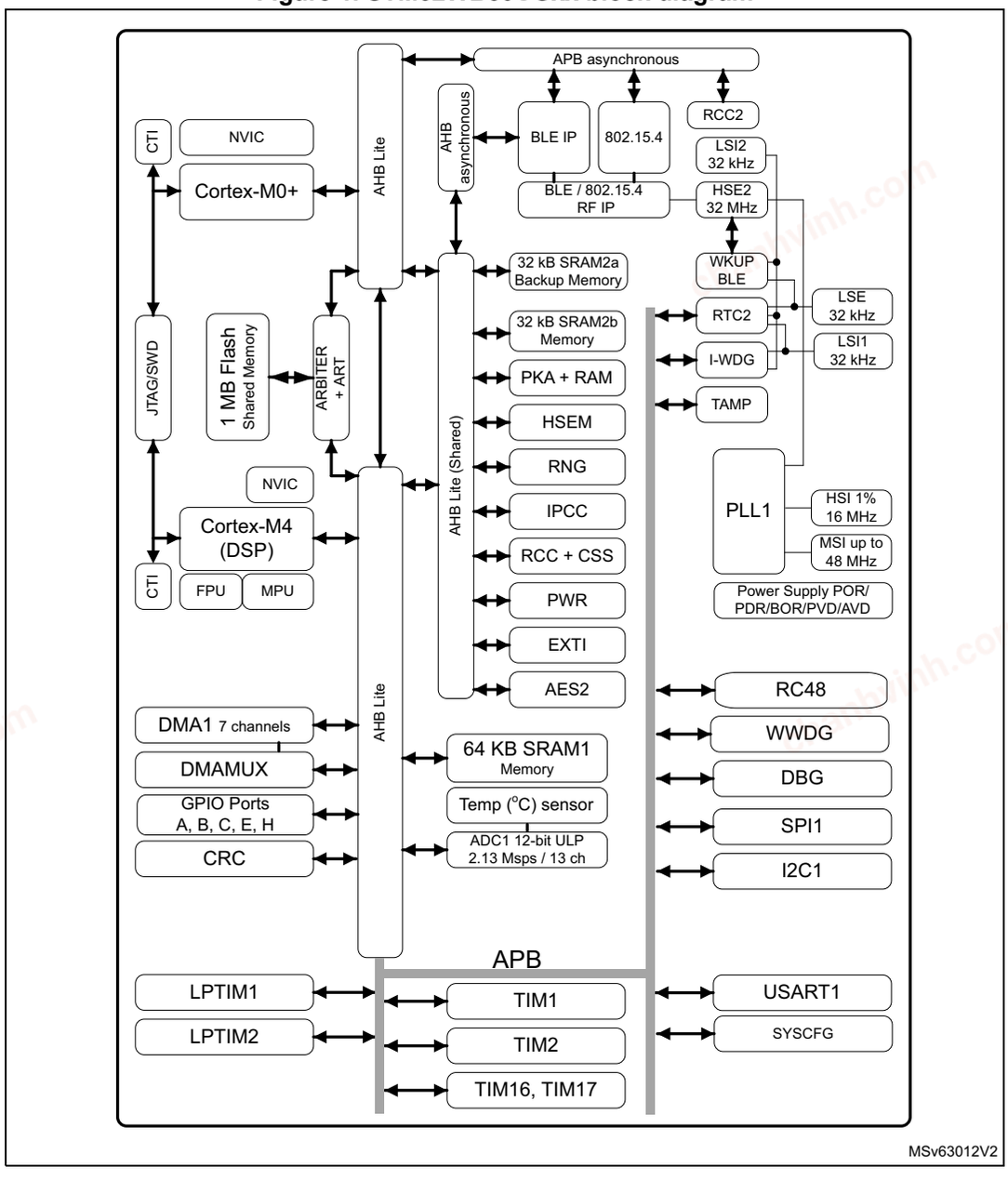
Table 1. STM32WB50CG and STM32WB30CE device features and peripheral counts

Feature		STM32WB50CG	STM32WB30CE
Flash memory density		1 M bytes	512 Kbytes
SRAM density		128 Kbytes	96 Kbytes
SRAM1		64 Kbytes	32 Kbytes
SRAM2		64 Kbytes	64 Kbytes
BLE		5.4	
802.15.4		Yes	
Timers	Advanced	1 (16 bits)	
	General purpose	2 (16 bits) + 1 (32 bits)	
	Low power	2 (16 bits)	
	SysTick	1	
Communication interface	SPI	1	
	I2C	1	
	USART(1)	1	
RTC		1	
Tamper pin		1	
Wake-up pin		2	
GPIOs		30	
12-bit ADC Number of channels		13 channels (incl. 3 internal)	
Internal V_{ref}		Yes	
Max CPU frequency		64 MHz	
Operating temperature		Ambient operating temperature:-10 to +85 °C Junction temperature: -10 to 105 °C	
Operating voltage		2.0 to 3.6 V	
Package		UFQFPN48, 7 mm x 7 mm, 0.5 mm pitch, solder pad	

1. USART peripheral can be used as SPI.

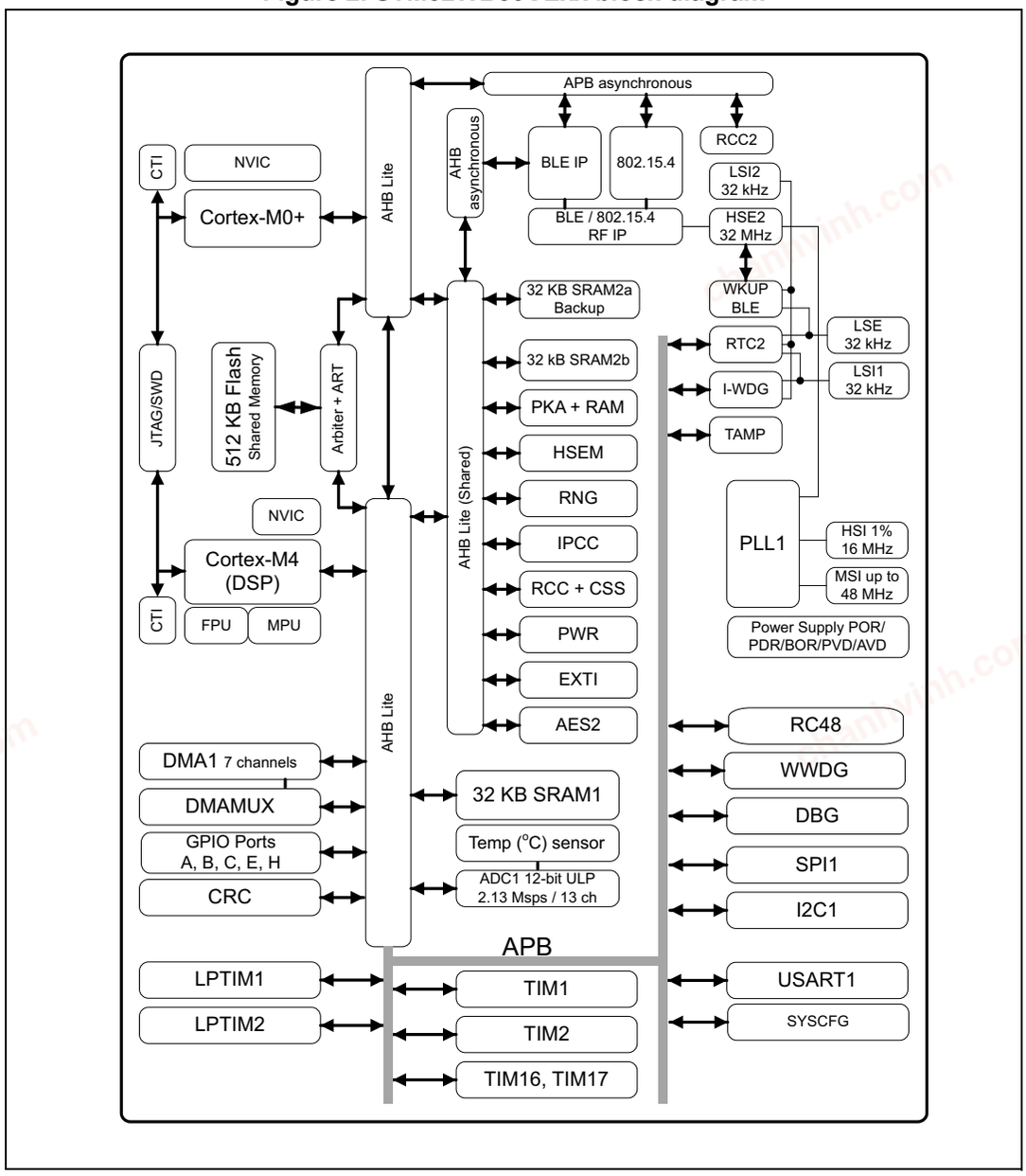
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Figure 1. STM32WB50CGxx block diagram



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Figure 2. STM32WB30CExx block diagram



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3 Functional overview

3.1 Architecture

The STM32WB50CG and STM32WB30CE multiprotocol wireless device embeds a Bluetooth Low Energy or an 802.15.4 RF subsystem that interfaces with a generic microcontroller subsystem using an Arm® Cortex®-M4 CPU (called CPU1) on which the host application resides.

The RF subsystem is composed of an RF analog front end, Bluetooth Low Energy or 802.15.4 digital MAC blocks as well as of a dedicated Arm® Cortex®-M0+ microcontroller (called CPU2), plus proprietary peripherals. The RF subsystem performs all of the Bluetooth Low Energy or 802.15.4 low layer stack, reducing the interaction with the CPU1 to high level exchanges.

Some functions are shared between the RF subsystem CPU (CPU2) and the Host CPU (CPU1):

- Flash memories
- SRAM1, SRAM2a, and SRAM2b (SRAM2a can be retained in Standby mode)
- Security peripherals (RNG, PKA)
- Clock RCC
- Power control (PWR)

The communication and the sharing of peripherals between the RF subsystem and the Cortex®-M4 CPU is performed through a dedicated inter processor communication controller (IPCC) and semaphore mechanism (HSEM).

3.2 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU is a processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions enabling efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32WB50CG and STM32WB30CE are compatible with all Arm® tools and software.

Figure 1 and *Figure 2* show the general block diagram of, respectively, the STM32WB50CG and STM32WB30CE devices.

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3.3 Memories

3.3.1 Adaptive real-time memory accelerator (ART Accelerator)

The ART Accelerator is a memory accelerator optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over flash memory technologies, which normally require the processor to wait for the flash memory at higher frequencies.

To release the processor near 80 DMIPS performance at 64 MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from flash memory at a CPU frequency up to 64 MHz.

3.3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU1 accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to eight protected areas, which can be divided up into eight subareas. The protection area sizes are between 32 bytes and the whole 4 Gbytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location prohibited by the MPU, the RTOS detects it and acts. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3.3 Embedded flash memory

The STM32WB50CG and STM32WB30CE devices feature, respectively, 1 Mbyte and 512 Kbytes of embedded flash memory available for storing programs and data, as well as some customer keys.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the flash memory cannot be read from or written to if either debug features are connected, boot in SRAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex®-M4 and Cortex®-M0+ JTAG and serial wire), boot in SRAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

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Table 2. Access status vs. readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from SRAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No(1)	No(1)	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(2)	No	No	N/A(2)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2a SRAM2b	1	Yes	Yes	Yes(2)	No	No	No(2)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. The option byte can be modified by the RF subsystem.
2. Erased when RDP changes from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 4-Kbyte granularity.
- Proprietary code readout protection (PCROP): two parts of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. Two areas can be selected, with 2-Kbyte granularity. An additional option bit (PCROP_RDP) makes possible to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

A section of the flash memory is secured for the RF subsystem CPU2, and cannot be accessed by the host CPU1.

The whole nonvolatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection
- the address of the ECC fail can be read in the ECC register

The embedded flash memory is shared between CPU1 and CPU2 on a time sharing basis. A dedicated HW mechanism allows both CPUs to perform Write/Erase operations.

3.3.4 Embedded SRAM

The STM32WB50CG device features 128 Kbytes of embedded SRAM, split in three blocks:

- **SRAM1**: 64 Kbytes mapped at address 0x2000 0000
- **SRAM2a**: 32 Kbytes located at address 0x2003 0000 also mirrored at 0x1000 0000, with hardware parity check (this SRAM can be retained in Standby mode)
- **SRAM2b**: 32 Kbytes located at address 0x2003 8000 (contiguous with SRAM2a) and mirrored at 0x1000 8000 with hardware parity check

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The STM32WB30CG device features 96 Kbytes of embedded SRAM, split in three blocks:

- **SRAM1**: 32 Kbytes mapped at address 0x2000 0000
- **SRAM2a**: 32 Kbytes located at address 0x2003 0000 also mirrored at 0x1000 0000, with hardware parity check (this SRAM can be retained in Standby mode)
- **SRAM2b**: 32 Kbytes located at address 0x2003 8000 (contiguous with SRAM2a) and mirrored at 0x1000 8000 with hardware parity check

SRAM2a and SRAM2b can be write-protected, with 1-Kbyte granularity. A section of the SRAM2a and SRAM2b is secured for the RF sub-system and cannot be accessed by the host CPU1.

The SRAMs can be accessed in read/write with 0 wait states for all CPU1 and CPU2 clock speeds.

3.4 Security and safety

The STM32WB50CG and STM32WB30CE contain many security blocks both for the Bluetooth Low Energy or IEEE 802.15.4 and the Host application.

It includes:

- Customer storage of the Bluetooth Low Energy or 802.15.4 keys
- Secure flash memory partition for RF subsystem-only access
- Secure SRAM partition, that can be accessed only by the RF subsystem
- True random number generator (RNG)
- Advance encryption standard hardware accelerators (AES-256bit, supporting chaining modes ECB, CBC, CTR, GCM, GMAC, CCM)
- Private key acceleration (PKA) including:
  - Modular arithmetic including exponentiation with maximum modulo size of 3136 bits
  - Elliptic curves over prime field scalar multiplication, ECDSA signature, ECDSA verification with maximum modulo size of 521 bits
- Cyclic redundancy check calculation unit (CRC)

A specific mechanism is in place to ensure that all the code executed by the RF subsystem CPU2 can be secure, whatever the Host application.

3.5 Boot modes and FW update

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user flash
- Boot from system memory
- Boot from embedded SRAM

The devices always boot on CPU1 core. The embedded bootloader code makes it possible to boot from various peripherals:

- UART
- I2C
- SPI

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Secure Firmware update (especially Bluetooth Low Energy or 802.15.4) from system boot and over the air is provided.

3.6 RF subsystem

The STM32WB50CG and STM32WB30CE embed an ultra-low power multi-standard radio Bluetooth Low Energy or 802.15.4 network processor, compliant with Bluetooth specification 5.4 and IEEE® 802.15.4-2011. The Bluetooth Low Energy features 1 Mbps transfer rate, supports multiple roles simultaneously acting at the same time as Bluetooth Low Energy sensor and hub device, embeds Elliptic Curve Diffie-Hellman (ECDH) key agreement protocol, thus ensuring a secure connection.

The Bluetooth Low Energy stack or 802.15.4 Low Level layer run on an embedded Arm® Cortex®-M0+ core (CPU2). The stack is stored on the embedded flash memory, which is also shared with the Arm® Cortex®-M4 (CPU1) application, making it possible in-field stack update.

3.6.1 RF front-end block diagram

The RF front-end is based on a direct modulation of the carrier in Tx, and uses a low IF architecture in Rx mode.

Thanks to an internal transformer at RF pins, the circuit directly interfaces the antenna (single ended connection, impedance close to 50 Ω). The natural bandpass behavior of the internal transformer, simplifies outside circuitry aimed for harmonic filtering and out of band interferer rejection.

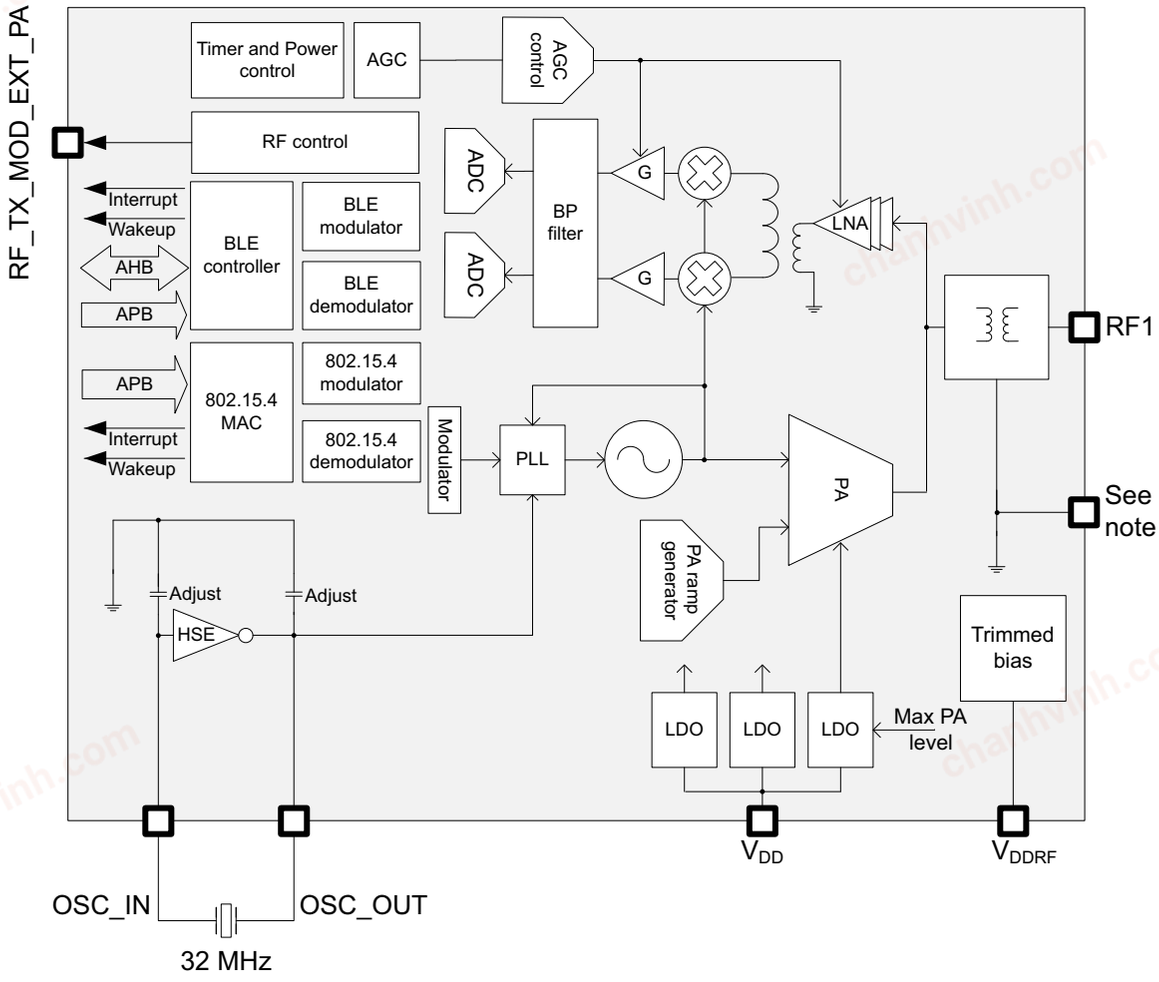
In Transmit mode, the maximum output power is user selectable through the programmable LDO voltage of the power amplifier. A linearized, smoothed analog control offers clean power ramp-up.

In receive mode the circuit can be used in standard high performance or in reduced power consumption (user programmable). The Automatic gain control (AGC) is able to reduce the chain gain at both RF and IF locations, for optimized interference rejection. Thanks to the use of complex filtering and highly accurate I/Q architecture, high sensitivity and excellent linearity can be achieved.

The bill of material is reduced thanks to the high degree of integration. The radio frequency source is synthesized form an external 32 MHz crystal that does not need any external trimming capacitor network thanks to a dual network of user programmable integrated capacitors.

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Figure 3. STM32WB50CG and STM32WB30CE RF front-end block diagram



Note: UFQFPN48: V_{SS} through exposed pad, and V_{SSRF} pin must be connected to ground plane

3.6.2 Bluetooth Low Energy general description

The Bluetooth Low Energy block is a master/slave processor, compliant with Bluetooth specification 5.4 standard.

It integrates a 2.4 GHz RF transceiver and a powerful Cortex®-M0+ core, on which a complete power-optimized stack for Bluetooth Low Energy protocol runs, providing master / slave role support

- GAP: central, peripheral, observer or broadcaster roles
- ATT/GATT: client and server
- SM: privacy, authentication and authorization
- L2CAP
- Link layer: AES-128 encryption and decryption

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In addition, according to Bluetooth specification 5.4, the Bluetooth Low Energy block provides:

- Multiple roles simultaneous support
- Master/slave and multiple roles simultaneously
- LE data packet length extension (making it possible to reach 800 kbps at application level)
- LE privacy 1.2
- LE secure connections
- Flexible Internet connectivity options

The devices support Piconet topology (master with up to eight slaves), Scatternet topology (master with up to six slaves and dynamically as slave with up to two masters, or master with up to four slaves and dynamically as slave with up to four masters), and multi slave topology (slave with up to eight masters).

The device allows the applications to meet the tight peak current requirements imposed by the use of standard coin cell batteries.

Ultra-low-power sleep modes and very short transition time between operating modes result in very low average current consumption during real operating conditions, resulting in longer battery life.

The Bluetooth Low Energy block integrates a full bandpass balun, thus reducing the need for external components.

The link between the Cortex®-M4 application processor (CPU1) running the application, and the Bluetooth Low Energy stack running on the dedicated Cortex®-M0+ (CPU2) is performed through a normalized API, using a dedicated IPCC.

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3.6.3 802.15.4 general description

The STM32WB50CG and STM32WB30CE embed a dedicated 802.15.4 hardware MAC:

- Support for 802.15.4 release 2011
- Advanced MAC frame filtering; hardwired firewall: Programmable filters based on source/destination addresses, frame version, security enabled, frame type
- 256-byte RX FIFO; Up to 8 frames capacity, additional frame information (timing, mean RSSI, LQI)
- 128-byte TX FIFO with retention
  - Content not lost, retransmissions possible under CPU2 control
- Automatic frame acknowledgment, with programmable delay
- Advanced channel access features
  - Full CSMA-CA support
  - Superframe timer
  - Beaconing support (require LSE)
  - Flexible TX control with programmable delay
- Configuration registers with retention available down to Standby mode for software/auto-restore
- Autonomous sniffer, wake-up based on timer or CPU2 request
- Automatic frame transmission/reception/sleep periods, Interrupt to the CPU2 on particular events

3.6.4 RF pin description

The RF block contains dedicated pins, listed in *Table 3*.

Table 3. RF pin list

Name	Type	Description
RF1	I/O	RF Input/output, must be connected to the antenna through a low-pass matching network
OSC_OUT		32 MHz main oscillator, also used as HSE source
OSC_IN		
RF_TX_ MOD_EXT_PA		External PA transmit control
VDDRF	V_{DD}	Dedicated supply, must be connected to V_{DD}
VSSRF(1)	V_{SS}	To be connected to GND

1. The exposed pad must be connected to GND plane for correct RF operation.

3.6.5 Typical RF application schematic

The schematic in *Figure 4* and the external components listed in *Table 3* are purely indicative. For more details refer to the “Reference design” provided in separate documents.

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Figure 4. External components for the RF part

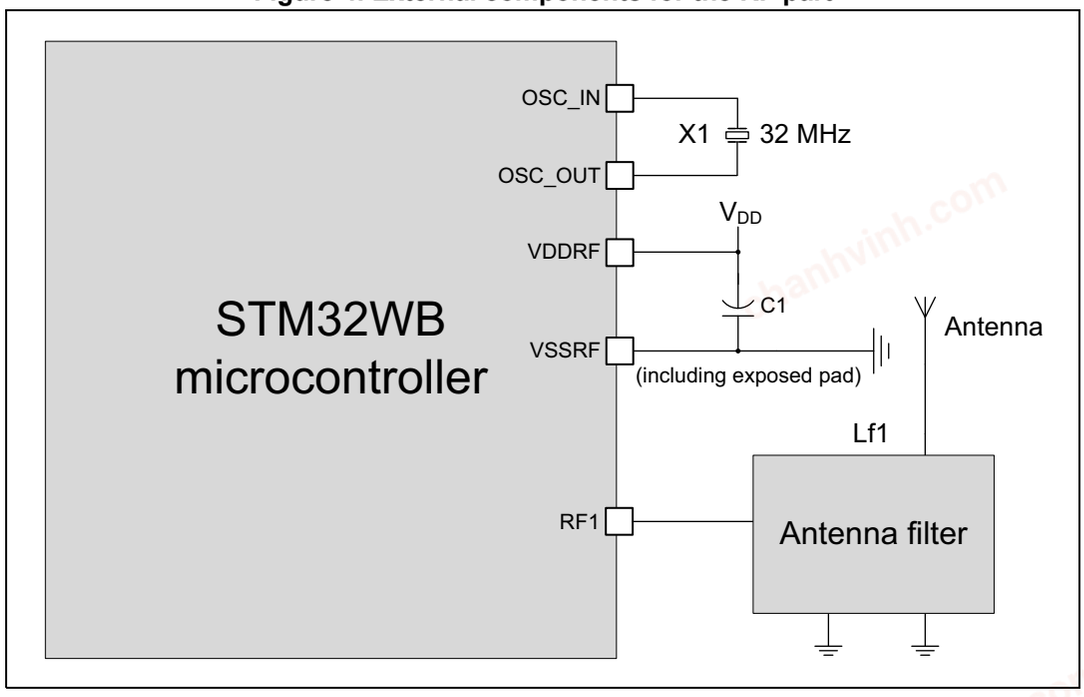


Table 4. Typical external components

Component	Description	Value
C1	Decoupling capacitance for RF	100 nF // 100 pF
X1	32 MHz crystal(1)	32 MHz
Antenna filter	Antenna filter and matching network	Refer to AN5165, on *www.st.com*
Antenna	2.4 GHz band antenna	-

1. e.g. NDK reference: NX2016SA 32 MHz EXS00A-CS06654.

Note: For more details refer to AN5165 "Development of RF hardware using STM32WB microcontrollers" available on www.st.com.

3.7 Power supply management

3.7.1 Power supply schemes

The devices have different voltage supplies (see *Figure 6*) and can operate within the following voltage ranges:

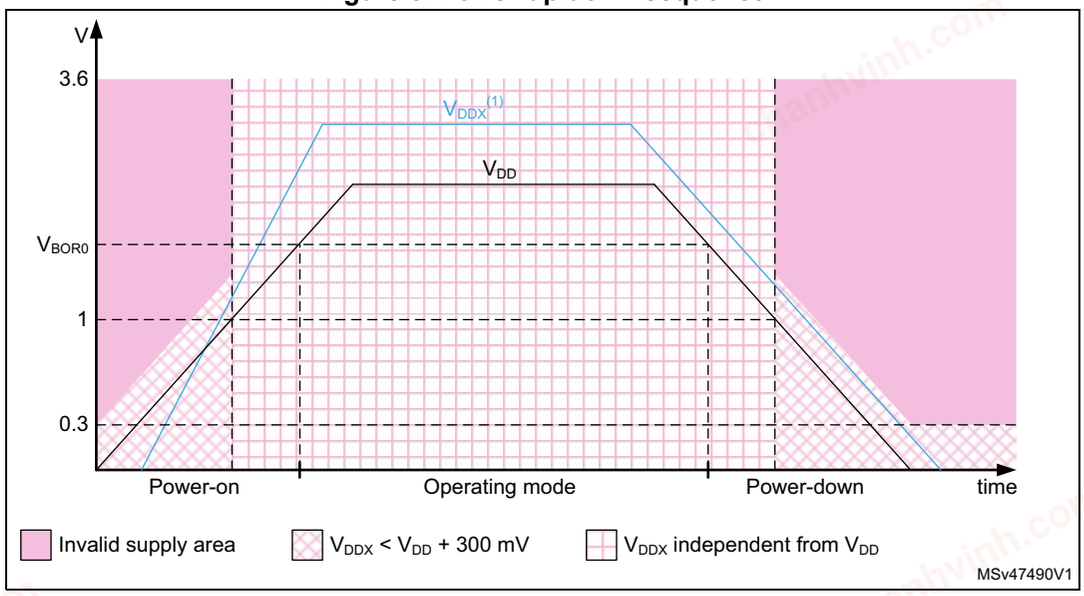
- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os (V_{DDIO}), the internal regulator and system functions such as RF, reset, power management and internal clocks. It is provided externally through VDD pins. V_{DDRF} must be always connected to VDD pins.
- V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC,. The V_{DDA} voltage level can be independent from the V_{DD} voltage. When not used V_{DDA} must be connected to V_{DD}.

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During power up/down, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V the other power supply (V_{DDA}), must remain below V_{DD} + 300 mV
- When V_{DD} is above 1 V all power supplies are independent.

Figure 5. Power-up/down sequence



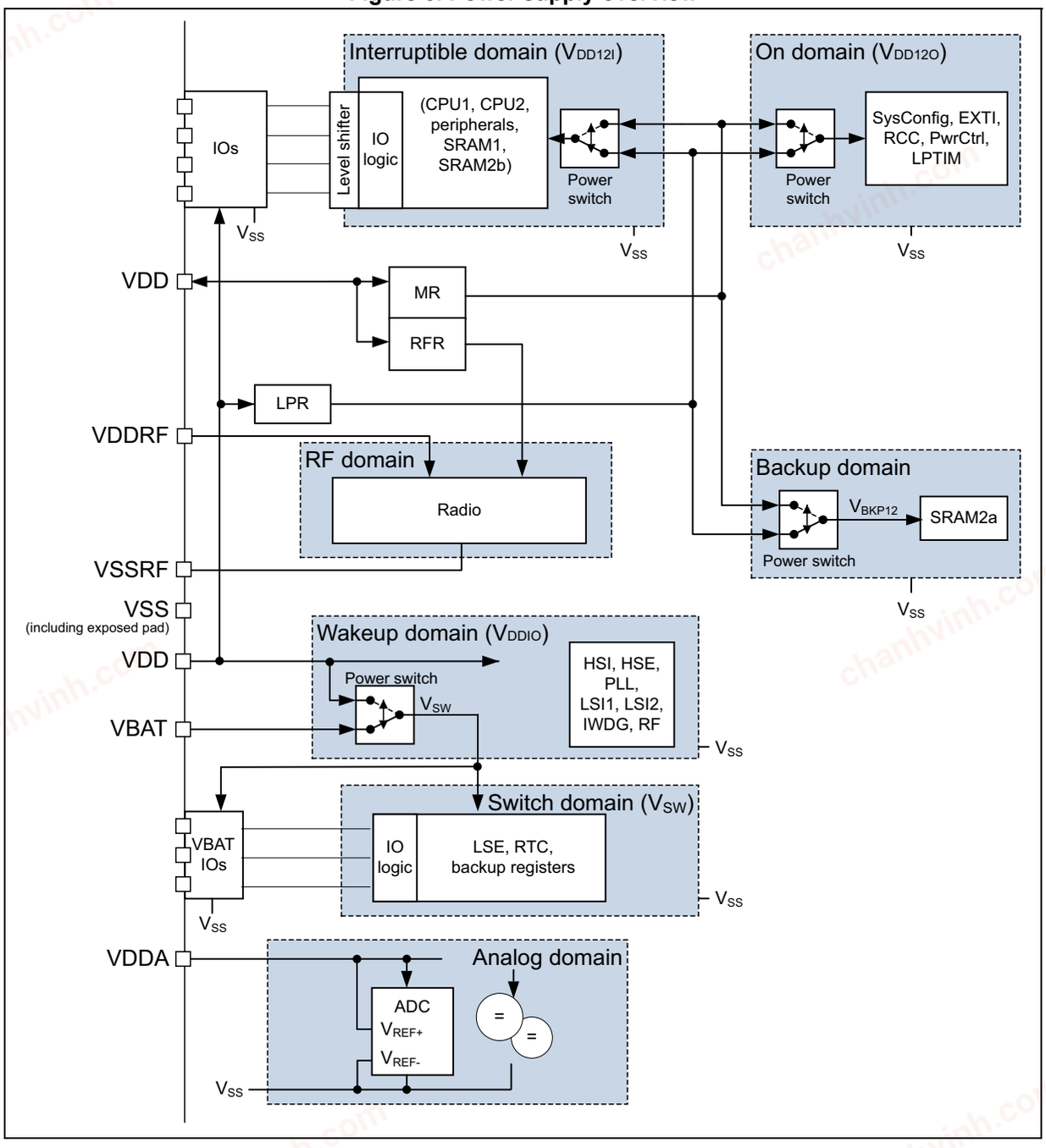
1. V_{DDX} refers to V_{DDA}.

During the power down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows the external decoupling capacitors to be discharged with different time constants during the power down transient phase.

Note: V_{DD} and V_{DDRF} must be wired together, so they can follow the same voltage sequence.

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Figure 6. Power supply overview



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3.7.2 Linear voltage regulator

Three embedded linear voltage regulators supply most of the digital and RF circuitries, the main regulator (MR), the low-power regulator (LPR) and the RF regulator (RFR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the SRAM2a in Standby with retention.
- The RFR is used to supply the RF analog part, its activity is automatically managed by the RF subsystem.

All the regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down, inducing zero consumption.

VCORE can also be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode. In this case the CPU is running at up to 2 MHz, and peripherals with independent clock can be clocked by HSI16 (in this mode the RF subsystem is not available).

3.7.3 Power supply supervisor

An integrated ultra-low-power brown-out reset (BOR) is active in all modes except Shutdown ensuring proper operation after power-on and during power down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 2.0 V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it with the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.7.4 Low-power modes

These ultra-low-power devices support several low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wake-up sources.

By default, the microcontroller is in Run mode, after a system or a power on reset. It is up to the user to select one of the low-power modes described below:

- **Sleep**

  In Sleep mode, only the CPU1 is stopped. All peripherals, including the RF subsystem, continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run**

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator operating current. The code can be executed from SRAM or from the flash memory, and the CPU1 frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16. The RF subsystem is not available in this mode and must be OFF.

- **Low-power sleep**

  This mode is entered from the low-power run mode. Only the CPU1 clock is stopped. When wake-up is triggered by an event or an interrupt, the system reverts to the

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low-power run mode. The RF subsystem is not available in this mode and must be OFF.

- **Stop 0, Stop 1 and Stop 2**

  Stop modes achieve the lowest power consumption while retaining the content of all the SRAM and registers. The LSE (or LSI) is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wake-up capability can enable the HSI16 RC during Stop modes to detect their wake-up condition.

  Three modes are available: Stop 0, Stop 1 and Stop 2. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wake-up sources, a smaller wake-up time but a higher consumption than Stop 2. In Stop 0 mode the main regulator remains ON, allowing a very fast wake-up time but with higher consumption.

  In these modes the RF subsystem can wait for incoming events in all Stop modes.

  The system clock when exiting from Stop 0, Stop1 or Stop2 modes can be either MSI up to 48 MHz or HSI16 if the RF subsystem is disabled. If the RF subsystem is used the exits must be set to HSI16 only.

- **Standby**

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off.

  The RTC can remain active (Standby mode with RTC).

  The brown-out reset (BOR) always remains active in Standby mode.

  The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1, SRAM2b and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2a can be retained in Standby mode, supplied by the low-power regulator (Standby with 32 KB SRAM2a retention mode).

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wake-up, timestamp, tamper) or a failure is detected on LSE (CSS on LSE, or from the RF system wake-up).

  The system clock after wake-up is 16 MHz, derived from the HSI16. In this mode the RF can be used.

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- **Shutdown**

  This mode achieves the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2a, SRAM2b and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wake-up, timestamp, tamper).

  The system clock after wake-up is 4 MHz, derived from the MSI.

  In this mode the RF is no longer operational.

When the RF subsystem is active, it changes the power state according to its needs (Run, Stop, Standby). This operation is transparent for the CPU1 host application and managed by a dedicated HW state machine. At any given time the effective power state reached is the higher one needed by both the CPU1 and RF sub-system.

Table 5 summarizes the peripheral features over all available modes. Wake-up capability is detailed in gray cells.

Table 5. Features over all modes(1)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
					-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
CPU1	Y	-	Y	-	-	-	-	-	-	-	-	-	-
CPU2	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Radio system (BLE, 802.15.4)	Y	Y	-	-	Y	Y	Y	Y	Y(2)	Y(2)			
Flash memory	Y(3)	Y	O(4)	O(4)	R	-	R	-	R	-	R	-	R
SRAM1	Y	Y(5)	Y	Y(5)	R	-	R	-	-	-	-	-	-
SRAM2a	Y	Y(5)	Y	Y(5)	R	-	R	-	R(6)	-	-	-	-
SRAM2b	Y	Y(5)	Y	Y(5)	R	-	R	-	-	-	-	-	-
Backup registers	Y	Y	Y	Y	R	-	R	-	R	-	R	-	R
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA1	O	O	O	O	-	-	-	-	-	-	-	-	-
High speed internal (HSI16)	O	O	O	O	O(7)	-	O(7)	-	-	-	-	-	-

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Table 5. Features over all modes[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
					-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)[8]	O	O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI1 or LSI2)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi speed internal (MSI)[9]	48	O	48	O	-	-	-	-	-	-	-	-	-
PLL VCO maximum frequency	344	O	-	-	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	O	O[10]	O	O[10]	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wake-up	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC tamper pins	1	1	1	1	1	O	1	O	1	O	1	O	1
USART1	O	O	O	O	O[11]	O[11]	-	-	-	-	-	-	-
I2C1	O	O	O	O	O[12]	O[12]	-	-	-	-	-	-	-
SPI1	O	O	O	O	-	-	-	-	-	-	-	-	-
ADC1	O	O	O	O	-	-	-	-	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers TIMx (x=1, 2, 16, 17)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power Timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power Timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
True random number generator (RNG)	O	O	-	-	-	-	-	-	-	-	-	-	-
AES2 hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
IPCC	O	-	O	-	-	-	-	-	-	-	-	-	-
HSEM	O	-	O	-	-	-	-	-	-	-	-	-	-

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Table 5. Features over all modes(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
					-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
PKA	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(13)	5 pins	(14)	5 pins	-

1. Legend: Y = Yes (enabled), O = Optional (disabled by default, can be enabled by software), R = Data retained, - = Not available.
2. Standby with SRAM2a Retention mode only. Stop2 is the deepest low power mode supported when RF is active. When the user application enters Standby mode, it must first stop all RF activities, and fully re-initialize the CPU2 when coming out of Standby mode. The application can use the full non secure SRAM2a to store its own content (to be retained in Standby mode).
3. Flash memory programming only possible in Run, not in Low Power Run.
4. The Flash memory can be configured in Power-down mode. By default, it is not in Power-down Run.
5. The SRAM clock can be gated on or off.
6. SRAM2a content is preserved when the bit RRS is set in PWR_CR3 register.
7. Some peripherals with wake-up from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
8. The HSE can be used by the RF subsystem according with the need to perform RF operation (Tx or Rx).
9. MSI maximum frequency.
10. In case RF will be used and HSE will fail.
11. UART reception is functional in Stop mode, and generates a wake-up interrupt on Start, address match or received frame event.
12. I2C address detection is functional in Stop mode, and generates a wake-up interrupt in case of address match.
13. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
14. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

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Table 6. STM32WB50CG and STM32WB30CE modes overview

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and peripherals	Wake-up source	Consumption(1)	Wake-up time
Run	MR	Yes	ON(2)	ON	Any	All	N/A	107 µA/MHz	N/A
LPRun	LPR	Yes	ON(2)	ON	Any except PLL	All except RF, RNG	N/A	103 µA/MHz	15.33 µs
Sleep	MR	No	ON(2)	ON(3)	Any	All	Any interrupt or event	41 µA/MHz	9 cycles
LPSleep	LPR	No	ON(2)	ON(3)	Any except PLL	All except RF, RNG	Any interrupt or event	45 µA/MHz	9 cycles
Stop 0	MR	No	OFF	ON	LSE, LSI, HSE(4), HSI16(5)	RF, BOR, PVD RTC, IWDG USART1(6) I2C1(7) LPTIMx (x=1, 2) All other peripherals are frozen.	Reset pin, all I/Os, RF, BOR, PVD RTC, IWDG USART1 I2C1 LPTIMx (x=1, 2)	105 µA	1.7 µs
Stop 1	LPR	No	OFF	ON	LSE, LSI, HSE(4), HSI16(5)	RF, BOR, PVD RTC, IWDG USART1(6) I2C1(7) LPTIMx (x=1, 2) All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD RTC, IWDG USART1 I2C1 LPTIMx (x=1, 2)	9.25 µA w/o RTC 9.45 µA w RTC	4.7 µs
Stop 2	LPR	No	OFF	ON	LSE, LSI	RF, BOR, PVD RTC, IWDG LPTIM1 All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD RTC, IWDG LPTIM1	1.85 µA w/o RTC 2.25 µA w RTC	5.71 µs

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Table 6. STM32WB50CG and STM32WB30CE modes overview (continued)

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and peripherals	Wake-up source	Consumption(1)	Wake-up time
Standby	LPR	No	OFF	SRAM2a ON(8)	LSE, LSI	RF, BOR, RTC, IWDG All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down	RF, Reset pin 2 I/Os (WKUPx)(9) BOR, RTC, IWDG	0.32 µA w/o RTC 0.60 µA w RTC	51 µs
	OFF			OFF				0.11 µA w/o RTC 0.39 µA w RTC	
Shutdown	OFF	No	OFF	OFF	LSE	RTC All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down(10)	2 I/Os (WKUPx)(9), RTC	0.028 µA w/o RTC 0.315 µA w/ RTC	-

1. Typical current at V_{DD} = 2.4 V, 25 °C. for STOPx, SHUTDOWN and Standby, else V_{DD} = 3.3 V, 25 °C.
2. The Flash memory controller can be placed in power-down mode if the RF subsystem is not in use and all the program is run from the SRAM.
3. The SRAM1 and SRAM2 clocks can be gated off independently.
4. HSE (32 MHz) automatically used when RF activity is needed by the RF subsystem.
5. HSI16 (16 MHz) automatically used by some peripherals.
6. U(S)ART reception is functional in Stop mode, and generates a wake-up interrupt on Start, Address match or Received frame event.
7. I2C address detection is functional in Stop mode, and generates a wake-up interrupt in case of address match.
8. SRAM1 and SRAM2b are OFF.
9. The I/Os with wake-up from Standby/Shutdown capability are: PA0, PA2.
10. I/Os can be configured with internal pull-up, pull-down or floating but the configuration is lost immediately when exiting the Shutdown mode.

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3.7.5 Reset mode

To improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.8 VBAT operation

The VBAT pin allows to power the device VBAT domain (RTC, LSE and Backup registers) from an external battery, an external supercapacitor, or from V_{DD} when no external battery nor an external supercapacitor are present. One anti-tamper detection pin is available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied only from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.9 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU1 resources and, consequently, reducing power supply consumption. In addition, these hardware connections result in fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run and Sleep, Stop 0, Stop 1 and Stop 2 modes.

Table 7. STM32WB50CG and STM32WB30CE CPU1 peripherals interconnect matrix

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADC1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
ADC	TIM1	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tamper	Y	Y	Y	Y	Y	Y(1)
All clock sources (internal and external)	TIM2 TIM16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-

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Table 7. STM32WB50CG and STM32WB30CE CPU1 peripherals interconnect matrix (continued)

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
CSS CPU (hard fault) SRAM (parity error) Flash memory (ECC error) PVD	TIM1 TIM16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y(1)
	ADC1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

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3.10 Clocks and startup

The STM32WB50CG and STM32WB30CE devices integrate several clock sources:

- LSE: 32.768 kHz external oscillator, for accurate RTC and calibration with other embedded RC oscillators
- LSI1: 32 kHz on-chip low-consumption RC oscillator
- LSI2: almost 32 kHz, on-chip high-stability RC oscillator, can be used by the RF subsystem instead of LSE
- HSE: high quality 32 MHz external oscillator with trimming, needed by the RF subsystem
- HSI16: 16 MHz high accuracy on-chip RC oscillator
- MSI: 100 kHz to 48 MHz multiple speed on-chip low power oscillator, can be trimmed using the LSE signal
- HSI48: 48 MHz on-chip RC oscillator

The clock controller (see *Figure 7*) distributes the clocks coming from the different oscillators to the core and the peripherals including the RF subsystem. It also manages clock gating for low power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. The MSI can supply a PLL.
  - System PLL that can be fed by HSE, HSI16 or MSI, with a maximum frequency of 64 MHz.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5%. The LSI source can be either the LSI1 or the LSI2 on-chip oscillator.
- **Peripheral clock sources:** Several peripherals (RNG, USARTs, I2C, LPTimers, ADC) have their own independent clock whatever the system clock. A PLL having three independent outputs for the highest flexibility can generate independent clocks for the ADC and the RNG.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application

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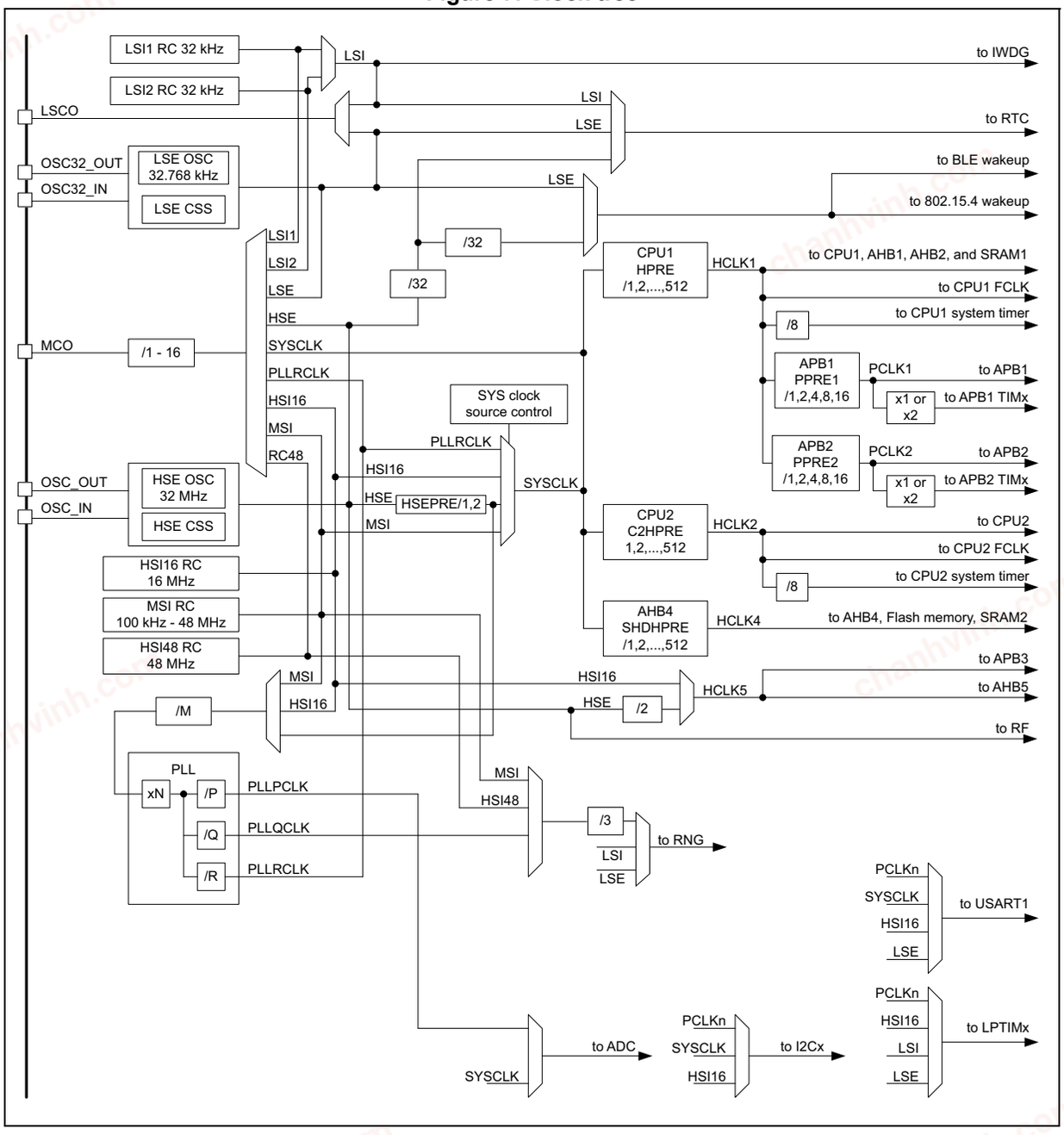
program as soon as the code execution starts.

- **Clock security system (CSS):** this feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software interrupt is generated if enabled. LSE failure can also be detected and an interrupt generated.
- Clock-out capability:
  - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSIx, LSE) are available down to Stop 1 low power state.
  - **LSCO (low-speed clock output):** it outputs LSI or LSE in all low-power modes down to Standby.

Several prescalers allow the user to configure the AHB frequencies, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 64 MHz.

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Figure 7. Clock tree



3.11 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked, if needed, following a specific sequence in order to avoid spurious writing to the I/Os registers.

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3.12 Direct memory access controller (DMA)

The device embeds one DMA. Refer to *Table 8* for the features implementation.

Direct memory access (DMA) is used to provide high-speed data transfer between peripherals and memory as well as between memories. Data can be quickly moved by DMA without any CPU action. This keeps CPU resources free for other operations.

The DMA controller has seven channels in total, a full cross matrix allows any peripheral to be mapped on any of the available DMA channels. The DMA has an arbiter for handling the priority between DMA requests.

The DMA supports:

- seven independently configurable channels (requests)
- A full cross matrix between peripherals and all the DMA channels exist. There is also a HW trigger possibility through the DMAMUX.
- Priorities between requests from DMA channels are software programmable (four levels consisting in very high, high, medium and low) or hardware in case of equality (request 1 has priority over request 2, etc.).
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management.
- Three event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically OR-ed together in a single interrupt request for each channel.
- Memory-to-memory transfer.
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers.
- Access to flash memory, SRAM, APB and AHB peripherals as source and destination.
- Programmable number of data to be transferred: up to 65536.

Table 8. DMA implementation

DMA features	DMA1
Number of regular channels	7

A DMAMUX block makes it possible to route any peripheral source to any DMA channel.

3.13 Interrupts and events

3.13.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 63 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

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The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.13.2 Extended interrupts and events controller (EXTI)

The EXTI manages wake-up through configurable and direct event inputs. It provides wake-up requests to the Power control, and generates interrupt requests to the CPUx NVIC and events to the CPUx event input.

Configurable events/interrupts come from peripherals able to generate a pulse, and make it possible to select the Event/Interrupt trigger edge and/or a SW trigger.

Direct events/interrupts are coming from peripherals having their own clearing mechanism.

3.14 Analog to digital converter (ADC)

The device embeds a successive approximation analog-to-digital converter with the following features:

- 12-bit native resolution, with built-in calibration
- Up to 16-bit resolution with 256 oversampling ratio
- 2.13 Msps maximum conversion rate with full resolution
  - Down to 78 ns sampling time
  - Increased conversion rate for lower resolution (up to 3.55 Msps for 6-bit resolution)
- Up to ten external channels and three internal channels: internal reference voltages, temperature sensor
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: two groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - The ADC supports multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into three data register or in SRAM with DMA controller support

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- Data pre-processing: left/right alignment and per channel offset compensation
- Built-in oversampling unit for enhanced SNR
- Channel-wise programmable sampling time
- Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
- Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 input channel, which is used to convert the sensor output voltage into a digital value.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored in the system memory area, accessible in read-only mode.

Table 9. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.14.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC. VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 10. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA} = 3.6 V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.15 True random number generator (RNG)

The devices embed a true RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

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3.16 Timers and watchdogs

The STM32WB50CG and STM32WB30CE include one advanced 16-bit timer, one general-purpose 32-bit timer, two 16-bit basic timers, two low-power timers, two watchdog timers and a SysTick timer. *Table 11* compares the features of the advanced control, general purpose and low power timers.

Table 11. Timer features

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16-bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM2	32-bits	Up, down, Up/down			4	No
General purpose	TIM16	16-bits	Up			2	1
General purpose	TIM17	16-bits	Up			2	1
Low power	LPTIM1 LPTIM2	16-bits	Up			1	1

3.16.1 Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 to 100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.16.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.16.2 General-purpose timers (TIM2, TIM16, TIM17)

There are up to three synchronizable general-purpose timers embedded in the STM32WB50CG and STM32WB30CE (see *Table 11* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2
  - Full-featured general-purpose timer

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  - Features four independent channels for input capture/output compare, PWM or one-pulse mode output. Can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.
  - The counter can be frozen in debug mode.
  - Independent DMA request generation, support of quadrature encoders.
- TIM16 and TIM17
  - General-purpose timers with mid-range features:
  - 16-bit auto-reload upcounters and 16-bit prescalers.
  - 1 channel and 1 complementary channel.
  - All channels can be used for input capture/output compare, PWM or one-pulse mode output.
  - The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.
  - The counters can be frozen in debug mode.

3.16.3 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers, having an independent clock running in Stop mode if they are clocked by LSE, LSIx or by an external clock. They are able to wake-up the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 modes.

The low-power timers support the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, either LSI1 or LSI2, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application)
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.16.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

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3.16.5 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- a maskable system interrupt generation when the counter reaches 0
- a programmable clock source.

3.17 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter, supporting the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- One anti-tamper detection pin with programmable filter.
- Timestamp feature, which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 20 backup registers are supplied through a switch that takes power either from the V_{DD} supply (when present) or from the VBAT pin.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- a 32.768 kHz external crystal (LSE)
- an external resonator or oscillator (LSE)
- one of the internal low power RC oscillators (LSI1 or LSI2, with typical frequency of 32 kHz)
- the high-speed external clock (HSE) divided by 32.

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The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by one of the LSIs, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (alarm, wake-up timer, timestamp or tamper) can generate an interrupt and wake-up the device from the low-power modes.

3.18 Inter-integrated circuit interface (I2C)

The devices embed one I2C. Refer to *Table 12* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 7: Clock tree*.
- Wake-up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 12. I2C implementation

I2C features(1)	I2C1
Standard-mode (up to 100 kbit/s)	X
Fast-mode (up to 400 kbit/s)	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X
Programmable analog and digital noise filters	X
SMBus/PMBus hardware support	X

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Table 12. I2C implementation (continued)

I2C features(1)	I2C1
Independent clock	X
Wake-up from Stop 0 / Stop 1 mode on address match	X
Wake-up from Stop 2 mode on address match	-

1. X: supported.

3.19 Universal synchronous/asynchronous receiver transmitter (USART)

The devices embed one universal synchronous receiver transmitter.

This interface provides asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and has LIN master/slave capability. It provides hardware management of the CTS and RTS signals, and RS485 driver enable.

The USART is able to communicate at speeds of up to 4 Mbit/s, and also provides Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

The USART supports synchronous operation (SPI mode), and can be used as an SPI master.

The USART has a clock domain independent from the CPU clock, allowing it to wake up the MCU from Stop mode using baudrates up to 200 kbaud. The wake up events from Stop mode are programmable and can be:

- the start bit detection
- any received data frame
- a specific programmed data frame.

The USART interface can be served by the DMA controller.

3.20 Serial peripheral interface (SPI1)

The SPI interface enables communication up to 32 Mbit/s in master and up to 24 Mbit/s in slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interface supports NSS pulse mode, TI mode and Hardware CRC calculation.

The SPI interface can be served by the DMA controller.

3.21 Development support

3.21.1 Serial wire JTAG debug port (SWJ-DP)

The embedded Arm® SWJ-DP interface is a combined JTAG and serial wire debug port that enables either a serial wire debug, or a JTAG probe to be connected to the target.

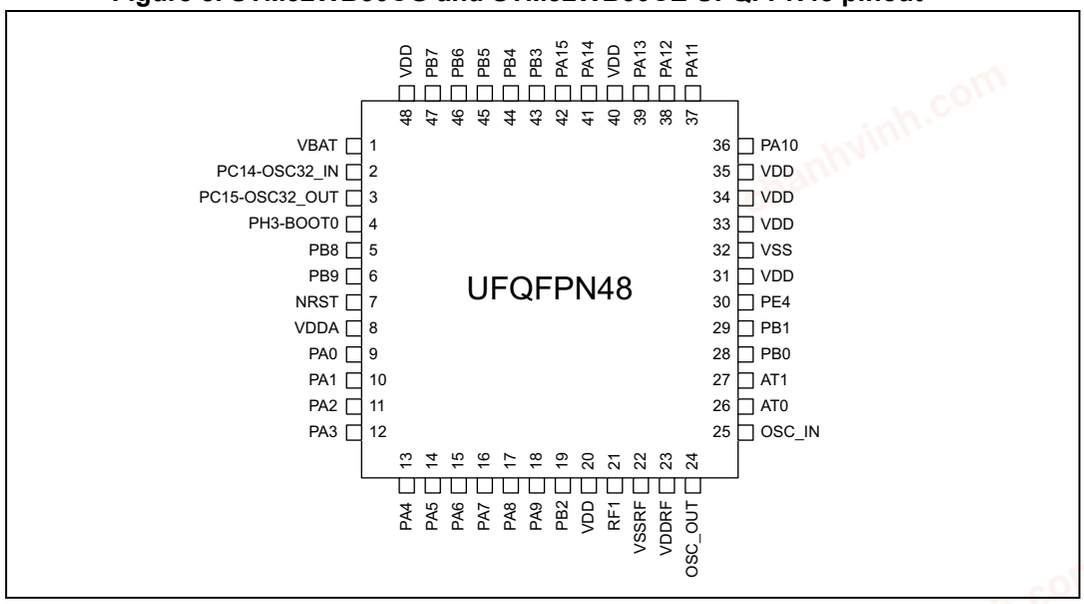
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Debug is performed using only two pins instead of the five required by the JTAG (JTAG pins can then be reused as GPIOs with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

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4 Pinouts and pin description

Figure 8. STM32WB50CG and STM32WB30CE UFQFPN48 pinout(1)(2)



1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Table 13. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RF	RF I/O
		RST	Bidirectional reset pin with weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_a(2)	I/O, with Analog switch function supplied by V_{DDA}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 14* are: FT_f, FT_fa.

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2. The related I/O structures in *Table 14* are: FT_a, FT_fa, TT_a.

Table 14. STM32WB50CG and STM32WB30CE pin and ball definitions

Pin (UFQFPN48)		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
1	VBAT	S	-	-	-	-
2	PC14-OSC32_IN	I/O	FT	(1)(2)	CM4_EVENTOUT	OSC32_IN
3	PC15-OSC32_OUT	I/O	FT	(1)(2)	CM4_EVENTOUT	OSC32_OUT
4	PH3-BOOT0	I/O	FT	-	CM4_EVENTOUT, LSCO(3)	-
5	PB8	I/O	FT_f	-	TIM1_CH2N, I2C1_SCL, TIM16_CH1, CM4_EVENTOUT	-
6	PB9	I/O	FT_fa	-	TIM1_CH3N, I2C1_SDA, IR_OUT, TIM17_CH1, CM4_EVENTOUT	-
7	NRST	I/O	RST	-	-	-
8	VDDA	S	-	(4)	-	-
9	PA0	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, CM4_EVENTOUT	ADC1_IN5, RTC_TAMP2/WKUP1
10	PA1	I/O	FT_a	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, CM4_EVENTOUT	ADC1_IN6
11	PA2	I/O	FT_a	-	LSCO(3), TIM2_CH3, CM4_EVENTOUT	ADC1_IN7, WKUP4
12	PA3	I/O	FT_a	-	TIM2_CH4, CM4_EVENTOUT	ADC1_IN8
13	PA4	I/O	FT_a	-	SPI1_NSS, LPTIM2_OUT, CM4_EVENTOUT	ADC1_IN9
14	PA5	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, CM4_EVENTOUT	ADC1_IN10
15	PA6	I/O	FT_a	-	TIM1_BKIN, SPI1_MISO, TIM16_CH1, CM4_EVENTOUT	ADC1_IN11
16	PA7	I/O	FT_fa	-	TIM1_CH1N, SPI1_MOSI, TIM17_CH1, CM4_EVENTOUT	ADC1_IN12
17	PA8	I/O	FT_a	-	MCO, TIM1_CH1, USART1_CK, LPTIM2_OUT, CM4_EVENTOUT	ADC1_IN15
18	PA9	I/O	FT_fa	-	TIM1_CH2, I2C1_SCL, USART1_TX, CM4_EVENTOUT	ADC1_IN16
19	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, SPI1_NSS, CM4_EVENTOUT	-
20	VDD	S	-	-	-	-
21	RF1	I/O	RF	(5)	-	-
22	VSSRF	S	-	-	-	-
23	VDDRF	S	-	-	-	-

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Table 14. STM32WB50CG and STM32WB30CE pin and ball definitions (continued)

Pin (UFQFPN48)		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
24	OSC_OUT	O	RF	(6)	-	-
25	OSC_IN	I	RF	(6)	-	-
26	AT0	O	RF	(7)	-	-
27	AT1	O	RF	(7)	-	-
28	PB0	I/O	TT	(8)	CM4_EVENTOUT, RF_TX_MOD_EXT_PA	-
29	PB1	I/O	TT	(8)	LPTIM2_IN1, CM4_EVENTOUT	-
30	PE4	I/O	FT	-	CM4_EVENTOUT	-
31	VDD	S	-	-	-	-
32	VSS	S	-	-	-	-
33	VDD	S	-	-	-	-
34	VDD	S	-	-	-	-
35	VDD	S	-	-	-	-
36	PA10	I/O	FT_f	-	TIM1_CH3, I2C1_SDA, USART1_RX, TIM17_BKIN, CM4_EVENTOUT	-
37	PA11	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, CM4_EVENTOUT	-
38	PA12	I/O	FT	-	TIM1_ETR, SPI1_MOSI, USART1_RTS, CM4_EVENTOUT	-
39	PA13(JTMS_SWDIO)	I/O	FT	(9)	JTMS-SWDIO, IR_OUT, CM4_EVENTOUT	-
40	VDD	S	-	-	-	-
41	PA14 (JTCK_SWCLK)	I/O	FT	(9)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, CM4_EVENTOUT	-
42	PA15 (JTDI)	I/O	FT	(9)	JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS, CM4_EVENTOUT, MCO	-
43	PB3 (JTDO)	I/O	FT_a	-	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, USART1_RTS, CM4_EVENTOUT	-
44	PB4 (NJTRST)	I/O	FT_a	(9)	NJTRST, SPI1_MISO, USART1_CTS, TIM17_BKIN, CM4_EVENTOUT	-
45	PB5	I/O	FT	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, USART1_CK, TIM16_BKIN, CM4_EVENTOUT	-
46	PB6	I/O	FT_fa	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, TIM16_CH1N, MCO, CM4_EVENTOUT	-

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Table 14. STM32WB50CG and STM32WB30CE pin and ball definitions (continued)

Pin (UFQFPN48)		Pin type	I/O structures	Notes	Alternate functions	Additional functions
Number	Name (function after reset)					
47	PB7	I/O	FT_fa	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TIM17_CH1N, CM4_EVENTOUT	PVD_IN
48	VDD	S	-	-	-	-

1. PC14 and PC15 are supplied through the power switch. As this switch only sinks a limited amount of current (3 mA), the use of the PC14 and PC15 GPIOs in output mode is limited:
   - the speed must not exceed 2 MHz with a maximum load of 30 pF
   - these GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the reference manual RM0471, available on *www.st.com*.
3. The clock on LSCO is available in Run, Stop, and on PA2 in Standby and Shutdown modes.
4. On UFQFPN48 VDDA is connected to V_{REF+}.
5. RF pin, use the nominal PCB layout.
6. 32 MHz oscillator pins, use the nominal PCB layout according to reference design (see AN5165).
7. Reserved for production, must be kept unconnected.
8. High frequency (above 32 KHz) may impact the RF performance. Set output speed GPIOB_OSPEEDRy[1:0] to 00 (y = 0 and 1) during RF operation.
9. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13 and PB4 pins and the internal pull-down on PA14 pin are activated.

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Table 15. Alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF12	AF11	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	TIM1	I2C1	SPI1	RF	USART1	IR	TIM1	-	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
A	PA0	-	TIM2_CH1	-	-	-	-	-	-	-	-	-	TIM2_ETR	CM4_ EVENTOUT
	PA1	-	TIM2_CH2	-	-	I2C1_SMBA	SPI1_SCK	-	-	-	-	-	-	CM4_ EVENTOUT
	PA2	LSCO	TIM2_CH3	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PA3	-	TIM2_CH4	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	-	-	-	-	-	LPTIM2_OUT	CM4_ EVENTOUT
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	-	-	-	-	LPTIM2_ETR	CM4_ EVENTOUT
	PA6	-	TIM1_BKIN	-	-	-	SPI1_MISO	-	-	-	TIM1_BKIN	-	TIM16_CH1	CM4_ EVENTOUT
	PA7	-	TIM1_CH1N	-	-	-	SPI1_MOSI	-	-	-	-	-	TIM17_CH1	CM4_ EVENTOUT
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK	-	-	-	LPTIM2_OUT	CM4_ EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C1_SCL	-	-	USART1_TX	-	-	-	-	CM4_ EVENTOUT
	PA10	-	TIM1_CH3	-	-	I2C1_SDA	-	-	USART1_RX	-	-	-	TIM17_BKIN	CM4_ EVENTOUT
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS	-	TIM1_BKIN2	-	-	CM4_ EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS	-	-	-	-	CM4_ EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	IR_OUT	-	-	-	CM4_ EVENTOUT
	PA14	JTCK-SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	-	SPI1_NSS	MCO	-	-	-	-	-	CM4_ EVENTOUT

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Table 15. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF12	AF11	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	TIM1	I2C1	SPI1	RF	USART1	IR	TIM1	-	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
B	PB0	-	-	-	-	-	-	RF_TX_ MOD_EXT_PA	-	-	-	-	-	CM4_ EVENTOUT
	PB1	-	-	-	-	-	-	-	-	-	-	-	LPTIM2_IN1	CM4_ EVENTOUT
	PB2	RTC_ OUT	LPTIM1_OUT	-	-	-	SPI1_NSS	-	-	-	-	-	-	CM4_ EVENTOUT
	PB3	JTDO-TRACE SWO	TIM2_CH2	-	-	-	SPI1_SCK	-	USART1_RTS	-	-	-	-	CM4_ EVENTOUT
	PB4	NJTRST	-	-	-	-	SPI1_MISO	-	USART1_CTS	-	-	-	TIM17_BKIN	CM4_ EVENTOUT
	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	-	USART1_CK	-	-	-	TIM16_BKIN	CM4_ EVENTOUT
	PB6	MCO	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX	-	-	-	TIM16_CH1N	CM4_ EVENTOUT
	PB7	-	LPTIM1_IN2	-	TIM1_BKIN	I2C1_SDA	-	-	USART1_RX	-	-	-	TIM17_CH1N	CM4_ EVENTOUT
	PB8	-	TIM1_CH2N	-	-	I2C1_SCL	-	-	-	-	-	-	TIM16_CH1	CM4_ EVENTOUT
	PB9	-	TIM1_CH3N	-	-	I2C1_SDA	-	-	-	IR_OUT	-	-	TIM17_CH1	CM4_ EVENTOUT
C	PC14	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
E	PE4	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
H	PH3	LSCO	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT

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5 Memory mapping

The STM32WB50CG and STM32WB30CE devices feature a single physical address space that can be accessed by the application processor and by the RF subsystem.

A part of the Flash memory and of the SRAM2a and SRAM2b memories are made secure, exclusively accessible by the CPU2, protected against execution, read and write from CPU1 and DMA.

In case of shared resources the SW should implement arbitration mechanism to avoid access conflicts. This happens for peripherals Reset and clock controller (RCC), Power controller (PWC), EXTI and Flash interface, and can be implemented using the built-in semaphore block (HSEM).

By default the RF subsystem and CPU2 operate in secure mode. This implies that part of the Flash and of the SRAM2 memories can only be accessed by the RF subsystem and by the CPU2. In this case the Host processor (CPU1) has no access to these resources.

The detailed memory map and the peripheral mapping of the devices can be found in the reference manual RM0471.

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6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on V_{DD} = V_{DDA} = V_{DDRF} = 3 V, T_A = 25 °C. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

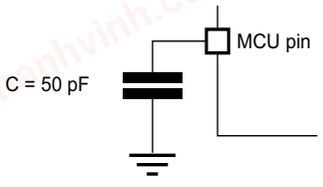
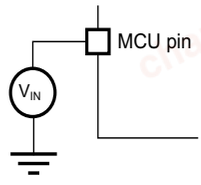


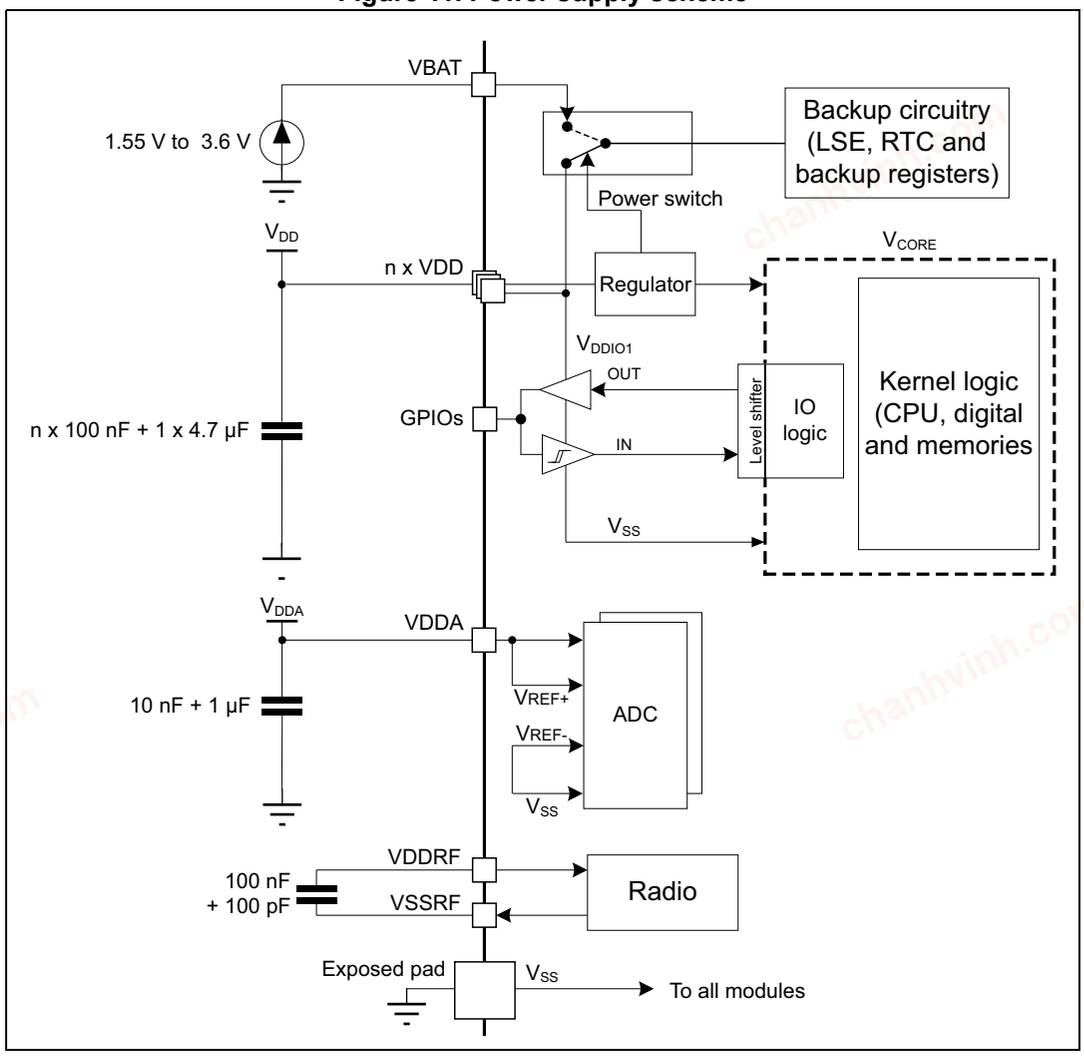
Figure 10. Pin input voltage



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6.1.6 Power supply scheme

Figure 11. Power supply scheme

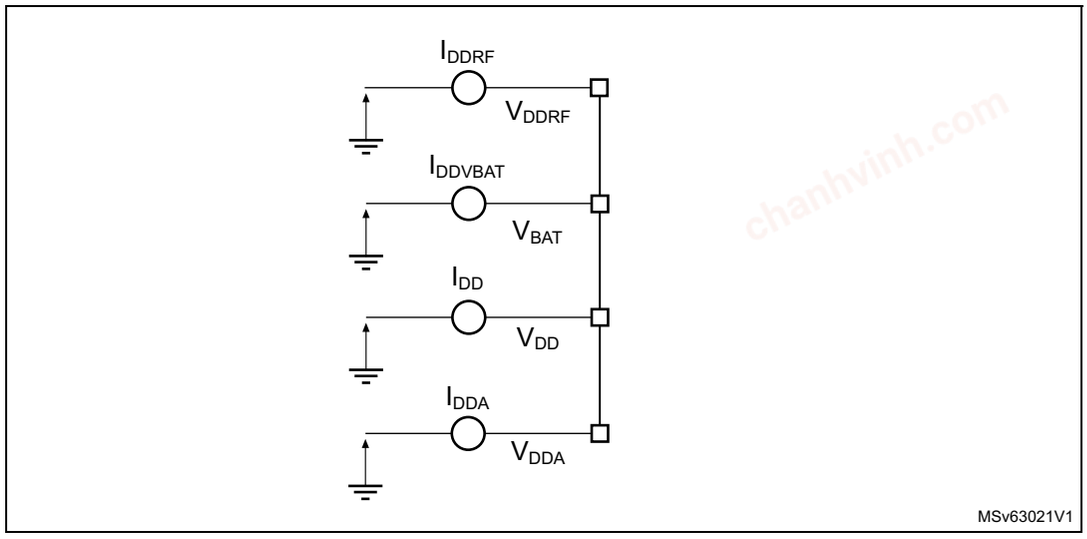


Caution: Each power supply pair (such as V_{DD} / V_{SS}, V_{DDA} / V_{SS}) must be decoupled with filtering ceramic capacitors as shown in *Figure 11*. These capacitors must be placed as close as possible to (or below) the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

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6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 16*, *Table 17* and *Table 18* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 16. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDRF}, V_{BAT})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDRF}) + 4.0(3)(4)	
	Input voltage on TT_xx pins		4.0	
	Input voltage on any other pin		4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	

1. All main power (VDD, VDDRF, VDDA, VBAT) and ground (VSS) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 17* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.

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Table 17. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	130	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	130	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, RST and B pins, except PB0 and PB1	–5 / +0(4)	
	Injected current on PB0 and PB1	-5/0	
$\sum\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(5)	25	

1. All main power (VDD, VDDRF, VDDA, VBAT) and ground (VSS) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count packages.
3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 16* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	110	

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6.3 Operating conditions

6.3.1 Summary of main performance

Table 19. Main performance at V_{DD} = 3.3 V

Parameter			Test conditions	Typ	Unit
I_{CORE}	Core current consumption		VBAT (V_{BAT} = 1.8 V, V_{DD} = 0 V)	0.002	µA
			Shutdown (V_{DD} = 2.0 V)	0.014	
			Standby (V_{DD} = 2.0 V, 32 KB SRAM2a retention)	0.35	
			Stop2	1.85	
			Sleep (16 MHz)	845	
			LP run (2 MHz)	320	
			Run (64 MHz)	8150	
			Radio RX(1)	7900	
			Radio TX 0 dBm output power(1)	8800	
I_{PERI}	Peripheral current consumption	BLE	Advertising with Stop2(2) (Tx = 0 dBm; Period 1.28 s; 31 bytes, 3 channels)	20	
			Advertising with Stop2(2) (Tx = 0 dBm, 6 bytes; period 10.24 s, 3 channels)	4	
		LP timers	-	6	
		RTC	-	2.5	

1. Power consumption including RF subsystem and digital processing.
2. Power consumption averaged over 100 s including Cortex M4, RF subsystem, digital processing and Cortex M0+.

6.3.2 General operating conditions

Table 20. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	64	
f_{PCLK2}	Internal APB2 clock frequency	-	0	64	
V_{DD}	Standard operating voltage	-	2.0(1)	3.6	V
V_{DDA}	Analog supply voltage	ADC used	2.0	3.6	
		ADC not used(2)	2.0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	
V_{DDRF}	Minimum RF voltage	-	2.0	3.6	V
V_{IN}	I/O input voltage	TT_xx I/O	–0.3	V_{DD} + 0.3	
		All I/O except TT_xx	–0.3	min (min (V_{DD}, V_{DDA}) + 3.6 V, 5.5 V)(3)(4)	

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Table 20. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 5	UFQFPN48	-	803	mW
T_A	Ambient temperature	Maximum power dissipation	–10	85	°C
		Low-power dissipation(5)		105	
T_J	Junction temperature range	-	–10	105	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. When not used, VDDA must be connected to VDD.
3. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}) + 3.6 V and 5.5V.
4. For operation with voltage higher than min (V_{DD}, V_{DDA}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled.
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Section 7.3: Thermal characteristics*).

6.3.3 RF BLE characteristics

Table 21. RF transmitter BLE characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{op}	Frequency operating range	-	2402	-	2480	MHz
F_{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	250	-	kHz
Rgfsk	On air data rate	-	-	1	-	Mbps
PLLres	RF channel spacing	-	-	2	-	MHz

Table 22. RF transmitter BLE characteristics (1 Mbps)(1)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
P_{rf}	Maximum output power		-	-	4.0	-	dBm
	0 dBm output power		-	-	0	-	
	Minimum output power		-	-	-20	-	
P_{band}	Output power variation over the band		Tx = 0 dBm - Typical	-0.5	-	0.4	dB
BW6dB	6 dB signal bandwidth		Tx = Maximum output power	-	670	-	kHz
IBSE	In band spurious emission	2 MHz	Bluetooth® Low Energy:-20 dBm	-	-50	-	dBm
		≥ 3 MHz	Bluetooth® Low Energy: -30 dBm	-	-53	-	
f_d	Frequency drift		Bluetooth® Low Energy: ±50 kHz	-50	-	+50	kHz
maxdr	Maximum drift rate		Bluetooth® Low Energy: ±20 kHz / 50 µs	-20	-	+20	kHz/ 50 µs

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Table 22. RF transmitter BLE characteristics (1 Mbps)(1) (continued)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
fo	Frequency offset		Bluetooth® Low Energy: ±150 kHz	-150	-	+150	kHz
Δf1	Frequency deviation average		Bluetooth® Low Energy: between 225 and 275 kHz	225	-	275	
Δfa	Frequency deviation Δf2 (average) / Δf1 (average)		Bluetooth® Low Energy:> 0.80	0.80	-	-	-
OBSE(2)	Out of band spurious emission	< 1 GHz	-	-	-61	-	dBm
		≥ 1 GHz	-	-	-46	-	

1. :Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

Table 23. RF receiver BLE characteristics (1 Mbps)

Symbol	Parameter	Test conditions	Typ	Unit
Prx_max	Maximum input signal	PER <30.8% Bluetooth® Low Energy: min -10 dBm	0	dBm
Psens(1)	High sensitivity mode	PER <30.8% Bluetooth® Low Energy: max -70 dBm	-96	
$Rssi_{maxrange}$	RSSI maximum value	-	-7	
$Rssi_{minrange}$	RSSI minimum value	-	-94	
$Rssi_{accu}$	RSSI accuracy	-	2	dB
C/Ico	Co-channel rejection	Bluetooth® Low Energy: 21 dB	8	

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Table 23. RF receiver BLE characteristics (1 Mbps) (continued)

Symbol	Parameter	Test conditions	Typ	Unit
C/I	Adjacent channel interference	Adj ≥ 5 MHz Bluetooth® Low Energy: -27 dB	-53	dB
		Adj ≤ -5 MHz Bluetooth® Low Energy:-27 dB	-53	
		Adj = 4 MHz Bluetooth® Low Energy:-27 dB	-48	
		Adj = -4 MHz Bluetooth® Low Energy:-15 dB	-33	
		Adj = 3 MHz Bluetooth® Low Energy:-27 dB	-46	
		Adj = 2 MHz Bluetooth® Low Energy:-17 dB	-39	
		Adj = -2 MHz Bluetooth® Low Energy:-15 dB	-35	
		Adj = 1 MHz Bluetooth® Low Energy: 15 dB	-2	
		Adj = -1 MHz Bluetooth® Low Energy: 15 dB	2	
C/Image	Image rejection (F_{image} = -3 MHz)	Bluetooth® Low Energy: -9 dB	-29	
P_IMD	Intermodulation	|f2-f1| = 3 MHz Bluetooth® Low Energy: -50 dBm	-34	dBm
		|f2-f1| = 4 MHz Bluetooth® Low Energy: -50 dBm	-30	
		|f2-f1| = 5 MHz Bluetooth® Low Energy:-50 dBm	-32	
P_OBB	Out of band blocking	30 to 2000 MHz Bluetooth® Low Energy: -30 dBm	-3	
		2003 to 2399 MHz Bluetooth® Low Energy: -35 dBm	-5	
		2484 to 2997 MHz Bluetooth® Low Energy: -35 dBm	-2	
		3 to 12.75 GHz Bluetooth® Low Energy: -30 dBm	7	

1. With ideal TX.

Table 24. RF BLE power consumption for V_{DD} = 3.3 V(1)

Symbol	Parameter	Typ	Unit
I_{txmax}	TX maximum output power consumption	12	mA
I_{tx0dbm}	TX 0 dBm output power consumption	8.8	
I_{rxlo}	Rx consumption	7.9	

1. Power consumption including RF subsystem and digital processing.

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6.3.4 RF 802.15.4 characteristics

Table 25. RF transmitter 802.15.4 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{op}	Frequency operating range	-	2405	-	2480	MHz
F_{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	5	-	
Roqpsk	On Air data rate	-	-	250	-	Kbps
PLLres	RF channel spacing	-	-	5	-	MHz
Prf	Maximum output power(1)	-	-	4	-	dBm
	0 dBm output power	-	-	0	-	
	Minimum output power	-	-	-20	-	
Pband	Output power variation over the band	Tx = 0 dBm - Typical	-0.5	-	0.4	dB
EVMrms	EVM rms	Pmax	-	8	-	%
Txpd	Transmit power density	|f - fc| > 3.5 MHz	-	-35	-	dB

1. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 26. RF receiver 802.15.4 characteristics

Symbol	Parameter	Conditions	Typ	Unit
Prx_max	Maximum input signal	PER < 1%	-10	dBm
Rsens	Sensitivity		-100	
C/adj	Adjacent channel rejection	-	35	dB
C/alt	Alternate channel rejection	-	46	

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Figure 13. Typical link quality indicator code vs. Rx level

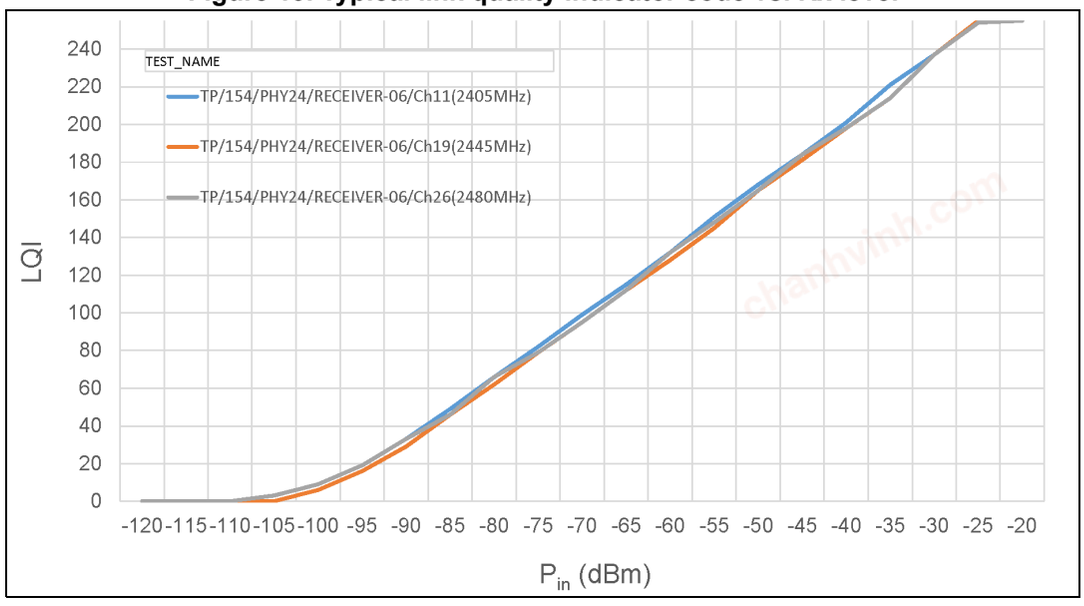


Figure 14. Typical energy detection (T = 27°C, V_{DD} = 3.3 V)

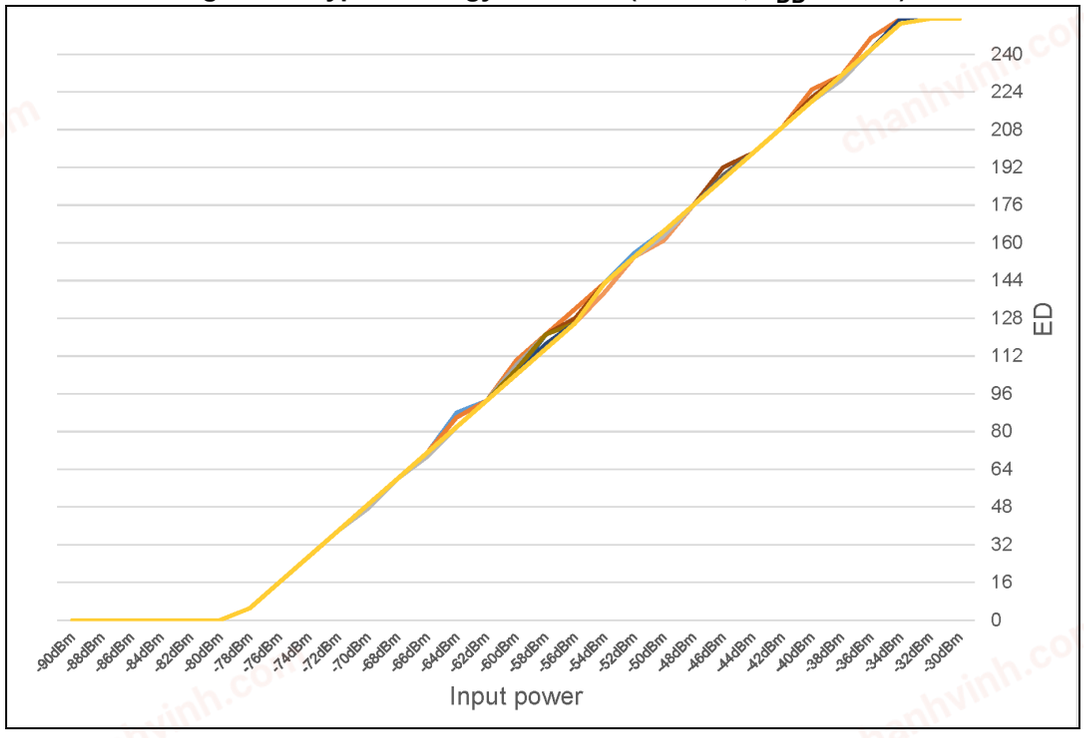


Table 27. RF 802.15.4 power consumption for V_{DD} = 3.3 V(1)

Symbol	Parameter	Typ	Unit
I_{txmax}	TX maximum output power consumption	10.7	mA
I_{tx0dbm}	TX 0 dBm output power consumption	9.1	
I_{rxlo}	Rx consumption	9.2	

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1. Power consumption including RF subsystem and digital processing.

6.3.5 Operating conditions at power-up / power-down

The parameters given in *Table 28* are derived from tests performed under the ambient temperature condition summarized in *Table 20*.

Table 28. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	-	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		10	∞	
t_{VDDRF}	V_{DDRF} rise time rate	-	-	∞	
	V_{DDRF} fall time rate		-	∞	

6.3.6 Embedded reset and power control block characteristics

The parameters given in *Table 29* are derived from tests performed under the ambient temperature conditions summarized in *Table 20: General operating conditions*.

Table 29. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.70	V
		Falling edge	1.60	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.10	2.14	
		Falling edge	1.96	2.00	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.10	2.15	2.19	
		Falling edge	2.00	2.05	2.10	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	
		Falling edge	2.31	2.36	2.41	

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Table 29. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

6.3.7 Embedded voltage reference

The parameters given in *Table 30* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 30. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–10 °C < T_A < +85 °C	1.182	1.212	1.232	V
$t_{S_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4[2]	-	-	µs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12[2]	
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20[2]	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5[2]	mV
T_{Coeff}	Temperature coefficient	–10 °C < T_A < +85 °C	-	30	50[2]	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25 °C	-	300	1000[2]	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200[2]	ppm/V

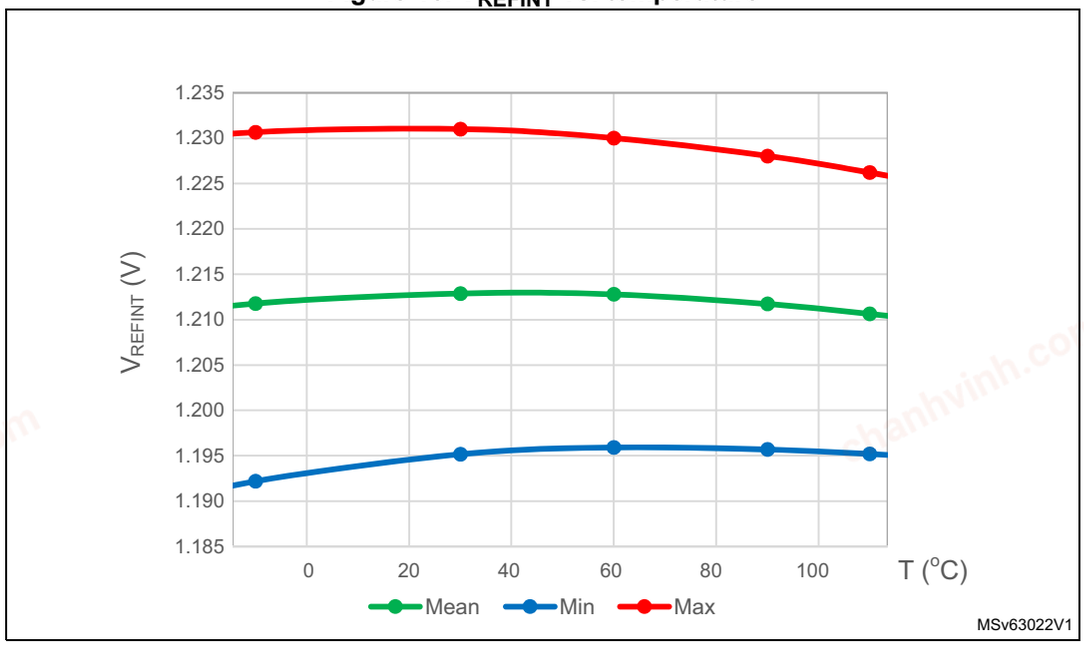
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Table 30. Embedded internal voltage reference (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 15. V_{REFINT} vs. temperature



6.3.8 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as shown in *Figure 12: Current consumption measurement scheme*.

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Typical and maximum current consumption

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0471 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- For flash memory and shared peripherals $f_{PCLK} = f_{HCLK} = f_{HCLKS}$

The parameters given in *Table 31* to *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 31. Current consumption in Run and Low-power run modes, code with data processing running from flash, ART enable (Cache ON Prefetch OFF), V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ			Max(1)		Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	25 °C	85 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE} = 32$ MHz f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	64 MHz	8.15	8.25	8.40	9.30	9.60	mA
			32 MHz	4.20	4.25	4.40	4.25	4.63	
			16 MHz	2.25	2.30	2.40	2.65	2.91	
I_{DD}(LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	2 MHz	0.335	0.360	0.470	0.480	0.910	
			1 MHz	0.170	0.210	0.325	0.270	0.730	
			400 kHz	0.0815	0.120	0.230	0.140	0.590	
			100 kHz	0.0415	0.076	0.190	0.070	0.550	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 32. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ			Max(1)		Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	25 °C	85 °C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSI16} up to 16 MHz included, f_{HCLK} = f_{HSE} = 32 MHz f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	64 MHz	8.80	8.90	9.00	10.50	10.80	mA
			32 MHz	4.50	4.55	4.70	4.63	4.89	
			16 MHz	2.40	2.40	2.55	2.50	2.70	
I_{DD}(LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} All peripherals disabled	2 MHz	0.265	0.285	0.385	0.440	0.940	
			1 MHz	0.135	0.170	0.270	0.290	0.760	
			400 kHz	0.066	0.097	0.195	0.200	0.670	
			100 kHz	0.031	0.0625	0.160	0.170	0.470	

1. Guaranteed by characterization results, unless otherwise specified.

Table 33. Typical current consumption in Run and Low-power run modes, with different codes running from flash, ART enable (Cache ON Prefetch OFF), V_{DD} = 3.3 V

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Frequency	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSI16} up to 16 MHz included, f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	f_{HCLK} = 64 MHz	Reduced code(1)	8.15	mA	127	µA/MHz
				Coremark	8.00		125	
				Dhrystone 2.1	8.10		127	
				Fibonacci	7.60		119	
				While(1)	6.85		107	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz All peripherals disabled		Reduced code(1)	320	µA	160	
				Coremark	350		175	
				Dhrystone 2.1	350		175	
				Fibonacci	390		195	
				While(1)	225		113	

1. Reduced code used for characterization results provided in *Table 31* and *Table 32*.

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Table 34. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, V_{DD} = 3.3 V

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Frequency	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, f_{HSI16} + PLL ON above 32 MHz All peripherals disable	f_{HCLK} = 64 MHz	Reduced code(1)	8.80	mA	138	µA/MHz
				Coremark	7.50		117	
				Dhrystone 2.1	8.60		134	
				Fibonacci	7.90		123	
				While(1)	8.00		125	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz All peripherals disable		Reduced code(1)	255	µA	128	
				Coremark	205		103	
				Dhrystone 2.1	250		125	
				Fibonacci	230		115	
				While(1)	220		110	

1. Reduced code used for characterization results provided in *Table 31* and *Table 32*.

Table 35. Current consumption in Sleep and Low-power sleep modes, flash memory ON

Symbol	Parameter	Conditions		TYP			MAX(1)		Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	25 °C	85 °C	
I_{DD}(Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE}$ up to 32 MHz f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	64 MHz	2.65	2.70	2.80	3.00	3.33	mA
			32 MHz	1.40	1.45	1.60	1.55	1.86	
			16 MHz	0.845	0.875	0.990	0.970	1.40	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	2 MHz	0.090	0.125	0.235	0.130	0.600	
			1 MHz	0.058	0.093	0.205	0.090	0.570	
			400 kHz	0.044	0.0725	0.185	0.070	0.540	
			100 kHz	0.0315	0.0635	0.0175	0.055	0.530	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 36. Current consumption in Low-power sleep modes, flash memory in Power down

Symbol	Parameter	Conditions		TYP			MAX(1)		Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	25 °C	85 °C	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	2 MHz	94.0	115	200	135	610	µA
			1 MHz	56.5	86.0	170	94.2	560	
			400 kHz	40.5	66.5	150	68.0	540	
			100 kHz	27.5	57.5	140	54.6	539	

1. Guaranteed by characterization results, unless otherwise specified.

Table 37. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX(1)			Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	0 °C	25 °C	85 °C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	BLE disabled	2.4 V	1.10	1.85	3.20	6.00	22.0	-	-	-	µA
			3.0 V	1.10	1.85	3.25	6.10	22.0	1.60	4.17	57.9	
			3.6 V	1.15	1.95	3.35	6.25	23.0	1.69	4.40	58.6	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled, BLE disabled	RTC clocked by LSI	2.4 V	1.45	2.25	3.55	6.40	22.5	-	-	-	
			3.0 V	1.50	2.30	3.70	6.55	22.5	2.11	4.64	58.3	
			3.6 V	1.75	2.50	3.95	6.85	23.5	2.26	5.12	59.7	
		RTC clocked by LSE quartz(2) in low drive mode	2.4 V	1.45	2.25	3.65	6.40	22.5	-	-	-	
			3.0 V	1.55	2.45	3.80	6.65	23.0	2.01	4.31	58.0	
			3.6 V	1.70	2.55	4.05	6.95	23.5	2.16	4.40	81.6	
I_{DD} (wake-up from Stop 2)	Supply current during wake-up from Stop 2 mode bypass mode	Wake-up clock is MSI = 32 MHz. See(3).	3.0 V	-	320	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wake-up with code execution from flash memory. Average value given for a typical wake-up time as specified in *Table 45*.

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Table 38. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX(1)			Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	0 °C	25 °C	85 °C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	BLE disabled	2.4 V	5.10	9.25	15.5	28.5	96.5	-	-	-	µA
			3.0 V	5.15	9.30	15.5	28.5	97.0	7.07	28.5	346.8	
			3.6 V	5.25	9.45	16.0	29.0	97.5	7.30	28.8	351.0	
I_{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC enabled, BLE disabled	RTC clocked by LSI	2.4 V	5.40	9.45	16.0	28.5	97.0	-	-	-	
			3.0 V	5.70	9.55	16.5	29.0	98.5	7.69	29.7	347.2	
			3.6 V	5.85	10.0	16.5	29.5	96.5	8.08	29.8	349.9	
		RTC clocked by LSE quartz(2) in Low drive mode	2.4 V	5.40	9.70	16.0	29.0	96.5	-	-	-	
			3.0 V	5.75	9.70	16.0	29.0	97.5	7.40	28.9	346.6	
			3.6 V	5.90	10.0	16.5	29.5	99.0	7.58	29.2	349.0	
I_{DD} (wake-up from Stop1)	Supply current during wake-up from Stop 1 bypass mode	Wake-up clock MSI = 32 MHz. See (3).	3.0 V	-	124	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wake-up with code execution from flash memory. Average value given for a typical wake-up time as specified in *Table 45*.

Table 39. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP					MAX(1)			Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	0 °C	25 °C	85 °C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode, RTC disabled, BLE disabled	-	2.4 V	97.5	105	110	125	195	-	-	-	µA
			3.0 V	98.5	105	110	125	195	117.3	134.3	461.8	
			3.6 V	100	105	115	125	200	165.0	135.7	494.0	
	Supply current during wake-up from Stop 0 Bypass mode	Wake-up clock MSI = 32 MHz. See (2).	3.0 V	-	349	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Wake-up with code execution from flash memory. Average value given for a typical wake-up time as specified in *Table 45*.

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Table 40. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)			Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	0 °C	25 °C	85 °C	
I_{DD} (Standby)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC disabled	BLE disabled, no independent watchdog	2.4 V	0.270	0.350	0.540	0.955	3.50	-	-	-	µA
			3.0 V	0.270	0.370	0.575	1.00	3.85	0.380	0.945	8.505	
			3.6 V	0.300	0.410	0.645	1.15	4.20	0.400	1.040	8.980	
		BLE disabled, with independent watchdog	2.4 V	0.280	0.595	0.790	1.20	4.00	-	-	-	
			3.0 V	0.290	0.670	0.855	1.35	4.15	0.730	1.253	8.774	
			3.6 V	0.295	0.770	0.990	1.50	4.60	0.851	1.356	9.360	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC enabled BLE disabled	RTC clocked by LSI, no independent watchdog	2.4 V	0.630	0.705	0.910	1.30	3.80	-	-	-	
			3.0 V	0.725	0.825	1.050	1.50	3.95	0.930	1.463	8.977	
			3.6 V	0.860	0.970	1.200	1.70	4.25	1.050	1.628	9.634	
		RTC clocked by LSI, with independent watchdog	2.4 V	0.635	0.790	0.975	1.40	4.10	-	-	-	
			3.0 V	0.725	0.915	1.100	1.55	4.50	1.028	1.573	9.072	
			3.6 V	0.870	1.050	1.300	1.80	4.90	1.144	1.723	9.730	
		RTC clocked by LSE quartz (2) in low drive mode	2.4 V	0.665	0.755	0.960	1.35	4.05	-	-	-	
			3.0 V	0.775	0.880	1.100	1.55	4.40	0.600	1.100	8.719	
			3.6 V	0.935	1.050	1.300	1.80	5.00	0.750	1.171	9.460	
I_{DD} (SRAM2a)(3)	Supply current to be subtracted in Standby mode when SRAM2a is not retained	-	2.4 V	0.165	0.245	0.375	0.650	2.15	-	-	-	µA
			3.0 V	0.155	0.250	0.385	0.630	2.25	-	-	-	
			3.6 V	0.155	0.235	0.375	0.670	2.20	-	-	-	
I_{DD} (wake-up from Standby)	Supply current during wake-up from Standby mode	Wake-up clock is HSI16. See (4).	3.0 V	-	1.73	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. The supply current in Standby with SRAM2a mode is: I_{DD}(Standby) + I_{DD}(SRAM2a). The supply current in Standby with RTC with SRAM2a mode is: I_{DD}(Standby + RTC) + I_{DD}(SRAM2a).
4. Wake-up with code execution from flash memory. Average value given for a typical wake-up time as specified in *Table 45*.

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Table 41. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					MAX(1)			Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	0 °C	25 °C	85 °C	
I_{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	2.4 V	0.059	0.014	0.055	0.120	0.785	-	-	-	µA
			3.0 V	0.064	0.037	0.070	0.180	1.000	-	0.185	2.670	
			3.6 V	0.071	0.093	0.140	0.280	1.300	-	0.247	3.120	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE quartz (2) in low drive mode	2.4 V	0.425	0.405	0.460	0.540	1.200	-	-	-	
			3.0 V	0.535	0.535	0.595	0.700	1.500	-	0.664	2.990	
			3.6 V	0.695	0.720	0.790	0.940	2.000	-	0.790	3.730	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 42. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	0 °C	25 °C	40 °C	55 °C	85 °C	0 °C	25 °C	40 °C	55 °C	85 °C	
I_{DD}(VBAT)	Backup domain supply current	RTC disabled	2.4 V	1.00	2.00	5.00	12.0	60.0	-	-	-	-	-	nA
			3.0 V	2.00	4.00	7.00	16.0	75.0	-	-	-	-	-	
			3.6 V	7.00	15.0	23.0	42.0	170	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	2.4 V	385	395	400	415	475	-	-	-	-	-	
			3.0 V	495	505	515	530	600	-	-	-	-	-	
			3.6 V	630	645	660	685	830	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 43. Current under Reset condition

Symbol	Conditions	TYP					MAX(1)					Unit
		0 °C	25 °C	40 °C	55 °C	85 °C	0 °C	25 °C	40 °C	55 °C	85 °C	
$I_{DD(RST)}$	2.4 V	-	-	-	-	-	-	-	-	-	-	µA
	3.0 V	-	550	-	-	-	-	750	-	-	-	
	3.6 V	-	750	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

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I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull resistors generate current consumption when the pin is externally held to the opposite level. The value of this consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 65: I/O static characteristics*.

For the output pins, all the internal or external pull-down/pull-down and the external load must be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins, which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 44*) the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal and external) connected to the pin: $I_{SW} = V_{DD} \times f_{SW} \times C$, where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the I/O supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{IO} + C_{EXT}$
- C_{IO} is the I/O pin capacitance
- C_{EXT} is the PCB board capacitance plus any connected external device pin capacitance.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

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On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 44*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 16: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 44*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 44. Peripheral current consumption

Peripheral		Run	Low-power run and sleep	Unit
AHB1	Bus Matrix(1)	2.40	1.80	µA/MHz
	CRC	0.465	0.380	
	DMA1	1.90	1.80	
	DMAMUX	4.15	4.45	
	All AHB1 peripherals	8.75	8.65	
AHB2(2)	ADC independent clock domain	2.55	2.10	
	ADC clock domain	2.25	1.90	
	All AHB2 peripherals	3.45	2.7	
AHB Shared	TRNG independent clock domain	3.80	N/A	
	TRNG clock domain	2.00	N/A	
	SRAM2	1.70	1.35	
	FLASH	8.35	8.45	
	AES2	6.95	7.00	
	PKA	4.40	4.25	
	All AHB shared peripherals	17.5	16.0	

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Table 44. Peripheral current consumption (continued)

Peripheral		Run	Low-power run and sleep	Unit
APB1	RTC	1.10	1.25	µA/MHz
	I2C1 independent clock domain	2.50	4.40	
	I2C1 clock domain	4.80	5.50	
	LPTIM1 independent clock domain	2.10	3.00	
	LPTIM1 clock domain	3.60	3.80	
	TIM2	5.65	4.90	
	LPTIM2 clock domain	3.95	4.50	
	LPTIM2 independent clock domain	2.20	3.80	
	WWDG	0.335	0.965	
	All APB1 peripherals	17.0	13.55	
APB2	AHB to APB2(3)	1.10	1.35	
	TIM1	8.20	7.25	
	TIM17	2.85	2.40	
	TIM16	2.75	2.55	
	USART1 independent clock domain	4.40	7.00	
	USART1 clock domain	8.80	7.75	
	SPI1	1.75	1.45	
	All APB2 on	25.5	22	
ALL		72.2	62.9	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. GPIOs consumption during read and write accesses.
3. The AHB to APB2 bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.9 Wake-up time from Low-power modes and voltage scaling transition times

The wake-up times given in *Table 45* are the latency between the event and the execution of the first user instruction.

The device goes in Low-power mode after the WFE (Wait For Event) instruction.

Table 45. Low-power mode wake-up timings(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up time from Sleep mode to Run mode	-	9	10	No. of CPU cycles
$t_{WULPSLEEP}$	Wake-up time from Low-power sleep mode to Low-power run mode	Wake-up in flash with memory in power-down during low-power sleep mode (FPDS = 1 in PWR_CR1) and with clock MSI = 2 MHz	9	10	

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Table 45. Low-power mode wake-up timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in flash memory	-	Wake-up clock MSI = 32 MHz	2.38	2.96	µs
			Wake-up clock HSI16 = 16 MHz	1.69	2.00	
	Wake up time from Stop 0 mode to Run mode in SRAM1	-	Wake-up clock MSI = 32 MHz	2.63	3.00	
			Wake-up clock HSI16 = 16 MHz	1.80	2.00	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in flash memory	-	Wake-up clock MSI = 32 MHz	4.67	5.56	
			Wake-up clock HSI16 = 16 MHz	5.09	6.03	
	Wake up time from Stop 1 mode to Run in SRAM1	-	Wake-up clock MSI = 32 MHz	4.88	5.55	
			Wake-up clock HSI16 = 16 MHz	5.29	5.95	
	Wake up time from Stop 1 mode to Low-power run mode in flash memory	Regulator in Low-power mode (LPR = 1 in PWR_CR1)	Wake-up clock MSI = 4 MHz	7.96	9.59	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			8.00	9.47	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in flash memory	-	Wake-up clock MSI = 32 MHz	5.27	6.07	µs
			Wake-up clock HSI16 = 16 MHz	5.71	6.52	
	Wake up time from Stop 2 mode to Run mode in SRAM1	-	Wake-up clock MSI = 32 MHz	5.20	5.94	
			Wake-up clock HSI16 = 16 MHz	5.64	6.42	
t_{WUSTBY}	Wake-up time from Standby mode to Run mode	-	Wake-up clock HSI16 = 16 MHz	51.0	58.1	µs

1. Guaranteed by characterization results (V_{DD} = 3 V, .T = 25 °C).

Table 46. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wake-up time from Low-power run mode to Run mode(2)	Code run with MSI 2 MHz	15.33	16.30	µs

1. Guaranteed by characterization results (V_{DD} = 3 V, T = 25 °C).
2. Time until REGLPF flag is cleared in PWR_SR2.

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Table 47. Wake-up time using USART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wake-up time needed to calculate the maximum USART baud rate allowing to wake-up up from Stop mode when USART clock source is HSI16	Stop mode 0	-	1.7	µs
		Stop mode 1/2	-	8.5	

1. Guaranteed by design.

6.3.10 External clock source characteristics

High-speed external user clock generated from an external source

The high-speed external (HSE) clock is supplied with a 32 MHz crystal oscillator or a sine or a square wave.

The STM32WB50CG and STM32WB30CE include internal programmable capacitances that can be used to tune the crystal frequency to compensate the PCB parasitic one.

The characteristics in *Table 48* and *Table 50* are measured over recommended operating conditions, unless otherwise specified. Typical values are referred to T_A = 25 °C and V_{DD} = 3.0 V.

Table 48. HSE crystal requirements(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{NOM}	Oscillator frequency	-	-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance.	-	-	(3)	ppm
C_L	Load capacitance	-	6	-	8	pF
ESR	Equivalent series resistance	-	-	-	100	Ω

1. 32 MHz XTAL is validated for the specific reference NX2016SA.
2. For information about the HSE crystal refer to AN5165 “*Development of RF hardware using STM32WB microcontrollers*”, available on *www.st.com*.
3. Refer to the standard specification: 50 ppm for BLE, 40 ppm for 802.15.4.

Table 49. HSE clock source characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	Oscillator frequency	-	-	32	-	MHz
f_{TOLHSE}	Frequency tolerance	Includes initial accuracy, stability over temperature and aging	-	-	(2)	ppm
V_{HSE}	Clock input voltage limits	Sine or square wave, AC-coupled(3)	0.4	-	1.6	V_{PP}
DuCy(HSE)	Duty cycle	-	45	50	55	%
t_r, t_f	Rise and fall times	10% - 90% square wave	-	-	15 * V_{PP}	ns

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Table 49. HSE clock source characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\varphi_{n(HSE)}$	Phase noise for 32 MHz	Offset = 10 kHz	-	-	-127	dBc/Hz
		Offset = 100 kHz	-	-	-135	
		Offset = 1 MHz	-	-	-138	

1. Guaranteed by design.
2. Refer to the standard specification: 50 ppm for BLE, 40 ppm for 802.15.4.
3. Only AC coupled is supported (capacitor 470 pF to 100 nF).

Table 50. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SUA(HSE)}$	Startup time for 80% amplitude stabilization	V_{DDRF} stabilized, XOTUNE = 000000, -10 to +85 °C range	-	1000	-	µs
$t_{SUR(HSE)}$	Startup time for XOREADY signal	V_{DDRF} stabilized, XOTUNE = 000000, -10 to +85 °C range	-	250	-	
$I_{DDRF(HSE)}$	HSE current consumption(1)	HSEGMC = 000, XOTUNE = 000000	-	50	-	µA
$XOT_{g(HSE)}$	XOTUNE granularity	Capacitor bank	-	1	5	ppm
$XOT_{fp(HSE)}$	XOTUNE frequency pulling		±20	±40	-	
$XOT_{nb(HSE)}$	XOTUNE number of tuning bits		-	6	-	bit
$XOT_{st(HSE)}$	XOTUNE setting time		-	-	0.1	ms

1. Current consumption in standalone mode. The current consumption at device level is 350 µA in design simulation.

Note: For information about the trimming of the oscillator refer to AN5165 "Development of RF hardware using STM32WB microcontrollers", available on www.st.com.

Low-speed external user clock generated from an external source

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. The information provided in this section is based on design simulation results obtained with typical external components specified in *Table 51*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time.

Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

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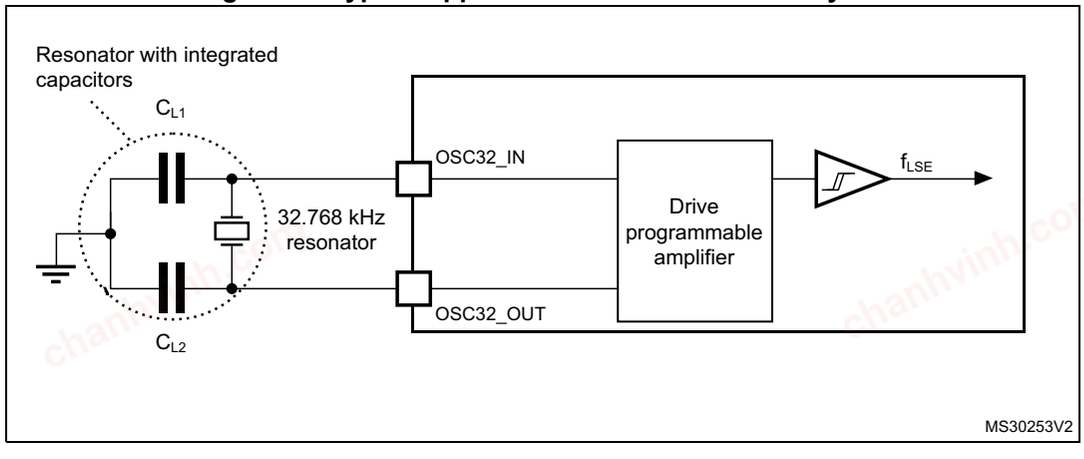
Table 51. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$G_{mcritmax}$	Maximum critical crystal g_m	LSEDRV[1:0] = 00 Low drive capability	-	-	0.50	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.70	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.70	
$t_{SU(LSE)}$(2)	Startup time	V_{DD} stabilized	-	2	-	s
f_{tolLSE}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling	-500	-	+500	ppm

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stable 32 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal refer to AN2867 "Oscillator design guide for STM8S, STM8A and STM32 microcontrollers" available from www.st.com.

Figure 16. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

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6.3.11 Internal clock source characteristics

The parameters given in *Table 52* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. The provided curves are characterization results, not tested in production.

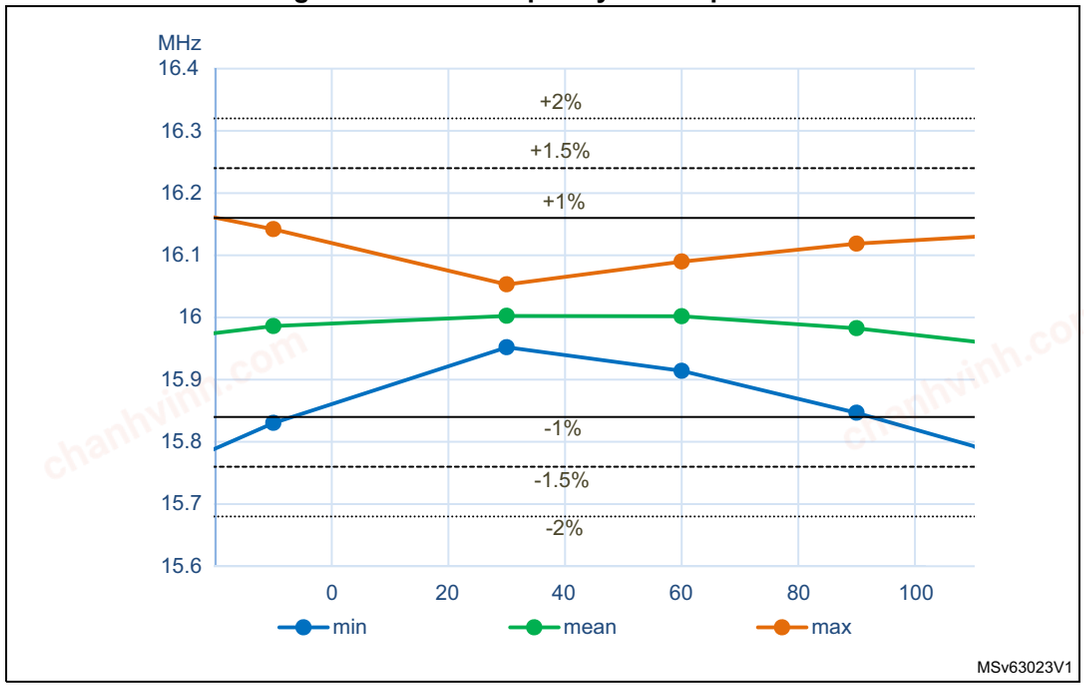
High-speed internal (HSI16) RC oscillator

Table 52. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 frequency	V_{DD} = 3.0 V, T_A = 30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty cycle	-	45	-	55	
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A = 0 to 85 °C	-1	-	1	
		T_A = -10 to 85 °C	-2	-	1.5	
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD} = 2 V to 3.6 V	-0.1	-	0.05	
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 17. HSI16 frequency vs. temperature



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Multi-speed internal (MSI) RC oscillator

Table 53. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD} = 3 V and T_A = 30 °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	789.6	800	810.4	
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL = 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
$\Delta_{TEMP}(MSI)^{(2)}$	MSI oscillator frequency drift over temperature	MSI mode	T_A = -0 to 85 °C	-3.5	-	3	%
			T_A = -10 to 105 °C	-8	-	6	

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Table 53. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
Δ_{VDD}(MSI)(2)	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD} = 2 to 3.6 V	-1.2	-	0.5	%
				V_{DD} = 2.4 to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD} = 2 to 3.6 V	-2.5	-	0.7	
				V_{DD} = 2.4 to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD} = 2 to 3.6 V	-5	-	1	
				V_{DD} = 2.4 to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}$ (MSI)(2)(4)	Frequency variation in sampling mode(3)	MSI mode	T_A = -10 to 85 °C		-	1	2	
CC jitter(MSI)(4)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(4)	RMS period jitter	PLL mode Range 11		-	-	50	-	
t_{SU}(MSI)(4)	MSI oscillator start-up time	Range 0		-	-	10	20	µs
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
t_{STAB}(MSI)(4)	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

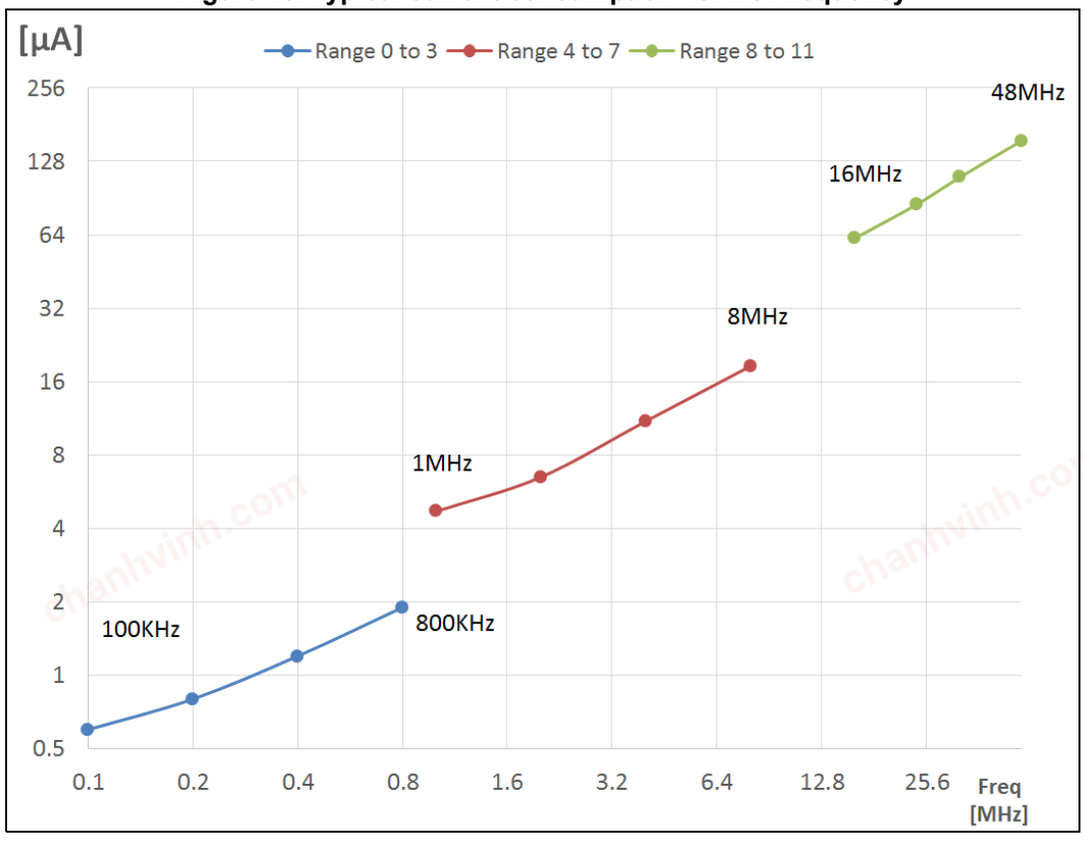
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Table 53. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$I_{DD}(MSI)^{(4)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Guaranteed by design.

Figure 18. Typical current consumption vs. MSI frequency



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High-speed internal 48 MHz (HSI48) RC oscillator

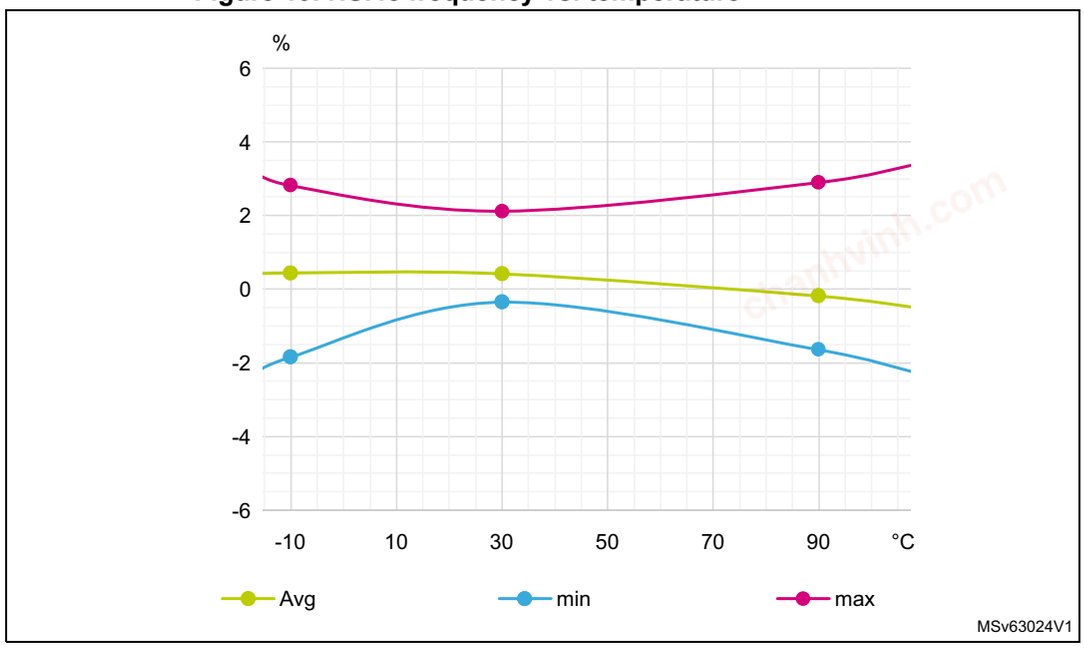
Table 54. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD} = 3.0 V, T_A = 30 °C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	
DuCy(HSI48)	Duty cycle	-	45(2)	-	55(2)	
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –10 to 85 °C	-	-	±3(3)	
		V_{DD} = 2 V to 3.6 V, T_A = –10 to 85 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	
		V_{DD} = 2 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	±0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	±0.25(2)	-	

1. V_{DD} = 3 V, T_A = –10 to 85 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

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Figure 19. HSI48 frequency vs. temperature



Low-speed internal (LSI) RC oscillator

Table 55. LSI1 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI1 frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 2 to 3.6 V, T_A = -10 to 85 °C	29.5	-	34	
$t_{SU}(LSI1)$(2)	LSI1 oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI1)$(2)	LSI1 oscillator stabilization time	5% of final frequency	-	125	180	
$I_{DD}(LSI1)$(2)	LSI1 oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 56. LSI2 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI2}	LSI2 frequency	V_{DD} = 3.0 V, T_A = 30 °C	21.6	-	44.2	kHz
		V_{DD} = 2 to 3.6 V, T_A = -10 to 85 °C	21.2	-	44.4	
$t_{SU}(LSI2)$(2)	LSI2 oscillator start-up time	-	0.7	-	3.5	ms
$I_{DD}(LSI2)$(2)	LSI2 oscillator power consumption	-	-	500	1180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

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6.3.12 PLL characteristics

The parameters given in *Table 57* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 57. PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	-	2	-	64	MHz
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	-	8	-	64	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	-	8	-	64	
f_{VCO_OUT}	PLL VCO output	-	96	-	344	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 64 MHz	-	40	-	ps
	RMS period jitter		-	30	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 96 MHz	-	200	260	µA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the two PLLs.

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6.3.13 Flash memory characteristics

Table 58. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	90.8	µs
t_{prog_row}	One row (64 double word) programming time	Normal programming	5.2	5.5	ms
		Fast programming	3.8	4.0	
t_{prog_page}	One page (4 KByte) programming time	Normal programming	41.8	43.0	
		Fast programming	30.4	31.0	
t_{ERASE}	Page (4 KByte) erase time	-	22.0	24.5	
t_{ME}	Mass erase time	-	22.1	25.0	
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	

1. Guaranteed by design.

Table 59. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –10 to +85 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

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6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 60*. They are based on the EMS levels and classes defined in application note AN1709 “EMC design guide for STM8, STM32 and Legacy MCUs”, available on *www.st.com*.

Table 60. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flow must include the management of runaway conditions such as:

- corrupted program counter
- unexpected reset
- critical data corruption (e.g. control registers)

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Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or on the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see AN1015 "*Software techniques for improving microcontrollers EMC performance*", available on *www.st.com*).

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with the IEC 61967-2 standard, which specifies the test board and the pin loading.

Table 61. EMI characteristics for f_{HSE} / f_{CPUM4}, f_{CPUM0} = 32 MHz / 64 MHz, 32 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Peripheral ON SMPS OFF or ON	Unit
S_{EMI}	Peak(1)	V_{DD} = 3.6 V, T_A = 25 °C, UFQFPN48 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	11	dBµV
			30 MHz to 130 MHz	5	
			130 MHz to 1 GHz	0	
			1 GHz to 2 GHz	8	
	Level(2)		0.1 MHz to 2 GHz	1.5	-

1. Refer to AN1709, "EMI radiated test" section.
2. Refer to AN1709, "EMI level classsification section.

6.3.15 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 62. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1 JS-002	C2a	500	

1. Guaranteed by characterization results.

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Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- a supply overvoltage is applied to each power supply pin
- a current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 63. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +85 °C conforming to JESD78A	II

6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA / 0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 64*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 64. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PB0, PB1	-5	N/A(2)	mA
	Injected current on PB0, PB1 pins	-5	0	

1. Guaranteed by characterization results.
2. Injection not possible.

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6.3.17 I/O port characteristics

For information on the GPIO configuration, refer to AN4899 *STM32 microcontroller GPIO hardware settings and low-power consumption*, available on *www.st.com*.

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 65* are derived from tests performed under the conditions summarized in *Table 20: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Table 65. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage(1)	2 V < V_{DD} < 3.6 V	-	-	0.3 x V_{DD}	V
	I/O input low level voltage(2)				0.39 x V_{DD} - 0.06	
V_{IH}	I/O input high level voltage(1)		0.7 x V_{DD}	-	-	
	I/O input high level voltage(2)		0.49 x V_{DD} + 0.26	-	-	
V_{hys}	TT_xx, FT_xxx and NRST I/Os input hysteresis		-	200	-	mV
I_{lkg}	FT_xx input leakage current	0 ≤ V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX}) +1 V(2)(3)(4)	-	-	650	
		Max(V_{DDXXX}) +1 V < V_{IN} ≤ 5.5 V(2)(3)(4)(5)(6)	-	-	200(7)	
	FT_lu, FT_u and PB2 I/Os input leakage current	0 ≤ V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX}) +1 V(2)(3)	-	-	2500	
		Max(V_{DDXXX}) +1 V < V_{IN} ≤ 5.5 V(1)(3)(4)(8)	-	-	250	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(3)	-	-	2000	
R_{PU}	Weak pull-up equivalent resistor(1)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(1)	V_{IN} = V_{DD}	25	40	55	
C_{IO}	I/O pin capacitance(9)	-	-	5	-	pF

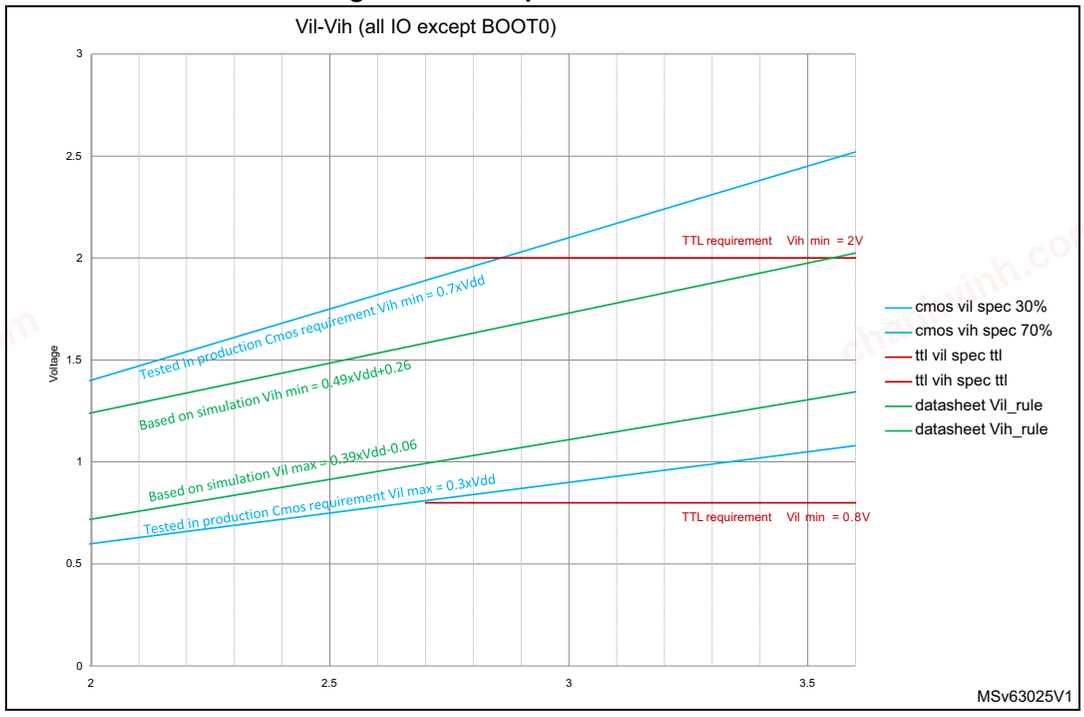
1. Tested in production.
2. Guaranteed by design, not tested in production.
3. Represents the pad leakage of the I/O itself. The total product pad leakage is given by $I_{Total_Ileak_max}$ = 10 µA + number of I/Os where V_{IN} is applied on the pad x $I_{lkg(Max)}$.

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4. Max(V_{DDXXX}) is the maximum value among all the I/O supplies.
5. V_{IN} must be lower than [Max(V_{DDXXX}) + 3.6 V].
6. Refer to *Figure 20: I/O input characteristics*.
7. To sustain a voltage higher than Min(V_{DD}, V_{DDA}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled. All FT_xx IO except FT_lu, FT_u and PB2.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS, whose contribution to the series resistance is minimal (~10%).
9. RF I/O structure excluded.

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters, as shown in *Figure 20* .

Figure 20. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL} / V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*.

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 16: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 16: Voltage characteristics*).

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Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT or TT unless otherwise specified).

Table 66. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	CMOS port(3) $\|I_{IO}\|$ = 8 mA $V_{DD} \geq 2.7$ V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DD} - 0.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	TTL port(3) $\|I_{IO}\|$ = 8 mA $V_{DD} \geq 2.7$ V	-	0.4	
V_{OH}(2)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DD} \geq 2.7$ V	-	1.3	
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DD} - 1.3	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA $V_{DD} \geq 2$ V	-	0.4	
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DD} - 0.45	-	
V_{OLFM+}(2)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with “f” option)	$\|I_{IO}\|$ = 20 mA $V_{DD} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DD} \geq 2$ V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 16: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. Guaranteed by design.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Table 67*.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

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Table 67. I/O AC characteristics(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5	MHz
			C = 50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	1	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
			C = 10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	1.5	
	Tr/Tf	Output rise and fall time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	ns
			C = 50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	52	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17	
			C = 10 pF, 2 V ≤ V_{DD} ≤ ≤2.7 V	-	37	
01	Fmax	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	MHz
			C = 50 pF, 2 V ≤ V_{DD} ≤ ≤2.7 V	-	10	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	
			C = 10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	15	
	Tr/Tf	Output rise and fall time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	9	ns
			C = 50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	16	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.5	
			C = 10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	9	
10	Fmax	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	MHz
			C = 50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	25	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100(3)	
			C = 10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	37.5	
	Tr/Tf	Output rise and fall time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.8	ns
			C = 50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	11	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.5	
			C = 10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	5	
11	Fmax	Maximum frequency	C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	120(3)	MHz
			C = 30 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	50	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	180(3)	
			C = 10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	75(3)	
	Tr/Tf	Output rise and fall time	C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C = 30 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	6	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.7	
			C = 10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	3.3	

1. The maximum frequency is achieved with a duty cycle between 45 and 55%, when loaded by the specified capacitance.
2. The fall and rise time are defined, respectively, between 90 and 10%, and between 10 and 90% of the output waveform.

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3. This value represents the I/O capability but the maximum system frequency is limited to 64 MHz.

6.3.18 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

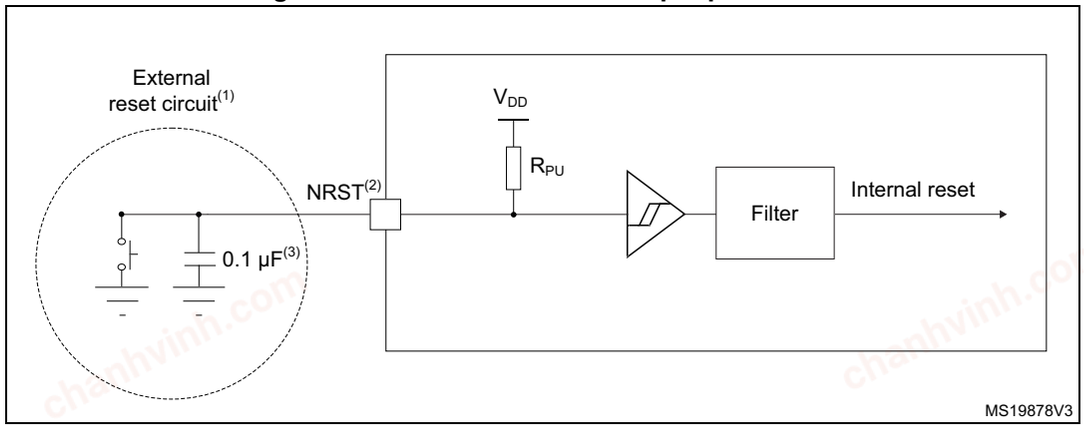
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 68. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	2 V ≤ V_{DD} ≤ 3.6 V	350	-	-	

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10%).

Figure 21. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 68*, otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

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6.3.19 Analog switches booster

Table 69. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	2	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for $2.0\ V \le V_{DD} \le 2.7\ V$	-	-	500	µA
	Booster consumption for $2.7\ V \le V_{DD} \le 3.6\ V$	-	-	900	

1. Guaranteed by design.

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6.3.20 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in *Table 70* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 20: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 70. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2	-	3.6	V
f_{ADC}	ADC clock frequency	-	-	-	32	MHz
f_s	Sampling rate	Resolution = 12 bits	-	-	2.13	Msps
		Resolution = 10 bits	-	-	2.46	
		Resolution = 8 bits	-	-	2.91	
		Resolution = 6 bits	-	-	3.55	
f_{TRIG}	External trigger frequency	f_{ADC} = 32 MHz Resolution = 12 bits	-	-	2.13	MHz
		Resolution = 12 bits	-	-	15	1 / f_{ADC}
V_{CMIN}	Input common mode	Differential mode	(V_{REF+}+ V_{REF-}) / 2 - 0.18	(V_{REF+}+ V_{REF-}) / 2	(V_{REF+}+ V_{REF-}) / 2 + 0.18	V
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 32 MHz	3.625			µs
		-	116			1 / f_{ADC}
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	1 / f_{ADC}
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 32 MHz	0.078	-	20.0	µs
		-	2.5	-	640.5	1 / f_{ADC}

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Table 70. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 32 MHz Resolution = 12 bits	0.469	-	20.41	µs
		Resolution = 12 bits	t_s + 12.5 cycles for successive approximations = 15 to 653			1 / f_{ADC}
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 2.13 Msps	-	340	415	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 2.13 Msps	-	64	80	
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 2.13 Msps	-	128	155	
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SS}.

Table 71. ADC sampling time(1)(2)

Resolution (bits)	RAIN (kΩ)	Minimum sampling time (ns)	Sampling cycles
12	0	57	2.5
	0.05	62	2.5
	0.1	67	2.5
	0.2	76	2.5
	0.5	104	6.5
	1	151	6.5
	5	526	24.5
	10	994	47.5
	20	1932	92.5
	50	4744	247.5
	100	9430	640.5

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Table 71. ADC sampling time[1][2] (continued)

Resolution (bits)	RAIN (kΩ)	Minimum sampling time (ns)	Sampling cycles
10	0	47	2.5
	0.05	51	2.5
	0.1	55	2.5
	0.2	62	2.5
	0.5	85	6.5
	1	124	6.5
	5	431	24.5
	10	816	47.5
	20	1584	92.5
	50	3891	247.5
	100	7734	247.5
8	0	37	2.5
	0.05	40	2.5
	0.1	43	2.5
	0.2	49	2.5
	0.5	67	2.5
	1	97	6.5
	5	337	12.5
	10	637	24.5
	20	1237	47.5
	50	3037	247.5
	100	6038	247.5

1. Guaranteed by design.
2. V_{DD} = 2 V, C_{pcb} = 4.7 pF, 105 °C, booster enabled.

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Table 72. ADC accuracy - Limited test conditions 1(1)(2)(3)

Symbol	Parameter	Conditions(4)		Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 32 MHz, Sampling rate ≤ 2.13 Msps, V_{DDA} = 3 V, T_A = 25 °C	Single ended	-	4	5	LSB
			Differential	-	3.5	4.5	
EO	Offset error		Single ended	-	1	2.5	
			Differential	-	1.5	2.5	
EG	Gain error		Single ended	-	2.5	4.5	
			Differential	-	2.5	3.5	
ED	Differential linearity error		Single ended	-	1	1.5	
			Differential	-	1	1.2	
EL	Integral linearity error		Single ended	-	1.5	2.5	
			Differential	-	1	2	
ENOB	Effective number of bits		Single ended	10.4	10.5	-	bits
			Differential	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	64.4	65	-	dB
			Differential	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	65	66	-	
			Differential	67	68	-	
THD	Total harmonic distortion	ADC clock frequency ≤ 32 MHz, Sampling rate ≤ 2.13 Msps, V_{DDA} = 3 V, T_A = 25 °C	Single ended	-	-74	-73	dB
			Differential	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative injection current: Injecting negative current on any analog input pins must be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins that may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disabled when V_{DDA} ≥ 2.4 V. No oversampling.

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Table 73. ADC accuracy - Limited test conditions 2(1)(2)(3)

Symbol	Parameter	Conditions(4)		Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 32 MHz, Sampling rate ≤ 2.13 Msps, V_{DDA} ≥ 2 V, T_A = 25 °C	Single ended	-	4	6.5	LSB
			Differential	-	3.5	5.5	
EO	Offset error		Single ended	-	1	5	
			Differential	-	1.5	3	
EG	Gain error		Single ended	-	2.5	6	
			Differential	-	2.5	3.5	
ED	Differential linearity error		Single ended	-	1	1.5	
			Differential	-	1	1.2	
EL	Integral linearity error		Single ended	-	1.5	3.5	
			Differential	-	1	2.5	
ENOB	Effective number of bits		Single ended	10	10.5	-	bits
			Differential	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	62	65	-	dB
			Differential	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	64	66	-	
			Differential	66.5	68	-	
THD	Total harmonic distortion	ADC clock frequency ≤ 32 MHz, Sampling rate ≤ 2.13 Msps, V_{DDA} ≥ 2 V, T_A = 25 °C	Single ended	-	-74	-67	dB
			Differential	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative injection current: Injecting negative current on any analog input pins must be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins that may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disabled when V_{DDA} ≥ 2.4 V. No oversampling.

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Table 74. ADC accuracy - Limited test conditions 3(1)(2)(3)

Symbol	Parameter	Conditions(4)		Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 32 MHz, Sampling rate ≤ 2.13 Msps, 2 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V,	Single ended	-	4.5	6.5	LSB
			Differential	-	4.5	5.5	
EO	Offset error		Single ended	-	2.5	5	
			Differential	-	2.5	3	
EG	Gain error		Single ended	-	3.5	6	
			Differential	-	3.5	5	
ED	Differential linearity error		Single ended	-	1.2	1.5	
			Differential	-	1	1.2	
EL	Integral linearity error		Single ended	-	2.5	3.5	
			Differential	-	2	2.5	
ENOB	Effective number of bits		Single ended	10	10.4	-	bits
			Differential	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	62	64	-	dB
			Differential	65	66	-	
SNR	Signal-to-noise ratio		Single ended	63	65	-	
			Differential	66	67	-	
THD	Total harmonic distortion	ADC clock frequency ≤ 32 MHz, Sampling rate ≤ 2.13 Msps, 2 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V,	Single ended	-	-71	-67	dB
			Differential	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative injection current: Injecting negative current on any analog input pins must be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins that may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disabled when V_{DDA} ≥ 2.4 V. No oversampling.

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Figure 22. ADC accuracy characteristics

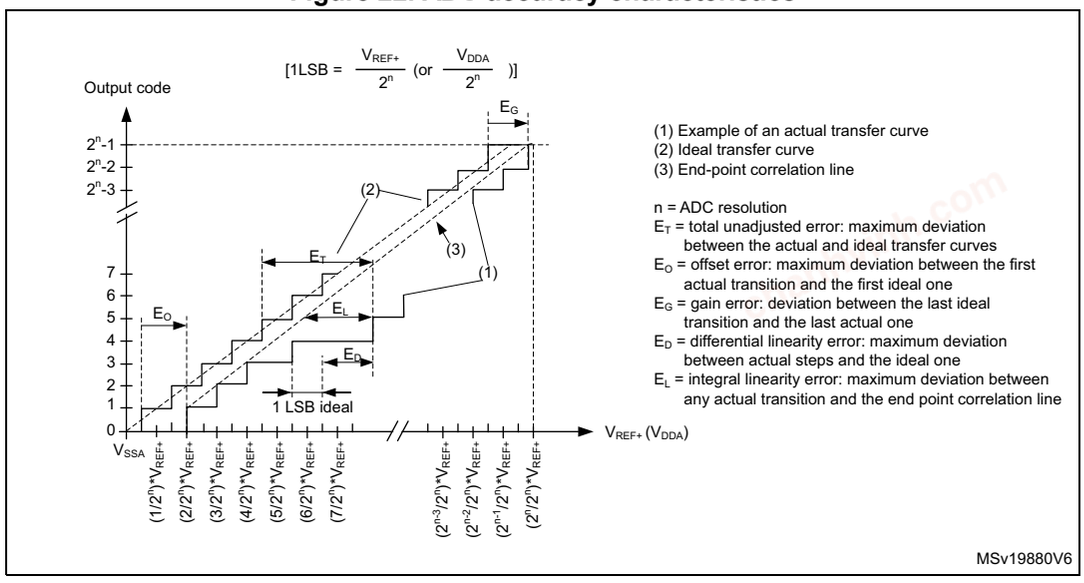
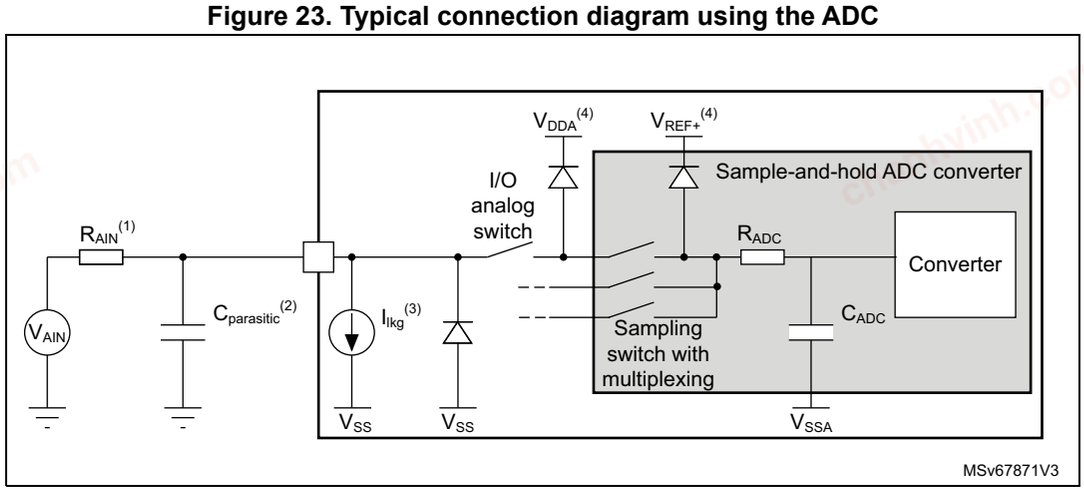


Figure 23. Typical connection diagram using the ADC



1. Refer to *Table 70: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 65: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} must be reduced.
3. Refer to *Table 65: I/O static characteristics* for the values of I_{lkg}.
4. Refer to *Figure 11: Power supply scheme*.

General PCB design guidelines

Power supply decoupling has to be performed as shown in *Figure 11: Power supply scheme*. The 10 nF capacitor needs to be ceramic (good quality), placed as close as possible to the chip.

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6.3.21 Temperature sensor characteristics

Table 75. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV / °C
V_{30}	Voltage at 30 °C (±5 °C)(3)	0.742	0.760	0.785	V
t_{START} (TS_BUF)(1)	Sensor buffer start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 9: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.22 V_{BAT} monitoring characteristics

Table 76. V_{BAT} monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	3 x 39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(2)	Error on Q	-10	-	10	%
t_{S_vbat}(2)	ADC sampling time when reading V_{BAT}	12	-	-	µs

1. 1.55 V < V_{BAT} < 3.6 V.
2. Guaranteed by design.

Table 77. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.23 Timer characteristics

The parameters given in the following tables are guaranteed by design. Refer to *Section 6.3.17* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

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Table 78. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	15.625	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 64 MHz	0	40	
Res_{TIM}	Timer resolution	TIM1, TIM16, TIM17	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	0.015625	1024	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	-	67.10	s

1. TIMx, is used as a general term where x stands for 1, 2, 16 or 17.

Table 79. IWDG min/max timeout period at 32 kHz (LSI1)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock vs. the LSI clock, hence there is always a full RC period of uncertainty.

6.3.24 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): bit rate up to 1 Mbit/s.

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Table 80. Minimum I2CCLK frequency in all I^2C modes

Symbol	Parameter	Condition		Min	Unit
$f_{(I2CCLK)}$	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog filter ON, DNF = 0	9	
			Analog filter OFF, DNF = 1	9	
		Fast-mode Plus	Analog filter ON, DNF = 0	19	
			Analog filter OFF, DNF = 1	16	

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to the reference manual RM0471).

The SDA and SCL I/O requirements are met with the following restriction: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. The 20 mA output drive requirement in Fast-mode Plus is supported partially.

This limits the maximum load C_{load} supported in Fast-mode Plus, given by these formulas:

- $t_r(SDA/SCL) = 0.8473 \times R_p \times C_{load}$
- $R_p(min) = [V_{DD} - V_{OL}(max)] / I_{OL}(max)$

where R_p is the I2C lines pull-up. Refer to *Section 6.3.17* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter, refer to *Table 81* for its characteristics.

Table 81. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	110(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

SPI characteristics

Unless otherwise specified, the parameters given in *Table 82* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 20: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.17* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

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Table 82. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode $2.0 < V_{DD} < 3.6$ V	-	-	32	MHz
		Master transmitter mode $2.0 < V_{DD} < 3.6$ V			32	
		Slave receiver mode $2.0 < V_{DD} < 3.6$ V			32	
		Slave mode transmitter/full duplex $2.7 < V_{DD} < 3.6$ V			32(2)	
		Slave mode transmitter/full duplex $2.0 < V_{DD} < 3.6$ V			20.5(2)	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	4 x T_{PCLK}	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	2 x T_{PCLK}	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK} - 1.5	T_{PCLK}	T_{PCLK} + 1	
$t_{su(MI)}$	Data input setup time	Master mode	1.5	-	-	ns
$t_{su(SI)}$		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	
$t_{dis(SO)}$	Data output disable time		9	-	16	
$t_{v(SO)}$	Data output valid time	Slave mode $2.7 < V_{DD} < 3.6$ V	-	14.5	15.5	ns
		Slave mode $2.0 < V_{DD} < 3.6$ V	-	15.5	24	
$t_{v(MO)}$		Master mode (after enable edge)	-	2.5	3	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	8	-	-	
$t_{h(MO)}$		Master mode (after enable edge)	1	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$, which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.

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Figure 24. SPI timing diagram - Slave mode and CPHA = 0

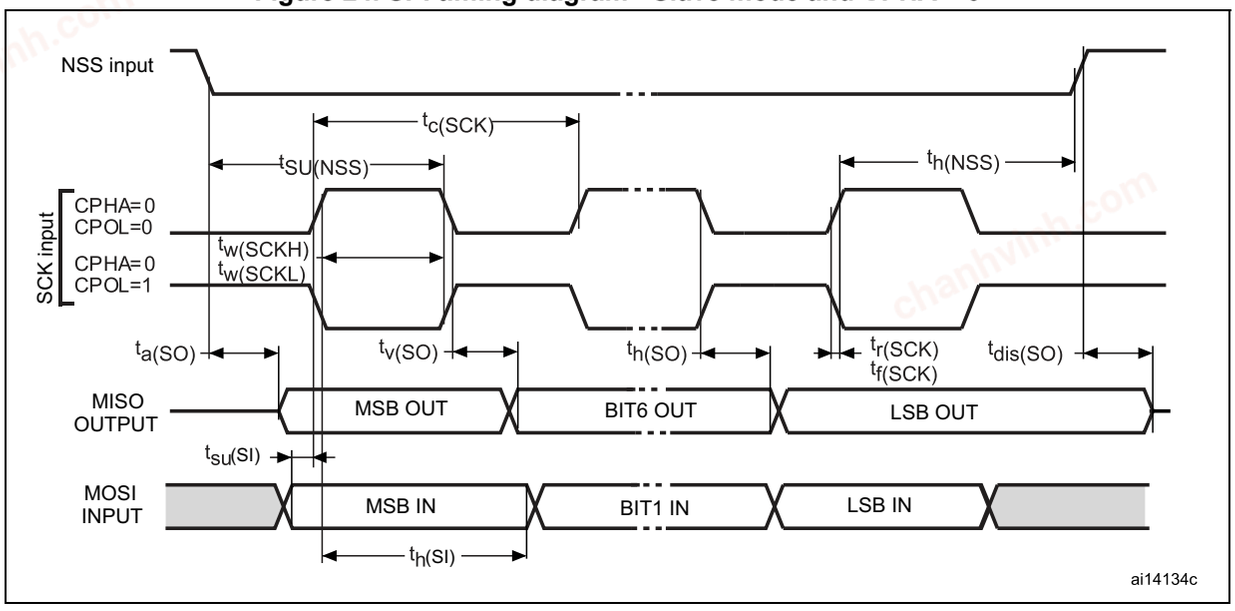
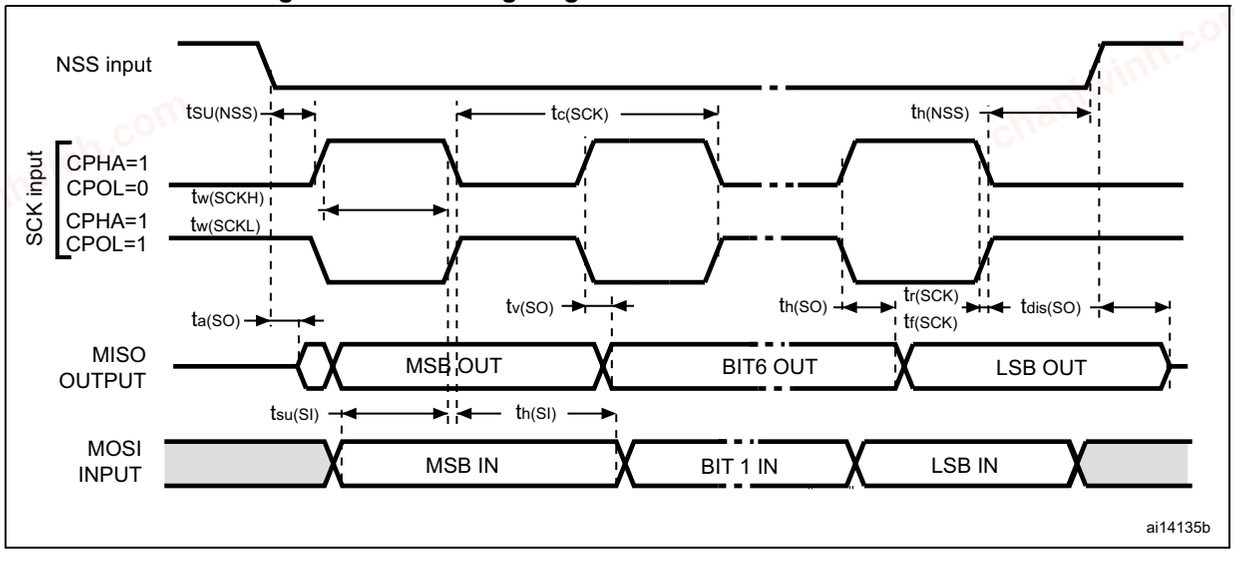


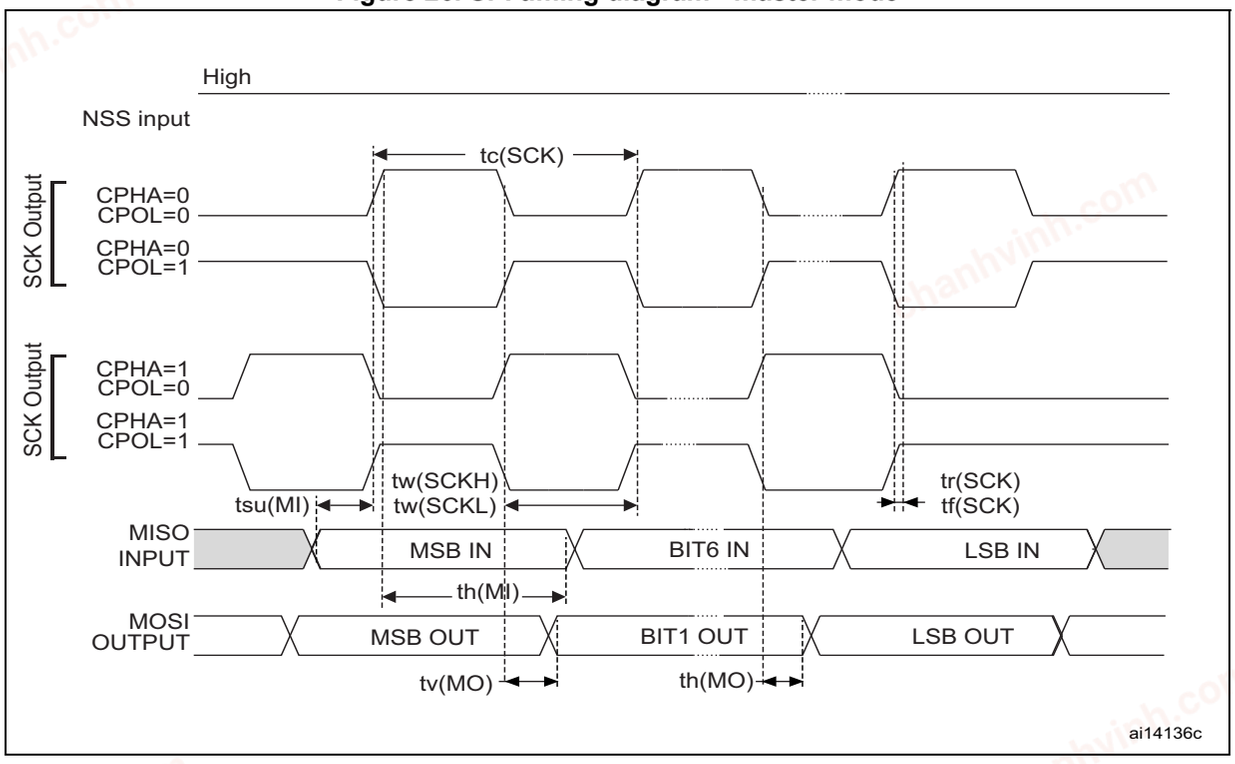
Figure 25. SPI timing diagram - Slave mode and CPHA = 1



1. Measurement points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

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Figure 26. SPI timing diagram - master mode



1. Measurement points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 83* and *Table 84* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 20: General operating conditions*. with the following configuration:

- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Table 83. JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/t_{c(TCK)}$	TCK clock frequency	2.7 < V_{DD} < 3.6 V	-	-	29	MHz
		2.0 < V_{DD} < 3.6 V	-	-	21	
$t_{isu(TMS)}$	TMS input setup time	-	2.5	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	2	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	1.5	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	2	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7 < V_{DD} < 3.6 V	-	13.5	16.5	
		2.0 < V_{DD} < 3.6 V	-	13.5	23	
$t_{oh(TDO)}$	TDO output hold time	-	11	-	-	

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Table 84. SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/t_{c(SWCLK)}$	SWCLK clock frequency	$2.7 < V_{DD} < 3.6$ V	-	-	55	MHz
		$2.0 < V_{DD} < 3.6$ V	-	-	35	
$t_{isu(TMS)}$	SWDIO input setup time	-	2.5	-	-	ns
$t_{ih(TMS)}$	SWDIO input hold time	-	2	-	-	
$t_{ov(TDO)}$	SWDIO output valid time	$2.7 < V_{DD} < 3.6$ V	-	16	18	
		$2.0 < V_{DD} < 3.6$ V	-	16	28	
$t_{oh(TDO)}$	SWDIO output hold time	-	13	-	-	

Refer to *Section 6.3.17* for more details on the input/output alternate function characteristics (CK, SD, WS).

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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Device marking

Refer to “*Reference device marking schematics for STM32 microcontrollers and microprocessors*” (TN1433) available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

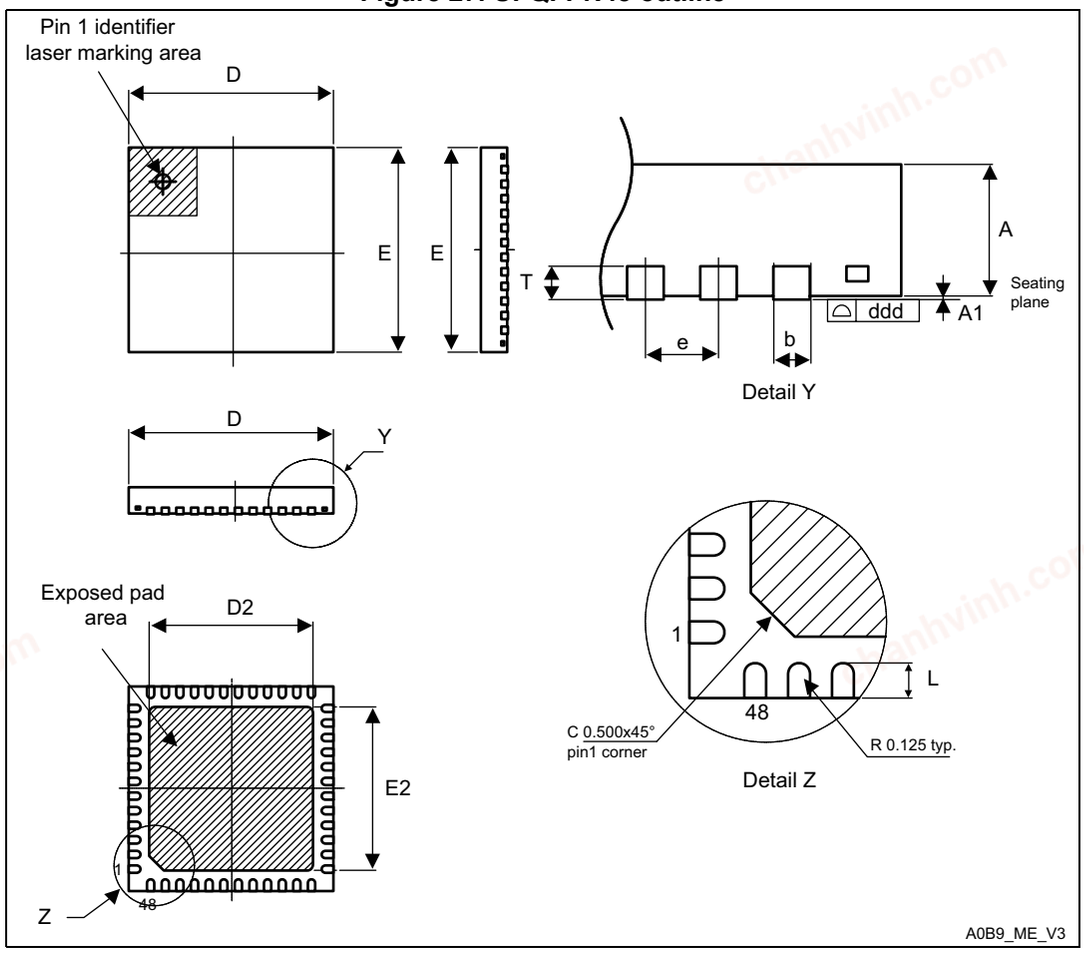
A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

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7.2 UFQFPN48 package information

UFQFPN48 is a 7 x 7mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 27. UFQFPN48 outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

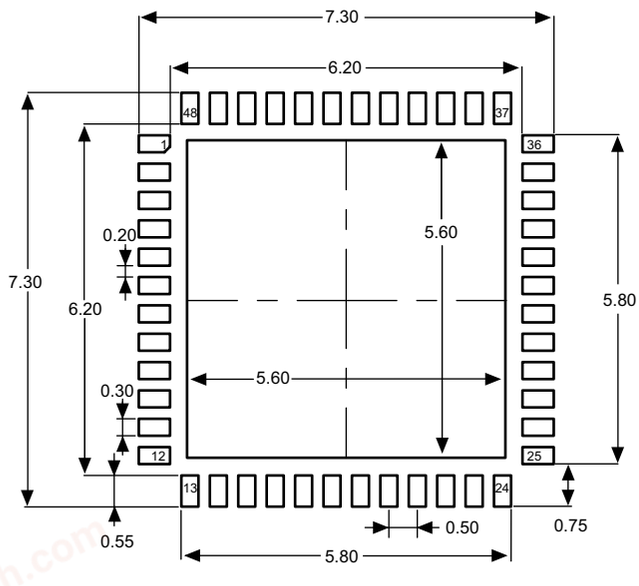
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Table 85. UFQFPN48 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 28. UFQFPN48 recommended footprint



1. Dimensions are expressed in millimeters.

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7.3 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 24: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watt. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

- $P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH})$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Note: As the radiated RF power is quite low (< 4 mW), it is not necessary to remove it from the chip power consumption.

Table 86. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFQFPN48 - 7 mm x 7 mm	24.9	°C/W
Θ_{JB}	**Thermal resistance junction-board** UFQFPN48 - 7 mm x 7 mm	13.0	
Θ_{JC}	**Thermal resistance junction-case** UFQFPN48 - 7 mm x 7 mm	1.3	

7.3.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.3.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the device at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following example shows how to calculate the temperature range needed for a given application.

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Example: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V and maximum eight I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V = 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 86* T_{Jmax} is calculated as follows:

– For UFQFPN48, 24.9 °C/W

T_{Jmax} = 82 °C + (24.9 °C/W × 447 mW) = 82 °C + 22 °C = 93 °C

This is within the range of the suffix 5 version parts (–10 < T_J < 105 °C), see *Section 8*.

In this case, parts must be ordered at least with the temperature range suffix 5 (see *Section 8*).

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8 Ordering information

Example: STM32 WB 50 C G U 5 A TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

WB = Wireless Bluetooth®

Device subfamily

50 = Die 5, full set of features

30 = Die 3, full set of features

Pin count

C = 48 pins

Flash memory size

G = 1 Mbytes

E = 512 Kbytes

Package

U = UFQFPN48 7 x 7 mm

Temperature range

5 = Industrial temperature range, -10 to 85 °C (105 °C junction)

Identification code

A = proprietary identification code

blank = non-proprietary identification code

Packing

TR = tape and reel

xxx = programmed parts

For a list of available options (speed, package, etc.) or for further information on any aspect of this device contact your nearest ST sales office.

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10 Revision history

Table 87. Document revision history

Date	Revision	Changes
08-Jul-2019	1	Initial release.
18-Feb-2020	2	Updated *Section 2: Description*, *I/O system current consumption* and *Example: High-performance application*. Updated *Table 1: STM32WB50CG and STM32WB30CE device features and peripheral counts*, *Table 5: Features over all modes*, *Table 20: General operating conditions*, *Table 21: RF transmitter BLE characteristics*, *Table 39: Current consumption in Stop 0 mode*, *Table 43: Current under Reset condition*, *Table 56: LSI2 oscillator characteristics*, *Table 82: SPI characteristics* and *Table 86: Package thermal characteristics*. Updated *Figure 1: STM32WB50CGxx block diagram*, *Figure 6: Power supply overview*, *Figure 7: Clock tree* and *Figure 11: Power supply scheme*. Added *JTAG/SWD interface characteristics* and footnote *3* to *Table 13*.
13-Mar-2020	3	Updated *Table 1: STM32WB50CG and STM32WB30CE device features and peripheral counts*. Updated *Figure 8: STM32WB50CG and STM32WB30CE UFQFPN48 pinout*[(1)(2)]. Updated *Table 48: HSE crystal requirements*. Removed former footnote *3* from *Table 13*. Minor text edits across the whole document.

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Table 87. Document revision history (continued)

Date	Revision	Changes
03-Jul-2020	4	Added STM32WB30CE device. Updated *Features*, *Section 2: Description*, *Section 3.3.4: Embedded SRAM*, *Section 3.6.5: Typical RF application schematic*, *Section 6.3.10: External clock source characteristics*, *Section 7.2: UFQFPN48 package information* and *Section 8: Ordering information*. Updated *Table 1: STM32WB50CG and STM32WB30CE device features and peripheral counts*, footnote of *Table 3: RF pin list*, *Table 14: STM32WB50CG and STM32WB30CE pin and ball definitions* and its footnotes, *Table 15: Alternate functions*, footnote *1* of *Table 16: Voltage characteristics*, footnote *1* of *Table 17: Current characteristics*, *Table 20: General operating conditions*, *Table 22: RF transmitter BLE characteristics (1 Mbps)*, *Table 23: RF receiver BLE characteristics (1 Mbps)*, *Table 26: RF receiver 802.15.4 characteristics*, footnote *3* of *Table 48: HSE crystal requirements*, *Table 58: Flash memory characteristics* and *Table 86: Package thermal characteristics*. Added footnotes to *Table 19: Main performance at VDD = 3.3 V*, *Table 24: RF BLE power consumption for VDD = 3.3 V*, *Table 27: RF 802.15.4 power consumption for VDD = 3.3 V* and *Table 76: V_{BAT} monitoring characteristics*. Updated *Figure 6: Power supply overview*, *Figure 11: Power supply scheme* and *Figure 22: ADC accuracy characteristics*. Added *Figure 2: STM32WB30CExx block diagram* and *Figure 30: STM32WB30CE UFQFPN48 marking example (package top view)*. Added *Table 49: HSE clock source characteristics*. Minor text edits across the whole document.
13-Apr-2021	5	Updated document title, *Features*, *Section 1: Introduction*, *Section 2: Description*, *Section 3.3.4: Embedded SRAM*, *Section 3.6: RF subsystem*, *Section 3.6.2: Bluetooth Low Energy general description*, *Section 3.7.3: Power supply supervisor*, *Section 3.14: Analog to digital converter (ADC)*, *Section 6.1.2: Typical values*, *Section 6.3.10: External clock source characteristics*, *Section 7.2: UFQFPN48 package information* and *Section 8: Ordering information*. Updated *Table 1: STM32WB50CG and STM32WB30CE device features and peripheral counts*, *Table 3: RF pin list*, *Table 5: Features over all modes*, *Table 6: STM32WB50CG and STM32WB30CE modes overview*, *Table 14: STM32WB50CG and STM32WB30CE pin and ball definitions*, *Table 15: Alternate functions*, *Table 19: Main performance at VDD = 3.3 V*, *Table 29: Embedded reset and power control block characteristics*, *Table 44: Peripheral current consumption*, *Table 49: HSE clock source characteristics*, footnote *2* of *Table 51: Low-speed external user clock characteristics* and *Table 76: V_{BAT} monitoring characteristics*. Added *Table 47: Wake-up time using USART*. Updated *Figure 3: STM32WB50CG and STM32WB30CE RF front-end block diagram*, *Figure 7: Clock tree* and *Figure 22: ADC accuracy characteristics*.
13-Jan-2022	6	Updated *Features*, *Section 3.6.2: Bluetooth Low Energy general description* and *Section 3.10: Clocks and startup*. Updated *Table 20: General operating conditions*. Updated *Figure 22: ADC accuracy characteristics*, *Figure 23: Typical connection diagram using the ADC* and its footnotes.

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Table 87. Document revision history (continued)

Date	Revision	Changes
08-Jun-2022	7	Updated document title, *Features*, *Section 2: Description*, *Section 3.6: RF subsystem*, *Section 3.6.2: Bluetooth Low Energy general description* and *Section 7.3: Thermal characteristics*. Updated footnote *2* of *Table 19: Main performance at VDD = 3.3 V*, footnotes of *Table 48: HSE crystal requirements*, and added footnote to *Table 50: HSE oscillator characteristics*. Updated *Table 61: EMI characteristics for fHSE / fCPUM4, fCPUM0 = 32 MHz / 64 MHz, 32 MHz*, *Table 65: I/O static characteristics* and its footnote *7*. Updated *Figure 7: Clock tree*, *Figure 24: SPI timing diagram - Slave mode and CPHA = 0*, *Figure 25: SPI timing diagram - Slave mode and CPHA = 1*, and *Figure 29: STM32WB50CG UFQFPN48 marking example (package top view)*. Added *Section 9: Important security notice*. Minor text edits across the whole document.
04-Apr-2023	8	Updated *Features*, *Section 6.2: Absolute maximum ratings*, *I/O system current consumption*, and *Section 6.3.17: I/O port characteristics*. Updated footnote *2* of *Table 5: Features over all modes*, footnote *1* of *Table 48: HSE crystal requirements*, and footnote *1* of *Table 67: I/O AC characteristics*. Added footnote to *Table 65: I/O static characteristics*. Updated *Table 61: EMI characteristics for fHSE / fCPUM4, fCPUM0 = 32 MHz / 64 MHz, 32 MHz*. Minor text edits across the whole document.
18-Aug-2023	9	Updated document title, *Features*, *Section 2: Description*, *Section 3.6: RF subsystem*, *Section 3.6.2: Bluetooth Low Energy general description*, and *Section 3.16: Timers and watchdogs*. Updated *Table 1: STM32WB50CG and STM32WB30CE device features and peripheral counts*, *Table 19: Main performance at VDD = 3.3 V*, and *Table 51: Low-speed external user clock characteristics*. Added *Section 7.1: Device marking*. Removed former *Device marking for UFQFPN48*.

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