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STM32U385xx

Datasheet

Ultra-low-power Arm® Cortex®-M33 32-bit MCU+TrustZone®+FPU, 144 DMIPS, 1 MB flash memory, 256 KB SRAM, SMPS, crypto



LQFP48 (7 × 7 mm)
LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)



UFQFPN32 (5 x 5 mm)
UFQFPN48 (7 x 7 mm)



UFBGA64 (5 × 5 mm)
UFBGA100 (7 × 7 mm)



WLCSP52, WLCSP68
(3.17 x 3.11 mm)

Product summary	
STM32U385xx	STM32U385CG, STM32U385KG, STM32U385RG, STM32U385VG

Product label



Features

Includes ST state-of-the-art patented technology.

Ultra-low-power

- 1.71 V to 3.6 V power supply
- -40 °C to +105 °C temperature range
- V_{BAT} mode: supply for RTC, 32 x 32-bit backup registers
- 1.6 µA Stop 3 mode with 8-Kbyte SRAM
- 2.2 µA Stop 3 mode with full SRAM
- 3.8 µA Stop 2 mode with 8-Kbyte SRAM
- 4.5 µA Stop 2 mode with full SRAM
- 9.5 µA/MHz Run mode @ 3.3 V (*While(1)* SMPS step-down converter mode)
- 13 µA/MHz Run mode @ 3.3 V/48 MHz (CoreMark® SMPS step-down converter mode)
- 16 µA/MHz Run mode @ 3.3 V/96 MHz (CoreMark® SMPS step-down converter mode)
- Brownout reset (BOR) in all modes except shutdown

Arm® 32-bit Cortex®-M33 CPU with TrustZone® and FPU

ART Accelerator

- 8-Kbyte instruction cache allowing 0-wait-state execution from flash and external memories: frequency up to 96 MHz, MPU, 144 DMIPS and DSP instructions

Power management

- Embedded regulator (LDO) and SMPS step-down converter supporting switch on-the-fly and voltage scaling

Benchmarks

- 1.5 DMIPS/MHz (Dhrystone 2.1)
- 387 CoreMark®(4.09 CoreMark®/MHz)
- 500 ULPMark™-CP
- 117 ULPMark™-CM
- 202000 SecureMark™-TLS

Memories

- 1-Mbyte flash memory with ECC, 2 banks read-while-write
- 256 Kbytes of SRAM including 64 Kbytes with hardware parity check
- OCTOSPI external memory interface supporting SRAM, PSRAM, NOR, NAND, and FRAM memories

Security and cryptography

- Arm® TrustZone® and securable I/Os, memories, and peripherals

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- Flexible life cycle scheme with RDP and password protected debug
- Root of trust due to unique boot entry and secure hide protection area (HDP)
- Secure firmware installation (SFI) from embedded root secure services (RSS)
- Secure data storage with hardware unique key (HUK)
- Secure firmware upgrade
- Support of Trusted firmware for Cortex®M (TF-M)
- Two AES coprocessors, one with side channel attack resistance (SCA) (SAES)
- Public key accelerator, SCA resistant
- Key hardware protection
- Attestation keys
- HASH hardware accelerator
- True random number generator, NIST SP800-90B compliant
- 96-bit unique ID
- 512-byte OTP (one-time programmable)
- Antitamper protection

Clock management

- 4 to 50 MHz crystal oscillator
- 32.768 kHz crystal oscillator for RTC (LSE)
- Internal 16 MHz factory-trimmed RC (±1 %)
- Internal low-power RC with frequency 32 kHz or 250 Hz (±5 %)
- 2 internal multispeed 3 MHz to 96 MHz oscillators
- Internal 48 MHz with clock recovery
- Accurate MSI in PLL-mode and up to 96 MHz with 32.768 kHz, 16 MHz, or 32 MHz crystal oscillator

General-purpose inputs/outputs

- Up to 82 fast I/Os with interrupt capability most 5 V-tolerant and up to 14 I/Os with independent supply down to 1.08 V

Up to 15 timers and 2 watchdogs

- 1x 16-bit advanced motor-control, 3x 32-bit and 3x 16-bit general purpose, 2x 16-bit basic, 4x low-power 16-bit timers (available in Stop mode), 2x watchdogs, 2x SysTick timer
- RTC with hardware calendar, alarms, and calibration

Up to 19 communication peripherals

- 1 USB 2.0 full-speed controller
- 1 SAI (serial audio interface)
- 3 I2C FM+(1 Mbit/s), SMBus/PMBus™
- 2 I3C (SDR), with support of I2C FM+ mode
- 2 USARTs and 2 UARTs (SPI, ISO 7816, LIN, IrDA, modem), 1 LPUART
- 3 SPIs (6 SPIs including 1 with OCTOSPI + 2 with USART)
- 1 CAN FD controller
- 1 SDMMC interface
- 1 audio digital filter with sound-activity detection

12-channel GPDMA controller, functional in Sleep and Stop modes (up to Stop 2)

Up to 21 capacitive sensing channels

- Support touch key, linear, and rotary touch sensors

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Rich analog peripherals (independent supply)

- 2× 12-bit ADC 2.5 Msps, with hardware oversampling
- 12-bit DAC module with 2 D/A converters, low-power sample and hold, autonomous in Stop 1 mode
- 2 operational amplifiers with built-in PGA
- 2 ultralow-power comparators

CRC calculation unit

Debug

- Development support: serial-wire debug (SWD), JTAG, Embedded Trace Macrocell™ (ETM)

All packages are ECOPACK2 compliant.

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1 Introduction

This document provides information on STM32U385xx devices, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging and ordering information.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32U385xx errata sheet (ES0626).

For information on the Arm® Cortex®-M33 core, refer to the *Arm® Cortex®-M33 Processor Technical Reference Manual*, available from the www.arm.com website.

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2 Description

The STM32U385xx devices belong to an ultra low-power microcontrollers family (STM32U3 series) based on the high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 96 MHz.

The Cortex®-M33 core features a single-precision FPU (floating-point unit), that supports all the Arm® single-precision data-processing instructions and all the data types.

The Cortex®-M33 core also implements a full set of DSP (digital signal processing) instructions and a MPU (memory protection unit) that enhances the application security.

STM32U3 series are the first STM32 series based on near-threshold voltage technology to deliver breakthrough improvement in battery life. With near-threshold technology, STM32U3 devices reduce the active consumption down to 10uA/MHz, resulting in far longer battery life for any application.

The devices embed high-speed memories (1-Mbyte flash memory and 256-Kbytes SRAM), one Octo/Quad-SPI flash memory interface, an extensive range of enhanced I/Os, peripherals connected to three APB buses, two AHB buses, and a 32-bit multi-AHB bus matrix.

The STM32U385xx devices embed several protection mechanisms for embedded flash memory and SRAM: readout protection, write protection, secure proprietary code readout protection, secure, and hide protection areas.

These devices offer two 12-bit ADC (2.5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, three general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, three general-purpose 16-bit timers, two basic 16-bit timers and up to four 16-bit low-power timers.

The STM32U385xx devices embed a low-power digital filter dedicated to audio signals (ADF), with one filter supporting sound-activity detection. In addition, up to 21 capacitive sensing channels are available.

STM32U3 series also feature standard and advanced communication interfaces such as:

- Three I2Cs
- Two I3Cs
- Three SPIs and one OCTOSPI
- Two USARTs, two UARTs and one low-power UART
- One SAI
- One SDMMC
- One FDCAN
- One USB full-speed (host, or device)

And several peripherals reinforcing security:

- AES coprocessor with DPA-resistance
- One public key accelerator (PKA), DPA resistant
- One HASH (SHA-256) hardware accelerator
- One true random number generator
- Coupling and chaining bridge (CCB)

The STM32U385xx devices offer high protection against transient and environmental perturbation attacks thanks to several internal monitoring generating secret data erase in case of attack.

The devices operate in the -40 to +105 °C (+110 °C junction) temperature ranges from a 1.71 to 3.6 V power supply.

Some independent power supplies are supported like an analog independent supply input for ADC, DAC, OPAMPs and comparators, a 3.3 V dedicated supply input for USB and up to 14 I/Os, that can be supplied independently down to 1.08 V. A VBAT input is available for connecting a backup battery in order to preserve the RTC functionality and to backup 32 32-bit registers.

The STM32U385xx devices offer 16 packages from 32-pin to 100-pin.

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Table 1. STM32U385xx features and peripheral counts

Peripherals		STM32U385KG	STM32U385CG	STM32U385CGY	STM32U385RG	STM32U385RG YxQ	STM32U385RG YxG	STM32U385VG
Flash memory (Mbytes)		1						
SRAM (KBytes)		256						
OCTOSPI		1 [1]			1			
Timers	Advanced control	1 (16 bit)						
	General purpose	3 (16 bit) + 3 (32 bit)						
	Basic	2 (16 bit)						
	Low power	4						
	SysTick timer	2						
	Watchdog timers (independent, window)	2						
Communication interfaces	SPI	2	3				3 [2]	3
	I2C	2	3					
	I3C	2						
	USART	2						
	UART	1			2		1	2
	LPUART	1						
	SAI	1						
	FDCAN	1						
	USB FS	1 host or 1 device						
	SDMMC	0			1 [3]	1	0	1
Audio digital filter (ADF)		1						
Real time clock (RTC)		Yes						
Tamper pins (legacy/SMPS package)		2/NA	3/3	NA/3	4/3	NA/3	NA/3	5/4
True random number generator		Yes						
SAES, AES		Yes						
Public key accelerator (PKA)		Yes						
HASH		Yes						
Coupling and chaining bridge		Yes						
GPIOs (legacy/SMPS package)		25/NA	37/33	NA/35	51/47	NA/52	NA/47	82/79
Wake-up pins [4] (legacy/SMPS package)		12/NA	17/15	NA/16	18/17	NA/17	NA/15	22/22
Number of I/Os down to 1.08 V (legacy/SMPS package)		0/NA	0/0	NA/0	0/0	NA/0	NA/14	0/0
Number of capacitive channels (legacy/SMPS package)		3/NA	6/5	NA/5	12/11	NA/13	NA/5	21/20
ADC	12-bit ADC	2						

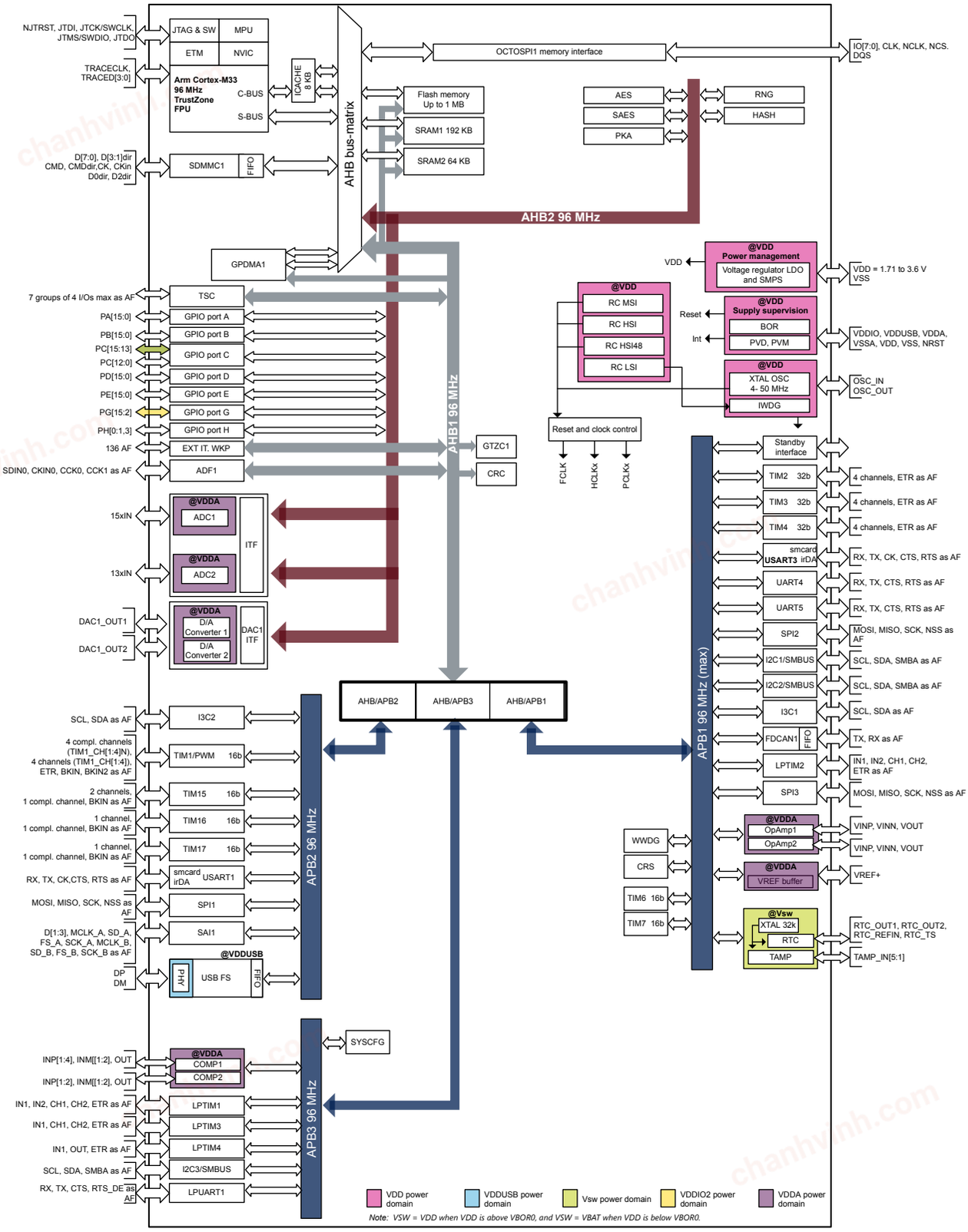
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Peripherals		STM32U385KG	STM32U385CG	STM32U385CGY	STM32U385RG	STM32U385RG YxQ	STM32U385RG YxG	STM32U385VG
ADC	Number of channels (5) (legacy/SMPS package)	10/NA	11/10	NA/11	17/15	NA/17	NA/11	20/18
DAC	12-bit DAC	1						
	Number of 12-bit D/A converters	2						
Internal voltage reference buffer		No						Yes
Analog comparator		2						
Operational amplifiers		2						
Maximum CPU frequency		96 MHz						
Operating voltage		1.71 to 3.60 V						
Operating temperatures		Ambient operating temperature: -40 to 105 °C Junction temperature: -40 to 110 °C						
Package		UFQFPN32	LQFP48, UFQFPN48	WLCSP52	LQFP64, UFBGA64	WLCSP68	WLCSP68	LQFP100, UFBGA100

1. *Only single-mode, dual-mode, and quad-mode are supported.*
2. *SPI 2 is partially supported with only SCK/MISO/MOSI signals.*
3. *Command direction signal not supported on devices with SMPS.*
4. *Maximum of 8 pins can be used simultaneously.*
5. *Number of pins with at least one ADC channel.*

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Figure 1. **STM32U385xx block diagram**



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3 Functional overview

3.1 Arm®Cortex®-M33 core with TrustZone® and FPU

The Cortex®-M33 with TrustZone® and FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex®-M33 processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. It features:

- Arm® TrustZone® technology, using the Armv8_M main extension supporting secure and nonsecure states
- MPUs (memory protection units), supporting up to 16 regions for secure and nonsecure applications
- Configurable SAU (secure attribute unit) supporting up to eight memory regions as secure or nonsecure
- Floating-point arithmetic functionality with support for single-precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex®-M33 processor supports the following bus interfaces:

- System AHB bus:
  The S-AHB (system AHB) bus interface is used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, external RAM and external device, or Vendor_SYS regions of the Armv8-M memory map.
- Code AHB bus:
  The C-AHB (code AHB) bus interface is used for any instruction fetch and data access to the code region of the Armv8-M memory map.

Figure 1 shows the general block diagram of the STM32U385xx devices.

3.2 Instruction cache (ICACHE)

The ICACHE is introduced on the C-AHB code bus of the Cortex®-M33 processor to improve performance when fetching instruction (or data) from both internal and external memories.

ICACHE offers the following features:

- Multibus interface:
  - Slave port receiving the memory requests from the Cortex®-M33 C-AHB code execution port
  - Master1 port performing refill requests to internal memories (Flash memory and SRAMs)
  - Master2 port performing refill requests to external memories (external flash memory and RAMs through Octo-SPI interface)
  - Second slave port dedicated to ICACHE registers access
- Close to zero wait-states instructions/data access performance:
  - 0 wait-state on cache hit
  - Hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - Critical-word-first refill policy, minimizing processor stalls on cache miss
  - Hit ratio improved by two-ways set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - Dual master ports allowing to decouple internal and external memory traffics, on fast and slow buses, respectively; also minimizing impact on interrupt latency
  - Optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - Performance monitoring by means of a hit counter and a miss counter
- Extension of cacheable region beyond the code memory space, by means of address remapping logic that allows four cacheable external regions to be defined
- Power consumption reduced intrinsically (more accesses to cache memory rather to bigger main memories); even improved by configuring ICACHE as direct mapped (rather than the default two-ways set-associative mode)
- TrustZone® security support

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- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

3.3 Memory protection unit

The MPU (memory protection unit) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to 16 protected areas. The MPU regions and registers are banked across secure and nonsecure states.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (realtime operating system).

If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded flash memory

The devices feature 1 Mbyte of embedded flash memory that is available for storing programs and data. The flash memory supports up to 10 000 cycles.

A 64-bit instruction prefetch is implemented and can optionally be enabled.

The flash memory interface features:

- Dual-bank operating modes
- Read-while-write (RWW)

This allows a read operation to be performed from one bank while an erase or program operation is performed to the other bank. The dual-bank boot is also supported. Each bank contains 128 pages of 4 Kbytes. The flash memory also embeds 512-byte OTP (one-time programmable) for user data.

Note: Program, erase, and option change operations are only allowed in Range 1. An error is reported when those operations are launched in Range 2.

The option bytes allow the configuration of flexible protections:

- Readout protection (RDP) to protect the whole memory, has four levels of protection available (see Table 2 and Table 3).
  - Level 0: no readout protection
  - Level 0.5: available only when TrustZone® is enabled
    All read/write operations (if no write protection is set) from/to the nonsecure flash memory are possible. The debug access to secure area is prohibited. Debug access to nonsecure area remains possible.
  - Level 1: memory readout protection
    The flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected. If TrustZone® is enabled, the nonsecure debug is possible and the boot in SRAM is not possible. Regressions from Level 1 to lower levels can be protected by password authentication.
  - Level 2: chip readout protection
    The debug features (Cortex®-M33 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled. A secure secret key can be configured in the secure options to allow the regression capability from Level 2 to Level 1. By default, this Level 2 selection is irreversible. If the secret key was previously configured in lower RDP levels, the device enables the RDP regression from Level 2 to Level 1 after password authentication through JTAG/SWD interface.

  Note: In order to reach the best protection level, it is recommended to activate TrustZone® and to set the RDP Level 2 with password authentication regression enabled.
- Write protection (WRP) to protect areas against erasing and programming. Two areas per bank can be selected with 4-Kbyte granularity.

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Table 2. Access status versus protection level and execution modes when TZEN = 0

Area	RDP level	User execution (boot from flash memory)			Debug/boot from RAM/bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Flash main memory	1	Yes	Yes	Yes	No	No	No(2)
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory(3)	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes(4)	1	Yes	Yes(2)	N/A	Yes	Yes(2)	N/A
	2	Yes	No(5)	N/A	N/A	N/A	N/A
OTP	1	Yes	Yes(6)	N/A	Yes	Yes(6)	N/A
	2	Yes	Yes(6)	N/A	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A	No	No	N/A(7)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	N/A	No	No	N/A(8)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. *When the protection level 2 is active, the debug port, the boot from RAM and the boot from system memory are disabled.*
2. *The flash main memory is erased when the RDP option byte changes from level 1 to level 0.*
3. *The system memory is only read-accessible, whatever the protection level (0, 1 or 2) and execution mode.*
4. *Option bytes are only accessible through the flash memory interface registers and OPSTRT bit.*
5. *SWAP_BANK option bit can be modified.*
6. *OTP can only be written once.*
7. *The backup registers are erased when RDP changes from level 1 to level 0.*
8. *All SRAMs are erased when RDP changes from level 1 to level 0.*

Table 3. Access status versus protection level and execution modes when TZEN = 1

Area	RDP level	User execution (boot from flash memory)			Debug/boot from RAM/bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Flash main memory	1	Yes	Yes	Yes	No	No	No(4)
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory(2)	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes(3)	1	Yes	Yes(4)	N/A	Yes	Yes(4)	N/A
	2	Yes	No(5)	N/A	N/A	N/A	N/A
OTP	1	Yes	Yes(6)	N/A	Yes	Yes(6)	N/A
	2	Yes	Yes(6)	N/A	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A	No	No	N/A(7)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	N/A	No	No	N/A(8)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. *When the protection level 2 is active, the debug port, the boot from RAM and the boot from system memory are disabled.*
2. *The system memory is only read-accessible, whatever the protection level (0, 1 or 2) and execution mode.*
3. *Option bytes are only accessible through the flash registers interface and OPTSTRT bit.*

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4. *The flash main memory is erased when the RDP option byte changes from level 1 to level 0.*
5. *SWAP_BANK option bit can be modified.*
6. *OTP can only be written once.*
7. *The backup registers are erased when RDP changes from level 1 to level 0.*
8. *All SRAMs are erased when RDP changes from level 1 to level 0.*

The whole nonvolatile memory embeds the error correction code (ECC) feature supporting:

- Single-error detection and correction
- Double-error detection
- ECC fail address report

3.4.1 TrustZone® security

When the TrustZone® security is enabled through option bytes, the whole flash memory is secure after reset and the following protections are available:

- Nonvolatile watermark based secure flash memory area
  The secure area can be accessed only in secure mode. One area per bank can be selected with a page granularity.
- Secure hide-protection area (HDP) and secure hide-protection extension area
  It is part of the flash memory secure area and can be protected to deny access to this area by any data read, write, and instruction fetch. For example, a software code in the secure flash memory hide-protection area can be executed only once and deny any further access to this area until the next system reset. One area per bank can be selected in the secure area. This area can be extended by pages that belong to the secure area (HDP extension).
- Volatile block based secure flash memory area
  Each page can be programmed on-the-fly as secure or nonsecure.

3.4.2 Privilege protection

Each flash memory page can be programmed on the fly as privileged or unprivileged.

3.5 Embedded SRAM

The STM32U385xx devices feature 256 Kbytes of SRAM, made of several blocks that can be powered down in Stop mode to reduce consumption:

- SRAM1: 2 × 16 Kbytes + 5 × 32 Kbytes blocks (total 192 Kbytes)
- SRAM2: 8 Kbytes + 24 Kbytes + 32 Kbytes blocks (total 64 Kbytes) with optional hardware parity check. In addition, SRAM2 blocks can be retained in Standby mode.

3.5.1 TrustZone® security

When the TrustZone® security is enabled, all SRAMs are secure after reset. Both SRAMs can be programmed as secure or nonsecure by blocks, using the MPCBB (block-based memory protection controller).

The granularity of SRAM secure block based is a page of 512 bytes.

3.5.2 Privilege protection

Both SRAMs can be programmed as privileged or unprivileged by blocks, using the MPCBB. The granularity of SRAM privilege block based is a page of 512 bytes.

3.6 Boot modes

At startup, a BOOT0 pin, nBOOT0 and nSWBOOT0 option bits of the FLASH_OPTR register, and ADD[24:0] option bytes of the FLASH_BOOT0R, FLASH_BOOT1R or FLASH_SBOOT0R registers are used to select the boot memory address that includes:

- Boot from any address in user flash memory.
- Boot from the system memory bootloader.
- Boot from any address in embedded SRAM.
- Boot from RSS (root security services).

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The BOOT0 value comes from the PH3-BOOT0 (PB7-BOOT0 for STM32U385KG) pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

The bootloader is located in the system memory, programmed by ST during production. The bootloader is used to reprogram the flash memory by using USART, I2C, SPI, FDCAN, or USB FS in device mode through the DFU (device firmware upgrade).

The bootloader is available on all devices. Refer to the application note STM32 microcontroller system memory boot mode (AN2606) for more details.

The embedded RSS are located in the secure information block, programmed by ST during production.

For example, the RSS enable the SFI (secure firmware installation), thanks to the RSSe SFI (RSS extension firmware).

This feature allows the customer to produce the confidentiality of the firmware to be provisioned into the STM32, when production is sub-contracted to untrusted third-party.

The RSS are available on all devices, after enabling the TrustZone® through the TZEN option bit. Refer to the application note overview secure firmware install (SFI) (AN4992) for more details.

Refer to Table 4 and Table 5 for boot modes when TrustZone® is disabled and enabled respectively.

Table 4. Boot modes when TrustZone® is disabled (TZEN = 0)

NBOOT0	BOOT0 pin	NSWBOOT0	Boot address option-byte selection	Boot area	ST programmed default value
-	0	1	ADD[24:0] in FLASH_BOOT0R	Nonsecure boot base address 0 defined by user option bytes in FLASH_BOOT0R	Flash: 0x0800 0000
-	1	1	ADD[24:0] in FLASH_BOOT1R	Nonsecure boot base address 0 defined by user option bytes in FLASH_BOOT1R	Bootloader: 0x0BF8 F000
1	-	0	ADD[24:0] in FLASH_BOOT0R	Nonsecure boot base address 0 defined by user option bytes in FLASH_BOOT0R	Flash: 0x0800 0000
0	-	0	ADD[24:0] in FLASH_BOOT1R	Nonsecure boot base address 0 defined by user option bytes in FLASH_BOOT1R	Bootloader: 0x0BF8 F000

When TrustZone® is enabled by setting the TZEN option bit, the boot space must be in the secure area. The ADD[24:0] option bytes in FLASH_SBOOT0R register option bytes are used to select the boot secure memory address.

A unique boot entry option can be selected by setting the BOOT_LOCK option bit, allowing to boot always at the secure base boot address selected by user option bytes. All other boot options are ignored.

Table 5. Boot modes when TrustZone® is enabled (TZEN = 1)

BOOT_LOCK	NBOOT0	BOOT0 pin	NSWBOOT0	RSS command	Boot address option-byte selection	Boot area	ST programmed default value
0	-	0	1	0	ADD[24:0] in FLASH_SBOOT0R	Secure boot base address 0 defined by user option bytes in FLASH_SBOOT0R	Flash: 0x0C00 0000
	-	1	1	0	N/A	RSS	RSS: 0x0FF8 0000
	1	-	0	0	ADD[24:0] in FLASH_SBOOT0R	Secure boot base address 0 defined by user option bytes in FLASH_SBOOT0R	Flash: 0x0C00 0000
	0	-	0	0	N/A	RSS	RSS: 0x0FF8 0000
	-	-	-	≠0	N/A	RSS	RSS: 0x0FF8 0000
1	-	-	-	-	ADD[24:0] in FLASH_SBOOT0R	Secure boot base address 0 defined by user option bytes in FLASH_SBOOT0R	Flash: 0x0C00 0000

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The boot address option bytes allow any boot memory address to be programmed. However, the allowed address space depends on the flash memory RDP level.

If the programmed boot memory address is out of the allowed memory-mapped area when RDP level is 0.5 or more, the default boot address is forced either in secure flash memory or nonsecure flash memory, depending on the TrustZone® security option as described in the table below.

Table 6. Boot space versus RDP protection

RDP	TZEN = 1	TZEN = 0
0	Any boot address	Any boot address
0.5	Boot address only in RSS (0x0FF8 0000) or secure flash memory: 0x0C00 0000 - 0x0C0F FFFF Otherwise, the forced boot address is 0x0FF8 0000.	N/A
1		Any boot address
2		Boot address only in flash memory 0x0800 0000 - 0x080F FFFF Otherwise, forced boot address is 0x0800 0000.

3.7 Global TrustZone® controller (GTZC)

GTZC is used to configure TrustZone® and privileged attributes within the full system.

The GTZC includes three different subblocks:

- TZSC: TrustZone® security controller
  This sub-block defines the secure/privileged state of slave peripherals. The TZSC informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.
- TZIC: TrustZone® illegal access controller
  This subblock gathers all security illegal access events in the system and generates a secure interrupt towards NVIC.
- MPCBB: Memory protection controller - block-based
  This sub-block configures the internal RAM in a TrustZone®-system product having segmented SRAM (pages of 512 bytes) with programmable-security and privileged attributes.

The GTZC main features are:

- Three independent 32-bit AHB interfaces for TZSC, TZIC, and MPCBB
- TZIC accessible only with secure transactions
- Secure and nonsecure access supported for privileged/unprivileged part of TZSC and MPCBB
- Set of registers to define product security settings:
  - Secure/privileged blocks for internal SRAMs
  - Secure/privileged access mode for securable peripherals
  - Secure/privileged access mode for securable masters

3.7.1 TrustZone® security architecture

The security architecture is based on Arm® TrustZone® with the Armv8_M main extension.

When the TrustZone® is enabled, the SAU (security attribution unit) and IDAU (implementation defined attribution unit) define the access permissions based on secure and nonsecure state.

- SAU: up to eight SAU configurable regions are available for security attribution.
- IDAU: It provides a first memory partition as nonsecure or nonsecure callable attributes. It is then combined with the results from the SAU security attribution and the higher security state is selected.

Based on IDAU security attribution, the flash memory, system SRAMs and peripherals memory space are aliased twice for secure and nonsecure states. However, the external memory space is not aliased.

Table 7 shows an example of typical SAU regions configuration based on IDAU regions. The user can split and choose the secure, nonsecure, or NSC regions for external memories as needed.

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Table 7. Example of memory map security attribution versus SAU configuration regions

Region description	Address range	IDAU security attribution	SAU security attribution typical configuration	Final security attribution
Code external memories	0x0000 0000 0x07FF FFFF	Nonsecure	Secure or nonsecure or NSC (1)	Secure or nonsecure or NSC
Code flash and SRAM	0x0800 0000 0x0BFF FFFF	Nonsecure		
	0x0C00 0000 0x0FFF FFFF	NSC	Secure or NSC	Secure or NSC
Code external memories	0x1000 0000 0x17FF FFFF	Nonsecure		
	0x1800 0000 0x1FFF FFFF			
SRAM	0x2000 0000 0x2FFF FFFF			
	0x3000 0000 0x3FFF FFFF	NSC	Secure or NSC	Secure or NSC
Peripherals	0x4000 0000 0x4FFF FFFF	Nonsecure		
	0x5000 0000 0x5FFF FFFF	NSC	Secure or NSC	Secure or NSC
External memories	0x6000 0000 0xDFFF FFFF	Nonsecure	Secure or nonsecure or NSC	Secure or nonsecure or NSC

1. *NSC = nonsecure callable.*

3.7.2 TrustZone®peripheral classification

When the TrustZone® security is active, a peripheral can be either securable or TrustZone®-aware type as follows:

- Securable: peripheral protected by an AHB/APB firewall gate that is controlled from TZSC to define security properties
- TrustZone®-aware: peripheral connected directly to AHB or APB bus and implementing a specific TrustZone® behavior such as a subset of registers being secure

3.7.3 Default TrustZone® security state

The default system security state is detailed below:

- CPU:
  - Cortex®-M33 is in a secure state after reset. The boot address must be in a secure address.
- Memory map:
  - SAU is fully secure after reset. Consequently, all memory map is fully secure. Up to eight SAU configurable regions are available for security attribution.
- Flash memory:
  - Flash memory security area is defined by watermarking user options.
  - Flash memory block-based area is nonsecure after reset.
- SRAMs:
  - All SRAMs are secure after reset. MPCBBx (memory protection block-based controllers) are secure.

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- External memories:
  - OCTOSPI does not support any TrustZone® protection.
- Peripherals
  - Securable peripherals are nonsecure after reset.
  - TrustZone®-aware peripherals are nonsecure after reset. Their secure configuration registers are secure.
- All GPIOs are secure after reset.
- Interrupts:
  - NVIC: All interrupts are secure after reset. NVIC is banked for secure and nonsecure state.
  - TZIC: All illegal access interrupts are disabled after reset.

3.8 Power supply management

The PWR (power controller) main features are:

- Power supplies and supply domains
  - Core domain (VCORE)
  - V_{DD} domain
  - Backup domain (V_{BAT})
  - Analog domain (V_{DDA})
  - SMPS power stage (V_{DDSMPS}, available only on SMPS packages)
  - V_{DDIO2} domain
  - V_{DDUSB} for USB transceiver
- System supply voltage regulation
  - SMPS step-down converter
  - Voltage regulator (LDO)
- Power supply supervision
  - BOR monitor
  - PVD monitor
  - PVM monitor (V_{DDA}, V_{DDUSB}, V_{DDIO2})
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes
- V_{BAT} battery charging
- TrustZone® security and privileged protection

3.8.1 Power supply schemes

The devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals. Those supplies must not be provided without a valid operating supply on the VDD pin:

- V_{DD} = 1.71 V to 3.6 V (functionality guaranteed down to V_{BORx} min value)

V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.

- V_{DDA} = 1.58 V (COMPs) / 1.6 V (DACs, OPAMPs) / 1.62 V (ADCs) / 1.8 V (VREFBUF) to 3.6 V

V_{DDA} is the external analog power supply for ADCs, DACs, voltage reference buffer, operational amplifiers, and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and must be connected to the VDD pin when these peripherals are not used.

- V_{DDSMPS} = 1.71 V to 3.6 V

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V_{DDSMPS} is the external power supply for the SMPS step-down converter. It is provided externally through a VDDSMPS supply pin. It must be connected to the same supply VDD pin when the SMPS is used in the application. When the SMPS is not used, it is recommended to connect both V_{DDSMPS} and V_{LXSMPS} to GND.

- V_{LXSMPS} is the switched SMPS step-down converter output.

Note: The SMPS power supply pins are available only on a specific package with SMPS step-down converter option.

- V_{DDUSB} = 3.0 V to 3.6 V

V_{DDUSB} is the external independent power supply for USB transceivers. V_{DDUSB} voltage level is independent from the V_{DD} voltage and must be connected to VDD or VSS pin (preferably to VDD) when the USB is not used.

- V_{DDIO2} = 1.08 V to 3.6 V

V_{DDIO2} is the external power supply for 14 I/Os (port G[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage and must be connected to VDD or VSS pin (preferably to VDD) when PG[15:2] are not used.

- V_{BAT} = 1.65 V to 3.6 V (functionality guaranteed down to V_{BOR_VBAT} min value)

V_{BAT} is the power supply when VDD is not present (through power switch) for RTC, TAMP, external 32 kHz oscillator, and backup registers.

- V_{REF-}, V_{REF+}

V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

V_{REF+} can be grounded when ADC and DAC are not active.

The internal voltage reference buffer supports four output voltages:

- V_{REF+} around 1.5 V. This requires $V_{DDA} \geq 1.8$ V.
- V_{REF+} around 1.8 V. This requires $V_{DDA} \geq 2.1$ V.
- V_{REF+} around 2.048 V. This requires $V_{DDA} \geq 2.4$ V.
- V_{REF+} around 2.5 V. This requires $V_{DDA} \geq 2.8$ V.

VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.

When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled.

V_{REF-} must always be equal to V_{SSA}.

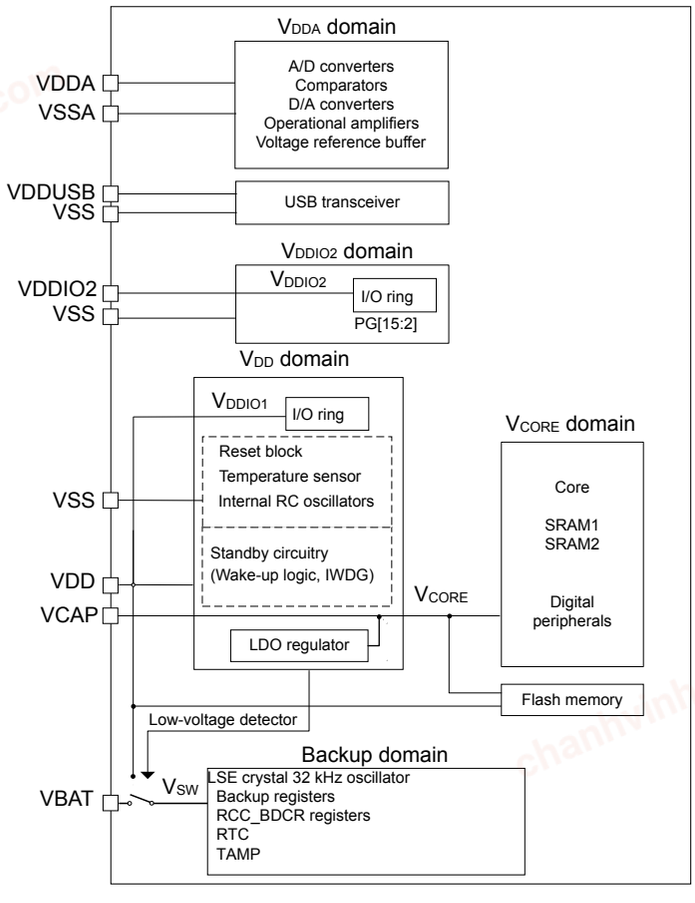
The STM32U385xx devices embed two regulators: one LDO and one SMPS in parallel to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, and embedded flash memory. The SMPS generates this voltage on VDD11 (two pins), with a total external capacitor of 4.7 µF typical. SMPS requires an external coil of 2.2 µH typical. The LDO generates this voltage on a VCAP pin connected to an external capacitor of 4.7 µF typical.

Both regulators can provide two different voltages (voltage scaling) and can operate in Stop mode.

It is possible to switch from SMPS to LDO and from LDO to SMPS on-the-fly.

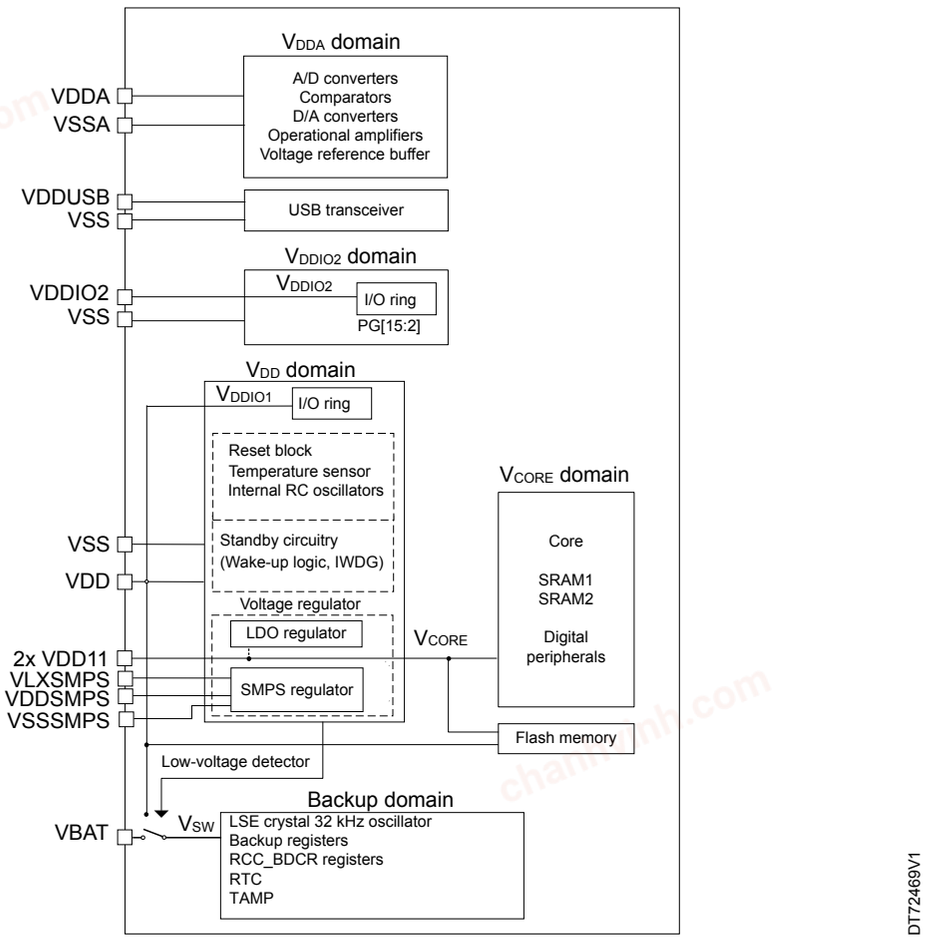
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Figure 2. STM32U385xx power supply overview (without SMPS)



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Figure 3. **STM32U385xxxxQ power supply overview (with SMPS)**



In this document, V_{DDIOx} (with x = 1 or 2) refers to the I/O power supply. V_{DDIO1} is supplied by V_{DD}. V_{DDIO2} is the independent power supply for PG[15:2].

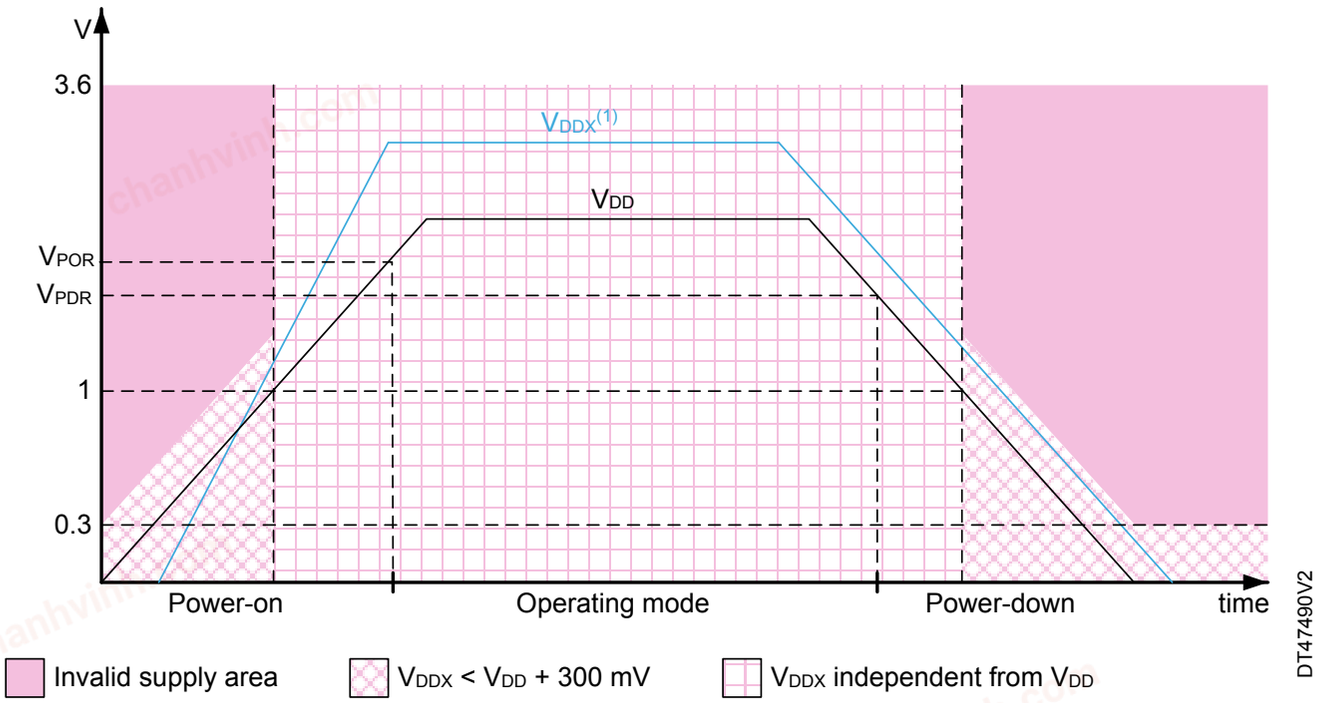
V_{SW} = V_{DD} when V_{DD} is above V_{BOR0}, and V_{SW} = V_{BAT} when V_{DD} is below V_{BOR0}.

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the powerdown transient phase.

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Figure 4. **Power-up/down sequence**



1. *V_{DDX} refers to any power supply among V_{DDA}, V_{DDUSB}, and V_{DDIO2}.*

3.8.2 Power supply supervisor

The device has an integrated brownout reset (BOR) circuitry. The BOR is active in all power modes (except for Shutdown mode), and cannot be disabled.

During power-on, the BOR keeps the device under reset until the supply voltage V_{DD} reaches the specified VBORx threshold. When V_{DD} drops below the selected threshold, a device reset is generated. When V_{DD} is above the VBORx upper limit, the device reset is released and the system can start.

Five BOR thresholds can be selected through option bytes. BOR0 provides the always enabled power-on/ powerdown functionality, independent from any other higher BOR level selection.

The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below and/or rises above the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor that compares the independent supply voltages V_{DDA}, V_{DDUSB}, and V_{DDIO2} to ensure that the peripheral is in its functional supply range.

The devices support dynamic voltage scaling. The dynamic voltage scaling is a power management technique that consists in increasing or decreasing the voltage used for the digital peripherals (V_{CORE}), according to the application performance and power consumption needs.

The regulator operates in the following ranges:

- Range 1 (V_{CORE} = 0.9 V) with CPU and peripherals running at up to 96 MHz
- Range 2 (V_{CORE} = 0.75 V) with CPU and peripherals running at up to 48 MHz

3.8.3 Reset mode

In order to improve the consumption under reset, the I/O state under and after reset is "analog state" (the I/O Schmitt trigger is disabled). In addition, when the reset source is internal (not coming from the NRST pin), the built-in pull-up resistor on the NRST pin is deactivated.

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3.8.4 VBAT operation

The VBAT pin allows the device V_{BAT} domain to be powered from an external battery or an external supercapacitor.

The VBAT pin supplies the RTC with LSE, antitamper detection (TAMP), backup registers. Five antitamper detection pins are available in V_{BAT} mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal V_{BAT} battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from V_{BAT}, neither external interrupts nor RTC/TAMP alarm/events exit the microcontroller from the V_{BAT} operation.

3.8.5 PWR TrustZone® security

When the TrustZone® security is activated by the TZEN option bit, some PWR register fields can be secured against nonsecure access.

The PWR TrustZone® security allows the following features to be secured:

- Low-power mode
- WKUP (wake-up) pins
- Voltage detection and monitoring
- V_{BAT} mode
- I/Os pull-up/pull-down configuration

Other PWR configuration bits are secure when:

- The system clock selection is secure in RCC: the voltage scaling configuration and the regulator booster (BOOSTEN) are secure.
- A GPIO is configured as secure: its corresponding bit for pull-up/pull-down configuration in Standby mode is secure.

3.9 Low-power modes

The ultra-low-power STM32U385xx devices support several low-power modes to save power when the CPU does not need to be kept running, for example when waiting for an external event. It is up to the user to select the mode that gives the best compromise between low-power consumption, short startup time, and available wake-up sources.

Table 8. STM32U385xx low-power modes overview details the related low-power modes.

Table 8. STM32U385xx low-power modes overview

Mode name	Entry	Wake-up source	Wake-up system clock	Effect on clocks	Voltage regulators
Sleep (Sleep-now or Sleep-on-exit)	WFI or return from ISR	Any interrupt	Same as before entering Sleep mode	CPU clock OFF No effect on other clocks or analog clock sources	Range 1, 2
	WFE	Wake-up event			
Stop 0	LPMS = 000 + SLEEPDEEP bit + WFI or return from ISR or WFE	Any EXTI line (configured in the EXTI registers) Any PWR wake-up line (WKUP pins and I3C reset pattern) Specific peripherals events/interrupts(1)	HSI16 when STOPWUCK = 1 in RCC_CFGR1 MSIS with the frequency before entering the Stop mode, limited to 48 MHz, when STOPWUCK = 0	All clocks OFF except LSI and LSE MSIK, MSIS or HSI16 can be enabled temporarily when requested by an autonomous peripheral, or forced to be kept enabled.	Range 1, 2
Stop 1	LPMS = 001 + SLEEPDEEP bit + WFI or return from ISR or WFE				Low-power regulator (SMPS or LDO)
Stop 2	LPMS = 010 + SLEEPDEEP bit + WFI or return from ISR or WFE				

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Mode name	Entry	Wake-up source	Wake-up system clock	Effect on clocks	Voltage regulators
Stop 3	LPMS = 011 + SLEEPDEEP bit + WFI or return from ISR or WFE	WKUP pin edge, RTC/TAMP events/ interrupts (1), external reset in NRST pin, IWDG events/ interrupts (1) or reset, I3C reset pattern	HSI16 when STOPWUCK = 1 in RCC_CFGR1 MSIS with the frequency before entering the Stop mode, limited to 48 MHz, when STOPWUCK = 0	All clocks OFF except LSI and LSE	Low-power regulator (SMPS or LDO)
Standby with SRAM2_ 8 Kbytes	LPMS = 10x+ RRS1 = 1 + SLEEPDEEP bit + WFI or return from ISR or WFE		MSIS from 3 MHz up to 12 MHz		
Standby with SRAM2_Full	LPMS = 10x+ RRS1 = RRS2 = RRS3 = 1+ SLEEPDEEP bit + WFI or return from ISR or WFE				
Standby	LPMS = 10x + RRS1 = RRS2 = RRS3 = 0 + SLEEPDEEP bit + WFI or return from ISR or WFE				OFF
Shutdown	LPMS = 11x + SLEEPDEEP bit + WFI or return from ISR or WFE	WKUP pin edge, RTC/TAMP events/ interrupts (1), external reset in NRST pin, I3C reset pattern	MSIS 12 MHz	All clocks OFF except LSE	OFF

1. *A wake-up event from Stop mode can be generated with the peripheral interrupt signal.*

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode
  CPU clock off, all peripherals including Cortex®-M33 core such as NVIC and SysTick can run and wake up the CPU when an interrupt or an event occurs.
- **Stop 0, Stop 1, Stop 2, and Stop 3** modes
  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. The SRAMs can be totally or partially switched off to further reduce consumption. All clocks in the core domain are stopped. The MSI (MSIS and MSIK) RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.
  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).
  Some peripherals are autonomous and can operate in Stop mode by requesting their kernel clock and their bus (APB or AHB) when needed, in order to transfer data with GPDMA1 depending on peripherals and power mode.
  In Stop 0 mode, the regulator remains in main regulator mode, allowing a very fast wake-up time but with much higher consumption.
  In Stop 1, the regulator is in low-power mode, and the whole core domain is fully powered. All autonomous peripherals are functional.
  In Stop 2 mode, most of the core domain (D1 domain) is put in a lower leakage mode, keeping registers retention, but without any possible functionality. The D2 domain, embedding APB3 peripherals, is kept fully powered, so those peripherals can be kept functional.
  Stop 3 is the lowest power mode with full retention, but the functional peripherals and sources of wake-up are reduced to the same ones than in Standby mode.
  The system clock when exiting from Stop mode can be either MSIS up to 48 MHz or HSI16, depending on software configuration.

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- **Standby** mode
The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the core domain is powered off. The MSI (MSIS and MSIK) RC, the HSI16 RC and the HSE crystal oscillators are also switched off.
The RTC can remain active (Standby mode with RTC, Standby mode without RTC).
The brownout reset (BOR) always remains active in Standby mode.
The state of each I/O during Standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.
After entering Standby mode, SRAMs and register contents are lost except for registers in the backup domain and Standby circuitry. Optionally, the full SRAM2 or 8 Kbytes or 24 Kbytes or 32 Kbytes can be retained in Standby mode, supplied by the low-power regulator (standby with SRAM2 retention mode).
The BOR can be configured in ultra-low-power mode to further reduce power consumption during Standby mode.
The device exits Standby mode when an external reset (NRST pin), an IWDG early wake-up event or reset, WKUP pin event (configurable rising or falling edge), an RTC event (alarm, periodic wake-up, timestamp), a tamper detection, or a I3C reset pattern detection occurs.
The system clock after wake-up is MSIS up to 12 MHz.
- **Shutdown** mode
The Shutdown mode allows the lowest power consumption. The internal regulator is switched off so that the core domain is powered off. The HSI16, the MSI (MSIS and MSIK), the LSI, and the HSE oscillators are also switched off.
The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).
The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to backup domain is not supported.
SRAMs and register contents are lost except for registers in the backup domain.
The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wake-up, timestamp), a tamper detection or a I3C reset pattern detection.
The system clock after wake-up is MSIS at 12 MHz.

3.9.1 Autonomous peripherals

Several peripherals support the autonomous mode that allows it to be functional and perform DMA transfers in Stop 0, Stop 1, and Stop 2 modes. Their interrupts wake up from Stop mode.

In Stop 0 and Stop 1 modes, the autonomous peripherals are DAC1 (2 channels), LPTIMx (x = 1 to 4), U(S)ARTx (x = 1, 3, 4, 5), LPUART1, SPIx (x = 1 to 3), I2Cx (x = 1 to 3), I3Cx (x = 1 to 2), ADF1 , and GPDMA1.

In Stop 2 mode, the autonomous peripherals are LPTIM1, LPTIM3, LPTIM4, LPUART1, and I2C3. If one of these peripherals requests the AHB/APB clocks for a DMA transfer, the whole core domain is switched to Stop 1 higher leakage mode and the clock is distributed to GPDMA1, enabled SRAMs, and peripherals in order to perform the autonomous peripheral DMA transfer. Then the core domain automatically returns to Stop 2 lower leakage mode.

Table 9. Functionalities depending on the working mode

Y = yes (enable). O = optional (disable by default, can be enabled by software). - = not available.

Peripheral	Run	Sleep	Stop 0/1		Stop 2		Stop 3		Standby		Shutdown		VBAT
			-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
CPU	Y	-	-	-	-	-	-	-	-	-	-	-	-
Flash memory (1 Mbyte)	O(1)	O(1)	-	O(2)	-	O(2)	-	-	-	-	-	-	-
SRAM1 (192 Kbytes)	Y(3)	Y(4)	O(5)	-	O(5)	-	O(5)	-	-	-	-	-	-
SRAM2 (64 Kbytes)	Y(3)	Y(4)	O(5)	O(6)	O(5)	O(6)	O(5)	-	O(7)	-	-	-	-
OCTOSPI1	O	O	-	-	-	-	-	-	-	-	-	-	-
Backup registers	Y	Y	Y	-	Y	-	Y	-	Y	-	Y	-	Y

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Peripheral	Run	Sleep	Stop 0/1		Stop 2		Stop 3		Standby		Shutdown		VBAT
			-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	-	-	-	-	-	-	-
Peripheral voltage monitor	O	O	O	O	O	O	-	-	-	-	-	-	-
GTZC	O	O	O	O(8)	O	O(8)	-	-	-	-	-	-	-
RAMCFG	O	O	O	O(6)	O	O(6)	-	-	-	-	-	-	-
GPDMA1	O	O	O(9)	O(9)	O(10)	O(10)	-	-	-	-	-	-	-
High-speed internal (HSI16)	O	O	(11)	-	(11)	-	-	-	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High-speed external (HSE)	O	O	-	-	-	-	-	-	-	-	-	-	-
Low-speed internal (LSI)	O	O	O	-	O	-	O	-	O	-	-	-	-
Low-speed external (LSE)	O	O	O	-	O	-	O	-	O	-	O	-	O
Multi-speed internal (MSIS and MSIK)	O	O	(11)	-	(11)	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	-	-	-	-	-	-	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	O	O	O
RTC/TAMP	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of TAMP tamper pins	5	5	5	O	5	O	5	O	5	O	5	O	5
USB	O	O	-	O	-	-	-	-	-	-	-	-	-
USARTx (x = 1, 3, 4, 5)	O	O	O(12)	O(12)	-	-	-	-	-	-	-	-	-
Low-power UART (LPUART1)	O	O	O(12)	O(12)	O(12)	O(12)	-	-	-	-	-	-	-
I2Cx (x = 1, 2)	O	O	O(13)	O(13)	-	-	-	-	-	-	-	-	-
I2C3	O	O	O(13)	O(13)	O(13)	O(13)	-	-	-	-	-	-	-
I3Cx (x=1, 2)	O	O	O(14)	O(14)	-	O(15)	-	O(15)	-	O(15)	-	O(15)	-
SPIx (x = 1, 2, 3)	O	O	O(16)	O(16)	-	-	-	-	-	-	-	-	-
FDCAN1	O	O	-	-	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	-	-	-	-	-	-	-	-	-	-	-
SAI1	O	O	-	-	-	-	-	-	-	-	-	-	-
ADC12	O	O	-	-	-	-	-	-	-	-	-	-	-
DAC1 (2 converters)	O	O	O(17)	-	-	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	-	-	-	-	-	-	-	-	-	-
OPAMPx (x = 1, 2)	O	O	O	-	-	-	-	-	-	-	-	-	-
COMPx (x = 1, 2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Temperature sensor	O	O	O	-	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	-	-	-	-	-	-	-	-	-	-	-

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Peripheral	Run	Sleep	Stop 0/1		Stop 2		Stop 3		Standby		Shutdown		VBAT
			-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
LPTIMx (x = 1, 3, 4)	O	O	O[18]	O[18]	O[18]	O[18]	-	-	-	-	-	-	-
LPTIM2	O	O	O[18]	O[18]	-	-	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	-	-	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	-	-	-	-	-	-	-	-	-	-	-
Audio digital filter (ADF)	O	O	O[19]	O[19]	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	-	-	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O	O	-	-	-	-	-	-	-	-	-	-	-
AES and secure AES	O	O	-	-	-	-	-	-	-	-	-	-	-
Public key accelerator (PKA)	O	O	-	-	-	-	-	-	-	-	-	-	-
HASH accelerator	O	O	-	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	-	-	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	[20]	22 pins	[20]	22 pins	[21]	22 pins	-

1. *The flash banks can be configured in power-down mode. By default, they are not in power-down mode.*
2. *Flash can be accessed by GPDMA1 in Stop 0, Stop 1 and Stop 2 modes. ECC error interrupt or NMI wakes up from these Stop modes.*
3. *The SRAMs can be definitively powered off independently until the next device power on reset.*
4. *The SRAM clock can be gated on or off independently.*
5. *Subblocks of SRAM1 and SRAM2 can be powered-off to save power consumption. SRAM1 and SRAM2 can be accessed by GPDMA1 in Stop 0, Stop 1 and Stop 2 modes.*
6. *Parity error interrupt or NMI wakes up from Stop mode.*
7. *Content of 32-Kbyte, 24-Kbyte and/or 8-Kbyte block.*
8. *Illegal access interrupt wakes up from Stop 0, 1, 2 modes.*
9. *GPDMA1 transfers are functional and autonomous in Stop 0 and 1 mode. Interrupts wake up from these Stop modes.*
10. *In Stop 2 mode, GPDMA1 supports only LPUART1, I2C3, LPTIM1, LPTIM3, and LPTIM4 requests. None of GPDMA1 triggers are supported. Interrupts wake up from Stop 2 modes.*
11. *Some peripherals with autonomous mode and wake-up from Stop capability can request HSI16, MSIS or MSIK to be enabled. In this case, the oscillator is woken up by the peripheral, and is automatically put off when no peripheral needs it.*
12. *USART and LPUART reception and transmission is functional and autonomous in Stop mode, in asynchronous and in SPI master modes. Interrupts wake up from Stop mode.*
13. *I2C reception and transmission is functional and autonomous in Stop mode. Interrupts wake up from Stop mode.*
14. *I3C reception and transmission, in controller and target modes, is functional and autonomous in Stop mode. Interrupts wake up from Stop mode .*
15. *I3C reset pattern detection wakes up from Stop 2, Stop 3, Standby and Shutdown modes. I3C pull-ups can be applied in Stop and Standby modes.*
16. *SPI reception and transmission is functional and autonomous in Stop mode. Interrupts wake up from Stop mode.*
17. *DAC1 (2 channels) conversion in sample and hold mode is functional and autonomous in Stop mode.*
18. *LPTIM is functional and autonomous in Stop mode. Interrupts wake up from Stop mode.*
19. *ADF is functional and autonomous in Stop mode. Interrupts wake up from Stop mode.*
20. *I/Os can be configured with internal pull-up, pull-down, or floating in Stop 3 and Standby mode.*
21. *I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.*

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3.10 Peripheral interconnect matrix

Several peripherals have direct connections between them, that allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep, Stop 0, Stop 1, and Stop 2 modes.

3.11 Reset and clock controller (RCC)

The RCC (reset and clock control) manages different reset types, and generates all clocks for the bus and peripherals.

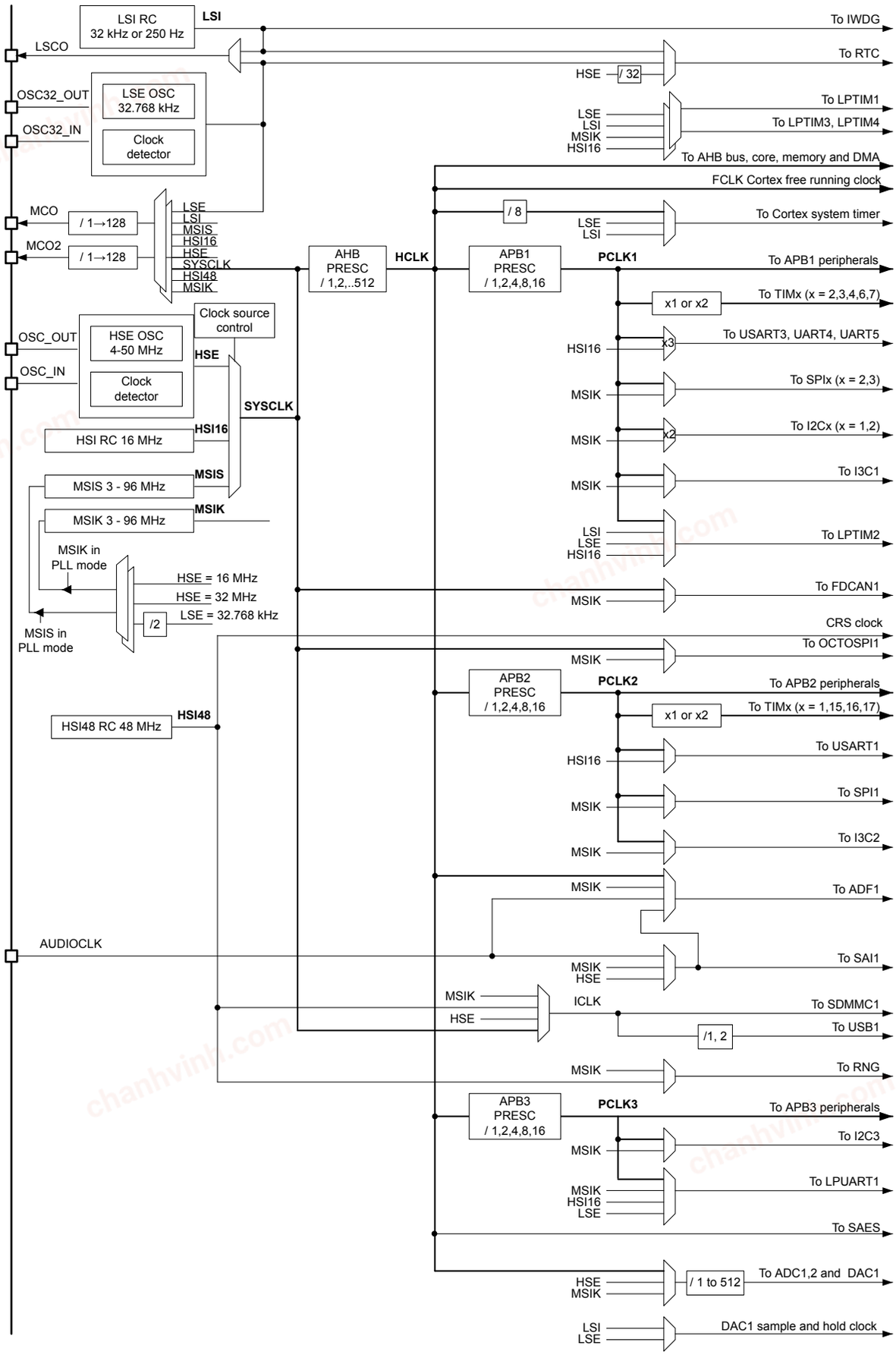
The clock controller distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- Clock prescaler: in order to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- Clock management: in order to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory.
- System clock source: three different clock sources can be used to drive the system clock (SYSCLK).
  - HSE: high-speed external crystal or clock, from 4 to 50 MHz.
  - HSI16: high-speed internal 16 MHz RC oscillator clock, trimmable by software.
  - MSIS: multi-speed internal RC oscillator clock, from 3 to 96 MHz (six possible frequencies, from two internal RC oscillators), trimmable by software. When a 32.768 kHz, a 32 MHz or a 16 MHz external oscillator is present in the application, the MSI frequency can be automatically trimmed by hardware to reach better accuracy.
- HSI48 (RC48 with clock recovery system) internal 48 MHz clock source that can be used to drive the USB, the SDMMC, or the RNG peripherals. This clock can be output on the MCO.
- Auxiliary clock source: two ultra-low-power clock sources that can be used to drive the real-time clock:
  - LSE (32.768 kHz low-speed external crystal). The LSE can also be configured in bypass mode for an external clock.
  - LSI (32 kHz low-speed internal RC), also used to drive the independent watchdog. The LSI clock accuracy is ± 5% accuracy. The LSI clock can be divided by 128 to output a 250 Hz as source clock.
- Peripheral clock sources: several peripherals can have their own independent clock whatever the system clock as a result of the MSIK, HSI48, HSI16 and/or low-speed oscillators.
- Startup clock: after reset, the microcontroller restarts by default with an internal 12 MHz clock MSI. The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- CSS (clock security system): this feature can be enabled by software. If an HSE clock failure occurs, the master clock automatically switches to HSI16 and a software interrupt is generated if enabled. LSE failure can also be detected and generates an interrupt.
- Clock-out capability:
  - MCO (microcontroller clock output): it outputs one of the internal clocks for external use by the application.
  - LSCO (low-speed clock output): it outputs LSI or LSE in all low-power modes (except V_{BAT} mode).

Several prescalers allow AHB and APB frequencies configuration. The maximum frequency of the AHB and the APB clock domains is 96 MHz.

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Figure 5. **Clock tree**



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3.11.1 RCC TrustZone®security

When the TrustZone® security is activated by the TZEN option bit and security is enabled in the RCC, the bits controlling the peripheral clocks and resets become TrustZone®-aware:

- If the peripheral is securable and programmed as secure in the TZSC, the peripheral clock and reset bits become secure.
- If the peripheral is TrustZone®-aware, the peripheral clock and reset bits become secure as soon as at least one function is configured as secure inside the peripheral.

A peripheral is in secure state:

- For securable peripherals by TZSC (TrustZone® security controller), the SEC security bit corresponding to this peripheral is set in the GTZC TZSC secure configuration registers.
- For TrustZone®-aware peripherals, a security feature of this peripheral is enabled through its dedicated bits.

3.12 Clock recovery system (CRS)

The clock recovery system (CRS) is an advanced digital controller acting on the internal fine-granularity trimmable RC oscillator HSI48. The CRS provides a powerful means for oscillator output frequency evaluation, based on comparison with a selectable synchronization signal. It can do automatic adjustments of oscillator trimming based on the measured frequency error value, while keeping the possibility of a manual trimming for faster start-up convergence.

The CRS is ideally suited to provide a precise clock to the USB peripheral. In such case, the synchronization signal can be derived from the start-of-frame (SOF) packet signalization on the USB bus. The synchronization signal can also be derived from the LSE oscillator output, a GPIO alternate function (CRS_SYNC), or it can be generated by user software.

3.13 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.13.1 GPIOs TrustZone® security

Each I/O pin of GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against a nonsecure access. The associated registers bit access is restricted to a secure software only. After reset, all GPIO ports are secure.

3.14 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all masters (CPU, GPDMA1, SDMMC1) and slave (flash memory, RAM, OCTOSPI, SRAMs, AHB, and APB) peripherals. It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

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3.15 General purpose direct memory access controller (GPDMA)

The general purpose direct memory access (GPDMA) controller is a bus master and system peripheral.

The GPDMA is used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

The GPDMA main features are:

- Dual bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during low-power modes
- Transfers arbitration based on a four-grade programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)
- Per channel event generation, on any of the following events: transfer complete, half transfer complete, data transfer error, user setting error, link transfer error, completed suspension, and trigger overrun.
- Per channel interrupt generation, with separately programmed interrupt enable per event
- 12 concurrent DMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intra-channel GPDMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode.
  - Intra-channel and inter-channel GPDMA transfers chaining via programmable GPDMA input triggers connection to GPDMA task completion events.
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive burst transfers
  - 2D source and destination addressing: programmable signed address offsets between successive burst transfers (non-contiguous addressing within a block, combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level, for a reduced set of channels.
  - Support for scatter-gather (multi-buffer transfers), data interleaving and deinterleaving via 2D addressing
  - Programmable GPDMA request and trigger selection
  - Programmable GPDMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the GPDMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting including FIFO level and event flags
- TrustZone® support:
  - Support for secure and nonsecure GPDMA transfers, independently at a first channel level, and independently at a source/destination and link sublevels
  - Secure and nonsecure interrupts reporting, resulting from any of the respectively secure and nonsecure channels
  - TrustZone®-aware AHB slave port, protecting any GPDMA secure resource (register, register field) from a nonsecure access

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- Privileged/unprivileged support:
  - Support for privileged and unprivileged GPDMA transfers, independently at channel level
  - Privileged-aware AHB slave port

3.16 Interrupts and events

3.16.1 Nested vectored interrupt controller (NVIC)

The devices embed an NVIC that is able to manage 16 priority levels and to handle up to 96 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M33.

The NVIC and the processor core interface are closely coupled, enabling low-latency interrupt processing and efficient processing of late-arriving interrupts.

The NVIC registers are banked across secure and nonsecure states.

All interrupts including the core exceptions are managed by the NVIC.

3.16.2 Extended interrupt/event controller (EXTI)

The EXTI manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run modes. The EXTI also includes the EXTI multiplexer I/O port selection.

The EXTI main features are the following:

- Up to 23 input events supported
- All event inputs allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Selectable active trigger edge
  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt, and event generation
  - Software trigger possibility
- TrustZone® secure events
  - The access to control and configuration bits of secure input events can be made secure and/or privileged.
- EXTI I/O port selection

3.17 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from 8-, 16-, or 32-bit data word and a generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

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The CRC main features are the following:

- Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7
- Alternatively, uses a fully programmable polynomial with programmable size (7, 8, 16, 32 bits)
- Handles 8-,16-, 32-bit data size
- Programmable CRC initial value
- Single input/output 32-bit data register
- Input buffer to avoid bus stall during calculation
- CRC computation done in four AHB clock cycles (HCLK) for the 32-bit data size
- General-purpose 8-bit register (can be used for temporary storage)
- Reversibility options on I/O data

3.18 Octo-SPI interface (OCTOSPI)

The OCTOSPI supports most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, HyperRAM™ and HyperFlash™ memories, with the following functional modes:

- Indirect mode: all the operations are performed using the OCTOSPI registers to preset commands, addresses, data, and transfer parameters.
- Automatic status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting.
- Memory-mapped mode: the external memory is memory mapped and is seen by the system as if it were an internal memory supporting read and write operation.

The OCTOSPI supports the following protocols with associated frame formats:

- The standard frame format with the command, address, alternate byte, dummy cycles, and data phase
- The HyperBus™ frame format

The OCTOSPI offers the following features:

- Three functional modes: Indirect, Status-polling, and Memory-mapped
- Read and write support in Memory-mapped mode
- Supports for single, dual, quad, and octal communication
- Dual memory configuration, where eight bits can be sent/received simultaneously by accessing two quad memories in parallel.
- SDR (single-data rate) and DTR (double-transfer rate) support
- Data strobe support
- Fully programmable opcode
- Fully programmable frame format
- Support wrapped-type access to memory in read direction
- HyperBus™ support
- Integrated FIFO for reception and transmission
- 8-, 16-, and 32-bit data accesses allowed
- DMA channel for Indirect mode operations
- DMA protocol support
- Interrupt generation on FIFO threshold, timeout, operation complete, and access error
- AHB interface with transaction acceptance limited to one (the interface accepts the next transfer on the AHB bus only once the previous is completed on memory side)

The OCTOSPI registers can be configured as secure through the TZSC controller.

3.19 Delay block

The delay block (DLYB) is used to generate an output clock that is dephased from the input clock. The phase of the output clock must be programmed by the user application. The output clock is then used to clock the data received by another peripheral such as an SDMMC1 or OCTOSPI interface.

The delay is voltage and temperature dependent, that may require the application to reconfigure and recenter the output clock phase with the received data.

The main features of DLYB are:

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- Input clock frequency ranging from 25 MHz to the maximum frequency supported by the communication interface (see datasheet)
- Up to 12 oversampling phases

3.20 Analog-to-digital converter (ADC)

The STM32U385xx devices embed up to 2 ADCs, ADC1 and ADC2. These are tightly coupled and can operate in dual mode (ADC1 is master). Each ADC module consists of one 12-bit successive approximation analog-to-digital converter. Each ADC has up to 19 multiplexed channels. A/D conversion of the various channels can be performed in single, continuous, scan, or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned (default configuration) 32-bit data register.

The ADCs are mapped on the AHB bus to allow fast data handling.

The analog watchdog features allow the application to detect if the input voltage goes outside the user-defined high or low thresholds.

A built-in hardware oversampler allows improving analog performances while off-loading the related computational burden from the CPU.

An efficient low-power mode is implemented to allow very low consumption at low frequency. The main features are:

- High performance
  - Up to 2 ADCs which can operate in dual mode
  - ADC1 is connected to 15 external channels + 4 internal channels
  - ADC2 is connected to 13 external channels + 6 internal channels
- 12, 10, 8 or 6-bit configurable resolution
- ADC conversion time is independent from the AHB bus clock frequency
- Faster conversion time by lowering resolution
- AHB slave bus interface to allow fast data handling
- Offset calibration support
- Channel-wise programmable sampling time
- Flexible sampling time control
- Up to 4 injected channels (analog inputs assignment to regular or injected channels is fully configurable)
- Hardware assistant to prepare the context of the injected channels to allow fast context switching
- Data alignment with in-built data coherency
- Data can be managed by DMA for regular channel conversions
- Data can be routed to MDF for post processing
- Four dedicated data registers for the injected channels
- Low-power
  - Speed adaptive low-power mode to reduce ADC consumption when operating at low frequency
  - Provides automatic control to avoid ADC overrun in low AHB bus clock frequency application (autodelay mode)
  - Allows slow bus frequency application while keeping optimum ADC performance
- Oversampler
  - 32-bit data register
  - Oversampling ratio adjustable from 2 to 1024
  - Programmable data right shift
- Data preconditioning
  - Gain compensation
  - Offset compensation

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- Analog input channels
  - External analog inputs (per ADC): up to 15 GPIO pads
  - 1 channel for the internal reference voltage (VREFINT)
  - 1 channel for the internal temperature sensor (VSENSE)
  - 1 channel for monitoring the external VBAT power supply pin
  - 1 channel for monitoring VCORE internal voltage
  - Connection to DAC internal channels
- Start-of-conversion can be initiated:
  - By software for both regular and injected conversions
  - By hardware triggers with configurable polarity (internal timers events or GPIO input events) for both regular and injected conversions
- Conversion modes
  - Each ADC can convert a single channel or can scan a sequence of channels
  - Single mode converts selected inputs once per trigger
  - Continuous mode converts selected inputs continuously
  - Discontinuous mode
- Interrupt generation at ADC ready, the end of sampling, the end of conversion (regular or injected), end of sequence conversion (regular or injected), analog watchdog 1, 2 or 3 or overrun events
- 3 analog watchdogs per ADC
- ADC input range: $V_{SSA} < V_{IN} < V_{REF+}$

3.20.1 Temperature sensor

The temperature sensor can be used to measure the junction temperature (TJ) of the device.

The temperature sensor is internally connected to the ADC input channels that are used to convert the sensor output voltage to a digital value. When not in use, the sensor can be put in power-down mode. It supports the temperature range –40 to 110°C.

The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 45°C from one chip to another). The uncalibrated internal temperature sensor is more suited for applications that detect temperature variations instead of absolute temperatures.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by STMicroelectronics in the system memory area, accessible in read-only mode.

Table 10. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	Temperature sensor 12-bit raw data acquired by ADC1 at 30°C (± 5°C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x0BFA 0710 - 0x0BFA 0711
TS_CAL2	Temperature sensor 12-bit raw data acquired by ADC1 at 110°C (± 5°C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x0BFA 0742 - 0x0BFA 0743

3.20.2 Internal voltage reference (VREFINT)

The VREFINT provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to ADC1 and ADC2 input channels.

The precise voltage of VREFINT is individually measured for each part by STMicroelectronics during production test and stored in the system memory area. It is accessible in read-only mode.

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Table 11. **Internal voltage reference calibration value**

Calibration value name	Description	Memory address
VREFINT_CAL	12-bit raw data acquired by ADC1 at 30°C (± 5°C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x0BFA 07A5 - 0x0BFA 07A6

3.20.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using ADC1 or ADC2 input channel. As the V_{BAT} voltage may be higher than the V_{DDA}, to ensure the correct operation of the ADC, the VBAT pin is internally connected to a bridge divider by 4. As a consequence, the converted digital value is one fourth of the V_{BAT} voltage. To prevent any unwanted consumption on the battery, it is recommended to enable the bridge divider only when needed, for ADC conversion.

3.21 Digital-to-analog converter (DAC)

The DAC module is a 12-bit, voltage output digital-to-analog converter. The DAC can be configured in 8- or 12-bit mode and may be used with the DMA controller. In 12-bit mode, the data may be left- or right-aligned.

The DAC features two output channels, each with its own converter. In dual DAC channel mode, conversions can be done independently or simultaneously when both channels are grouped together for synchronous update operations. An input reference pin, VREF+ (shared with other analog peripherals) is available for better resolution. An internal reference can also be set on the same input.

The DAC_OUTx pin can be used as a general-purpose input/output (GPIO) when the DAC output is disconnected from the output pad and connected to on chip peripheral. The DAC output buffer can be optionally enabled to allow a high drive output current. An individual calibration can be applied on each DAC output channel. The DAC output channels support a low-power mode, the sample and hold mode.

The digital interface supports the following features:

- One DAC interface, maximum two output channels
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave and triangular-wave generation
- Dual DAC channel for independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- Double data DMA capability to reduce the bus activity
- External triggers for conversion
- DAC output channel buffered/unbuffered modes
- Buffer offset calibration
- Each DAC output can be disconnected from the DAC_OUTx output pin
- DAC output connection to on-chip peripherals
- Sample and hold mode for low-power operation in Stop mode.
- Autonomous mode to reduce the power consumption for the system
- Voltage reference input

3.22 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer that can be used as voltage reference for ADCs, DACs and also as voltage reference for external components through the VREF+ pin.

The internal voltage reference buffer supports four voltages: 1.5 V, 1.8 V, 2.048 V, and 2.5 V.

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages, the internal voltage reference buffer is not available.

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3.23 Comparators (COMP)

The device embeds two ultra-low-power comparators, COMP1 and COMP2. These comparators can be used for a variety of functions including:

- Wake-up from low-power mode triggered by an analog signal
- Analog signal conditioning
- Cycle-by-cycle current control loop when combined with a PWM output from a timer

The COMP main features are:

- Each comparator has configurable plus and minus inputs used for flexible voltage selection:
  - Multiplexed I/O pins
  - Internal reference voltage and three submultiple values (1/4, 1/2, 3/4) provided by a scaler (buffered voltage divider)
  - Programmable hysteresis
- Programmable speed/consumption
- Outputs that can be redirected to an I/O or to timer inputs for triggering break events for fast PWM shutdowns
- Comparator outputs with blanking source
- Comparators that can be combined as a window comparator
- Interrupt generation capability for each comparator with wake-up from Sleep and Stop modes (through the EXTI controller)

3.24 Operational amplifiers (OPAMP)

The STM32U385xx devices embed two operational amplifiers with two inputs and one output each. The three I/Os can be connected to the external pins, this enables any type of external interconnections. The operational amplifier can be configured internally as a follower or as an amplifier with a non-inverting gain ranging from 2 to 16. The positive input can be connected to the internal DAC. The output can be connected to the internal ADC.

The operational amplifier features are:

- Rail-to-rail input voltage range
- Low input bias current
- Low input offset voltage
- Low-power mode
- High-speed mode to achieve a better slew rate
- Fast wake-up time
- Gain bandwidth of 1.6 MHz

3.25 Audio digital filter (ADF)

The ADF is a high-performance module dedicated to the connection of external ∑Δ modulators. It is mainly targeted for the following applications:

- Audio capture signals
- Metering

The ADF features one digital serial interface (SITF0) and one digital filter (DFLT0) with flexible digital processing options to offer up to 24-bit final resolution.

The ADF serial interface supports several standards allowing the connection of various ∑Δ modulator sensors:

- SPI interface
- Manchester coded 1-wire interface
- PDM interface

The ADF converts an input data stream into clean decimated digital data words. This conversion is done thanks to low-pass digital filters and decimation blocks. In addition, it is possible to insert a high-pass filter.

The conversion speed and resolution are adjustable according to configurable parameters for digital processing: filter type, filter order, decimation ratio. The maximum output data resolution is up to 24 bits. There are two conversion modes: single conversion and continuous modes. The data can be automatically stored in a system RAM buffer through DMA, thus reducing the software overhead.

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A SAD (sound activity detector) is available for the detection of "speech-like" signals. The SAD is connected at the output of DFLT0. Several parameters can be programmed to properly adjust the SAD to the sound environment. The SAD can strongly reduce the power consumption by preventing the storage of samples into the system memory as long as the observed signal does not match the programmed criteria.

All the digital processing is performed using only the kernel clock. The ADF requests the bus interface clock (AHB clock) only when data must be transferred or when a specific event requests the attention of the system processor.

The ADF main features are:

- AHB interface
- One serial digital input:
  - Configurable SPI interface to connect various digital sensors
  - Configurable Manchester coded interface support
  - Compatible with PDM interface to support digital microphones
- Two common clocks input/output for ∑Δ modulators
- One flexible digital filter path, including:
  - An MCIC filter configurable in Sinc4 or Sinc5 filter with an adjustable decimation ratio
  - A reshape filter to improve the out-off band rejection and in-band ripple
  - A high-pass filter to cancel the DC offset
  - Gain control
  - Saturation blocks
- Clock absence detector
- 24-bit signed output data resolution
- Continuous or single conversion
- Possibility to delay independently each bitstream
- One trigger input
- Autonomous functionality in Stop modes
- DMA can be used to read the conversion data
- Interrupts services

3.26 Touch sensing controller (TSC)

The TSC provides a simple solution to add capacitive sensing functionality to any application. A capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (such as glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The TSC is fully supported by the STMTouch touch sensing firmware library that is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The TSC main features are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 21 capacitive sensing channels
- Up to seven capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to three capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

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Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.27 Coupling and chaining bridge

The coupling and chaining bridge (CCB) is a sophisticated security mechanism designed to ensure that private keys are protected, even against CPU access, and are wrapped with unique device keys, and stored securely in a secure storage.

The CCB can be programmed to implement special coupling and chaining operations, which are required to protect private keys used in PKA protected operations.

These coupling and chaining operations involve the PKA, the SAES, and sometimes the RNG peripherals.

The main features of CCB are:

- AHB system slave port, mapping multiple peripherals
  - AHB configuration slave port (CCB peripheral), for which any read access is supported. For writes they must be 32-bit word accesses only, otherwise an AHB error occurs.
- Support for coupling PKA RAM writes to SAES input data register
- Support for read and write chaining between PKA RAM and SAES
- Support for SAES to CCB read chaining, with comparison to a 128-bit reference tag
- Support for RNG output chaining with either PKA RAM or SAES_IVR registers
- Dedicated sequences to support three PKA protected operations: modular exponentiation, scalar multiplication, and ECDSA (elliptic curve digital signature algorithm) signature
  - One-time sequence to prepare a PKA protected operation (blob creation)
  - Many-time sequence to execute PKA protected operation (blob usage)
- Optional private key generation for ECDSA signature, and for ECC private key cryptography (key never accessible to the application in clear-text)
- Possibility to encrypt, with AES-256, any PKA blob encryption key using the device unique secret key DHUK (in the SAES). This makes the PKA encrypted blob usable only on this device.
- Software-reset capability
- Repository for cryptographic subsystem tamper event flags

3.28 Random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a nondeterministic random bit generator (NDRBG).

The RNG true random number generator has been precertified NIST SP800-90B. It has also been tested using the German BSI statistical tests of AIS-31 (T0 to T8).

The RNG main features are the following:

- The RNG delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage.
- It can be used as the entropy source to construct a nondeterministic random bit generator (NDRBG).
- In the NIST configuration, it produces four 32-bit random samples every 412 AHB clock cycles if $f_{AHB} < f_{threshold}$ (256 RNG clock cycles otherwise).
- It embeds startup and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- It can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration).
- It has an AMBA® AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored).

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3.29 Secure advanced encryption standard hardware accelerator (SAES) and encryption standard hardware accelerator (AES)

The devices embed two AES accelerators: SAES and AES. The SAES with hardware unique key embeds protection against differential power analysis (DPA) and related side channel attacks. The SAES can share its current key register information with the faster AES using a dedicated hardware bus.

The SAES and the AES can be used to both encrypt and decrypt data using the AES algorithm. It is a fully compliant implementation of the advanced encryption standard (AES) as defined by Federal Information Processing Standards Publication (FIPS PUB 197, Nov 2001).

Multiple chaining modes are supported for key sizes of 128 or 256 bits.

The SAES embeds protection against differential power analysis (DPA) and related side channel attacks.

To improve the confidentiality of the keys it manipulates, the SAES can create hardware secret keys, usable but never readable in the clear by the application. Such keys can be encrypted with a device nonvolatile and unique master key (256 bits) or an application-defined master key stored in backup registers (also 256 bits) written then locked at boot time. Those hardware secret keys can also be made immediately unusable in case of a security breach.

The SAES peripheral is connected by hardware to the true random number generator RNG (for side-channel resistance). It is also connected to the faster AES hardware accelerator, in order to share hardware secret keys if allowed by the SAES peripheral.

The SAES and AES peripherals support:

- Compliant implementation of standard NIST Special Publication 197, Advanced Encryption Standard (AES) and Special Publication 800-38A, Recommendation for Block Cipher Modes of Operation
- 128-bit data block processing
- Support for cipher keys length of 128-bit and 256-bit
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
- Additional chaining modes supported by AES only:
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- 528 or 743 clock cycle latency in ECB encryption mode for SAES processing one
- 128-bit block of data with, respectively, 128-bit or 256-bit key
- 51 or 75 clock cycle latency in ECB encryption mode for AES processing one 128-bit block of data with, respectively, 128-bit or 256-bit key
- Integrated round key scheduler to compute the last round key for AES ECB/CBC decryption
- 256-bit register for storing the cryptographic key (four 32-bit registers), with key atomicity enforcement
- 128-bit registers for storing initialization vectors (four 32-bit registers)
- One 32-bit input buffer and one 32-bit output buffer
- Automatic data flow control with support of single-transfer direct memory access (DMA) using two channels (one for incoming data, one for processed data)
- Data swapping logic to support 1-, 8-, 16-, or 32-bit data
- Possibility for software to suspend a message if the SAES/AES needs to process another message with a higher priority (suspend/resume operation)
- SAES additional features:
  - Security context enforcement for keys
  - Hardware secret key encryption/decryption (wrapped key mode) and sharing with faster AES peripheral (Shared key mode)
  - Protection against differential power analysis (DPA) and related side-channel attacks

On top of standard AES encryption and decryption with a key loaded by software, SAES peripheral allows the following advanced use cases:

- Allow or deny the sharing of a key between a secure and a nonsecure application, enforced by hardware

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- Encrypt a shared key with a hardware secret key, with the result that stays hardware secret in write-only SAES key registers (wrapped key mode)
- Encrypt once a key using side-channel resistant AES, then share it to a faster AES engine by decrypting it (shared key mode)
- Decrypt a 256-bit random number using a 256-bit hardware secret master key, and use the result as a device unique hardware secret key (to encrypt local data)

Note: All hardware secret keys can no longer be used when a security breach is detected.

3.30 HASH hardware accelerator (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA1, SHA-2 family), and the HMAC (keyed-hash message authentication code) algorithm. HMAC is suitable for applications requiring message authentication.

The hash processor computes FIPS (Federal Information Processing Standards) approved digests of length of 160, 224, 256 bits, for messages of any length less than 264 bits (for SHA-1, SHA-224 and SHA-256) or less than 2^{128} bits (for SHA-384, SHA-512).

The HASH main features are:

- Suitable for data authentication applications, compliant with:
  - Federal Information Processing Standards Publication FIPS PUB 180-4, Secure Hash Standard (SHA-1 and SHA-2 family)
  - Federal Information Processing Standards Publication FIPS PUB 186-4, Digital Signature Standard (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, HMAC: Keyed-Hashing for Message Authentication and Federal Information Processing Standards Publication FIPS PUB 198-1, The Keyed-Hash Message Authentication Code (HMAC)
- Fast computation of SHA-1, SHA2-224, SHA2-256, SHA2-384, and SHA2-512
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
  - Support for SHA-2 truncated outputs (SHA2-512/224, SHA2-512/256)
  - 98 clock cycles for processing one 1024-bit block of data using either SHA2-384 or SHA2-512 algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message:
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit string
  - Supported word swapping format: bits, bytes, half-words, and 32-bit words
- Support for HMAC mode with all supported algorithm
- Automatic padding to complete the input bit string to fit digest minimum block size
- Single 32-bit, write-only, input register associated to an internal input FIFO, corresponding to a 64-byte block size (16 x 32 bits)
- AHB slave peripheral, accessible by 32-bit words only (else an AHB error is generated)
- 8 x 32-bit words (H0 to H7) for output messages
- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of 4 supported.
- Interruptible message digest computation, on a per-32-bit word basis
  - Reloadable digest registers
  - Hashing computation suspend/resume mechanism, including DMA

3.31 Public key accelerator (PKA)

The PKA is intended for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann, or ECC (elliptic curve cryptography) over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

For a given operation, all needed computations are performed within the accelerator, so no further hardware/ software elaboration is needed to process the inputs or the outputs.

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When manipulating secrets, the PKA incorporates a protection against side-channel attacks (SCA), including differential power analysis (DPA), certified SESIP, and PSA security assurance level 3.

The PKA main features are:

- Acceleration of RSA, DH, and ECC over GF(p) operations, based on the Montgomery method for fast modular multiplications. More specifically:
  - RSA modular exponentiation, RSA Chinese remainder theorem (CRT) exponentiation
  - ECC scalar multiplication, point on curve check, complete addition, double base ladder, projective to affine
  - ECDSA signature generation and verification
- Capability to handle operands up to 4160 bits for RSA/DH and 640 bits for ECC.
- When manipulating secrets: protection against side-channel attacks (SCA), including differential power analysis (DPA), certified SESIP, and PSA security assurance level 3. Applicable to modular exponentiation, ECC scalar multiplication, and ECDSA signature generation
- Arithmetic and modular operations such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication.
- Built-in Montgomery domain inward and outward transformations.
- AMBA® AHB slave peripheral, accessible through 32-bit word single accesses only (otherwise an AHB bus error is generated, and write accesses are ignored).
- Support for CCB chaining operations required to protect private key used in PKA protected operations
- Hardware protections to monitor usage of private keys during protected operation initialization

3.32 Timers and watchdogs

The devices include an advanced control timer, up to six general-purpose timers, two basic timers, up to four low-power timers, two watchdog timers and two SysTick timers.

The table below compares the features of the advanced control, general-purpose and basic timers.

Table 12. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16 bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	6	4
General-purpose	TIM2, TIM3, TIM4	32 bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16 bits	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16 bits	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16 bits	Up	Any integer between 1 and 65536	Yes	0	No
Low-power	LPTIM1, LPTIM2, LPTIM3, LPTIM4	16 bits	Up	1, 2, 4, 8, 16, 32, 64, or 128	Yes	2(1)	No

1. *LPTIM4 has no capture/compare channel.*

3.32.1 Advanced-control timers (TIM1)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted deadtimes. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture

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- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 - 100%)
- One-pulse mode output

In Debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in the next section) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.32.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32U385xx devices (see Table 12. Timer feature comparison for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, and TIM4

They are full-featured general-purpose timers with 32-bit autoreload up/downcounter and 16-bit prescaler.

These timers feature four independent channels for input capture/output compare, PWM, or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counters can be frozen in Debug mode.

All have independent DMA request generation and support quadrature encoders.

- TIM15, 16, and 17

They are general-purpose timers with mid-range features.

They have 16-bit autoreload upcounters and 16-bit prescalers.

- TIM15 has two channels and one complementary channel
- TIM16 and TIM17 have one channel and one complementary channel

All channels can be used for input capture/output compare, PWM, or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in Debug mode.

3.32.3 Basic timers (TIM6 and TIM7)

The basic timers TIM6 and TIM7 consist of a 16-bit auto-reload counter driven by a programmable prescaler. They may be used as generic timers for time-base generation. The basic timer can also be used for triggering the digital-to-analog converter. This is done with the trigger output of the timer.

3.32.4 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4)

The devices embed four low-power timers. Due to its diversity of clock sources, the LPTIM is able to keep running in all power modes except for Standby mode. They are able to wake up the system from Stop mode.

LPTIM1, LPTIM3, and LPTIM4 are active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

The low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
  - Internal clock sources: configurable internal clock source (see Section 3.11: Reset and clock controller (RCC))
  - External clock source over LPTIM input (working with no LP oscillator running, used by Pulse Counter application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger

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- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Repetition counter
- Up to 2 independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on 10 events
- DMA request generation on the following events:
  - Update event
  - Input capture

3.32.5 Infrared interface

An infrared interface (IRTIM) for remote control is available on the device. It can be used with an infrared LED to perform remote control functions. It uses internal connections with USART1, UART4, TIM16, and TIM17.

3.32.6 Independent watchdog (IWDG)

The independent watchdog (IWDG) peripheral offers a high safety level, thanks to its capability to detect malfunctions due to software or hardware failures.

The IWDG is clocked by an independent clock, and stays active even if the main clock fails. In addition, the watchdog function is performed in the VDD voltage domain, allowing the IWDG to remain functional even in low-power modes.

The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, making it very reliable to detect any unexpected behavior.

The main features of IWDG are:

- 12-bit down-counter
- Dual voltage domain, thus enabling operation in low-power modes
- Independent clock
- Early wake-up interrupt generation
- Reset generation
  - In case of timeout
  - In case of refresh outside the expected window

3.32.7 Window watchdog (WWDG)

The system window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence.

The watchdog circuit generates a device reset on expiry of a programmed time period, unless the program refreshes the contents of the down-counter before the T6 bit becomes cleared.

A device reset is also generated when the 7-bit down-counter value (in the control register) is refreshed before the down-counter reaches the window register value. This implies that the counter must be refreshed within a limited window.

The WWDG clock is prescaled from the APB clock and has a configurable time window that can be programmed to detect abnormally late or early application behavior.

The WWDG is best suited for applications that require the watchdog to react within an accurate timing window.

The main features of WWDG are:

- Programmable free-running down-counter
- Conditional reset:
  - Reset (if WWDG activated) when the down-counter value becomes lower than 0x40
  - Reset (if WWDG activated) if the down-counter is reloaded outside the window

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- Early wake-up interrupt (EWI) (if enabled and WWDG activated) when the down-counter is equal to 0x40

3.32.8 SysTick timer

The Cortex®-M33 with TrustZone® embeds two SysTick timers.

When TrustZone® is activated, two SysTick timers are available:

- SysTick, secure instance
- SysTick, nonsecure instance

When TrustZone® is disabled, only one SysTick timer is available. This timer (secure or nonsecure) is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.33 Real-time clock (RTC)

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in BCD (binary-coded decimal) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode
- 17-bit autoreload wake-up timer (WUT) for periodic events with programmable resolution and period
- TrustZone® support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or nonsecure configuration
  - Alarm A, alarm B, wake-up timer and timestamp individual privilege protection

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The RTC clock sources can be one of the following:

- 32.768 kHz external crystal (LSE)
- External resonator or oscillator (LSE)
- Internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- High-speed external clock (HSE), divided by a prescaler in the RCC.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake-up the device from the low-power modes.

3.34 Tamper and backup registers (TAMP)

The antitamper detection circuit is used to protect sensitive data from external attacks. Thirty-two 32-bit backup registers are retained in all low-power modes and also in V_{BAT} mode. The backup registers, as well as other secrets in the device, are protected by this antitamper detection circuit with five tamper pins and nine internal tampers. The external tamper pins can be configured for edge detection, or level detection with or without filtering.

TAMP main features:

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- A tamper detection can optionally erase the backup registers, SRAM2, cache, and cryptographic peripherals. The device resources protected by tamper are named "device secrets". The list of device secrets is configurable by software.
- 32 32-bit backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the backup domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off.
- Up to five tamper pins for five external tamper detection events:
  - Passive tampers: ultra-low-power edge or level detection with internal pull-up hardware management
  - Configurable digital filter
- Nine internal tamper events to protect against transient or environmental perturbation attacks
- Each tamper can be configured in two modes:
  - Confirmed mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Potential mode: most of the secrets erase following a tamper detection are launched by software
- Any tamper detection can generate an RTC timestamp event.
- TrustZone® support:
  - Tamper secure or nonsecure configuration
  - Backup registers configuration in three configurable-size areas:
    - One read/write secure area
    - One write secure/read nonsecure area
    - One read/write nonsecure area
- Boot hardware key for secure AES, stored in backup registers, protected against read and write access
- Tamper configuration and backup registers privilege protection
- Monotonic counter

3.35 Inter-integrated circuit interface (I2C)

The device embeds three I2C. Refer to Table 13 for the features implementation.

The I^2C (inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I^2C bus. It provides multicontroller capability, and controls all I^2C bus-specific sequencing, protocol, arbitration, and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode Plus (Fm+).

The I2C peripheral supports:

- I^2C-bus specification rev 3.0 compatibility:
  - Target and controller modes
  - Multicontroller capability
  - Standard-mode (up to 100 kHz)
  - Fast-mode (up to 400 kHz)
  - Fast-mode Plus (up to 1 MHz)
  - 7-bit and 10-bit addressing mode
  - Multiple 7-bit target addresses (2 addresses, 1 with configurable mask)
  - Programmable setup and hold times
  - Easy to use event management
  - Optional clock stretching
  - Software reset
- System management bus (SMBus) specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Command and data acknowledge control
  - Address resolution protocol (ARP) support
  - SMBus alert
  - Timeouts and idle condition detection
- Power system management protocol (PMBus) specification rev 1.3 compatibility

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- Independent clock: a choice of independent clock sources allowing the I²C communication speed to be independent from the PCLK reprogramming
- Autonomous functionality in Stop modes with wake-up from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 13. I2C implementation

I2C features	I2C1	I2C2	I2C3
Standard-mode (up to 100 Kbit/s)	X	X	X
Fast-mode (up to 400 Kbit/s)	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	X	X	X
Independent clock	X	X	X
Autonomous in Stop 0, Stop 1 mode with wake-up capability	X	X	X
Autonomous in Stop 2 mode with wake-up capability	-	-	X

1. *X = supported.*

3.36 Improved inter-integrated circuit interface (I3C)

The devices embed two instances of I3C. The I3C interface handles communication between this device and others, such as sensors and host processor, connected on an I3C bus. An I3C bus is a two-wire, serial single-ended, multidrop bus, intended to improve a legacy I²C bus.

The I3C SDR-only peripheral implements all the features required by the MIPI® I3C specification v1.1. It can control all I3C bus-specific sequencing, protocol, arbitration, and timing, and can act as controller (formerly known as master), or as target (formerly known as slave).

When acting as controller, the I3C peripheral improves the features of the I²C interface preserving some backward compatibility: it allows an I²C target to operate on an I3C bus in legacy I²C fast mode (Fm) or legacy I ²C fast mode plus (Fm+), provided that the latter does not perform clock stretching.

The I3C peripheral can be used with DMA, to off-load the CPU.

The I3C peripheral supports:

- MIPI® I3C specification v1.1, as:
  - I3C SDR-only primary controller
  - I3C SDR-only secondary controller
  - I3C SDR-only target
  - I3C SCL bus clock frequency up to 12.5 MHz
- Registers configuration from the host application via the APB slave port
- Queued data transfers:
  - Transmit FIFO (TX-FIFO) for data bytes/words to be transmitted on the I3C bus
  - Receive FIFO (RX-FIFO) for received data bytes/words on the I3C bus
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Queued control/status transfers, when controller:
  - Control FIFO (C-FIFO) for control words to be sent on the I3C bus
  - Optional status FIFO (S-FIFO) for status words as received on the I3C bus
  - For each FIFO, optional DMA mode with a dedicated DMA channel

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- Messages:
  - Legacy I^2C read/write messages to legacy I^2C targets in Fm/Fm+
  - I3C SDR read/write private messages
  - I3C SDR broadcast CCC messages
  - I3C SDR read/write direct CCC messages
- Frame-level management, when controller:
  - Software-triggered or hardware-triggered transfer
  - Optional C-FIFO and TX-FIFO preload
  - Multiple messages encapsulation
  - Optional arbitrable header generation on the I3C bus
  - HDR exit pattern generation on the I3C bus for error recovery
- Programmable bus timing, when controller:
  - SCL high and low period
  - SDA hold time
  - Bus free (minimum) time
  - Bus available/idle condition time
  - Clock stall time
- Target-initiated requests management:
  - Simultaneous support up to four targets, when controller
  - In-band interrupts, with programmable IBI payload (up to 4 bytes), with pending read notification support
  - Bus control request, with recovery flow support and hand-off delay
  - Hot-join mechanism
- HDR exit pattern detection, when target
- Bus error management:
  - CEx with x = 0, 1, 2, 3 when controller
  - TEx with x = 0, 1, ..., 6 when target
  - Bus control switch error and recovery
  - Target reset
- Individual programmable event-based management:
  - Per-event identification with flag reporting and clear control
  - Host application notification via flag polling, and/or via interrupt with a per-event programmable enable
  - Error type identification
- Wake-up from Stop mode(s), as controller:
  - On an in-band interrupt without payload
  - On a hot-join request
  - On a controller-role request
- Wake-up from Stop mode(s), as target:
  - On a reset pattern
  - On a missed start
- Wake-up from Standby and Shutdown modes on a target reset pattern
- Autonomous mode and transfers during Stop mode(s) with DMA
- Multiclock domain management:
  - Separate APB clock and kernel clock, driven from independently programmed clock sources via the RCC, in addition to SCL clock
  - Minimum operating frequency for the kernel clock and the APB clock vs. the application-driven SCL clock

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Table 14. **I3C peripheral controller/target features versus MIPI® v1.1**

Feature	MIPI® I3C v1.1	I3C peripheral		Comments
		When controller	When target	
I3C SDR message	X	X	X	-
Legacy I²C message (Fm/Fm+)	X	X	-	Mandatory when controller and the I3C bus is mixed with (external) legacy I²C target(s)
HDR DDR message	X	-	-	Optional in MIPI v1.1
HDR-TSL/TSP, HDR-BT	X	-	-	Optional in MIPI v1.1
Dynamic address assignment	X	X	X	-
Static address	X	X	-	No (intended) support of the peripheral as a target on an I²C bus
Grouped addressing	X	X	-	Optional in MIPI v1.1
CCCs	X	X	X	Mandatory and some optional CCCs supported
Error detection and recovery	X	X	X	-
In-band interrupt (with MDB)	X	X	X	-
Secondary controller	X	X	X	-
Hot-join mechanism	X	X	X	-
Target reset	X	X	X	-
Synchronous timing control	X	X	-	Optional in MIPI v1.1
Asynchronous timing control 0	X	X	-	Mandatory in MIPI v1.1 when controller Optional in MIPI V1.1 when target
Asynchronous timing control 1,2,3	X	-	-	Optional in MIPI v1.1
Device to device tunneling	X	X	-	Optional in MIPI v1.1
Multilane data transfer	X	-	-	Optional in MIPI v1.1
Monitoring device early termination	X	-	-	Optional in MIPI v1.1

3.37 Universal synchronous/asynchronous receiver transmitter (USART)

The devices have two embedded universal synchronous receiver transmitters (USART1 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

The USART offers a flexible means to perform full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications are possible by using the DMA (direct memory access) for multibuffer configuration.

The USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data
- Each FIFO can be enabled/disabled by software and come with a status flag.

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- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection
- Programmable data word length (7, 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous SPI master/slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from Stop mode capability
- LIN master synchronous break send capability and LIN slave break detection capability
  - 13-bit break generation and 10/11-bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16-bit duration for Normal mode
- Smartcard mode
  - Supports the T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

Refer to Table 15. USART and LPUART features for more details.

3.38 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one low-power UART. The LPUART is an UART that enables bidirectional UART communications with a limited power consumption. Only 32.768 kHz LSE clock is required to enable UART communications up to 9600 baud. Higher baud rates can be reached when the LPUART is clocked by clock sources different from the LSE clock.

Even when the microcontroller is in low-power mode, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption. The LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption.

It supports Half-duplex Single-wire communications and modem operations (CTS/RTS). It also supports multiprocessor communications DMA (direct memory access) can be used for data transmission/reception.

The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source

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- Two internal FIFOs to transmit and receive data
  Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: Wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from Stop capability

Table 15. USART and LPUART features

Modes/features	USART1/3	UART4/5	LPUART1
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous SPI mode (master/slave)	X	-	-
Smartcard mode	X	-	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual-clock domain and wake-up from low power	X	X	X
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Auto-baud rate detection	X	X	-
Driver enable	X	X	X
USART data length	7, 8, and 9 bits		
Tx/Rx FIFO	X	X	X
Tx/Rx FIFO size	8 bytes		

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Modes/features	USART1/3	UART4/5	LPUART1
Autonomous in Stop 0 and Stop 1 mode with wake-up capability	X	X	X
Autonomous in Stop 2 mode with wake-up capability	-	-	X

1. *X = supported.*

3.39 Serial peripheral interface (SPI)

The devices embed three serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex, and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave and can operate in multislave or multimaster configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to setup communication with concrete slave and to assure it handles the data flow properly. The Motorola® data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- From 4-bit up to 32-bit data size selection or fixed to multiply of 8-bit
- Multimaster or multislave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of APB bus clock
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO x MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola® and Texas Instruments® formats support
- Hardware CRC feature can secure communication at the end of transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun, the mode fault and frame error at dependency on the operating mode
- Two multiples of 8-bit embedded Rx and Tx FIFOs (FIFO size depends on instance)
- Configurable FIFO thresholds (data packing)
- Capability to handle data streams by system DMA controller
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Autonomous functionality in Stop modes (handling of the transaction flow and required clock distribution) with wake-up from stop capability
- Optional status pin RDY signalizing the slave device ready to handle the data flow.

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Table 16. **SPI features**

SPI feature	SPI1, SPI2 (full feature set instances)	SPI3 (limited feature set instance)
Data size	Configurable from 4 to 32-bit	8/16-bit
CRC computation	CRC polynomial length configurable from 5 to 33-bit	CRC polynomial length 9/17-bit
Size of FIFOs	16x 8-bit	8x 8-bit
Number of transfered data	Up to 65536	Up to 1024, no remaining data counter (CTSIZE)
Autonomous in Stop 0 and Stop 1 mode with wake-up capability	Yes	Yes

3.40 Serial audio interfaces (SAI)

The devices embed one SAI. Refer to Table 17. SAI features for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio subblocks that can be transmitters or receivers with their respective FIFO
- 8-word integrated FIFOs for each audio subblock
- Synchronous or asynchronous mode between the audio subblocks
- Master or slave configuration independent for both audio subblocks
- Clock generator for each audio block to target independent audio frequency sampling when both audio subblocks are configured in master mode
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97
- Up to 16 slots available with configurable size
- Number of bits by frame may be configurable
- PDM interface, supporting up to 4 microphone pairs
- SPDIF output available if required
- Frame synchronization active level configurable (offset, bit length, level)
- First active bit position in the slot is configurable
- LSB first or MSB first for data transfer
- Mute mode
- Stereo/mono audio frame capability
- Communication clock strobing edge configurable (SCK)
- Error flags with associated interrupts if enabled respectively
  - Overrun and underrun detection
  - Anticipated frame synchronization signal detection in Slave mode
  - Late frame synchronization signal detection in Slave mode
  - Codec not ready for the AC'97 mode in reception
- Interruption sources when enabled:
  - Errors
  - FIFO requests
- 2-channel DMA interface

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Table 17. **SAI features**

SAI features	SAI1
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X
Mute mode	X
Stereo/mono audio frame capability.	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X
FIFO size	X (8 words)
SPDIF	X
PDM	X(2)

1. *X = supported.*
2. *Only signals D[3:1], and CK[2:1] are available.*

3.41 Secure digital input/output and MultiMediaCards interface (SDMMC)

The SDMMC (SD/SDIO embedded MultiMediaCard eMMC™ host interface) provides an interface between the AHB bus and SD memory cards, SDIO cards and eMMC devices.

The MultiMediaCard system specifications are available through the MultiMediaCard association website at www.jedec.org, published by the MMCA technical committee.

SD memory card and SD I/O card system specifications are available through the SD card Association website at www.sdcard.org.

The SDMMC features include the following:

- Compliance with Embedded MultiMediaCard System Specification Version 5.1

Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit

(HS200 SDMMC_CK speed limited to maximum allowed I/O speed) (HS400 is not supported).

- Full compatibility with previous versions of MultiMediaCards (backward compatibility).
- Full compliance with SD memory card specifications version 6.0

(SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).

- Full compliance with SDIO card specification version 4.0

Card support for two different databus modes: 1-bit (default) and 4-bit

(SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).

- Data transfer up to 208 Mbyte/s for the 8-bit mode

(Depending maximum allowed I/O speed).

- Data and command output enable signals to control external bidirectional drivers
- IDMA linked list support

The MultiMediaCard/SD bus connects cards to the host.

The current version of the SDMMC supports only one SD/SDIO/eMMC card at any one time and a stack of eMMC.

Table 18. **SDMMC features**

SDMMC modes/features	SDMMC1
Variable delay (SDR104, HS200)	X
SDMMC_CKIN	X
SDMMC_CDIR, SDMMC_D0DIR	X
SDMMC_D123DIR	X

1. *X = supported.*

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3.42 Controller area network (FDCAN)

The controller area network (CAN) subsystem consists of one CAN module, a shared message RAM memory and a configuration block.

The modules (FDCAN) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 0.8-Kbyte message RAM implements filters, receives FIFOs, transmits event FIFOs and transmits FIFOs.

The FDCAN main features are:

- Conform with CAN protocol version 2.0 part A, B, and ISO 11898-1: 2015, -4
- CAN FD with maximum 64 data bytes supported
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering
- 2 receive FIFOs of three payloads each (up to 64 bytes per payload)
- Separate signaling on reception of high priority messages
- Configurable transmit FIFO / queue of three payloads (up to 64 bytes per payload)
- Transmit Event FIFO
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains: APB bus interface and CAN core kernel clock
- Power-down support

3.43 USB full-speed (USB)

The devices embed a USB full-speed device/host peripheral with integrated transceivers. The USB peripheral implements an interface between a full-speed USB 2.0 bus and the APB2 bus. USB suspend/resume are supported, which permits to stop the device clocks for low-power consumption.

This interface requires a precise 48 MHz clock that can be generated by the internal 48 MHz oscillator (HSI48) in automatic-trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) that allows crystal less operation.

The USB full-speed features are:

- USB specification version 2.0 full-speed compliant
- Supports both Host and Device modes
- Configurable number of endpoints from 1 to 8
- Dedicated packet buffer memory (SRAM) of 2048 bytes
- Cyclic redundancy check (CRC) generation/checking, Non-return-to-zero Inverted (NRZI) encoding/decoding and bit-stuffing
- Isochronous transfers support
- Double-buffered bulk/isochronous endpoint/channel support
- USB Suspend/Resume operations
- Frame locked clock pulse generation
- USB 2.0 Link Power Management support (Device mode only)
- Battery Charging Specification Revision 1.2 support (Device mode only)
- USB connect / disconnect capability (controllable embedded pull-up resistor on USB_DP line)

Table 19. USB features

USB features(1)	USB
Host mode	X
Number of endpoints	8
Size of dedicated packet buffer memory SRAM	2048 bytes
Dedicated packet buffer memory SRAM access scheme	32 bits

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USB features(1)	USB
USB 2.0 Link Power Management (LPM) support in device	X
Battery Charging Detection BCD support for device	X
Embedded pull-up resistor on USB_DP line	X

1. *X = supported*

3.44 Development support

3.44.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be reused as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.44.2 Embedded Trace Macrocell

The Arm Embedded Trace Macrocell (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The ETM operates with third party debugger software tools.

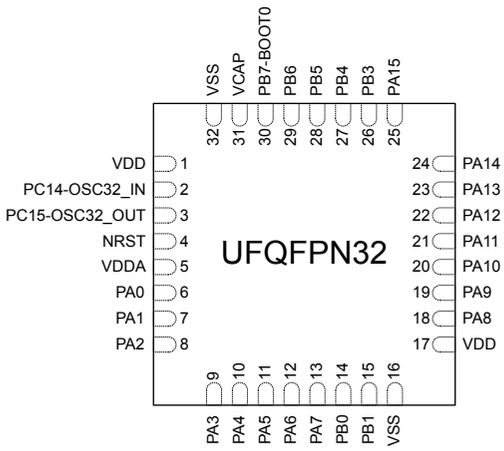
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4 Pinouts/ballouts, pin description, and alternate functions

4.1 Pinout/ballout schematics

Figure 6. UFQFPN32 pinout

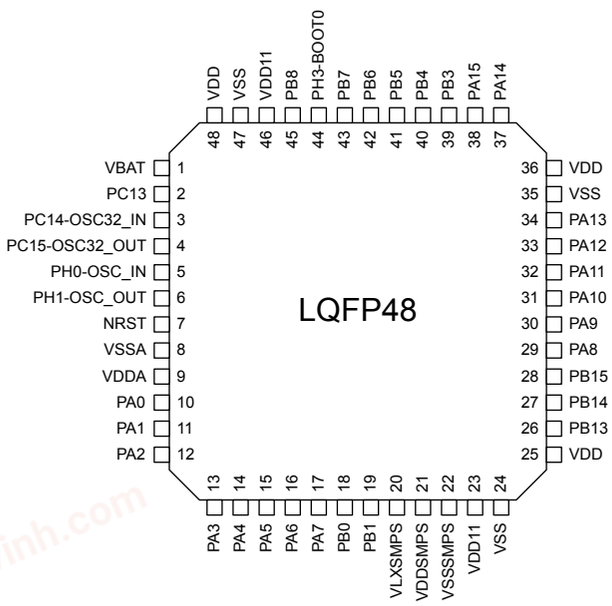
Package top view



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Figure 7. LQFP48_SMPS pinout

Package top view

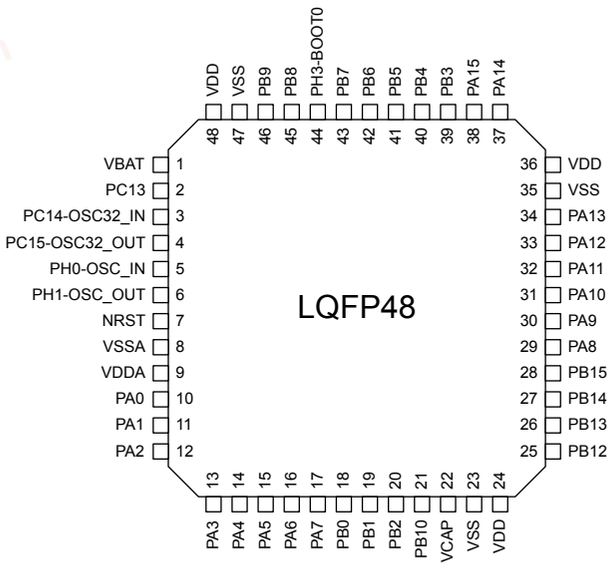


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Figure 8. **LQFP48 pinout**

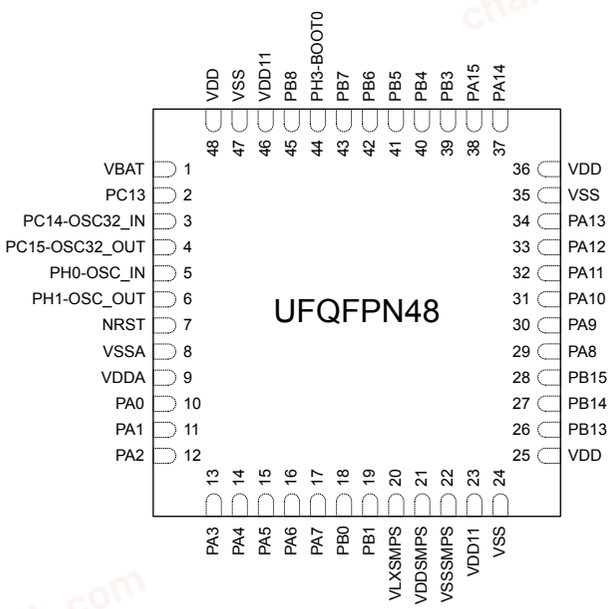
Package top view



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Figure 9. **UFQFPN48_SMPS pinout**

Package top view

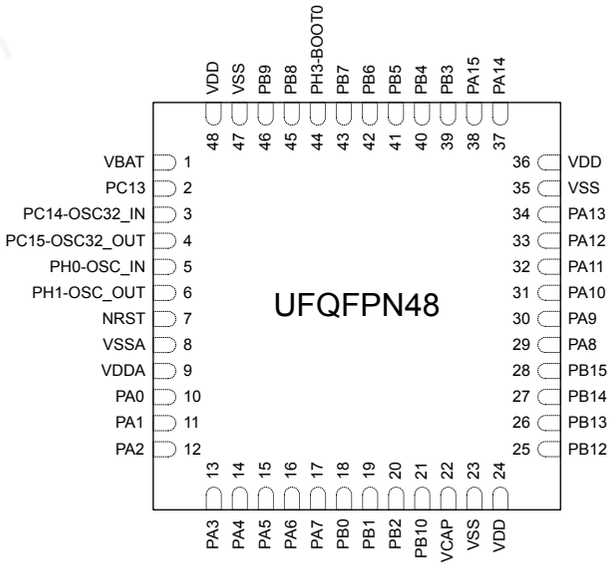


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Figure 10. UFQFPN48 pinout

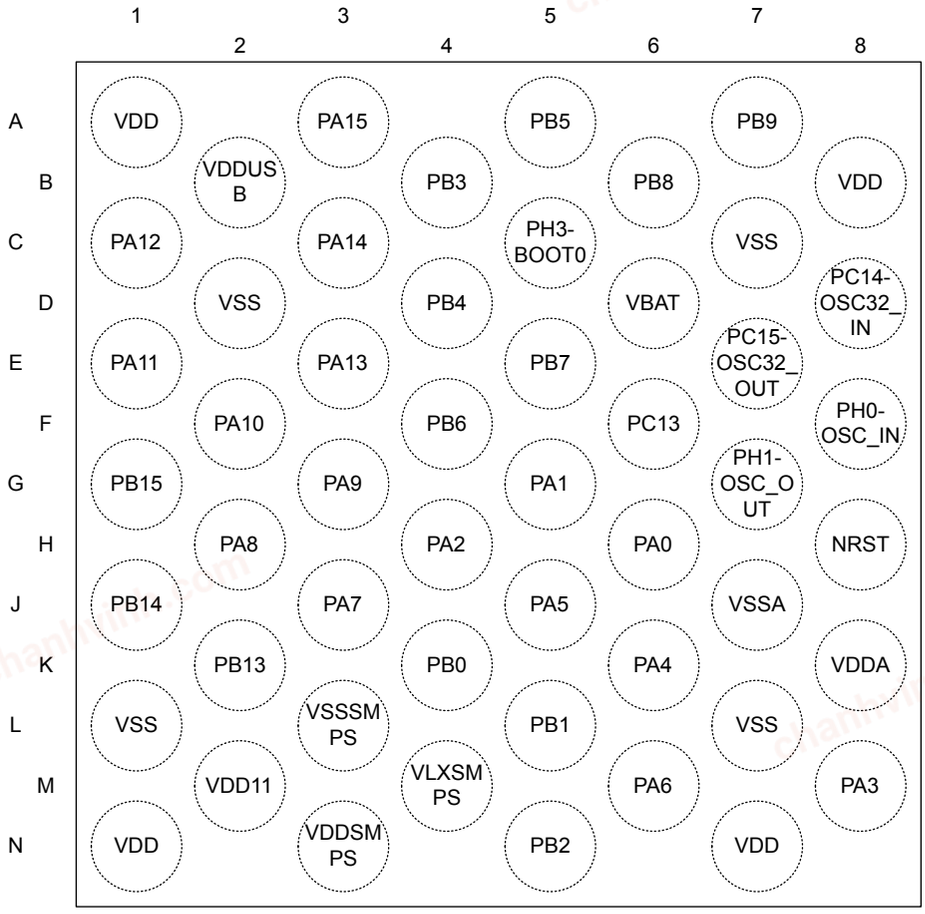
Package top view



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Figure 11. WLCSP52_SMPS ballout

Package top view

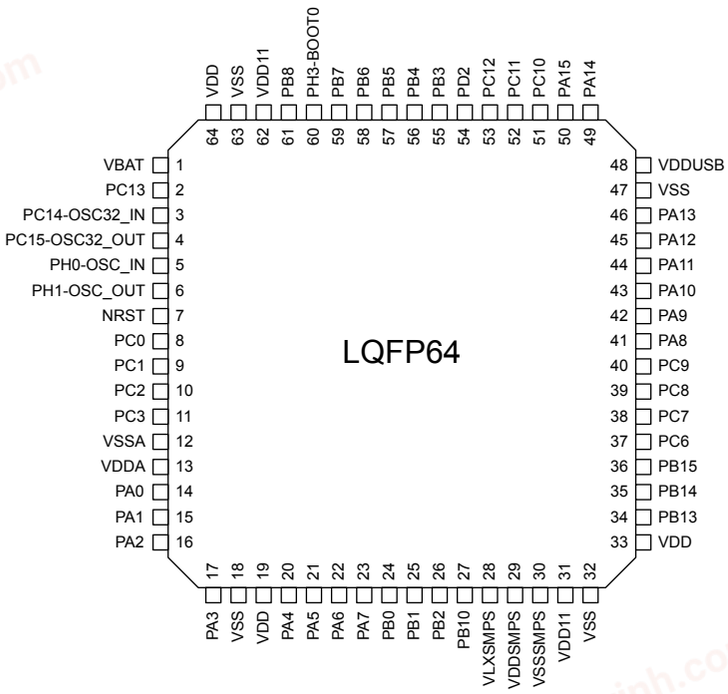


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Figure 12. **LQFP64_SMPS pinout**

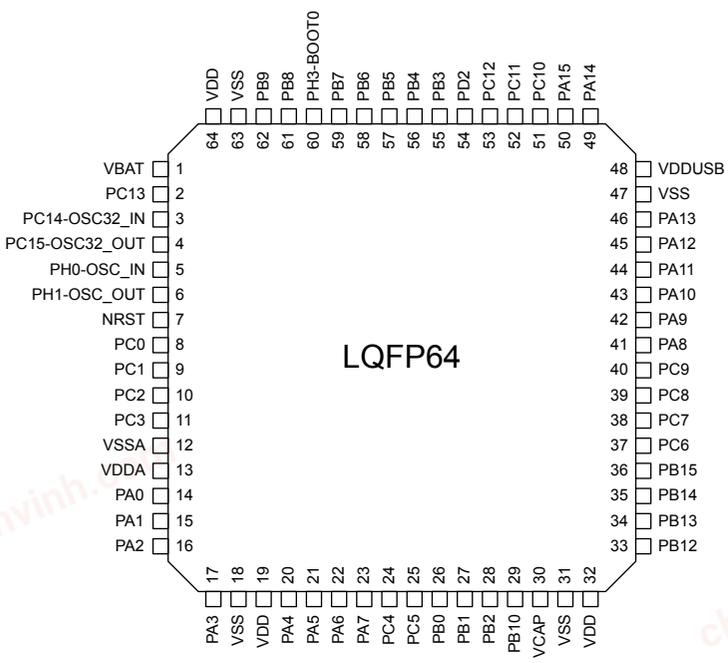
Package top view



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Figure 13. **LQFP64 pinout**

Package top view

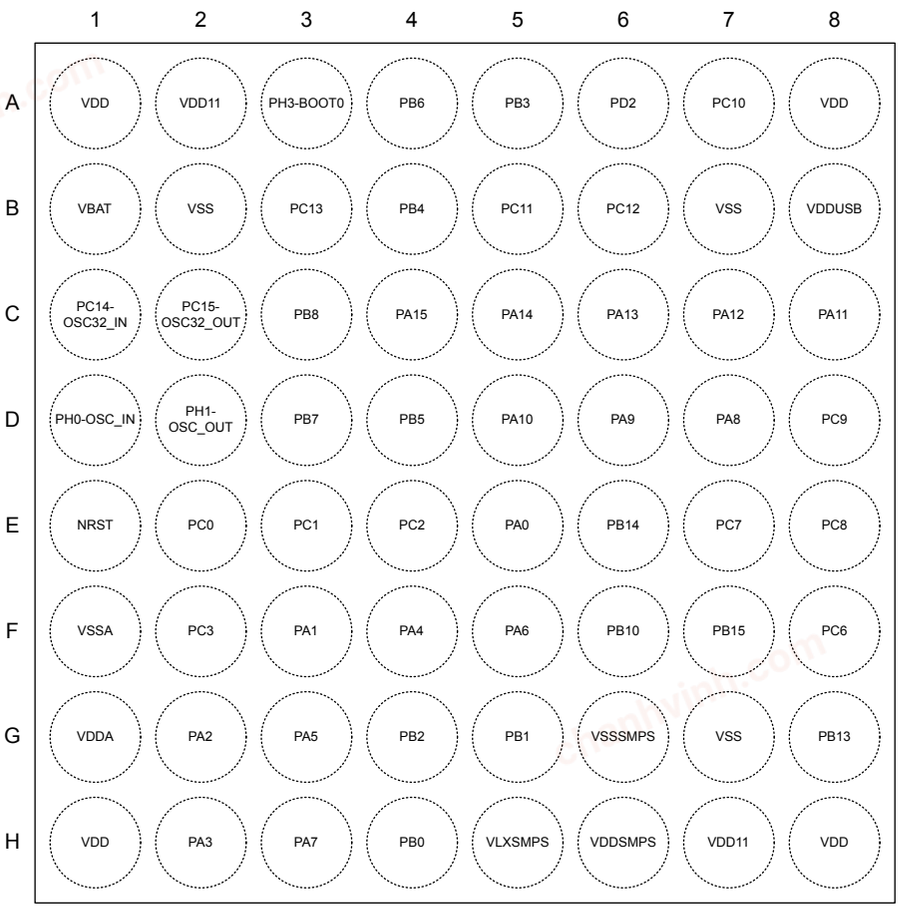


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Figure 14. UFBGA64_SMPS ballout

Package top view

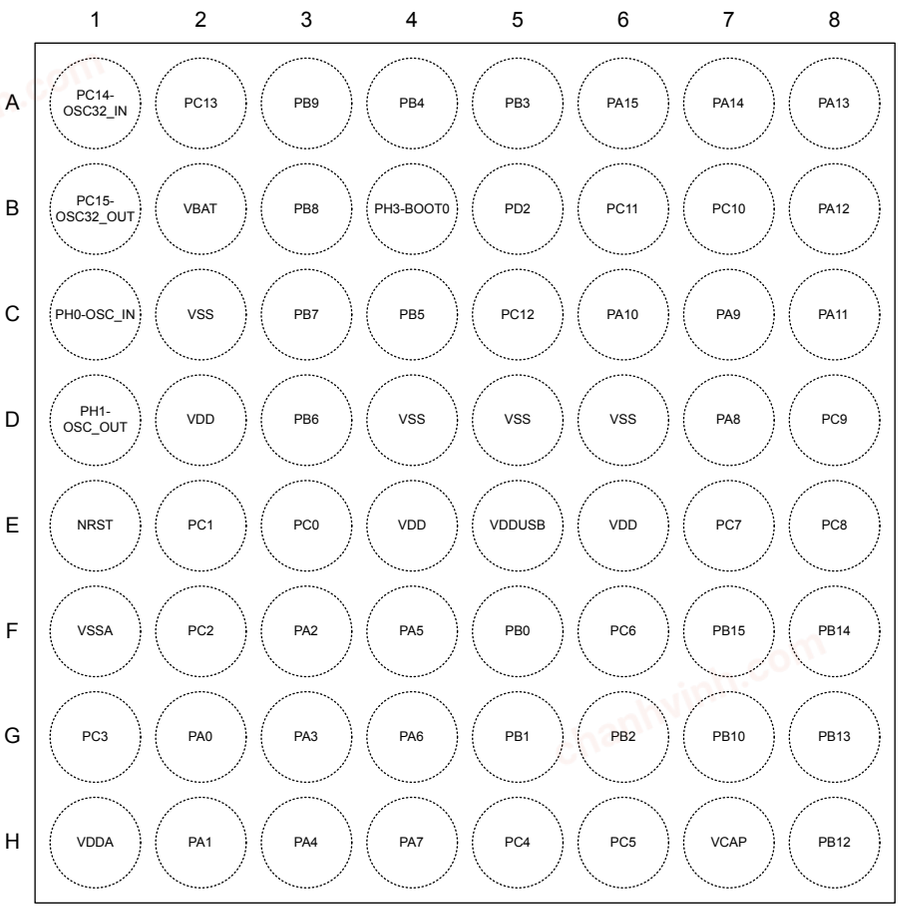


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Figure 15. UFBGA64 ballout

Package top view

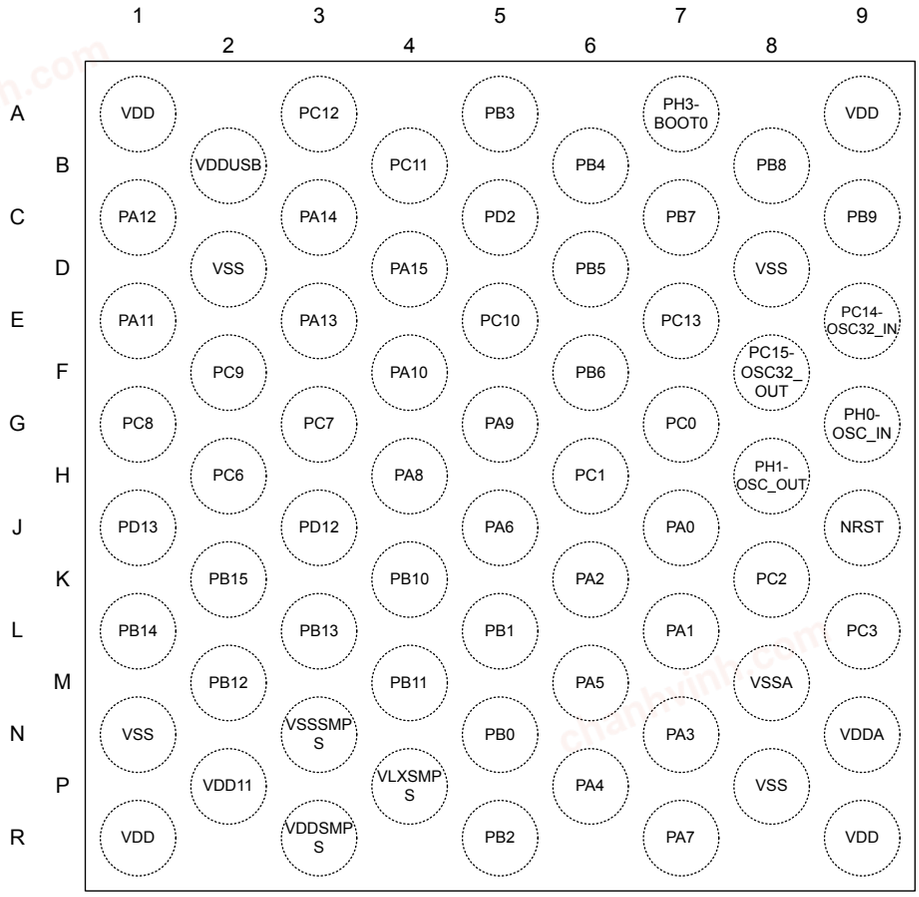


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Figure 16. WLCSP68-Q_SMPS ballout

Package top view

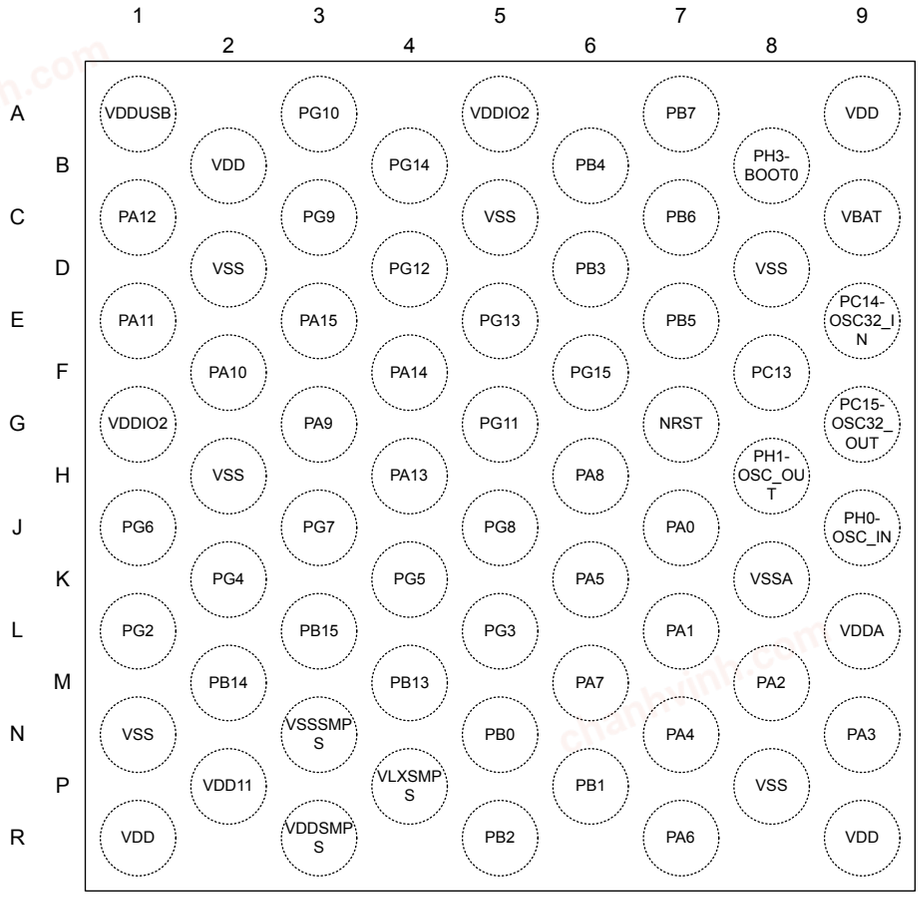


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Figure 17. **WLCSP68-G_SMPS ballout**

Package top view

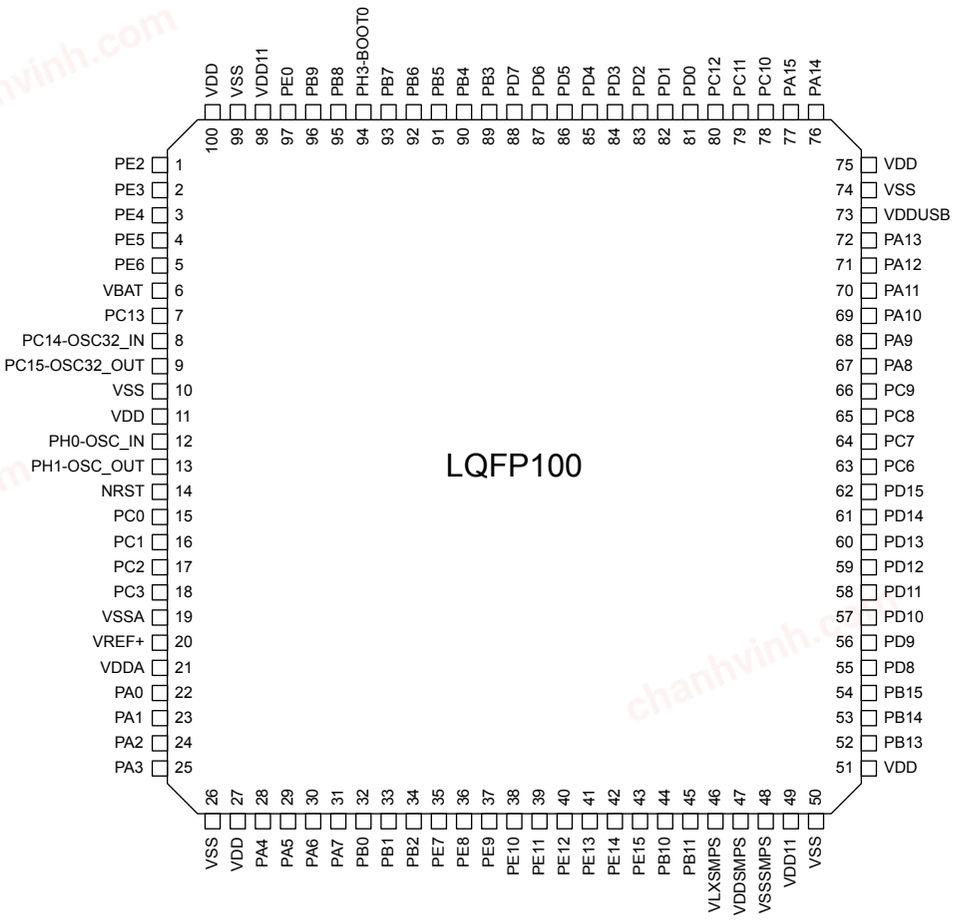


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Figure 18. LQFP100_SMPS pinout

Package top view

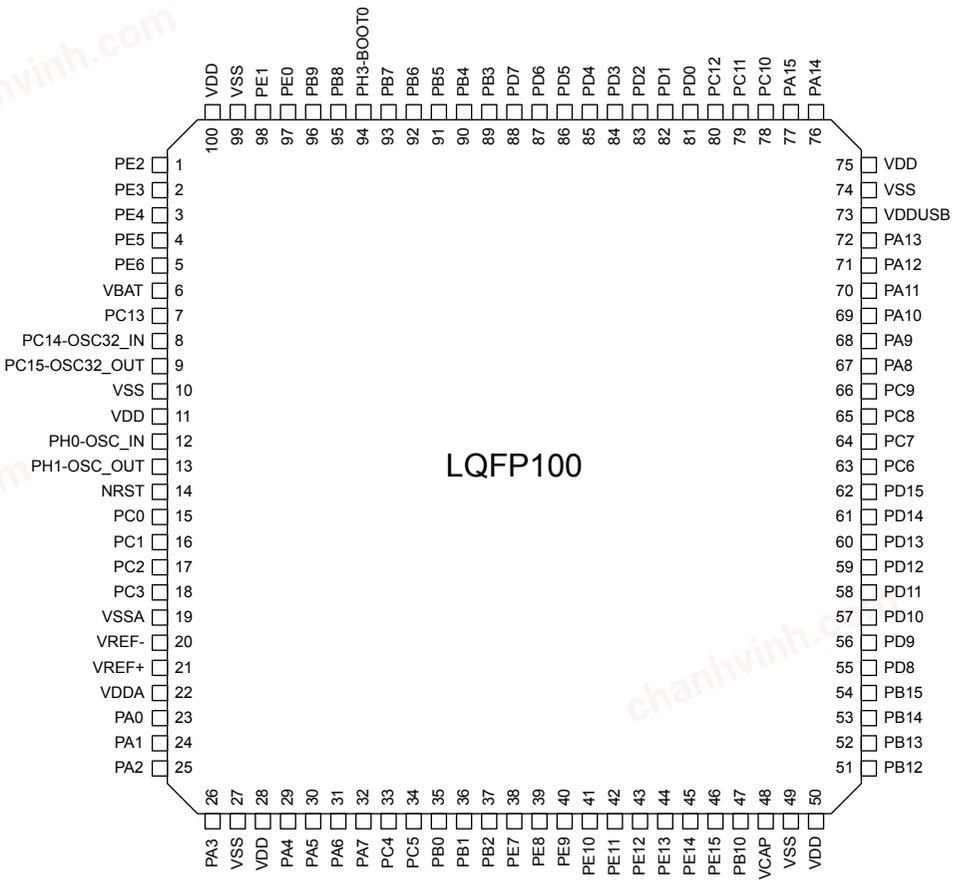


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Figure 19. LQFP100 pinout

Package top view

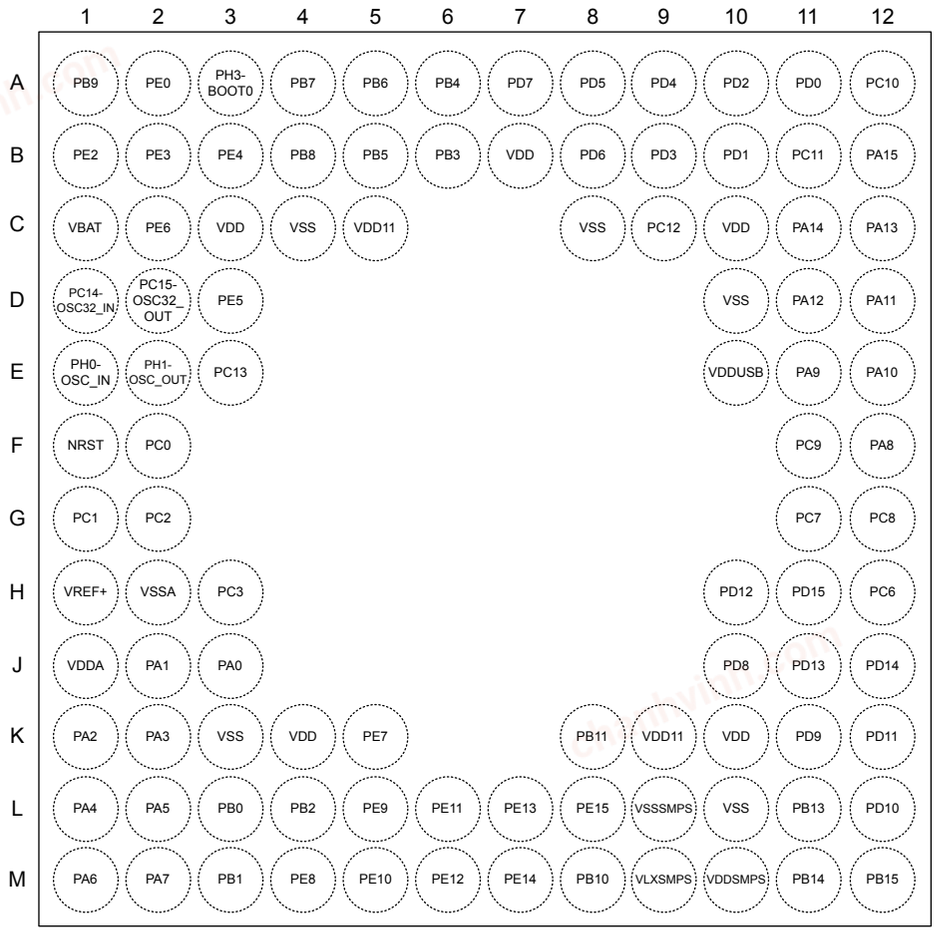


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Figure 20. UFBGA100_SMPS ballout

Package top view

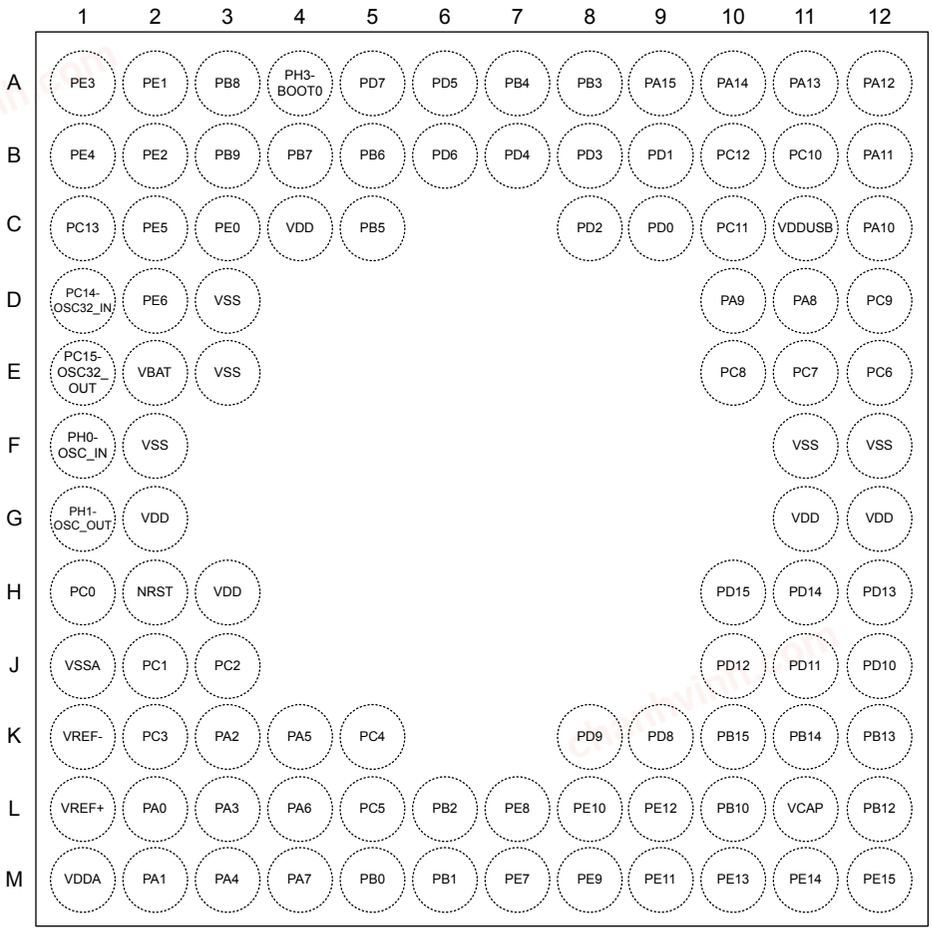


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Figure 21. UFBGA100 ballout

Package top view



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4.2 Pin description

Table 20. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input/output pin
I/O structure		FT	5 V-tolerant I/O
		TT	3.6 V-tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os(1)	
		_a	I/O, with analog switch function supplied by V_{DDA}
		_f	I/O, Fm+ capable
		_h	I/O with high-speed low-voltage mode
		_s	I/O supplied only by V_{DDIO2}
		_t	I/O with a function supplied by V_{SW}
		_u	I/O, with USB function supplied by V_{DDUSB}
		_o	I/O with OSC32_IN/OSC32_OUT capability
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. *The related I/O structures in the table below are a concatenation of various options. Examples: FT_hat, FT_fs, FT_u, TT_a.*

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Table 21. STM32U385xx pin/ball definitions

The function availability depends on the chosen device.

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
-	-	-	-	-	-	-	1	B1	-	-	-	-	1	B2	PE2	I/O	FT_a	-	TRACECLK, TIM3_ETR, SAI1_CK1, TSC_G7_IO1, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	-	2	B2	-	-	-	-	2	A1	PE3	I/O	FT_ha	-	TRACED0, TIM3_CH1, OCTOSPI1_DQS, TSC_G7_IO2, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	-	3	B3	-	-	-	-	3	B1	PE4	I/O	FT_a	-	TRACED1, TIM3_CH2, SAI1_D2, TSC_G7_IO3, SAI1_FS_A, EVENTOUT	WKUP1
-	-	-	-	-	-	-	4	D3	-	-	-	-	4	C2	PE5	I/O	FT_a	-	TRACED2, TIM3_CH3, SAI1_CK2, TSC_G7_IO4, SAI1_SCK_A, EVENTOUT	WKUP2
-	-	-	-	-	-	-	5	C2	-	-	-	-	5	D2	PE6	I/O	FT_t	-	TRACED3, TIM3_CH4, SAI1_D1, SAI1_SD_A, EVENTOUT	WKUP3, TAMP_IN3
1	1	D6	1	B1	-	C9	6	C1	-	1	1	B2	6	E2	VBAT	S	-	-	-	-
2	2	F6	2	B3	E7	F8	7	E3	-	2	2	A2	7	C1	PC13	I/O	FT	(1), (2)	EVENTOUT	WKUP2, RTC_TS/ RTC_OUT1, TAMP_IN1
3	3	D8	3	C1	E9	E9	8	D1	2	3	3	A1	8	D1	PC14-OSC32_IN (PC14)	I/O	FT_o	(1), (2)	EVENTOUT	OSC32_IN
4	4	E7	4	C2	F8	G9	9	D2	3	4	4	B1	9	E1	PC15-OSC32_OUT (PC15)	I/O	FT_o	(1), (2)	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	10	L10	-	-	-	-	10	D3	VSS	S	-	-	-	-
-	-	-	-	-	-	-	11	B7	-	-	-	-	11	C4	VDD	S	-	-	-	-
5	5	F8	5	D1	G9	J9	12	E1	-	5	5	C1	12	F1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	6	G7	6	D2	H8	H8	13	E2	-	6	6	D1	13	G1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
7	7	H8	7	E1	J9	G7	14	F1	4	7	7	E1	14	H2	NRST (NRST)	I/O	RST	-	-	-
-	-	-	8	E2	G7	-	15	F2	-	-	8	E3	15	H1	PC0	I/O	FT_fha	-	LPTIM1_IN1, OCTOSPI1_IO7, I2C3_SCL(boot), SPI2_RDY, I3C2_SCL, LPUART1_RX, SDMMC1_D5, LPTIM2_IN1, EVENTOUT	ADC1_IN1
-	-	-	9	E3	H6	-	16	G1	-	-	9	E2	16	J2	PC1	I/O	FT_fha	-	TRACED0, LPTIM1_CH1, SPI2_MOSI, I2C3_SDA(boot), I3C1_SDA, I3C2_SDA, LPUART1_TX, OCTOSPI1_IO4, SAI1_SD_A, EVENTOUT	ADC1_IN2
-	-	-	10	E4	K8	-	17	G2	-	-	10	F2	17	J3	PC2	I/O	FT_ha	-	LPTIM1_IN2, SPI2_MISO, OCTOSPI1_IO5, EVENTOUT	ADC2_IN1
-	-	-	11	F2	L9	-	18	H3	-	-	11	G1	18	K2	PC3	I/O	FT_ha	-	LPTIM1_ETR, LPTIM3_CH1, SAI1_D1, SPI2_MOSI, OCTOSPI1_IO6, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC2_IN2
8	8	J7	12	F1	M8	K8	19	H2	-	8	12	F1	19	J1	VSSA	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	20	K1	VREF-	S	-	-	-	-
-	-	-	-	-	-	-	20	H1	-	-	-	-	21	L1	VREF+	S	-	-	-	VREFBUF_OUT
9	9	K8	13	G1	N9	L9	21	J1	5	9	13	H1	22	M1	VDDA	S	-	-	-	-
10	10	H6	14	E5	J7	J7	22	J3	6	10	14	G2	23	L2	PA0	I/O	FT_at	-	TIM2_CH1, SPI3_RDY, UART4_TX, AUDIOCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC1_IN3, WKUP1, TAMP_IN2
11	11	G5	15	F3	L7	L7	23	J2	7	11	15	H2	24	M2	PA1	I/O	FT_fhat	-	LPTIM1_CH2, TIM2_CH2, I2C2_SMBA, I2C1_SMBA, SPI1_SCK, I3C1_SDA(boot), UART4_RX, OCTOSPI1_DQS, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC1_IN4, WKUP3, TAMP_IN5
12	12	H4	16	G2	K6	M8	24	K1	8	12	16	F3	25	K3	PA2	I/O	FT_ha	-	TIM2_CH3, SPI1_RDY, LPUART1_TX, OCTOSPI1_NCS, TIM15_CH1, EVENTOUT	COMP1_INP3, ADC1_IN5, WKUP4/LSCO

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
13	13	M8	17	H2	N7	N9	25	K2	9	13	17	G3	26	L3	PA3	I/O	TT_ha	-	TIM2_CH4, SAI1_CK1, LPUART1_RX, OCTOSPI1_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, COMP1_INP4, ADC1_IN6, WKUP5
-	-	L7	18	-	P8	P8	26	K3	-	-	18	C2	27	E3	VSS	S	-	-	-	-
-	-	N7	19	H1	R9	R9	27	C3	-	-	19	E6	28	G11	VDD	S	-	-	-	-
14	14	K6	20	F4	P6	N7	28	L1	10	14	20	H3	29	M3	PA4	I/O	TT_ha	-	OCTOSPI1_NCS, SPI1_NSS(boot[4]), SPI3_NSS, SAI1_FS_B, LPTIM2_CH1, EVENTOUT	ADC1_IN7, ADC2_IN3, DAC1_OUT1, WKUP2
15	15	J5	21	G3	M6	K6	29	L2	11	15	21	F4	30	K4	PA5	I/O	TT_a	-	PWR_CSLEEP, TIM2_CH1, TIM2_ETR, SPI1_SCK(boot[4]), USART3_RX, LPTIM2_ETR, EVENTOUT	ADC1_IN8, ADC2_IN4, DAC1_OUT2, WKUP6
16	16	M6	22	F5	J5	R7	30	M1	12	16	22	G4	31	L4	PA6	I/O	FT_fha	-	TIM1_BKIN, TIM3_CH1, I3C2_SDA, I2C2_SDA, SPI1_MISO(boot[4]), I3C1_SDA, USART3_CTS/ USART3_NSS, LPUART1_CTS, OCTOSPI1_IO3, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC1_IN9, ADC2_IN5, WKUP7
17	17	J3	23	H3	R7	M6	31	M2	13	17	23	H4	32	M4	PA7	I/O	FT_fha	-	PWR_CSTOP, TIM1_CH1N, TIM3_CH2, I2C3_SCL, SPI1_MOSI(boot[4]), I3C1_SCL, USART3_TX, OCTOSPI1_IO2, LPTIM2_CH2, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC1_IN10, ADC2_IN6, WKUP8
-	-	-	-	-	-	-	-	-	-	-	24	H5	33	K5	PC4	I/O	FT_ha	-	USART3_TX, OCTOSPI1_IO7, EVENTOUT	COMP1_INM2, ADC1_IN11, ADC2_IN7
-	-	-	-	-	-	-	-	-	-	-	25	H6	34	L5	PC5	I/O	FT_at	-	TIM1_CH4N, SAI1_D3, USART3_RX, EVENTOUT	COMP1_INP1, ADC1_IN12, ADC2_IN8, WKUP5, TAMP_IN4

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
18	18	K4	24	H4	N5	N5	32	L3	14	18	26	F5	35	M5	PB0	I/O	TT_ha	-	TIM1_CH2N, TIM3_CH3, LPTIM3_CH1, SPI1_NSS, USART3_CK, OCTOSPI1_IO1, COMP1_OUT, AUDIOCLK, EVENTOUT	OPAMP2_VOUT, ADC1_IN13, ADC2_IN9
19	19	L5	25	G5	L5	P6	33	M3	15	19	27	G5	36	M6	PB1	I/O	FT_ha	-	TIM1_CH3N, TIM3_CH4, LPTIM3_CH2, USART3_RTS/ USART3_DE, LPUART1_RTS/ LPUART1_DE, OCTOSPI1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM1, ADC1_IN14, ADC2_IN10, WKUP4
-	-	N5	26	G4	R5	R5	34	L4	-	20	28	G6	37	L6	PB2	I/O	FT_fha	-	LPTIM1_CH1, I2C2_SCL, I2C3_SMBA, SPI1_RDY, I3C1_SCL, OCTOSPI1_DQS, EVENTOUT	COMP1_INP2, ADC1_IN15, WKUP1, RTC_OUT2
-	-	-	-	-	-	-	35	K5	-	-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, SAI1_SD_B, EVENTOUT	WKUP6
-	-	-	-	-	-	-	36	M4	-	-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, SAI1_SCK_B, EVENTOUT	WKUP7
-	-	-	-	-	-	-	37	L5	-	-	-	-	40	M8	PE9	I/O	FT_h	-	TIM1_CH1, ADF1_CCK0, OCTOSPI1_NCLK, SAI1_FS_B, EVENTOUT	-
-	-	-	-	-	-	-	38	M5	-	-	-	-	41	L8	PE10	I/O	FT_ha	-	TIM1_CH2N, ADF1_SDI0, TSC_G5_IO1, OCTOSPI1_CLK, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	-	39	L6	-	-	-	-	42	M9	PE11	I/O	FT_ha	-	TIM1_CH2, SPI1_RDY, TSC_G5_IO2, OCTOSPI1_NCS, EVENTOUT	-
-	-	-	-	-	-	-	40	M6	-	-	-	-	43	L9	PE12	I/O	FT_ha	-	TIM1_CH3N, SPI1_NSS, TSC_G5_IO3, OCTOSPI1_IO0, EVENTOUT	-
-	-	-	-	-	-	-	41	L7	-	-	-	-	44	M10	PE13	I/O	FT_ha	-	TIM1_CH3, SPI1_SCK, TSC_G5_IO4, OCTOSPI1_IO1, EVENTOUT	-
-	-	-	-	-	-	-	42	M7	-	-	-	-	45	M11	PE14	I/O	FT_h	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, OCTOSPI1_IO2, EVENTOUT	-

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
-	-	-	-	-	-	-	43	L8	-	-	-	-	46	M12	PE15	I/O	FT_h	-	TIM1_BKIN, TIM1_CH4N, SPI1_MOSI, OCTOSPI1_IO3, EVENTOUT	-
-	-	-	27	F6	K4	-	44	M8	-	21	29	G7	47	L10	PB10	I/O	FT_fh	-	TIM2_CH3, LPTIM3_CH1, I3C2_SCL, I2C2_SCL(boot), SPI2_SCK, I3C1_SCL, USART3_TX, LPUART1_RX, TSC_SYNC, OCTOSPI1_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT	WKUP8
-	-	-	-	-	M4	-	45	K8	-	-	-	-	-	-	PB11	I/O	FT_fh	-	TIM2_CH4, I2C2_SDA(boot), SPI2_RDY, USART3_RX, LPUART1_TX, OCTOSPI1_NCS, COMP2_OUT, EVENTOUT	-
20	20	M4	28	H5	P4	P4	46	M9	-	-	-	-	-	-	VLXSMPS	S	-	-	-	-
21	21	N3	29	H6	R3	R3	47	M10	-	-	-	-	-	-	VDDSMPS	S	-	-	-	-
22	22	L3	30	G6	N3	N3	48	L9	-	-	-	-	-	-	VSSSMPS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	22	30	H7	48	L11	VCAP	S	-	-	-	-
23	23	M2	31	H7	P2	P2	49	K9	-	-	-	-	-	-	VDD11	S	-	-	-	-
24	24	L1	32	B2	N1	N1	50	C4	16	23	31	D4	49	F11	VSS	S	-	-	-	-
25	25	N1	33	A1	R1	R1	51	K10	17	24	32	D2	50	G12	VDD	S	-	-	-	-
-	-	-	-	-	M2	-	-	-	-	25	33	H8	51	L12	PB12	I/O	FT_fha	-	TIM1_BKIN, I3C1_SDA, I2C2_SMBA, SPI2_NSS, I3C2_SDA, USART3_CK, LPUART1_RTS/ LPUART1_DE, TSC_G1_IO1, OCTOSPI1_NCLK, TIM15_BKIN, EVENTOUT	-
26	26	K2	34	G8	L3	M4	52	L11	-	26	34	G8	52	K12	PB13	I/O	FT_fha	-	TIM1_CH1N, LPTIM3_IN1, I3C1_SCL, I2C2_SCL, SPI2_SCK, I3C2_SCL, USART3_CTS/ USART3_NSS, LPUART1_CTS, TSC_G1_IO2, TIM15_CH1N, EVENTOUT	-

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
27	27	J1	35	E6	L1	M2	53	M11	-	27	35	F8	53	K11	PB14	I/O	FT_fha	-	TIM1_CH2N, LPTIM3_ETR, I2C2_SDA, SPI2_MISO, I3C2_SDA, USART3_RTS/ USART3_DE, TSC_G1_IO3, TIM15_CH1, EVENTOUT	-
28	28	G1	36	F7	K2	L3	54	M12	-	28	36	F7	54	K10	PB15	I/O	FT_a	-	RTC_REFIN, TIM1_CH3N, LPTIM2_IN2, SAI1_D3, SPI2_MOSI, TSC_G1_IO4, TIM15_CH2, EVENTOUT	WKUP7
-	-	-	-	-	-	-	55	J10	-	-	-	-	55	K9	PD8	I/O	FT	-	USART3_TX, EVENTOUT	-
-	-	-	-	-	-	-	56	K11	-	-	-	-	56	K8	PD9	I/O	FT	-	LPTIM2_IN2, USART3_RX, LPTIM3_IN1, EVENTOUT	-
-	-	-	-	-	-	-	57	L12	-	-	-	-	57	J12	PD10	I/O	FT_a	-	LPTIM2_CH2, USART3_CK, TSC_G6_IO1, LPTIM3_ETR, EVENTOUT	-
-	-	-	-	-	-	-	58	K12	-	-	-	-	58	J11	PD11	I/O	FT_a	-	I2C3_SMBA, USART3_CTS/ USART3_NSS, TSC_G6_IO2, LPTIM2_ETR, EVENTOUT	ADC2_IN11
-	-	-	-	-	J3	-	59	H10	-	-	-	-	59	J10	PD12	I/O	FT_fha	-	TIM4_CH1, I3C1_SCL, I2C3_SCL, USART3_RTS/ USART3_DE, TSC_G6_IO3, LPTIM2_IN1, EVENTOUT	ADC2_IN12
-	-	-	-	-	J1	-	60	J11	-	-	-	-	60	H12	PD13	I/O	FT_fha	-	TIM4_CH2, I3C1_SDA, I2C3_SDA, TSC_G6_IO4, LPTIM4_IN1, LPTIM2_CH1, EVENTOUT	ADC2_IN13
-	-	-	-	-	-	-	61	J12	-	-	-	-	61	H11	PD14	I/O	FT	-	TIM4_CH3, LPTIM3_CH1, EVENTOUT	-
-	-	-	-	-	-	-	62	H11	-	-	-	-	62	H10	PD15	I/O	FT	-	TIM4_CH4, LPTIM3_CH2, EVENTOUT	-
-	-	-	-	-	-	L1	-	-	-	-	-	-	-	-	PG2	I/O	FT_hs	(6)	SPI1_SCK(boot(5)), OCTOSPI1_IO3, EVENTOUT	-
-	-	-	-	-	-	L5	-	-	-	-	-	-	-	-	PG3	I/O	FT_hs	(6)	SPI1_MISO(boot(5)), OCTOSPI1_IO4, EVENTOUT	-
-	-	-	-	-	-	K2	-	-	-	-	-	-	-	-	PG4	I/O	FT_hs	(6)	SPI1_MOSI(boot(5)), OCTOSPI1_IO0, EVENTOUT	-

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
-	-	-	-	-	-	K4	-	-	-	-	-	-	-	-	PG5	I/O	FT_hs	(6)	SPI1_NSS(boot(5)), LPUART1_CTS, OCTOSPI1_IO1, EVENTOUT	-
-	-	-	-	-	-	J1	-	-	-	-	-	-	-	-	PG6	I/O	FT_hs	(6)	OCTOSPI1_DQS, I2C3_SMBA, SPI1_RDY, LPUART1_RTS/ LPUART1_DE, EVENTOUT	-
-	-	-	-	-	-	J3	-	-	-	-	-	-	-	-	PG7	I/O	FT_fhs	(6)	SAI1_CK1, I2C3_SCL, I3C1_SCL, LPUART1_TX, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	J5	-	-	-	-	-	-	-	-	PG8	I/O	FT_fhs	(6)	I2C3_SDA, I3C1_SDA, LPUART1_RX, OCTOSPI1_IO2, EVENTOUT	-
-	-	-	-	-	-	H2	-	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	G1	-	-	-	-	-	-	-	-	VDDIO2	S	-	-	-	-
-	-	-	37	F8	H2	-	63	H12	-	-	37	F6	63	E12	PC6	I/O	FT_ha	-	PWR_CSLEEP, TIM3_CH1, SDMMC1_D0DIR, TSC_G4_IO1, OCTOSPI1_IO3, SDMMC1_D6, EVENTOUT	-
-	-	-	38	E7	G3	-	64	G11	-	-	38	E7	64	E11	PC7	I/O	FT_ha	-	TIM3_CH2, SDMMC1_D123DIR, TSC_G4_IO2, SDMMC1_D7, LPTIM2_CH2, EVENTOUT	-
-	-	-	39	E8	G1	-	65	G12	-	-	39	E8	65	E10	PC8	I/O	FT_ha	-	PWR_CSTOP, TIM3_CH3, TSC_G4_IO3, SDMMC1_D0, LPTIM3_CH1, EVENTOUT	-
-	-	-	40	D8	F2	-	66	F11	-	-	40	D8	66	D12	PC9	I/O	FT_ha	-	TRACED0, TIM3_CH4, TSC_G4_IO4, USB_NOE, SDMMC1_D1, LPTIM3_CH2, EVENTOUT	-
29	29	H2	41	D7	H4	H6	67	F12	18	29	41	D7	67	D11	PA8	I/O	FT_h	-	MCO, TIM1_CH1, SAI1_CK2, SPI1_RDY, USART1_CK, MCO2, TRACECLK, SAI1_SCK_A, LPTIM2_CH1, EVENTOUT	-
30	30	G3	42	D6	G5	G3	68	E11	19	30	42	C7	68	D10	PA9	I/O	FT	-	MCO, TIM1_CH2, SPI2_SCK, USART1_TX(boot), LPUART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
31	31	F2	43	D5	F4	F2	69	E12	20	31	43	C6	69	C12	PA10	I/O	FT	-	CRS_SYNC, TIM1_CH3, LPTIM2_IN2, SAI1_D1, USART1_RX(boot), LPUART1_RX, MCO2, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-
32	32	E1	44	C8	E1	E1	70	D12	21	32	44	C8	70	B12	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS/ USART1_NSS, FDCAN1_RX, EVENTOUT	USB_DM (boot)
33	33	C1	45	C7	C1	C1	71	D11	22	33	45	B8	71	A12	PA12	I/O	FT_u	-	TIM1_ETR, TIM4_ETR, SPI1_MOSI, USART1_RTS/ USART1_DE, FDCAN1_TX, EVENTOUT	USB_DP (boot)
34	34	E3	46	C6	E3	H4	72	C12	23	34	46	A8	72	A11	PA13 (JTMS/ SWDIO)	I/O	FT	(3)	JTMS/SWDIO, IR_OUT, USB_NOE, SAI1_SD_B, EVENTOUT	-
35	35	-	47	G7	-	-	-	-	-	35	47	D5	-	-	VSS	S	-	-	-	-
-	-	B2	48	B8	B2	A1	73	E10	-	-	48	E5	73	C11	VDDUSB	S	-	-	-	-
-	-	D2	-	-	D2	D2	74	C8	-	-	-	-	74	F12	VSS	S	-	-	-	-
36	36	A1	-	H8	A1	B2	75	C10	-	36	-	-	75	G2	VDD	S	-	-	-	-
37	37	C3	49	C5	C3	F4	76	C11	24	37	49	A7	76	A10	PA14 (JTCK/ SWCLK)	I/O	FT	(3)	JTCK/SWCLK, LPTIM1_CH1, I2C2_SMBA, I2C1_SMBA, I2C3_SMBA, SAI1_FS_B, EVENTOUT	-
38	38	A3	50	C4	D4	E3	77	B12	25	38	50	A6	77	A9	PA15 (JTDI)	I/O	FT_a	(3)	JTDI, TIM2_CH1, TIM2_ETR, SAI1_D2, SPI1_NSS, SPI3_NSS(boot),USART3_RTS/ USART3_DE, UART4_RTS/ UART4_DE, TSC_G3_IO1, EVENTOUT	-
-	-	-	51	A7	E5	-	78	A12	-	-	51	B7	78	B11	PC10	I/O	FT_ha	-	TRACED1, LPTIM3_ETR, ADF1_CCK1, SPI3_SCK, USART3_TX(boot), UART4_TX, TSC_G3_IO2, OCTOSPI1_IO0, SDMMC1_D2, EVENTOUT	-

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
-	-	-	52	B5	B4	-	79	B11	-	-	52	B6	79	C10	PC11	I/O	FT_ha	-	LPTIM3_IN1, ADF1_SDI0, OCTOSPI1_NCS, SPI3_MISO, USART3_RX(boot), UART4_RX, TSC_G3_IO3, SDMMC1_D3, EVENTOUT	-
-	-	-	53	B6	A3	-	80	C9	-	-	53	C5	80	B10	PC12	I/O	FT_ha	-	TRACED3, SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, OCTOSPI1_IO1, SDMMC1_CK, EVENTOUT	-
-	-	-	-	-	-	-	81	A11	-	-	-	-	81	C9	PD0	I/O	FT	-	SPI2_NSS(boot), FDCAN1_RX, EVENTOUT	-
-	-	-	-	-	-	-	82	B10	-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK(boot), FDCAN1_TX, EVENTOUT	-
-	-	-	54	A6	C5	-	83	A10	-	-	54	B5	83	C8	PD2	I/O	FT_h	-	TRACED2, TIM3_ETR, USART3_RTS/ USART3_DE, UART5_RX, TSC_SYNC, OCTOSPI1_IO2, SDMMC1_CMD, LPTIM4_ETR, EVENTOUT	-
-	-	-	-	-	-	-	84	B9	-	-	-	-	84	B8	PD3	I/O	FT_h	-	SPI2_SCK, SPI2_MISO(boot), EVENTOUT	-
-	-	-	-	-	-	-	85	A9	-	-	-	-	85	B7	PD4	I/O	FT_h	-	SPI2_MOSI(boot), OCTOSPI1_IO4, EVENTOUT	-
-	-	-	-	-	-	-	86	A8	-	-	-	-	86	A6	PD5	I/O	FT_h	-	SPI2_RDY, OCTOSPI1_IO5, EVENTOUT	-
-	-	-	-	-	-	-	87	B8	-	-	-	-	87	B6	PD6	I/O	FT_h	-	SAI1_D1, SPI3_MOSI, OCTOSPI1_IO6, SAI1_SD_A, EVENTOUT	-
-	-	-	-	-	-	-	88	A7	-	-	-	-	88	A5	PD7	I/O	FT_h	-	OCTOSPI1_IO7, LPTIM4_OUT, EVENTOUT	-
-	-	-	-	-	-	C3	-	-	-	-	-	-	-	-	PG9	I/O	FT_hs	(6)	SPI3_SCK, USART1_TX, OCTOSPI1_IO6, TIM15_CH1N, EVENTOUT	-
-	-	-	-	-	-	A3	-	-	-	-	-	-	-	-	PG10	I/O	FT_hs	(6)	LPTIM1_IN1, SPI3_MISO, USART1_RX, OCTOSPI1_IO7, TIM15_CH1, EVENTOUT	-

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
-	-	-	-	-	-	G5	-	-	-	-	-	-	-	-	PG11	I/O	FT_hs	(6)	LPTIM1_IN2, OCTOSPI1_IO5, SPI3_MOSI, USART1_CTS/ USART1_NSS, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	-	D4	-	-	-	-	-	-	-	-	PG12	I/O	FT_hs	(6)	LPTIM1_ETR, SPI3_NSS, USART1_RTS/ USART1_DE, OCTOSPI1_NCS, EVENTOUT	-
-	-	-	-	-	-	E5	-	-	-	-	-	-	-	-	PG13	I/O	FT_fhs	(6)	I2C1_SDA, I3C2_SCL, SPI3_RDY, USART1_CK, OCTOSPI1_CLK, EVENTOUT	-
-	-	-	-	-	-	B4	-	-	-	-	-	-	-	-	PG14	I/O	FT_fhs	(6)	LPTIM1_CH2, I2C1_SCL, I3C2_SDA, OCTOSPI1_NCLK, EVENTOUT	-
-	-	-	-	-	-	C5	-	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	A5	-	-	-	-	-	-	-	-	VDDIO2	S	-	-	-	-
-	-	-	-	-	-	F6	-	-	-	-	-	-	-	-	PG15	I/O	FT_hs	(6)	LPTIM1_CH1, I2C1_SMBA, OCTOSPI1_DQS, EVENTOUT	-
39	39	B4	55	A5	A5	D6	89	B6	26	39	55	A5	89	A8	PB3 (JTDO/ TRACESWO)	I/O	FT_fha	-	JTDO/TRACESWO, TIM2_CH2, LPTIM1_CH1, ADF1_CCK0, I2C1_SDA, SPI1_SCK, SPI3_SCK(boot), USART1_RTS/ USART1_DE, CRS_SYNC, SAI1_SCK_B, EVENTOUT	COMP2_INM2
40	40	D4	56	B4	B6	B6	90	A6	27	40	56	A4	90	A7	PB4 (NJTRST)	I/O	FT_fha	(3)	NJTRST, LPTIM1_CH2, TIM3_CH1, ADF1_SDI0, I2C3_SDA, SPI1_MISO, SPI3_MISO(boot), USART1_CTS/ USART1_NSS, UART5_RTS/ UART5_DE, TSC_G2_IO1, OCTOSPI1_IO4, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT	COMP2_INP1
41	41	A5	57	D4	D6	E7	91	B5	28	41	57	C4	91	C5	PB5	I/O	FT_ha	-	LPTIM1_IN1, TIM3_CH2, OCTOSPI1_NCLK, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI(boot), USART1_CK, UART5_CTS, TSC_G2_IO2, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	WKUP6

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Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48 SMPS	UFQFPN48 SMPS	WLCSP52 SMPS	LQFP64 SMPS	UFBGA64 SMPS	WLCSP68 SMPS-Q	WLCSP68 SMPS-G	LQFP100 SMPS	UFBGA100 SMPS	UFQFPN32	LQFP48 UFQFPN48	LQFP64	UFBGA64	LQFP100	UFBGA100						
42	42	F4	58	A4	F6	C7	92	A5	29	42	58	D3	92	B5	PB6	I/O	FT_fha	-	LPTIM1_ETR, TIM4_CH1, I2C1_SCL(boot), I3C1_SCL, I3C2_SCL, USART1_TX, TSC_G2_IO3, OCTOSPI1_IO5, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP2, WKUP3
43	43	E5	59	D3	C7	A7	93	A4	30	43	59	C3	93	B4	PB7	I/O	FT_fha	(7)	LPTIM1_IN2, TIM4_CH2, I2C1_SDA(boot), USART1_RX, UART4_CTS, TSC_G2_IO4, OCTOSPI1_IO6, TIM17_CH1N, EVENTOUT	COMP2_INM1, PVD_IN, WKUP4
44	44	C5	60	A3	A7	B8	94	A3	-	44	60	B4	94	A4	PH3-BOOT0 (PH3)	I/O	FT_fh	-	TIM4_CH4, I3C1_SDA, I3C2_SDA, EVENTOUT	-
45	45	B6	61	C3	B8	-	95	B4	-	45	61	B3	95	A3	PB8	I/O	FT_fh	-	TIM4_CH3, SAI1_CK1, I2C1_SCL, I3C2_SCL, SPI3_RDY, SDMMC1_CKIN, FDCAN1_RX(boot), SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	WKUP5
-	-	A7	-	-	C9	-	96	A1	-	46	62	A3	96	B3	PB9	I/O	FT_fh	-	IR_OUT, TIM4_CH4, SAI1_D2, I2C1_SDA, SPI2_NSS, I3C2_SDA, SDMMC1_CDIR, FDCAN1_TX(boot), SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-
-	-	-	-	-	-	-	97	A2	-	-	-	-	97	C3	PE0	I/O	FT	-	TIM4_ETR, TIM16_CH1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	98	A2	PE1	I/O	FT	-	TIM17_CH1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	31	-	-	-	-	-	VCAP	S	-	-	-	-
46	46	-	62	A2	-	-	98	C5	-	-	-	-	-	-	VDD11	S	-	-	-	-
47	47	C7	63	B7	D8	D8	99	D10	32	47	63	D6	99	F2	VSS	S	-	-	-	-
48	48	B8	64	A8	A9	A9	100	K4	1	48	64	E4	100	H3	VDD	S	-	-	-	-

1. *PC13, PC14 and PC15 are supplied through the power switch (by VSW). Since the switch only sinks a limited amount of current (3 mA), the use of PC13 to PC15 GPIOs in output mode is limited. PC13 speed must not exceed 2 MHz with a maximum load of 30 pF. Refer to FT_o electrical characteristics for PC14, PC15. These GPIOs must not be used as current sources (for example to drive a LED).*
2. *After a backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function depends on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the backup domain and RTC register descriptions in the product reference manual.*

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3. *After reset, this pin is configured as JTAG/SWD alternate functions. The internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.*
4. *Boot for all packages except WLCSP68 SMPS-G package.*
5. *Boot only for WLCSP68 SMPS-G package.*
6. *Power supply is VDDIO2.*
7. *On the UFQFPN32 package the pin PB7 is internally connected to BOOT0, and therefore it is denoted as PB7-BOOT0.*

4.3 Alternate functions

Table 22. Alternate function AF0 to AF7

See Table 23 for AF8 to AF15.

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2	LPTIM1/2/3/ TIM1/2/3/4	ADF1/I2C1/2/ I3C1/2/ OCTOSPI1/SAI1/ SPI2/ TIM1/USB	I2C1/2/3/ LPTIM3	I2C3/I3C1/2/ OCTOSPI1/ SPI1/2/3	I3C1/2/ SPI3	USART1/3
Port A	PA0	-	TIM2_CH1	-	-	-	-	SPI3_RDY	-
	PA1	LPTIM1_CH2	TIM2_CH2	-	I2C2_SMBA	I2C1_SMBA	SPI1_SCK	I3C1_SDA	-
	PA2	-	TIM2_CH3	-	-	-	SPI1_RDY	-	-
	PA3	-	TIM2_CH4	-	SAI1_CK1	-	-	-	-
	PA4	-	-	-	OCTOSPI1_NCS	-	SPI1_NSS	SPI3_NSS	-
	PA5	PWR_CSLEEP	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	USART3_RX
	PA6	-	TIM1_BKIN	TIM3_CH1	I3C2_SDA	I2C2_SDA	SPI1_MISO	I3C1_SDA	USART3_CTS/ USART3_NSS
	PA7	PWR_CSTOP	TIM1_CH1N	TIM3_CH2	-	I2C3_SCL	SPI1_MOSI	I3C1_SCL	USART3_TX
	PA8	MCO	TIM1_CH1	-	SAI1_CK2	-	SPI1_RDY	-	USART1_CK
	PA9	MCO	TIM1_CH2	-	SPI2_SCK	-	-	-	USART1_TX
	PA10	CRS_SYNC	TIM1_CH3	LPTIM2_IN2	SAI1_D1	-	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS/ USART1_NSS
	PA12	-	TIM1_ETR	TIM4_ETR	-	-	SPI1_MOSI	-	USART1_RTS/ USART1_DE
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_CH1	-	I2C2_SMBA	I2C1_SMBA	I2C3_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	SAI1_D2	-	SPI1_NSS	SPI3_NSS	USART3_RTS/ USART3_DE

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2	LPTIM1/2/3/ TIM1/2/3/4	ADF1/I2C1/2/ I3C1/2/ OCTOSPI1/SAI1/ SPI2/ TIM1/USB	I2C1/2/3/ LPTIM3	I2C3/I3C1/2/ OCTOSPI1/ SPI1/2/3	I3C1/2/ SPI3	USART1/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	-	LPTIM3_CH1	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	-	LPTIM3_CH2	-	-	USART3_RTS/ USART3_DE
	PB2	-	LPTIM1_CH1	-	I2C2_SCL	I2C3_SMBA	SPI1_RDY	I3C1_SCL	-
	PB3	JTDO/ TRACESWO	TIM2_CH2	LPTIM1_CH1	ADF1_CCK0	I2C1_SDA	SPI1_SCK	SPI3_SCK	USART1_RTS/ USART1_DE
	PB4	NJTRST	LPTIM1_CH2	TIM3_CH1	ADF1_SDI0	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS/ USART1_NSS
	PB5	-	LPTIM1_IN1	TIM3_CH2	OCTOSPI1_NCLK	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	-	I2C1_SCL	I3C1_SCL	I3C2_SCL	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	-	I2C1_SDA	-		USART1_RX
	PB8	-	-	TIM4_CH3	SAI1_CK1	I2C1_SCL	I3C2_SCL	SPI3_RDY	-
	PB9	-	IR_OUT	TIM4_CH4	SAI1_D2	I2C1_SDA	SPI2_NSS	I3C2_SDA	-
	PB10	-	TIM2_CH3	LPTIM3_CH1	I3C2_SCL	I2C2_SCL	SPI2_SCK	I3C1_SCL	USART3_TX
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	SPI2_RDY	-	USART3_RX
	PB12	-	TIM1_BKIN	-	I3C1_SDA	I2C2_SMBA	SPI2_NSS	I3C2_SDA	USART3_CK
	PB13	-	TIM1_CH1N	LPTIM3_IN1	I3C1_SCL	I2C2_SCL	SPI2_SCK	I3C2_SCL	USART3_CTS/ USART3_NSS
	PB14	-	TIM1_CH2N	LPTIM3_ETR	-	I2C2_SDA	SPI2_MISO	I3C2_SDA	USART3_RTS/ USART3_DE
	PB15	RTC_REFIN	TIM1_CH3N	LPTIM2_IN2	SAI1_D3	-	SPI2_MOSI	-	-
Port C	PC0	-	LPTIM1_IN1	-	OCTOSPI1_IO7	I2C3_SCL	SPI2_RDY	I3C2_SCL	-
	PC1	TRACED0	LPTIM1_CH1	-	SPI2_MOSI	I2C3_SDA	I3C1_SDA	I3C2_SDA	-
	PC2	-	LPTIM1_IN2		-	-	SPI2_MISO	-	-
	PC3	-	LPTIM1_ETR	LPTIM3_CH1	SAI1_D1		SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	TIM1_CH4N	-	SAI1_D3	-	-	-	USART3_RX
	PC6	PWR_CSLEEP	-	TIM3_CH1	-	-	-	-	-
	PC7	-	-	TIM3_CH2	-	-	-	-	-

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2	LPTIM1/2/3/ TIM1/2/3/4	ADF1/I2C1/2/ I3C1/2/ OCTOSPI1/SAI1/ SPI2/ TIM1/USB	I2C1/2/3/ LPTIM3	I2C3/I3C1/2/ OCTOSPI1/ SPI1/2/3	I3C1/2/ SPI3	USART1/3
Port C	PC8	PWR_CSTOP	-	TIM3_CH3	-	-	-	-	-
	PC9	TRACED0	-	TIM3_CH4	-	-	-	-	-
	PC10	TRACED1	-	LPTIM3_ETR	ADF1_CCK1	-	-	SPI3_SCK	USART3_TX
	PC11	-		LPTIM3_IN1	ADF1_SDI0	-	OCTOSPI1_NCS	SPI3_MISO	USART3_RX
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-
Port D	PD0	-	-	-	-	-	SPI2_NSS	-	-
	PD1	-	-	-	-	-	SPI2_SCK	-	-
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	USART3_RTS/ USART3_DE
	PD3	-	-	-	SPI2_SCK	-	SPI2_MISO	-	-
	PD4	-	-	-	-	-	SPI2_MOSI	-	-
	PD5	-	-	-	-	-	SPI2_RDY	-	-
	PD6	-	-	-	SAI1_D1	-	SPI3_MOSI	-	-
	PD7	-	-	-	-	-	-	-	-
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	LPTIM2_IN2	-	-	-	-	USART3_RX
	PD10	-	-	LPTIM2_CH2	-	-	-	-	USART3_CK
	PD11	-	-	-	-	I2C3_SMBA	-	-	USART3_CTS/ USART3_NSS
	PD12	-	-	TIM4_CH1	I3C1_SCL	I2C3_SCL	-	-	USART3_RTS/ USART3_DE
	PD13	-	-	TIM4_CH2	I3C1_SDA	I2C3_SDA	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2	LPTIM1/2/3/ TIM1/2/3/4	ADF1/I2C1/2/ I3C1/2/ OCTOSPI1/SAI1/ SPI2/ TIM1/USB	I2C1/2/3/ LPTIM3	I2C3/I3C1/2/ OCTOSPI1/ SPI1/2/3	I3C1/2/ SPI3	USART1/3
Port E	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECLK	-	TIM3_ETR	SAI1_CK1	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	OCTOSPI1_DQS	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	SAI1_D2	-	-	-	-
	PE5	TRACED2	-	TIM3_CH3	SAI1_CK2	-	-	-	-
	PE6	TRACED3	-	TIM3_CH4	SAI1_D1	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	-	-
	PE8	-	TIM1_CH1N	-	-	-	-	-	-
	PE9	-	TIM1_CH1	-	ADF1_CCK0	-	-	-	-
	PE10	-	TIM1_CH2N	-	ADF1_SDI0	-	-	-	-
	PE11	-	TIM1_CH2	-	-	-	SPI1_RDY	-	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	-	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	-	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_CH4N	-	SPI1_MOSI	-	-
Port G	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	OCTOSPI1_DQS	I2C3_SMBA	SPI1_RDY	-	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	I3C1_SCL	-	-
	PG8	-	-	-	-	I2C3_SDA	I3C1_SDA	-	-
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	-	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	OCTOSPI1_IO5	-	-	SPI3_MOSI	USART1_CTS/ USART1_NSS
	PG12	-	LPTIM1_ETR	-	-	-	-	SPI3_NSS	USART1_RTS/ USART1_DE

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		CRS/LPTIM1/ SYS_AF	LPTIM1/ TIM1/2	LPTIM1/2/3/ TIM1/2/3/4	ADF1/I2C1/2/ I3C1/2/ OCTOSPI1/SAI1/ SPI2/ TIM1/USB	I2C1/2/3/ LPTIM3	I2C3/I3C1/2/ OCTOSPI1/ SPI1/2/3	I3C1/2/ SPI3	USART1/3
Port G	PG13	-	-	-	-	I2C1_SDA	I3C2_SCL	SPI3_RDY	USART1_CK
	PG14	-	LPTIM1_CH2	-	-	I2C1_SCL	I3C2_SDA	-	-
	PG15	-	LPTIM1_CH1		-	I2C1_SMBA	-	-	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH3	-	-	TIM4_CH4	I3C1_SDA	-	-	I3C2_SDA	-

Table 23. Alternate function AF8 to AF15

See Table 22 for AF0 to AF7.

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	FDCAN1/ TSC	CRS /OCTOSPI1/ USB	MCO2	COMP1/2/ SDMMC1/ SYS_AF	LPTIM2/4/ SAI1	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port A	PA0	UART4_TX	-	-	-	-	AUDIOCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	OCTOSPI1_DQS	-	-	-	TIM15_CH1N	
	PA2	LPUART1_TX	-	OCTOSPI1_NCS	-	-	-	TIM15_CH1	
	PA3	LPUART1_RX	-	OCTOSPI1_CLK		-	SAI1_MCLK_A	TIM15_CH2	
	PA4	-	-	-	-	-	SAI1_FS_B	LPTIM2_CH1	
	PA5	-	-	-	-	-	-	LPTIM2_ETR	
	PA6	LPUART1_CTS	-	OCTOSPI1_IO3	-	-	-	TIM16_CH1	
	PA7	-	-	OCTOSPI1_IO2	-	-	LPTIM2_CH2	TIM17_CH1	
	PA8	-	-	-	MCO2	TRACECLK	SAI1_SCK_A	LPTIM2_CH1	
	PA9	LPUART1_TX	-	-	-	-	SAI1_FS_A	TIM15_BKIN	
	PA10	LPUART1_RX	-	-	MCO2	-	SAI1_SD_A	TIM17_BKIN	
	PA11	-	FDCAN1_RX	-		-	-	-	
	PA12	-	FDCAN1_TX	-		-	-	-	
	PA13	-	-	USB_NOE	-	-	SAI1_SD_B	-	
	PA14	-	-	-	-	-	SAI1_FS_B	-	

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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	FDCAN1/ TSC	CRS /OCTOSPI1/ USB	MCO2	COMP1/2/ SDMMC1/ SYS_AF	LPTIM2/4/ SAI1	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port A	PA15	UART4_RTS/ UART4_DE	TSC_G3_IO1	-	-	-	-	-	
Port B	PB0	-	-	OCTOSPI1_IO1	-	COMP1_OUT	AUDIOCLK	-	
	PB1	LPUART1_RTS/ LPUART1_DE	-	OCTOSPI1_IO0	-	-	-	LPTIM2_IN1	
	PB2	-	-	OCTOSPI1_DQS	-	-	-	-	
	PB3	-	-	CRS_SYNC	-	-	SAI1_SCK_B	-	
	PB4	UART5_RTS/ UART5_DE	TSC_G2_IO1	OCTOSPI1_IO4	-	-	SAI1_MCLK_B	TIM17_BKIN	
	PB5	UART5_CTS	TSC_G2_IO2	-		COMP2_OUT	SAI1_SD_B	TIM16_BKIN	
	PB6	-	TSC_G2_IO3	OCTOSPI1_IO5	-	-	SAI1_FS_B	TIM16_CH1N	
	PB7	UART4_CTS	TSC_G2_IO4	OCTOSPI1_IO6		-	-	TIM17_CH1N	
	PB8	SDMMC1_CKIN	FDCAN1_RX	-	-	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	
	PB9	SDMMC1_CDIR	FDCAN1_TX	-	-	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	
	PB10	LPUART1_RX	TSC_SYNC	OCTOSPI1_CLK	-	COMP1_OUT	SAI1_SCK_A	-	
	PB11	LPUART1_TX	-	OCTOSPI1_NCS	-	COMP2_OUT	-	-	
	PB12	LPUART1_RTS/ LPUART1_DE	TSC_G1_IO1	OCTOSPI1_NCLK	-	-	-	TIM15_BKIN	
	PB13	LPUART1_CTS	TSC_G1_IO2	-	-	-	-	TIM15_CH1N	
	PB14	-	TSC_G1_IO3	-	-	-	-	TIM15_CH1	
	PB15	-	TSC_G1_IO4	-	-	-	-	TIM15_CH2	
Port C	PC0	LPUART1_RX	-	-	-	SDMMC1_D5	-	LPTIM2_IN1	
	PC1	LPUART1_TX	-	OCTOSPI1_IO4	-	-	SAI1_SD_A	-	
	PC2	-	-	OCTOSPI1_IO5	-	-	-	-	
	PC3	-	-	OCTOSPI1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	
	PC4	-		OCTOSPI1_IO7	-	-	-	-	
	PC5	-	-	-	-	-	-	-	
	PC6	SDMMC1_D0DIR	TSC_G4_IO1	OCTOSPI1_IO3		SDMMC1_D6	-	-	
	PC7	SDMMC1_D123DIR	TSC_G4_IO2	-	-	SDMMC1_D7	-	LPTIM2_CH2	
	PC8	-	TSC_G4_IO3	-	-	SDMMC1_D0	-	LPTIM3_CH1	

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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	FDCAN1/ TSC	CRS /OCTOSPI1/ USB	MCO2	COMP1/2/ SDMMC1/ SYS_AF	LPTIM2/4/ SAI1	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port C	PC9	-	TSC_G4_IO4	USB_NOE	-	SDMMC1_D1	-	LPTIM3_CH2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	OCTOSPI1_IO0	-	SDMMC1_D2	-	-	
	PC11	UART4_RX	TSC_G3_IO3	-	-	SDMMC1_D3	-	-	
	PC12	UART5_TX	TSC_G3_IO4	OCTOSPI1_IO1	-	SDMMC1_CK	-	-	
	PC13	-	-	-	-	-	-	-	
	PC14	-	-	-	-	-	-	-	
	PC15	-	-	-	-	-	-	-	
Port D	PD0	-	FDCAN1_RX	-	-	-	-	-	
	PD1	-	FDCAN1_TX	-	-	-	-	-	
	PD2	UART5_RX	TSC_SYNC	OCTOSPI1_IO2	-	SDMMC1_CMD	LPTIM4_ETR	-	
	PD3	-	-	-	-	-	-	-	
	PD4	-	-	OCTOSPI1_IO4	-	-	-	-	
	PD5	-	-	OCTOSPI1_IO5	-	-	-	-	
	PD6	-	-	OCTOSPI1_IO6	-	-	SAI1_SD_A	-	
	PD7	-	-	OCTOSPI1_IO7	-	-	LPTIM4_OUT	-	
	PD8	-	-	-	-	-	-	-	
	PD9	-	-	-	-	-	-	LPTIM3_IN1	
	PD10	-	TSC_G6_IO1	-	-	-	-	LPTIM3_ETR	
	PD11	-	TSC_G6_IO2	-	-	-	-	LPTIM2_ETR	
	PD12	-	TSC_G6_IO3	-	-	-	-	LPTIM2_IN1	
	PD13	-	TSC_G6_IO4	-	-	-	LPTIM4_IN1	LPTIM2_CH1	
	PD14	-	-	-	-	-	-	LPTIM3_CH1	
	PD15	-	-	-	-	-	-	LPTIM3_CH2	
Port E	PE0	-	-	-	-	-	-	TIM16_CH1	
	PE1	-	-	-	-	-	-	TIM17_CH1	
	PE2	-	TSC_G7_IO1	-	-	-	SAI1_MCLK_A	-	
	PE3	-	TSC_G7_IO2	-	-	-	SAI1_SD_B	-	
	PE4	-	TSC_G7_IO3	-	-	-	SAI1_FS_A	-	

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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/ SDMMC1/ UART4/5	FDCAN1/ TSC	CRS /OCTOSPI1/ USB	MCO2	COMP1/2/ SDMMC1/ SYS_AF	LPTIM2/4/ SAI1	LPTIM2/3/ TIM2/15/16/17	EVENTOUT
Port E	PE5	-	TSC_G7_IO4	-	-	-	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	-	-	-	SAI1_SD_A	-	
	PE7	-	-	-	-	-	SAI1_SD_B	-	
	PE8	-	-	-	-	-	SAI1_SCK_B	-	
	PE9	-	-	OCTOSPI1_NCLK		-	SAI1_FS_B	-	
	PE10	-	TSC_G5_IO1	OCTOSPI1_CLK	-	-	SAI1_MCLK_B	-	
	PE11	-	TSC_G5_IO2	OCTOSPI1_NCS	-	-	-	-	
	PE12	-	TSC_G5_IO3	OCTOSPI1_IO0	-	-	-	-	
	PE13	-	TSC_G5_IO4	OCTOSPI1_IO1	-	-	-	-	
	PE14	-	-	OCTOSPI1_IO2	-	-	-	-	
	PE15	-	-	OCTOSPI1_IO3	-	-	-	-	
Port G	PG2	-	-	OCTOSPI1_IO3	-	-	-	-	
	PG3	-	-	OCTOSPI1_IO4	-	-	-	-	
	PG4	-	-	OCTOSPI1_IO0	-	-	-	-	
	PG5	LPUART1_CTS	-	OCTOSPI1_IO1	-	-	-	-	
	PG6	LPUART1_RTS/ LPUART1_DE	-	-	-	-	-	-	
	PG7	LPUART1_TX	-	-	-	-	SAI1_MCLK_A	-	
	PG8	LPUART1_RX	-	OCTOSPI1_IO2	-	-	-	-	
	PG9	-	-	OCTOSPI1_IO6	-	-	-	TIM15_CH1N	
	PG10	-	-	OCTOSPI1_IO7	-	-	-	TIM15_CH1	
	PG11	-	-	-	-	-	-	TIM15_CH2	
	PG12	-	-	OCTOSPI1_NCS		-	-	-	
	PG13	-	-	OCTOSPI1_CLK	-	-	-	-	
	PG14	-	-	OCTOSPI1_NCLK	-	-	-	-	
	PG15	-	-	OCTOSPI1_DQS	-	-	-	-	
Port H	PH0	-	-	-	-	-	-	-	
	PH1	-	-	-	-	-	-	-	
	PH3	-	-	-	-	-	-	-	

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5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = T_A(Max) (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes, and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range and supply voltage range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 22.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 23.

Figure 22. Pin loading conditions

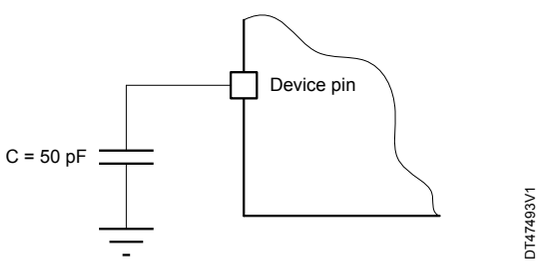
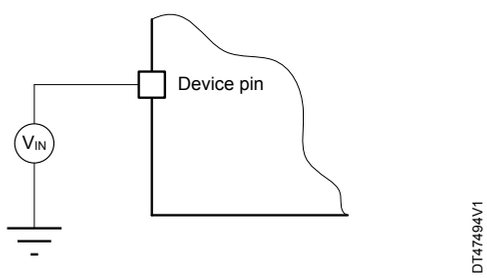


Figure 23. Pin input voltage

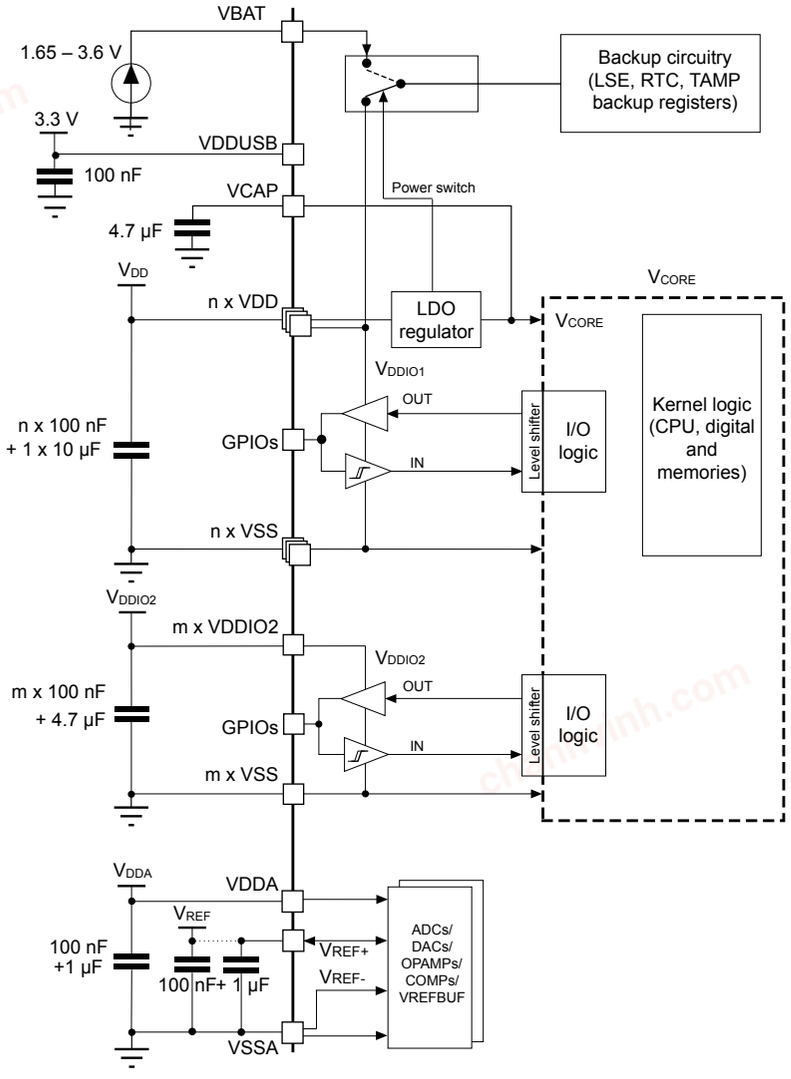


5.1.6 Power supply scheme

Each power supply pair (such as V_{DD}/V_{SS} or V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown in the following figures. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the proper functionality of the device.

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Figure 24. **STM32U385xx power supply scheme (without SMPS)**

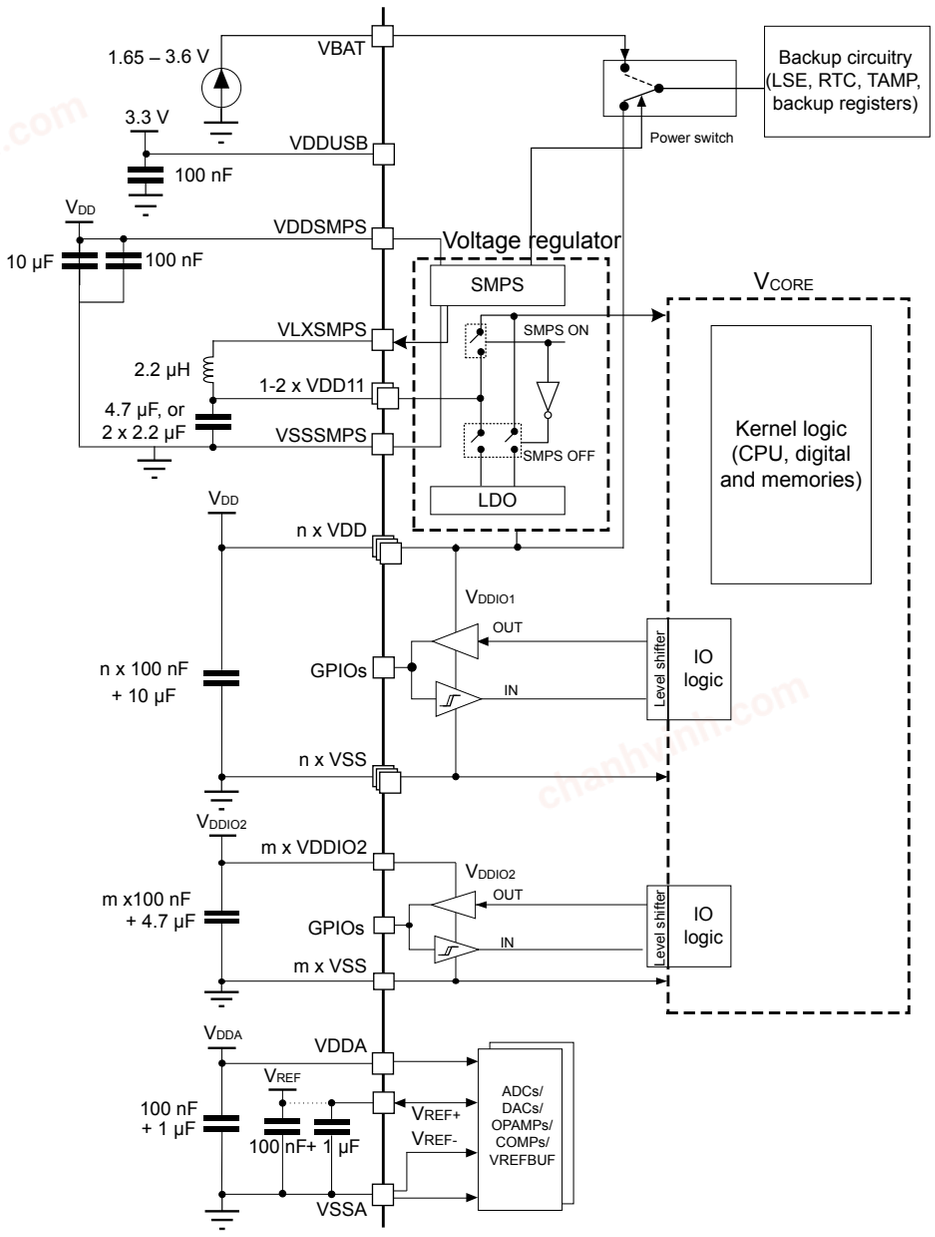


The external capacitor on VCAP pin requires the following characteristics:

- COUT = 4.7 µF
- COUT ESR < 20 mΩ at 3 MHz
- COUT rated voltage ≥ 10 V

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Figure 25. STM32U385xx power supply scheme (with SMPS)



Note: SMPS and LDO regulators provide, in a concurrent way, the V_{CORE} supply depending on application requirements. However, only one of them is active at the same time. When SMPS is active, it feeds the V_{CORE} on the two VDD11 pins supplied by the filtered SMPS VLXSMPS output pin. A 2.2 µH coil and a 2.2 µF capacitor on each VDD11 pin are then required. When LDO is active, it supplies the V_{CORE} and regulates it using the same decoupling capacitors on VDD11 pins.

Note: It is recommended to add a decoupling capacitor of 100 nF near each VDD11 pin/ball, but it is not mandatory.

The external capacitors on VDD11 pins require the following characteristics:

- COUT = 2 × 2.2 µF ±20%
- COUT ESR < 20 mΩ at 3 MHz
- COUT rated voltage ≥ 10 V

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The external capacitor on VDDSMPS pin requires the following characteristics:

- CIN = 10 µF ±20%
- CIN ESR < 10 mΩ at 3 MHz
- CIN rated voltage ≥ 10 V

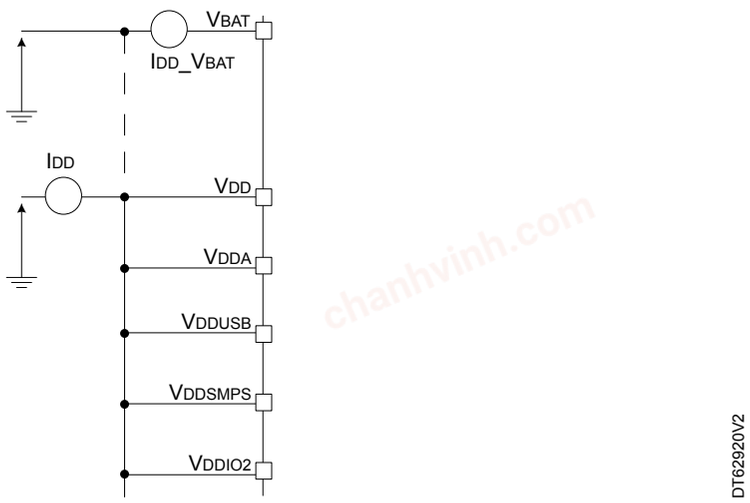
The external inductance between VLXSMPS and VDD11 requires the following characteristics:

- L = 2.2 µH ±20%
- L ISAT > 0.5 A
- L DCR < 200 mΩ

5.1.7 Current consumption measurement

The I_{DD} parameters given in various tables in the next sections, represent the total MCU consumption including the current supplying V_{DD}, V_{DDIO2}, V_{DDA}, V_{DDUSB}, V_{BAT}, and V_{DDSMPS} (if the device embeds the SMPS).

Figure 26. Current consumption measurement



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 24, Table 25, and Table 26 may damage permanently the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard. Extended mission profiles are available on demand.

Table 24. Voltage characteristics

All main power (VDD, VDDSMPS, VDDA, VDDUSB, VDDIO2, VBAT) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}[(1)(2)(3)], V_{DDSMPS}, V_{DDA}, V_{DDUSB}, V_{DDIO2}[(1)(2)(3)], V_{BAT}, V_{REF+})	-0.3	4.0	V
V_{DDIOx}[(2)] - V_{SS}	I/O supply when HSLV[(3)] = 0	-0.3	4.0	
	I/O supply when HSLV = 1	-0.3	2.75	
V_{IN}[(4)]	Input voltage on FT_xx pins	V_{SS} - 0.3	Min (min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0, 6.0)[(5)(6)]	

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Symbol	Ratings	Min	Max	Unit
V_{IN}(4)	Input voltage on FT_t and FT_o pins in V_{BAT} mode	V_{SS} - 0.3	Min (min (V_{BAT}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0, 6.0) (5)(6)	V
	PC13	V_{SS} - 0.3	Min (min (V_{DD},V_{SW}) + 4.0, 6.0)	
	Input voltage on any other pins	V_{SS} - 0.3	4.0	
V_{REF+} - V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	
ΔV_{DDx}	Variations between different VDDx power pins of the same domain	-	50.0	mV
V_{SSx} - V_{SS}	Variations between all the different ground pins(7)	-	50.0	

1. *If HSLV = 0.*
2. *V_{DDIO1} or V_{DDIO2} or V_{SW}. V_{DDIO1} = V_{DD}.*
3. *HSLV = High-speed low-voltage mode. Refer to General-purpose I/Os (GPIO) section of RM0487.*
4. *V_{IN} maximum must always be respected. Refer to Table 25 for the maximum allowed injected current values.*
5. *This formula has to be applied only on the power supplies related to the I/O structure described in the pin definition table.*
6. *To sustain a voltage higher than 4 V, the internal pull-up/pull-down resistors must be disabled.*
7. *Including VREF- pin.*

Table 25. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	150	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
IV_{DD}	Maximum current into each VDD power pin (source)(1)	100	
IV_{SS}	Maximum current out of each VSS ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	120	
	Total output current sourced by sum of all I/Os and control pins(2)	120	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xx, TT_xx, RST pins	-5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. *All main power (V_{DD}, V_{DDSMPS}, V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.*
2. *This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins, referring to high pin count QFP packages.*
3. *A negative injection is induced by V_{IN} < V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. Refer also to Table 24 for the minimum allowed input voltage values.*
4. *Positive injection (when V_{IN} > V_{DDIOx}) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.*
5. *When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the negative injected currents (instantaneous values).*

Table 26. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	110	

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5.3 Operating conditions

5.3.1 General operating conditions

Table 27. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	HSLV[1] = 0	1.71[2]	-	3.6	V
		HSLV = 1	1.71[2]	-	2.7	
V_{DDSMPS}	Supply voltage for the internal SMPS step-down converter	-	V_{DD}			
V_{DDIO2}	Supply voltage for PG[15:2] I/Os	At least one I/O in PG[15:2] used, HSLV = 0	1.08	-	3.6	
		At least one I/O in PG[15:2] used, HSLV = 1			2.7	
		PG[15:2] not used	0		3.6	
V_{DDUSB}	USB supply voltage	USB used	3.0	-	3.6	
		USB not used	0			
V_{DDA}	Analog supply voltage	COMP used	1.58	-	3.6	
		DAC or OPAMP used	1.60	-		
		ADC used	1.62	-		
		VREFBUF used (normal mode)	1.80	-		
		ADC, DAC, COMP, OPAMP, and VREFBUF not used	1.58	-		
V_{BAT}	Backup domain supply voltage	-	1.65[3]	-	3.6	
V_{IN}	I/O input voltage	All I/Os except TT_xx pins	-0.3	-	Min(min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 3.6, 5.5)[4][5]	
		PC13	VSS -0.3		Min (min) V_{DD}, V_{SW}) + 3.6 V, 5.5 V)	
		Input voltage on FT_t and FT_o pins in V_{BAT} mode	-0.3		3.6	
		TT_xx I/Os	-0.3		V_{DDIOx} + 0.3	
I_{IO_SW}	Sum of output current sourced by all I/Os powered by V_{SW}[6]	-	-		3	mA
V_{CORE}	Internal regulator ON	Range 1	0.8	0.9	1.0	V
		Range 2	0.65	0.75	0.85	
f_{HCLK}	AHB clock frequency	Range 1	-	-	96	MHz
		Range 2			48	
f_{PCLKx} (x = 1, 2, 3)	APB1, APB2, APB3 clock frequency	Range 1	-	-	96	
		Range 2			48	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_D	Power dissipation at TA = 85 °C for suffix 6(7)	UFQFPN32	See Section 6.11: Package thermal characteristics for application appropriate thermal resistance and package. The power dissipation is then calculated according to ambient temperature (T_A) and maximum junction temperature (T_J) and selected thermal resistance.			mW
		LQFP48				
		UFQFPN48				
		WLCSP52				
		LQFP64				
		UFBGA64				
		WLCSP68-G				
		WLCSP68-Q				
		LQFP100				
		UFBGA100				
P_D	Power dissipation at TA = 105 °C for suffix 7(7)	UFQFPN32				
		LQFP48				
		UFQFPN48				
		WLCSP52				
		LQFP64				
		UFBGA64				
		WLCSP68-G				
		WLCSP68-Q				
		LQFP100				
		UFBGA100				
T_A	Ambient temperature for suffix 6	Maximum power dissipation	–40	-	85	°C
		Low-power dissipation(8)			105	
	Ambient temperature for suffix 7	Maximum power dissipation			105	
		Low-power dissipation(8)			110	
T_J	Junction temperature range	Suffix 6 version	-40	-	105	
		Suffix 7 version			110	

1. *HSLV means high-speed low-voltage mode (refer to the product reference manual).*
2. *When RESET is released, the functionality is guaranteed down to V_{BORx} min.*
3. *In V_{BAT} mode, the functionality is guaranteed down to V_{BOR_VBAT} min.*
4. *This formula has to be applied only on the power supplies related to the I/O structure described by the pin definition table. The maximum I/O input voltage is the smallest value between Min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 3.6 V, and 5.5 V.*
5. *For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled.*
6. *The I/Os powered by V_{SW} are: PC13, PC14, PC15*
7. *If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see Section 6.11: Package thermal characteristics).*
8. *In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_J max (see Section 6.11: Package thermal characteristics).*

5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are derived from tests performed under the ambient temperature condition summarized in Table 27.

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Table 28. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise-time rate	-	0	∞	µs/V
	V_{DD} fall-time rate	ULPMEN = 0	20	∞	
		Standby mode, BOR level 0 selected with ULPMEN = 1	250	∞	ms/V

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature conditions summarized in Table 27.

Table 29. Embedded reset and power control block characteristics

The values in this table are evaluated by characterization and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after BOR0 released	V_{DD} rising	-	-	-	900	µs
V_{BOR0}	Brownout reset threshold 0	Rising edge	-	1.63	1.65	1.67	V
		Falling edge	Range 1	1.62	1.63	1.65	
			Range 2 and low-power modes	1.61	1.63	1.65	
V_{BOR1}	Brownout reset threshold 1	Rising edge	-	2.07	2.09	2.11	
		Falling edge	-	2.00	2.02	2.04	
V_{BOR2}	Brownout reset threshold 2	Rising edge	-	2.28	2.30	2.32	
		Falling edge	-	2.17	2.20	2.23	
V_{BOR3}	Brownout reset threshold 3	Rising edge	-	2.57	2.60	2.63	
		Falling edge	-	2.48	2.51	2.54	
V_{BOR4}	Brownout reset threshold 4	Rising edge	-	2.86	2.89	2.92	
		Falling edge	-	2.77	2.80	2.83	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	-	2.12	2.14	2.16	
		Falling edge	-	2.02	2.04	2.06	
V_{PVD1}	Programmable voltage detector threshold 1	Rising edge	-	2.27	2.30	2.32	
		Falling edge	-	2.17	2.20	2.23	
V_{PVD2}	Programmable voltage detector threshold 2	Rising edge	-	2.43	2.45	2.48	
		Falling edge	-	2.32	2.35	2.37	
V_{PVD3}	Programmable voltage detector threshold 3	Rising edge	-	2.57	2.60	2.63	
		Falling edge	-	2.48	2.51	2.54	
V_{PVD4}	Programmable voltage detector threshold 4	Rising edge	-	2.70	2.73	2.76	
		Falling edge	-	2.60	2.63	2.66	
V_{PVD5}	Programmable voltage detector threshold 5	Rising edge	-	2.86	2.89	2.92	
		Falling edge	-	2.76	2.80	2.83	
V_{PVD6}	Programmable voltage detector threshold 6	Rising edge	-	2.94	2.97	3.00	
		Falling edge	-	2.85	2.89	2.92	
V_{hyst_BOR0}	Hysteresis voltage of BOR0	-	-	-	19	-	mV

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BOR (unless BOR0) and PVD	-	-	-	83	-	mV
$t_{BOR0_sampling}$	BOR0 sampling period	ULPMEN = 1	-	-	30	55	ms
I_{DD_BOR0}	additional BOR0 consumption if ULPMEN = 0 versus ULPMEN = 1	Standby mode	-	-	60	-	nA
$I_{DD_BOR_PVD}$(1)	BOR(2) (unless BOR0) and PVD consumption from V_{DD}(3)	-	-	-	1	1.5	µA
V_{BOR_VBAT}(1)	V_{BAT} brownout reset threshold		-	1.58	-	1.65	V
$t_{BOR_VBAT_sampling}$	V_{BAT} BOR sampling period in VBAT mode	MONEN=0	-	-	0.5	2.5	s
V_{AVM1}	V_{DDA} voltage monitor 1 threshold	Rising edge	-	1.62	1.67	1.71	V
		Falling edge	-	1.59	1.63	1.67	
V_{AVM2}	V_{DDA} voltage monitor 2 threshold	Rising edge	-	1.80	1.85	1.89	
		Falling edge	-	1.76	1.81	1.85	
V_{IO2VM}	V_{DDIO2} voltage monitor threshold	-	-	0.98	1.01	1.03	
V_{UVM}	V_{DDUSB} voltage monitor threshold	-	-	1.18	1.21	1.24	-
V_{hyst_AVM}	Hysteresis of V_{DDA} voltage monitor	-	-	-	40	-	mV
I_{DD_VM}(1)	Voltage monitor consumption from V_{DD} (AVM1, AVM2, IO2VM, or UVM single instance)	-	-	-	0.4	0.6	µA
$I_{DD_AVM_A}$(1)	V_{DDA} voltage monitor consumption from V_{DDA} (Resistor bridge)	-	-	-	1.25	1.85	

1. *Specified by design. Not tested in production.*
2. *BOR0 is enabled in all modes (except Shutdown) and its consumption is therefore included in the supply current characteristics tables (refer to Section 5.3.6: Supply current characteristics).*
3. *This is also the consumption saved in Standby mode when ULPMEN = 1*

5.3.4 SMPS characteristics

SMPS is asynchronous in all ranges and in low-power modes.

5.3.5 Embedded voltage reference

The parameters given in Table 30. Embedded internal voltage reference are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 1.

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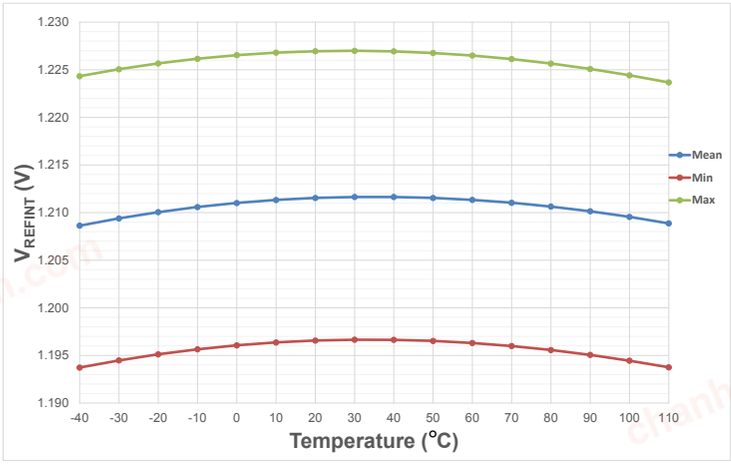
Table 30. Embedded internal voltage reference

The values in this table are specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltages	Range 1	1.175	1.215	1.243	V
		Range 2 and low-power modes	1.170	1.215	1.248	V
$t_{S_vrefint}$(2)	ADC sampling time when reading the internal reference voltage	-	12.65	-	-	µs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enabled	-		4	6	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-		1.5	2.1	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	8.75	mV
T_{coeff}	Average temperature coefficient	-40 °C < T_J < 110 °C	-	28	78	ppm/°C
A_{coeff}	Long-term stability	1000 hours, T_J = 25°C	-	400	1000	ppm
$V_{DDcoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V		726	1900	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	V_{DD} = 3.3 V	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage	V_{DD} = 3.3 V	49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage	V_{DD} = 3.3 V	74	75	76	

1. *V_{REFINT} does not take into account package and soldering effects.*
2. *The shortest sampling time for the application can be determined by multiple iterations.*

Figure 27. V_{REFINT} versus temperature



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5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Section 5.1.7: Current consumption measurement.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait-state number, depending on the f_{HCLK} frequency (refer to the tables *Number of wait states according to CPU clock (HCLK) frequency* available in the product reference manual).
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$.
- The voltage scaling range is adjusted to f_{HCLK} frequency as follows:
  - Voltage range 1: Up to 96 MHz
  - Voltage range 2: Up to 48 MHz

The parameters given in the tables below are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 27. General operating conditions .

Table 31. Current consumption in Run mode on LDO, Coremark code with data processing running from flash memory, ICACHE ON in 1-way, prefetch ON

The current consumption from SRAM is similar.

Symbol	Parameter	Conditions			Typ				Max at 1.71 V ≤ V_{DD} ≤ 3.6 V(1)				Unit
		Voltage scaling		f_{HCLK} (MHz)	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 1	96	4.60	5.00	6.15	7.80	6.0	7.1	11	17	mA
			Range 2	48	2.05	2.40	3.35	4.75	3.0	3.8	6.7	11	
				24	1.15	1.45	2.45	3.85	2.0	2.8	5.7	10	
				12	0.68	1.00	2.00	3.40	1.5	2.3	5.2	9.5	
				6	0.45	0.79	1.75	3.15	1.2	2.1	4.9	9.2	
				3	0.34	0.68	1.65	3.05	1.1	1.9	4.8	9.1	
		$f_{HCLK} = f_{HSI}$, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 2	16	0.995	1.35	2.3	3.7	1.8	2.7	5.5	9.8	
		$f_{HCLK} = f_{HSE}$ bypass mode, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 1	96	4.85	5.25	6.4	8.1	6.3	7.4	11	17	
			Range 2	48	2.2	2.55	3.5	4.9	3.1	4.0	6.8	12	
				32	1.55	1.9	2.85	4.3	2.4	3.3	6.1	11	
				24	1.2	1.55	2.55	3.95	2.0	2.9	5.8	11	
				12	0.755	1.1	2.05	3.45	1.6	2.4	5.2	9.5	
				6	0.51	0.845	1.8	3.2	1.3	2.1	5.0	9.3	
				3	0.385	0.725	1.7	3.1	1.1	2.0	4.9	9.2	
				1	0.305	0.645	1.6	3	1.1	1.9	4.8	9	
				0.4	0.28	0.62	1.6	3	1.0	1.9	4.8	9	

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Symbol	Parameter	Conditions			Typ				Max at 1.71 V ≤ V_{DD} ≤ 3.6 V(1)				Unit
		Voltage scaling		f_{HCLK} (MHz)	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} bypass mode, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 2	0.1	0.27	0.605	1.55	3	1.0	1.9	4.7	9	mA

1. *Evaluated by characterization. Not tested in production.*

Table 32. Current consumption in Run mode on SMPS, Coremark code with data processing running from flash memory, ICACHE ON in 1-way, prefetch ON

The current consumption from SRAM is similar.

Symbol	Parameter	Conditions			Typ at V_{DD} = 1.8 V				Max at 1.71 V ≤ V_{DD} ≤ 3.6 V(1) (2)				Unit
		Voltage scaling		f_{HCLK} (MHz)	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{MSI}, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 1	96	2.50	2.75	3.45	4.4	3.9	4.7	6.8	11	mA
			Range 2	48	1	1.2	1.75	2.5	1.6	2.1	3.8	6.1	
				24	0.56	0.75	1.3	2.05	1.1	1.6	3.3	5.6	
				12	0.35	0.54	1.05	1.85	0.8	1.3	3.0	5.4	
				6	0.24	0.43	0.96	1.7	0.64	1.2	2.9	5.2	
				3	0.19	0.37	0.9	1.65	0.57	1.1	2.8	5.2	
		f_{HCLK} = f_{HSI}, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 2	16	0.58	0.77	1.3	2.1	1.1	1.6	3.3	5.7	
		f_{HCLK} = f_{HSE} bypass mode, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 1	96	2.65	2.9	3.6	4.55	3.7	4.4	6.6	10	
			Range 2	48	1.05	1.25	1.8	2.55	1.6	2.1	3.8	6.2	
				32	0.76	0.94	1.45	2.25	1.3	1.8	3.4	5.9	
				24	0.6	0.78	1.3	2.1	1.1	1.6	3.3	5.7	
				12	0.37	0.55	1.1	1.85	0.78	1.3	3.0	5.4	
				6	0.25	0.44	0.97	1.75	0.65	1.2	2.9	5.3	
				3	0.19	0.38	0.91	1.7	0.58	1.1	2.8	5.2	
				1	0.16	0.34	0.87	1.65	0.54	1.1	2.8	5.2	
				0.4	0.14	0.33	0.86	1.6	0.52	1.1	2.7	5.1	
				0.1	0.14	0.32	0.85	1.6	0.52	1.1	2.7	5.1	

1. *Evaluated by characterization. Not tested in production.*
2. *The maximum value is at V_{DD} = 1.71 V in Run mode on SMPS.*

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Table 33. Current consumption in Run mode on SMPS, Coremark code with data processing running from flash memory, ICACHE ON in 1-way, prefetch ON V_{DD} = 3 V

The current consumption from SRAM is similar.

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ at V_{DD} = 3.0 V				Max at V_{DD} = 3.0 V(1)				Unit
		Voltage scaling			25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disable, flash bank 2 in power down, all SRAMs enabled	Range 1	96	1.65	1.85	2.3	3	2.6	3.1	4.6	7	mA
			Range 2	48	0.66	0.8	1.2	1.75	1.1	1.5	2.6	4.3	
				24	0.38	0.51	0.89	1.45	0.7	1.2	2.3	3.9	
				12	0.25	0.38	0.76	1.3	0.55	0.97	2.1	3.8	
				6	0.18	0.31	0.69	1.25	0.47	0.9	2.1	3.7	
				3	0.15	0.28	0.66	1.2	0.44	0.86	2	3.6	
		$f_{HCLK} = f_{HSI}$, all peripherals disable, flash bank 2 in power down, all SRAMs enabled	Range 2	16	0.45	0.59	0.97	1.55	0.78	1.2	2.4	4	
		$f_{HCLK} = f_{HSE}$ bypass mode, all peripherals disable, flash bank 2 in power down, all SRAMs enabled	Range 1	96	1.85	2.05	2.5	3.2	2.5	3.2	4.8	7.2	
			Range 2	48	0.75	0.91	1.3	1.85	1.2	1.6	2.7	4.4	
				32	0.54	0.71	1.1	1.65	0.87	1.4	2.5	4.1	
				24	0.43	0.6	0.97	1.55	0.75	1.3	2.4	4	
				12	0.27	0.45	0.82	1.4	0.57	1.1	2.2	3.9	
				6	0.19	0.37	0.75	1.3	0.48	0.96	2.1	3.8	
				3	0.15	0.33	0.71	1.25	0.45	0.91	2.1	3.7	
				1	0.12	0.3	0.68	1.25	0.41	0.89	2.1	3.7	
				0.4	0.12	0.3	0.67	1.25	0.41	0.88	2.1	3.7	
				0.1	0.11	0.29	0.67	1.2	0.4	0.87	2	3.6	

1. *Evaluated by characterization. Not tested in production.*

Table 34. Typical current consumption in Run modes on LDO, with different codes running from flash memory, ICACHE ON (1-way), prefetch ON

The current consumption from SRAM is similar.

Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
		Voltage scaling		Code	1.8 V	3 V	3.3 V		1.8 V	3 V	3.3 V	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ = 48 MHz, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 2	Reduced code	2.15	2.15	2.15	mA	44.8	44.8	44.8	µA/MHz
				Coremark	2.05	2.05	2.05		42.7	42.7	42.7	
				SecureMark	2.25	2.25	2.25		46.9	46.9	46.9	
				Dhrystone 2.1	2.35	2.35	2.35		49	49	49	
				While(1)	1.5	1.5	1.5		31.3	31.3	31.3	
				Fibonacci	1.8	1.8	1.8		37.5	37.5	37.5	

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Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
		Voltage scaling		Code	1.8 V	3 V	3.3 V		1.8 V	3 V	3.3 V	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ = 96 MHz, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 1	Reduced code	4.75	4.75	4.75	mA	49.5	49.5	49.5	µA/ MHz
				Coremark	4.55	4.55	4.60		47.4	47.4	47.9	
				SecureMark	4.95	4.95	4.95		51.6	51.6	51.6	
				Dhrystone 2.1	5.15	5.15	5.15		53.6	53.6	53.6	
				While(1)	3.4	3.4	3.4		35.4	35.4	35.4	
				Fibonacci	4	3.95	4		41.7	41.1	41.7	
		$f_{HCLK} = f_{MSI}$ = 24 MHz, ePOD booster disabled, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 2	Reduced code	1.15	1.15	1.2	mA	47.9	47.9	50	µA/ MHz
				Coremark	1.15	1.15	1.15		47.9	47.9	47.9	
				SecureMark	1.2	1.2	1.2		50	50	50	
				Dhrystone 2.1	1.25	1.25	1.25		52.1	52.1	52.1	
				While(1)	0.85	0.84	0.85		35.2	35.0	35.2	
				Fibonacci	0.99	0.99	1		41.3	41.3	41.5	

Table 35. Typical current consumption in Run modes on LDO, with different codes running from flash memory in low-power mode, ICACHE1 way, prefetch ON

The current consumption from SRAM is similar.

Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
		Voltage scaling		Code	1.8 V	3 V	3.3 V		1.8 V	3 V	3.3 V	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ = 24 MHz, ePOD booster disabled, all peripherals disable, flash memory bank 2 in powered down, SRAM2 enabled, SRAM1 in power down	Range 2	Reduced code	1.15	1.15	1.15	mA	47.9	47.9	47.9	µA/ MHz
				Coremark	1.1	1.1	1.1		45.8	45.8	45.8	
				SecureMark	1.2	1.2	1.2		50	50	50	
				Dhrystone 2.1	1.25	1.25	1.25		52.1	52.1	52.1	
				While(1)	0.81	0.81	0.81		33.8	33.8	33.8	
				Fibonacci	0.96	0.96	0.96		40	40	40	

Table 36. Typical current consumption in Run modes on SMPS, with different codes running from flash memory, ICACHE ON (1-way), prefetch ON

The current consumption from SRAM is similar.

Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
		Voltage scaling		Code	1.8 V	3 V	3.3 V		1.8 V	3 V	3.3 V	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ = 48 MHz, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 2	Reduced code	1.05	0.70	0.66	mA	21.9	14.6	13.6	µA/ MHz
				Coremark	1	0.66	0.62		20.8	13.8	12.9	
				SecureMark	1.10	0.72	0.68		22.9	15	14.1	
				Dhrystone 2.1	1.15	0.75	0.71		24.0	15.6	14.7	
				While(1)	0.74	0.49	0.46		15.4	10.1	9.5	
				Fibonacci	0.88	0.57	0.54		18.2	11.9	11.1	

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Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
		Voltage scaling		Code	1.8 V	3 V	3.3 V		1.8 V	3 V	3.3 V	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ = 96 MHz, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 1	Reduced code	2.65	1.75	1.65	mA	27.6	18.2	17.2	µA/ MHz
				Coremark	2.50	1.65	1.55		26.04	17.2	16.1	
				SecureMark	2.75	1.80	1.70		28.6	18.8	17.7	
				Dhrystone 2.1	2.85	1.85	1.75		29.7	19.3	18.2	
				While(1)	1.90	1.25	1.2		19.8	13	12.5	
				Fibonacci	2.20	1.45	1.35		22.9	15.1	14.1	
		$f_{HCLK} = f_{MSI}$ = 24 MHz,ePOD booster disabled, all peripherals disable, flash memory bank 2 in powered down, all SRAMs enabled	Range 2	Reduced code	0.59	0.40	0.38	mA	24.6	16.5	15.6	µA/ MHz
				Coremark	0.57	0.38	0.36		23.5	15.8	14.8	
				SecureMark	0.61	0.41	0.39		25.4	17.1	16.04	
				Dhrystone 2.1	0.64	0.43	0.4		26.5	17.7	16.7	
				While(1)	0.43	0.29	0.28		17.7	12.1	11.5	
				Fibonacci	0.50	0.34	0.32		20.6	13.96	13.1	

Table 37. Typical current consumption in Run modes on SMPS, with different codes running from flash memory in low-power mode, ICACHE1 way, prefetch ON

The current consumption from SRAM is similar.

Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
		Voltage scaling	Code		1.8 V	3 V	3.3 V		1.8 V	3 V	3.3 V	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ = 24 MHz, ePOD booster disabled, all peripherals disable,flash bank 2 in power down, SRAM2 enabled, SRAM1 in power down	Range 2	Reduced Code	0.56	0.37	0.35	mA	23.3	15.4	14.4	µA/MHz
				Coremark	0.54	0.35	0.33		22.3	14.6	13.8	
				SecureMark	0.58	0.38	0.36		24.2	15.8	15	
				Dhrystone 2.1	0.61	0.40	0.38		25.2	16.7	15.6	
				While(1)	0.40	0.26	0.25		16.7	10.8	10.2	
				Fibonacci	0.47	0.31	0.29		19.4	12.7	11.9	

Table 38. Current consumption in Sleep mode on LDO, flash memory in power down

Symbol	Parameter	Conditions			Typ				Max at 1.71 V ≤ V_{DD} 3.6 V(1)				Unit
		Voltage scaling		f_{HCLK} (MHz)	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Sleep)	Supply current in Sleep mode	$f_{HCLK} = f_{MSI}$, all peripherals disable, all SRAMs enabled	Range 1	96	1.5	1.9	3.1	4.7	2.5	3.6	7.3	13.0	mA
			Range 2	48	0.71	1.05	2	3.4	1.5	2.3	5.2	9.4	
				24	0.44	0.78	1.75	3.15	1.2	2.0	4.9	9.1	
				12	0.33	0.66	1.65	3	0.99	1.9	4.8	9.0	
				6	0.27	0.6	1.55	2.95	0.92	1.8	4.7	8.9	
				3	0.24	0.57	1.55	2.95	0.89	1.8	4.7	8.9	

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Symbol	Parameter	Conditions			Typ				Max at 1.71 V ≤ V_{DD} 3.6 V(1)				Unit
		Voltage scaling		f_{HCLK} (MHz)	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Sleep)	Supply current in Sleep mode	f_{HCLK} = f_{HSI}, all peripherals disable, all SRAMs enabled	Range 2	16	0.53	0.87	1.85	3.25	1.3	2.1	5.0	9.2	mA
		f_{HCLK} = f_{HSE} bypass mode, all peripherals disable, all SRAMs enabled	Range 1	96	1.75	2.2	3.35	5	2.8	3.9	7.7	13	
			Range 2	48	0.84	1.2	2.15	3.55	1.6	2.5	5.4	9.6	
				32	0.66	0.99	1.95	3.35	1.4	2.3	5.1	9.3	
				24	0.54	0.87	1.85	3.25	1.3	2.1	5.0	9.2	
				12	0.40	0.73	1.7	3.1	1.1	2.0	4.9	9.1	
				6	0.32	0.66	1.6	3	0.98	1.9	4.8	9	
				3	0.29	0.62	1.6	3	0.94	1.8	4.8	9	
				1	0.26	0.6	1.55	2.95	0.92	1.8	4.7	8.9	
				0.4	0.25	0.59	1.55	2.95	0.91	1.8	4.7	8.9	
				0.1	0.25	0.59	1.55	2.95	0.91	1.8	4.7	8.9	

1. *Evaluated by characterization. Not tested in production.*

Table 39. Current consumption in Sleep mode on SMPS, flash memory in power down

Symbol	Parameter	Conditions			Typ at V_{DD} = 1.8 V				Max at 1.71 V ≤ V_{DD} 3.6 V(1)(2)				Unit
		Voltage scaling		f_{HCLK} (MHz)	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Sleep)	Supply current in Sleep mode	f_{HCLK} = f_{MSI}, all peripherals disable, all SRAMs enabled	Range 1	96	0.87	1.10	1.80	2.75	1.50	2.30	4.80	8.30	mA
			Range 2	48	0.36	0.54	1.05	1.85	0.72	1.30	2.90	5.40	
				24	0.23	0.41	0.93	1.70	0.57	1.10	2.80	5.20	
				12	0.17	0.35	0.88	1.65	0.50	1.00	2.70	5.20	
				6	0.14	0.33	0.85	1.60	0.47	0.97	2.70	5.10	
				3	0.13	0.31	0.83	1.60	0.45	0.95	2.70	5.10	
		f_{HCLK} = f_{HSI}, all peripherals disable, all SRAMs enabled	Range 2	16	0.35	0.54	1.05	1.85	0.71	1.30	2.90	5.40	
		f_{HCLK} = f_{HSE} bypass mode, all peripherals disable, all SRAMs enabled	Range 1	96	0.98	1.20	1.90	2.85	1.70	2.40	4.60	8.00	
			Range 2	48	0.40	0.58	1.10	1.85	0.77	1.30	3.00	5.40	
				32	0.31	0.49	1.00	1.80	0.67	1.20	2.80	5.30	
				24	0.26	0.44	0.96	1.70	0.60	1.10	2.80	5.20	
				12	0.19	0.37	0.89	1.65	0.52	1.10	2.70	5.20	
				6	0.15	0.33	0.86	1.60	0.48	0.98	2.70	5.10	
				3	0.14	0.32	0.84	1.60	0.46	0.96	2.70	5.10	
				1	0.12	0.31	0.83	1.60	0.45	0.95	2.60	5.10	
				0.4	0.12	0.30	0.82	1.60	0.44	0.94	2.60	5.10	
				0.1	0.12	0.30	0.82	1.60	0.44	0.94	2.60	5.10	

1. *Evaluated by characterization. Not tested in production.*
2. *The maximum value is at V_{DD} = 1.71 V in Sleep mode on SMPS..*

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Table 40. Current consumption in Sleep mode on SMPS, flash memory in power down, V_{DD} = 3.0 V

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ at V_{DD} = 3.0 V				Max at V_{DD} = 3.0 V(1)				Unit
		Voltage scaling			25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Sleep)	Supply current in Sleep mode	f_{HCLK} = f_{MSI}, all peripherals disable, all SRAMs enabled	Range 1	96	0.63	0.80	1.25	1.95	1.10	1.70	3.40	5.80	mA
			Range 2	48	0.24	0.37	0.75	1.30	0.49	0.92	2.10	3.80	
				24	0.16	0.29	0.67	1.20	0.41	0.84	2.00	3.60	
				12	0.13	0.26	0.63	1.20	0.37	0.80	2.00	3.60	
				6	0.11	0.24	0.62	1.15	0.35	0.78	2.00	3.60	
				3	0.10	0.23	0.61	1.15	0.34	0.77	1.90	3.60	
		f_{HCLK} = f_{HSI}, all peripherals disable, all SRAMs enabled	Range 2	16	0.30	0.43	0.81	1.35	0.55	0.99	2.20	3.80	
		f_{HCLK} = f_{HSE} bypass mode, all peripherals disable, all SRAMs enabled	Range 1	96	0.82	0.99	1.45	2.15	1.30	2.00	3.60	6.10	
			Range 2	48	0.30	0.49	0.86	1.40	0.56	1.10	2.20	3.90	
				32	0.24	0.42	0.80	1.35	0.49	0.98	2.10	3.80	
				24	0.20	0.37	0.75	1.30	0.45	0.92	2.10	3.80	
				12	0.15	0.33	0.70	1.25	0.40	0.88	2.00	3.70	
				6	0.12	0.30	0.67	1.20	0.36	0.84	2.00	3.60	
				3	0.11	0.28	0.66	1.20	0.35	0.83	2.00	3.60	
				1	0.10	0.27	0.65	1.20	0.33	0.81	2.00	3.60	
				0.4	0.09	0.27	0.65	1.20	0.33	0.81	2.00	3.60	
				0.1	0.09	0.27	0.65	1.20	0.33	0.81	2.00	3.60	

1. *Evaluated by characterization. Not tested in production.*

Table 41. SRAM1/SRAM2 current consumption in Run/Sleep modes with LDO and SMPS

Symbol	Parameter		Voltage scaling	f_{HCLK} (MHz)	Typ				Max				Unit
					25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (SRAM1)	LDO	SRAM1 supply current in Run/ Sleep mode (SRAM1PD = 1 vs. SRAM1PD = 0)	Range 2	24	0.02	0.06	0.18	0.35	0.08	0.18	0.53	1.10	mA
				48	0.02	0.06	0.18	0.35	0.08	0.19	0.54	1.10	
			Range 1	96	0.02	0.07	0.19	0.38	0.08	0.20	0.57	1.20	
I_{DD} (SRAM2)		SRAM2 supply current in Run/ Sleep mode (SRAM2PD = 1 vs. SRAM2PD = 0)	Range 2	24	0.01	0.02	0.07	0.14	0.03	0.07	0.22	0.42	mA
				48	0.01	0.02	0.07	0.14	0.03	0.07	0.22	0.42	
			Range 1	96	0.01	0.03	0.08	0.15	0.03	0.08	0.23	0.45	
I_{DD} (SRAM1)	SMPS V_{DD} = 3.0 V	SRAM1 supply current in Run/ Sleep mode (SRAM1PD = 1 vs. SRAM1PD = 0)	Range 2	24	0.02	0.05	0.14	0.27	0.07	0.15	0.41	0.80	mA
				48	0.02	0.05	0.14	0.27	0.07	0.15	0.41	0.80	
			Range 1	96	0.02	0.05	0.14	0.28	0.07	0.15	0.42	0.83	

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Symbol	Parameter		Voltage scaling	f_{HCLK} (MHz)	Typ				Max				Unit
					25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (SRAM2)	SMPS V_{DD} = 3.0 V	SRAM2 supply current in Run/ Sleep mode (SRAM2PD = 1 vs. SRAM2PD = 0)	Range 2	24	0.01	0.02	0.05	0.11	0.03	0.06	0.16	0.32	mA
				48	0.01	0.02	0.05	0.10	0.03	0.06	0.16	0.30	
			Range 1	96	0.01	0.02	0.05	0.11	0.03	0.06	0.17	0.33	
I_{DD} (SRAM1)	SMPS[1]	SRAM1 supply current in Run/ Sleep mode (SRAM1PD = 1 vs. SRAM1PD = 0)	Range 2	24	0.03	0.08	0.23	0.44	0.12	0.25	0.72	1.40	mA
				48	0.03	0.08	0.23	0.44	0.12	0.26	0.72	1.40	
			Range 1	96	0.03	0.08	0.23	0.46	0.13	0.27	0.74	1.50	
I_{DD} (SRAM2)		SRAM2 supply current in Run/ Sleep mode (SRAM2PD = 1 vs. SRAM2PD = 0)[1]	Range 2	24	0.01	0.03	0.09	0.18	0.05	0.10	0.28	0.56	mA
				48	0.01	0.03	0.09	0.17	0.05	0.10	0.28	0.53	
			Range 1	96	0.01	0.03	0.09	0.18	0.05	0.11	0.29	0.58	

1. *The typical value is measured at V_{DD} = 1.8 V. The maximum value is for 1.71 V ≤ VDD ≤ 3.6 V and is at VDD = 1.71 V in Run/Sleep mode on SMPS.*

Table 42. Flash banks static power consumption, when supplied by LDO/SMPS

Symbol	Parameter	Typ				Max				Unit
		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Flash_Bank1)[1]	Flash bank 1 static consumption in normal mode (PD1 = 1 vs. PD1 = 0)	18	19	21	25	25	26	29	35	µA
I_{DD} (Flash_Bank2)[1]	Flash bank 2 static consumption in normal mode (PD2 = 1 vs. PD2 = 0)	18	18	20	23	25	25	28	32	
I_{DD} (Flash_Bank_LPM)[2]	One Flash bank additional static consumption in normal mode versus low-power mode (LPM = 0 vs. LPM = 1)	10	11	11	15	14	15	15	21	

1. *When flash memory is in power down in Sleep mode (SLEEP_PD=1), Bank 1 and Bank 2 are in power down.*
2. *If no bank is in power-down, the flash memory additional static consumption in normal mode versus low-power mode is 2 x IDD(Flash_Bank_LPM)*

Table 43. Current consumption in Stop 0 mode on SMPS

Symbol	Parameter	Conditions	Typ				Max[1]				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode, regulator in Range 2, RTC disabled, 8 KB SRAM2 + ICACHE retained	1.8	81.5	220	615	1200	300	660	1900	3600	µA
		2.4	68	175	480	910	250	530	1500	2800	
		3	60.5	150	400	760	220	450	1200	2300	
		3.3	59	140	375	710	220	420	1200	2200	
		3.6	57	135	355	670	210	410	1100	2100	
	Supply current in Stop 0 mode, regulator in Range 2, RTC disabled, all SRAMs retained	1.8	89	235	645	1250	330	710	2000	3800	
		2.4	75	185	510	970	270	560	1600	3000	
		3	68	160	430	820	250	480	1300	2500	
		3.3	66	155	405	770	240	470	1300	2400	

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Symbol	Parameter	Conditions	Typ				Max(1)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode, regulator in Range 2, RTC disabled, all SRAMs retained	3.6	64	145	385	730	230	440	1200	2200	µA

1. *Evaluated by characterization. Not tested in production.*

Table 44. Current consumption in Stop 0 mode on LDO

Symbol	Parameter	Conditions	Typ				Max(1)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode, regulator in Range 2, RTC disabled, 8 KB SRAM2 + ICACHE retained	1.8	165	455	1250	2400	600	1400	3800	7200	µA
		2.4	165	455	1250	2400	600	1400	3800	7200	
		3	165	455	1250	2400	600	1400	3800	7200	
		3.3	165	455	1250	2450	600	1400	3800	7400	
		3.6	165	455	1250	2450	600	1400	3800	7400	
	Supply current in Stop 0 mode, regulator in Range 2, RTC disabled, all SRAMs retained	1.8	175	465	1300	2450	640	1400	3900	7400	
		2.4	175	465	1300	2500	640	1400	3900	7500	
		3	175	465	1300	2500	640	1400	3900	7500	
		3.3	175	465	1300	2500	640	1400	3900	7500	
		3.6	175	465	1300	2500	640	1400	3900	7500	

1. *Evaluated by characterization. Not tested in production.*

Table 45. Current consumption in Stop 1 mode on LDO

Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled, 8 KB SRAM2 + ICACHE retained	1.8	145	430	1250	2400	530	1300	3800	7200	µA
		2.4	145	435	1250	2450	530	1400	3800	7400	
		3	145	435	1250	2450	530	1400	3800	7400	
		3.3	145	435	1250	2450	530	1400	3800	7400	
		3.6	145	435	1250	2450	530	1400	3800	7400	
	Supply current in Stop 1 mode, RTC disabled, all SRAMs retained	1.8	150	445	1300	2500	550	1400	3900	7500	
		2.4	150	445	1300	2500	550	1400	3900	7500	
		3	150	445	1300	2500	550	1400	3900	7500	
		3.3	150	445	1300	2500	550	1400	3900	7500	
		3.6	150	450	1300	2500	550	1400	3900	7500	
I_{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC(1) clocked by LSI 32 kHz, 8 KB SRAM2 + ICACHE retained	1.8	145	430	1250	2400	530	1300	3800	7200	
		2.4	145	435	1250	2450	530	1400	3800	7400	
		3	145	435	1250	2450	530	1400	3800	7400	
		3.3	145	435	1250	2450	530	1400	3800	7400	
		3.6	145	435	1250	2450	530	1400	3800	7400	

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Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC(1) clocked by LSE bypassed at 32768 Hz, 8 KB SRAM2 + ICACHE retained	1.8	145	430	1250	2400	530	1300	3800	7200	µA
		2.4	145	435	1250	2450	530	1400	3800	7400	
		3	145	435	1250	2450	530	1400	3800	7400	
		3.3	145	435	1250	2450	530	1400	3800	7400	
		3.6	145	435	1250	2450	530	1400	3800	7400	
	Supply current in Stop 1 mode, RTC(1) clocked by LSE quartz in low-drive mode, RCC_BDCR.LSESYSEN = 0, 8 KB SRAM2 + ICACHE retained	1.8	140	425	1250	2400	-	-	-	-	
		2.4	140	425	1250	2400	-	-	-	-	
		3	140	430	1250	2400	-	-	-	-	
		3.3	140	430	1250	2400	-	-	-	-	
		3.6	140	430	1250	2450	-	-	-	-	

1. *RTC with default configuration except RTC_CALR.LPCAL = 1*
2. *Evaluated by characterization. Not tested in production.*

Table 46. Current consumption during wake-up from Stop 1 mode on LDO

Symbol	Parameter	Conditions		Typ	Unit
		V_{DD}		25°C	
Q_{DD} (wake-up from Stop 1)	Electrical charge consumed during wake-up from Stop 1 mode	Wake-up clock is MSI 48 MHz	3	12	nAs
		Wake-up clock is HSI 16 MHz		12	
		Wake-up clock is MSI 3 MHz		18	

Table 47. Current consumption in Stop 1 mode on SMPS

Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled, 8 KB SRAM2 + ICACHE retained	1.8	82	220	615	1200	300	660	1900	3600	µA
		2.4	68	175	480	910	250	530	1500	2800	
		3	61	150	400	760	220	450	1200	2300	
		3.3	58	140	375	710	210	420	1200	2200	
		3.6	57	135	355	670	210	410	1100	2100	
	Supply current in Stop 1 mode, RTC disabled, all SRAMs retained	1.8	89	230	645	1250	320	690	2000	3800	
		2.4	75	185	505	970	280	560	1600	3000	
		3	68	160	430	820	250	480	1300	2500	
		3.3	65	150	405	770	240	450	1300	2400	
		3.6	64	145	385	725	230	440	1200	2200	
I_{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC(1) clocked by LSI 32 kHz, 8 KB SRAM2 + ICACHE retained	1.8	82	220	615	1200	300	660	1900	3600	
		2.4	69	175	480	910	250	530	1500	2800	
		3	61	150	400	760	220	450	1200	2300	
		3.3	59	140	375	710	220	420	1200	2200	
		3.6	57	135	355	670	210	410	1100	2100	

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Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC(1) clocked by LSE bypassed at 32768 Hz, 8 KB SRAM2 + ICACHE retained	1.8	82	220	615	1200	300	660	1900	3600	µA
		2.4	69	175	480	910	250	530	1500	2800	
		3	61	150	400	760	220	450	1200	2300	
		3.3	59	140	375	710	220	420	1200	2200	
		3.6	57	135	355	670	210	410	1100	2100	
	Supply current in Stop 1 mode, RTC(1) clocked by LSE quartz in low-drive mode, RCC_BDCR.LSESYSEN=0, 8 KB SRAM2 + ICACHE retained	1.8	81	215	605	1100	-	-	-	-	
		2.4	68	170	470	900	-	-	-	-	
		3	60	145	395	755	-	-	-	-	
		3.3	58	140	370	705	-	-	-	-	
		3.6	57	135	350	665	-	-	-	-	

1. *RTC with default configuration but RTC_CALR.LPCAL = 1*
2. *Evaluated by characterization. Not tested in production.*

Table 48. Current consumption during wake-up from Stop 1 mode on SMPS

Symbol	Parameter	Conditions		Typ	Unit
		V_{DD}		25°C	
Q_{DD} (wake-up from Stop 1)	Electrical charge consumed during wake-up from Stop 1 mode	Wake-up clock is MSI 48 MHz	3	6	nAs
		Wake-up clock is HSI 16 MHz		6	
		Wake-up clock is MSI 3 MHz		10	

Table 49. Current consumption in Stop 2 mode on LDO

Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled, 8 KB SRAM2 + ICACHE retained	1.8	13	41.5	125	255	47	130	380	770	µA
		2.4	13	42.5	130	255	47	130	390	770	
		3	13	42.5	130	260	47	130	390	780	
		3.3	13	43	130	260	47	130	390	780	
		3.6	13.5	44	130	260	49	140	390	780	
	Supply current in Stop 2 mode, RTC disabled, all SRAMs retained	1.8	15.5	49.5	155	315	56	150	470	950	
		2.4	15.5	50	155	320	56	150	470	960	
		3	15.5	50.5	155	320	56	160	470	960	
		3.3	15.5	51.0	160	320	56	160	480	960	
		3.6	16	51.5	160	325	58	160	480	980	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC(1) clocked by LSI 32 kHz, 8 KB SRAM2 + ICACHE retained	1.8	13	42	125	255	47	130	380	770	
		2.4	13	43	130	255	47	130	390	770	
		3	13.5	43	130	260	49	130	390	780	
		3.3	13.5	43.5	130	260	49	140	390	780	
		3.6	14	44.5	135	260	51	140	410	780	

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Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC(1) clocked by LSI 250 Hz, 8 KB SRAM2 + ICACHE retained	1.8	13	41.5	125	255	47	130	380	770	µA
		2.4	13	42.5	130	255	47	130	390	770	
		3	13	43	130	260	47	130	390	780	
		3.3	13	43	130	260	47	130	390	780	
		3.6	13.5	44	130	260	49	140	390	780	
	Supply current in Stop 2 mode, RTC(1) clocked by LSE bypassed at 32768 Hz, 8 KB SRAM2 + ICACHE retained	1.8	13.0	42	125	255	47	130	380	770	
		2.4	13	43	130	255	47	130	390	770	
		3	13	43	130	260	47	130	390	780	
		3.3	13.5	43.5	130	260	49	140	390	780	
		3.6	14.0	44	135	260	51	140	410	780	
	Supply current in Stop 2 mode, RTC(1) clocked by LSE quartz in low-drive mode, RCC_BDCR.LSESYSEN = 0, 8 KB SRAM2 + ICACHE retained	1.8	13	41.5	125	250	-	-	-	-	
		2.4	13	42	130	255	-	-	-	-	
		3	13	42.5	130	255	-	-	-	-	
		3.3	13	43	130	255	-	-	-	-	
		3.6	13.5	44	130	260	-	-	-	-	
	Supply current in Stop 2 mode, RTC(1) clocked by LSE quartz in low-drive mode, RCC_BDCR.LSESYSEN = 1, 8 KB SRAM2 + ICACHE retained	1.8	13	41.5	125	250	-	-	-	-	
		2.4	13	42.5	130	255	-	-	-	-	
		3	13	42.5	130	255	-	-	-	-	
		3.3	13.5	43	130	255	-	-	-	-	
		3.6	14	44	130	260	-	-	-	-	

1. *RTC with default configuration but RTC_CALR.LPCAL = 1*
2. *Evaluated by characterization. Not tested in production.*

Table 50. SRAM static power consumption in Stop 2 when supplied by LDO

Symbol	Parameter	Typ				Max(3)				Unit
		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (SRAM1_16kB)(1)	SRAM1 16-Kbyte page x (x = 1, or 2) static consumption (SRAM1PDSx = 1 vs. SRAM1PDSx = 0)	0.21	0.41	1.65	3.95	0.74	1.30	5	12	µA
I_{DD} (SRAM1_32kB)(1)	SRAM1 32-Kbyte page x (x = 3, ..., 6, or 7) static consumption (SRAM1PDSx = 1 vs. SRAM1PDSx = 0)	0.38	0.86	3.25	7.40	1.40	2.60	9.8	23	
I_{DD} (SRAM2_32kB)(2)	SRAM2 32-Kbyte page 1 static consumption (SRAM2PDS1 = 1 vs. SRAM2PDS1 = 0)	0.47	1.20	4.25	9.50	1.70	3.60	13	29	
I_{DD} (SRAM2_24kB)(2)	SRAM2 24-Kbyte page 2 static consumption (SRAM2PDS2 = 1 vs. SRAM2PDS2 = 0)	0.35	0.85	3.25	7.2	1.30	2.60	10	22	
I_{DD} (SRAM2_8kB)(2)	SRAM2 8-Kbyte page 3 static consumption (SRAM2PDS3 = 1 vs. SRAM2PDS3 = 0)	0.18	0.25	1.10	2.37	0.65	0.75	3.3	7.2	

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Symbol	Parameter	Typ				Max(3)				Unit
		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (ICRAM)	ICACHE SRAM static consumption (ICRAMPDS = 1 vs. ICRAMPDS = 0)	0.13	0.32	1.30	2.8	0.46	0.96	3.9	8.4	µA
I_{DD} (PRAM)	FDCAN and USB SRAM static consumption (PRAMPDS = 1 vs. PRAMPDS = 0)	0.11	0.16	0.44	0.81	0.40	0.48	1.4	2.5	
I_{DD} (PKARAM)	PKA SRAM static consumption (PKARAMPDS = 1 vs. PKARAMPDS = 0)	0.11	0.18	0.68	1.25	0.38	0.54	2.1	3.8	

1. *SRAM1 total consumption is 2 x I_{DD}(SRAM1_16kB) + 5 × I_{DD}(SRAM1_32kB).*
2. *SRAM2 total consumption is I_{DD}(SRAM2_32kB) + I_{DD}(SRAM2_24kB) + IDD(SRAM2_8kB).*
3. *Evaluated by characterization. Not tested in production.*

Table 51. Current consumption during wake-up from Stop 2 mode on LDO

Symbol	Parameter	Conditions		Typ	Unit
		V_{DD}		25°C	
Q_{DD} (wake-up from Stop 2)	Electrical charge consumed during wake-up from Stop 2 mode	Wake-up clock is MSI 48 MHz	3.0	12	nAs
		Wake-up clock is HSI 16 MHz		12	
		Wake-up clock is MSI 3 MHz		18	

Table 52. Current consumption in Stop 2 mode on SMPS

Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled, 8 KB SRAM2 + ICACHE retained	1.8	6.2	20	61.5	125	23	60	190	380	µA
		2.4	4.7	15.5	47.5	96.5	17	47	150	290	
		3	4.0	13	40	81.0	15	39	120	250	
		3.3	3.8	12.5	37.5	77	14	38	120	240	
		3.6	4.1	12	36.5	74.5	15	36	110	230	
	Supply current in Stop 2 mode, RTC disabled, all SRAMs retained	1.8	7.5	23.5	74.5	155	28	71	230	470	
		2.4	5.7	18	57	120	21	54	180	360	
		3	4.8	15	47.5	99.5	18	45	150	300	
		3.3	4.6	14.5	45	93.5	17	44	140	290	
		3.6	4.7	14	43.5	90	17	42	140	270	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC(1) clocked by LSI 32 kHz, 8 KB SRAM2 + ICACHE retained	1.8	6.5	20.5	62	125	24	62	190	380	
		2.4	5.1	16	48	97	19	48	150	300	
		3	4.4	13.5	40.5	81.5	16	41	130	250	
		3.3	4.3	13	38.5	77.5	16	39	120	240	
		3.6	4.6	13	37	75	17	39	120	230	
	Supply current in Stop 2 mode, RTC(1) clocked by LSI 250 Hz, 8 KB SRAM2 + ICACHE retained	1.8	6.3	20	61.5	125	23	60	190	380	
		2.4	4.8	15.5	48	96.5	18	47	150	290	
		3	4.1	13	40	81.5	15	39	120	250	
		3.3	4.0	12.5	38	77	15	38	120	240	
		3.6	4.2	12.5	37	74.5	15	38	120	230	

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Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC(1) clocked by LSE bypassed at 32768 Hz, 8 KB SRAM2 + ICACHE retained	1.8	6.4	20.5	62	125	23	62	190	380	µA
		2.4	5.0	15.5	48	97	18	47	150	300	
		3	4.2	13	40	81.5	16	39	120	250	
		3.3	4.2	12.5	38	77.5	15	38	120	240	
		3.6	4.4	12.5	37	75	16	38	120	230	
	Supply current in Stop 2 mode, RTC(1) clocked by LSE quartz in low-drive mode, RCC_BDCR.LSESYSEN = 0, 8 KB SRAM2 + ICACHE retained	1.8	6.4	20	61	125	-	-	-	-	
		2.4	5.0	15.5	47.5	95.5	-	-	-	-	
		3	4.3	13	39.5	81	-	-	-	-	
		3.3	4.1	12.5	38	76.5	-	-	-	-	
		3.6	4.4	12.5	37	74	-	-	-	-	
	Supply current in Stop 2 mode, RTC(1) clocked by LSE quartz in low-drive mode, RCC_BDCR.LSESYSEN = 1, 8 KB SRAM2 + ICACHE retained	1.8	6.5	20	61	125	-	-	-	-	
		2.4	5.1	15.5	47.5	96	-	-	-	-	
		3	4.4	13.5	40	81	-	-	-	-	
		3.3	4.3	12.5	38	77	-	-	-	-	
		3.6	4.5	12.5	37	74.5	-	-	-	-	

1. *RTC with default configuration but RTC_CALR.LPCAL = 1*
2. *Evaluated by characterization. Not tested in production.*

Table 53. SRAM static power consumption in Stop 2 when supplied by SMPS

Symbol	Parameter	Typ				Max(3)				Unit
		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (SRAM1_16kB)(1)	SRAM1 16-Kbyte page x (x = 1, or 2) static consumption (SRAM1PDSx = 1 vs. SRAM1PDSx = 0)	0.05	0.14	0.45	1.10	0.17	0.41	1.40	3.30	µA
I_{DD} (SRAM1_32kB)(1)	SRAM1 32-Kbyte page x (x = 3, ..., 6, or 7) static consumption (SRAM1PDSx = 1 vs. SRAM1PDSx = 0)	0.10	0.26	0.91	2.15	0.35	0.78	2.80	6.50	
I_{DD} (SRAM2_32kB)(2)	SRAM2 32-Kbyte page 1 static consumption (SRAM2PDS1 = 1 vs. SRAM2PDS1 = 0)	0.12	0.34	1.20	2.75	0.44	1.10	3.60	8.30	
I_{DD} (SRAM2_24kB)(2)	SRAM2 24-Kbyte page 2 static consumption (SRAM2PDS2 = 1 vs. SRAM2PDS2 = 0)	0.08	0.25	0.90	2.05	0.31	0.75	2.70	6.20	
I_{DD} (SRAM2_8kB)(2)	SRAM2 8-Kbyte page 3 static consumption (SRAM2PDS3 = 1 vs. SRAM2PDS3 = 0)	0.03	0.08	0.32	0.69	0.12	0.25	0.96	2.10	
I_{DD} (ICRAM)	ICACHE SRAM static consumption (ICRAMPDS = 1 vs. ICRAMPDS = 0)	0.03	0.09	0.32	0.78	0.13	0.27	0.96	2.40	

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Symbol	Parameter	Typ				Max(3)				Unit
		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (PRAM)	FDCAN and USB SRAM static consumption (PRAMPDS = 1 vs. PRAMPDS = 0)	0.03	0.05	0.13	0.30	0.12	0.15	0.40	0.90	µA
I_{DD} (PKARAM)	PKA SRAM static consumption (PKARAMPDS = 1 vs. PKARAMPDS = 0)	0.03	0.06	0.20	0.41	0.11	0.18	0.60	1.30	

1. *SRAM1 total consumption is 2 × IDD (SRAM1_16kB) + 5 × IDD (SRAM1_32kB).*
2. *SRAM2 total consumption is IDD (SRAM2_32kB) + IDD(SRAM2_24kB) + IDD (SRAM2_8kB).*
3. *Evaluated by characterization. Not tested in production.*

Table 54. Current consumption during wake-up from Stop 2 mode on SMPS

Symbol	Parameter	Conditions		Typ	Unit
		V_{DD}		25°C	
Q_{DD} (wake-up from Stop 2)	Electrical charge consumed during wake-up from Stop 2 mode	Wake-up clock is MSI 48 MHz	3	10	nAs
		Wake-up clock is HSI 16 MHz		10	
		Wake-up clock is MSI 3 MHz		15	

Table 55. Current consumption in Stop 3 mode on LDO

Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 3)	Supply current in Stop 3 mode, RTC disabled, 8 KB SRAM2 + ICACHE retained	1.8	4.65	16.0	51.0	110	17	48	160	330	µA
		2.4	4.70	16.0	51.5	110	17	48	160	330	
		3	4.80	16.0	52.0	110	18	48	160	330	
		3.3	4.90	16.5	53.0	110	18	50	160	330	
		3.6	5.30	17.0	54.5	115	20	51	170	350	
	Supply current in Stop 3 mode, RTC disabled, all SRAMs retained	1.8	7.00	23.0	76.5	165	26	69	230	500	
		2.4	7.05	23.0	77.0	170	26	69	240	510	
		3	7.15	23.5	77.5	170	26	71	240	510	
		3.3	7.30	23.5	79.0	170	27	71	240	510	
		3.6	7.75	24.5	80.0	170	28	74	240	510	
I_{DD} (Stop 3 with RTC)	Supply current in Stop 3 mode, RTC(1) clocked by LSI 32 kHz, 8 KB SRAM2 + ICACHE retained	1.8	4.95	16.0	51.5	110	18	48	160	330	
		2.4	5.05	16.5	52.0	110	19	50	160	330	
		3	5.25	16.5	52.5	110	19	50	160	330	
		3.3	5.45	17.0	53.5	110	20	51	170	330	
		3.6	5.90	18.0	55.0	115	22	54	170	350	

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Symbol	Parameter	Conditions	Typ				Max(2)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 3 with RTC)	Supply current in Stop 3 mode, RTC(1) clocked by LSI 250 Hz, 8 KB SRAM2 + ICACHE retained	1.8	4.80	16.0	51.0	110	18	48	160	330	µA
		2.4	4.80	16.0	51.5	110	18	48	160	330	
		3	4.90	16.5	52.5	110	18	50	160	330	
		3.3	5.05	16.5	53.0	110	19	50	160	330	
		3.6	5.65	17.5	54.5	115	21	53	170	350	
	Supply current in Stop 3 mode, RTC(1) clocked by LSE bypassed at 32768 Hz, 8 KB SRAM2 + ICACHE retained	1.8	4.90	16.0	51.0	110	18	48	160	330	
		2.4	5.00	16.5	52.0	110	19	50	160	330	
		3	5.10	16.5	52.5	110	19	50	160	330	
		3.3	5.25	17.0	53.5	110	19	51	170	330	
		3.6	5.70	17.5	54.5	115	21	53	170	350	
	Supply current in Stop 3 mode, RTC(1) clocked by LSE quartz in low-drive mode, RCC_BDCR.LSESYSEN = 0, 8 KB SRAM2 + ICACHE retained	1.8	4.95	16.0	50.5	105	-	-	-	-	
		2.4	5.05	16.0	51.5	110	-	-	-	-	
		3	5.10	16.5	52.5	110	-	-	-	-	
		3.3	5.30	17.0	53.5	110	-	-	-	-	
		3.6	5.75	17.5	54.5	115	-	-	-	-	
	Supply current in Stop 3 mode, RTC(1) clocked by LSE quartz in low-drive mode, RCC_BDCR.LSESYSEN = 1, 8 KB SRAM2 + ICACHE retained	1.8	5.00	16.0	51.0	105	-	-	-	-	
		2.4	5.05	16.5	51.5	110	-	-	-	-	
		3	5.20	16.5	52.5	110	-	-	-	-	
		3.3	5.40	17.0	53.5	110	-	-	-	-	
		3.6	5.90	17.5	55.0	115	-	-	-	-	

1. *RTC with default configuration except RTC_CALR.LPCAL = 1*
2. *Evaluated by characterization. Not tested in production.*

Table 56. SRAM static power consumption in Stop 3 when supplied by LDO

Symbol	Parameter	Typ				Max(3)				Unit
		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (SRAM1_16kB) (1)	SRAM1 16-Kbyte page x (x = 1, or 2) static consumption (SRAM1PDSx = 1 vs. SRAM1PDSx = 0)	0.11	0.41	1.55	3.40	0.40	1.30	4.70	11.00	µA
I_{DD} (SRAM1_32kB) (1)	SRAM1 32-Kbyte page x (x = 3, ..., 6, or 7) static consumption (SRAM1PDSx = 1 vs. SRAM1PDSx = 0)	0.26	0.83	3.05	6.85	0.94	2.50	9.20	21.00	
I_{DD} (SRAM2_32kB) (2)	SRAM2 32-Kbyte page 1 static consumption (SRAM2PDS1 = 1 vs. SRAM2PDS1 = 0)	0.31	0.93	3.95	8.90	1.20	2.80	12.00	27.00	
I_{DD} (SRAM2_24kB) (2)	SRAM2 24-Kbyte page 2 static consumption (SRAM2PDS2 = 1 vs. SRAM2PDS2 = 0)	0.22	0.78	3.05	6.70	0.80	2.40	9.20	21.00	

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Symbol	Parameter	Typ				Max(3)				Unit
		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (SRAM2_8kB)(2)	SRAM2 8-Kbyte page 3 static consumption (SRAM2PDS3 = 1 vs. SRAM2PDS3 = 0)	0.07	0.24	1.05	2.25	0.26	0.72	3.20	6.80	µA
I_{DD} (ICRAM)	ICACHE SRAM static consumption (ICRAMPDS = 1 vs. ICRAMPDS = 0)	0.10	0.27	1.20	2.45	0.35	0.81	3.60	7.40	
I_{DD} (PRAM)	FDCAN and USB SRAM static consumption (PRAMPDS = 1 vs. PRAMPDS = 0)	0.03	0.08	0.39	0.70	0.11	0.25	1.20	2.10	
I_{DD} (PKARAM)	PKA SRAM static consumption (PKARAMPDS = 1 vs. PKARAMPDS = 0)	0.06	0.10	0.55	1.50	0.21	0.30	1.70	4.50	

1. *SRAM1 total consumption is 2 × I_{DD}(SRAM1_16kB) + 5 × I_{DD}(SRAM1_32kB).*
2. *SRAM2 total consumption is I_{DD}(SRAM2_32kB) + I_{DD}(SRAM2_24kB) + I_{DD}(SRAM2_8kB).*
3. *Evaluated by characterization. Not tested in production.*

Table 57. Current consumption during wake-up from Stop 3 mode on LDO

Symbol	Parameter	Conditions		Typ	Unit
			V_{DD}	25°C	
Q_{DD} (wake-up from Stop 3)	Electrical charge consumed during wakeup from Stop 3 mode	Wake-up clock is MSI 48 MHz	3.0	150	nAs
		Wake-up clock is HSI 16 MHz		150	
		Wake-up clock is MSI 3 MHz		160	

Table 58. Current consumption in Stop 3 mode on SMPS

Symbol	Parameter	Conditions	Typ				Max(1)				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 3)	Supply current in Stop 3 mode, RTC disabled, 8 KB SRAM2 + ICACHE retained	1.8	2.25	7.5	24	52.5	8.2	23	72	160	µA
		2.4	1.75	5.8	19	41.5	6.4	18	57	130	
		3	1.55	5.0	16.5	36	5.6	15	50	110	
		3.3	1.60	5.0	16	35	5.8	15	48	110	
		3.6	1.95	5.4	16.5	35	7.1	17	50	110	
	Supply current in Stop 3 mode, RTC disabled, all SRAMs retained	1.8	3.30	10.5	35.5	79.5	12.0	32	110	240	
		2.4	2.55	8.2	27.5	62	9.2	25	83	190	
		3	2.20	7.0	23.5	52.5	8.0	21	71	160	
		3.3	2.20	6.8	22.5	50.5	8.0	21	68	160	
		3.6	2.50	7.1	22.5	49.5	9.1	22	68	150	
I_{DD} (Stop 3 with RTC)	Supply current in Stop 3 mode, RTC(2) clocked by LSI 32 kHz, 8 KB SRAM2 + ICACHE retained	1.8	2.55	7.8	24.5	52.5	9.2	24	74	160	
		2.4	2.15	6.2	19.5	42	7.8	19	59	130	
		3	2.00	5.5	17	36.5	7.3	17	51	110	
		3.3	2.10	5.5	16.5	35.5	7.6	17	50	110	
		3.6	2.50	6.0	17	35.5	9.1	18	51	110	

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Symbol	Parameter	Conditions	Typ				Max[1]				Unit
		V_{DD}	25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Stop 3 with RTC)	Supply current in Stop 3 mode, RTC[2] clocked by LSI 250 Hz, 8 KB SRAM2 + ICACHE retained	1.8	2.35	7.6	24.5	52.5	8.5	23	74	160	µA
		2.4	1.90	6.0	19.0	41.5	6.9	18	57	130	
		3	1.70	5.2	16.5	36	6.2	16	50	110	
		3.3	1.75	5.1	16.0	35.5	6.4	16	48	110	
		3.6	2.10	5.6	16.5	35.5	7.6	17	50	110	
	Supply current in Stop 3 mode, RTC[2] clocked by LSE bypassed at 32768 Hz, 8 KB SRAM2 + ICACHE retained	1.8	2.45	7.7	24.5	53	8.9	23	74	160	
		2.4	2.00	6.1	19.5	42	7.3	19	59	130	
		3	1.85	5.3	16.5	36.5	6.7	16	50	110	
		3.3	1.95	5.3	16.5	35.5	7.1	16	50	110	
		3.6	2.30	5.8	16.5	35.5	8.3	18	50	110	
	Supply current in Stop 3 mode, RTC[2] clocked by LSE quartz in low-drive mode, RCC_BDCR. LSESYSEN = 0, 8 KB SRAM2 + ICACHE retained	1.8	2.55	7.7	24.5	52.5	-	-	-	-	
		2.4	2.10	6.1	19.5	42	-	-	-	-	
		3	1.90	5.4	16.5	36.5	-	-	-	-	
		3.3	1.95	5.4	16.5	35.5	-	-	-	-	
		3.6	2.35	5.8	16.5	35.5	-	-	-	-	
	Supply current in Stop 3 mode, RTC[2] clocked by LSE quartz in low-drive mode, RCC_BDCR. LSESYSEN = 1, 8 KB SRAM2 + ICACHE retained	1.8	2.60	7.8	24.5	52.5	-	-	-	-	
		2.4	2.20	6.2	19.5	42	-	-	-	-	
		3	2.00	5.5	17.0	36.5	-	-	-	-	
		3.3	2.10	5.5	16.5	35.5	-	-	-	-	
		3.6	2.45	5.9	17.0	35.5	-	-	-	-	

1. *Evaluated by characterization. Not tested in production.*
2. *RTC with default configuration but RTC_CALR.LPCAL=1*

Table 59. SRAM static power consumption in Stop 3 when supplied by SMPS

Symbol	Parameter	Typ				Max [1]				Unit
		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (SRAM1_16kB)[2]	SRAM1 16-Kbyte page x (x = 1, or 2) static consumption (SRAM1PDSx = 1 vs. SRAM1PDSx = 0)	0.04	0.14	0.44	1.05	0.15	0.41	1.40	3.20	µA
I_{DD} (SRAM1_32kB)[2]	SRAM1 32-Kbyte page x (x = 3, ..., 6, or 7) static consumption (SRAM1PDSx = 1 vs. SRAM1PDSx = 0)	0.08	0.25	0.90	2.05	0.30	0.75	2.70	6.20	
I_{DD} (SRAM2_32kB)[3]	SRAM2 32-Kbyte page 1 static consumption (SRAM2PDS1 = 1 vs. SRAM2PDS1 = 0)	0.10	0.32	1.15	2.55	0.35	0.96	3.50	7.70	
I_{DD} (SRAM2_24kB)[3]	SRAM2 24-Kbyte page 2 static consumption (SRAM2PDS2 = 1 vs. SRAM2PDS2 = 0)	0.07	0.23	0.85	1.95	0.24	0.69	2.60	5.90	
I_{DD} (SRAM2_8kB)[3]	SRAM2 8-Kbyte page 3 static consumption (SRAM2PDS3 = 1 vs. SRAM2PDS3 = 0)	0.02	0.10	0.32	0.72	0.09	0.29	0.95	2.20	
I_{DD} (ICRAM)	ICACHE SRAM static consumption (ICRAMPDS = 1 vs. ICRAMPDS = 0)	0.03	0.11	0.35	0.76	0.12	0.33	1.10	2.30	

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Symbol	Parameter	Typ				Max (1)				Unit
		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (PRAM)	FDCAN and USB SRAM static consumption (PRAMPDS = 1 vs. PRAMPDS = 0)	0.01	0.02	0.11	0.24	0.02	0.06	0.32	0.71	µA
I_{DD} (PKARAM)	PKA SRAM static consumption (PKARAMPDS = 1 vs. PKARAMPDS = 0)	0.01	0.05	0.17	0.45	0.03	0.14	0.51	1.40	

1. *Evaluated by characterization. Not tested in production.*
2. *SRAM1 total consumption is 2 x IDD(SRAM1_16kB) + 5 x IDD(SRAM1_32kB).*
3. *SRAM2 total consumption is IDD(SRAM2_32kB) + IDD(SRAM2_24kB) + IDD(SRAM2_8kB).*

Table 60. Current consumption during wake-up from Stop 3 mode on SMPS

Symbol	Parameter	Conditions		Typ	Unit
		V_{DD}		25°C	
Q_{DD} (wake-up from Stop 3)	Electrical charge consumed during wake-up from Stop 3 mode	Wake-up clock is MSI 48 MHz	3.0	50	µA
		Wake-up clock is HSI 16 MHz		40	
		Wake-up clock is MSI 3 MHz		60	

Table 61. Current consumption in Standby mode

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions		Typ				Max (2)				Unit
		V_{DD}		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog, PWR_CR1. ULPMEN = 1	1.8	0.10	0.4	1.9	6.6	0.31	0.94	4.8	17	µA
			2.4	0.12	0.4	2.0	7.0	0.38	1.1	5.0	18	
			3	0.18	0.6	2.5	7.9	0.55	1.5	6.2	20	
			3.3	0.33	0.9	3.2	9.4	1.1	2.3	8.0	24	
			3.6	0.81	1.7	4.7	11.5	2.5	4.3	12	29	
		No independent watchdog	1.8	0.12	0.5	2.0	6.2	0.36	1.30	5.0	16	
			2.4	0.21	0.5	2.1	6.8	0.64	1.3	5.3	17	
			3	0.27	0.7	2.5	7.5	0.84	1.7	6.3	19	
			3.3	0.41	1.0	3.2	8.9	1.3	2.5	8.0	23	
			3.6	0.87	1.8	4.7	11.0	2.7	4.4	12	28	
		with independent watchdog clocked by LSI 32 kHz	1.8	0.43	0.7	2.2	6.6	1.4	1.8	5.4	17	
			2.4	0.54	0.8	2.5	7.1	1.7	2.2	6.2	18	
			3	0.69	1.1	2.9	8.0	2.2	2.8	7.3	20	
			3.3	0.90	1.5	3.7	9.4	2.8	3.7	9.3	24	
			3.6	1.40	2.3	5.2	11.5	4.4	5.8	13	29	
		with independent watchdog clocked by LSI 250 Hz	1.8	0.26	0.5	2.0	6.5	0.81	1.4	5.0	17	
			2.4	0.30	0.6	2.2	6.9	0.92	1.5	5.4	18	
			3	0.36	0.8	2.6	7.6	1.2	2.0	6.5	19	

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Symbol	Parameter	Conditions	V_{DD}	Typ 25°C	Typ 55°C	Typ 85°C	Typ 105°C	Max (2) 30°C	Max (2) 55°C	Max (2) 85°C	Max (2) 105°C	Unit
I_{DD} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	with independent watchdog clocked by LSI 250 Hz	3.3	0.54	1.1	3.4	9.0	1.7	2.8	8.4	23	µA
			3.6	1.00	1.9	4.8	11.0	3.2	4.8	12	28	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC(1) clocked by LSI 32 kHz, no independent watchdog	1.8	0.44	0.7	2.2	6.6	1.4	1.8	5.4	17	
			2.4	0.55	0.9	2.5	7.1	1.8	2.2	6.2	18	
			3	0.70	1.1	2.9	8.0	2.2	2.8	7.3	20	
			3.3	0.91	1.5	3.8	9.4	2.9	3.7	9.4	24	
			3.6	1.40	2.4	5.2	11.5	4.4	5.9	13	29	
		RTC(1) clocked by LSI 250 Hz, no independent watchdog	1.8	0.26	0.5	2.0	6.5	0.81	1.4	5.0	17	
			2.4	0.30	0.6	2.2	6.9	0.94	1.5	5.5	18	
			3	0.37	0.8	2.6	7.6	1.2	2.0	6.5	19	
			3.3	0.54	1.1	3.4	9.0	1.7	2.8	8.4	23	
			3.6	1.00	2.0	4.8	11.0	3.2	4.9	12	28	
		RTC(1) and independent watchdog clocked by LSI 32 kHz	1.8	0.50	0.8	2.3	6.7	1.6	2.0	5.7	17	
			2.4	0.64	0.9	2.5	7.2	2.0	2.4	6.3	18	
			3	0.82	1.2	3.1	8.1	2.6	3.0	7.7	21	
			3.3	1.05	1.6	3.9	9.5	3.3	4.0	10	24	
			3.6	1.55	2.5	5.4	11.5	4.9	6.3	14	29	
		RTC(1) and independent watchdog clocked by LSI 250 Hz	1.8	0.26	0.5	2.1	6.5	0.81	1.4	5.2	17	
			2.4	0.30	0.6	2.2	6.9	0.94	1.5	5.5	18	
			3	0.38	0.8	2.6	7.6	1.2	2.0	6.5	19	
			3.3	0.54	1.1	3.4	9.0	1.7	2.8	8.4	23	
			3.6	1.00	2.0	4.8	11.0	3.2	4.9	12	28	
		RTC(1) clocked by LSE bypassed at 32768 Hz	1.8	0.36	0.6	2.1	6.6	1.2	1.6	5.3	17	
			2.4	0.45	0.8	2.4	7.1	1.4	1.9	5.9	18	
			3	0.56	1.0	2.8	7.9	1.8	2.5	7.0	20	
			3.3	0.74	1.3	3.6	9.3	2.3	3.3	9.0	24	
			3.6	1.25	2.2	5.1	11.5	3.9	5.4	13	29	
		RTC(1) clocked by LSE quartz in low-drive mode	1.8	0.45	0.7	2.2	6.6	-	-	-	-	
			2.4	0.55	0.9	2.5	7.1	-	-	-	-	
			3	0.63	1.1	2.9	7.9	-	-	-	-	
			3.3	0.79	1.4	3.7	9.3	-	-	-	-	
			3.6	1.25	2.2	5.1	11.5	-	-	-	-	

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Symbol	Parameter	Conditions		Typ				Max (2)				Unit
		V_{DD}		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (SRAM2)	Supply current to be added in Standby mode when full SRAM2 and BKPSRAM are retained	LDO	1.8	1.19	3.3	12	26	4.3	10	35	78	µA
			2.4	1.15	3.3	11	26	4.2	11	35	78	
			3	1.13	3.4	12	26	4.1	11	35	77	
			3.3	1.14	3.3	11	26	4.2	10	34	77	
			3.6	1.14	3.3	11	26	4.1	10	35	77	
I_{DD} (SRAM2_8K)	Supply current to be added in Standby mode when SRAM2 8 KB page 1 is retained		1.8	0.43	1.2	4.1	9.4	1.6	3.6	13	29	
			2.4	0.40	1.2	4.3	9.3	1.5	3.8	13	28	
			3	0.45	1.3	4.2	9.0	1.7	3.8	13	27	
			3.3	0.53	1.4	4.2	9.2	2.0	4.2	13	28	
			3.6	0.39	1.2	4.0	9.0	1.4	3.5	12	27	
I_{DD} (SRAM2)	Supply current to be added in Standby mode when full SRAM2 is retained	SMPS	1.8	0.63	1.7	5.5	12.4	2.3	5.1	17	38	
			2.4	0.40	1.2	4.1	9.3	1.5	3.6	13	28	
			3	0.35	1.0	3.3	7.5	1.3	3.0	10	23	
			3.3	0.33	0.9	3.0	6.7	1.2	2.7	9.0	20	
			3.6	0.29	0.7	2.6	6.0	1.1	2.1	7.7	18	
I_{DD} (SRAM2_8K)	Supply current to be added in Standby mode when SRAM2 8 KB page 1 is retained		1.8	0.29	0.7	2.2	4.9	1.1	2.1	6.5	15	
			2.4	0.17	0.5	1.5	3.3	0.6	1.4	4.5	10	
			3	0.14	0.4	1.2	2.5	0.51	1.2	3.6	7.5	
			3.3	0.13	0.3	1.1	2.2	0.47	1.0	3.2	6.5	
			3.6	0.11	0.2	0.7	2.0	0.40	0.6	2.1	6.0	

Table 62. Current consumption during wake-up from Standby mode

Symbol	Parameter	Conditions		Typ	Unit
		V_{DD}		25°C	
Q_{DD} (wakeup from Standby)	Electrical charge consumed during wakeup from Standby mode	Wake-up clock is MSI 12 MHz	3	2.5	uAs
		Wake-up clock is MSI 3 MHz		2.5	

Table 63. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		Typ				Max (1)				Unit
		V_{DD}		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained), RTC disabled	-	1.8	0.12	0.4	1.7	4.3	0.58	1.3	4.2	11	µA
			2.4	0.14	0.4	1.8	4.6	0.64	1.3	4.5	12	
			3	0.20	0.6	2.2	5.4	0.75	1.6	5.5	14	
			3.3	0.36	0.9	3.0	6.7	1.2	2.4	7.4	17	
			3.6	0.82	1.8	4.4	8.9	2.6	4.4	11	23	

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Symbol	Parameter	Conditions		Typ				Max (1)				Unit
		V_{DD}		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained), RTC enabled	RTC(2) clocked by LSE bypassed at 32768 Hz	1.8	0.30	0.6	1.8	4.5	0.92	1.7	4.5	12	µA
			2.4	0.34	0.7	2.0	4.8	1.1	1.7	5.0	12	
			3	0.45	0.9	2.5	5.6	1.4	2.2	6.2	14	
			3.3	0.65	1.2	3.2	7.0	2.1	3.0	8.0	18	
			3.6	1.15	2.1	4.7	9.3	3.6	5.2	12	24	
		RTC(2) clocked by LSE quartz in low-drive mode	1.8	0.45	0.8	2.0	4.6	-	-	-	-	
			2.4	0.49	0.8	2.2	5.0	-	-	-	-	
			3	0.58	1.0	2.6	5.7	-	-	-	-	
			3.3	0.73	1.4	3.4	7.1	-	-	-	-	
			3.6	1.25	2.2	4.8	9.4	-	-	-	-	

1. *Evaluated by characterization. Not tested in production.*
2. *RTC with default configuration but RTC_CALR.LPCAL = 1*

Table 64. Current consumption during wake-up from Shutdown mode

Symbol	Parameter	Conditions		Typ	Unit
		V_{DD}		25°C	
Q_{DD} (wakeup from Shutdown)	Electrical charge consumed during wakeup from Shutdown mode	Wake-up clock is MSI 12 MHz	3.0	15	uAs

Table 65. Current consumption in V_{BAT} mode

Symbol	Parameter	Conditions		Typ				Max(1)				Unit
		V_{DD}		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
I_{DD} (V_{BAT})	Supply current in VBAT mode (backup registers retained), RTC disabled	-	1.8	0.01	0.07	0.33	0.85	0.04	0.18	0.83	2.2	µA
			2.4	0.01	0.08	0.36	0.91	0.04	0.20	0.90	2.3	
			3	0.02	0.10	0.42	1.00	0.07	0.25	1.1	2.5	
			3.3	0.06	0.20	0.70	1.65	0.20	0.49	1.8	4.2	
			3.6	0.17	0.37	0.99	2.05	0.53	0.93	2.5	5.2	
I_{DD}(V_{BAT} with RTC)	Supply current in VBAT mode (backup registers retained), RTC enabled	RTC(2) clocked by LSE bypassed at 32 KHz	1.8	0.30	0.38	0.67	1.20	0.36	0.52	1.2	2.6	
			2.4	0.37	0.45	0.76	1.35	0.43	0.61	1.4	2.8	
			3	0.46	0.56	0.91	1.50	0.56	0.76	1.6	3.1	
			3.3	0.56	0.71	1.25	2.20	0.74	1.10	2.4	4.8	
			3.6	0.73	0.95	1.60	2.70	1.20	1.6	3.2	5.9	
		RTC(2) clocked by LSE bypassed at 32 KHz, RTC_CALR. LPCAL = 1	1.8	0.23	0.30	0.59	1.15	0.28	0.43	1.2	2.5	
			2.4	0.26	0.35	0.66	1.20	0.32	0.49	1.3	2.6	
			3	0.32	0.42	0.76	1.40	0.40	0.61	1.5	3.0	
			3.3	0.40	0.55	1.10	2.05	0.56	0.9	2.2	4.6	
			3.6	0.56	0.77	1.40	2.50	1.0	1.4	3.0	5.7	

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Symbol	Parameter	Conditions		Typ				Max(1)				Unit
		V_{DD}		25°C	55°C	85°C	105°C	30°C	55°C	85°C	105°C	
$I_{DD}(V_{BAT}$ with RTC)	Supply current in VBAT mode (backup registers retained), RTC enabled	RTC(2) clocked by LSE quartz in low-drive mode	1.8	0.42	0.51	0.79	1.35	-	-	-	-	µA
			2.4	0.47	0.56	0.86	1.40	-	-	-	-	
			3	0.52	0.63	0.97	1.60	-	-	-	-	
			3.3	0.59	0.75	1.30	2.25	-	-	-	-	
			3.6	0.75	0.98	1.60	2.70	-	-	-	-	
		RTC(2) clocked by LSE quartz in low-drive mode, RTC_CALR. LPCAL = 1	1.8	0.35	0.43	0.72	1.25	-	-	-	-	
			2.4	0.37	0.45	0.76	1.30	-	-	-	-	
			3	0.39	0.49	0.84	1.45	-	-	-	-	
			3.3	0.44	0.60	1.15	2.10	-	-	-	-	
			3.6	0.58	0.81	1.45	2.55	-	-	-	-	

1. *Evaluated by characterization. Not tested in production.*
2. *RTC with default configuration except for what is specified*

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up or pull-down generate current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in Section 5.3.14: I/O port characteristics.

For the output pins, any internal or external pull-up or pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of the ADC input pins that must be configured as analog inputs.

Caution: *Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.*

I/O dynamic current consumption

In addition to the on-chip peripheral current consumption (see Table 67 for peripheral current consumption in Run mode), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal and external) connected to the pin:

$I_{SW} = V_{DDIOx} \times f_{SW} \times C$

Where:

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load.
- V_{DDIOx} is the I/O supply voltage.
- f_{SW} is the I/O switching frequency.
- C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$.
- C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

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On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the table below. The MCU is placed under the following conditions:

- All I/O pins are in analog mode.
- The given value is calculated by measuring the difference of the current consumptions:
  - When the peripheral is clocked on
  - When the peripheral is clocked off
- The ambient operating temperature and supply voltage conditions are summarized in Table 27. General operating conditions .
- The power consumption of the digital part of the on-chip peripherals is given in the table below. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 66. Typical dynamic current consumption of peripherals

Indep = Independent clock domain

Bus	Peripheral	LDO			SMPS			Unit
		Range 1	Range 2	Stop 1/2	Range 1	Range 2	Stop 1/2	
AHB1	ADF1	0.83	0.71	1.1	0.27	0.21	0.35	µA/MHz
	ADF1 Indep	0.24	0.18	-	0.08	0.06	-	
	CRC1	0.31	0.26	-	0.1	0.08	-	
	FLASH	2.47	2.14	-	0.81	0.62	-	
	GPDMA1	1.26	1.09	1.53	0.41	0.32	0.5	
	GTZC1	0.24	0.21	-	0.08	0.06	-	
	PWR	0.07	0.05	-	0.02	0.02	-	
	RAMCFG	0.29	0.25	-	0.1	0.07	-	
	SRAM1	0.42	0.36	-	0.14	0.11	-	
	TSC	1.29	1.11	-	0.43	0.33	-	
AHB2	ADC12	5.42	4.7	-	1.77	1.36	-	
	ADC12 Indep	1.07	0.92	-	0.35	0.27	-	
	AES1	1.45	1.27	-	0.47	0.36	-	
	CCB	0.49	0.43	-	0.17	0.13	-	
	DAC1	1.41	1.22	3.53	0.46	0.36	1.18	
	GPIOA	0.05	0.04	-	0.02	0.01	-	
	GPIOB	0.08	0.07	-	0.03	0.02	-	
	GPIOC	0.05	0.04	-	0.02	0.01	-	
	GPIOD	0.08	0.07	-	0.03	0.02	-	
	GPIOE	0.05	0.04	-	0.02	0.01	-	
	GPIOG	0.06	0.05	-	0.02	0.02	-	
	GPIOH	0.04	0.03	-	0.01	0.01	-	
	HASH1	1.13	0.97	-	0.37	0.28	-	
	OSPI1	0.69	0.6	-	0.25	0.18	-	
	OSPI1 Indep	0.44	0.38	-	0.14	0.11	-	
	PKA	5.69	4.92	-	1.86	1.43	-	
	RNG1	1.37	1.18	-	0.45	0.35	-	

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Bus	Peripheral	LDO			SMPS			Unit
		Range 1	Range 2	Stop 1/2	Range 1	Range 2	Stop 1/2	
AHB2	RNG1 Indep	0.14	0.11	-	0.05	0.03	-	µA/MHz
	SAES	4.36	3.76	-	1.41	1.1	-	
	SDMMC1	7.75	6.68	-	2.56	1.94	-	
	SDMMC1 Indep	0.93	0.8	-	0.31	0.23	-	
	SRAM2	0.8	0.7	-	0.28	0.2	-	
APB1	CRS	0.28	0.23	-	0.09	0.06	-	
	FDCAN1	3.31	2.85	-	1.08	0.82	-	
	FDCAN1 Indep	1.8	1.57	-	0.59	0.45	-	
	I2C1	0.61	0.52	2.84	0.19	0.15	0.93	
	I2C1 Indep	1.38	1.19	-	0.45	0.35	-	
	I2C2	0.6	0.51	2.9	0.19	0.15	0.94	
	I2C2 Indep	1.44	1.23	-	0.47	0.36	-	
	I3C1	0.34	0.3	2.8	0.11	0.08	0.91	
	I3C1 Indep	1.6	1.37	-	0.52	0.4	-	
	LPTIM2	0.94	0.82	-	0.31	0.23	-	
	LPTIM2 Indep	2.58	2.22	-	0.85	0.65	-	
	OPAMP	0.28	0.24	-	0.1	0.07	-	
	RTCAPB	2.49	2.15	3.35	0.82	0.62	1.09	
	SPI2	1.34	1.15	2.77	0.43	0.33	0.9	
	SPI2 Indep	0.57	0.49	-	0.19	0.14	-	
	SPI3	1.07	0.91	2.38	0.34	0.27	0.77	
	SPI3 Indep	0.46	0.39	-	0.15	0.12	-	
	TIM2	2.65	2.28	-	0.86	0.69	-	
	TIM3	2.63	2.26	-	0.85	0.67	-	
	TIM4	2.64	2.27	-	0.86	0.68	-	
	TIM6	0.62	0.53	-	0.2	0.17	-	
	TIM7	0.63	0.54	-	0.2	0.16	-	
	UART4	3.73	3.2	2.13	1.21	0.93	0.69	
	UART4 Indep	2.46	2.12	-	0.8	0.61	-	
	UART5	3.7	3.17	2.09	1.2	0.92	0.68	
	UART5 Indep	2.46	2.12	-	0.81	0.61	-	
	USART3	4.28	3.69	2.3	1.39	1.07	0.75	
	USART3 Indep	2.83	2.44	-	0.93	0.71	-	
	VREF	0.16	0.14	-	0.06	0.04	-	
	WWDG1	0.23	0.19	-	0.07	0.06	-	
APB2	I3C2	0.38	0.31	2.75	0.12	0.09	0.9	
	I3C2 Indep	1.7	1.46	-	0.56	0.42	-	
	SAI1	1.18	1.01	-	0.38	0.3	-	
	SAI1 Indep	0.73	0.62	-	0.24	0.18	-	
	SPI1	1.27	1.08	2.62	0.41	0.32	0.86	

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Bus	Peripheral	LDO			SMPS			Unit
		Range 1	Range 2	Stop 1/2	Range 1	Range 2	Stop 1/2	
APB2	SPI1 Indep	0.68	0.59	-	0.22	0.17	-	µA/MHz
	TIM1	3.89	3.35	-	1.27	0.97	-	
	TIM15	2.28	1.96	-	0.75	0.58	-	
	TIM16	1.41	1.2	-	0.46	0.36	-	
	TIM17	1.71	1.46	-	0.56	0.43	-	
	USART1	3.95	3.38	2	1.29	0.99	0.65	
	USART1 Indep	2.63	2.27	-	0.86	0.66	-	
	USB1	2.41	2.06	-	0.78	0.6	-	
	USB1 Indep	0.77	0.66	-	0.25	0.19	-	
APB3	COMP	0.26	0.22	0.26	0.08	0.06	0.08	
	I2C3	0.64	0.55	2.13	0.21	0.16	0.7	
	I2C3 Indep	1.49	1.29	1.49	0.49	0.37	0.49	
	LPTIM1	1.13	0.97	1.13	0.37	0.28	0.37	
	LPTIM1 Indep	2.96	2.57	2.95	0.98	0.74	0.97	
	LPTIM3	0.88	0.75	0.88	0.29	0.22	0.28	
	LPTIM3 Indep	2.59	2.22	2.57	0.85	0.64	0.85	
	LPTIM4	0.71	0.61	0.71	0.23	0.18	0.23	
	LPTIM4 Indep	1.68	1.43	1.67	0.55	0.42	0.55	
	LPUART1	1.16	1.01	1.15	0.38	0.29	0.38	
	LPUART1 Indep	2	1.72	2	0.66	0.5	0.66	
	SYSCFG	0.28	0.25	-	0.09	0.07	-	
-	ALL_ON	104.17	99.41	58.74	37.58	28.85	19.25	

5.3.7 Wake-up time from low-power modes and voltage scaling transition times

The wake-up times given in the table below are the latency between the event and the execution of the first user instruction (FSTEN = 1 in PWR_CR3 if not mentioned).

The device goes in low-power mode after the WFE (wait for event) instruction.

Table 67. Low-power mode wake-up timings on LDO

Symbol	Parameter	Conditions		Typ (3 V, 30°C)	Max (1)(3 V)	Unit
t_{wu}(Sleep	Wake-up time from Sleep mode to Run mode	SLEEP_PD=0	-	15	18	CPU cycles
		SLEEP_PD = 1 with MSI = 48 MHz	-	9.5	18	µs
t_{wu}(Stop 0)	Wake up time from Stop 0 mode to Run mode all SRAMs retained	Wake-up in flash, range 2, PWR_CR2.FLASHFWU = 1 PWR_CR2.SRAMFWU=1 ICACHE OFF	MSI 48 MHz	3.7	4	µs
		Wake-up in flash, range 2, PWR_CR2.FLASHFWU = 0 PWR_CR2.SRAMFWU=0	MSI 48 MHz	9.8	18	
			HSI 16 MHz	9.7	18	
			MSI 3 MHz	14.7	23	

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Symbol	Parameter	Conditions		Typ (3 V, 30°C)	Max (1)(3 V)	Unit
t_{wu}(Stop 0)	Wake up time from Stop 0 mode to Run mode all SRAMs retained	Wake-up in SRAM2, range 2 PWR_CR2.FLASHFWU = 0 PWR_CR2.SRAMFWU=0	MSI 48 MHz	3.5	4	µs
			HSI 16 MHz	4.9	5	
			MSI 3 MHz	10.8	11	
t_{wu}(Stop 1)	Wake-up time from Stop 1 mode to Run mode all SRAMs retained	Wake-up in flash, PWR_CR2.FLASHFWU = 1 PWR_CR2.SRAMFWU = 1 ICACHE OFF	MSI 48 MHz	15.8	19	µs
		Wake-up in flash, PWR_CR2.FLASHFWU = 0 PWR_CR2.SRAMFWU = 0	MSI 48 MHz	21.8	32	
			HSI 16 MHz	20.0	31	
			MSI 3 MHz	26.8	37	
		Wake-up in SRAM2, range 2 PWR_CR2.FLASHFWU = 0 PWR_CR2.SRAMFWU = 0	MSI 48 MHz	15.6	19	
			HSI 16 MHz	16.9	21	
			MSI 3 MHz	22.9	27	
t_{wu}(Stop 2)	Wake-up time from Stop 2 mode to Run mode all SRAMs retained	Wake-up in flash ICACHE OFF	MSI 48 MHz	28.5	45	µs
			HSI 16 MHz	29.4	46	
			MSI 3 MHz	40.9	58	
		Wake-up in SRAM2, range 2	MSI 48 MHz	19.9	33	
			HSI 16 MHz	23.9	36	
			MSI 3 MHz	36.4	49	
t_{wu}(Stop 3)	Wake-up time from Stop 3 mode to Run mode all SRAMs retained	Wake-up in flash, PWR_CR3.FSTEN = 0 ICACHE OFF	MSI 48 MHz	45.6	58	µs
		Wake-up in flash PWR_CR3.FSTEN=1 ICACHE OFF	MSI 48 MHz	39.2	58	
			HSI 16 MHz	40.1	58	
			MSI 3 MHz	51.8	70	
		Wake-up in SRAM2, range 2	MSI 48 MHz	31.6	45	
			HSI 16 MHz	34.4	48	
			MSI 3 MHz	45.6	60	
t_{wu}(Standby with SRAM2)	Wake-up time from Standby with SRAM2 mode to Run mode	Wake-up in flash, PWR_CR3.FSTEN = 0	MSI 12 MHz	56.2	73	µs
		Wake-up in flash PWR_CR3.FSTEN=1	MSI 12 MHz	56.2	73	

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Symbol	Parameter	Conditions		Typ (3 V, 30°C)	Max (1)(3 V)	Unit
t_{wu}(Standby with SRAM2)	Wake-up time from Standby with SRAM2 mode to Run mode	Wake-up in flash PWR_CR3.FSTEN=1	MSI 3 MHz	131.6	149	µs
t_{wu}(Standby)	Wake-up time from Standby mode to Run mode	Wake-up in flash, PWR_CR3.FSTEN = 0	MSI 12 MHz	62.9	131	µs
		Wake-up in flash PWR_CR3.FSTEN = 1	MSI 12 MHz	62.9	81	
			MSI 3 MHz	138.4	158	
t_{wu}(Shutdown)	Wake-up time from Shutdown mode to Run mode	-	MSI 12 MHz	190.4	298	µs

1. *Evaluated by characterization and not tested in production. Temperature range from -40°C to 110°C*

Table 68. Low-power mode wake-up timings on SMPS

.

Symbol	Parameter	Conditions		Typ (3 V, 30°C)	Max(1) (3 V)	Unit
t_{wu}(Sleep)	Wake-up time from Sleep mode to Run mode	SLEEP_PD = 0	-	15	18	Number of CPU cycles
		SLEEP_PD = 1 with MSI = 48 MHz	-	9.5	18	µs
t_{wu}(Stop 0)	Wake-up time from Stop 0 mode to Run mode all SRAMs retained	Wake-up in flash, range 2, PWR_CR2.FLASHFWU = 1 PWR_CR2.SRAMFWU = 1 ICACHE OFF	MSI 48 MHz	3.7	4	µs
		Wake-up in flash, range 2, PWR_CR2.FLASHFWU = 0 PWR_CR2.SRAMFWU = 0	MSI 48 MHz	9.8	18	
			HSI 16 MHz	9.7	18	
			MSI 3 MHz	14.7	23	
		Wake-up in SRAM2, range 2 PWR_CR2.FLASHFWU = 0 PWR_CR2.SRAMFWU = 0	MSI 48 MHz	3.5	4	
			HSI 16 MHz	4.9	5	
			MSI 3 MHz	10.8	11	
t_{wu}(Stop 1)	Wake-up time from Stop 1 mode to Run mode all SRAMs retained	Wake-up in flash, PWR_CR2.FLASHFWU = 1 PWR_CR2.SRAMFWU = 1 ICACHE OFF	MSI 48 MHz	9.1	10	µs
		Wake-up in flash, PWR_CR2.FLASHFWU = 0 PWR_CR2.SRAMFWU = 0	MSI 48 MHz	15.1	23	
			HSI 16 MHz	15.0	23	
			MSI 3 MHz	19.3	23	
		Wake-up in SRAM2, range 2 PWR_CR2.FLASHFWU = 0 PWR_CR2.SRAMFWU = 0	MSI 48 MHz	8.9	10	

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Symbol	Parameter	Conditions		Typ (3 V, 30°C)	Max(1) (3 V)	Unit
t_{wu}(Stop 1)	Wake-up time from Stop 1 mode to Run mode all SRAMs retained	Wake-up in SRAM2, range 2 PWR_CR2.FLASHFWU = 0 PWR_CR2.SRAMFWU = 0	HSI 16 MHz	10.2	11	µs
			MSI 3 MHz	16.2	17	
t_{wu}(Stop 2)	Wake-up time from Stop 2 mode to Run mode all SRAMs retained	Wake-up in flash ICACHE OFF	MSI 48 MHz	28.5	45	µs
			HSI 16 MHz	29.3	46	
			MSI 3 MHz	40.9	58	
		Wake-up in SRAM2, range 2	MSI 48 MHz	19.9	33	
			HSI 16 MHz	24	36	
			MSI 3 MHz	36.4	49	
t_{wu}(Stop 3)	Wake-up time from Stop 3 mode to Run mode all SRAMs retained	Wake-up in flash, PWR_CR3.FSTEN = 0 ICACHE OFF	MSI 48 MHz	39.1	56	µs
		Wake-up in flash PWR_CR3.FSTEN = 1 ICACHE OFF	MSI 48 MHz	39.1	56	
			HSI 16 MHz	40.0	57	
			MSI 3 MHz	51.6	69	
		Wake-up in SRAM2, range 2	MSI 48 MHz	31.4	44	
			HSI 16 MHz	34.2	47	
			MSI 3 MHz	45.4	58	
t_{wu}(Standby with SRAM2)	Wake-up time from Standby with SRAM2 mode to Run mode	Wake-up in flash, PWR_CR3.FSTEN = 0	MSI 12 MHz	56.2	73	µs
		Wake-up in flash, PWR_CR3.FSTEN = 1	MSI 12 MHz	56.2	73	
			MSI 3 MHz	131.6	149	
t_{wu}(Standby)	Wake-up time from Standby mode to Run mode	Wake-up in flash, PWR_CR3.FSTEN = 0	MSI 12 MHz	62.9	132	µs
		Wake-up in flash, PWR_CR3.FSTEN =1	MSI 12 MHz	62.9	81	
			MSI 3 MHz	138.3	158	
t_{wu}(Shutdown)	Wake-up time from Shutdown mode to Run mode	-	MSI 12 MHz	192.0	300	µs

1. *Evaluated by characterization and not tested in production. Temperature range from -40°C to 110°C*

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Table 69. Regulator mode transition times

Symbol	Parameter	Conditions	Typ (3 V, 30 °C)	Max(1) (3 V)	Unit
t_{LDO}(2)	SMPS to LDO transition time	Range 2 (EPOD booster OFF)	17.9	21	µs
		Range 2 (EPOD booster ON)	16.6	21	
		Range 1 (with EPOD booster ON)	15.6	19	
t_{SMPS}(2)	LDO to SMPS transition time	Range 2 (EPOD booster OFF)	14.6	17	µs
		Range 2 (EPOD booster ON)	13.4	16	
		Range 1 (with EPOD booster ON)	16.5	19	
t_{VOST} (without EPOD booster)	Range 1 to range 2	LDO	5.3	8.7	µs
		SMPS	3.6	4.7	
	Range 2 to range 1	LDO	19.5	22	
		SMPS	26.2	31	
t_{VOST} (with EPOD booster)	Range 1 to range 2	LDO	4.4	7.3	µs
		SMPS	2.8	3.7	
	Range 2 to range 1	LDO	18.9	23	
		SMPS	25.1	23	

1. *Evaluated by characterization and not tested in production. Temperature range from -40°C to 110°C.*
2. *Time to PWR_SVMSR.REGS change*

Table 70. Wake-up time using USART/LPUART

Symbol	Parameter	Typ	Max(1)	Unit
$t_{WUUSART}$/ $t_{WULPUART}$	Wake-up time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode when USART/LPUART clock source is HSI16/MSI	-	(2)	µs

1. *Guaranteed by design.*
2. *This wakeup time is HSI16 or the MSI oscillator maximum startup time*

5.3.8 External clock timing characteristics

High-speed external user clock generated from an external source

In bypass mode, the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in Section 5.3.14: I/O port characteristics. However, the recommended clock input waveform is shown in the figure below.

Table 71. High-speed external user clock characteristics

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Digital mode (HSEYBYP = 1, HSEEXT = 1)	-	-	50	MHz
		Analolog mode (HSEYBYP = 1, HSEEXT = 0)	4	-	50	
V_{HSEH}	OSC_IN input pin high-level voltage	Digital mode (HSEYBYP = 1, HSEEXT = 1)	0.7 × V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low-level voltage	Digital mode (HSEYBYP = 1, HSEEXT = 1)	V_{SS}	-	0.3 × V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Digital mode (HSEYBYP = 1, HSEEXT = 1), voltage scaling range 1	7	-	-	ns
		Digital mode (HSEYBYP = 1, HSEEXT = 1), voltage scaling range 2	18	-	-	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$DuCy_{HSE}$	OSC_IN duty cycle	Digital mode (HSEYBYP = 1, HSEEXT = 1)	45	-	55	%
$V_{HSE_ext_PP}$	OSC_IN peak-to-peak amplitude	Analog mode (HSEBYP = 1, HSEEXT = 0)	0.2	-	2/3 V_{DD}	V
V_{HSE_ext}	OSC_IN input range		0	-	V_{DD}	
$t_{r(HSE)}$, $t_{f(HSE)}$	OSC_IN rise and fall time		0.05 / f_{ext_ext}	-	0.3 / f_{ext_ext}	ns

Figure 28. AC timing diagram for high-speed external clock source (digital mode)

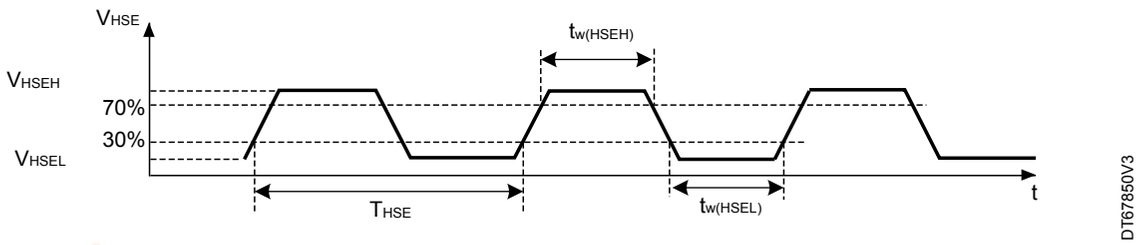
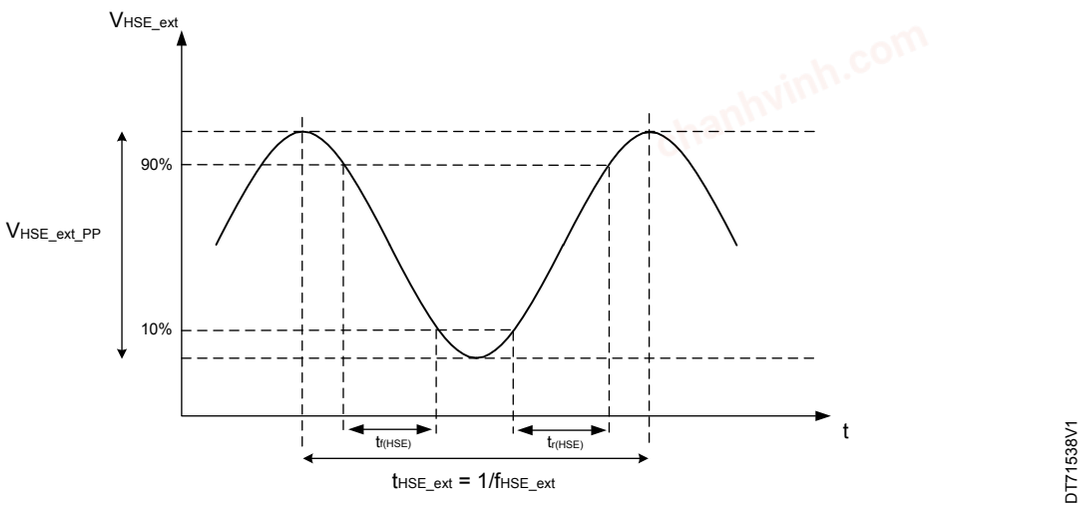


Figure 29. AC timing diagram for high-speed external clock source (analog mode)



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Low-speed external user clock generated from an external source

In bypass mode, the LSE oscillator is switched off and the input pin is directly connected to the LSE clock detector (LSECSS). The external clock signal has to respect the parameters specified in Table 72, as shown also by the waveforms in Figure 30 and Figure 31

Table 72. Low-speed external user clock characteristics

Specified by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	5	32.768	40	kHz
$V_{LSE_ext_PP}$	OSC32_IN peak-to-peak amplitude	0.3	-	V_{SW}	V
V_{LSE_ext}	OSC32_IN input range	0	-	V_{SW}(1)	
$t_{w(LSEH)}$	OSC32_IN high or low time for square signal input	10	-	-	µs
$t_{w(LSEL)}$					

1. *In case V_{BAT} mode is used, V_{LSE_ext} must be lower than V_{BOR0} in order to respect this requirement when the switch to V_{BAT} occurs.*

Figure 30. AC timing diagram for low-speed external square clock source

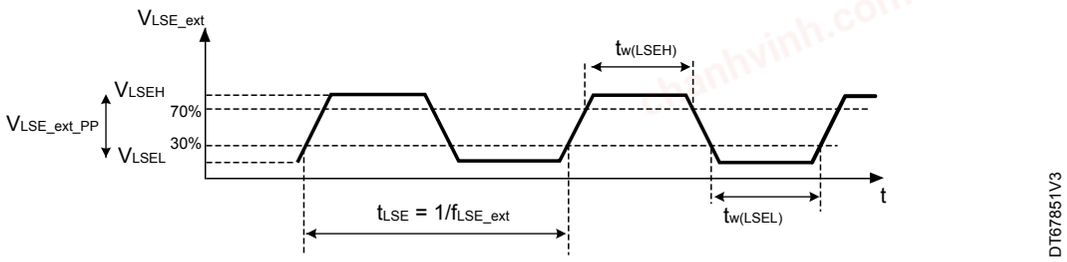
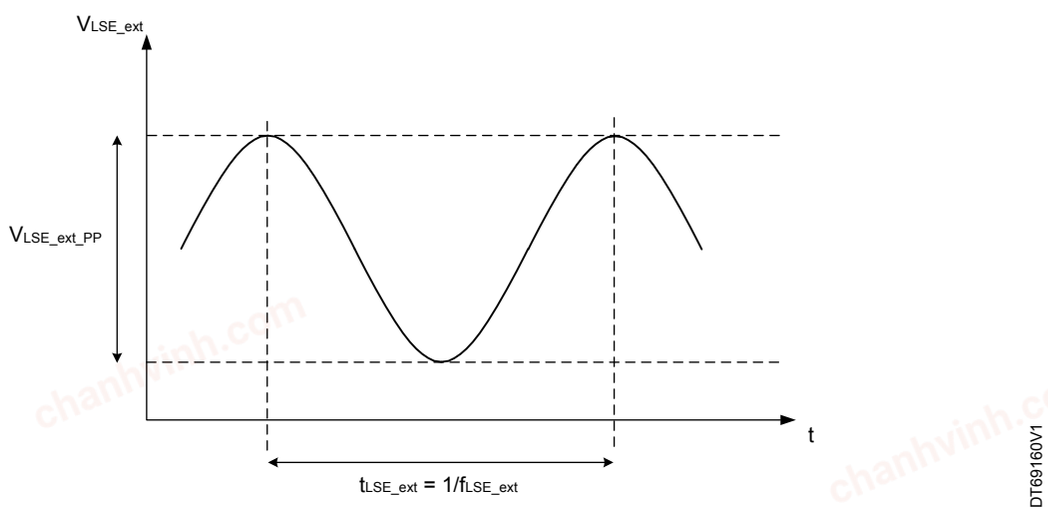


Figure 31. AC timing diagram for low-speed external sinusoidal clock source



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below.

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In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins, in order to minimize the output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 73. HSE oscillator characteristics

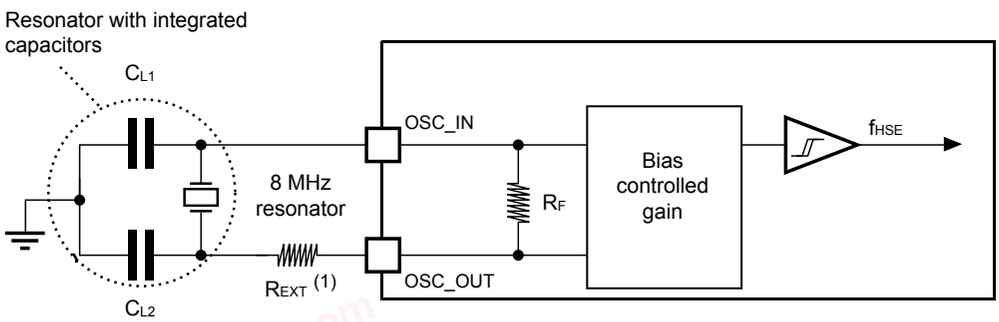
Specified by design and not tested in production.

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	50	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup[2]	-	-	8	µA
		V_{DD} = 3 V, Rm = 30 Ω, C_L = 10 pF @ 4 MHz	-	790	-	
		V_{DD} = 3 V, Rm = 30 Ω, C_L = 10 pF @ 8 MHz	-	910	-	
		V_{DD} = 3 V, Rm = 45 Ω, C_L = 10 pF @ 8 MHz	-	930	-	
		V_{DD} = 3 V, Rm = 30 Ω, C_L = 5 pF @ 48 MHz	-	1430	-	
		V_{DD} = 3 V, Rm = 30 Ω, C_L = 10 pF @ 48 MHz	-	1960	-	
		V_{DD} = 3 V, Rm = 30 Ω, C_L = 20 pF @ 48 MHz	-	3000	-	
$Gm_{critmax}$	Maximum critical crystal transconductance G_m	Startup	-	-	1.5	mA/V
$t_{su(HSE)}$[3]	Startup time	V_{DD} stabilized	-	2	-	ms

1. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*
2. *This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.*
3. *$t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

Note: For information on selecting the crystal, refer to the application note 'Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs' (AN2867).

Figure 32. Typical application with a 8 MHz crystal



(1): R_{EXT} value depends on the crystal characteristics.

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Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 74. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

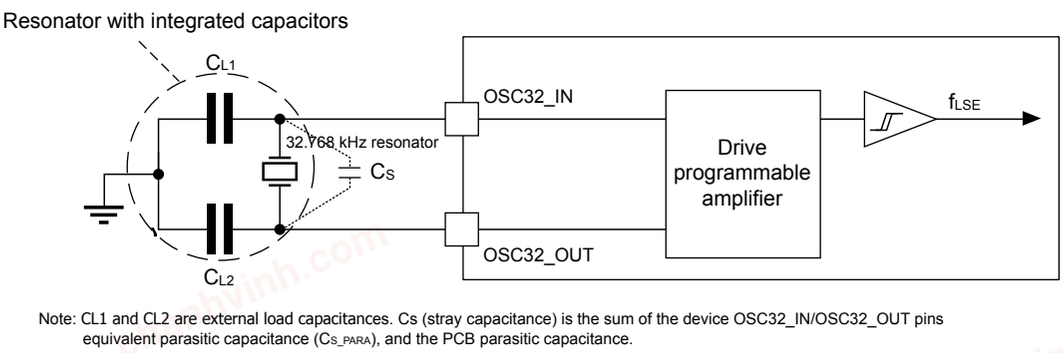
Specified by design and not tested in production.

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00, low-drive capability	-	340	-	nA
		LSEDRV[1:0] = 01, medium low-drive capability	-	380	-	
		LSEDRV[1:0] = 10, medium high-drive capability	-	520	-	
		LSEDRV[1:0] = 11, high-drive capability	-	660	-	
$Gm_{critmax}$	Maximum critical crystal Gm	LSEDRV[1:0] = 00, low-drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, medium low-drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, medium high-drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, high-drive capability	-	-	2.7	
C_{S_PARA}	Internal stray parasitic capacitance[2]	-	-	3	-	pF
$t_{SU(LSE)}$[3]	Startup time	V_{DD} is stabilized	-	2	-	s

1. *Refer to the note below this table.*
2. *C_{S_PARA} is the equivalent capacitance seen by the crystal due to OSC32_IN and OSC32_OUT internal parasitic capacitances.*
3. *$t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer*

Note: For information on selecting the crystal, refer to the application note 'Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs' (AN2867).

Figure 33. Typical application with a 32.768 kHz crystal



Note: CL1 and CL2 are external load capacitances. Cs (stray capacitance) is the sum of the device OSC32_IN/OSC32_OUT pins equivalent parasitic capacitance (C_{S_PARA}), and the PCB parasitic capacitance.

Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

5.3.9 Internal clock timing characteristics

The parameters given in the tables below are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 27. The curves provided are characterization results, not tested in production.

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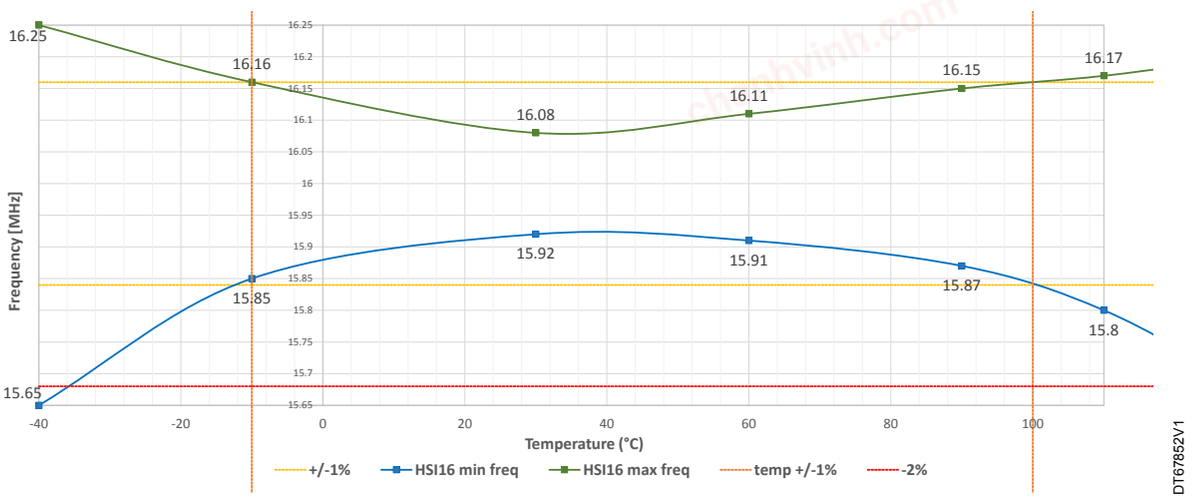
High-speed internal (HSI16) RC oscillator

Table 75. HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}(1)	HSI16 frequency after factory calibration	V_{DD} = 3.0 V, T_J = 30 °C	15.92	16	16.08	MHz
		T_J = –10 °C to 100 °C, 1.58 ≤ V_{DD} ≤ 3.6 V	15.84	-	16.16	
		T_J = –40 °C to 110 °C, 1.58 ≤ V_{DD} ≤ 3.6 V	15.65	-	16.25	
TRIM(2)	HSI16 user trimming step	-	18	29	40	kHz
$DuCy_{(HSI16)}$(2)	Duty cycle	-	45	-	55	%
$t_{su(HSI16)}$(2)	HSI16 oscillator startup time	-	-	2.5	3.6	µs
$t_{stab(HSI16)}$(2)	HSI16 oscillator stabilization time	At 1 % of target frequency	-	4	6	
$I_{DD(HSI16)}$(2)	HSI16 oscillator power consumption	-	-	150	210	µA

1. *Evaluated by characterization. Not tested in production. Does not take into account package and soldering effects.*
2. *Specified by design. Not tested in production.*

Figure 34. HSI16 frequency versus temperature and V_{DD}



Multispeed internal (MSI) RC oscillator

Table 76. MSI oscillator characteristics

Evaluated by characterization and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration	V_{DD} = 3 V and T_J = 30 °C	MSI mode	MSI Range 0(1)	95.50	96.00	96.50	MHz
				MSI Range 1	47.75	48.00	48.25	
				MSI Range 2	23.88	24.00	24.12	
				MSI Range 3	11.95	12.00	12.06	
				MSI Range 4(1)	23.88	24.00	24.12	
				MSI Range 5	11.95	12.00	12.06	
				MSI Range 6	5.97	6.00	6.03	
				MSI Range 7	2.98	3.00	3.02	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration	V_{DD} = 3 V and T_J = 30 °C	PLL mode [2] XTAL = 32.768 kHz	MSI Range 0	-	96.01	-	MHz
				MSI Range 1	-	48.005	-	
				MSI Range 2	-	24.0026	-	
				MSI Range 3	-	12.0013	-	
				MSI Range 4 MSIPLL1N[1:0] = 0x	-	23.986	-	
				MSI Range 5 MSIPLL1N[1:0] = 0x	-	11.003	-	
				MSI Range 6 MSIPLL1N[1:0] = 0x	-	5.9966	-	
				MSI Range 7 MSIPLL1N[1:0] = 0x	-	2.9983	-	
				MSI Range 4 MSIPLL1N[1:0] = 10	-	22.5772	-	
				MSI Range 5 MSIPLL1N[1:0] = 10	-	11.2866	-	
				MSI Range 6 MSIPLL1N[1:0] = 10	-	5.6443	-	
				MSI Range 7 MSIPLL1N[1:0] = 10	-	2.82215	-	
				MSI Range 4 MSIPLL1N[1:0] = 11	-	24.576	-	
				MSI Range 5 MSIPLL1N[1:0] = 11	-	12.288	-	
				MSI Range 6 MSIPLL1N[1:0] = 11	-	6.144	-	
				MSI Range 7 MSIPLL1N[1:0] = 11	-	3.072	-	
			PLL mode XTAL = 16 MHz	MSI Range 0	-	96	-	MHz
				MSI Range 1	-	48	-	
				MSI Range 2	-	24	-	
				MSI Range 3	-	12	-	
				MSI Range 4 MSIPLL1N[1:0] = 0x	-	24.0156	-	
				MSI Range 5 MSIPLL1N[1:0] = 0x	-	12.0078	-	
				MSI Range 6 MSIPLL1N[1:0] = 0x	-	6.0039	-	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration	V_{DD} = 3 V and T_J = 30 °C	PLL mode XTAL = 16 MHz	MSI Range 7 MSIPLL1N[1:0] = 0x	-	3.00195	-	MHz
				MSI Range 4 MSIPLL1N[1:0] = 10	-	22.5809	-	
				MSI Range 5 MSIPLL1N[1:0] = 10	-	11.29045	-	
				MSI Range 6 MSIPLL1N[1:0] = 10	-	5.6452	-	
				MSI Range 7 MSIPLL1N[1:0] = 10	-	2.8226	-	
				MSI Range 4 MSIPLL1N[1:0] = 11	-	24.577	-	
				MSI Range 5 MSIPLL1N[1:0] = 11	-	12.2885	-	
				MSI Range 6 MSIPLL1N[1:0] = 11	-	6.1442	-	
				MSI Range 7 MSIPLL1N[1:0] = 11	-	3.0721	-	
DuCy(MSI)(3)	Duty cycle	MSI Range 0			45	-	55	%
		MSI Range 4			40	-	60	
		MSI others ranges			48	-	52	
TRIM	User trimming step	-			-	0.4	-	%
USER TRIM COVERAGE	User trimming coverage	64 steps			-	±6	-	%
Δ_{TEMP}(MSI)(4)	MSI oscillator frequency drift over temperature (reference is 30 °C)	MSI mode	TJ = -40 to 110 °C	-	-3	-	2	%
Δ_{VDD}(MSI)(4)	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	MSI range 0 to 3	V_{DD} = 1.58 V to 3.6 V	-2	-	1	%
				V_{DD} = 2.4 V to 3.6 V	-1	-	1	
			MSI range 4 to 7	V_{DD} = 1.58 V to 3.6 V	-2	-	1	
				V_{DD} = 2.4 V to 3.6 V	-1	-	1	
$\Delta F_{SAMPLING}$(MSI) (4)(3)	MSI frequency variation in sampling mode (MSIBIAS = 1)	MSI mode	TJ = -40 to 110 °C	-	-	-	0.2	-
CC jitter(MSI)(3)	RMS Cycle-to-cycle jitter	PLL mode	96 MHz (Range 0)	-	-	14	-	ps

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
CC jitter(MSI)(3)	RMS Cycle-to-cycle jitter	PLL mode	24 MHz (Range 4, MSIPLL1N[1:0] = 0x)	-	-	35.5	-	ps
			22.5 MHz (Range 4, MSIPLL1N[1:0] = 10)			38		
			24.6 MHz (Range 4, MSIPLL1N[1:0] = 11)			34.5		
P jitter(MSI)(3)	RMS period jitter	PLL mode	96 MHz (Range 0)	-	-	11	-	ps
			24 MHz (Range 4, MSIPLL1N[1:0] = 0x)			26		
			22.5 MHz (Range 4, MSIPLL1N[1:0] = 10)			28		
			24.6 MHz (Range 4, MSIPLL1N[1:0] = 11)			25		
t_{su}(MSI)(3)	MSI oscillator startup time (5)	MSI range 0 to 3	-	-	-	-	130 ns + 38 cycles of 96 MHz	-
		MSI range 4 to 7	-	-	-	-	350 ns + 16 cycles of 24 MHz	
t_{switch}(MSI)(3)	MSI oscillator transition time(6)	-	-	-	-	2 destination + 2 source MSI cycles(7)	-	-
t_{stab}(MSI)(3)	MSI oscillator stabilization time	Normal mode	Supply Range 1	Final frequency	-	-	10	µs
			Supply Range 2 and Stop modes		-	-	200	
		PLL mode MSIPLLFAST = 0	MSI Range 0 to 3, CKIN = 16 MHz	1% of final frequency	-	-	0.15	ms
			MSI Range 0 to 3, CKIN = 32.768 kHz		-	-	0.8	
			MSI Range 4 to 7		-	-	0.75	
		PLL mode MSIPLLFAST = 1	MSI Range 0 to 3	1% of final frequency	-	-	28 cycles of 96 MHz	-
			MSI Range 4 to 7		-	-	15 cycles of 24 MHz	-
I_{DD}(MSI OFF PLLFAST)(3)	MSI PLL mode oscillator power consumption when disabled with PLL accuracy retention	LDO	MSIPLLEN = 1 and MSIPLLFAST = 1	MSI Range 0 to 3, CKIN = 16 MHz	-	32	-	µA
				MSI Range 0 to 3, CKIN = 32.768 kHz	-	20	-	
				MSI Range 4 to 7	-	8	-	
		SMPS		MSI Range 0 to 3, CKIN = 16 MHz	-	25	-	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{DD}(MSI OFF PLLFAST)(3)	MSI PLL mode oscillator power consumption when disabled with PLL accuracy retention	SMPS	MSIPLLEN = 1 and MSIPLLFAST = 1	MSI Range 0 to 3, CKIN = 32.768 kHz	-	14	-	µA
				MSI Range 4 to 7	-	6.5	-	
I_{DD}(MSI)(3)	MSI oscillator power consumption when ON in continuous mode (voltage scaling Range 1)	LDO	-	MSI Range 0 to 3	-	32 + 0.7 µA/MHz	-	µA
				MSI Range 4 to 7	-	24 + 0.5 µA/MHz	-	
		SMPS	-	MSI Range 0 to 3	-	28 + 0.2 µA/MHz	-	µA
				MSI Range 4 to 7	-	23.3 + 0.15 µA/MHz -	-	
	MSI oscillator power consumption when ON in sampling mode (voltage scaling Range 2 and Stop modes)	LDO	-	MSI Range 0 to 3	-	12 + 0.7 µA/MHz	-	µA
				MSI Range 4 to 7	-	4 + 0.5 µA/MHz	-	
		SMPS	-	MSI Range 0 to 3	-	8 + 0.2 µA/MHz	-	µA
				MSI Range 4 to 7	-	3.3 + 0.15 µA/MHz	-	

1. *Tested in production*
2. *In PLL mode, the MSI accuracy is the LSE crystal accuracy.*
3. *Specified by design. Not tested in production.*
4. *This is a deviation for an individual part once the initial frequency has been measured.*
5. *The MSI startup time is the time when the four MSIRC are in power down.*
6. *This delay is the time to switch from one MSIRC to another one. In case the destination MSIRC is in power down, the total delay is tsu(MSI) + tswitch(MSI).*
7. *When the source and destination clocks are generated from the same MSIRCx (x=0, 1).*

High-speed internal 48 MHz (HSI48) RC oscillator

Table 77. HSI48 oscillator characteristics

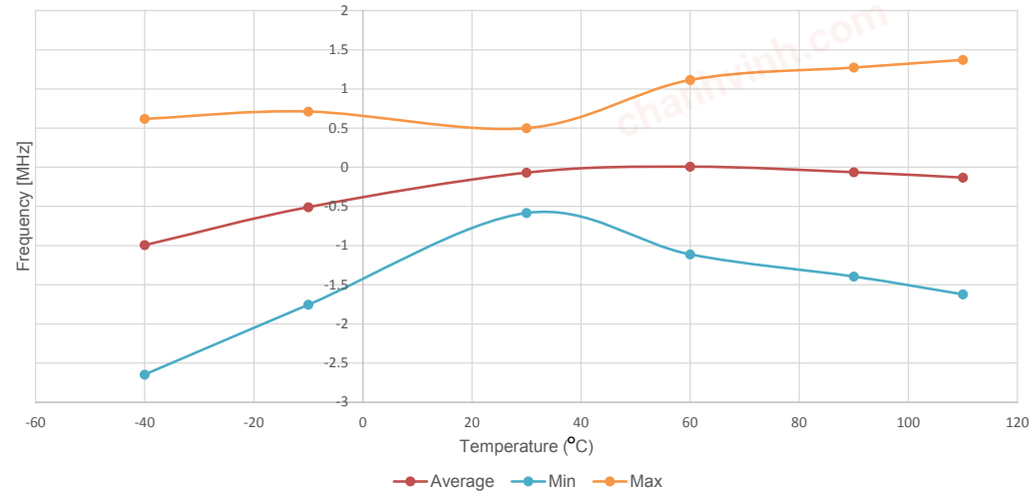
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency after factory calibration	V_{DD} = 3.0 V, T_J = 30 °C	47.5	48	48.5	MHz
TRIM(1)	User trimming step	-	-	0.12	0.18	%
USER TRIM COVERAGE(2)	User trimming coverage	±63 steps	±4.5	±7.56	-	
$DuCy_{(HSI48)}$(1)	Duty cycle	-	45	-	55	
ACC_{HSI48_REL}(2)	Accuracy of the HSI48 oscillator over temperature (factory calibrated)(3) Reference is 3 V and 30 °C.	1.58 V ≤ V_{DD} ≤ 3.6 V, T_J = –40 to 110 °C	-3	-	2	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta_{VDD(HSI48)}$(1)	HSI48 oscillator frequency drift with V_{DD}(4)	3.0 V ≤ V_{DD} ≤ 3.6 V	-	0.025	0.05	%
		1.58 V ≤ V_{DD} ≤ 3.6 V	-	0.05	0.1	
N_T jitter(1)	Next transition jitter Accumulated jitter on 28 cycles(5)	-	-	± 0.15	-	ns
P_T jitter(1)	Paired transition jitter Accumulated jitter on 56 cycles(5)	-	-	± 0.25	-	
$t_{su(HSI48)}$(1)	HSI48 oscillator startup time	-	-	2.5	6	µs
$I_{DD(HSI48)}$(1)	HSI48 oscillator power consumption	-	-	350	400	µA

1. *Specified by design. Not tested in production.*
2. *Evaluated by characterization. Not tested in production.*
3. *$\Delta f_{HSI} = ACC_{HSI48_REL} + \Delta V_{DD}$.*
4. *These values are obtained with one of the following formulas: (Freq(3.6 V) - Freq(3.0 V)) / Freq(3.0 V) or (Freq(3.6 V) Freq(1.58 V)) / freq(1.58 V).*
5. *Jitter measurements are performed without the clock source activated in parallel.*

Figure 35. HSI48 frequency versus temperature



DT77004V1

Low-speed internal (LSI) RC oscillator

Table 78. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.0 V, T_J = 30 °C, LSIPREDIV = 0	31.4	32.0	32.6	kHz
		V_{DD} = 3.0 V, T_J = 30 °C, LSIPREDIV = 1	0.245	0.25	0.255	
		1.71 V ≤ V_{DD} ≤ 3.6, T_J = –40 to 110 °C LSIPREDIV = 0(1)	30.4	32.0	33.6	
DuCy(LSI)	LSI duty cycle	LSIPREDIV = 1	-	50	-	%
$t_{SU(LSI)}$(2)	LSI oscillator startup time	-	-	230	260	µs
$t_{STAB(LSI)}$(2)	LSI oscillator stabilization time	5% of final frequency	-	230	260	
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	LSIPREDIV = 0	-	140	255	nA
		LSIPREDIV = 1	-	130	240	

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1. *Evaluated by characterization, not tested in production, unless otherwise specified.*
2. *Specified by design, not tested in production.*

5.3.10 Flash memory characteristics

Table 79. Flash memory characteristics

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}	64-bit programming time	Normal mode	72.8	80.8	µs
		Burst mode	42.2	46.8	
t_{prog_page}	One 4-Kbyte page programming time	f_{AHB} = 96 MHz, normal mode	37.2	41.3	ms
		f_{AHB} = 96 MHz, burst mode	21.6	24.0	
t_{prog_bank}	One 512-Kbyte bank programming time	f_{AHB} = 96 MHz, normal mode	4767.3	5291.7	
		f_{AHB} = 96 MHz, burst mode	2764.9	3069	
t_{ERASE}	One 4-Kbyte page erase time	10 k endurance cycles	11.8	13.1	
t_{ME}	Mass erase time (one bank)	10 k endurance cycles	11.9	13.2	
	Mass erase time (two banks)		23.9	26.5	
I_{DD}(2)	Average consumption from V_{DD}	Write mode	1.4	-	mA
		Erase mode	1.7	-	
	Maximum current (peak)	Write mode	4.0	-	
		Erase mode	6.4	-	

1. *Evaluated by characterization after cycling. Not tested in production.*
2. *Evaluated by characterization. Not tested in production.*

Table 80. Flash memory endurance and data retention

Symbol	Parameter	Conditions		Min(1)	Unit
N_{END}	Endurance	Whole bank	T_A = –40 to 105 °C	10	Kcycle
t_{RET}	Data retention		T_A = 85 °C after 1 Kcycle(2)	30	Year
			T_A = 105 °C after 1 Kcycle(2)	15	
			T_A = 55 °C after 10 Kcycles(2)	30	
			T_A = 85 °C after 10 Kcycles(2)	15	
			T_A = 105 °C after 10 Kcycles(2)	10	

1. *Evaluated by characterization. Not tested in production.*
2. *Cycling performed over the whole temperature range.*

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through the I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs as follows:

- Electrostatic discharge (ESD) (positive and negative): applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB (fast transient voltage burst) (positive and negative): applied to VDD and VSS pins through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

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A device reset allows normal operations to be resumed.

The test results are given in the table below. They are based on the EMS levels and classes defined in application note *EMC design guide for STM8, STM32 and Legacy MCUs* (AN1709).

Table 81. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25°C, f_{HCLK} = 96 MHz, LQFP100_SMPS package conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25°C, f_{HCLK} = 96 MHz, LQFP100_SMPS package conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

The EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. Note that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for one second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note *Software techniques for improving microcontrollers EMC performance (AN1015)* for more details.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard that specifies the test board and the pin loading.

Table 82. EMI characteristics for f_{HSE} = 16 MHz and f_{HCLK} = 96 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak[1]	V_{DD} = 3.6 V, T_A = 25 ° C, LQFP100_SMPS package compliant with IEC 61967-2	0.1 MHz to 30 MHz	22	dBµV
			30 MHz to 130 MHz	10	
			130 MHz to 1 GHz	10	
			1 GHz to 2 GHz	18	
	Level[2]		0.1 MHz to 2 GHz	4	

1. *Refer to the EMI radiated test section of the application note EMC design guide for STM8, STM32 and Legacy MCUs (AN1709).*
2. *Refer to the EMI level classification section of the application note EMC design guide for STM8, STM32 and Legacy MCUs (AN1709).*

5.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, latch-up) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

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Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 83. ESD absolute maximum ratings

Specified by design and not tested in production.

Symbol	Ratings	Conditions	Packages	PINs	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25°C conforming to ANSI/ESDA/JEDEC JS- 001	All	-	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	TA = 25°C conforming to ANSI/ESDA/JEDEC JS- 002	LQFP100 LDO & SMPS	-	C1	250	
			UFQFPN 48 LDO & SMPS	-	C2a	500	
			UFQFPN 32				
			UFBGA100 LDO & SMPS				
			WLCSP68(1) and WLCSP52				
			LQFP64				
			LQFP48 SMPS				
			UFBGA64 LDO & SMPS	-	TBD	TBD	
			LQFP48 LDO	All except PA3	C2a	500	
				PA3	C1	250	

1. *For both WLCSP68 packages, WLCSP68-G and WLCSP68-Q.*

Static latch-up

The following complementary static tests are required on three parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output, and configurable I/O pin.

These tests are compliant with EIA/JESD 78E IC latch-up standard.

Table 84. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_J = 110°C conforming to JESD78	2

5.3.13 I/O current injection characteristics

As a general rule, the current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) must be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller if abnormal injection accidentally happens, some susceptibility tests are performed on a sample basis during the device characterization.

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Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating-input mode. While this current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter, such as an ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the 5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in the table below. The negative induced leakage current is caused by the negative injection. The positive induced leakage current is caused by the positive injection.

Table 85. I/O current injection susceptibility

The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.
Evaluated by characterization. Not tested in production.

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on PA3/PA4/PA5 and PB0 pins	0	0	mA
	Injected current on PB2/PB5 pins	0	N/A	
	Injected current on all other pins	5	N/A	

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 86 are derived from tests performed under the conditions summarized in Table 27. All I/Os are designed as CMOS and TTL-compliant.

Note: For information on GPIO configuration, refer to the application note STM32 GPIO configuration for hardware settings and low-power consumption (AN4899).

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Table 86. I/O static characteristics

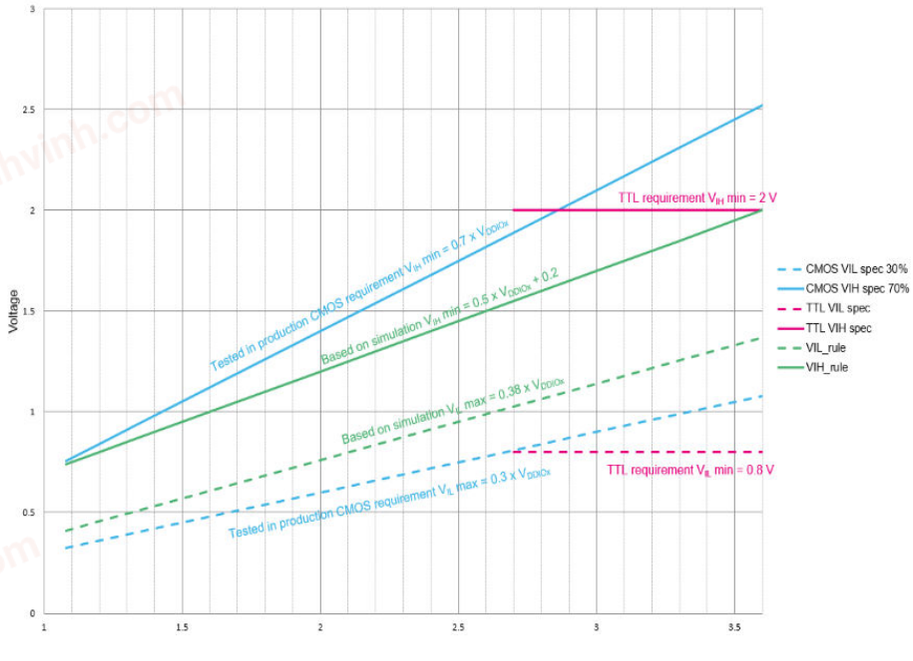
The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.
All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in the figure below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)	I/O input low-level voltage	1.08 V ≤ V_{DDIOx} ≤ 3.6 V		-	-	0.3 V_{DDIOx}	V
		All I/Os		-	-	0.38 V_{DDIOx}(2)	
V_{IH}(1)	I/O input high-level voltage	1.08 V ≤ V_{DDIOx} ≤ 3.6 V		0.7 V_{DDIOx}	-	-	
		All I/Os		0.5 V_{DDIOx} + 0.2(2)	-	-	
V_{hys}(2)	Input hysteresis	TT_xx, FT_xx I/Os		-	250	-	mV
I_{lkg}(2)(3)	Input leakage current	All I/Os except FT_u, FT_d, FT_o, FT_t, TT_xx	V_{IN} ≤ Max (V_{DDxxx})(4)	-	-	150	nA
			Max (V_{DDXXX}) < V_{IN}(5) ≤ Max (V_{DDXXX}) + 1 V	-	-	2000	
			Max (V_{DDXXX}) + 1 V < V_{IN} ≤ 5.5 V(5)	-	-	500	
		FT_o I/Os	V_{IN} ≤ Max (V_{DDXXX})	-	-	50	
			Max (V_{DDXXX}) ≤ V_{IN} ≤ Max (V_{DDXXX}) + 1 V	-	-	500	
			Max (V_{DDXXX}) +1 V ≤ V_{IN} ≤ 5.5 V(5)	-	-	200	
		FT_u I/O	V_{IN}≤ Max (V_{DDXXX})	-	-	200	
			Max (V_{DDXXX}) ≤ V_{IN} ≤ Max (V_{DDXXX}) + 1 V	-	-	2500	
			Max (V_{DDXXX}) ≤ V_{IN} ≤ 5.5	-	-	500	
		FT_t	V_{IN} ≤ Max (V_{DDXXX})	-	-	300	
			Max (V_{DDXXX}) < V_{IN} ≤ Max (V_{DDXXX}) + 1 V(5)	-	-	3000	
			Max (V_{DDXXX}) + 1 V < V_{IN} ≤ 5.5 V(5)	-	-	600	
I_{lkg} (2)(3)	Input leakage current	TT_xx I/Os	V_{IN} ≤ Max (V_{DDXXX})	-	-	500	nA
R_{PU}	Weak pull-up equivalent resistor(6)	-		30	40	50	kΩ
R_{PD}	Weak pulldown equivalent resistor(6)	-		30	40	50	
C_{IO}	I/O pin capacitance	-		-	5	-	pF

1. *Refer to Figure 36. I/O input characteristics (all I/Os except BOOT0).*
2. *Specified by design. Not tested in production.*
3. *This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_Ileak_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] × I_{lkg} max.*
4. *Max (V_{DDxxx}) is the maximum value of all the I/O supplies. The I/O supplies depend on the I/O structure options, as described in Table 20.*
5. *To sustain a voltage higher than Min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) +0.3 V, the internal pull-up and pull-down resistors must be disabled.*
6. *The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).*

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Figure 36. **I/O input characteristics (all I/Os except BOOT0)**



Output driving current

The GPIOs (except PC13, PC14, PC15) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}). PC13, PC14, PC15 are limited in source capability: +3 mA shared between the three I/Os. These GPIOs have the same sink capability than other GPIOs.

In the user application, the number of I/O pins tat can drive current must be limited to respect the absolute maximum rating specified in Section 5.2: Absolute maximum ratings:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating $\sum I_{VDD}$ (see Table 25. Current characteristics).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating $\sum I_{VSS}$ (see Table 25. Current characteristics).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 27. All I/Os are CMOS- and TTL-compliant (FT or TT unless otherwise specified).

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Table 87. Output voltage characteristics (all I/Os except FT_o and PC13)

The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.
The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 25, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low-level voltage	CMOS port(1), $\|I_{IO}\|$ = 8 mA, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high-level voltage		V_{DDIOx} - 0.4	-	
V_{OL}(2)	Output low-level voltage	TTL port(1),$\|I_{IO}\|$ = 8 mA, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	0.4	
V_{OH}(2)	Output high-level voltage		2.4	-	
V_{OL}(2)	Output low-level voltage	All I/Os, $\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	1.3	
V_{OH}(2)	Output high-level voltage		V_{DDIOx} - 1.3	-	
V_{OL}(2)	Output low-level voltage	$\|I_{IO}\|$ = 4 mA, 1.58 V ≤ V_{DDIOx} ≤ 3.6 V	-	0.4	
V_{OH}(2)	Output high-level voltage		V_{DDIOx} - 0.4	-	
V_{OL}(2)	Output low-level voltage	$\|I_{IO}\|$ = 1 mA, 1.08 V ≤ V_{DDIOx} < 3.6 V	-	0.4	
V_{OH}(2)	Output high-level voltage		V_{DDIOx} - 0.4	-	
V_{OLFM+}(2)	Output low-level voltage for a FT_f I/O pin in FM+ mode	$\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	0.4	
		$\|I_{IO}\|$ = 10 mA, 1.58 V ≤ V_{DDIOx} ≤ 3.6 V	-	0.4	
		$\|I_{IO}\|$ = 2 mA, 1.08 V ≤ V_{DDIOx} < 3.6 V	-	0.4	

1. *TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*
2. *Specified by design. Not tested in production.*

Table 88. Output voltage characteristics for FT_o and PC13 I/Os

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low-level voltage	$\|I_{IO}\|$ = 0.5 mA, 2.7 V ≤ V_{SW} ≤ 3.6 V,	-	0.4	V
V_{OH}	Output high-level voltage		V_{SW} - 0.4	-	
V_{OL}	Output low-level voltage	$\|I_{IO}\|$ = 0.25 mA, 1.58 V ≤ V_{SW} ≤ 3.6 V	-	0.4	
V_{OH}	Output high-level voltage		V_{SW} - 0.4	-	

Output AC characteristics

The definition and values of output AC characteristics are given in Figure 37. Output AC characteristics definition and in the table below respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 27.

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Table 89. Output AC characteristics, HSLV OFF (all I/Os except FT_o I/Os and PC13)

FT_o I/O characteristics are provided in Table 91.
The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.
The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the product reference manual for a description of GPIO port configuration register.
Specified by design. Not tested in production.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency all I/Os	C = 50 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	16	MHz
			C = 50 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	4	
			C = 50 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	1	
			C = 10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	20	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	4	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	1	
	t_r/t_f	Output rise and fall time all I/Os	C = 50 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	16.2	ns
			C = 50 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	30.1	
			C = 50 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	56.4	
			C = 10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	10.2	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	20.7	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	39.8	
01	Fmax	Maximum frequency all I/Os	C = 30 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	40	MHz
			C = 30 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	12	
			C = 30 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	3	
			C = 10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	55	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	12	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} ≤<1.58 V	-	3	
	t_r/t_f	Output rise and fall time all I/Os	C = 30 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	5.4	ns
			C = 30 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	9.5	
			C = 30 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	17.6	
			C = 10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	3.6	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	6.5	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	11.9	
10 and 11[1]	Fmax	Maximum frequency all I/Os	C = 30 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	80[2]	MHz
			C = 30 pF, 1.58 V ≤ V_{DDIOx} < 2 V	-	40[2]	
			C = 30 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	6	
			C = 10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	110[2][3]	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2 V	-	50[2]	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	6	
	t_r/t_f	Output rise and fall time all I/Os	C = 30 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	3.3[2]	ns
			C = 30 pF, 1.58 V ≤ V_{DDIOx} < 2 V	-	6.3[2]	
			C = 30 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	11.8	
			C = 10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	2.1[2]	

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Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10 and 11(1)	t_r/t_f	Output rise and fall time all I/Os	C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2 V	-	3.8(2)	ns
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	7.2	
Fm+	Fmax	Maximum frequency	C = 550 pF, 1.08 V ≤ V_{DDIOx} < 3.6 V	-	1	MHz
	t_f	Output fall time(4)	C = 100 pF, 1.58 V ≤ V_{DDIOx} < 3.6 V	-	50	ns
			C = 100 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	80	
			C = 550 pF, 1.58 V ≤ V_{DDIOx} < 3.6 V	-	100	
			C = 550 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	220	

1. *Very high speed config 11 has the same characteritics as High speed config 10.*
2. *Compensation system enabled.*
3. *The I/O frequency is actually limited by the device maximum frequency (96 MHz)*
4. *The fall time is defined between 70% and 30% of the output waveform according to I2C specification.*

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Table 90. Output AC characteristics, HSLV ON (all I/Os)

The I/O structure options listed in this table can be a concatenation of options including the option explicitly listed. For instance, TT_a refers to any TT I/O with _a option. TT_xx refers to any TT I/O and FT_xx refers to any FT I/O.
The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the product reference manual for a description of GPIO port configuration register.
Specified by design. Not tested in production.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C = 50 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	8	MHz
			C = 50 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	2	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	10	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	2	
	t_r/t_f	Output rise and fall time	C = 50 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	16.8	ns
			C = 50 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	30.1	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	10.4	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	17.8	
01	Fmax	Maximum frequency	C = 30 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	50	MHz
			C = 30 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	10	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	50	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	10	
	t_r/t_f	Output rise and fall time	C = 30 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	5.2	ns
			C = 30 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	9.9	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	3	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	5.3	
10 and 11[1]	Fmax	Maximum frequency	C = 30 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	67[2]	MHz
			C = 30 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	20	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	110[2][3]	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	20	
	t_r/t_f	Output rise and fall time	C = 30 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	4.5[2]	ns
			C = 30 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	8.9	
			C = 10 pF, 1.58 V ≤ V_{DDIOx} < 2.7 V	-	2.2[2]	
			C = 10 pF, 1.08 V ≤ V_{DDIOx} < 1.58 V	-	4.4	

1. *Very high speed config 11 has the same characteritics as High speed config 10.*
2. *Compensation system enabled.*
3. *The I/O frequency is actually limited by the device maximum frequency (96 MHz).*

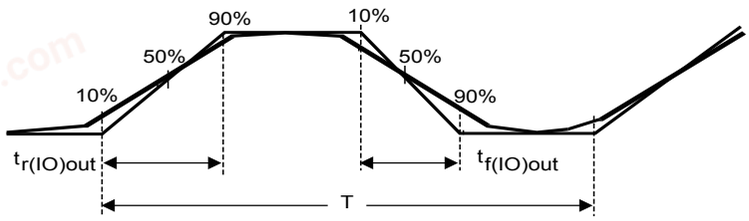
Table 91. Output AC characteristics for FT_o and PC13 I/Os

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Max	Unit
Fmax	Maximum frequency	C_L = 50 pF, 2.7 V ≤ V_{SW} ≤ 3.6 V, V_{DD} off	-	0.5	MHz
		C_L = 50 pF, 1.58 V ≤ V_{SW} < 2.7 V, V_{DD} off	-	0.25	
t_r/t_f	Output rise and fall time	C_L = 50 pF, 2.7 V ≤ V_{SW} ≤ 3.6 V, V_{DD} off	-	400	ns
		C_L = 50 pF, 1.58 V ≤ V_{SW} < 2.7 V, V_{DD} off	-	900	

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Figure 37. **Output AC characteristics definition**



Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

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5.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 27

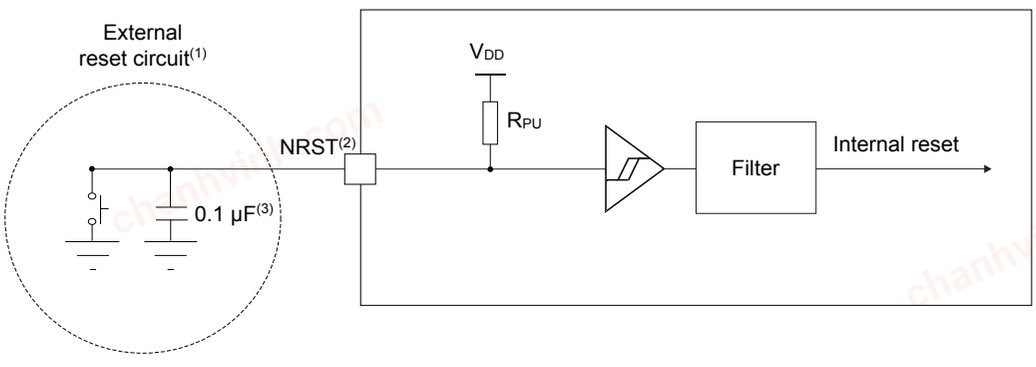
Table 92. **NRST pin characteristics**

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low-level voltage	-	-	-	0.3 x V_{DDIOx}	V
$V_{IH(NRST)}$	NRST input high-level voltage	-	0.7 x V_{DDIOx}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$t_{F(NRST)}$	NRST input filtered pulse	-	-	-	50	ns
$t_{NF(NRST)}$	NRST input not-filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	330	-	-	
		1.58 V ≤ V_{DD} ≤ 3.6 V	1000	-	-	

1. *The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10 % order).*

Figure 38. **Recommended NRST pin protection**



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(1): The reset network protects the device against parasitic resets.

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(2): The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in the above table. Otherwise the reset is not taken into account by the device.

(3): The external capacitor on NRST must be placed as close as possible to the device.

5.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 93. EXTI input characteristics

Specified by design and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	25	-	-	ns

5.3.17 Analog switches booster

Table 94. Analog switches booster characteristics

Specified by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.6	1.8	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	-	-	125	µA

5.3.18 12-bit analog-to-digital converter ADC characteristics

Unless otherwise specified, the parameters given in Table 95 are values derived from tests performed under ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage conditions summarized in Table 27.

Note: It is recommended to perform a calibration after each power-up.

Table 95. 12-bit ADC characteristics

The voltage booster on the ADC switches must be used when V_{DDA} < 2.4 V (embedded I/O switches).

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog power supply for ADC ON	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	-	1	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	1.62 V ≤ V_{DDA} ≤ 3.6 V	0.14	-	55	MHz
	ADC clock duty cycle	-	45	-	55	%
f_s	Sampling rate	Resolution = 12 bits	0.01	-	2.75	Msps
		Resolution = 10 bits	0.012	-	3.05	
		Resolution = 8 bits	0.014	-	3.43	
		Resolution = 6 bits	0.0175	-	3.92	
t_{TRIG}	External trigger period	Resolution = 12 bits	16	-	-	$1/f_{ADC}$
V_{AIN}(1)	Conversion voltage range	-	0	-	V_{REF+}	V
R_{AIN}(2)	External input impedance T_j = 110°C	Resolution = 12 bits	-	-	2.2	kΩ
		Resolution = 10 bits	-	-	6.8	
		Resolution = 8 bits	-	-	33.0	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{AIN}(2)	External input impedance T_j = 110°C	Resolution = 6 bits	-	-	47.0	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
$t_{ADCVREG_STUP}$	ADC LDO startup ready flag time	-	-	-	25	µs
t_{STAB}	ADC power-up time	LDO already started	(3 × 1/f_{ADC}) + 1 conversion			Cycle
t_{OFF_CAL}	Offset calibration time	-	123			1/f_{ADC}
t_{LATR}	Trigger conversion latency	WAIT = 0, AUTOFF = 0, DPD = 0, f_{ADC} = HCLK	3			
t_s	Sampling time	-	1.5	-	1499.5	
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits	t_s + N + 0.5			
$I_{DDA(ADC)}$	ADC consumption on V_{DDA}	f_s = 2.5 Msps	-	360	-	µA
		f_s = 1 Msps	-	180	-	
		f_s = 10 ksps	-	10	-	
		AUTOFF = 1, DPD = 0, no conversion	-	9	-	
		AUTOFF = 1, DPD = 1, no conversion	-	0.1	-	
$I_{DDV(ADC)}$	ADC consumption on V_{REF+}	f_s = 2.5 Msps	-	18	-	
		f_s = 1 Msps	-	10.2	-	
		f_s = 10 ksps	-	0.12	-	
		AUTOFF = 1, DPD = 0, no conversion	-	0.01	-	
		AUTOFF = 1, DPD = 1, no conversion	-	0.01	-	

1. *Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}.*
2. *The maximum value of Rain is specified to keep leakage induced offset within the specified tolerance. The tolerance is 2 LSBs.*

Table 96. Maximum R_{AIN} for 12-bit ADC

BOOSTEN and ANASWVDD configured properly according to V_{DD} and V_{DDA} values.
The values are provided without an external capacitor.
Specified by design. Not tested in production.

Resolution(1)	RAIN max (Ω)(2)	Sampling time [ns]	Sampling cycle at 35 MHz	Sampling cycle at 55 MHz
12 bits	47	276	11.5	23.5
	68	288		
	100	306		
	150	336	23.5	
	220	377		
	330	442		46.5
	470	526		
	680	650		
	1000	840	46.5	
	1500	1134		246.5
	2200	1643	246.5	
	3300	2395		
	4700	3342		

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Resolution(1)	RAIN max (Ω)(2)	Sampling time [ns]	Sampling cycle at 35 MHz	Sampling cycle at 55 MHz
12 bits	6800	4754	246.5	1499.5
	10000	6840		
	15000	9967	1499.5	
	22000	14068		
	33000	19933		N/A
10 bits	47	86	6.5	6.5
	68	90		
	100	95		
	150	108		
	220	116		
	330	136		11.5
	470	161		
	680	212	11.5	23.5
	1000	276		
	1500	376	23.5	
	2200	516		46.5
	3300	735	46.5	
	4700	1012		246.5
	6800	1423	246.5	
	10000	2040		
	15000	2978		
	22000	4356		
	33000	6443		1499.5
	47000	8925	1499.5	
8 bits	47	45	2.5	2.5
	68	46	6.5	6.5
	100	48		
	150	53		
	220	59		
	330	69		
	470	81		
	680	101		
	1000	130		11.5
	1500	177		
	2200	242	11.5	23.5
	3300	345	23.5	
	4700	475		46.5
	6800	670		
	10000	963	246.5	246.5
	15000	1417		
	22000	2040		

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Resolution[1]	RAIN max (Ω)[2]	Sampling time [ns]	Sampling cycle at 35 MHz	Sampling cycle at 55 MHz
8 bits	33000	2995	246.5	246.5
	47000	4158		
6 bits	47	32	1.5	2.5
	68	32		
	100	33		
	150	35		
	220	37		
	330	41	2.5	
	470	49		6.5
	680	61		
	1000	79	6.5	
	1500	106		
	2200	146		11.5
	3300	207	11.5	
	4700	286		23.5
	6800	404	23.5	
	10000	584		46.5
	22000	1250	46.5	246.5
	33000	1853	246.5	
	47000	2607		

1. *The tolerance is 1 LSB*
2. *The maximum value of RAIN is obtained in a worst-case scenario: channel conversion in scan mode with channel i connected to VREF+ and channel i + 1 connected to VREF-.*

Table 97. 12-bit ADC accuracy

ADC DC accuracy values are measured after internal calibration. Resolution = 12 bits, no oversampling.
The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V.
Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	-	-	±3	±7.5	LSB
EO	Offset error	-	-	±2	±5.5	
EG	Gain error	-	-	±2	±6.5	
ED	Differential linearity error	-	-	-0.9/+1	-0.9/+1.5	
EL	Integral linearity error	-	-	±2	±3.5	
ENOB	Effective number of bits	-	9.9	10.9	-	bits
SINAD	Signal-to-noise and distortion ratio	-	61.4	67.4	-	dB
SNR	Signal-to-noise ratio	-	61.6	67.5	-	
THD	Total harmonic distortion	-	-	-74	-70	

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Figure 39. **ADC accuracy characteristics**

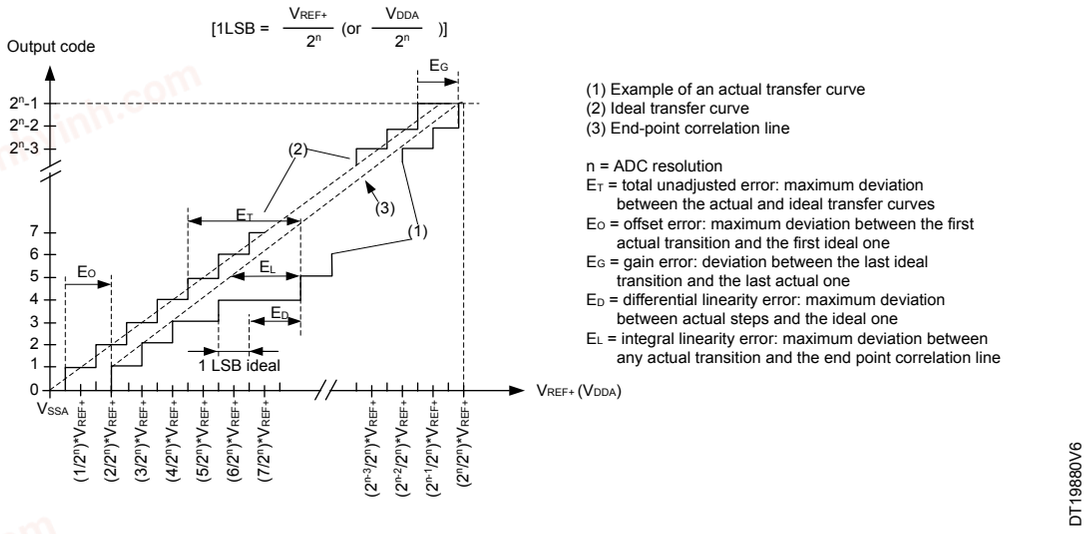
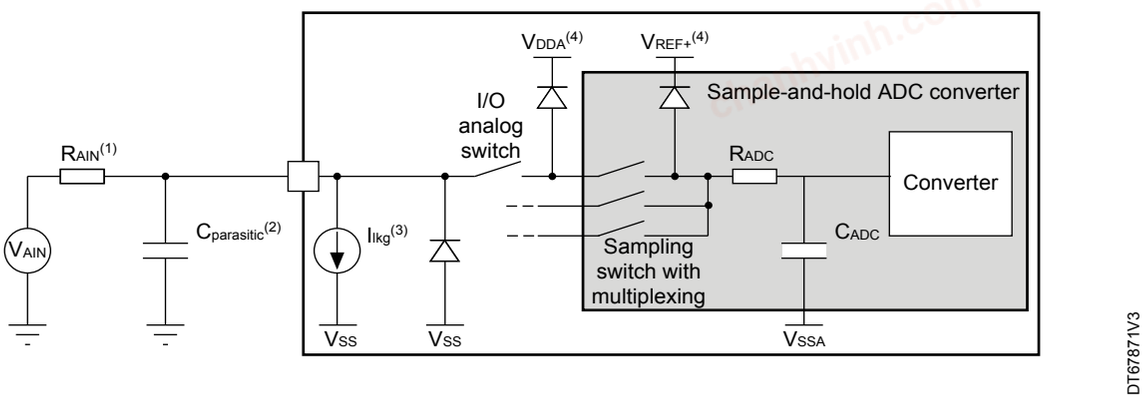


Figure 40. **Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function**



(1): Refer to the ADCx characteristic table for the values of R_{AIN} and C_{ADC}.

(2): $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Table 86. I/O static characteristics for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades the conversion accuracy. To remedy this, f_{ADC} must be reduced.

(3): Refer to Table 86. I/O static characteristics for the values of I_{lkg}.

(4): Refer to Section 5.1.6: Power supply scheme.

General PCB design guidelines

The power-supply decoupling must be performed as shown in the corresponding power-supply scheme. The 100 nF capacitor must be ceramic (good quality) and must be placed as close as possible to the chip.

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5.3.19 Temperature sensor characteristics

Table 98. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{SENSE} linearity with temperature	-	-	1.3	°C
Avg_Slope[1]	Average slope	2	2.5	3.0	mV/°C
V_{30}[2]	Voltage at 30° C (± 1 ° C)	700	752	800	mV
Delta($V_{continuous}$ - $V_{sampling}$)[3]	Difference of voltage between continuous and sampling modes[4]	-	-	–10/+4	
t_{START} (TS_BUF)[3]	Sensor buffer startup time	-	1	10	µs
t_{S_temp}[3]	ADC sampling time when reading the temperature	13	-	-	
$I_{DD(TS)}$[3]	Temperature sensor consumption from V_{DD}, when selected by ADC	-	14	20	µA

1. *Evaluated by characterization. Not tested in production.*
2. *Measured at V_{REF+} = V_{DDA} = 3.0 V ± 10 mV. The V_{30} A/D conversion result is stored in the TS_CAL1 byte. Refer to Table 10. Temperature sensor calibration values.*
3. *Specified by design. Not tested in production.*
4. *The temperature sensor is in continuous mode when the regulator is in range 1. The temperature sensor is in sampling mode when the regulator is in range 2, or when the device is in Stop 1 mode.*

5.3.20 V_{CORE} monitoring characteristics

Table 99. V_{CORE} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{S_VCORE}[1]	ADC sampling time when reading the V_{CORE} voltage	1	-	-	µs

1. *Specified by design. Not tested in production.*

5.3.21 V_{BAT} monitoring characteristics

Table 100. V_{BAT} monitoring characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	4x 25.6	-	kΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er[2]	Error on Q	-5	-	5	%
t_{S_VBAT}[2]	ADC sampling time when reading the V_{BAT}	5	-	-	µs

1. *1.58 V ≤ V_{BAT} ≤ 3.6 V*
2. *Specified by design. Not tested in production.*

Table 101. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

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5.3.22 Digital-to-analog converter characteristics

Table 102. DAC characteristics

Specified by design and not tested in production.

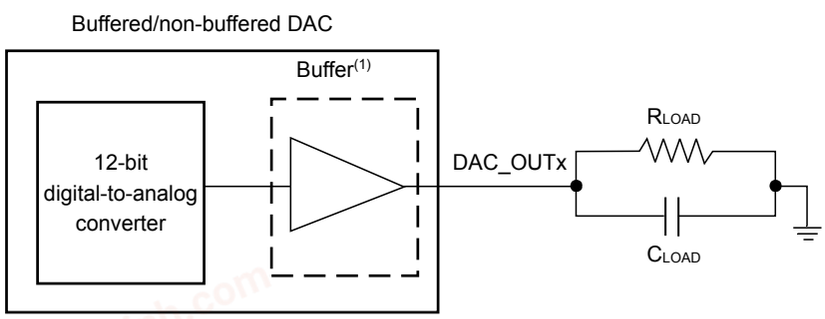
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	-		1.6	-	3.6	V
V_{REF+}	Positive reference voltage	-		1.6	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output impedance	DAC output buffer OFF		10	13	16	
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DDA} = 2.7 V		-	-	1.5	
		V_{DDA} = 2.0 V		-	-	2.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DDA} = 2.7 V		-	-	16.5	
		V_{DDA} = 2.0 V		-	-	17.5	
C_L	Capacitive load	DAC output buffer OFF		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} - 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ± 0.5 LSB, ± 1 LSB, ± 2 LSB, ± 4 LSB, or ± 8 LSB)	Normal mode DAC output buffer ON C_L ≥ 50 pF, R_L ≤ 5 kΩ	± 0.5 LSB	-	2.05	3.05	µs
			± 1 LSB	-	1.90	3	
			± 2 LSB	-	1.85	2.85	
			± 4 LSB	-	1.80	2.8	
			± 8 LSB	-	1.75	2.65	
		Normal mode DAC output buffer OFF, ± 1 LSB, C_L = 10 pF		-	1.7	3	
t_{WAKEUP}[1]	Wake-up time from off state (setting the ENx bit in the DAC control register) until the final value ± 1 LSB	Normal mode DAC output buffer ON C_L ≤ 50 pF, R_L = 5 kΩ		-	4.2	7.5	
		Normal mode DAC output buffer OFF, C_L ≤ 10 pF		-	2	5	
PSRR	DC V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON C_L ≤ 50 pF, R_L = 5 kΩ		-	-80	-28	dB
t_{SAMP}	Sampling time in sample and hold mode, C_{SH} = 100 nF (code transition between the lowest input code and the highest input code when DACOUT reaches the final value ± 1 LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	1.9	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	15	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	8	µs
I_{leak}	Output leakage current	-		-	-	[2]	nA
CI_{int}	Internal sample and hold capacitor	-		7	9.2	11	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1520	-	µV
		V_{REF+} = 1.6 V		-	680	-	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDA(DAC)}$	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	330	510	µA
			No load, worst code (0xF1C)	-	470	680	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	-	0.3	
		Sample and hold mode, C_{SH} = 100 nF		-	330 × T_{ON}(3) /(T_{ON} + T_{OFF})	680 × T_{ON} /(T_{ON} + T_{OFF}) (3)	
$I_{DDV(DAC)}$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	170	240	
			No load, worst code (0x0E4)	-	300	400	
		DAC output buffer OFF	No load, middle/worst code (0x800)	-	145	180	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF (worst code)		-	170 × T_{ON} /(T_{ON} + T_{OFF}) (3)	400 × T_{ON} /(T_{ON} + T_{OFF}) (3)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF (worst code)		-	145 × T_{ON} /(T_{ON} + T_{OFF}) (3)	180 × T_{ON} /(T_{ON} + T_{OFF}) (3)	

1. *In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).*
2. *Refer to Table 86. I/O static characteristics.*
3. *T_{ON} is the refresh phase duration. T_{OFF} is the hold phase duration (see the product reference manual for more details).*

Figure 41. 12-bit buffered/non-buffered DAC



(1) The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

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Table 103. DAC accuracy

Specified by design and not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential nonlinearity(1)	DAC output buffer ON		-	-	± 2	LSB
		DAC output buffer OFF		-	-	± 2	
-	Monotonicity	10 bits		guaranteed			-
INL	Integral nonlinearity(2)	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ		-	-	± 4	LSB
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	-	± 4	
Offset	Offset error at code 0x800(2)	DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	-	± 8	LSB
Offset1	Offset error at code 0x001(3)	DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	-	± 5	
OffsetCal	Offset error at code 0x800(2) after calibration	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	± 5	
			V_{REF+} = 1.6 V	-	-	± 5	
Gain	Gain error(4)	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ		-	-	± 0.5	%
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	-	± 0.5	
TUE	Total unadjusted error	DAC output buffer OFF, C_L ≤ 50 pF, no R_L		-	-	± 10	LSB
		DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ, after calibration		-	-	± 14	
SNR	Signal-to-noise ratio(5)	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ, 1 kHz, BW = 500 kHz		-	70.6	-	dB
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L, 1 kHz, BW = 500 kHz		-	72	-	
THD	Total harmonic distortion(5)	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ, 1 kHz		-	-79	-	
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L, 1 kHz		-	-81	-	
SINAD	Signal-to-noise and distortion ratio(5)	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ, 1 kHz		-	70.1	-	
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L, 1 kHz		-	71.5	-	
ENOB	Effective number of bits	DAC output buffer ON, C_L ≤ 50 pF, R_L ≥ 5 kΩ, 1 kHz		-	11.3	-	bits
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L, 1 kHz		-	11.6	-	

1. *Difference between two consecutive codes minus 1 LSB.*
2. *Difference between the value measured at code i and the value measured at code i on a line drawn between code 0 and last code 4095.*
3. *Difference between the value measured at code (0x001) and the ideal value.*
4. *Difference between the ideal transfer-function slope and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (VREF+ - 0.2 V) when the buffer is ON.*
5. *Signal is -0.5 dBFS with Fsampling = 1 MHz.*

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5.3.23 Voltage reference buffer characteristics

Table 104. VREFBUF characteristics

Specified by design and not tested in production, unless otherwise specified.

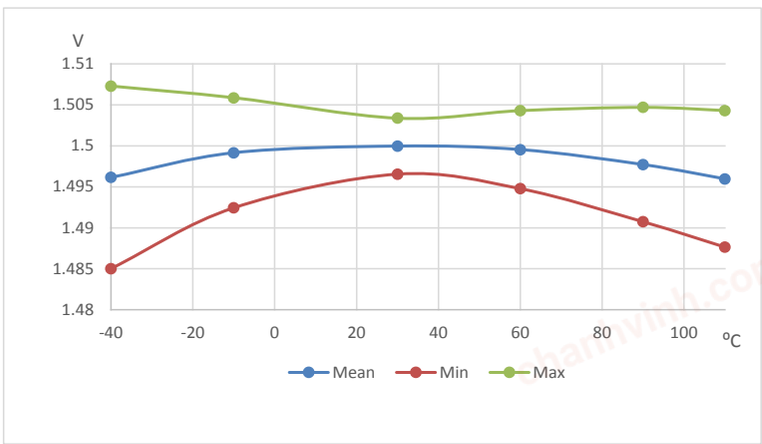
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VRS = 000	1.8	-	3.6	V
			VRS = 001	2.1	-		
			VRS = 010	2.4	-		
			VRS = 011	2.8	-		
		Degraded mode(1)	VRS = 000	1.62	-	1.8	
			VRS = 001		-	2.1	
			VRS = 010		-	2.4	
			VRS = 011		-	2.8	
V_{REFBUF_OUT}(2)	Voltage reference buffer output	Normal mode at V_{DDA} = 3 V, T_J = 30 °C, I_{load} = 10 µA	VRS = 000	1.496	1.5	1.504	
			VRS = 001	1.795	1.8	1.805	
			VRS = 010	2.042	2.048	2.054	
			VRS = 011	2.493	2.5	2.507	
		Degraded mode(1)	VRS = 000	Min (V_{DDA} - 0.15; 1.496)	-	1.504	
			VRS = 001	Min (V_{DDA} - 0.15; 1.795)	-	1.805	
			VRS = 010	Min (V_{DDA} - 0.15; 2.042)	-	2.054	
			VRS = 011	Min (V_{DDA} - 0.15; 2.493)	-	2.507	
TRIM	Trim step	-		0.1	0.175	0.25	%
C_L	Load capacitor(3)	-		0.5	1.10	1.50	µF
esr	C_L equivalent serial resistor	-		-	-	2	Ω
I_{load}	Static load current	-		-	-	4	mA
R_{PD}	Pull-down resistance	-		-	-	400	Ω
I_{line_reg}	Line regulation	$V_{DDAmin} \le V_{DDA} \le 3.6$ V, Normal mode, 500 µA ≤ I_{load} ≤ 4 mA		± 0.016	± 0.033	± 0.053	%
I_{load_reg}	Load regulation(4)	Normal mode, 500 µA ≤ I_{load} ≤ 4 mA		-	50	400	ppm/mA
T_{Coeff}	Temperature coefficient	–40 ° C < T_J < +110 ° C		-	-	$T_{coeff_vrefint}$ + 50	ppm/°C
PSRR	Power supply rejection	DC		-	65	-	dB
		100 kHz		-	30	-	
t_{START}	Startup time	C_L = 0.5 µF		-	110	200	µs
		C_L = 1.1 µF		-	240	350	
		C_L = 1.5 µF		-	320	500	
I_{INRUSH}	Control of DC current drive on V_{REFBUF_OUT}(5) during startup phase	-		-	8	11	mA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	14	18	µA
		I_{load} = 500 µA	-	16	20	
		I_{load} = 4 mA	-	42	50	

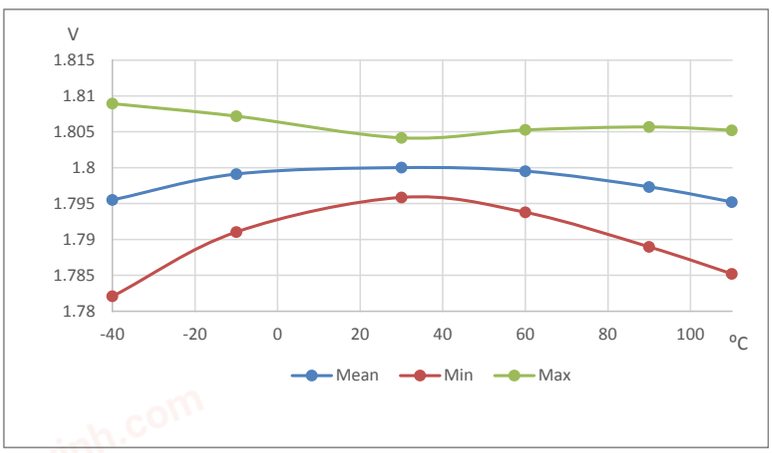
1. *In degraded mode, the voltage reference buffer can not accurately maintain the output voltage (V_{DDA} - drop voltage).*
2. *Evaluated by characterization. Not tested in production.*
3. *The capacitive load must include a 100 nF capacitor in order to cut off the high-frequency noise.*
4. *The load regulation value only takes into account the die and package resistance. The parasitic resistance on PCB degrades this value.*
5. *To correctly control the VREFBUF inrush current during startup phase and scaling change, the V_{DDA} voltage must be in the range of [1.8 V-3.6 V], [2.1 V-3.6 V], [2.4 V-3.6 V] and [2.8 V-3.6 V] for VRS = 000, 001, 010 and 011 respectively.*

Figure 42. V_{REFBUF_OUT} versus temperature (VRS = 000)



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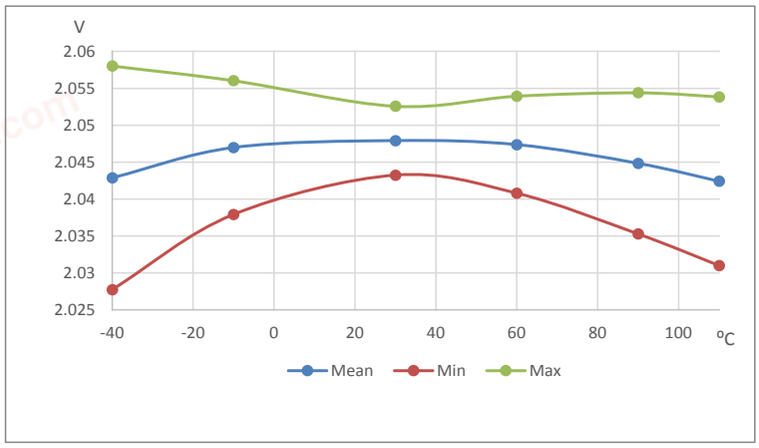
Figure 43. V_{REFBUF_OUT} versus temperature (VRS = 001)



DT69706V2

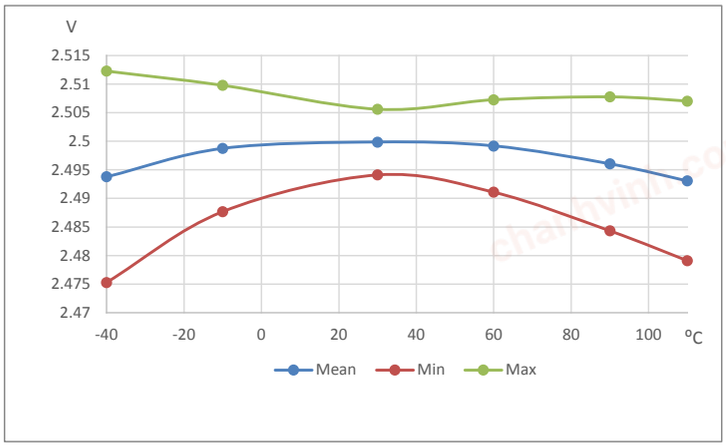
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Figure 44. V_{REFBUF_OUT} versus temperature (VRS = 010)



DT69707V2

Figure 45. V_{REFBUF_OUT} versus temperature (VRS = 011)



DT69708V2

5.3.24 Comparator characteristics

Table 105. COMP characteristics

The input capacitance is negligible compared to the I/O capacitance.
Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for COMP ON	-	1.58	-	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	V
V_{REFINT}(1)	Scaler input voltage	-	(1)			V
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	Scaler bridge disabled(2)	-	0.2	0.25	µA
		Scaler bridge enabled(3)	-	0.7	1	µA
t_{START_SCALER}	Scaler startup time	-	-	130	220	µs
t_{START}(4)	Comparator startup time to reach propagation delay specification	High-speed mode	-	-	8	µs
		Intermediate mode	-	-	12	µs
		Medium mode	-	-	16	µs
		Ultra-low-power mode	-	-	60	µs

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_D(4)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	-	50	100	ns
		Intermediate mode	-	240	490	
		Medium mode	-	400	740	
		Ultra-low-power mode	-	4	7.5	µs
V_{offset}(4)	Comparator offset error	Full common mode range	-	±8	±20	mV
V_{hys}(4)	Comparator hysteresis	No hysteresis	-	0	-	
		Low hysteresis	-	13	-	
		Medium hysteresis	-	26	-	
		High hysteresis	-	39	-	
I_{bias}(4)	Comparator input bias current	-	(5)			nA
$I_{DDA(COMP)}$(4)	Comparator consumption from V_{DDA}	High-speed mode, static	-	43	72	µA
		High-speed mode, with 50 kHz, ±100 mV overdrive square signal	-	44	73	
		Intermediate mode, static	-	8.5	14	
		Intermediate mode with 50 kHz, ±100 mV overdrive square signal	-	9	15	
		Medium mode, static	-	4	7	
		Medium mode, with 50 kHz, ±100 mV overdrive square signal	-	4.5	7.5	
		Ultra-low-power mode, static	-	0.38	1.05	
		Ultra-low-power mode, with 50 kHz, ±100 mV overdrive square signal	-	1.5	2.5	

1. *Refer to Table 30*
2. *No V_{REFINT} division, includes only buffer consumption.*
3. *V_{REFINT} division, includes resistor bridge and buffer consumption.*
4. *Evaluated by characterization. Not tested in production.*
5. *Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in Table 86. I/O static characteristics.*

5.3.25 Operational amplifiers characteristics

Table 106. OPAMP characteristics

OPA_RANGE must be set to 1 in OPAMP1_CSR.
Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage range for OPAMP ON	-	1.60	-	3.6	V
CMIR	Common mode input range	-	0	-	V_{DDA}	
VI_{OFFSET}	Input offset voltage	T_J = 30°C, no load on output, normal mode	-	-	±3	mV
		T_J= 30°C, no load on output, low-power mode	-	-	±3	
		All voltages and temperature, normal mode	-	-	±7	
		All voltages and temperature, low-power mode	-	-	±11.5	
ΔVI_{OFFSET}	Input offset voltage drift over temperature	Normal mode	-	±7	-	µV/°C
		Low-power mode	-	±15	-	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 × V_{DDA})	-		-	1.05	1.25	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 × V_{DDA})	-		-	1.05	1.25	
I_{LOAD}	Drive current	Normal mode		-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode		-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or VDDA)	Normal mode		3.9	-	-	kΩ
		Low-power mode		20	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	79	-	dB
		Low-power mode		-	69	-	
PSRR	Power supply rejection ratio	Normal mode	C_{LOAD} ≤ 50 pF, (1) R_{LOAD} ≥ 3.9 kΩ, DC	35	75	-	
		Low-power mode	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 20 kΩ(1), DC	32	69	-	
GBW	Gain bandwidth product	Normal mode		0.4	2	3.1	MHz
		Low-power mode		0.23	0.5	0.76	
SR(1)	Slew rate (from 10% and 90% of output voltage)	Normal mode	Standard speed mode (OPAHSM = 0)	0.5	1	3.2	V/µs
		Low-power mode		0.14	0.25	0.75	
		Normal mode	High speed mode (OPAHSM = 1)	1.4	3.2	5.6	
		Low-power mode		0.38	0.82	1.5	
AO	Open loop gain	Normal mode		72	105	-	dB
		Low-power mode		77	106	-	
φm	Phase margin	Normal mode		54	67	-	°
		Low-power mode		54	65	-	
GM	Gain margin	Normal mode		-	9	-	dB
		Low-power mode		-	17	-	
V_{OHSAT}(1)	High saturation voltage	Normal mode	I_{LOAD} max or R_{LOAD} min, Input at V_{DDA}	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(1)	Low saturation voltage	Normal mode	I_{LOAD} max or R_{LOAD} min, Input at 0 V	-	-	100	
		Low-power mode		-	-	50	
t_{WAKEUP}	Wake-up time from OFF state	Normal mode	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 3.9 kΩ, follower config.	-	4	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 20 kΩ, follower config.	-	20	40	
I_{bias}	OPAMP input bias current	General purpose input		-	-	(2)	nA
PGA gain(1)	Non-inverting gain value	PGA_GAIN[1:0] = 00		-	2	-	-

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PGA gain(1)	Non-inverting gain value	PGA_GAIN[1:0] = 01		-	4	-	-
		PGA_GAIN[1:0] = 10		-	8	-	
		PGA_GAIN[1:0] = 11		-	16	-	
Rnetwork	R2/R1 internal resistance values in non-inverting PGA mode(3)	PGA gain = 2		-	80/80	-	kΩ/ kΩ
		PGA gain = 4		-	120/40	-	
		PGA gain = 8		-	140/20	-	
		PGA gain = 16		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		-18	-	18	%
PGA gain error	PGA gain error	-		-1	-	1	
PGA BW	PGA bandwidth for different non inverting gain	PGA gain = 2		-	GBW/2	-	MHz
		PGA gain = 4		-	GBW/4	-	
		PGA gain = 8		-	GBW/8	-	
		PGA gain = 16		-	GBW/16	-	
en	Voltage noise density	Normal mode	At 1 kHz, output loaded with 3.9 kΩ	-	220	-	nV /√Hz
		Low-power mode	At 1 kHz, output loaded with 20 kΩ	-	350	-	
		Normal mode	At 10 kHz, output loaded with 3.9 kΩ	-	190	-	
		Low-power mode	at 10 kHz, output loaded with 20 kΩ	-	210	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no load, quiescent mode, standard speed	-	130	190	µA
		Low-power mode		-	40	58	
		Normal mode	no load, quiescent mode, high-speed mode	-	138	205	
		Low-power mode		-	42	60	

1. *Evaluated by characterization. Not tested in production.*
2. *Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in Table 86. I/O static characteristics.*
3. *R2 is the internal resistance between the OPAMP output and the OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.*

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Figure 46. **OPAMP voltage noise density, normal mode, R_{LOAD} = 3.9 kΩ**

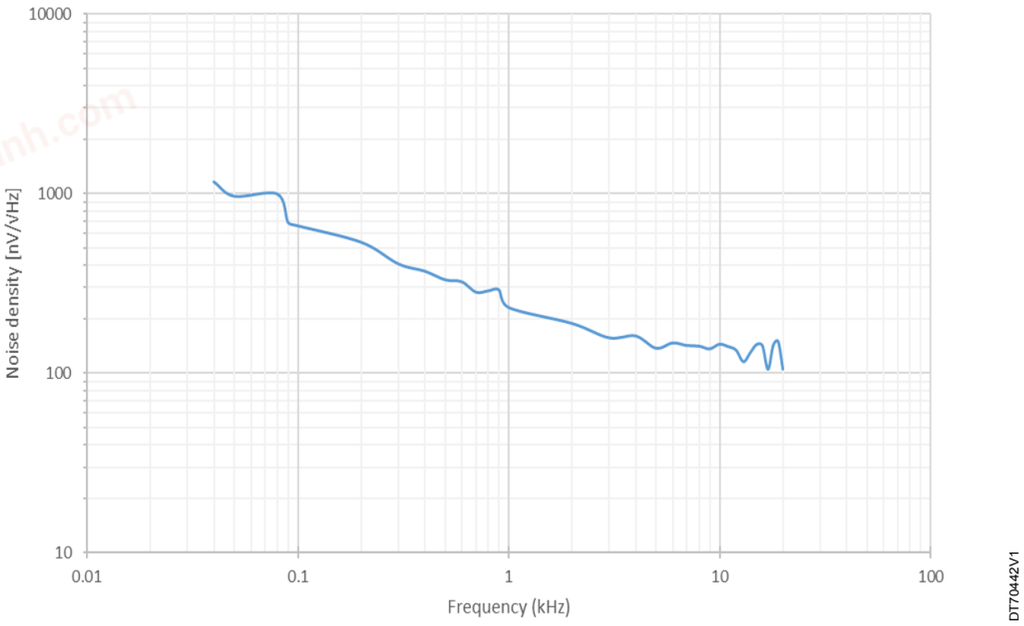
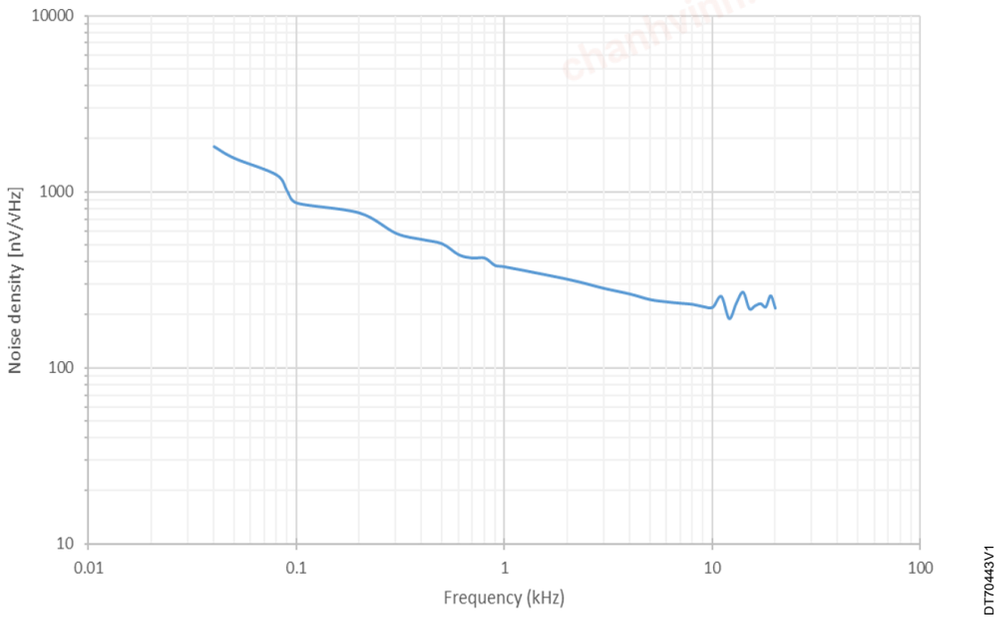


Figure 47. **OPAMP voltage noise density, low-power mode, R_{LOAD} = 20 kΩ**



5.3.26 ADF characteristics

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points done at 0.5 × V_{DD} level
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scaling range 1

Refer to Table 86. I/O static characteristics for more details on the input/output alternate function characteristics.

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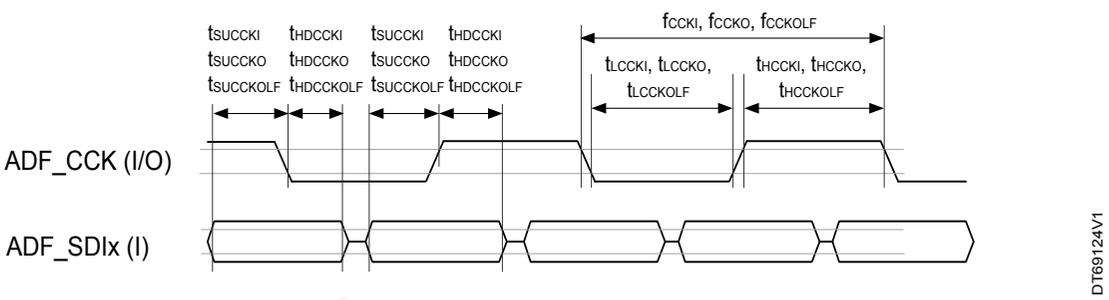
Table 107. ADF characteristics

Evaluated by characterization and not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CCKI}	Input clock frequency via ADF_CCK[1:0] pin, in SLAVE SPI mode	1.71 ≤ V_{DD} ≤ 3.6 V	-	-	25	MHz
f_{CCKO}	Output clock frequency in MASTER SPI mode		-	-	25	
f_{CCKOLF}	Output clock frequency in LF_MASTER SPI mode		-	-	5	
f_{SYMB}	Input symbol rate in Manchester mode		-	-	20	
t_{HCCKI} t_{LCCKI}	ADF_CCK[1:0] input clock high and low time	In SLAVE SPI mode	2 × Tadf_proc_ck(1)	-	-	ns
t_{HCCKO} t_{LCCKO}	ADF_CCK[1:0] output clock high and low time	In MASTER SPI mode	2 × Tadf_proc_ck	-	-	
$t_{HCCKOLF}$ $t_{LCCKOLF}$	ADF_CCK[1:0] output clock high and low time	In LF_MASTER SPI mode	Tadf_proc_ck	-	-	
t_{SUCCKI}	Data setup time with respect to ADF_CCK[1:0] input	In SLAVE SPI mode: ADF_CCK[1:0] configured in input, measured on rising and falling edge	4.5	-	-	
t_{HDCCKI}	Data hold time with respect to ADF_CCK[1:0] input		1.0	-	-	
t_{SUCCKO}	Data setup time with respect to ADF_CCK[1:0] output	In MASTER SPI mode: ADF_CCK[1:0] configured in output, measured on rising and falling edge	4.5	-	-	
t_{HDCCKO}	Data hold time with respect to ADF_CCK[1:0] output		0.5	-	-	
$t_{SUCCKOLF}$	Data setup time with respect to ADF_CCK[1:0] output	In LF_MASTER SPI mode: ADF_CCK[1:0] configured in output, measured on rising and falling edge	15	-	-	
$t_{HDCCKOLF}$	Data hold time with respect to ADF_CCK[1:0] output		0	-	-	

1. *Tadf_proc_ck is the period of the ADF processing clock.*

Figure 48. ADF timing diagram



5.3.27 Timer characteristics

The parameters given in Table 108, Table 109, and Table 110 are specified by design, not tested in production.

Refer to Table 86. I/O static characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

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Table 108. TIMx characteristics

Symbol	Parameter	Conditions	Min	Max	Unit(1)
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96 MHz	10.4	-	ns
fEXT	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 96 MHz	0	48	
ResTIM	Timer resolution	TIMx (except TIM2/TIM3/TIM4)	-	16	bit
		TIM2/TIM3/TIM4	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96 MHz	0.010	682.7	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96 MHz	-	44.739	s

1. *TIMx, is used as a general term in which x stands for 1, 2, 3, 4, 6, 7, 15, 16, 17.*

Table 109. IWDG min/max timeout period at 32 kHz (LSI)

For the values in this table, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock, so that there is always a full RC period of uncertainty.

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

Table 110. WWDG min/max timeout value at 96 MHz (PCLK)

Prescaler	WDGTB	Min timeout values	Max timeout value	Unit
1	0	0.0427	2.731	ms
2	1	0.0853	5.461	
4	2	0.1707	10.923	
8	3	0.3413	21.845	
16	4	0.6827	43.691	
32	5	1.3653	87.381	
64	6	2.7307	174.763	
128	7	5.4613	349.525	

5.3.28 OCTOSPI characteristics

Unless otherwise specified, the parameters given in Table 111, Table 112, and Table 113 are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in Table 27, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Delay block enabled for DTR (with DQS)/HyperBus

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- Measurement points done at 0.5 × V_{DD} level
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scaling range 1

Refer to Table 86. I/O static characteristics for more details on the input/output alternate function characteristics.

Table 111. OCTOSPI characteristics in SDR mode

Measured values in this table apply to Octo- and Quad-SPI data modes. Delay block bypassed.
Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(CLK)}$	OCTOSPI clock frequency	2.7 V < V_{DDIOX} < 3.6 V Voltage range 1 C_L = 15 pF	-	-	96	MHz
		1.71 V < V_{DDIOX} < 3.6 V Voltage range 1 C_L = 15 pF	-	-	93	
		1.71 V < V_{DDIOX} < 3.6 V Voltage range 2 C_L = 15 pF	-	-	48	
		1.08 V ≤ V_{DDIO2} ≤ 1.32 V C_L = 15 pF	-	-	15	
$t_{w(CLKH)}$ $t_{w(CLKL)}$	OCTOSPI clock high and low time (even division)	PRESCALER[7:0] = n (n = 0, 1, 3, 5,..255)	$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$	ns
$t_{w(CLKH)}$	OCTOSPI clock high and low time (odd division)	PRESCALER[7:0] = n (n = 2, 4, 6,..254)	(n/2) × $t_{(CLK)}$/(n+1) - 0.5	-	(n/2) × $t_{(CLK)}$/(n+1)	
$t_{w(CLKL)}$			((n/2)+1) × $t_{(CLK)}$/(n+1) - 0.5	-	((n/2)+1) × $t_{(CLK)}$/(n+1)	
$ts_{(DQ)}$	Data input setup time	Voltage range 1	3	-	-	
		Voltage range 2	5	-	-	
$th_{(DQ)}$	Data input hold time	Voltage range 1	3	-	-	
		Voltage range 2	3.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage range 1	-	1	3	
		Voltage range 2	-	1.5	3.5	
$t_{h(OUT)}$	Data output hold time	Voltage range 1	0	-	-	
		Voltage range 2	0	-	-	

Table 112. OCTOSPI characteristics in DTR mode (no DQS)

Measured values in this table apply to Octo- and Quad-SPI data modes. Delay block bypassed.
Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(CLK)}$	OCTOSPI clock frequency	1.71 V < V_{DDIOX} < 3.6 V Voltage range 1 C_L = 15 pF	-	-	48(1)	MHz
		1.71 V < V_{DDIOX} < 3.6 V Voltage range 2 CL = 15 pF	-	-	24(1)	
		1.08 V ≤ V_{DDIO2} ≤ 1.32 V C_L = 15 pF	-	-	15(1)	
$t_{w(CLKH)}$ $t_{w(CLKL)}$	OCTOSPI clock high and low time (even division)	PRESCALER[7:0] = n (n = 0, 1, 3, 5,..255)	$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$tw_{w(CLKH)}$	OCTOSPI clock high and low time (odd division)	PRESCALER[7:0] = n (n = 2, 4, 6,..254)	(n/2) × $t_{(CLK)}$/(n+1) - 0.5	-	(n/2) × $t_{(CLK)}$/(n+1) + 0.5	ns
$t_{w(CLKL)}$			((n/2)+1) × $t_{(CLK)}$/(n+1) - 0.5	-	((n/2)+1) × $t_{(CLK)}$/(n+1) + 0.5	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input setup time	Voltage range 1	3	-	-	
		Voltage range 2	5	-	-	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	Voltage range 1	3.5	-	-	
		Voltage range 2	4	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time, DHQC = 0	Voltage range 1	-	8.5	13	
		Voltage range 2	-	12.5	21.5	
	Data output valid time, DHQC = 1	Voltage range 1 All prescaler values (except 0)	-	$t_{(CLK)}$/4 + 1.5	$t_{(CLK)}$/4 + 3.5	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time, DHQC = 0	Voltage range 1	5.5	-	-	
		Voltage range 2	10	-	-	
	Data output hold time, DHQC = 1	Voltage range 1 All prescaler values (except 0)	$t_{(CLK)}$/4 - 1	-	-	

1. *Activating DHQC is mandatory to reach this frequency.*

Table 113. OCTOSPI characteristics in DTR mode (with DQS)/HyperBus

Delay block bypassed.
Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(CLK)}$	OCTOSPI clock frequency	1.71 V < V_{DDIOX} < 3.6 V Voltage range 1 C_L = 15 pF	-	-	48(1)(2)	MHz
		1.7 V < V_{DDIOX} < 3.6 V Voltage range 2 C_L = 15 pF	-	-	24(1)(2)	
		1.08 V ≤ V_{DDIO2} ≤ 1.32 V C_L = 15 pF	-	-	15(1)(2)	
$t_{w(CLKH)}$	OCTOSPI clock high and low time (even division)	PRESCALER[7:0] = n (n = 0, 1, 3, 5,..255)	$t_{(CLK)}$/2 - 0.5	-	$t_{(CLK)}$/2 + 0.5	ns
$t_{w(CLKL)}$						
$t_{w(CLKH)}$	OCTOSPI clock high and low time (odd division)	PRESCALER[7:0] = n (n = 2, 4, 6,..254)	(n/2) × $t_{(CLK)}$/(n+1) - 0.5	-	(n/2) × $t_{(CLK)}$/(n+1) + 0.5	
$tw_{w(CLKL)}$			((n/2)+1) × $t_{(CLK)}$/(n+1) - 0.5	-	((n/2)+1) × $t_{(CLK)}$/(n+1) + 0.5	
$t_{v(CLKL)}$	Clock valid time	-	-	-	$t_{(CLK)}$ + 2	
$th_{v(CLK)}$	Clock hold time	-	$t_{(CLK)}$/2 - 1	-	-	
$V_{ODr(CLK)}$(3)	CLK, NCLK crossing level on CLK rising edge	V_{DDIOX} = 1.8 V	1230	-	1450	mV
$V_{ODf(CLK)}$(3)	CLK, NCLK crossing level on CLK falling edge	V_{DDIOX} = 1.8 V	819	-	900	
$t_{w(CS)}$	Chip select high time	-	3 × $t_{(CLK)}$	-	-	ns
$t_{v(DQ)}$	Data input valid time	-	0	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	ns
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	3 × $t_{(CLK)}$	
$t_{sr(DQ)}$ $t_{sf(DQ)}$	Data input setup time	Voltage range 1	-0.5	-	-	
		Voltage range 2	1.25	-	-	
$t_{hr(DQ)}$ $t_{hf(IN)}$	Data input hold time	Voltage range 1	2.5	-	-	
		Voltage range 2	2.5	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time, DHQC = 0	Voltage range 1	-	8.5	13	
		Voltage range 2	-	12.5	21.5	
	Data output valid time, DHQC = 1	Voltage range 1 All prescaler values (except 0)	-	$t_{(CLK)}/4$ + 1.5	$t_{(CLK)}/4$ + 3.5	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time, DHQC = 0	Voltage range 1	5.5	-	-	
		Voltage range 2	10	-	-	
	Data output hold time, DHQC = 1	Voltage range 1 All prescaler values (except 0)	$t_{(CLK)}/4$ - 1	-	-	

1. *Maximum frequency values are given for a RWDS to DQ skew of maximum ±1.0 ns.*
2. *Activating DHQC is mandatory to reach this frequency.*
3. *P10/PB5, PB4/PB5, and PA3/PB5 are recommended to be in line with crossing specification.*

Figure 49. OCTOSPI timing diagram - SDR mode

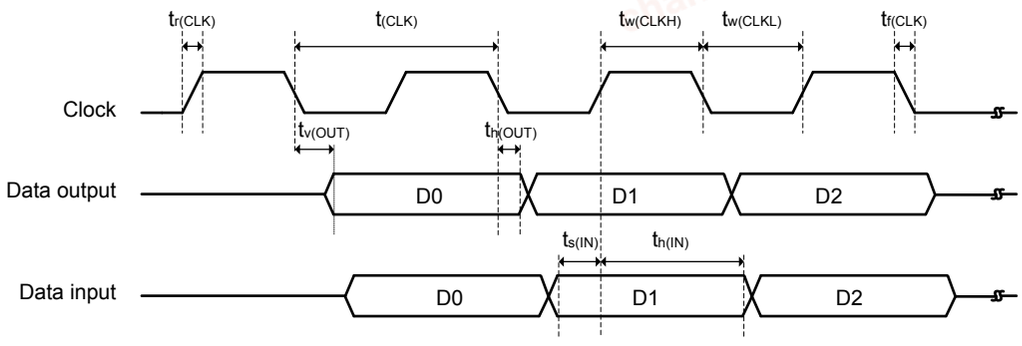
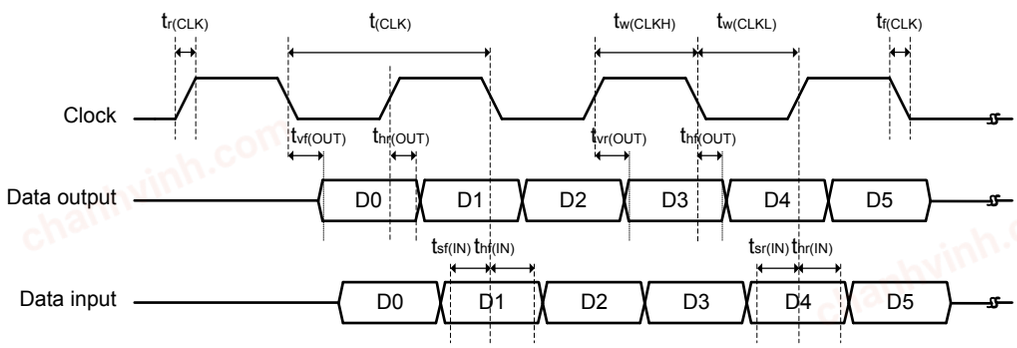


Figure 50. OCTOSPI timing diagram - DDR mode



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Figure 51. **OCTOSPI HyperBus clock**

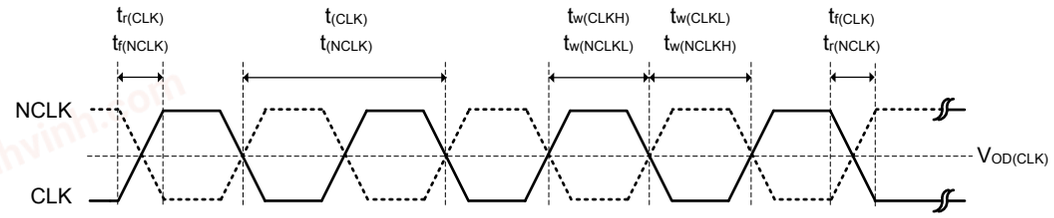


Figure 52. **OCTOSPI HyperBus read**

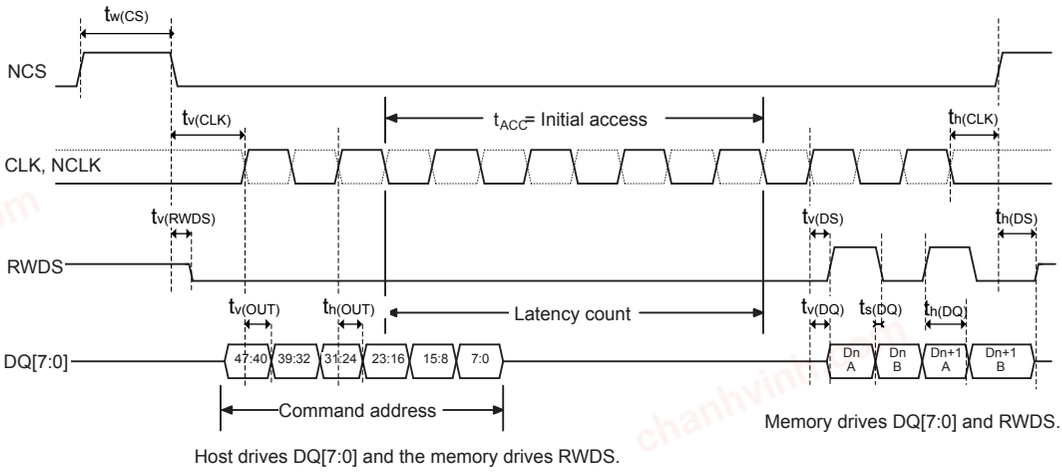
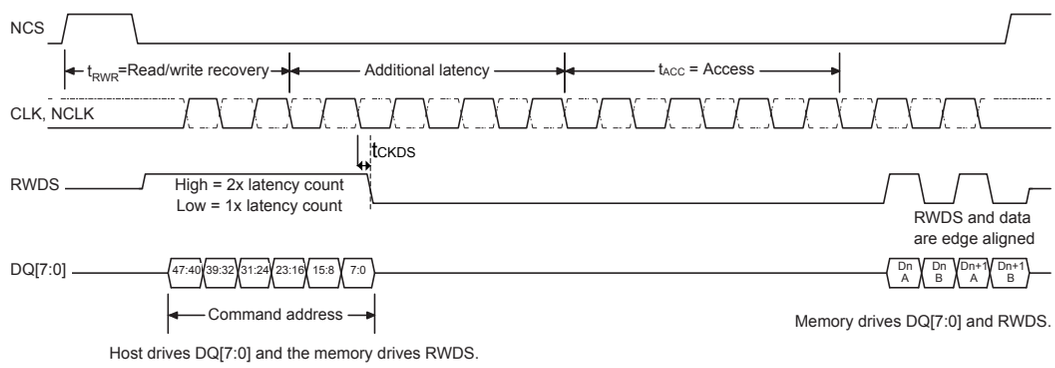
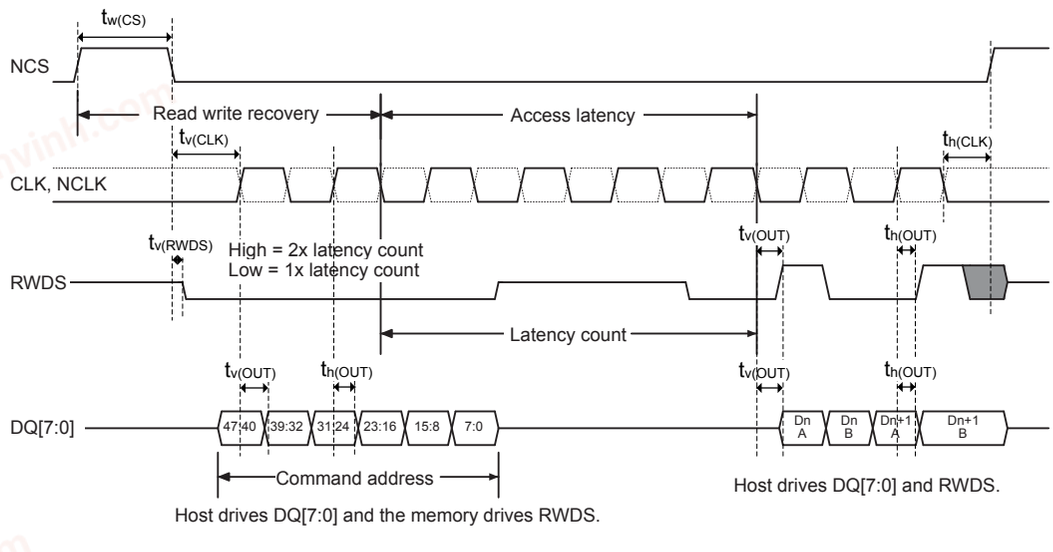


Figure 53. **OCTOSPI HyperBus read with double latency**



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Figure 54. **OCTOSPI HyperBus write**



5.3.29 SD/SDIO/e.MMC card host interfaces (SDMMC) characteristics

Unless otherwise specified, the parameters given in Table 114 and Table 115 are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in Table 27, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load CL = 30 pF, unless otherwise specified
- Measurement points done at 0.5 × V_{DD} level
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scaling range 1

Refer to Table 86. I/O static characteristics for more details on the input/output alternate function characteristics.

Table 114. **SD/e.MMC characteristics (V_{DD} = 2.7 V to 3.6 V)**

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	96(1)	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} = 48 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 48 MHz	9.5	10.5	-	
CMD, D inputs (referenced to CK) in e.MMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) modes						
t_{ISU}	Input setup time HS	-	4	-	-	ns
t_{IH}	Input hold time HS	-	1.5	-	-	
t_{IDW}(3)	Input valid window (variable window)	-	4.5	-	-	
CMD, D outputs (referenced to CK) in e.MMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) modes						
t_{OV}	Output valid time HS	-	-	6	6.6	ns
t_{OH}	Output hold time HS	-	4	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISU}	Input setup time SD	-	4	-	-	ns
t_{IH}	Input hold time SD	-	0.5	-	-	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D outputs (referenced to CK) in SD default mode						
t_{OV}	Output valid default time SD	-	-	0.5	1.5	ns
t_{OH}	Output hold default time SD	-	0	-	-	

1. *With capacitive load C_L = 20 pF.*
2. *For SD 1.8 V support, an external voltage converter is needed.*
3. *Minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Table 115. e.MMC characteristics (V_{DD} = 1.71 V to 1.9 V)

Evaluated by characterization. Not tested in production.

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	-	-	84	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} = 48 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 48 MHz	9.5	10.5	-	
CMD, D inputs (referenced to CK) in e.MMC mode						
t_{ISU}	Input setup time HS	-	3	-	-	ns
t_{IH}	Input hold time HS	-	2.5	-	-	
t_{IDW}[2]	Input valid window (variable window)	-	5	-	-	
CMD, D outputs (referenced to CK) in e.MMC mode						
t_{OV}	Output valid time HS	-	-	6	7.5	ns
t_{OH}	Output hold time HS	-	4	-	-	

1. *With capacitive load CL = 20 pF.*
2. *Minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Figure 55. SD high-speed mode

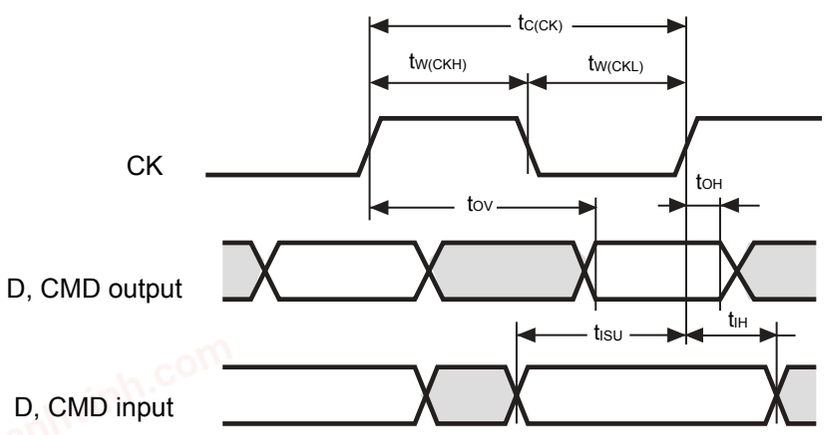
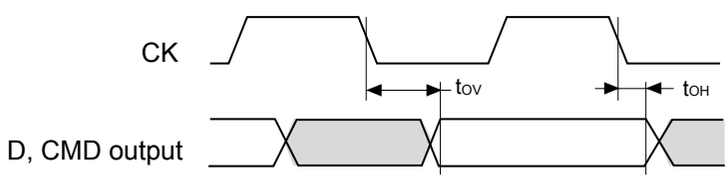
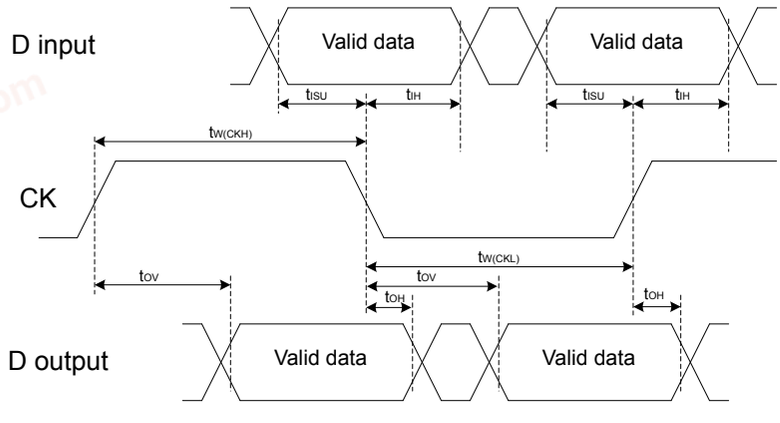


Figure 56. SD default mode



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Figure 57. **SDMMC DDR mode**



5.3.30 Delay block characteristics

Unless otherwise specified, the parameters given in Table 116 are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in Table 27.

Table 116. **Delay block characteristics**

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	560	1360	2560	ps
t_{Δ}	Unit delay	-	55	63	87	

5.3.31 I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bitrate up to 100 Kbit/s
- Fast-mode (Fm): with a bitrate up to 400 Kbit/s
- Fast-mode Plus (Fm+): with a bitrate up to 1 Mbit/s

The I2C timings requirements are specified by design, not tested in production, when the I2C peripheral is properly configured (refer to the product reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low-level output-current maximum requirement. Refer to Table 86. I/O static characteristics for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics.

Table 117. **I2C analog filter characteristics**

The measurement points are performed at 50% V_{DD}.
Evaluated by characterization. Not tested in production.

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(1)	160(2)	ns

1. *Spikes with widths below t_{AF} min are filtered.*
2. *Spikes with width above t_{AF} max are not filtered.*

5.3.32 I3C interface characteristics

The I3C interface meets the timing requirements of the MIPI® I3C specification v1.1.

The I3C peripheral supports:

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- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

The parameters given in Table 118 below are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O Compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V
- Voltage scaling range 1

The I3C timings are in line with the MIPI specification, except for the ones given in Table 118, I3C open-drain measured timing. For tS_{U_OD}, this can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register. For further details refer to AN5879.

Table 118. Open drain timing measurements

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Unit
t_{SU_OD}	SDA data setup time during open drain mode	Controller 1.71 V ≤ V_{DDIOX} ≤ 3.6 V	21(1)	ns
		Controller 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	24.5(1)	

1. *SDA data setup time during open drain mode is required to be Min 3ns in the MIPI specification.*

Table 119. Push pull timing measurements

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Max	Unit
t_{SCO}	Clock in to data out for target	Target 1.71 V ≤ V_{DDIOX} ≤ 3.6 V	11.5	ns
		Target 1.2 V ≤ V_{DDIO2} ≤ 1.32 V	12	
		Target 1.08 V ≤ V_{DDIO2} ≤ 1.2 V	14(1)	

1. *t_{SCO} clock in to data out is required to be Max 12 ns in MIPI specification.*

5.3.33 USART characteristics

Unless otherwise specified, the parameters given in Table 120 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in not found, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points done at 0.5 × V_{DD} level
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V
- Voltage scaling range 1

Refer to Section 5.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

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Table 120. USART (SPI mode) characteristics

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{CK}	USART clock frequency	SPI master mode 1.71 V ≤ V_{DDIOX} ≤ 3.6 V		-		12	MHz
		SPI slave mode 1.71 V ≤ V_{DDIOX} ≤ 3.6 V				32	
		SPI master or slave mode 1.08 V ≤ V_{DDIO2} ≤ 1.32 V				15	
$t_{su(NSS)}$	NSS setup time	SPI Ssave mode		t_{ker}(1) + 3	-	-	ns
$t_{h(NSS)}$	NSS hold time	SPI slave mode		2	-	-	
$t_{w(CKH)}$	CK high and low time	SPI master mode		1/ f_{CK} /2-1	1/ f_{CK} /2	1/ f_{CK} /2+1	
$t_{w(CKL)}$							
$t_{su(RX)}$	Data input setup time	SPI master mode		14/22(2)	-	-	
$t_{su(RX)}$		SPI slave mode		2.5	-	-	
$t_{h(RX)}$	Data input hold time	SPI master mode		0.5	-	-	
$t_{h(RX)}$		SPI slave mode		1	-	-	
$t_{v(TX)}$	Data output valid time	SPI Slave mode	2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	11.5	15.5	
			1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-			
			1.08 V ≤ V_{DDO2} ≤ 1.32 V		15.5	23.5	
$t_{v(TX)}$		SPI Master mode	2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	0.5	2	
			1.71 V ≤ V_{DDIOX} ≤ 3.6 V			2.5	
$t_{h(TX)}$	Data output hold time	SPI slave mode		8	-	-	
$t_{h(TX)}$	Data output hold time	SPI master mode		0	-	-	

1. *T_{ker} is the usart_ker_ck_pres clock period.*
2. *When using SPI on port G.*

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Figure 58. **USART timing diagram in SPI master mode**

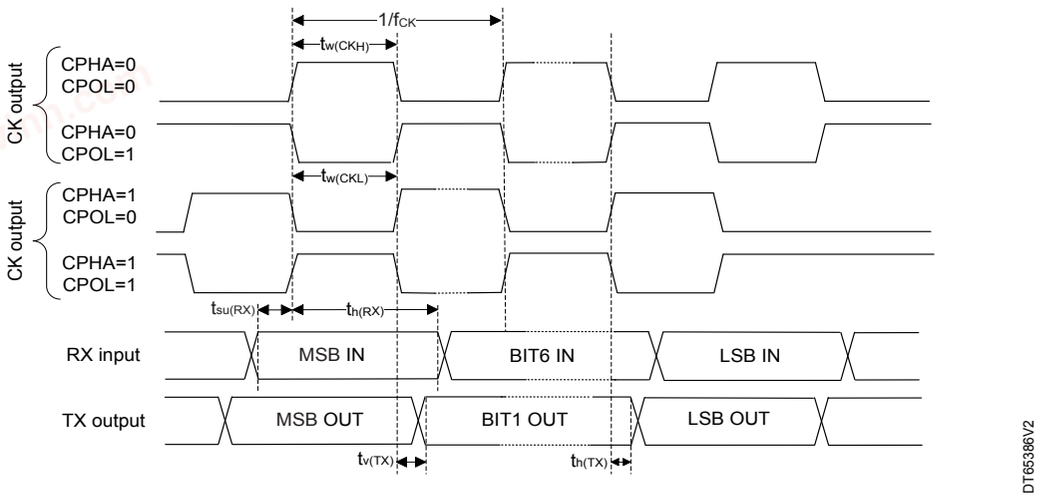
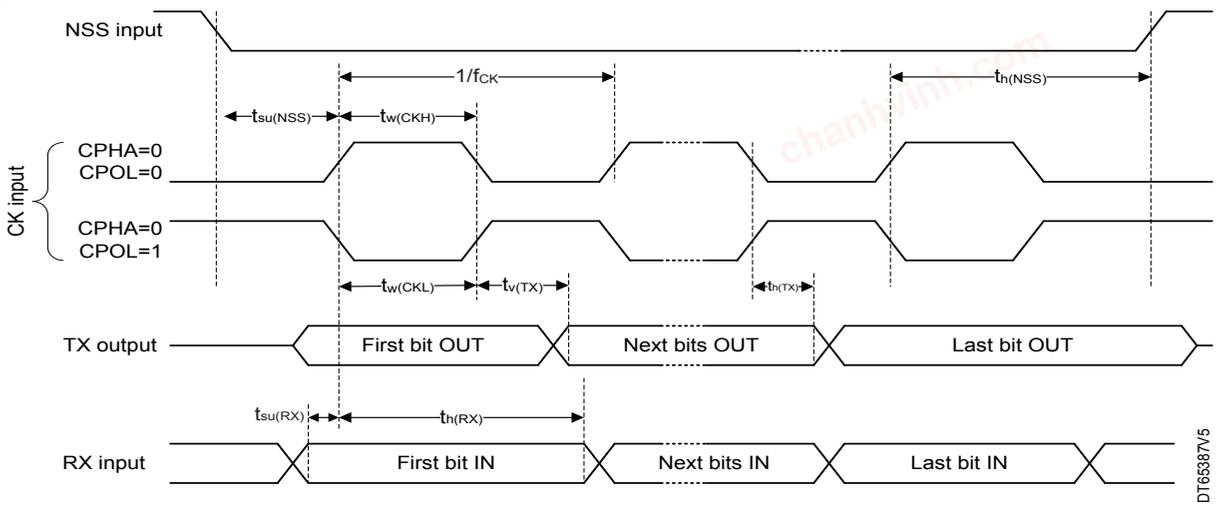


Figure 59. **USART timing diagram in SPI slave mode**



5.3.34 SPI characteristics

Unless otherwise specified, the parameters given in Table 121 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in Table 27.

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points done at 0.5 × V_{DD} level
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to Table 86. I/O static characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

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Table 121. SPI characteristics

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode,1.71 V ≤ V_{DDIOX} ≤ 3.6 V, Voltage range 1	-	-	48/33(1)	MHz
		Slave receiver mode, 1.71 V ≤ V_{DDIOX} ≤ 3.6 V, Voltage range 1	-	-	96	
		Slave mode transmitter/full duplex(3), 1.71 V ≤ V_{DDIOX} ≤ 3.6 V, Voltage range 1	-	-	33/25(2)	
		Slave mode transmitter/full duplex(3), 2.7 V ≤ V_{DDIOX} ≤ 3.6 V, voltage range 1	-	-	31	
		Master or slave mode, 1.71 V ≤ V_{DDIOX} ≤ 3.6 V, Voltage range 2	-	-	24/18.5(2)	
		Master or slave mode, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V(4)	-	-	15	
$t_{su(NSS)}$	NSS setup time	Slave mode	4 x T_{PCLK}	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 x T_{PCLK}	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode(5)	t_{SCK} - 1	t_{SCK}	t_{SCK} + 1	
$t_{su(MI)}$	Data input setup time	Master mode	3.5	-	-	
$t_{su(SI)}$		Slave mode	2.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	3	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	12	14.5	28	
$t_{dis(SO)}$	Data output disable time	Slave mode	7	14	28	
$t_{v(SO)}$	Data output valid time	Slave mode, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V, Voltage range 1	-	12	16	ns
		Slave mode, 1.71 V ≤ V_{DDIOX} < 2.7 V, Voltage range 1	-	12	15/20(2)	
		Slave mode, 1.71 V ≤ V_{DDIOX} ≤ 3.6 V, Voltage range 2	-	15	20.5/26.5(2)	
		Slave mode, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V(4)	-	19	22	
$t_{v(MO)}$		Master mode	-	0.5	1.5/7.5(6)	
$t_{h(SO)}$	Data output hold time	Slave mode	8.5	-	-	
		Slave mode, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V(4)	13	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. *When using PA5, PA9, PD1*
2. *When using PA11.*
3. *Maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which must fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.*
4. *The SPI is mapped on port G I/Os, that is supplied by V_{DDIO2} specified down to 1.08 V. The SPI is tested at this value.*
5. *t_{SCK} = $t_{spi_ker_ck}$ × baud rate prescaler.*
6. *When using PA12/PB15.*

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Figure 60. **SPI timing diagram - slave mode and CPHA = 0**

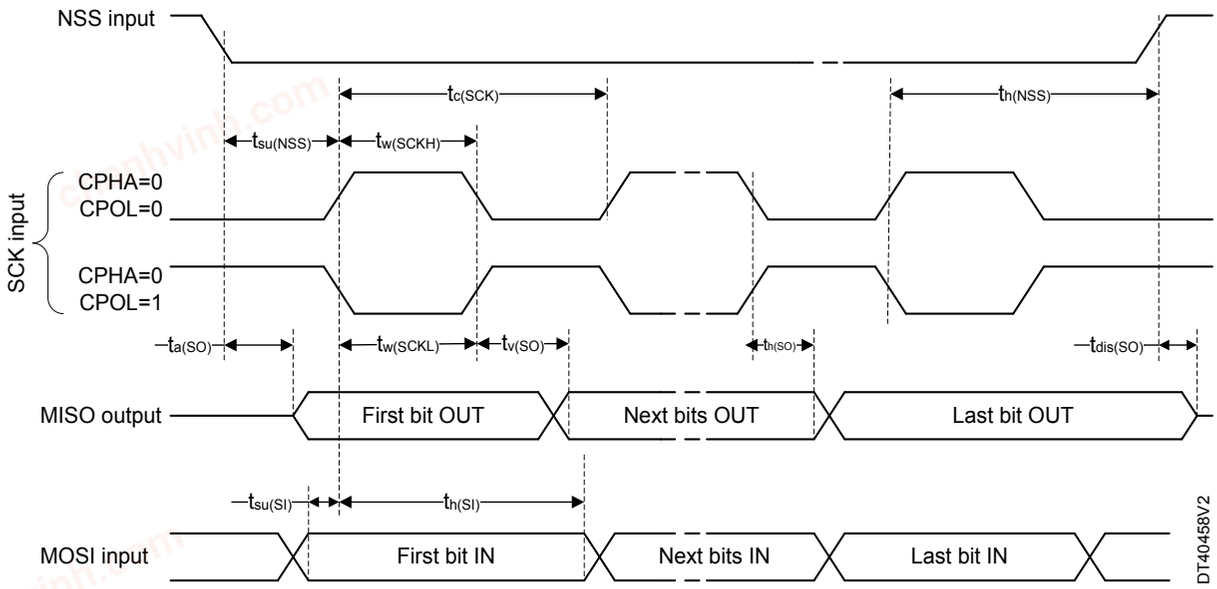
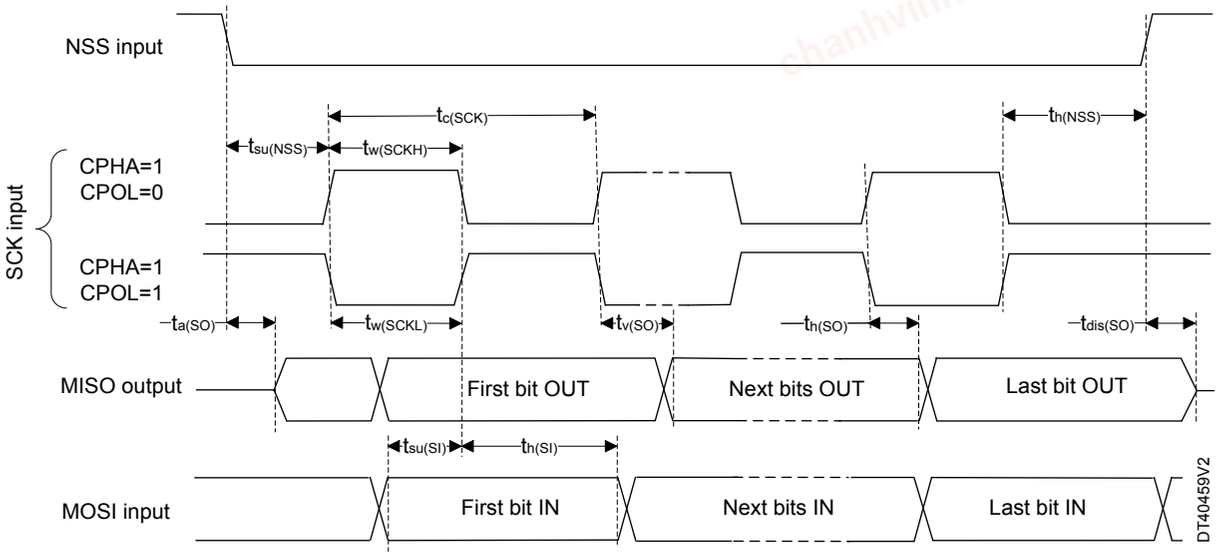


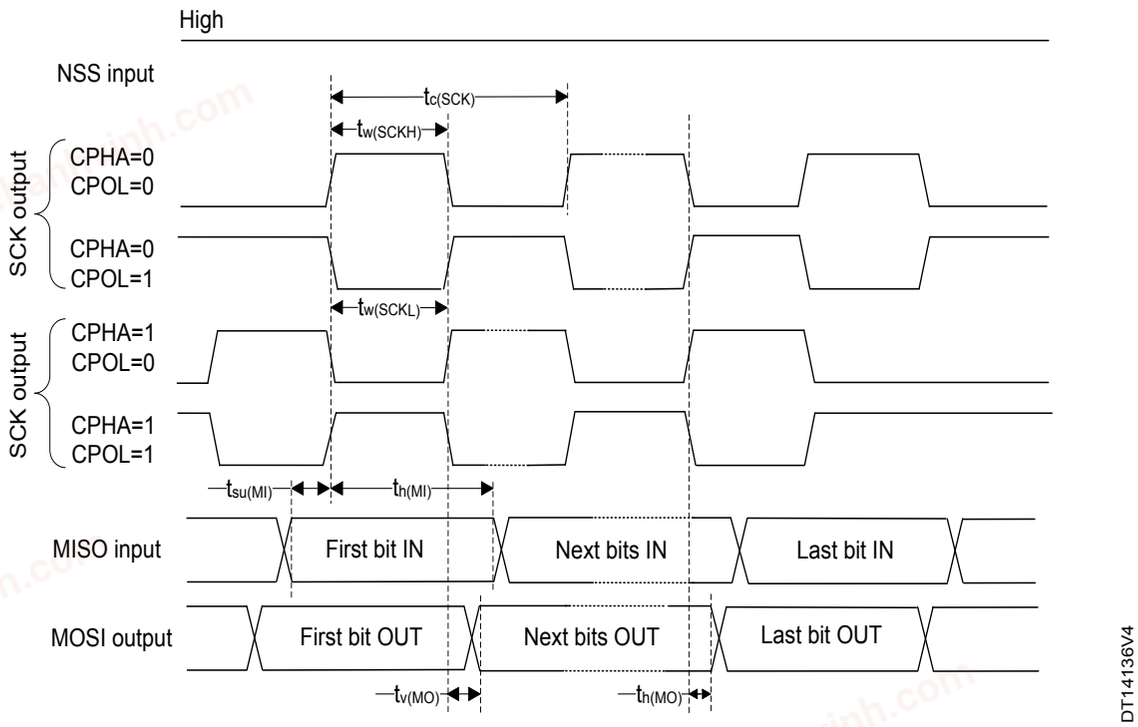
Figure 61. **SPI timing diagram - slave mode and CPHA = 1**



Note: Measurement points are done at 0.3 V_{DD} and 0.7 V_{DD} levels.

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Figure 62. **SPI timing diagram - master mode**



Note: Measurement points are done at 0.3 V_{DD} and 0.7 V_{DD} levels.

5.3.35 SAI characteristics

Unless otherwise specified, the parameters given in Table 122 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized inTable 27, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points done at 0.5 × V_{DD} level
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V
- Voltage scaling range 1

Refer to Table 86. I/O static characteristics for more details on the input/output alternate function characteristics (SCK, SD, FS).

Table 122. **SAI characteristics**

Evaluated by characterization. Not tested in production.

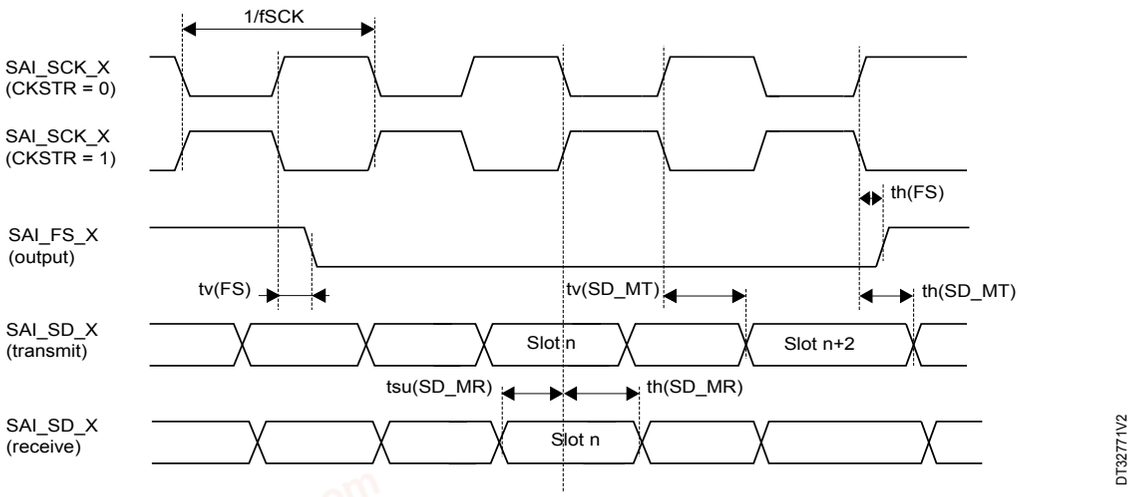
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI main clock output	-	-	50	MHz
f_{SCK}	SAI clock frequency(1)	Master transmitter, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	28.5	
		Master transmitter, 1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	28.5/19.5(2)(3)	
		Master receiver, 1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	31/21.5(3)	
		Slave transmitter, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	30	
		Slave transmitter, 1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	30/20.5(2)	
		Slave receiver, 1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	50	

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Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(FS)}$	FS valid time	Master mode, 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	16	ns
		Master mode 1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	16/23(3)	
$t_{h(FS)}$	FS hold time	Master mode	8	-	
$t_{su(FS)}$	FS setup time	Slave mode	1.5	-	
$t_{h(FS)}$	FS hold time	Slave mode	1	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD_B_SR)}$		Slave receiver	2	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	1.5	-	
$t_{h(SD_B_SR)}$		Slave receiver	1	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge), 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	16.5	
		Slave transmitter (after enable edge), 1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	16.5/24(2)	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7.5	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge), 2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	17.5	
		Master transmitter (after enable edge), 1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	17.5/25.5(2)	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	7	-	

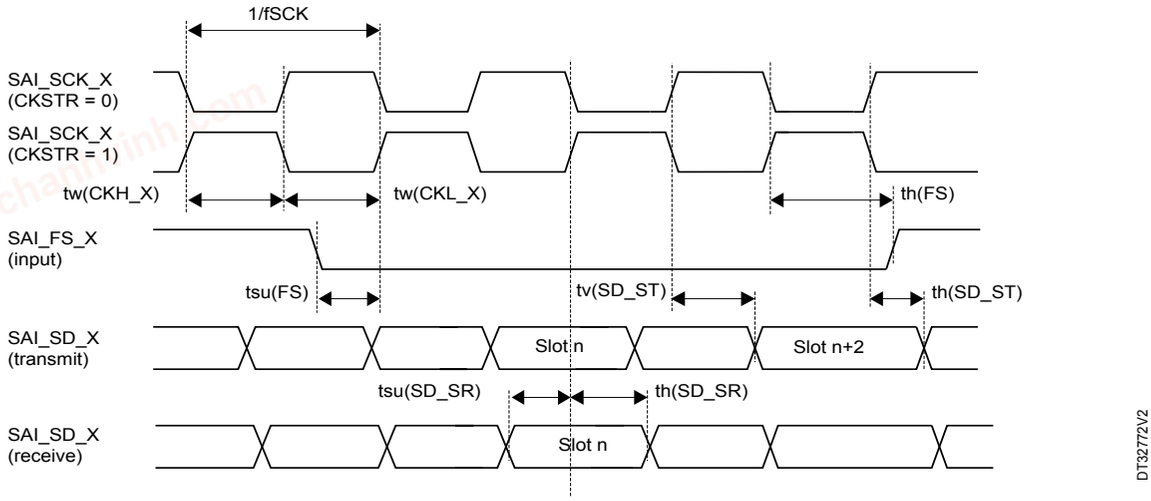
1. *APB clock frequency that must be at least twice SAI clock frequency.*
2. *When using PE6/PA10/PA13/PE7*
3. *When using PE4/PA9/PA14*

Figure 63. SAI master timing diagram



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Figure 64. **SAI slave timing digram**



5.3.36 USB_FS characteristics

Table 123. **USB_FS characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating supply voltage	-	3.0(1)	-	3.6	V
R_{PUI}	Embedded USB_DP pullup value during idle	-	900	-	1575	Ω
R_{PUR}	Embedded USB_DP pullup value during reception	-	1425	-	3090	
Z_{DRV}	Output driver impedance(2)	High and low driver	28	36	44	

1. *USB functionality is ensured down to 2.7 V, but some USB electrical characteristics are degraded in 2.7 to 3.0 V range.*
2. *No external termination series resistors are required on USB_DP (D+) and USB_DM (D-). The matching impedance is already included in the embedded driver.*

5.3.37 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in Table 124 and Table 125 are derived from tests performed under the ambient temperature, f_{HCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 27, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points done at 0.5 × V_{DD} level

Refer to Table 86. I/O static characteristics for more details on the input/output characteristics.

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Table 124. JTAG characteristics

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{TCK}	TCK clock frequency	1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	-	34	MHz
$ti_{su(TMS)}$	TMS input setup time	-	4	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	-	0.5	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1.5	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	0.5	-	-	
$t_{ov(TDO)}$	TDO output valid time	1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	13.5	14.5	
$t_{oh(TDO)}$	TDO output hold time	-	8.5	-	-	

Figure 65. JTAG timing diagram

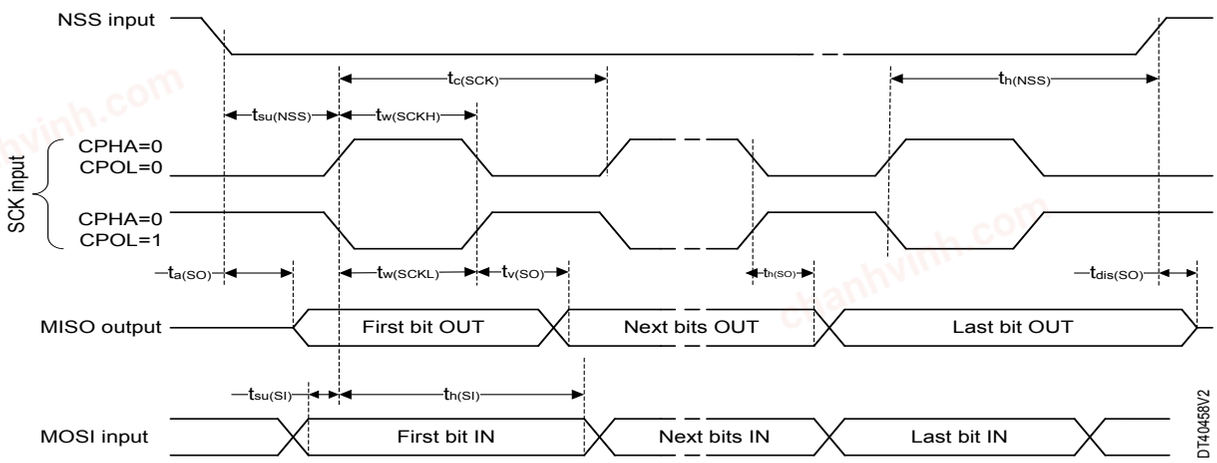


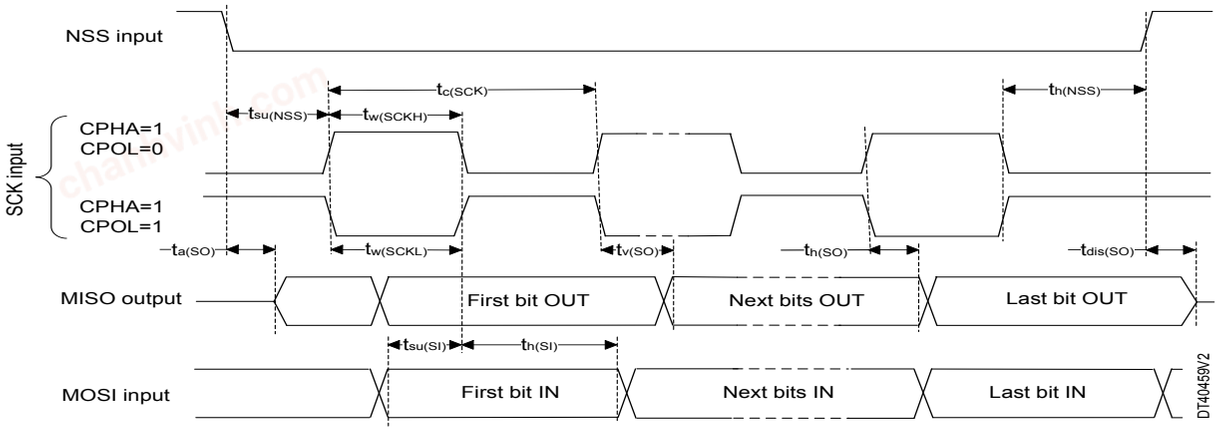
Table 125. SWD characteristics

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{SWCLK}	SWCLK clock frequency	2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	-	66	MHz
		1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	-	38	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time	-	0.5	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	2.7 V ≤ V_{DDIOX} ≤ 3.6 V	-	11.5	15	
		1.71 V ≤ V_{DDIOX} ≤ 3.6 V	-	11.5	26	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	9.5	-	-	

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Figure 66. **SWD timing diagram**



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6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

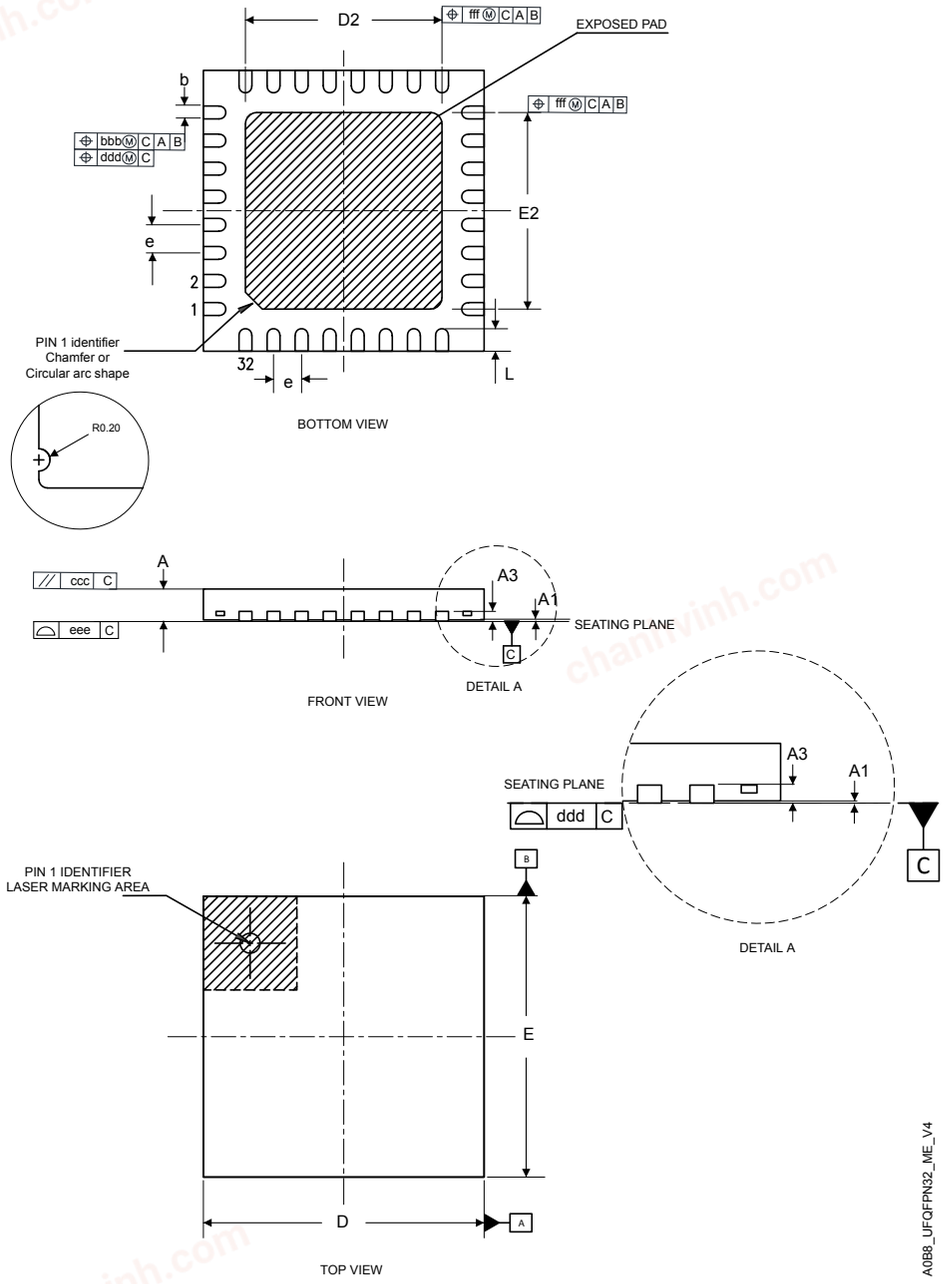
A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

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6.2 UFQFPN32 package information (A0B8)

This UFQFPN is a 32 pins, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package.

Figure 67. UFQFPN32 - Outline



1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.*

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Table 126. UFQFPN32 - Mechanical data

Symbol	millimeters(1)			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A(3)(4)	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1(5)	0.00	-	0.05	0.000	-	0.0020
A3(6)	-	0.15	-	-	0.0060	-
b(7)	0.18	0.25	0.30	0.0071	0.010	0.0118
D(8)(9)		5.00 BSC			0.1969 BSC	
D2	3.50	3.60	3.70	0.139	0.143	0.147
E(8)(9)		5.00 BSC			0.1969 BSC	
E2	3.50	3.60	3.70	0.139	0.143	0.147
e(9)	-	0.50	-	-	0.02	-
N(10)			32			
K	0.15	-	-	0.006	-	-
L	0.30	-	0.50	0.0119	-	0.0199
R	0.09	-	-	0.004	-	-

1. *All dimensions are in millimetres. Dimensioning and tolerancing schemes are conform to ASME Y14.5M-2018 except European .*
2. *Values in inches are converted from mm and rounded to 4 decimal digits.*
3. *UFQFPN stands for Ultra thin Fine pitch Quad Flat Package No lead: A ≤ 0.60mm / Fine pitch e ≤ 1.00mm.*
4. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
5. *A1 is the vertical distance from the bottom surface of the plastic body to the nearest metallized package feature.*
6. *A3 is the distance from the seating plane to the upper surface of the terminals.*
7. *Dimension b applies to metallized terminal. If the terminal has the optional radius on the other end of the terminal, the dimension b must not be measured in that radius area.*
8. *Dimensions D and E do not include mold protrusion, not to exceed 0,15mm.*
9. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to Table 127*
10. *N represents the total number of terminals.*

Table 127. Tolerance of form and position

Symbol(1)	Tolerance of form and position(2) In millimeters	Tolerance of form and position(3) In inches
aaa	0.15	0.006
bbb	0.10	0.004
ccc	0.10	0.004
ddd	0.05	0.002
eee	0.10	0.004
fff	0.10	0.004

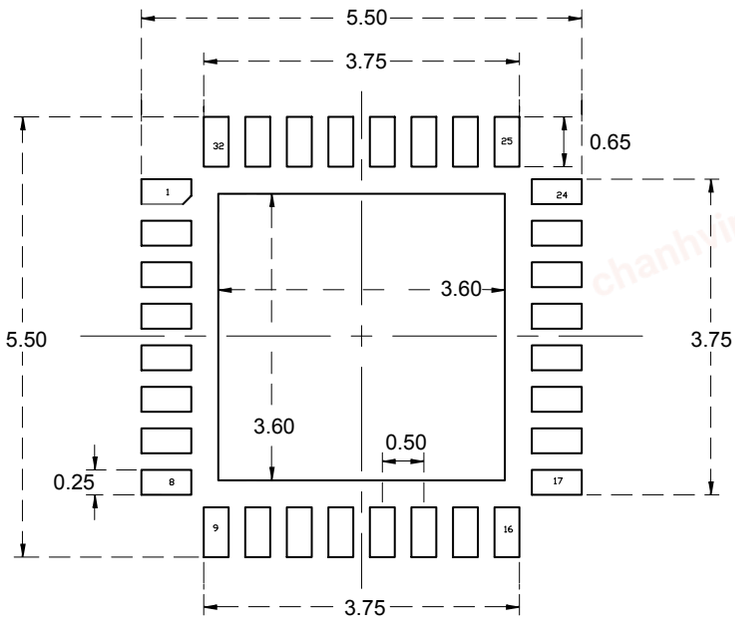
1. *For the tolerance of form and position definitions see Table 128.*
2. *All dimensions are in millimetres. Dimensioning and tolerancing schemes are conform to ASME Y14.5M-2018 except European .*
3. *Values in inches are converted from mm and rounded to 4 decimal digits.*

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Table 128. Tolerance of form and position symbol definition

Symbol	Definition
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centres of the profile zones are defined by the basic dimensions D and E.
bbb	The tolerance that controls the position of the terminals with respect to Datums A and B. The centre of the tolerance zone for each terminal is defined by basic dimension e as related to datums A and B.
ccc	The tolerance located parallel to the seating plane in which the top surface of the package must be located.
ddd	The tolerance that controls the position of the terminals to each other. The centres of the profile zones are defined by basic dimension e.
eee	The unilateral tolerance located above the seating plane wherein the bottom surface of all terminals must be located = coplanarity
fff	The tolerance that controls the position of the exposed metal heat feature. The centre of the tolerance zone is the data defined by the centrelines of the package body

Figure 68. UFQFPN32 - Footprint example



1. *Dimensions are expressed in millimeters.*

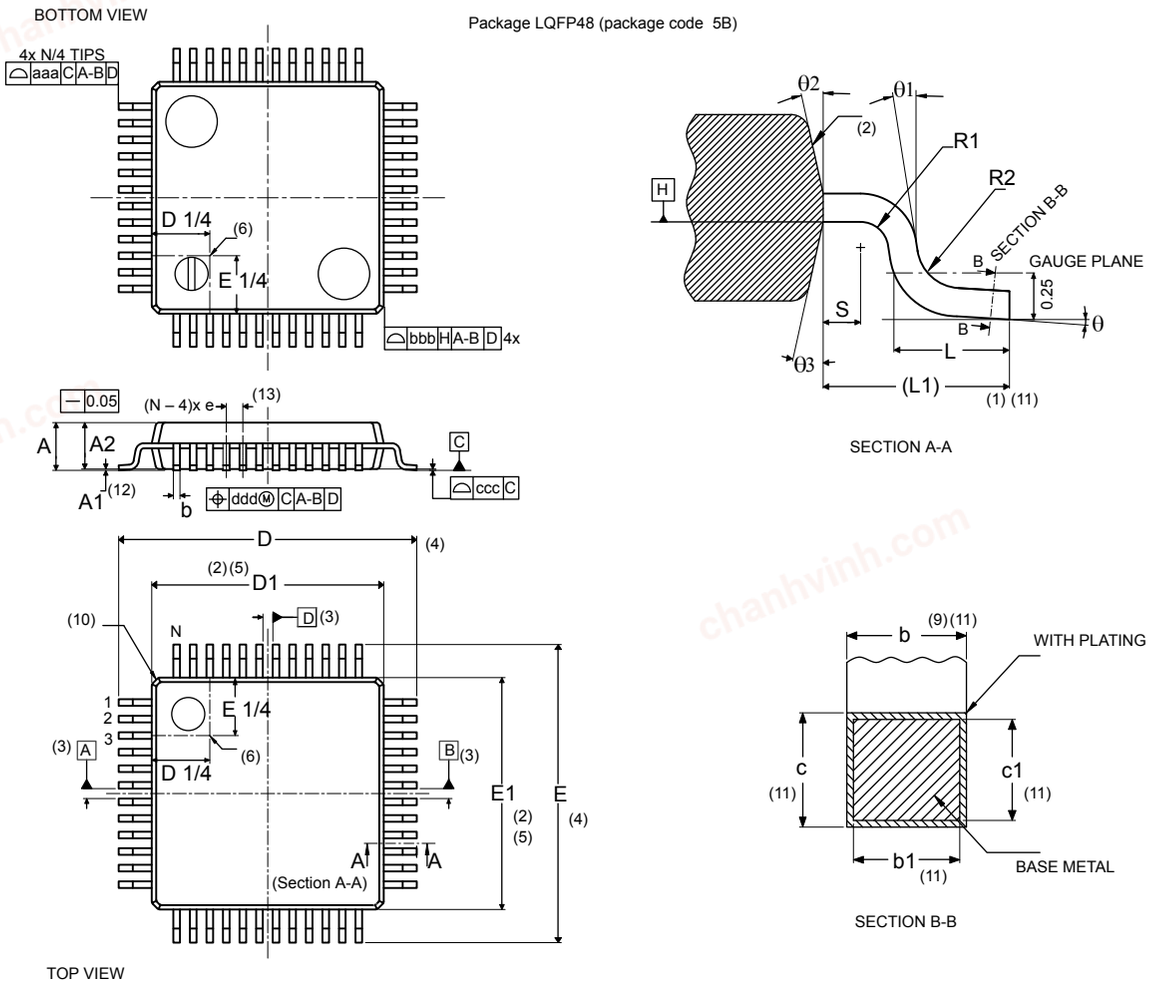
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6.3 LQFP48 package information (5B)

This LQFP is a 48-pins, 7 x 7 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 69. LQFP48- Outline(15.)



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Table 129. **LQFP48 - Mechanical data**

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	9.00 BSC			0.3543 BSC		
D1[4.][5.]	7.00 BSC			0.2756 BSC		
E[4.]	9.00 BSC			0.3543 BSC		
E1[4.][5.]	7.00 BSC			0.2756 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13.]	48					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.][7.]	0.20			0.0079		
bbb[1.][7.]	0.20			0.0079		
ccc[1.][7.]	0.08			0.0031		
ddd[1.][7.]	0.08			0.0031		

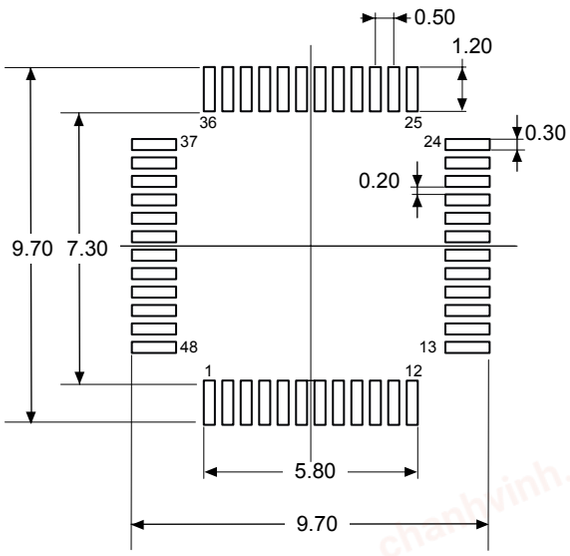
Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

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10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits
15. Drawing is not to scale.

Figure 70. LQFP48 - Footprint example



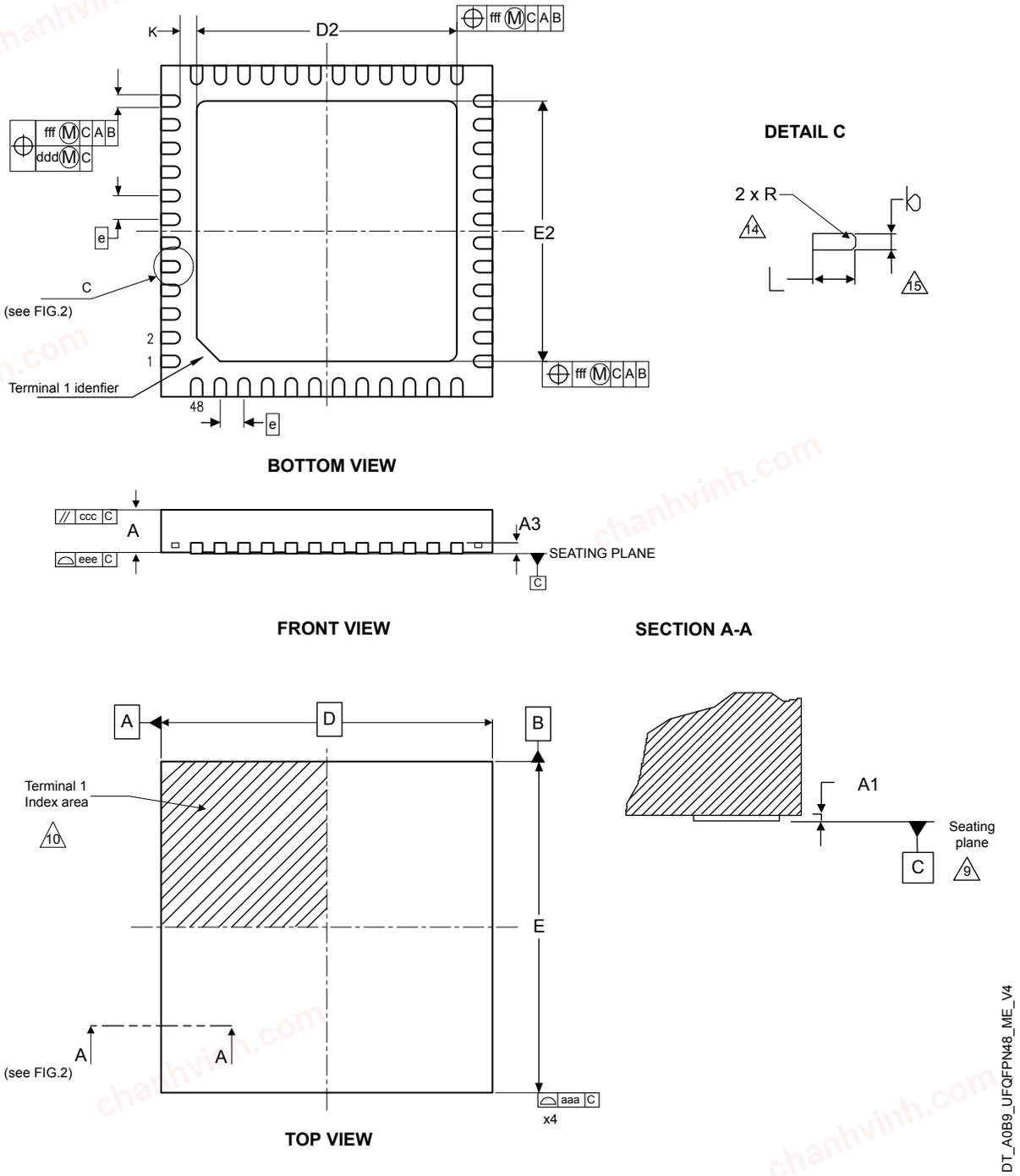
1. Dimensions are expressed in millimeters.

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6.4 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 71. UFQFPN48 - Outline



1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the under side of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.*

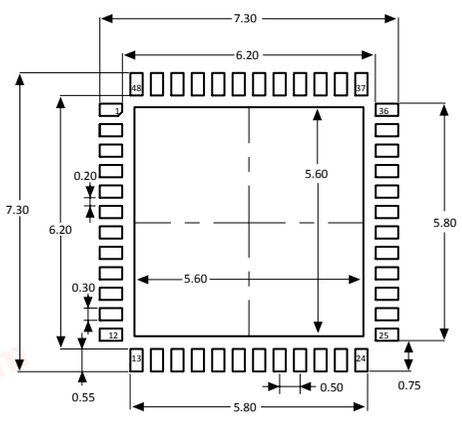
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Table 130. UFQFPN48 - Mechanical data

Symbol	Millimeters			Inches (1)		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	-	0.05	0.0000	-	0.0020
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D(2)		7.00 BSC			0.2756 BSC	
D2(3)	5.50	5.60	5.70	0.2165	0.2205	0.2244
E(2)		7.00 BSC			0.2756 BSC	
E2(3)	5.50	5.60	5.70	0.2165	0.2205	0.2244
e		0.50 BSC			0.0197 BSC	
N			48			
L	0.30	-	0.50	0.0118	-	0.0197
R	0.10	-	-	0.0039	-	-
aaa		0.15			0.0059	
bbb		0.10			0.0039	
ccc		0.10			0.0039	
ddd		0.05			0.0020	
eee		0.08			0.0031	
fff		0.10			0.0039	

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.*
3. *Dimensions D2 and E2 are not in accordance with JEDEC.*

Figure 72. UFQFPN48 - Footprint example



DT_A0B9_UFQFPN48_FP_V3

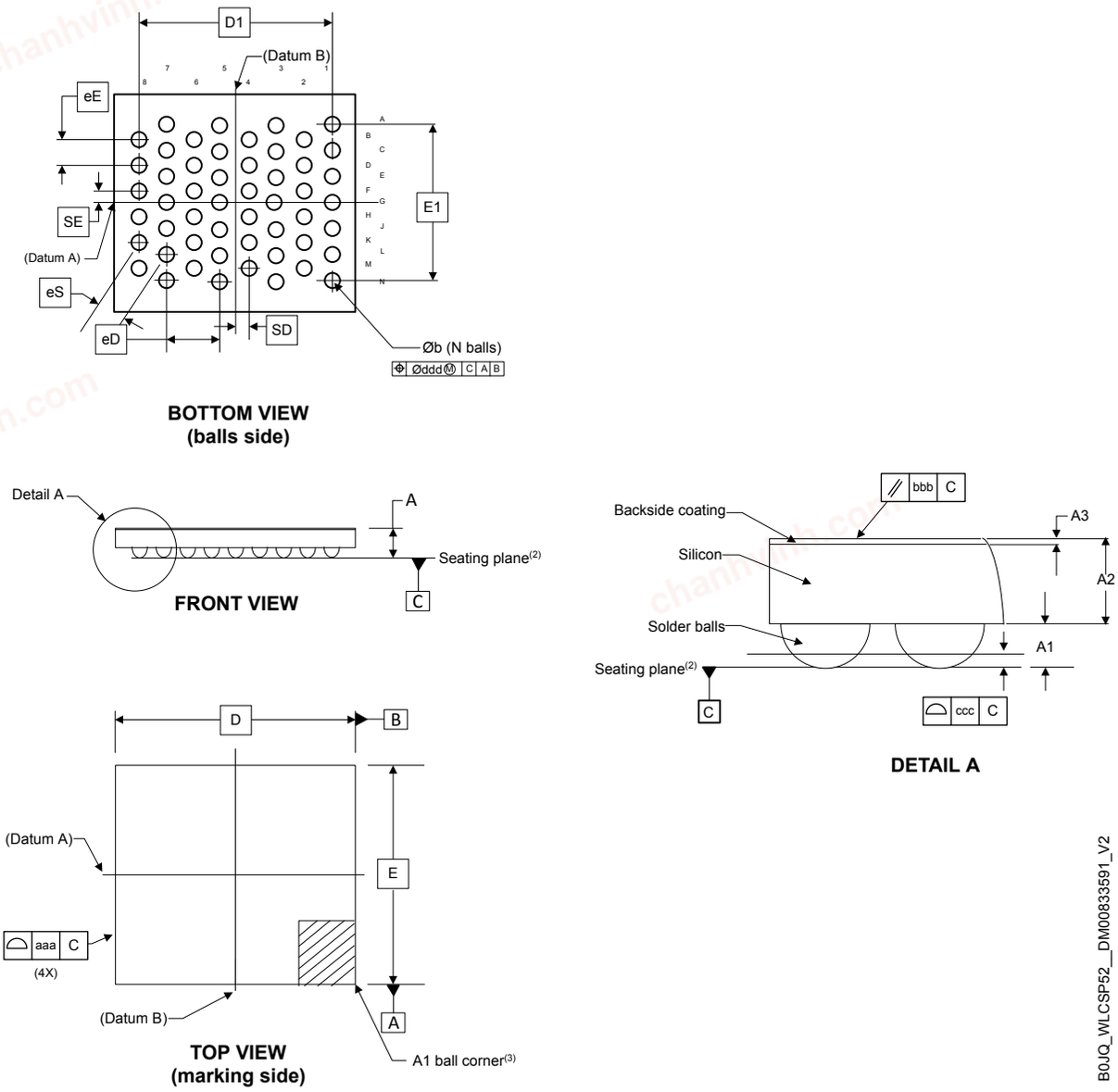
1. *Dimensions are expressed in millimeters.*

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6.5 WLCSP52 package information (B0JQ)

This WLCSP is a 52-ball, 3.17 x 3.11 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 73. WLCSP52 - Outline



1. *Drawing is not to scale.*
2. *Datum C (seating plane) is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.*
3. *The A1 corner is identified on the top surface of the package by using a marking or a physical feature. A distinguish feature is allowable on the bottom surface of the package to identify the A1 corner. Exact shape of each corner is optional.*

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Table 131. **WLCSP52 - Mechanical data**

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	-	-	0.58	-	-	0.0228
A1(3)	0.14	-	-	0.0055	-	-
A2	-	0.38	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b(4)	0.23	0.25	0.28	0.0091	0.0098	0.0110
D(5)	3.17 BSC			0.1248 BSC		
D1(5)	2.43 BSC			0.0957 BSC		
E(5)	3.11 BSC			0.1224 BSC		
E1(5)	2.40 BSC			0.0945 BSC		
eD(5)(6)	0.69 BSC			0.0272 BSC		
eE(5)(6)	0.40 BSC			0.0157 BSC		
eS(5)(6)	0.40 BSC			0.0157 BSC		
N(7)	52					
SD(5)(8)	0.173 BSC			0.0068 BSC		
SE(5)(8)	0.200 BSC			0.0079 BSC		
aaa(9)	0.02			0.0008		
bbb(9)	0.06			0.0024		
ccc(9)	0.03			0.0012		
ddd(9)	0.015			0.0006		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height A is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to Datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances, refer to form and position table. On the drawing, these dimensions are framed. For the tolerances, refer to form and position values.*
6. *e represents the solder balls grid pitch(es).*
7. *N represents the total number of balls.*
8. *Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.*
9. *Tolerance of form and position drawing*

6.5.1 Device marking for WLCSP52

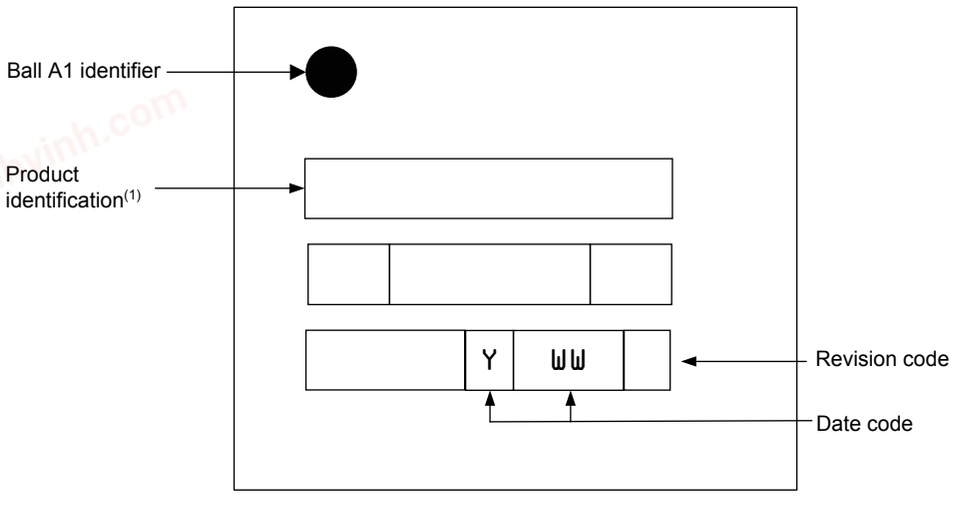
The following figure gives an example of topside marking versus ball A1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

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Figure 74. **WLCSP52 Device marking**



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

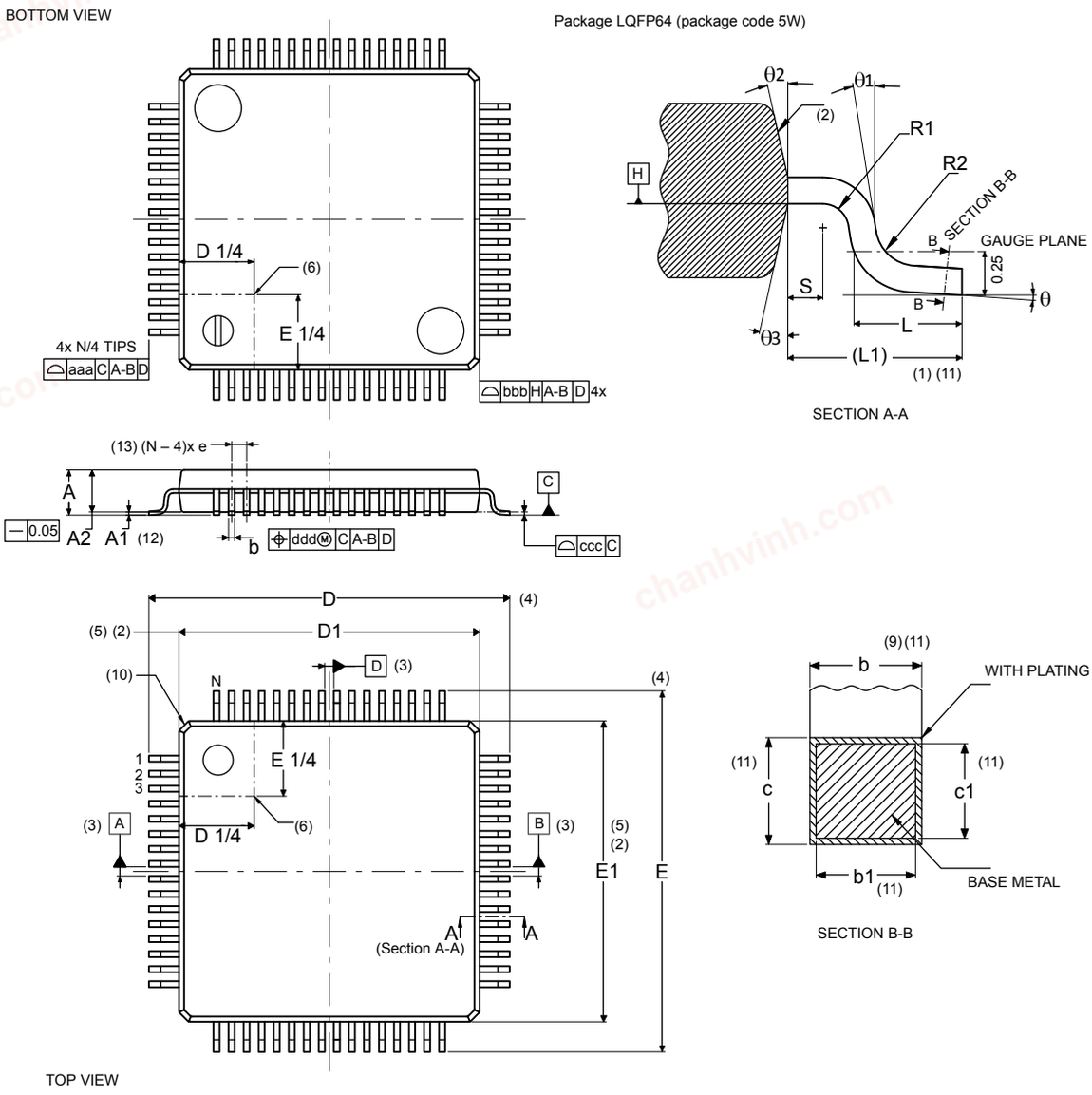
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6.6 LQFP64 package information (5W)

This is a 64-pins, 10 x 10 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 75. LQFP64 - Outline(15.)



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Table 132. **LQFP64 - Mechanical data**

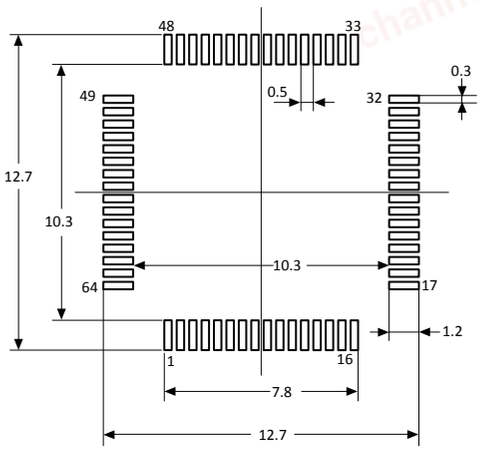
Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	00067	0.0079	0.0091
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	12.00 BSC			0.4724 BSC		
D1[2.][5.]	10.00 BSC			0.3937 BSC		
E[4.]	12.00 BSC			0.4724 BSC		
E1[2.][5.]	10.00 BSC			0.3937 BSC		
e	0.500 BSC			0.0197 BSC		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
N[13.]	64					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]	0.20			0.0079		
bbb[1.]	0.20			0.0079		
ccc[1.]	0.08			0.0031		
ddd[1.]	0.08			0.0031		

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Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 76. LQFP64 - Footprint example



1. *Dimensions are expressed in millimeters.*

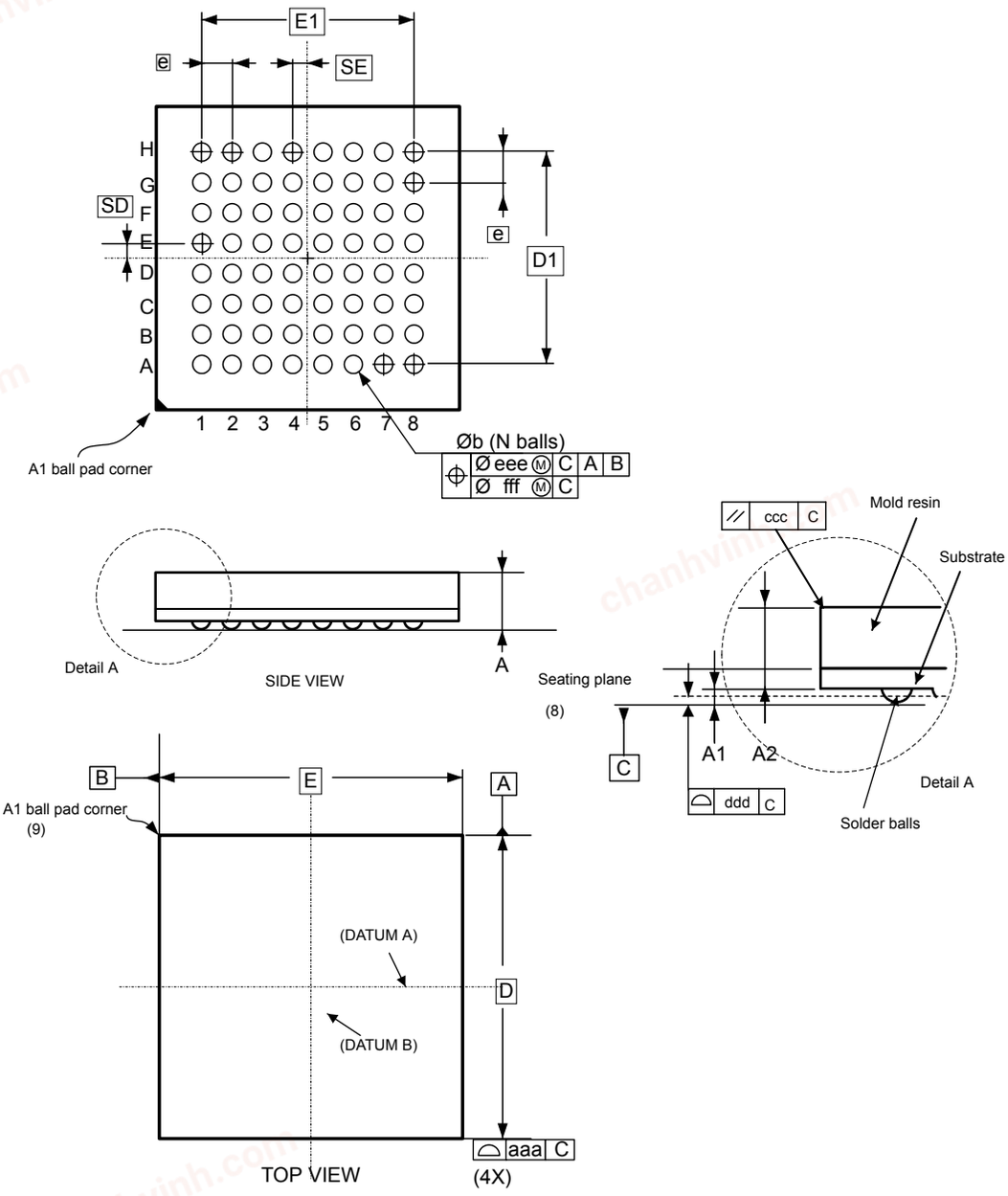
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6.7 UFBGA64 package information (A019)

This UFBGA is a 64-ball, 5 x 5 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 77. UFBGA64 - Outline(13.)



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Table 133. **UFBGA64 - Mechanical data**

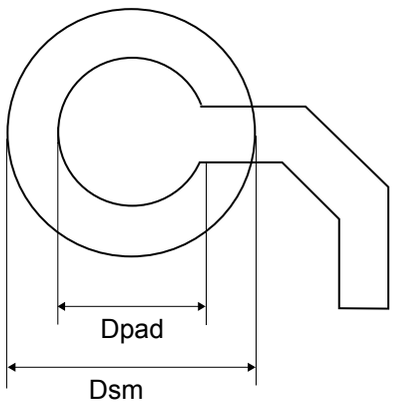
Symbol	millimeters[1.]			inches [12.]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2.][3.]	-	-	0.60	-	-	0.0236
A1[4.]	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-
b[5.]	0.23	0.28	0.33	0.0090	0.0110	0.0130
D[6.]	5.00 BSC			0.1969 BSC		
D1	3.50 BSC			0.1378 BSC		
E	5.00 BSC			0.1969 BSC		
E1	3.50 BSC			0.1378 BSC		
e[9.]	0.50 BSC			0.0197 BSC		
N[10.]	64					
SD[11.]	0.25 BSC			0.0098 BSC		
SE[11.]	0.25 BSC			0.0098 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.05			0.0020		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ultra profile fine pitch ball grid array: 0.50 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale

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Figure 78. **UFBGA64 - Footprint example**



DT_BGA_WLCSP_FT_V1

Table 134. **UFBGA64 - Recommended PCB design rules (0.50 mm pitch BGA)**

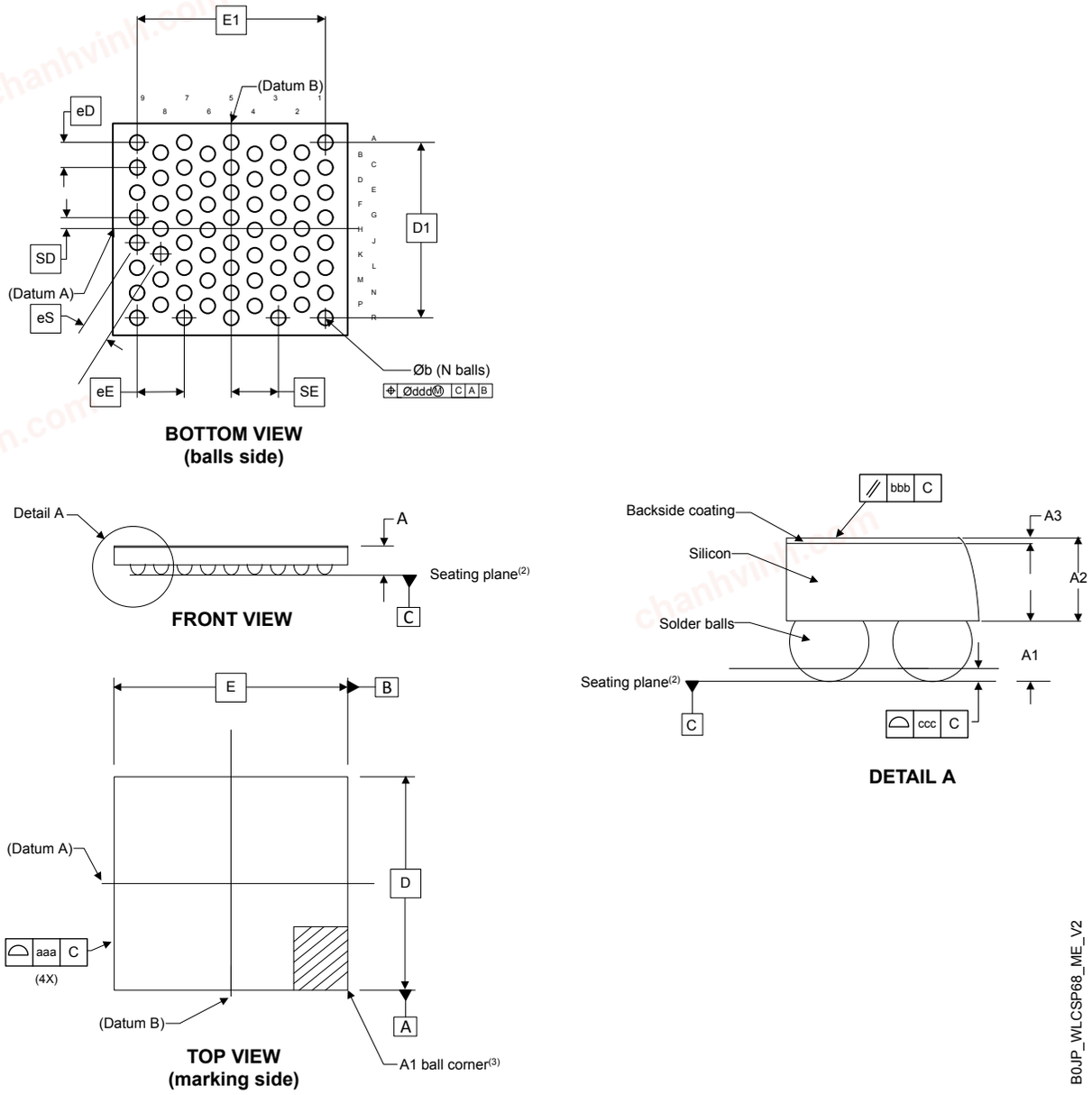
Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm aperture diameter
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

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6.8 WLCSP68 package information (B0JP)

This WLCSP is a 68-ball, 3.11 x 3.17 mm, 0.35 mm pitch, wafer level chip scale package.

Figure 79. WLCSP68 - Outline



1. *Drawing is not to scale*
2. *Datum C (seating plane) is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.*
3. *The A1 corner is identified on the top surface of the package by using a marking or a physical feature. A distinguish feature is allowable on the bottom surface of the package to identify the A1 corner. Exact shape of each corner is optional.*

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Table 135. **WLCSP68 - Mechanical data**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.58	-	-	0.0228
A1[3]	0.12	-	-	0.0047	-	-
A2	-	0.38	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b[4]	0.20	0.23	0.25	0.0079	0.0091	0.0098
D[5]	3.11 BSC			0.1224 BSC		
D1[5]	2.45 BSC			0.0965 BSC		
E[5]	3.17 BSC			0.1248 BSC		
E1[5]	2.43 BSC			0.0957 BSC		
eD[5][6]	0.35 BSC			0.0138 BSC		
eE[5][6]	0.61 BSC			0.0240 BSC		
N[7]	68					
SD[5][8]	0.175 BSC			0.0069 BSC		
SE[5][8]	0.606 BSC			0.0239		
aaa[9]	0.02			0.0008		
bbb[9]	0.06			0.0024		
ccc[9]	0.03			0.0012		
ddd[9]	0.015			0.0006		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height A is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to Datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances, refer to form and position table. On the drawing, these dimensions are framed. For the tolerances, refer to form and position values.*
6. *e represents the solder balls grid pitch(es).*
7. *N represents the total number of balls.*
8. *Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.*
9. *Tolerance of form and position drawing*

6.8.1 Device marking for WLCSP68

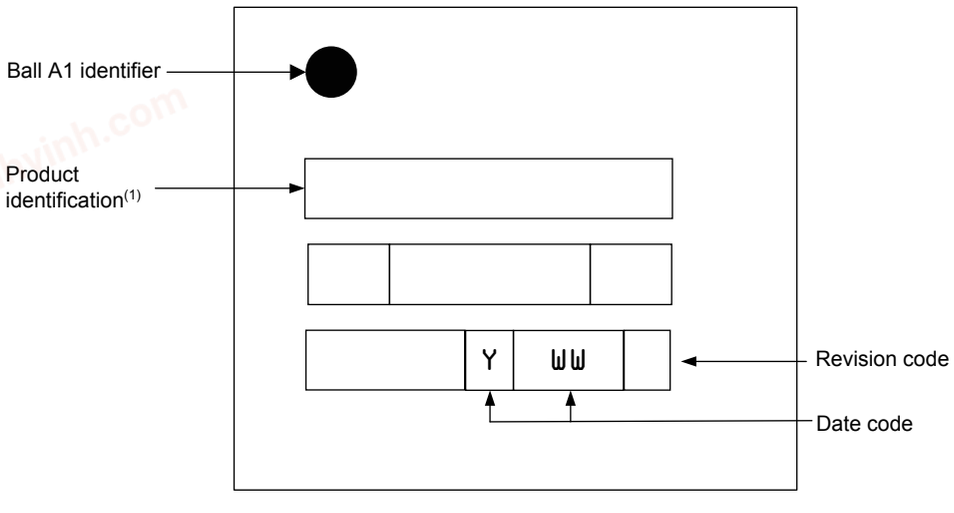
The following figure gives an example of topside marking versus ball A1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

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Figure 80. **WLCSP68 Device marking**



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

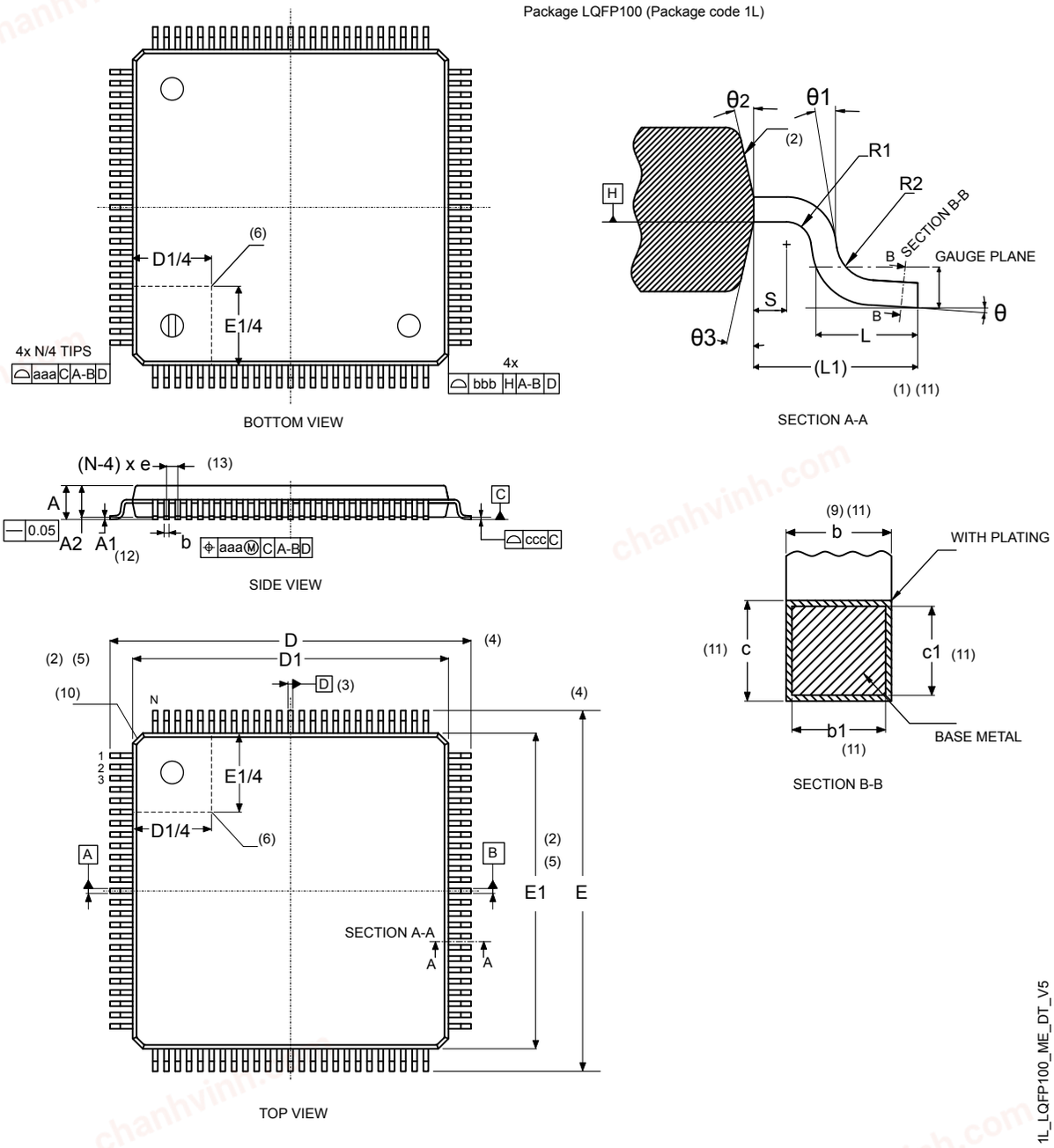
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6.9 LQFP100 package information (1L)

This LQFP is a 100-pin, 14 x 14 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 81. LQFP100 - Outline(15.)



1L_LQFP100_ME_DT_V5

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Table 136. **LQFP100 - Mechanical data**

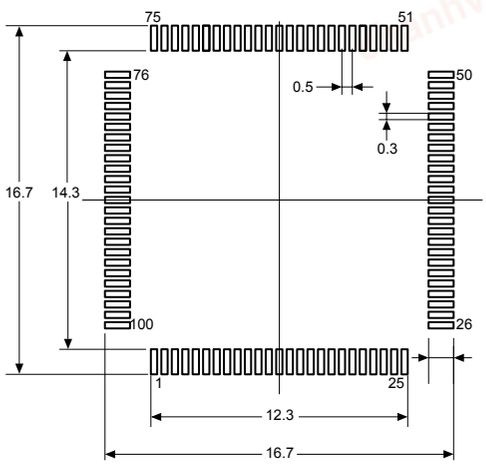
Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	16.00 BSC			0.6299 BSC		
D1[2.][5.]	14.00 BSC			0.5512 BSC		
E[4.]	16.00 BSC			0.6299 BSC		
E1[2.][5.]	14.00 BSC			0.5512 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1[1.][11.]	-	1.00	-	-	0.0394	-
N[13.]	100					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]	0.20			0.0079		
bbb[1.]	0.20			0.0079		
ccc[1.]	0.08			0.0031		
ddd[1.]	0.08			0.0031		

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Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion is allowed inwards the leads.
9. Dimension “b” does not include a dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. The exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 82. LQFP100 - Footprint example



1. *Dimensions are expressed in millimeters.*

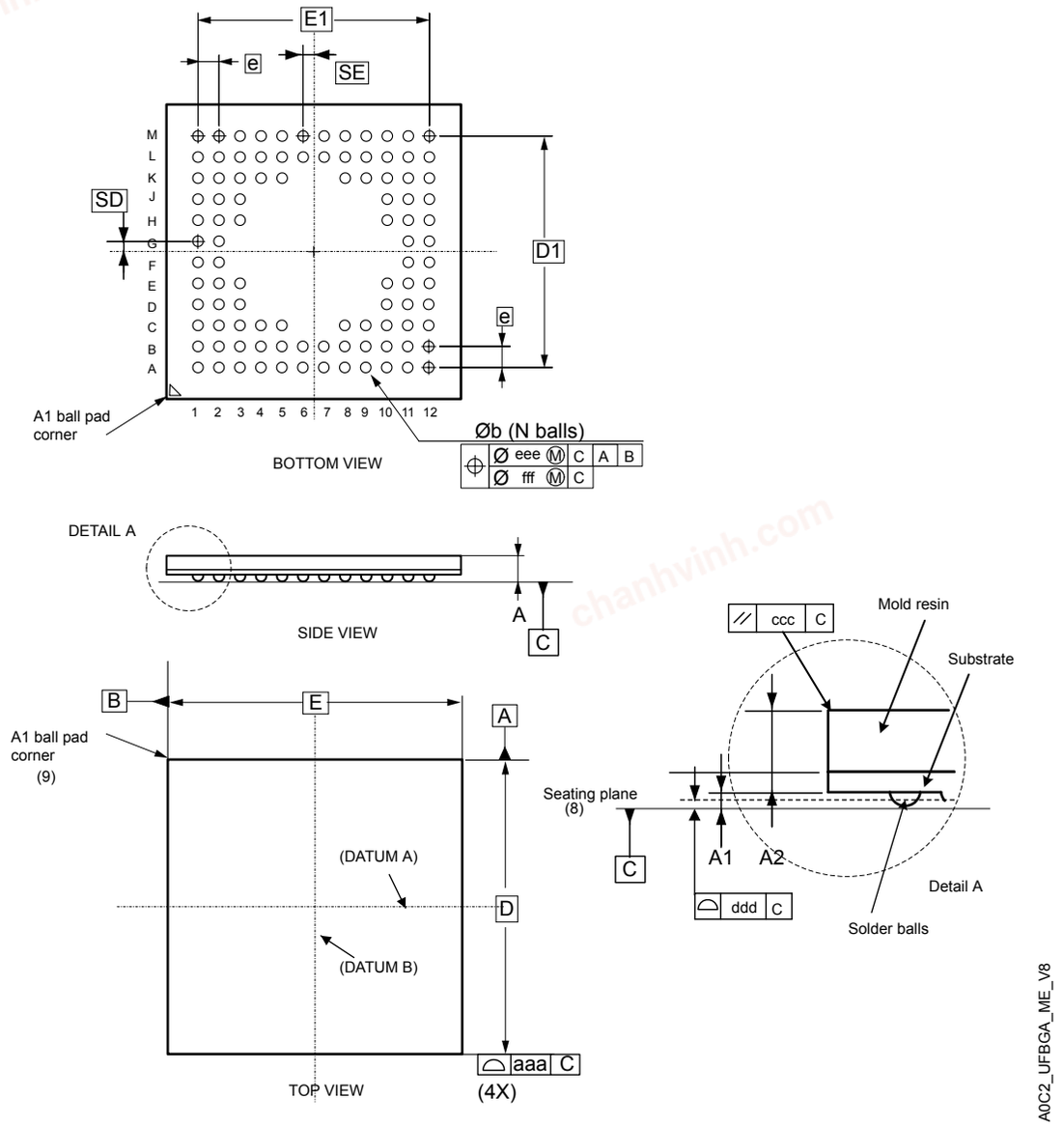
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6.10 UFBGA100 package information (A0C2)

This UFBGA is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 83. UFBGA100 - Outline(13.)



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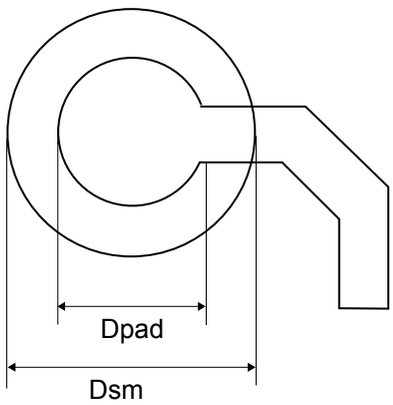
Table 137. **UFBGA100 - Mechanical data**

Symbol	millimeters[1.]			inches [12.]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2.][3.]	-	-	0.60	-	-	0.0236
A1[4.]	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-
b[5.]	0.23	0.28	0.33	0.0090	0.0110	0.0130
D	7.00 BSC			0.2756 BSC		
D1	5.50 BSC			0.2165 BSC		
E	7.00 BSC			0.2756 BSC		
E1	5.50 BSC			0.2165 BSC		
e[9.]	0.50 BSC			0.0197 BSC		
N[10.]	100					
SD[11.]	0.25 BSC			0.0098 BSC		
SE[11.]	0.25 BSC			0.0098 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.05			0.0020		

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ultra profile fine pitch ball grid array: 0.50 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

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Figure 84. **UFBGA100 - Footprint example**



DT_BGA_WLCSP_FT_V1

Table 138. **UFBGA100 - Recommended PCB design rules (0.50 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm aperture diameter
Stencil thickness	Between 0.100 mm and 0.125 mm

6.11 Package thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the following equation:

$$T_J \max = T_A \max + \left(P_D \max \times \Theta_{JA}\right)$$

where:

- T_A max is the maximum ambient temperature in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W.
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max:

$$P_D \max = P_{INT} \max + P_{I/O} \max$$

- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

$$P_{I/O} \max = \sum\left(V_{OL} \times I_{OL}\right) + \sum\left(\left(V_{DDIOx} - V_{OH}\right)\right) \times I_{OH}$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

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Table 139. **Package thermal characteristics**

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	UFQFPN32 5 × 5 mm	36	°C/W
		LQFP48 7 × 7 mm	49.4	
		UFQFPN48 7 × 7 mm	29.0	
		WLCSP52	-	
		LQFP64 10 × 10 mm	42.6	
		UFBGA64 7 × 7 mm	-	
		WLCSP68	-	
		LQFP100 - 14 × 14 mm	36.7	
		UFBGA100 7 × 7 mm	-	
Θ_{JB}	Thermal resistance junction-board	UFQFPN32 5 × 5 mm	17.7	
		LQFP48 7 × 7 mm	26.8	
		UFQFPN48 7 × 7 mm	13.4	
		WLCSP52	-	
		LQFP64 10 × 10 mm	25.0	
		UFBGA64 7 × 7 mm	-	
		WLCSP68	-	
		LQFP100 - 14 × 14 mm	22.6	
		UFBGA100 7 × 7 mm	-	
Θ_{JC}	Thermal resistance junction-top case	UFQFPN32 5 × 5 mm	13.9	
		LQFP48 7 × 7 mm	13.0	
		UFQFPN48 7 × 7 mm	9.7	
		WLCSP52	-	
		LQFP64 10 × 10 mm	10.9	
		UFBGA64 7 × 7 mm	-	
		WLCSP68	-	
		LQFP100 - 14 × 14 mm	9.0	
		UFBGA100 7 × 7 mm	-	

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7 Ordering information

Example: STM32 U 385 V G T 6 Q TR

Device family

STM32 = Arm®-based 32-bit microcontroller

Product type

U = Ultra-low-power

Device subfamily

385 = STM32U385xx with AES hardware encryption

Pin count

K = 32 pins

C = 48/52 balls/pins

R = 64/68 balls/pins

V = 100 balls/pins

Flash memory size

G = 1 Mbyte

Package

T = LQFP

U = UFQFPN

I = UFBGA

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85°C (105 °C junction)

7 = Industrial temperature range, –40 to 105°C (110 °C junction)

Dedicated pinout

Q = Dedicated pinout including SMPS step-down converter

G = Dedicated pinout including SMPS step-down converter and GPIO port G

Packing

TR = Tape and reel

xxx = Programmed parts

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

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Revision history

Table 140. **Document revision history**

Date	Revision	Changes
24-Feb-2025	1	Initial release.
28-Feb-2025	2	Updated Section 2: Description.

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