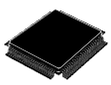
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STM32U083xC

Datasheet

Ultra-low-power Arm® Cortex®-M0+ 32-bit MCU, 256-Kbyte flash memory, 40-Kbyte SRAM, USB, LCD, AES



LQFP48
(7 x 7 mm)
LQFP64
(10 x 10 mm)
LQFP80
(12 x 12 mm)



UFQFPN32
(5 x 5 mm)
UFQFPN48
(7 x 7 mm)



UFBGA64
(5 x 5 mm)
UFBGA81
(5 x 5 mm)



WLCSP42
(2.82 x 2.93 mm)

Product summary	
STM32U083xC	STM32U083KC, STM32U083HC, STM32U083CC, STM32U083RC, STM32U083MC

Product label

SUSTAINABLE TECHNOLOGY

Features

Includes ST state-of-the-art patented technology.

Ultra-low-power features (ultra-low-power devices)

- 1.71 V to 3.6 V power supply
- -40 °C to 85/125 °C temperature range
- VBAT mode: 130 nA (with RTC and 9 x 32-bit backup registers)
- Shutdown mode (6 wake-up pins): 16 nA
- Standby mode (6 wake-up pins): 160 nA with RTC, 30 nA without RTC
- Stop 2 mode: 825 nA with RTC, 695 nA without RTC
- Run mode (LDO mode): 52 µA/MHz
- Batch acquisition mode (BAM)
- 4 µs wake-up from Stop mode
- Brownout reset (BOR)

Core

- 32-bit Arm® Cortex®-M0+ CPU, frequency up to 56 MHz

ART Accelerator

- 1-Kbyte instruction cache allowing 0-wait-state execution from flash memory

Benchmarks

- 1.13 DMIPS/MHz (Drystone 2.1)
- 134 CoreMark® (2.4 CoreMark/MHz at 56 MHz)
- 407 ULPMark™-CP
- 143 ULPMark™-PP
- 19.7 ULPMark™-CM

Memories

- 256-Kbyte single bank flash memory, proprietary code readout protection
- 40-Kbyte SRAM with hardware parity check

Rich analog peripherals (independent supply)

- 1x 12-bit ADC (0.4 µs conversion time), up to 16-bit with hardware oversampling
- 1x 12-bit DAC output channel, low-power sample and hold
- 1x general-purpose operational amplifier with built-in PGA (variable gain up to 16)
- 2x ultra-low-power comparators

LCD driver

- 8×48 or 4×52 segments, with step-up converter

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General-purpose inputs/outputs

- Up to 69 fast I/Os, most of them 5 V-tolerant

20 communication interfaces

- USB 2.0 full-speed crystal-less solution with LPM and BCD
- 7x USARTs/LPUARTs (SPI, ISO 7816, LIN, IrDA, modem)
- 4x I2C interfaces supporting Fast-mode and Fast-mode Plus (up to 1 Mbit/s)
- 3x SPIs, plus 4x USARTs in SPI mode
- IRTIM (Infrared interface)

Security

- Customer code protection
- Robust read out protection (RDP): 3 protection level states and password-based regression (128-bit PSWD)
- Hardware protection feature (HDP)
- Secure boot
- AES: 128/256-bit key encryption hardware accelerator
- True random number generation, candidate for NIST SP 800-90B certification
- Candidate for Arm® PSA level 1 and SESIP level 3 certifications
- 5 passive anti-tamper pins
- 96-bit unique ID

Clock management

- 4 to 48 MHz crystal oscillator
- 32 kHz crystal oscillator for RTC (LSE)
- Internal 16 MHz factory-trimmed RC (±1%)
- Internal low-power 32 kHz RC (±5%)
- Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
- Internal 48 MHz with clock recovery
- PLL for system clock, USB, ADC

10 timers, RTC, and 2 watchdogs

- 1x 16-bit advanced motor-control, 1x 32-bit and 3x 16-bit general purpose, 2x 16-bit basic, 3x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- RTC with hardware calendar, alarms and calibration

CRC calculation unit

Up to 21 capacitive sensing channels

- Supporting touchkey, linear and rotary touch sensors

12-channel DMA controller

- Flexible mapping (DMAMUX)

Debug

- Development support: serial wire debug (SWD)

All packages are ECOPACK2 compliant.

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1 Introduction

This document provides information on STM32U083xC devices, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging and ordering information.

It must be read in conjunction with the STM32U083xC reference manual (RM0503).

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32U083xC errata sheet (ES0602).

For information on the Arm® Cortex®-M0+ core, refer to the Cortex-M0+ Technical Reference Manual, available from the www.arm.com website.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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2 Description

The STM32U083xC devices are ultra-low-power microcontrollers based on the high-performance Arm® Cortex®-M0+ 32-bit RISC core operating at a frequency of up to 56 MHz.

The STM32U083xC devices embed high-speed memories (256-Kbyte flash memory and 40-Kbyte SRAM with hardware parity check), and an extensive range of enhanced I/Os and peripherals connected to APB and AHB buses, and a 32-bit multi-AHB bus matrix.

They also embed protection mechanisms for embedded flash memory and SRAM, such as readout protection and write protection.

The STM32U083xC devices offer a 12-bit ADC, a 12-bit DAC, two embedded rail-to-rail analog comparators, one operational amplifier, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, three general-purpose 16-bit timers, and three 16-bit low-power timers

The devices also embed up to 21 capacitive sensing channels, plus an integrated LCD controller that enables to drive 8x48 or 4x52 segments with internal step-up converter.

They also feature standard and advanced communication interfaces, namely four I2Cs, three SPIs, four USARTs and three low-power UARTs, plus one crystal-less USB full-speed device.

In addition, the STM32U083xC devices embed an AES hardware accelerator.

The STM32U083xC operate in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V V_{DD} power supply using an internal LDO regulator. A comprehensive set of power-saving modes makes possible the design of low-power applications.

Independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMP and comparator, as well as VBAT input allowing the backup of the RTC and backup registers.

The STM32U083xC offer eight packages from 32 to 81 pins.

Refer to the table below for the list of peripherals available on each part number.

Table 1. Device features and peripheral counts

Peripherals		STM32U083MC	STM32U083RC	STM32U083CC	STM32U083HC	STM32U083KC
Flash memory (Kbytes)		256				
SRAM (Kbytes)		40				
Timers	Advanced control	1 (16 bits)				
	General purpose	3 (16 bits) 1 (32 bits)				
	Basic	2 (16 bits)				
	Low power	3 (16 bits)				
	SysTick	1				
	Watchdog timers (independent, window)	2				
Communication interfaces	SPI	3				
	I2C	4				
	USART	4				
	LPUART	3				
	USB	Yes				
RTC		Yes				
Tamper pins		5	5	4	3	3
LCD COM x SEG		Yes 8x48 or 4x52	Yes 8x33 or 4x37	Yes 4x24	Yes 3x19	Yes 3x17

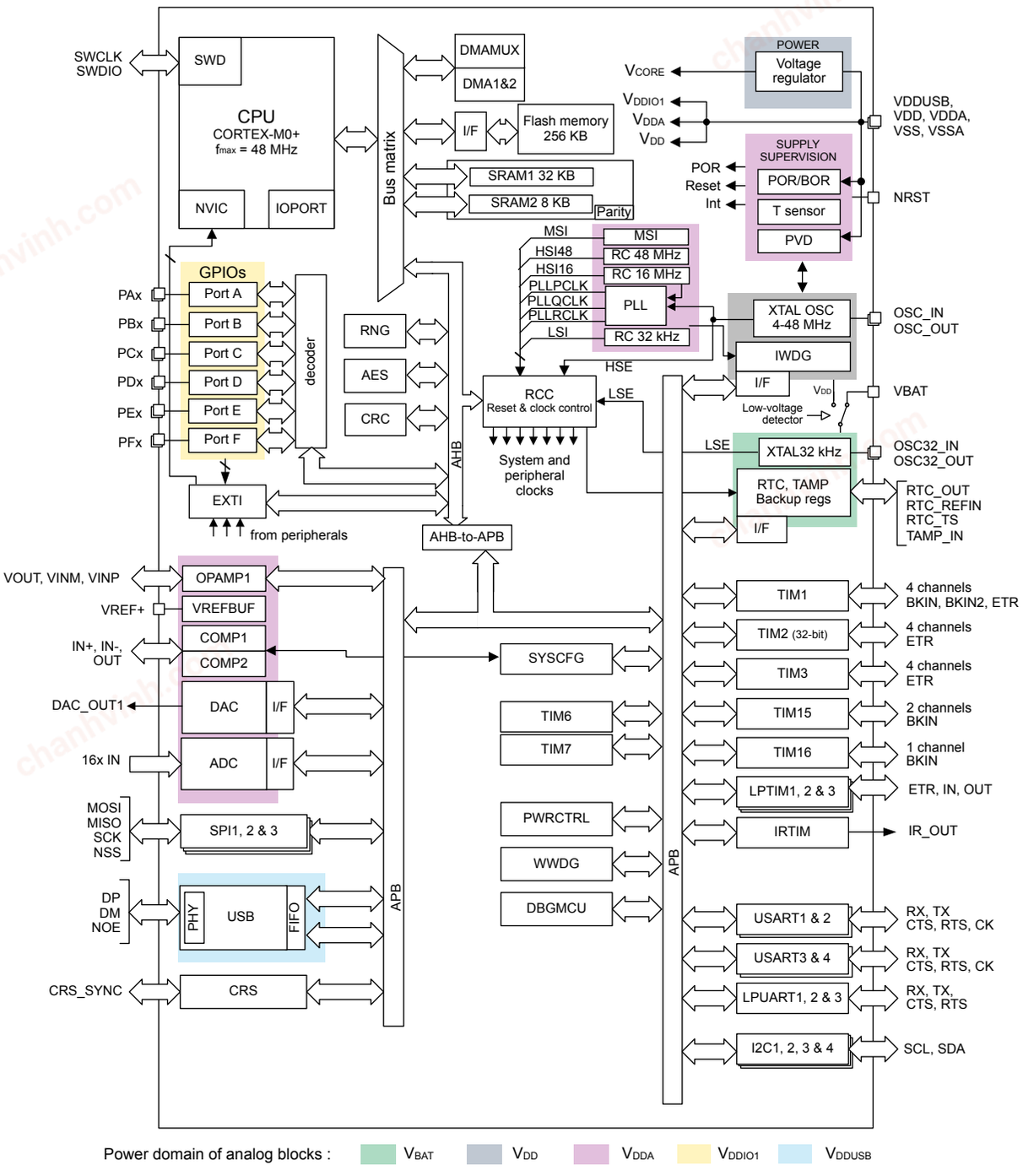
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Peripherals	STM32U083MC	STM32U083RC	STM32U083CC	STM32U083HC	STM32U083KC
True random number generator (RNG)	Yes				
AES hardware accelerator	Yes				
GPIOs	68/69[1]	53	39	33	27
Wake-up pins	6	6	6	4	3
Capacitive sensing Number of channels	21	18	12	9	8
12-bit ADC	1				1
Number of channels	16				10
12-bit DAC	1				
Internal voltage reference buffer	Yes	No			
Analog comparators	2				
Operational amplifier	1				
Max. CPU frequency (MHz)	56				
Operating voltage (V_{DD})	1.71 to 3.6 V				
Operating temperature	Ambient operating temperature:-40 to 85 °C/-40 to 125 °C Junction temperature:-40 to 105 °C/-40 to 130 C				
Packages	LQFP80, UFBGA81	LQFP64, UFBGA64	LQFP48, UFBGA48	WLCSP42	UFQFPN32

1. *LQFP80 and UFBGA81 offer 68 and 69 GPIOs, respectively.*

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Figure 1. **Block diagram**



DT71260V6

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3 Functional overview

3.1 Arm® Cortex®-M0+ core with MPU

The Arm Cortex -M0+ is an entry-level 32-bit Arm Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- A simple architecture, easy to learn and program
- ultra-low power, energy-efficient operation
- Excellent code density
- Deterministic, high-performance interrupt handling
- Upward compatibility with Cortex-M processor family
- Platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area- and power-optimized 32-bit core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to embedded Arm core, the STM32U083xC devices are compatible with Arm tools and software.

The Cortex-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC) described in Section 3.14.1: Nested vectored interrupt controller (NVIC).

3.2 Adaptive real-time memory accelerator (ART Accelerator)

The ART Accelerator is a memory accelerator optimized for STM32 industry-standard Arm® Cortex®-M0+ processors. It balances the inherent performance advantage of the Arm Cortex-M0+ over flash memory technologies, which normally requires the processor to wait for the flash memory at higher frequencies.

To release the processor near 67 DMIPS performance at 56 MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit flash memory. Based on benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from flash memory at a CPU frequency up to 56 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to corrupt accidentally the memory or resources used by any other active task.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

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3.4 Memories

3.4.1 Embedded flash memory

STM32U083xC devices feature 256 Kbytes of embedded flash memory available for storing code and data.

Flexible protections can be configured thanks to option bytes:

- Robust readout protection (RDP) with password-based regression (128-bit PSWD). Three protections level states are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M0+ serial wire), boot in RAM and bootloader selection are disabled. This selection is irreversible.

  Refer to Table 2 for the memory area access versus the RDP protection level.
- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.

Table 2. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
User memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option memory	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup memory	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. *Erased upon RDP change from Level 1 to Level 0.*

The whole nonvolatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- Readout of the ECC fail address from the ECC register

Securable area

A part of the flash memory can be hidden from the application once the code it contains is executed. As soon as the security is enabled on the securable area through the FLASH_HDPCR and FLASH_SECR registers, the securable memory cannot be accessed until the system resets. The securable area generally contains the secure boot code to execute only once at boot. This helps to isolate secret code from untrusted application code.

3.4.2 Embedded SRAM

STM32U083xC devices have 40-Kbyte SRAM with hardware parity check. Hardware parity check allows memory data errors to be detected, which contributes to increasing functional safety of applications.

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The embedded SRAM is split between two regions, as follows:

- SRAM1: 32 Kbytes with hardware parity check, mapped at address 0x2000 0000
- SRAM2: 8 Kbytes with hardware parity check, located at address 0x1000 0000
  SRAM2 is also mapped at address 0x2000 8000, offering a contiguous address space with SRAM1 (8 Kbytes aliased by bit band).
  The content of SRAM2 is retained in Standby mode.
  It is write-protected with a 1-Kbyte granularity.

The memory can be read/write-accessed at CPU clock speed, with 0 wait states.

3.5 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- Boot from user flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot pin is shared with a standard GPIO and can be enabled through the boot selector option bit. The boot loader is located in system memory. It manages the flash memory reprogramming through one of the following interfaces:

- USART on pins PA9/PA10, PC10/PC11, or PA2/PA3
- I2C-bus on pins PB6/PB7 or PB10/PB11
- SPI on pins PA4/PA5/PA6/PA7 or PB12/PB13/PB14/PB15
- USB on pins PA11/12

3.6 Power supply management

3.6.1 Power supply schemes

The STM32U083xC devices require a 1.71 to 3.6 V operating supply voltage (V_{DD}).

Several different power supplies are provided to specific peripherals:

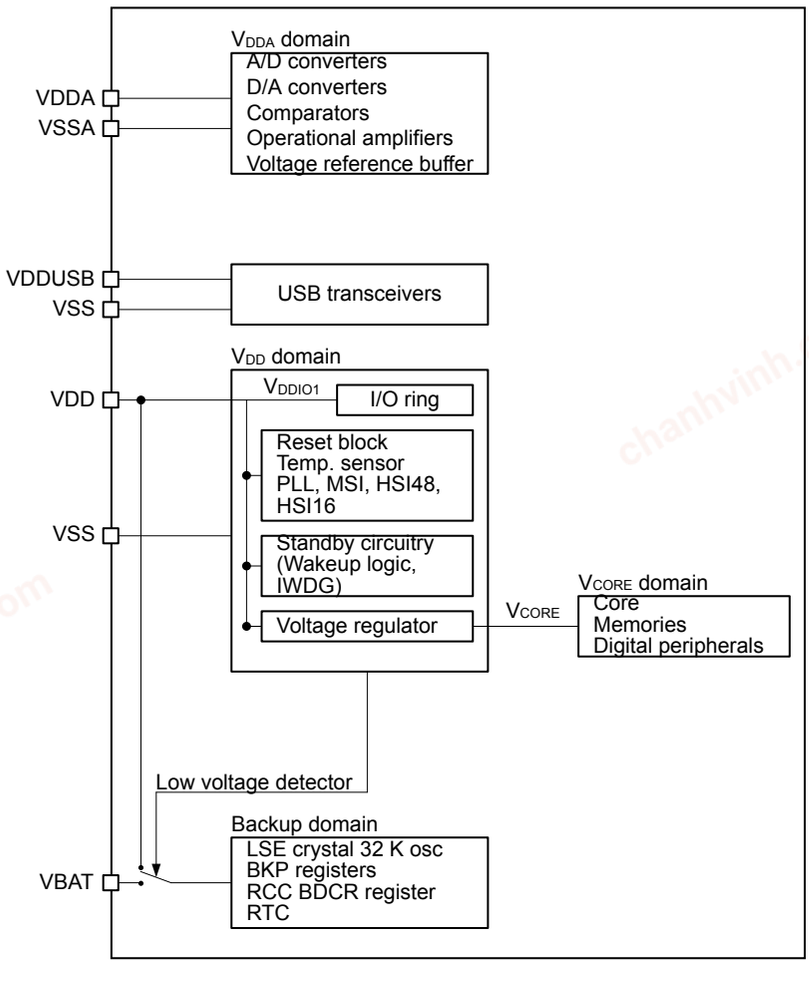
- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- V_{DDA} = 1.62 V (ADC/COMP)/1.80 V (DAC/OPAMP)/2.4 V (VREFBUF) to 3.6 V: external analog power supply for ADC, OPAMP, DAC, and comparator. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- V_{DDUSB} = 3.0 to 3.6 V: external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
- V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present. When VBAT pin is not available on the package, VBAT pad is internally bonded to VDD/VDDA pin.
- V_{REF+} is the analog peripheral input reference voltage, or the output of the internal voltage reference buffer (when enabled). When V_{DDA} < 2 V, V_{REF+} must be equal to V_{DDA}. When VDDA ≥ 2 V, V_{REF+} must be between 2 V and V_{DDA}. It can be grounded when the analog peripherals using V_{REF+} are not active.
  The internal voltage reference buffer supports two output voltages, which is configured with VRS bit of the VREFBUF_CSR register:
  - V_{REF+} around 2.048 V (requiring V_{DDA} equal to or higher than 2.4 V)
  - V_{REF+} around 2.5 V (requiring V_{DDA} equal to or higher than 2.8 V)

  V_{REF+} is delivered through VREF+ pin. On packages without VREF+ pin, VREF+ is internally connected to V_{DDA}, and the internal voltage reference buffer must be kept disabled (refer to datasheets for package pinout description).
- V_{CORE}
  An embedded linear voltage regulator is used to supply the V_{CORE} internal digital power. V_{CORE} is the power supply for digital peripherals, SRAM and flash memory. The flash memory is also supplied with V_{DD}.

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Note: When the functions supplied by V_{DDA} are not used, this supply should preferably be shorted to V_{DD}.
If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant.
V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1}, with V_{DDIO1} = V_{DD}.

Figure 2. Power supply overview



3.6.2 Power supply supervisor

The device has an integrated power-on/power-down (POR/PDR) reset active in all power modes except Shutdown and ensuring proper operation upon power-on and power-down. It maintains the device in reset when the supply voltage is below $V_{POR/PDR}$ threshold, without the need for an external reset circuit. Brownout reset (BOR) function allows extra flexibility. It can be enabled and configured through option bytes, by selecting one of four thresholds for rising V_{DD} and other four for falling V_{DD}.

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to V_{PVD} threshold. It allows generating an interrupt when V_{DD} level crosses the V_{PVD} threshold, selectively while falling, while rising, or while falling and rising. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

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3.6.3 Voltage regulator

Two embedded linear voltage regulators, main regulator (MR), and low-power regulator (LPR), supply most of digital circuitry in the device:

- The MR is used in Run, Sleep and Stop 0 modes.
- The LPR is used in Low-power run, Low-power sleep, Stop 1, and Stop 2 modes. It is also used to supply the 8-Kbyte SRAM2 in Standby mode, in order to ensure SRAM2 retention.

Both regulators are powered down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down, thus inducing zero consumption.

3.6.4 V_{BAT} operation

The V_{BAT} power domain, consuming very little energy, includes RTC, and LSE oscillator and backup registers.

In V_{BAT} mode, the RTC domain is supplied from VBAT pin. The power source can be, for example, an external battery or an external supercapacitor. Two anti-tamper detection pins are available.

The RTC domain can also be supplied from VDD/VDDA pin.

By means of a built-in switch, an internal voltage supervisor allows automatic switching of RTC domain powering between V_{DD} and voltage from V_{BAT} pin to ensure that the supply voltage of the RTC domain (V_{BAT}) remains within valid operating conditions. If both voltages are valid, the RTC domain is supplied from VDD/VDDA pin.

An internal circuit for charging the battery on VBAT pin can be activated if the V_{DD} voltage is within a valid range.

Note: External interrupts and RTC alarm/events cannot cause the microcontroller to exit the VBAT mode, as in that mode the V_{DD} is not within a valid range.

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3.7 Low-power modes

By default, the microcontroller is in Run mode after system or power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run mode**
  This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator operating current. The code can be executed from SRAM or from flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep mode**
  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When the wake-up is triggered by an event or an interrupt, the system reverts to the Low-power run mode.
- **Stop 0, Stop 1, and Stop 2 modes**
  The Stop modes achieve a lowest power consumption while retaining the content of SRAM and registers. All the clocks in the V_{CORE} domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE and LSI clocks are still running.
  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).
  Some peripherals with the wake-up capability can enable the HSI16 RC during Stop mode, to detect their wake-up condition.
  Three Stop modes are available, Stop 0, Stop 1 and Stop2:
  - In Stop2 mode, most of the V_{CORE} domain is put in lower-leakage mode.
  - Stop 1 offers the largest number of active peripherals and wake-up sources, a smaller wake-up time, but with a higher consumption than Stop 2 mode.
  - In Stop 0 mode, the main regulator remains on, allowing a very fast wake-up time, but with a much higher consumption.

  When exiting from Stop 0, Stop 1 or Stop 2 mode, the system clock can be either the MSI clock (up to 48 MHz) or HSI16, depending on software configuration.
- **Standby mode**
  The Standby mode is used to achieve one of the lowest power consumption, with POR/PDR always active in this mode. The main regulator is switched off to power down V_{CORE} domain. The low-power regulator is either switched off or kept active. In the latter case, it only supplies SRAM to ensure data retention. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are also powered down. The RTC can remain active (Standby mode with RTC, Standby mode without RTC).
  For each I/O, the software can determine whether a pull-up, a pull-down or no resistor must be applied to that I/O during Standby mode.
  Upon entering Standby mode, register contents are lost except for registers in the RTC domain and standby circuitry. The SRAM contents can be retained through register setting.
  The device exits Standby mode upon external reset event (NRST pin), IWDG reset event, wake-up event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wake-up, timestamp, tamper), or when a failure is detected on LSE (CSS on LSE).
- **Shutdown mode**
  The Shutdown mode enables to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.
  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).
  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.
  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.
  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wake-up, timestamp, tamper).
  The system clock after wake-up is MSI at 4 MHz.

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Table 3. Functionalities depending on the mode

Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (256 Kbytes)	O(1)	O(1)	O(1)	O(1)	-	-	-	-	-	-	-	-	-
SRAM1 (32 Kbytes)	Y	Y(2)	Y	Y(2)	Y	-	Y	-	-	-	-	-	-
SRAM2 (8 Kbytes)	Y	Y(2)	Y	Y(2)	Y	-	Y	-	O(3)	-	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor (PVMx; x = 1, 2, 3)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
High-speed Internal (HSI16)	O	O	O	O	(4)	-	(4)	-	-	-	-	-	-
Oscillator RC48 (HSI48)	O	O	-	-	-	-	-	-	-	-	-	-	-
High-speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low-speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi-Speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto-wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC tamper pins	2	2	2	2	2	O	2	O	2	O	2	O	2
USARTx (x = 1, 2, 3, 4)	O	O	O	O	O(5)	O(5)	-	-	-	-	-	-	-
LPUARTx (x = 1 to x = 3)	O	O	O	O	O(5)	O(5)	O(5)	O(5)	-	-	-	-	-
I2Cx (x = 2, 4)	O	O	O	O	O(6)	O(6)	-	-	-	-	-	-	-
I2Cx (x = 1, 3)	O	O	O	O	O(6)	O(6)	O(6)	O(6)	-	-	-	-	-
SPIx (x = 1 to 3)	O	O	O	O	-	-	-	-	-	-	-	-	-
ADC1	O	O	O	O	-	-	-	-	-	-	-	-	-
DAC1	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMP1	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x = 1, 2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-

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Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
LPTIMx (x = 1 to 3)	O	O	O	O	O	O	O	O	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
LCD	O	O	O	O	O	O	O	O	-	-	-	-	-
True random number generator (RNG)	O(7)	O(7)	-	-	-	-	-	-	-	-	-	-	-
AES hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(8)	5 pins(9)	(10)	5 pins(9)	-

1. *The flash memory can be configured in power-down mode. By default, it is not in power-down mode.*
2. *The SRAM clock can be gated on or off.*
3. *SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.*
4. *Some peripherals with wake-up from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.*
5. *UART and LPUART reception is functional in Stop mode, and generates a wake-up interrupt on Start, address match or received frame event.*
6. *I2C address detection is functional in Stop mode, and generates a wake-up interrupt in case of address match.*
7. *Voltage scaling Range 1 only.*
8. *I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.*
9. *The I/Os with wake-up from Standby/Shutdown capability are PA0, PA1, PA2, PB15, PC5, and PC13.*
10. *I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.*

3.8 Peripheral interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

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Table 4. **Interconnect of peripherals**

Interconnect source	Interconnect destination	Interconnect action	Run Low-power run	Sleep Low-power sleep	Stop
TIMx	TIMx	Timer synchronization or chaining	Y	Y	-
	ADCx DACx	Conversion triggers	Y	Y	-
	DMA	Memory-to-memory transfer trigger	Y	Y	-
	COMPx	Comparator output blanking	Y	Y	-
COMPx	TIM1, 2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	-
	LPTIMx	Low-power timer triggered by analog signals comparison	Y	Y	Y
ADCx	TIM1	Timer triggered by analog watchdog	Y	Y	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	-
	LPTIMx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y
All clock sources (internal and external)	TIM16	Clock source used as input channel for RC measurement and trimming	Y	Y	-
CSS RAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1, 15, 16	Timer break	Y	Y	-
CPU (HardFault)	TIM1 15, 16	Timer break	Y	-	-
GPIOs	TIMx	External trigger	Y	Y	-
	LPTIMx	External trigger	Y	Y	Y
	ADCx DACx	Conversion external trigger	Y	Y	-

3.9 Reset and clock controller (RCC)

3.9.1 Reset mode

During and upon exiting reset, the schmitt triggers of I/Os are disabled so as to reduce power consumption. In addition, when the reset source is internal, the built-in pull-up resistor on NRST pin is deactivated.

3.9.2 Clocks and startup

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.

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- **Safe clock** switching: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**: two different sources can deliver SYSCLK system clock:
  - 4-48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). It can supply clock to system PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software. It can supply clock to system PLL.
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies form 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach an accuracy better than ± 0.25%. The MSI can supply a PLL.
  - System PLL, which can be fed by HSE, HSI16 or MSI. It provides a system clock up to 56 MHz.
- **Auxiliary clock source**: three ultra-low-power clock sources for the real-time clock (RTC), and the LCD controller:
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ± 5% accuracy, also used to clock an independent watchdog.
- **Peripheral clock sources**: several peripherals (RNG, USARTs, I2Cs, LPTIMs, ADC) have their own clock independent of the system clock.
- **Clock security system (CSS)**: in the event of HSE clock failure, the system clock is automatically switched to HSI16 and, if enabled, a software interrupt is generated. LSE clock failure can also be detected and generate an interrupt. The CSS feature can be enabled by software.
- **Clock output**:
  - **MCO (microcontroller clock output)** provides one of the internal clocks for external use by the application
  - **LSCO (low speed clock output)** provides LSI or LSE in all low-power modes (except in VBAT operation).

Several prescalers enable the application to configure AHB and APB domain clock frequencies, 56 MHz at maximum.

3.10 Clock recovery system (CRS)

The STM32U083xC devices embed a special block, which enables automatic trimming of the internal 48 MHz oscillator, to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin, or generated by the user software. For faster lock-in during startup, it is also possible to combine automatic trimming with manual trimming action.

3.11 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function (AF). Most of the GPIO pins are shared with special digital or analog functions.

Through a specific sequence, this special function configuration of I/Os can be locked, such as to avoid spurious writing to I/O control registers.

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3.12 Direct memory access controller (DMA)

The direct memory access (DMA) controller is a bus master and system peripheral with single-AHB architecture.

With seven channels, it performs data transfers between memory-mapped peripherals and/or memories, to offload the CPU.

Each channel is dedicated to managing memory access requests from one or more peripherals. The unit includes an arbiter for handling the priority between DMA requests.

Main features of the DMA controller:

- Single-AHB master
- Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-to-peripheral data transfers
- Access, as source and destination, to on-chip memory-mapped devices such as flash memory, SRAM, and AHB and APB peripherals
- All DMA channels independently configurable:
  - Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
  - Priority between the requests is programmable by software (four levels per channel: very high, high, medium, low) and by hardware in case of equality (such as request to channel 1 has priority over request to channel 2).
  - Transfer size of source and destination are independent (byte, half-word, word), emulating packing and unpacking. Source and destination addresses must be aligned on the data size.
  - Support of transfers from/to peripherals to/from memory with circular buffer management
  - Programmable number of data to be transferred: 0 to 2^{16} - 1
- Generation of an interrupt request per channel. Each interrupt request originates from any of the three DMA events: transfer complete, half transfer, or transfer error.

3.13 DMA request multiplexer (DMAMUX)

The DMAMUX request multiplexer enables routing a DMA request line between the peripherals and the DMA controller. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. DMAMUX may also be used as a DMA request generator from programmable events on its input trigger signals.

3.14 Interrupts and events

The device flexibly manages events causing interrupts of linear program execution, called exceptions. The Cortex®-M0+ processor core, a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI) are the assets contributing to handling the exceptions. Exceptions include core-internal events such as, for example, a division by zero and, core-external events such as logical level changes on physical lines. Exceptions result in interrupting the program flow, executing an interrupt service routine (ISR) then resuming the original program flow.

The processor context (contents of program pointer and status registers) is stacked upon program interrupt and unstacked upon program resume, by hardware. This avoids context stacking and unstacking in the interrupt service routines (ISRs) by software, thus saving time, code and power. The ability to abandon and restart load-multiple and store-multiple operations significantly increases the device's responsiveness in processing exceptions.

3.14.1 Nested vectored interrupt controller (NVIC)

The configurable nested vectored interrupt controller is tightly coupled with the core. It handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupts, and Cortex®-M0+ exceptions. It provides flexible priority management.

The tight coupling of the processor core with NVIC significantly reduces the latency between interrupt events and start of corresponding interrupt service routines (ISRs). The ISR vectors are listed in a vector table, stored in the NVIC at a base address. The vector address of an ISR to execute is hardware-built from the vector table base address and the ISR order number used as offset.

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If a higher-priority interrupt event happens while a lower-priority interrupt event occurring just before is waiting for being served, the later-arriving higher-priority interrupt event is served first. Another optimization is called tail-chaining. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context unstacking and stacking is skipped. This reduces latency and contributes to power efficiency.

Features of the NVIC:

- Low-latency interrupt processing
- Four priority levels
- Handling of a non-maskable interrupt (NMI)
- Handling of 32 maskable interrupt lines
- Handling of 10 Cortex-M0+ exceptions
- Later-arriving higher-priority interrupt processed first
- Tail-chaining
- Interrupt vector retrieval by hardware

3.14.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller adds flexibility in handling physical line events and allows identifying wake-up events at processor wake-up from Stop mode.

The EXTI controller has a number of channels, of which some with rising, falling or rising, and falling edge detector capability. Any GPIO and a few peripheral signals can be connected to these channels.

The channels can be independently masked.

The EXTI controller can capture pulses shorter than the internal clock period.

A register in the EXTI controller latches every event even in Stop mode, which enables the software to identify the origin of the processor wake-up from Stop mode or, to identify the GPIO and the edge event having caused an interrupt.

3.15 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

3.16 Analog-to-digital converter (ADC)

A native 12-bit analog-to-digital converter is embedded into STM32U083xC devices. It can be extended to 16-bit resolution through hardware oversampling. The ADC has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference, V_{BAT} monitoring). It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of ~2 Msps even with a low CPU speed. An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate in the whole V_{DD} supply range.

The ADC features a hardware oversampler up to 256 samples, improving the resolution to 16 bits (refer to AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions with timers.

3.16.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to an ADC input to convert the sensor output voltage into a digital value.

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The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor may vary from part to part due to process variation, the uncalibrated internal temperature sensor is suitable only for relative temperature measurements.

To improve the accuracy of the temperature sensor, each part is individually factory-calibrated by ST. The resulting calibration data are stored in the part's engineering bytes, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 6E68 - 0x1FFF 6E69
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 6E8A - 0x1FFF 6E8B

3.16.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to an ADC input. The V_{REFINT} voltage is individually precisely measured for each part by ST during production test and stored in the part's engineering bytes. It is accessible in read-only mode.

Table 6. Internal voltage reference calibration values

Calibration value name	Description	Memory address
V_{REFINT}	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 6EA4 - 0x1FFF 6EA5

3.16.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using an internal ADC input. As the V_{BAT} voltage may be higher than V_{DDA} and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by three. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.17 Digital-to-analog converter (DAC)

The single-channel 12-bit buffered DAC converts a digital value into an analog voltage available on the channel output. The architecture of either channel is based on integrated resistor string and an inverting amplifier.

Features of the DAC:

- One DAC output channel
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability
- Triggering with timer events, synchronized with DMA
- Triggering with external events
- Sample-and-hold low-power mode, with internal or external capacitor

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3.18 Voltage reference buffer (VREFBUF)

When enabled, an embedded buffer provides the internal reference voltage to analog blocks (for example ADC) and to VREF+ pin for external components.

The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is disabled.

On some packages, the VREF+ pad of the silicon die is double-bonded with supply pad to common VDD/VDDA pin and so the internal voltage reference buffer cannot be used.

3.19 Comparators (COMP)

STM32U083xC embed two embedded rail-to-rail analog comparators with programmable reference voltage (internal or external), hysteresis, speed (low for low-power), and output polarity.

The reference voltage can be one of the following:

- External, from an I/O
- Internal, from DAC
- Internal reference voltage (V_{REFINT}) or its submultiple (1/4, 1/2, 3/4)

The comparators can wake up the device from Stop mode, generate interrupts, breaks or triggers for the timers and can be also combined into a window comparator.

3.20 Operational amplifier (OPAMP)

The STM32U083xC devices embed one operational amplifier with external and internal follower routing and PGA capability.

Features of the operational amplifier:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.21 Liquid crystal controller (LCD)

The LCD drives up to eight common terminals and 48 segment terminals to drive up to 352 pixels.

Features of the LCD:

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to eight pixels can be programmed to blink
  Unneeded segments and common pins can be used as general I/O pins
  LCD RAM can be updated at any time owing to a double-buffer
  The LCD controller can operate in Stop mode

3.22 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (such as glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library that is free to use and allows touch sensing functionality to be implemented reliably in the end application.

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The main features of the touch sensing controller are the following:

- Charge transfer acquisition principle
- Up to 21 capacitive sensing channels
- Up to three capacitive sensing channels can be acquired in parallel offering a very good response time
- Five selectable thresholds (V_{IH}, V_{REF}, 3/4 V_{REF}, 1/2 V_{REF}, 1/4 V_{REF}) using the digital threshold or the ultra-low-power comparator
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to three capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with the STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.23 True random-number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

3.24 Advanced-encryption-standard (AES) hardware accelerator

The embedded AES hardware accelerator can encipher or decipher data, using AES algorithm.

Features of AES:

- Encryption/decryption using AES Rijndael Block Cipher algorithm
- NIST-FIPS-197-compliant implementation of AES encryption/decryption algorithm
- 128-bit and 256-bit register for storing the encryption, decryption or derivation key (four 32-bit registers)
- Electronic codebook (ECB), cipher block chaining (CBC), counter (CTR), Galois counter (GCM), Galois message authentication code (GMAC) and cipher message authentication code (CMAC) modes supported
- Key scheduler
- Key derivation for decryption
- 128-bit data block processing
- 128-bit and 256-bit key length
- 32-bit input and output buffers
- Register access supporting 32-bit data width
- 128-bit register for the initialization vector when AES is configured in CBC mode or for the 32-bit counter initialization when CTR mode is selected, GCM mode or CMAC mode
- Automatic data flow control with support of direct memory access (DMA) using 2 channels, one for incoming data, the other for outcoming data
- Message processing suspend to process another message with higher priority

3.25 Timers and watchdogs

The device includes an advanced-control timer, six general-purpose timers, two basic timers, three low-power timers, two watchdog timers and a SysTick timer. Table 7 compares features of the advanced-control, general-purpose and basic timers.

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Table 7. **Timer feature comparison**

Timer type	Timer	Counter resolution	Counter type	Maximum operating frequency	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced-control	TIM1	16-bit	Up, down, up/down	56 MHz	Integer from 1 to 2^{16}	Yes	4	3
General-purpose	TIM2	32-bit	Up, down, up/down	56 MHz	Integer from 1 to 2^{16}	Yes	4	-
	TIM3	16-bit	Up, down, up/down	56 MHz	Integer from 1 to 2^{16}	Yes	4	-
	TIM15	16-bit	Up	56 MHz	Integer from 1 to 2^{16}	Yes	2	1
	TIM16	16-bit	Up	56 MHz	Integer from 1 to 2^{16}	Yes	1	1
Basic	TIM6 and TIM7	16-bit	Up	56 MHz	Integer from 1 to 2^{16}	Yes	-	-
Lower-power	LPTIM1, LPTIM2, and LPTIM3	16-bit	Up	56 MHz	2^n where n = 0 to 7	No	N/A	-

3.25.1 Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM unit multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM output (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled, so as to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in Section 3.25.2: General-purpose timers (TIM2, 3, 15, 16)) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.25.2 General-purpose timers (TIM2, 3, 15, 16)

There are four synchronizable general-purpose timers embedded in the device (refer to Table 7 for comparison). Each general-purpose timer can be used to generate PWM outputs or act as a simple timebase.

- TIM2, TIM3
  These are full-featured general-purpose timers:
  - TIM2 with 32-bit auto-reload up/downcounter and 16-bit prescaler
  - TIM3 with 16-bit auto-reload up/downcounter and 16-bit prescaler

  They have four independent channels for input capture/output compare, PWM, or onepulse mode output. They can operate together or in combination with other general-purpose timers via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request and support quadrature encoders. Their counters can be frozen in debug mode.
- TIM15, TIM16
  These are general-purpose timers featuring:
  - 16-bit auto-reload upcounter and 16-bit prescaler
  - 2 channels and 1 complementary channel for TIM15
  - 1 channel and 1 complementary channel for TIM16

  All channels can be used for input capture/output compare, PWM or one-pulse mode output. The timers can operate together via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request. Their counters can be frozen in debug mode.

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3.25.3 Basic timers (TIM6 and TIM7)

These timers are mainly used for triggering DAC conversions. They can also be used as generic 16-bit timebases.

3.25.4 Low-power timers (LPTIM1, LPTIM2, and LPTIM3)

These timers have an independent clock. When fed with LSE, LSI or external clock, they keep running in Stop mode and they can wake up the system from it.

Features of LPTIM1, LPTIM2, and LPTIM3:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output (pulse, PWM)
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Selectable clock source:
  - Internal: LSE, LSI, HSI16 or APB clocks
  - External: over LPTIM input (working even with no internal clock source running, used by pulse counter application)
- Programmable digital glitch filter
- Encoder mode

3.25.5 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 32 kHz internal RC (LSI).

Independent of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. Its counter can be frozen in debug mode.

3.25.6 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked by the system clock. It has an early-warning interrupt capability. Its counter can be frozen in debug mode.

3.25.7 SysTick timer

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter.

Features of SysTick timer:

- 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.26 Real-time clock (RTC), tamper (TAMP) and backup registers

The device embeds an RTC and nine 32-bit backup registers, located in the RTC domain of the silicon die.

The ways of powering the RTC domain are described in Section 3.6.1: Power supply schemes.

The RTC is an independent BCD timer/counter.

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Features of the RTC:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Programmable alarm
- On-the-fly correction from 1 to 32767 RTC clock pulses, usable for synchronization with a master clock
- Reference clock detection - a more precise second-source clock (50 or 60 Hz) can be used to improve the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Five anti-tamper detection pins with programmable filter
- Timestamp feature to save a calendar snapshot, triggered by an event on the timestamp pin or a tamper event, or by switching to VBAT mode
- 17-bit auto-reload wake-up timer (WUT) for periodic events, with programmable resolution and period
- Multiple clock sources and references:
  - A 32.768 kHz external crystal (LSE)
  - An external resonator or oscillator (LSE)
  - The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
  - The high-speed external clock (HSE) divided by 32

When clocked by LSE, the RTC operates in VBAT mode and in all low-power modes. When clocked by LSI, the RTC does not operate in VBAT mode, but it does in low-power modes except for the Shutdown mode.

All RTC events (alarm, wake-up timer, timestamp or tamper) can generate an interrupt and wake the device up from the low-power modes.

The backup registers allow keeping 20 bytes of user application data in the event of VDD failure, if a valid backup supply voltage is provided on VBAT pin. They are not affected by the system reset, power reset, and upon the device wake-up from Standby or Shutdown modes.

3.27 Inter-integrated circuit interface (I2C)

The device embeds four I2C peripherals. Refer to Table 8 for the features.

The I^2C-bus interface handles communication between the microcontroller and the serial I^2C-bus. It controls all I^2C-bus-specific sequencing, protocol, arbitration and timing.

Features of the I2C peripheral:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and extra output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Clock stretching
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent of the PCLK reprogramming
- Wake-up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

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Table 8. I²C implementation

I²C features	I2C1	I2C2	I2C3	I2C4
Standard mode (up to 100 kbit/s)	X	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X	X
Fast mode Plus (up to 1 Mbit/s) with extra output drive I/Os	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	-	-	-	-
Independent clock	X	-	X	-
Wake-up from Stop mode on address match	X	-	X	-

3.28 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The devices embed universal synchronous/asynchronous receivers/transmitters that communicate at speeds of up to 8 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, synchronous SPI master/slave communication and single-wire half-duplex communication mode. Some can also support smartcard communication (ISO 7816), IrDA SIR ENDEC, LIN master/slave capability and auto baud rate feature, and have a clock domain independent of the CPU clock, which allows them to wake up the MCU from Stop mode. The wake-up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 9. USART implementation

X: supported

USART modes/ features	USART1 USART2	USART3 USART4
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous SPI mode (master/slave)	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wake-up from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver enable	X	X

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3.29 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed three LPUARTs. The peripherals support asynchronous serial communication with minimum power consumption, as well as half-duplex single wire communication and modem operations (CTS/RTS). They allow multiprocessor communication.

The LPUARTs have a clock domain independent of the CPU clock, and can wake up the system from Stop mode using baud rates up to 220 Kbaud. The Stop mode wake-up events are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUARTs can wait for an incoming frame while having an extremely low energy consumption. To reach higher baud rates, a higher speed clock can be used.

The LPUART interface can be served by the DMA controller.

3.30 Serial peripheral interface (SPI)

The devices contain three SPIs running at up to 32 Mbits/s in master and slave modes. It supports half-duplex, full-duplex and simplex communications. A 3-bit prescaler gives eight master mode frequencies. The frame size is configurable from 4 bits to 16 bits. The SPI peripherals support NSS pulse mode, TI mode and hardware CRC calculation.

The SPI peripherals can be served by the DMA controller.

Table 10. SPI implementation

X: supported

SPI modes/ features	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	-	-	-
TI mode	X	X	X

3.31 Universal serial bus device (USB)

The devices embed a USB controller with full-speed USB device compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up, and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up to 1 Kbyte and suspend/resume support. It requires a precise 48 MHz clock that is generated from the internal main PLL (the clock source must use an HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which enables crystal less operation.

3.32 Debug support

3.32.1 Serial wire debug port (SW-DP)

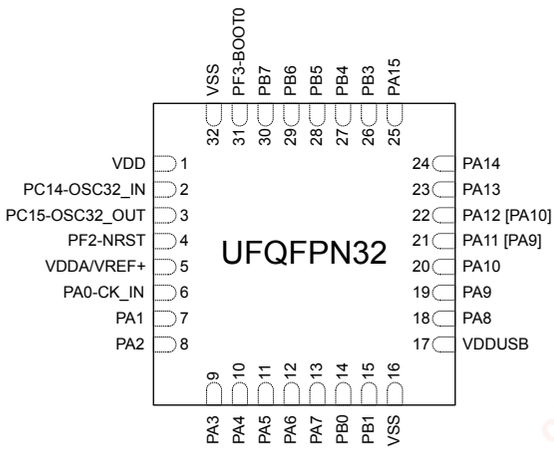
An Arm® SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

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4 Pinouts/ballouts, pin description, and alternate functions

4.1 Pinout/ballout schematics

Figure 3. UFQFPN32 pinout



DT71261V1

1. *The above figure shows the package top view.*

Figure 4. WLCSP42 ballout

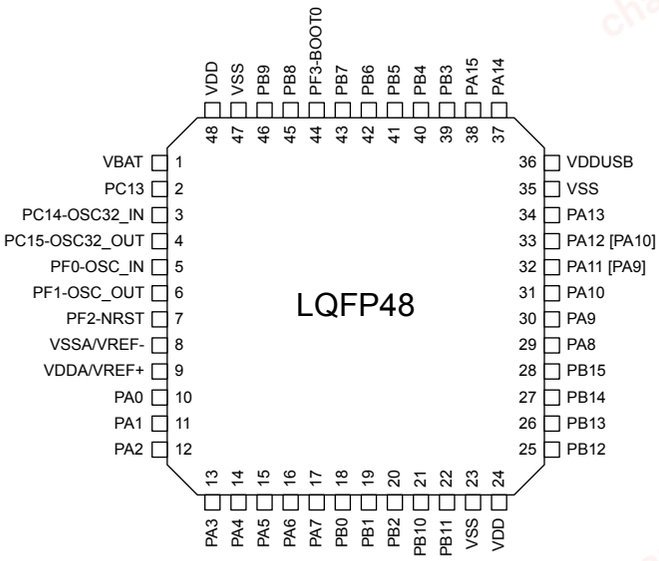
	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	VSS	NC	PA15	NC	PB5	NC	PB7	NC	PB8	NC	VSS
B	VDDUSB	NC	PA13	NC	PB3	NC	PB6	NC	VBAT	NC	VDD	NC
C	NC	PA12	NC	PA9	NC	PB4	NC	PF3	NC	PC15	NC	PC14
D	PA11	NC	PA8	NC	PA14	NC	PC13	NC	PF1	NC	PF0	NC
E	NC	PA10	NC	PA5	NC	PA3	NC	PA1	NC	VSSA/VREF-	NC	PF2
F	VSS	NC	PB1	NC	PB0	NC	PA7	NC	PA0	NC	VDDA/VREF+	NC
G	NC	VDD	NC	PB10	NC	PB2	NC	PA6	NC	PA4	NC	PA2

DT71292V1

1. *The above figure shows the package top view.*

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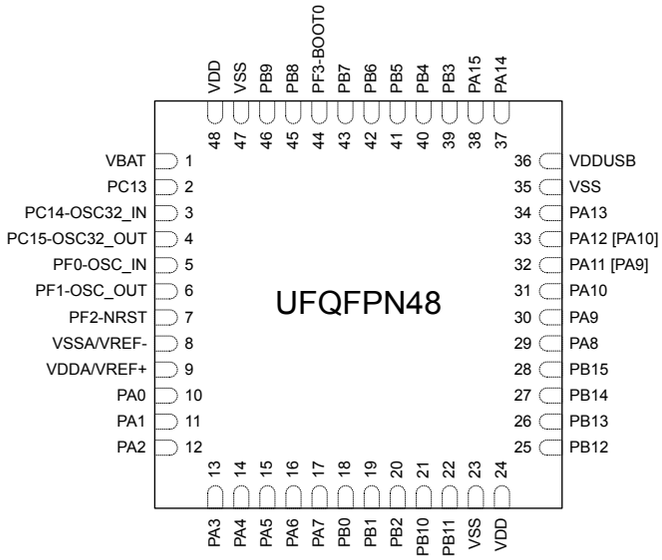
Figure 5. **LQFP48 pinout**



DT71263V1

1. *The above figure shows the package top view.*

Figure 6. **UFQFPN48 pinout**

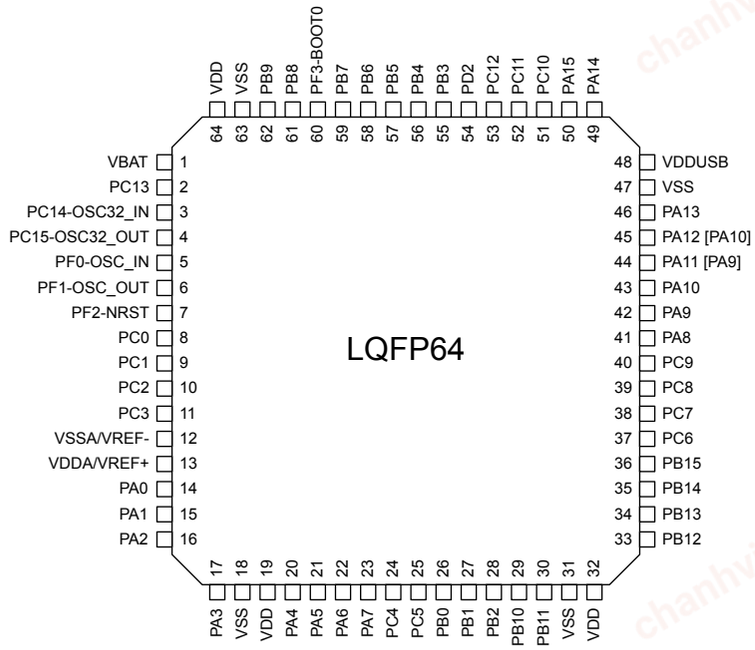


DT71264V1

1. *The above figure shows the package top view.*

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Figure 7. LQFP64 pinout



DT71265V1

1. *The above figure shows the package top view.*

Figure 8. UFBGA64 ballout

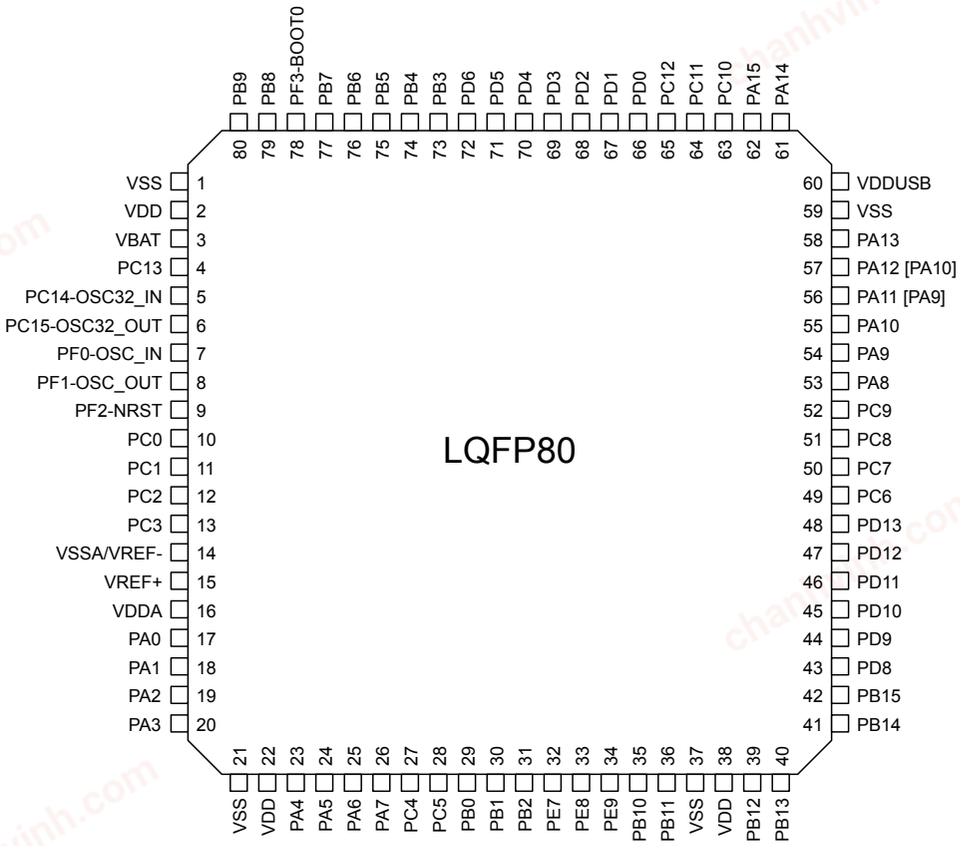
	1	2	3	4	5	6	7	8
A	PC14-OSC32_IN	PC13	PB9	PB4	PB3	PA15	PA14	PA13
B	PC15-OSC32_OUT	VBAT	PB8	PF3-BOOT0	PD2	PC11	PC10	PA12 [PA10]
C	PF0-OSC_IN	VSS	PB7	PB5	PC12	PA10	PA9	PA11 [PA9]
D	PF1-OSC_OUT	VDD	PB6	VSS	VSS	VSS	PA8	PC9
E	PF2-NRST	PC1	PC0	VDD	VDDUSB	VDD	PC7	PC8
F	VSSA/VREF-	PC2	PA2	PA5	PB0	PC6	PB15	PB14
G	PC3	PA0	PA3	PA6	PB1	PB2	PB10	PB13
H	VDDA/VREF+	PA1	PA4	PA7	PC4	PC5	PB11	PB12

DT71266V1

1. *The above figure shows the package top view.*

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Figure 9. LQFP80 pinout



DT71267V2

1. *The above figure shows the package top view.*

Figure 10. UFBGA81 ballout

	1	2	3	4	5	6	7	8	9
A	PB8	PF3-BOOT0	PB4	PB5	PD4	PD0	PC12	PC10	PA15
B	VBAT	PB9	PB7	PB6	PD6	PD1	PC11	PA14	PA13
C	PC15-OSC32_OUT	PC14-OSC32_IN	PE3	PB3	PD5	PD2	VDDUSB	PA12 [PA10]	PA11 [PA9]
D	PF1-OSC_OUT	PF0-OSC_IN	VDD	VSS	PD3	VSS	PA9	PA10	PC9
E	PC0	PF2-NRST	PC13	PA1	PC8	PC7	PA8	PC6	PD13
F	PC1	PC2	PA0	VSS	PB0	VSS	PB15	PD11	PD12
G	PC3	VSSA/VREF-	VDD	PC5	PE7	PE8	VDD	PD9	PD10
H	VREF+	PA2	PA5	PA7	PB1	PE9	PB11	PB13	PD8
J	VDDA	PA3	PA4	PA6	PC4	PB2	PB10	PB12	PB14

DT71293V1

1. *The above figure shows the package top view.*

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4.2 Pin description

Table 11. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I/O	Input /output pin
I/O structure		FT	5V-tolerant I/O
		TT	3.6V-tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Options for TT and FT I/Os	
		_a	I/O with analog switch function supplied by V_{DDA}
		_f	I2C Fm+ capable I/O
		_l	I/O with LCD function supplied by VLCD
		_u	I/O with USB function, supplied by V_{DDUSB}
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. STM32U083xC pin/ball definition

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
UFQFPN32	WLCSP42	LQFP48	UFQFPN48	LQFP64	UFBGA64	LQFP80	UFBGA81						
-	-	-	-	-	-	-	C3	PE3	I/O	FT	-	TIM3_CH1, EVENTOUT	-
-	B9	1	1	1	B2	3	B1	VBAT	S	-	-	-	-
-	D7	2	2	2	A2	4	E3	PC13	I/O	FT	(1)(2)	LPTIM1_CH3, LPTIM3_CH3, EVENTOUT	WKUP2, TAMP_IN1, RTC_TS/RTC_OUT1
2	C12	3	3	3	A1	5	C2	PC14-OSC32_IN	I/O	FT	(1)(2)	EVENTOUT	OSC32_IN

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
UFQFPN32	WLCSP42	LQFP48	UFQFPN48	LQFP64	UFBGA64	LQFP80	UFBGA81						
3	C10	4	4	4	B1	6	C1	PC15-OSC32_OUT	I/O	FT	(1)(2)	OSC32_EN, OSC_EN, EVENTOUT	OSC32_OUT, OSC32_EN
-	D11	5	5	5	C1	7	D2	PF0-OSC_IN	I/O	FT	-	EVENTOUT	OSC_IN
-	D9	6	6	6	D1	8	D1	PF1-OSC_OUT	I/O	FT	-	OSC_EN, EVENTOUT	OSC_OUT
4	E12	7	7	7	E1	9	E2	PF2-NRST	I/O	RST	-	MCO	NRST
-	-	-	-	8	E3	10	E1	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C4_SCL, I2C3_SCL, LPUART1_RX, LPUART2_TX, LCD_SEG18, LCD_BIAS1, LPTIM2_IN1, EVENTOUT	ADC1_IN0
-	-	-	-	9	E2	11	F1	PC1	I/O	FT_fla	-	LPTIM1_CH1, I2C4_SDA, I2C3_SDA, LPUART1_TX, LPUART2_RX, LCD_SEG19, LCD_BIAS2, EVENTOUT	ADC1_IN1
-	-	-	-	10	F2	12	F2	PC2	I/O	FT_la	-	MCO2, LPTIM1_IN2, SPI2_MISO, LCD_SEG20, LCD_BIAS3, EVENTOUT	ADC1_IN2
-	-	-	-	11	G1	13	G1	PC3	I/O	FT_la	-	LPTIM1_ETR, LPTIM3_CH1, SPI2_MOSI, USART4_CK, LCD_VLCD, LPTIM2_ETR, EVENTOUT	ADC1_IN3
-	E10	8	8	12	F1	14	G2	VSSA/VREF-	S	-	-	-	-
-	-	-	-	-	-	15	H1	VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	-	-	-	16	J1	VDDA	S	-	-	-	-
5	F11	9	9	13	H1	-	-	VDDA/VREF+	S	-	-	-	-
-	F9	10	10	14	G2	17	F3	PA0	I/O	FT_la	-	TIM2_CH1, USART2_CTS, USART4_TX, LCD_SEG42, COMP1_OUT, TIM2_ETR, EVENTOUT	OPAMP1_VINP, COMP1_INM3, ADC1_IN4, WKUP1, TAMP_IN2
6	-	-	-	-	-	-	-	PA0-CK_IN	I/O	FT_la	-	TIM2_CH1, USART2_CTS, USART4_TX, LCD_SEG42, COMP1_OUT, TIM2_ETR, EVENTOUT	OPAMP1_VINP, COMP1_INM3, ADC1_IN4, CK_IN, WKUP1, TAMP_IN2
7	E8	11	11	15	H2	18	E4	PA1	I/O	FT_la	-	TIM2_CH2, LPTIM1_CH2, SPI1_SCK, SPI2_SCK, USART2_RTS/USART2_DE, USART4_RX, LCD_SEG0, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, COMP1_INP3, ADC1_IN5, WKUP3, TAMP_IN5
8	G12	12	12	16	F3	19	H2	PA2	I/O	FT_la	-	TIM2_CH3, USART2_TX, LPUART1_TX, LCD_SEG1, COMP2_OUT, TIM15_CH1, EVENTOUT	COMP2_INM3, ADC1_IN6, WKUP4/ LSCO
9	E6	13	13	17	G3	20	J2	PA3	I/O	TT_la	-	TIM2_CH4, USART2_RX, LPUART1_RX, LCD_SEG2, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, COMP2_INP3, ADC1_IN7
-	-	-	-	18	C2	21	-	VSS	S	-	-	-	-
-	-	-	-	19	D2	22	G3	VDD	S	-	-	-	-

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
UFQFPN32	WLCSP42	LQFP48	UFQFPN48	LQFP64	UFBGA64	LQFP80	UFBGA81						
10	G10	14	14	20	H3	23	J3	PA4	I/O	TT_la	-	SPI1_NSS, SPI3_NSS, USART2_CK, LPUART3_TX, LCD_SEG43, LPTIM2_CH1, EVENTOUT	COMP1_INM4, COMP2_INM5, ADC1_IN8, DAC1_OUT1
11	E4	15	15	21	F4	24	H3	PA5	I/O	FT_la	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, USART3_TX, LPUART3_RX, LCD_SEG44, LPTIM2_ETR, EVENTOUT	COMP1_INM4, COMP2_INM5, ADC1_IN9
12	G8	16	16	22	G4	25	J4	PA6	I/O	FT_fla	-	TIM1_BKIN, TIM3_CH1, I2C2_SDA, I2C3_SDA, SPI1_MISO, COMP1_OUT, USART3_CTS, LPUART1_CTS, TSC_G5_IO1, LCD_SEG3, TIM16_CH1, EVENTOUT	ADC1_IN10
13	F7	17	17	23	H4	26	H4	PA7	I/O	FT_fla	-	TIM1_CH1N, TIM3_CH2, I2C2_SCL, I2C3_SCL, SPI1_MOSI, USART3_RX, LCD_SEG4, COMP2_OUT, LPTIM2_CH2, EVENTOUT	ADC1_IN14
-	-	-	-	24	H5	27	J5	PC4	I/O	FT_la	-	USART3_TX, LPUART3_TX, LCD_SEG22, EVENTOUT	COMP1_INM1, ADC1_IN15
-	-	-	-	25	H6	28	G4	PC5	I/O	FT_la	-	LPTIM3_CH3, USART3_RX, LPUART3_RX, LCD_SEG23, EVENTOUT	COMP1_INP1, ADC1_IN16, WKUP5, TAMP_IN4
14	F5	18	18	26	F5	29	F5	PB0	I/O	FT_la	-	TIM1_CH2N, TIM3_CH3, LPTIM3_CH1, SPI1_NSS, USART3_CK, LPUART2_CTS, TSC_G5_IO2, LCD_SEG5, COMP1_OUT, EVENTOUT	ADC1_IN17
15	F3	19	19	27	G5	30	H5	PB1	I/O	FT_la	-	TIM1_CH3N, TIM3_CH4, LPTIM3_CH2, USART3_RTS/USART3_DE, LPUART1_RTS_DE, TSC_SYNC, LPUART2_RTS_DE, LCD_SEG6, LPTIM2_IN1, EVENTOUT	COMP1_INM2, ADC1_IN18
-	G6	20	20	28	G6	31	J6	PB2	I/O	FT_la	-	RTC_OUT2, LPTIM1_CH1, LCD_VLCD, EVENTOUT	COMP1_INP2, RTC_OUT2
-	-	-	-	-	-	32	G5	PE7	I/O	FT_l	-	TIM1_ETR, LCD_SEG45, EVENTOUT	-
-	-	-	-	-	-	33	G6	PE8	I/O	FT_l	-	TIM1_CH1N, LCD_SEG46, EVENTOUT	-
-	-	-	-	-	-	34	H6	PE9	I/O	FT_l	-	TIM1_CH1, LPTIM1_CH3, LCD_SEG47, EVENTOUT	-
-	G4	21	21	29	G7	35	J7	PB10	I/O	FT_fl	-	TIM2_CH3, LPTIM3_CH1, I2C4_SCL, I2C2_SCL, SPI2_SCK, USART3_TX, LPUART1_RX, TSC_G5_IO3, LPUART2_RX, LCD_SEG10, COMP1_OUT, EVENTOUT	-
-	-	22	22	30	H7	36	H7	PB11	I/O	FT_fl	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, USART3_RX, LPUART1_TX, TSC_G5_IO4, LPUART2_TX, LCD_SEG11, COMP2_OUT, EVENTOUT	-
16	F1	23	23	31	D6	37	D4	VSS	S	-	-	-	-
17	G2	24	24	32	E6	38	D3	VDD	S	-	-	-	-
-	-	25	25	33	H8	39	J8	PB12	I/O	FT_l	-	TIM1_BKIN, SPI2_NSS, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, LCD_SEG12, TIM15_BKIN, EVENTOUT	-

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
UFQFPN32	WLCSP42	LQFP48	UFQFPN48	LQFP64	UFBGA64	LQFP80	UFBGA81						
-	-	26	26	34	G8	40	H8	PB13	I/O	FT_fl	-	TIM1_CH1N, LPTIM3_IN1, I2C2_SCL, SPI2_SCK, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, TIM15_CH1N, EVENTOUT	-
-	-	27	27	35	F8	41	J9	PB14	I/O	FT_fl	-	TIM1_CH2N, LPTIM3_ETR, I2C2_SDA, SPI2_MISO, USART3_RTS/USART3_DE, TSC_G1_IO3, LCD_SEG14, TIM15_CH1, EVENTOUT	-
-	-	28	28	36	F7	42	F7	PB15	I/O	FT_l	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, TSC_G1_IO4, LCD_SEG15, TIM15_CH2, EVENTOUT	WKUP7, TAMP_IN3
-	-	-	-	-	-	43	H9	PD8	I/O	FT_l	-	USART3_TX, LPUART3_TX, LCD_SEG28, EVENTOUT	-
-	-	-	-	-	-	44	G8	PD9	I/O	FT_l	-	LPTIM3_IN1, USART3_RX, LPUART3_RX, LCD_SEG29, EVENTOUT	-
-	-	-	-	-	-	45	G9	PD10	I/O	FT_la	-	LPTIM3_ETR, USART3_CK, TSC_G6_IO1, LCD_SEG30, LPTIM2_CH2, EVENTOUT	COMP2_INP4
-	-	-	-	-	-	46	F8	PD11	I/O	FT_l	-	USART3_CTS, LPUART3_CTS, TSC_G6_IO2, LCD_SEG31, LPTIM2_ETR, EVENTOUT	-
-	-	-	-	-	-	47	F9	PD12	I/O	FT_fl	-	I2C4_SCL, USART3_RTS/USART3_DE, LPUART3_RTS_DE, TSC_G6_IO3, LCD_SEG32, LPTIM2_IN1, EVENTOUT	-
-	-	-	-	-	-	48	E9	PD13	I/O	FT_fl	-	I2C4_SDA, TSC_G6_IO4, LCD_SEG33, LPTIM2_CH1, EVENTOUT	-
-	-	-	-	37	F6	49	E8	PC6	I/O	FT_la	-	TIM3_CH1, LPUART2_TX, TSC_G4_IO1, LCD_SEG24, EVENTOUT	COMP1_INP5
-	-	-	-	38	E7	50	E6	PC7	I/O	FT_l	-	TIM3_CH2, LPTIM3_CH4, LPUART2_RX, TSC_G4_IO2, LCD_SEG25, LPTIM2_CH2, EVENTOUT	-
-	-	-	-	39	E8	51	E5	PC8	I/O	FT_l	-	TIM3_CH3, LPTIM3_CH1, TSC_G4_IO3, LCD_SEG26, EVENTOUT	-
-	-	-	-	40	D8	52	D9	PC9	I/O	FT_l	-	TIM3_CH4, LPTIM3_CH2, TSC_G4_IO4, USB_NOE, LCD_SEG27, EVENTOUT	-
18	D3	29	29	41	D7	53	E7	PA8	I/O	FT_l	-	MCO, TIM1_CH1, MCO2, USART1_CK, TSC_G7_IO1, LCD_COM0, LPTIM2_CH1, EVENTOUT	-
19	C4	30	30	42	C7	54	D7	PA9	I/O	FT_fla	-	MCO, TIM1_CH2, I2C1_SCL, I2C2_SCL, USART1_TX, TSC_G7_IO2, LCD_COM1, TIM15_BKIN, EVENTOUT	COMP1_INP4
20	E2	31	31	43	C6	55	D8	PA10	I/O	FT_fl	-	TIM1_CH3, MCO2, I2C1_SDA, I2C2_SDA, SPI2_NSS, USART1_RX, TSC_G7_IO3, CRS_SYNC, LCD_COM2, EVENTOUT	-
21	D1	32	32	44	C8	56	C9	PA11 [PA9]	I/O	FT_u	(3)	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, SPI2_MISO, USART1_CTS, COMP1_OUT, EVENTOUT	USB_DM

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
UFQFPN32	WLCSP42	LQFP48	UFQFPN48	LQFP64	UFBGA64	LQFP80	UFBGA81						
22	C2	33	33	45	B8	57	C8	PA12 [PA10]	I/O	FT_u	(3)	TIM1_ETR, SPI1_MOSI, SPI2_MOSI, USART1_RTS/USART1_DE, EVENTOUT	USB_DP
23	B3	34	34	46	A8	58	B9	PA13 (SWDIO)	I/O	FT_l	(4)	SWDIO, IR_OUT, TSC_G7_IO4, USB_NOE, LCD_SEG40, EVENTOUT	-
-	A2	35	35	47	D5	59	D6	VSS	S	-	-	-	-
-	B1	36	36	48	E5	60	C7	VDDUSB	S	-	-	-	-
24	D5	37	37	49	A7	61	B8	PA14 (SWCLK)	I/O	FT_l	(4)	SWCLK, LPTIM1_CH1, TSC_G3_IO4, LCD_SEG41, EVENTOUT	-
25	A4	38	38	50	A6	62	A9	PA15	I/O	FT_l	-	TIM2_CH1, TIM2_ETR, USART2_RX, LPTIM3_IN2, SPI1_NSS, SPI3_NSS, USART3_RTS/USART3_DE, USART4_RTS/USART4_DE, TSC_G3_IO1, LCD_SEG17, LPTIM3_CH3, EVENTOUT	-
-	-	-	-	51	B7	63	A8	PC10	I/O	FT_l	-	LPTIM3_ETR, SPI3_SCK, USART3_TX, USART4_TX, TSC_G3_IO2, LCD_COM4/ LCD_SEG28/LCD_SEG48, EVENTOUT	-
-	-	-	-	52	B6	64	B7	PC11	I/O	FT_l	-	LPTIM3_IN1, SPI3_MISO, USART3_RX, USART4_RX, TSC_G3_IO3, LCD_COM5/ LCD_SEG29/LCD_SEG49, EVENTOUT	-
-	-	-	-	53	C5	65	A7	PC12	I/O	FT_l	-	LPTIM3_CH3, SPI3_MOSI, USART3_CK, USART4_CK, LCD_COM6/LCD_SEG30/ LCD_SEG50, EVENTOUT	-
-	-	-	-	-	-	66	A6	PD0	I/O	FT_l	-	SPI2_NSS, LCD_SEG34, EVENTOUT	-
-	-	-	-	-	-	67	B6	PD1	I/O	FT_l	-	LPTIM1_CH4, SPI2_SCK, LCD_SEG35, EVENTOUT	-
-	-	-	-	54	B5	68	C6	PD2	I/O	FT_l	-	TIM3_ETR, USART3_RTS/USART3_DE, TSC_SYNC, LCD_COM7/LCD_SEG31/LCD_SEG51, EVENTOUT	-
-	-	-	-	-	-	69	D5	PD3	I/O	FT_l	-	SPI2_MISO, USART2_CTS, LCD_SEG36, EVENTOUT	-
-	-	-	-	-	-	70	A5	PD4	I/O	FT_l	-	LPTIM1_CH3, SPI2_MOSI, USART2_RTS/ USART2_DE, LCD_SEG37, EVENTOUT	-
-	-	-	-	-	-	71	C5	PD5	I/O	FT_l	-	USART2_TX, LCD_SEG38, EVENTOUT	-
-	-	-	-	-	-	72	B5	PD6	I/O	FT_l	-	USART2_RX, LCD_SEG39, EVENTOUT	-
26	B5	39	39	55	A5	73	C4	PB3	I/O	FT_fla	-	TIM2_CH2, LPTIM1_CH3, I2C2_SCL, I2C3_SCL, SPI1_SCK, SPI3_SCK, USART1_RTS/USART1_DE, LCD_SEG7, EVENTOUT	COMP2_INM2
27	C6	40	40	56	A4	74	A3	PB4	I/O	FT_fla	-	LPTIM1_CH4, TIM3_CH1, I2C2_SDA, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS, LPUART3_RTS_DE, TSC_G2_IO1, LCD_SEG8, EVENTOUT	COMP2_INP1

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
UFQFPN32	WLCSP42	LQFP48	UFQFPN48	LQFP64	UFBGA64	LQFP80	UFBGA81						
28	A6	41	41	57	C4	75	A4	PB5	I/O	FT_l	-	LPTIM1_IN1, TIM3_CH2, SPI1_MOSI, SPI3_MOSI, USART1_CK, LPUART3_CTS, TSC_G2_IO2, LCD_SEG9, COMP2_OUT, TIM16_BKIN, EVENTOUT	-
-	-	-	-	-	-	-	F4	VSS	S		-	-	-
29	B7	42	42	58	D3	76	B4	PB6	I/O	FT_fa	-	LPTIM1_ETR, I2C4_SCL, I2C1_SCL, I2C2_SCL, LPUART3_TX, USART1_TX, TSC_G2_IO3, LPUART2_TX, TIM16_CH1N, EVENTOUT	COMP2_INP2
30	A8	43	43	59	C3	77	B3	PB7	I/O	FT_fla	-	LPTIM1_IN2, I2C4_SDA, I2C1_SDA, I2C2_SDA, LPUART3_RX, USART1_RX, USART4_CTS, TSC_G2_IO4, LPUART2_RX, LCD_SEG21, EVENTOUT	COMP2_INM1, PVD_IN
31	C8	44	44	60	B4	78	A2	PF3-BOOT0 (BOOT0)	I/O	FT	-	EVENTOUT	-
-	A10	45	45	61	B3	79	A1	PB8	I/O	FT_fl	-	LPTIM1_IN2, LPTIM3_IN2, I2C2_SCL, I2C1_SCL, USART3_TX, LCD_SEG16, TIM16_CH1, EVENTOUT	-
-	-	46	46	62	A3	80	B2	PB9	I/O	FT_fl	-	IR_OUT, LPTIM3_CH4, I2C2_SDA, I2C1_SDA, SPI2_NSS, USART3_RX, LCD_COM3, LPTIM1_CH4, EVENTOUT	-
32	A12	47	47	63	D4	1	F6	VSS	S	-	-	-	-
1	B11	48	48	64	E4	2	G7	VDD	S	-	-	-	-

1. *PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:*
   - *The speed should not exceed 2 MHz with a maximum load of 30 pF*
   - *These GPIOs must not be used as current sources (for example to drive a LED).*
2. *After an RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers. The RTC registers are not reset upon system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the RM0503 reference manual.*
3. *Pins PA9/PA10 can be remapped in place of pins PA11/PA12 (default mapping), using SYSCFG_CFGR1 register.*
4. *Upon reset, these pins are configured as SW debug alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.*

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4.3 Alternate functions

Table 13. Port A alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/ TIM1/2	I2C4/ LPTIM1/3/ TIM1/2/3	I2C2/4/ SYS_AF/ USART2	I2C1/2/3/4/ LPTIM3	I2C2/SPI1/2	COMP1/ LPUART3/ SPI2/3	USART1/2/3	LPUART1/2/3/ USART4	TSC	CRS/ LPUART2/USB	LCD	COMP1/2/LCD	-	LPTIM1/2/3/ TIM2/15/16	EVENTOUT
Port A	PA0	-	TIM2_CH1	-	-	-	-	-	USART2_CTS	USART4_TX	-	-	LCD_SEG42	COMP1_OUT	-	TIM2_ETR	EVENTOUT
	PA1	-	TIM2_CH2	LPTIM1_CH2	-	-	SPI1_SCK	SPI2_SCK	USART2_RTS/ USART2_DE	USART4_RX	-	-	LCD_SEG0	-	-	TIM15_CH1N	EVENTOUT
	PA2	-	TIM2_CH3	-	-	-	-	-	USART2_TX	LPUART1_TX	-	-	LCD_SEG1	COMP2_OUT	-	TIM15_CH1	EVENTOUT
	PA3	-	TIM2_CH4	-	-	-	-	-	USART2_RX	LPUART1_RX	-	-	LCD_SEG2	-	-	TIM15_CH2	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK	LPUART3_TX	-	-	LCD_SEG43	-	-	LPTIM2_CH1	EVENTOUT
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	USART3_TX	LPUART3_RX	-	-	LCD_SEG44	-	-	LPTIM2_ETR	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	I2C2_SDA	I2C3_SDA	SPI1_MISO	COMP1_OUT	USART3_CTS	LPUART1_CTS	TSC_G5_IO1	-	LCD_SEG3	-	-	TIM16_CH1	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	I2C2_SCL	I2C3_SCL	SPI1_MOSI	-	USART3_RX	-	-	-	LCD_SEG4	COMP2_OUT	-	LPTIM2_CH2	EVENTOUT
	PA8	MCO	TIM1_CH1	-	MCO2	-	-	-	USART1_CK	-	TSC_G7_IO1	-	LCD_COM0	-	-	LPTIM2_CH1	EVENTOUT
	PA9	MCO	TIM1_CH2	-	-	I2C1_SCL	I2C2_SCL	-	USART1_TX	-	TSC_G7_IO2	-	LCD_COM1	-	-	TIM15_BKIN	EVENTOUT
	PA10	-	TIM1_CH3	-	MCO2	I2C1_SDA	I2C2_SDA	SPI2_NSS	USART1_RX	-	TSC_G7_IO3	CRS_SYNC	LCD_COM2	-	-	-	EVENTOUT
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	SPI2_MISO	USART1_CTS	-	-	-	-	COMP1_OUT	-	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	SPI2_MOSI	USART1_RTS/ USART1_DE	-	-	-	-	-	-	-	EVENTOUT
	PA13	SWDIO	IR_OUT	-	-	-	-	-	-	-	TSC_G7_IO4	USB_NOE	LCD_SEG40	-	-	-	EVENTOUT
	PA14	SWCLK	LPTIM1_CH1	-	-	-	-	-	-	-	TSC_G3_IO4	-	LCD_SEG41	-	-	-	EVENTOUT
	PA15	-	TIM2_CH1	TIM2_ETR	USART2_RX	LPTIM3_IN2	SPI1_NSS	SPI3_NSS	USART3_RTS/ USART3_DE	USART4_RTS/ USART4_DE	TSC_G3_IO1	-	LCD_SEG17	-	-	LPTIM3_CH3	EVENTOUT

Table 14. Port B alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/ TIM1/2	I2C4/ LPTIM1/3/ TIM1/2/3	I2C2/4/ SYS_AF/ USART2	I2C1/2/3/4/ LPTIM3	I2C2/ SPI1/2	COMP1/ LPUART3/ SPI2/3	USART1/2/3	LPUART1/2/3/ USART4	TSC	CRS/ LPUART2/USB	LCD	COMP1/2/LCD	-	LPTIM1/2/3/ TIM2/15/16	EVENTOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	-	LPTIM3_CH1	SPI1_NSS	-	USART3_CK	LPUART2_CTS	TSC_G5_IO2	-	LCD_SEG5	COMP1_OUT	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	-	LPTIM3_CH2	-	-	USART3_RTS/ USART3_DE	LPUART1_RTS_DE	TSC_SYNC	LPUART2_RTS_DE	LCD_SEG6	-	-	LPTIM2_IN1	EVENTOUT
	PB2	RTC_OUT2	LPTIM1_CH1	-	-	-	-	-	-	-	-	-	LCD_VLCD	-	-	-	EVENTOUT
	PB3	-	TIM2_CH2	LPTIM1_CH3	I2C2_SCL	I2C3_SCL	SPI1_SCK	SPI3_SCK	USART1_RTS/ USART1_DE	-	-	-	LCD_SEG7	-	-		EVENTOUT
	PB4	-	LPTIM1_CH4	TIM3_CH1	I2C2_SDA	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS	LPUART3_RTS_DE	TSC_G2_IO1	-	LCD_SEG8	-	-		EVENTOUT
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	-	SPI1_MOSI	SPI3_MOSI	USART1_CK	LPUART3_CTS	TSC_G2_IO2	-	LCD_SEG9	COMP2_OUT	-	TIM16_BKIN	EVENTOUT
	PB6	-	LPTIM1_ETR	-	I2C4_SCL	I2C1_SCL	I2C2_SCL	LPUART3_TX	USART1_TX	-	TSC_G2_IO3	LPUART2_TX	-	-	-	TIM16_CH1N	EVENTOUT
	PB7	-	LPTIM1_IN2	-	I2C4_SDA	I2C1_SDA	I2C2_SDA	LPUART3_RX	USART1_RX	USART4_CTS	TSC_G2_IO4	LPUART2_RX	LCD_SEG21	-	-	-	EVENTOUT

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/ TIM1/2	I2C4/ LPTIM1/3/ TIM1/2/3	I2C2/4/ SYS_AF/ USART2	I2C1/2/3/4/ LPTIM3	I2C2/ SPI1/2	COMP1/ LPUART3/ SPI2/3	USART1/2/3	LPUART1/2/3/ USART4	TSC	CRS/ LPUART2/USB	LCD	COMP1/2/LCD	-	LPTIM1/2/3/ TIM2/15/16	EVENTOUT
Port B	PB8	-	LPTIM1_IN2	LPTIM3_IN2	I2C2_SCL	I2C1_SCL	-	-	USART3_TX	-	-	-	LCD_SEG16	-	-	TIM16_CH1	EVENTOUT
	PB9	-	IR_OUT	LPTIM3_CH4	I2C2_SDA	I2C1_SDA	SPI2_NSS	-	USART3_RX	-	-	-	LCD_COM3	-	-	LPTIM1_CH4	EVENTOUT
	PB10	-	TIM2_CH3	LPTIM3_CH1	I2C4_SCL	I2C2_SCL	SPI2_SCK	-	USART3_TX	LPUART1_RX	TSC_G5_IO3	LPUART2_RX	LCD_SEG10	COMP1_OUT	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	-	USART3_RX	LPUART1_TX	TSC_G5_IO4	LPUART2_TX	LCD_SEG11	COMP2_OUT	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	-	SPI2_NSS	-	USART3_CK	LPUART1_RTS_DE	TSC_G1_IO1	-	LCD_SEG12	-	-	TIM15_BKIN	EVENTOUT
	PB13	-	TIM1_CH1N	LPTIM3_IN1	-	I2C2_SCL	SPI2_SCK	-	USART3_CTS	LPUART1_CTS	TSC_G1_IO2	-	LCD_SEG13	-	-	TIM15_CH1N	EVENTOUT
	PB14	-	TIM1_CH2N	LPTIM3_ETR	-	I2C2_SDA	SPI2_MISO	-	USART3_RTS/ USART3_DE	-	TSC_G1_IO3	-	LCD_SEG14	-	-	TIM15_CH1	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	-	-	SPI2_MOSI	-	-	-	TSC_G1_IO4	-	LCD_SEG15	-	-	TIM15_CH2	EVENTOUT

Table 15. Port C alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/ TIM1/2	I2C4/ LPTIM1/3/ TIM1/2/3	I2C2/4/ SYS_AF/ USART2	I2C1/2/3/4/ LPTIM3	I2C2/SPI1/2	COMP1/ LPUART3/ SPI2/3	USART1/2/3	LPUART1/2/3/ USART4	TSC	CRS/ LPUART2/USB	LCD	COMP1/2/ LCD	-	LPTIM1/2/3/ TIM2/15/16	EVENTOUT
Port C	PC0	-	LPTIM1_IN1	I2C4_SCL	-	I2C3_SCL	-	-	-	LPUART1_RX	-	LPUART2_TX	LCD_SEG18	-	-	LPTIM2_IN1	EVENTOUT
	PC1	-	LPTIM1_CH1	I2C4_SDA	-	I2C3_SDA	-	-	-	LPUART1_TX	-	LPUART2_RX	LCD_SEG19	-	-	-	EVENTOUT
	PC2	MCO2	LPTIM1_IN2	-	-	-	SPI2_MISO	-	-	-	-	-	LCD_SEG20	-	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	LPTIM3_CH1	-	-	SPI2_MOSI	-	-	USART4_CK	-	-	LCD_VLCD	-	-	LPTIM2_ETR	EVENTOUT
	PC4	-	-	-	-	-	-	-	USART3_TX	LPUART3_TX	-	-	LCD_SEG22	-	-	-	EVENTOUT
	PC5	-	-	-	-	LPTIM3_CH3	-	-	USART3_RX	LPUART3_RX	-	-	LCD_SEG23	-	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	-	-	-	-	-	LPUART2_TX	TSC_G4_IO1	-	LCD_SEG24	-	-	-	EVENTOUT
	PC7	-	-	TIM3_CH2	-	LPTIM3_CH4	-	-	-	LPUART2_RX	TSC_G4_IO2	-	LCD_SEG25	-	-	LPTIM2_CH2	EVENTOUT
	PC8	-	-	TIM3_CH3	-	LPTIM3_CH1	-	-	-	-	TSC_G4_IO3	-	LCD_SEG26	-	-	-	EVENTOUT
	PC9	-	-	TIM3_CH4	-	LPTIM3_CH2	-	-	-	-	TSC_G4_IO4	USB_NOE	LCD_SEG27	-	-	-	EVENTOUT
	PC10	-	-	LPTIM3_ETR	-	-	-	SPI3_SCK	USART3_TX	USART4_TX	TSC_G3_IO2	-	LCD_COM4/ LCD_SEG28/ LCD_SEG48	-	-	-	EVENTOUT
	PC11	-	-	LPTIM3_IN1	-	-	-	SPI3_MISO	USART3_RX	USART4_RX	TSC_G3_IO3	-	LCD_COM5/ LCD_SEG29/ LCD_SEG49	-	-	-	EVENTOUT
	PC12	-	-	-	-	LPTIM3_CH3	-	SPI3_MOSI	USART3_CK	USART4_CK	-	-	LCD_COM6/ LCD_SEG30/ LCD_SEG50	-	-	-	EVENTOUT
	PC13	-	-	LPTIM1_CH3	-	LPTIM3_CH3	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	OSC32_EN	OSC_EN	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

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Table 16. Port D alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/ TIM1/2	I2C4/ LPTIM1/3/ TIM1/2/3	I2C2/4/ SYS_AF/ USART2	I2C1/2/3/4/ LPTIM3	I2C2/SPI1/2	COMP1/ LPUART3/ SPI2/3	USART1/2/3	LPUART1/2/3/ USART4	TSC	CRS/ LPUART2/ USB	LCD	COMP1/2/ LCD	-	LPTIM1/2/3/ TIM2/15/16	EVENTOUT
Port D	PD0	-	-	-	-	-	SPI2_NSS	-	-	-	-	-	LCD_SEG34	-	-	-	EVENTOUT
	PD1	-	LPTIM1_CH4	-	-	-	SPI2_SCK	-	-	-	-	-	LCD_SEG35	-	-	-	EVENTOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	USART3_RTS/ USART3_DE	-	TSC_SYNC	-	LCD_COM7/ LCD_SEG31/ LCD_SEG51	-	-	-	EVENTOUT
	PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS	-	-	-	LCD_SEG36	-	-	-	EVENTOUT
	PD4	-	LPTIM1_CH3	-	-	-	SPI2_MOSI	-	USART2_RTS/ USART2_DE	-	-	-	LCD_SEG37	-	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	LCD_SEG38	-	-	-	EVENTOUT
	PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	LCD_SEG39	-	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	LPUART3_TX	-	-	LCD_SEG28	-	-	-	EVENTOUT
	PD9	-	-	-	-	LPTIM3_IN1	-	-	USART3_RX	LPUART3_RX	-	-	LCD_SEG29	-	-	-	EVENTOUT
	PD10	-	-	-	-	LPTIM3_ETR	-	-	USART3_CK	-	TSC_G6_IO1	-	LCD_SEG30	-	-	LPTIM2_CH2	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	LPUART3_CTS	TSC_G6_IO2	-	LCD_SEG31	-	-	LPTIM2_ETR	EVENTOUT
	PD12	-	-	-	-	I2C4_SCL	-	-	USART3_RTS/ USART3_DE	LPUART3_RTS_DE	TSC_G6_IO3	-	LCD_SEG32	-	-	LPTIM2_IN1	EVENTOUT
	PD13	-	-	-	-	I2C4_SDA	-	-	-	-	TSC_G6_IO4	-	LCD_SEG33	-	-	LPTIM2_CH1	EVENTOUT

Table 17. Port E alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/TIM1/2	I2C4/LPTIM1/3/ TIM1/2/3	I2C2/4/ SYS_AF/ USART2	I2C1/2/3/4/ LPTIM3	I2C2/ SPI1/2	COMP1/ LPUART3/ SPI2/3	USART1/2/3	LPUART1/2/3/ USART4	TSC	CRS/ LPUART2/USB	LCD	COMP1/2/LCD		LPTIM1/2/3/ TIM2/15/16	EVENTOUT
Port E	PE3	-	-	TIM3_CH1	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	LCD_SEG45	-	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	LCD_SEG46	-	-	-	EVENTOUT
	PE9	-	TIM1_CH1	LPTIM1_CH3	-	-	-	-	-	-	-	-	LCD_SEG47	-	-	-	EVENTOUT

Table 18. Port F alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	LPTIM1/ SYS_AF/ TIM1/2	I2C4/LPTIM1/3/ TIM1/2/3	I2C2/4/ SYS_AF/ USART2	I2C1/2/3/4/ LPTIM3	I2C2/ SPI1/2	COMP1/ LPUART3/ SPI2/3	USART1/2/3	LPUART1/2/3/ USART4	TSC	CRS/ LPUART2/USB	LCD	COMP1/2/LCD		LPTIM1/2/3/ TIM2/15/16	EVENTOUT
Port F	PF0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PF1	OSC_EN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PF2	MCO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

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5 Memory mapping

Refer to the product line reference manual (RM0503) for details on the memory mapping as well as the boundary addresses for all peripherals.

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6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an junction temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} =V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 11.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 12.

Figure 11. Pin loading conditions

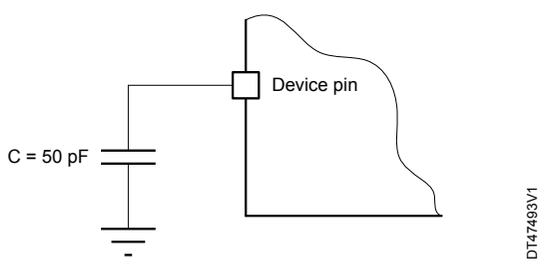
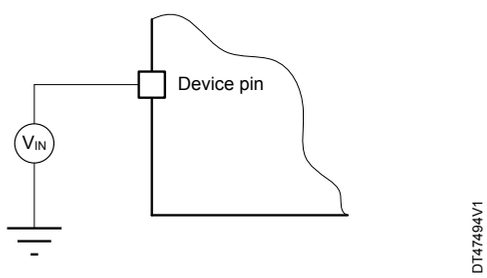


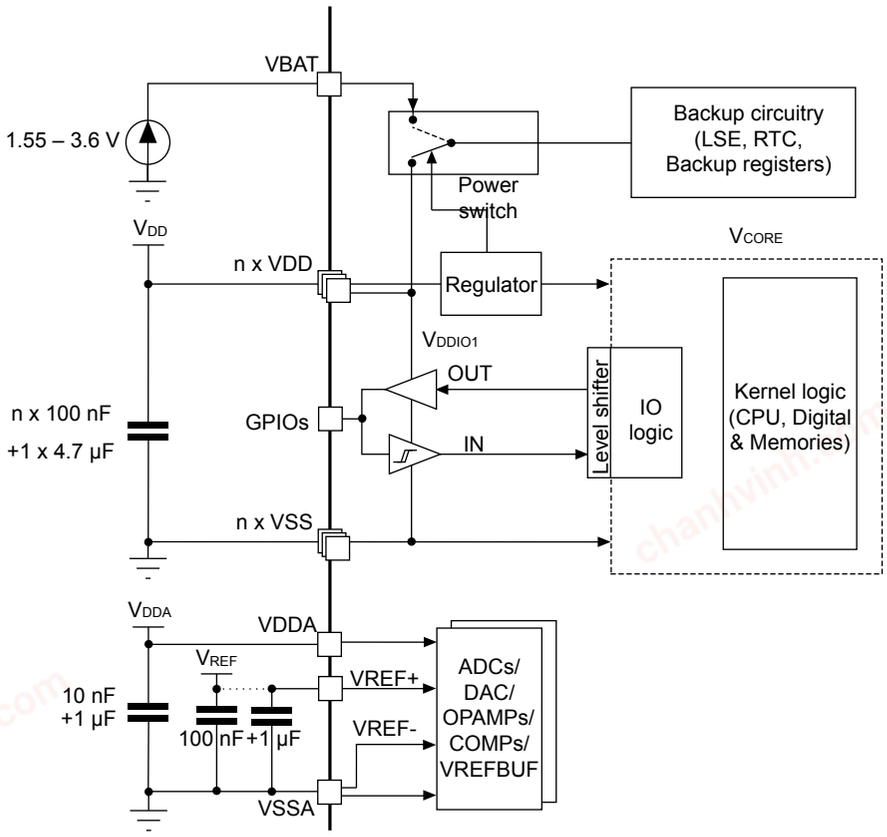
Figure 12. Pin input voltage



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6.1.6 Power supply scheme

Figure 13. **Power supply scheme**

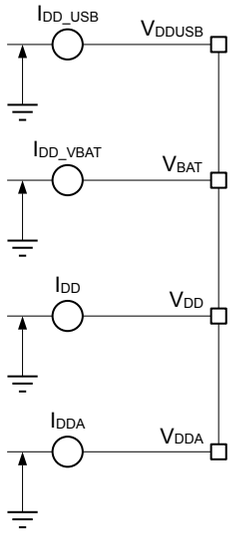


Caution: Each power supply pair (such as V_{DD}/V_{SS}, V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

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6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



The I_{DD_ALL} parameters given in Table 26. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, bypass mode, ART enabled (cache ON, prefetch OFF), HSE clock used as system clock to Table 43. Current consumption in VBAT mode represent the total MCU consumption including the current supplying V_{DD}, V_{DDA}, V_{DDUSB}, and V_{BAT}.

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 19. Voltage characteristics, Table 20. Current characteristics and Table 21. Thermal characteristics may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 19. Voltage characteristics

All main power (V_{DD}, V_{DDA}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDUSB}, V_{BAT}, V_{REF+})	-0.3	4.0	V
V_{IN}(1)	Input voltage on FT_xxx pins	V_{SS} - 0.3	min (V_{DD}, V_{DDA}, V_{DDUSB}) + 4.0(2)(3)	V
	Input voltage on TT_xx pins	V_{SS} - 0.3	4.0	
	Input voltage on any other pins	V_{SS} - 0.3	4.0	
$\lvert\Delta V_{DDX}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(4)	-	50	mV
V_{REF+} - V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	V

1. *V_{IN} maximum must always be respected. Refer to Table 20. Current characteristics for the maximum allowed injected current values.*
2. *To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.*
3. *This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.*
4. *Including VREF- pin.*

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Table 20. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	140	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)	140	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, RST	-5/+0(4)	
$\Sigma\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)	25	

1. *All main power (V_{DD}, V_{DDA}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.*
2. *This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.*
3. *Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.*
4. *A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to Table 19. Voltage characteristics for the maximum allowed input voltage values.*
5. *When several inputs are submitted to a current injection, the maximum $\Sigma\lvert I_{INJ(PIN)}\rvert$ is the absolute sum of the negative injected currents (instantaneous values).*

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	56	MHz
f_{PCLK}	Internal APB clock frequency	-	0	56	
V_{DD}	Standard operating voltage	-	1.71(1)	3.6	V
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		OPAMP used	1.8		
		ADC, OPAMP, COMP not used	0		
V_{BAT}	Backup domain supply voltage	-	1.55	3.6	
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	

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Symbol	Parameter	Conditions	Min	Max	Unit
		USB not used	0	3.6	V
V_{IN}	I/O input voltage	TT_xx I/Os	-0.3	V_{DDIOx} + 0.3	V
		All I/Os except TT_xx pins	-0.3	Min(Min(V_{DD}, V_{DDA}, V_{DDUSB}) + 3.6, 5.5)(2)(3)	
T_A	Ambient temperature for suffix 6	Maximum power dissipation	-40	85	°C
		Low-power dissipation(4)		105	
	Ambient temperature for suffix 3	Maximum power dissipation		125	
		Low-power dissipation(4)		130	
T_J	Junction temperature range	Suffix 6 version	-40	105	
		Suffix 3 version		130	

1. *When RESET is released, the functionality is guaranteed down to V_{BOR0} min.*
2. *This formula has to be applied only on the power supplies related to the I/O structure described by the pin definition table. The maximum I/O input voltage is the smallest value between Min (V_{DD}, V_{DDA}, V_{DDUSB}) + 3.6 V and 5.5 V.*
3. *For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDUSB}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled.*
4. *In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_J max (see Section 7.10: Package thermal characteristics).*

6.3.2 Operating conditions at power-up / power-down

The parameters given in Table 23 are derived from tests performed under the ambient temperature condition summarized in Section 6.3.1: General operating conditions.

Table 23. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate	ULPEN = 0	10	∞	
		ULPEN = 1	100	∞	ms/V
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	µs/V
	V_{DDUSB} fall time rate	-	10	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in Table 24. Embedded reset and power control block characteristics are derived from tests performed under the ambient temperature conditions summarized in Section 6.3.1: General operating conditions.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brownout reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brownout reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	

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Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{BOR2}	Brownout reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brownout reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brownout reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)[2]	BOR (except BOR0) and PVD consumption from V_{DD}[3]	-	-	1.1	1.6	µA
	BOR[3] (except BOR0) and PVD average consumption from V_{DD} with ENULP = 1	-	-	55	1000	nA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1)[2]	PVM1 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4)[2]	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. *Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.*
2. *Specified by design, not tested in production.*
3. *BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.*

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6.3.4 Embedded voltage reference

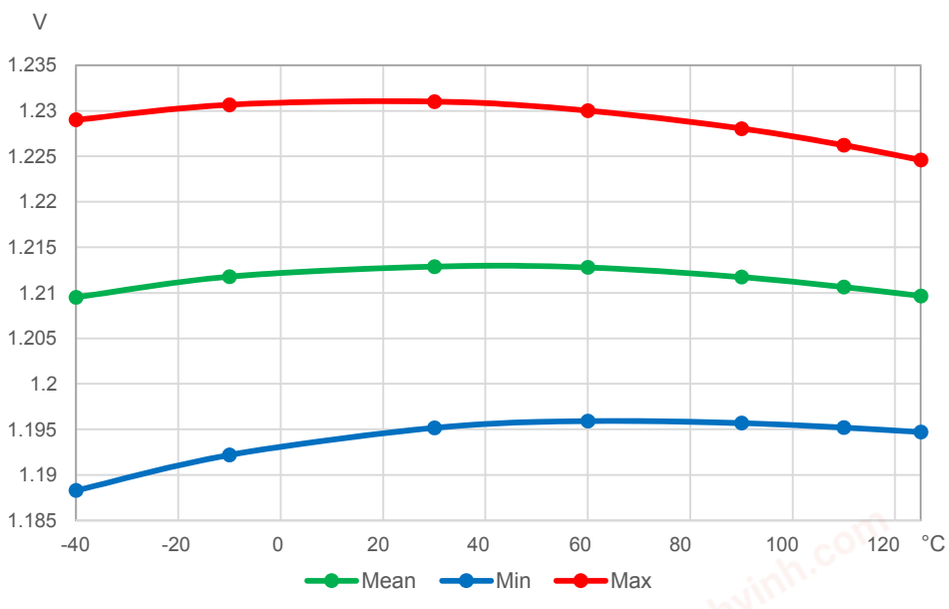
The parameters given in Table 25. Embedded internal voltage reference are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Table 25. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Temperature coefficient	-40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. *The shortest sampling time can be determined in the application by multiple iterations.*
2. *Specified by design, not tested in production.*

Figure 15. V_{REFINT} versus temperature



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6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Figure 14. Current consumption measurement scheme.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0503 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in Table 26 to Table 43 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

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Table 26. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, bypass mode, ART enabled (cache ON, prefetch OFF), HSE clock used as system clock

Symbol	Parameter	Conditions			Typ					Max(1)					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$, bypass mode, peripherals disabled	Range 1	48 MHz	3.75	3.75	3.85	3.95	4.10	4.1	4.15	4.3	4.5	4.9	mA
				32 MHz	2.55	2.55	2.60	2.70	2.90	2.8	2.85	2.95	3.15	3.5	
				24 MHz	1.95	1.95	2.05	2.10	2.30	2.15	2.2	2.3	2.5	2.85	
				16 MHz	1.35	1.35	1.40	1.50	1.65	1.45	1.5	1.65	1.8	2.15	
			Range 2	16 MHz	1.10	1.15	1.20	1.25	1.40	1.25	1.25	1.35	1.5	1.85	
				8 MHz	0.620	0.630	0.675	0.745	0.895	0.68	0.705	0.795	0.94	1.255	
				4 MHz	0.365	0.375	0.415	0.480	0.630	0.4	0.425	0.505	0.645	0.955	
				2 MHz	0.235	0.245	0.285	0.350	0.500	0.26	0.28	0.36	0.5	0.805	
				1 MHz	0.170	0.185	0.220	0.285	0.435	0.19	0.21	0.285	0.425	0.73	
				400 kHz	0.135	0.145	0.180	0.245	0.395	0.145	0.17	0.245	0.38	0.685	
				100 kHz	0.115	0.125	0.160	0.225	0.375	0.125	0.145	0.22	0.36	0.665	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.165	0.175	0.215	0.285	0.440	-	-	-	-	-	
				1 MHz	0.090	0.100	0.140	0.210	0.365	-	-	-	-	-	
				400 kHz	0.045	0.055	0.095	0.165	0.320	-	-	-	-	-	
				100 kHz	0.020	0.030	0.070	0.140	0.300	-	-	-	-	-	

1. *Evaluated by characterization, unless otherwise specified.*

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Table 27. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, ART enabled (cache ON, prefetch OFF), MSI clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max(1)					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	Range 1	48 MHz	3.75	3.85	3.95	4.10	4.35	4.15	4.4	4.6	4.8	5.25	mA
				32 MHz	2.55	2.65	2.70	2.80	3.00	2.8	2.95	3.1	3.35	3.75	
				24 MHz	1.95	2.00	2.10	2.20	2.35	2.15	2.25	2.4	2.6	3	
				16 MHz	1.35	1.40	1.45	1.55	1.70	1.5	1.55	1.7	1.9	2.25	
			Range 2	16 MHz	1.15	1.15	1.20	1.30	1.45	1.25	1.3	1.45	1.6	1.9	
				8 MHz	0.610	0.630	0.675	0.745	0.900	0.67	0.715	0.805	0.95	1.275	
				4 MHz	0.365	0.375	0.415	0.485	0.635	0.4	0.43	0.51	0.655	0.965	
				2 MHz	0.235	0.255	0.290	0.355	0.505	0.26	0.285	0.365	0.505	0.815	
				1 MHz	0.175	0.185	0.225	0.290	0.435	0.19	0.215	0.295	0.43	0.74	
				400 kHz	0.135	0.145	0.180	0.245	0.395	0.145	0.17	0.245	0.38	0.69	
				100 kHz	0.115	0.125	0.160	0.225	0.375	0.125	0.145	0.225	0.36	0.665	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.160	0.175	0.215	0.285	0.445	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.100	0.100	0.140	0.210	0.375	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.045	0.055	0.095	0.165	0.320	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.020	0.030	0.070	0.140	0.300	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

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Table 28. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, bypass mode, ART disabled (cache ON, prefetch OFF), HSE clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max(1)					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$, bypass mode , peripherals disabled	Range 1	48 MHz	4.30	4.35	4.45	4.55	4.75	4.75	4.85	5	5.2	5.6	mA
				32 MHz	2.95	3.00	3.05	3.15	3.30	3.25	3.3	3.45	3.6	4	
				24 MHz	2.65	2.65	2.70	2.80	3.00	2.9	2.95	3.1	3.3	3.65	
				16 MHz	1.80	1.85	2.00	2.00	2.15	2	2.05	2.15	2.35	2.7	
			Range 2	16 MHz	1.30	1.30	1.35	1.40	1.55	1.4	1.45	1.55	1.7	2	
				8 MHz	0.805	0.815	0.865	0.930	1.090	0.885	0.91	1	1.145	1.465	
				4 MHz	0.455	0.470	0.505	0.575	0.725	0.5	0.525	0.605	0.745	1.055	
				2 MHz	0.280	0.295	0.330	0.395	0.545	0.31	0.335	0.41	0.55	0.86	
				1 MHz	0.195	0.205	0.240	0.310	0.455	0.215	0.235	0.31	0.45	0.76	
				400 kHz	0.145	0.155	0.200	0.255	0.405	0.155	0.18	0.255	0.39	0.7	
				100 kHz	0.115	0.125	0.165	0.230	0.375	0.13	0.15	0.225	0.36	0.67	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.220	0.235	0.275	0.340	0.500	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.115	0.125	0.165	0.240	0.395	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.055	0.065	0.105	0.175	0.335	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.025	0.035	0.075	0.145	0.305	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

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Table 29. Current consumption in Run and Low-power run modes, code with data processing running from flash memory, bypass mode, ART disabled (cache ON, prefetch OFF), MSI clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max(1)					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	Range 1	48 MHz	4.35	4.45	4.60	4.70	4.95	4.8	5	5.25	5.5	6	mA
				32 MHz	2.95	3.05	3.15	3.25	3.45	3.25	3.4	3.6	3.85	4.3	
				24 MHz	2.65	2.70	2.80	2.90	3.10	2.9	3.05	3.25	3.45	3.9	
				16 MHz	1.80	1.85	1.95	2.05	2.25	2	2.1	2.25	2.45	2.85	
			Range 2	16 MHz	1.30	1.30	1.40	1.45	1.60	1.4	1.5	1.6	1.75	2.1	
				8 MHz	0.795	0.815	0.860	0.935	1.100	0.875	0.92	1	1.15	1.5	
				4 MHz	0.455	0.475	0.510	0.590	0.730	0.5	0.53	0.62	0.76	1.05	
				2 MHz	0.280	0.295	0.335	0.400	0.550	0.31	0.34	0.42	0.56	0.87	
				1 MHz	0.195	0.210	0.245	0.315	0.465	0.215	0.24	0.32	0.46	0.765	
				400 kHz	0.145	0.155	0.190	0.255	0.405	0.155	0.18	0.25	0.39	0.7	
				100 kHz	0.115	0.130	0.165	0.235	0.375	0.13	0.15	0.225	0.365	0.67	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.220	0.230	0.275	0.345	0.505	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.115	0.135	0.175	0.240	0.400	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.055	0.065	0.105	0.175	0.335	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.025	0.035	0.075	0.145	0.305	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

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Table 30. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, bypass mode, HSE clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max(1)					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$, bypass mode , peripherals disabled	Range 1	48 MHz	3.45	3.45	3.50	3.60	3.80	3.8	3.85	3.95	4.1	4.5	mA
				32 MHz	2.35	2.35	2.40	2.50	2.65	2.6	2.6	2.7	2.9	3.25	
				24 MHz	1.80	1.80	1.85	1.95	2.10	1.95	2	2.1	2.25	2.65	
				16 MHz	1.25	1.25	1.30	1.40	1.55	1.35	1.4	1.5	1.65	2	
			Range 2	16 MHz	1.05	1.05	1.10	1.15	1.30	1.15	1.2	1.25	1.4	1.7	
				8 MHz	0.580	0.595	0.630	0.700	0.845	0.64	0.665	0.745	0.88	1.2	
				4 MHz	0.345	0.355	0.395	0.460	0.610	0.38	0.4	0.48	0.615	0.925	
				2 MHz	0.225	0.235	0.275	0.340	0.485	0.25	0.27	0.35	0.485	0.79	
				1 MHz	0.165	0.180	0.215	0.290	0.425	0.185	0.205	0.28	0.42	0.725	
				400 kHz	0.130	0.140	0.180	0.245	0.390	0.145	0.165	0.24	0.38	0.685	
				100 kHz	0.115	0.125	0.160	0.225	0.375	0.125	0.145	0.225	0.36	0.665	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.070	0.080	0.120	0.190	0.350	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.040	0.050	0.090	0.160	0.315	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.020	0.030	0.070	0.145	0.295	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.010	0.020	0.060	0.135	0.290	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

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Table 31. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, MSI clock used as system clock

TBD stands for "to be defined".

Symbol	Parameter	Conditions			Typ					Max(1)					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	Range 1	48 MHz	3.50	3.55	3.65	3.75	3.95	3.85	3.95	4.15	4.35	4.8	mA
				32 MHz	2.35	2.40	2.50	2.60	2.75	2.6	2.7	2.85	3.05	3.45	
				24 MHz	1.80	1.85	1.90	2.00	2.20	2	2.05	2.2	2.4	2.8	
				16 MHz	1.25	1.30	1.35	1.40	1.60	1.35	1.45	1.55	1.75	2.1	
			Range 2	16 MHz	1.05	1.10	1.15	1.20	1.35	1.15	1.2	1.3	1.5	1.8	
				8 MHz	0.575	0.590	0.630	0.695	0.850	0.63	0.66	0.745	0.89	1.2	
				4 MHz	0.345	0.355	0.395	0.460	0.610	0.375	0.405	0.485	0.625	0.935	
				2 MHz	0.225	0.240	0.275	0.345	0.490	0.25	0.275	0.35	0.49	0.8	
				1 MHz	0.170	0.180	0.215	0.285	0.430	0.185	0.2	0.285	0.425	0.73	
				400 kHz	0.130	0.140	0.180	0.245	0.395	0.145	0.165	0.245	0.38	0.69	
				100 kHz	0.115	0.125	0.160	0.225	0.375	0.125	0.15	0.225	0.36	0.67	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run	2 MHz	0.070	0.080	0.120	0.190	0.355	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.040	0.050	0.090	0.160	0.320	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.020	0.030	0.070	0.145	0.295	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.010	0.020	0.060	0.130	0.290	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization, unless otherwise specified.*

Table 32. Typical current consumption in Run and Low-power run modes, with different codes running from flash memory, ART enabled (cache ON, prefetch OFF)

Symbol	Parameter	Conditions			Typical consumption				Typical consumption				Typical consumption			
		Clock source	Range	Code	25 °C, 1.8 V				25 °C, 3.0 V				25 °C, 3.6 V			
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disabled	Range 1, 48 MHz	Coremark	3640	µA	76	µA/ MHz	3760	µA	78	µA/ MHz	3830	µA	80	µA/ MHz
				Reduced code	3880		81		4060		85		4090		85	
				Dhrystone 2.1	3660		76		3830		80		3870		81	
				Fibonacci	3490		73		3650		76		3690		77	
				While(1)	2490		52		2610		54		2640		55	
			Range 2, 16 MHz	Coremark	1090		68		1130		71		1150		72	
				Reduced code	1160		73		1210		76		1220		76	

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Symbol	Parameter	Conditions			Typical consumption				Typical consumption				Typical consumption			
		Clock source	Range	Code	25 °C, 1.8 V				25 °C, 3.0 V				25 °C, 3.6 V			
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disabled	Range 2, 16 MHz	Dhrystone 2.1	1100	µA	69	µA/ MHz	1150	µA	72	µA/ MHz	1160	µA	73	µA/ MHz
				Fibonacci	1050		66		1080		68		1090		68	
				While(1)	780		49		810		51		820		51	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run, 2 MHz	Coremark	160		80		160		80		160		80	
				Reduced code	170		85		170		85		170		85	
				Dhrystone 2.1	160		80		160		80		160		80	
				Fibonacci	150		75		150		75		150		75	
				While(1)	110		55		110		55		110		55	

Table 33. Typical current consumption in Run and Low-power run modes, with different codes running from flash memory, ART disabled

Symbol	Parameter	Conditions			Typical consumption				Typical consumption				Typical consumption			
		Clock source	Range	Code	25 °C, 1.8 V				25 °C, 3.0 V				25 °C, 3.6 V			
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disabled	Range 1, 48 MHz	Coremark	4160	µA	87	µA/ MHz	4370	µA	91	µA/ MHz	4420	µA	92	µA/ MHz
				Reduced code	4310		90		4540		95		4590		96	
				Dhrystone 2.1	4200		88		4430		92		4480		93	
				Fibonacci	4190		87		4380		91		4440		93	
				While(1)	2490		52		2600		54		2620		55	
			Range 2, 16 MHz	Coremark	1240		78		1290		81		1300		81	
				Reduced code	1280		80		1330		83		1350		84	
				Dhrystone 2.1	1250		78		1300		81		1320		83	
				Fibonacci	1240		78		1300		81		1320		83	
				While(1)	780		49		810		51		820		51	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run, 2 MHz	Coremark	210		105		220		110		220		110	
				Reduced code	220		110		230		115		230		115	
				Dhrystone 2.1	220		110		220		110		220		110	
				Fibonacci	230		115		240		120		240		120	
				While(1)	110		55		110		55		110		55	

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Table 34. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions			Typical consumption				Typical consumption				Typical consumption			
		Clock source	Range	Code	25 °C, 1.8 V				25 °C, 3.0 V				25 °C, 3.6 V			
$I_{DD\ (Run)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, all peripherals disabled	Range 1, 48 MHz	Coremark	3340	µA	70	µA/ MHz	3480	µA	73	µA/ MHz	3510	µA	73	µA/ MHz
				Reduced code	3400		71		3540		74		3580		75	
				Dhrystone 2.1	3310		69		3450		72		3490		73	
				Fibonacci	3490		73		3630		76		3680		77	
				While(1)	2690		56		2810		59		2840		59	
			Range 2, 16 MHz	Coremark	1020		64		1060		66		1070		67	
				Reduced code	1030		64		1070		67		1080		68	
				Dhrystone 2.1	1010		63		1050		66		1060		66	
				Fibonacci	1060		66		1100		69		1110		69	
				While(1)	850		53		880		55		890		56	
$I_{DD\ (LPRun)}$	Supply current in Low-power run mode		Low-power run, 2 MHz	Coremark	138		69		138		69		138		69	
				Reduced code	140		70		140		70		140		70	
				Dhrystone 2.1	140		70		140		70		140		70	
				Fibonacci	140		70		150		75		150		75	
				While(1)	110		55		110		55		120		60	

Table 35. Current consumption in Sleep and Low-power sleep modes, flash memory ON, HSE clock used as system clock

Symbol	Parameter	Conditions			Typ					Max					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Sleep)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$, bypass mode, peripherals disabled	Range 1	48 MHz	1.25	1.25	1.30	1.40	1.60	1.4	1.4	1.5	1.7	2.05	mA
				32 MHz	0.885	0.900	0.910	1.00	1.20	0.975	1	1.1	1.25	1.6	
				24 MHz	0.695	0.710	0.755	0.835	1.00	0.765	0.795	0.89	1.05	1.4	
				16 MHz	0.505	0.520	0.565	0.640	0.810	0.555	0.585	0.68	0.84	1.2	
			Range 2	16 MHz	0.445	0.455	0.490	0.560	0.710	0.485	0.51	0.59	0.73	1.05	
				8 MHz	0.275	0.285	0.325	0.390	0.540	0.305	0.325	0.405	0.545	0.85	
				4 MHz	0.190	0.205	0.245	0.305	0.455	0.21	0.235	0.31	0.445	0.755	
				2 MHz	0.155	0.160	0.195	0.265	0.410	0.165	0.185	0.26	0.4	0.705	
				1 MHz	0.130	0.145	0.175	0.240	0.390	0.14	0.165	0.24	0.375	0.68	

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Symbol	Parameter	Conditions			Typ					Max					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Sleep)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE}$, bypass mode, peripherals disabled	Range 2	400 kHz	0.115	0.125	0.165	0.230	0.375	0.13	0.15	0.225	0.36	0.665	mA
				100 kHz	0.110	0.120	0.155	0.220	0.370	0.12	0.145	0.22	0.355	0.66	
$I_{DD\ (LPSleep)}$	Supply current in Low-power run mode		-	2 MHz	0.060	0.070	0.110	0.180	0.340	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.035	0.045	0.085	0.155	0.315	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.020	0.035	0.070	0.140	0.305	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.015	0.025	0.065	0.135	0.295	TBD	TBD	TBD	TBD	TBD	

Table 36. Current consumption in Sleep and Low-power sleep modes, flash memory ON, MSI clock used as system clock

Symbol	Parameter	Conditions			Typ					Max					Unit
		Clock source	Range	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Sleep)}$	Supply current in Run mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	Range 1	48 MHz	1.30	1.35	1.40	1.50	1.65	1.45	1.5	1.65	1.8	2.2	mA
				32 MHz	0.915	0.940	0.95	1.10	1.25	1	1.065	1.15	1.35	1.7	
				24 MHz	0.715	0.740	0.800	0.870	1.05	0.785	0.835	0.94	1.1	1.47	
				16 MHz	0.525	0.545	0.590	0.670	0.84	0.575	0.615	0.715	0.88	1.24	
			Range 2	16 MHz	0.455	0.475	0.515	0.585	0.735	0.5	0.535	0.625	0.765	1.08	
				8 MHz	0.275	0.280	0.320	0.385	0.535	0.295	0.32	0.4	0.54	0.85	
				4 MHz	0.190	0.200	0.240	0.305	0.450	0.21	0.235	0.31	0.445	0.755	
				2 MHz	0.150	0.160	0.200	0.265	0.410	0.165	0.19	0.265	0.4	0.705	
				1 MHz	0.130	0.140	0.180	0.245	0.400	0.145	0.165	0.24	0.375	0.685	
				400 kHz	0.115	0.125	0.165	0.230	0.375	0.125	0.15	0.225	0.36	0.665	
				100 kHz	0.110	0.120	0.155	0.220	0.370	0.12	0.14	0.215	0.355	0.655	
$I_{DD\ (LPSleep)}$	Supply current in Low-power run mode		-	2 MHz	0.060	0.070	0.110	0.180	0.345	TBD	TBD	TBD	TBD	TBD	
				1 MHz	0.040	0.050	0.090	0.160	0.315	TBD	TBD	TBD	TBD	TBD	
				400 kHz	0.025	0.035	0.070	0.145	0.305	TBD	TBD	TBD	TBD	TBD	
				100 kHz	0.015	0.025	0.065	0.135	0.295	TBD	TBD	TBD	TBD	TBD	

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Table 37. Current consumption in Sleep and Low-power sleep modes, flash memory in power-down mode

Symbol	Parameter	Conditions		Typ					Max					Unit
		Clock source	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (LPSleep)}$	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$, peripherals disabled	2 MHz	61.5	72.5	110	180	340	TBD	TBD	TBD	TBD	TBD	µA
			1 MHz	38.5	49.5	88.5	160	315	TBD	TBD	TBD	TBD	TBD	
			400 kHz	22.5	33.0	72.0	140	300	TBD	TBD	TBD	TBD	TBD	
			100 kHz	15.5	26.0	65.0	135	295	TBD	TBD	TBD	TBD	TBD	

Table 38. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions	Typ					Max					Unit
		V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 0)}$	Supply current in Stop 0 mode, RTC disabled	1.8 V	100	110	140	195	310	254	276	350	490	770	µA
		2.4 V	100	110	140	195	315	257	279	356	490	795	
		3.0 V	105	110	145	200	320	260	281	359	495	805	
		3.3 V	105	110	145	200	320	260	282	360	495	805	
		3.6 V	105	115	145	200	325	262	285	362	500	810	

Table 39. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 1)}$	Supply current in Stop 1 mode, RTC disabled	LCD disabled	EN_ULP = 0	1.8 V	3.20	10.5	39.5	91.5	200	8.10	27.5	99	230	500	µA
				2.4 V	3.20	10.5	39.5	91.5	210	8.10	27.5	100	230	520	
				3.0 V	3.30	10.5	39.5	92.5	210	8.00	27.5	100	230	530	
				3.3 V	3.30	11.0	40.0	93.5	215	8.00	27.5	100	235	535	
				3.6 V	3.35	11.0	40.0	93.5	215	8.10	27.5	100	235	535	
			EN_ULP = 1	1.8 V	3.20	10.5	39.5	92.0	195	8.10	27.5	100	230	495	
				2.4 V	3.20	10.5	39.5	91.5	205	8.10	27.5	99	230	520	
				3.0 V	3.30	10.5	39.5	92.5	210	8.00	27.5	100	230	530	
				3.3 V	3.30	10.5	40.0	93.0	210	8.00	27.5	100	230	530	
				3.6 V	3.35	11.0	40.0	93.5	215	8.10	27.5	100	235	535	

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Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 1)}$	Supply current in Stop 1 mode, RTC disabled	LCD enabled, clocked by LSI	EN_ULP = 0	1.8 V	3.50	11.0	39.5	92.0	200	9.00	29.0	100	230	500	µA
				2.4 V	3.60	11.0	39.5	92.0	210	9.00	29.0	100	230	525	
				3.0 V	3.70	11.0	40.0	93.0	210	9.00	29.0	100	230	530	
				3.3 V	3.80	11.5	40.5	93.5	215	10.0	29.0	100	235	535	
				3.6 V	3.90	11.5	40.5	94.5	215	10.0	30.0	100	235	535	
	Supply current in Stop 1 mode, RTC enabled	RTC clocked by LSI	EN_ULP = 0 LPCAL = 1	1.8 V	3.60	11.0	40.0	92.0	195	9.00	29.0	100	230	495	
				2.4 V	3.70	11.0	40.0	92.0	210	9.00	29.0	100	230	520	
				3.0 V	3.90	11.5	40.0	93.0	210	10.0	29.0	100	230	530	
				3.3 V	3.90	11.5	40.5	93.5	215	10.0	30.0	100	235	535	
				3.6 V	4.10	11.5	41.0	94.5	215	10.0	30.0	100	235	535	
		RTC clocked by LSE, bypassed at 32768 Hz, LCD disabled	EN_ULP = 0 LPCAL = 1	1.8 V	3.40	11.0	39.5	92.5	195	9.00	27.5	100	230	485	
				2.4 V	3.40	11.0	39.5	91.5	210	9.00	27.5	100	230	525	
				3.0 V	3.50	11.0	39.5	93.5	215	9.00	27.5	100	235	535	
				3.3 V	3.50	11.0	39.5	93.0	215	9.00	29.0	100	235	535	
				3.6 V	3.55	11.0	40.0	94.0	215	9.10	29.0	100	235	540	
			EN_ULP = 0 LPCAL = 0	1.8 V	3.50	11.0	39.5	92.5	195	9.00	29.0	100	230	485	
				2.4 V	3.60	11.0	39.5	92.0	210	9.00	29.0	100	230	530	
				3.0 V	3.80	11.0	40.0	93.0	215	10.0	29.0	100	230	535	
				3.3 V	3.80	11.5	40.0	93.5	215	10.0	29.0	100	235	535	
				3.6 V	4.00	11.5	40.5	94.5	215	10.0	30.0	101	235	540	
		RTC clocked by LSE quartz in low-drive mode, LCD disabled	EN_ULP = 0 LPCAL = 0	1.8 V	3.40	11.0	39.5	92.0	190	9.00	29.0	100	230	4800	
				2.4 V	3.70	11.0	39.5	92.5	210	9.00	29.0	100	230	5300	
				3.0 V	3.80	11.5	40.0	93.0	215	10.0	29.0	100	230	5350	
				3.3 V	3.90	11.5	40.5	93.5	215	10.0	29.0	100	235	5350	
				3.6 V	4.05	11.5	41.0	94.5	215	10.0	30.0	100	235	5400	
			EN_ULP = 0 LPCAL = 1	1.8 V	3.30	11.0	39.5	92.0	195	8.00	27.5	100	230	4850	
				2.4 V	3.40	11.0	39.5	92.0	210	9.00	27.5	100	230	5250	
				3.0 V	3.40	11.0	39.5	93.5	215	9.00	27.5	100	235	5350	
				3.3 V	3.50	11.0	40.0	93.5	215	9.00	29.0	100	235	5350	

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Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 1)}$	Supply current in Stop 1 mode, RTC enabled	RTC clocked by LSE quartz in low-drive mode, LCD disabled	EN_ULP = 0 LPCAL = 1	3.6 V	3.65	11.0	40.5	93.5	215	9.10	29.0	100	235	5350	µA
			EN_ULP = 1 LPCAL = 1	1.8 V	3.40	11.0	39.5	91.5	190	9.00	27.5	100	230	4800	
				2.4 V	3.40	11.0	39.5	92.0	210	9.00	27.5	100	230	5300	
				3.0 V	3.50	11.0	39.5	93.0	215	9.00	27.5	100	230	5350	
				3.3 V	3.50	11.0	40.0	93.5	215	9.00	29.0	100	235	5350	
				3.6 V	3.65	11.0	40.5	94.0	215	9.10	29.0	100	235	5350	
		RTC clocked by LSE quartz in low-drive mode, LCD enabled	-	1.8 V	3.30	11.0	39.5	92.0	190	8.00	27.5	100	230	4800	
				2.4 V	3.40	11.0	39.5	92.0	210	9.00	27.5	100	230	5300	
				3.0 V	3.50	11.0	39.5	93.0	210	9.00	27.5	100	230	5300	
				3.3 V	3.50	11.0	40.0	93.5	215	9.00	29.0	100	235	5350	
				3.6 V	3.65	11.0	40.5	94.0	215	9.10	29.0	100	235	5400	

Table 40. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 2)}$	Supply current in Stop 2 mode, RTC disabled	LCD disabled	EN_ULP = 0	1.8 V	695	2250	9550	22500	53000	2450	5650	24000	56000	130000	nA
				2.4 V	720	2350	9850	23000	54500	2500	5900	24500	57500	135000	
				3.0 V	750	2500	10000	23500	56000	2550	6200	25500	59500	140000	
				3.3 V	770	2550	10500	24000	57500	2550	6400	26000	60500	145000	
				3.6 V	805	2650	11000	25000	58500	2600	6650	27000	62000	145000	
			EN_ULP = 1	1.8 V	760	2250	8800	21500	52000	2450	5650	22000	54000	130000	
				2.4 V	775	2300	8950	22000	53500	2500	5700	22500	55500	135000	
				3.0 V	795	2300	9150	22500	55000	2550	5800	23000	56500	135000	
				3.3 V	805	2350	9250	23000	56000	2550	5850	23000	57500	140000	
				3.6 V	830	2400	9450	23500	57500	2600	6000	23500	58500	145000	
		LCD enabled, clocked by LSI	EN_ULP = 0	1.8 V	1000	2500	9100	22000	52500	2550	6250	22500	55000	130000	
				2.4 V	1100	2600	9250	22500	54000	2750	6500	23000	56500	135000	
				3.0 V	1200	2700	9550	23000	55500	2950	6800	24000	57500	140000	

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Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 2)}$	Supply current in Stop 2 mode, RTC disabled	LCD enabled, clocked by LSI	EN_ULP = 0	3.3 V	1250	2800	9700	23500	56500	3100	6950	24500	58500	140000	nA
				3.6 V	1300	2850	9950	24000	58000	3250	7200	25000	60000	145000	
	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI, LCD disabled	EN_ULP = 0 LPCAL = 1	1.8 V	1100	2600	9150	22000	52500	2750	6500	23000	55000	130000	
				2.4 V	1200	2700	9400	22500	54000	3000	6800	23500	56500	135000	
				3.0 V	1300	2850	9700	23000	55500	3300	7150	24000	58000	140000	
				3.3 V	1400	2950	9850	23500	56500	3500	7350	24500	59000	140000	
				3.6 V	1450	3050	10000	24000	58000	3650	7650	25500	60000	145000	
		RTC clocked by LSE , bypassed at 32768 Hz, LCD disabled	EN_ULP = 0 LPCAL = 1	1.8 V	830	2350	9000	22000	53000	2550	5850	22500	55000	130000	
				2.4 V	870	2400	9200	22500	54500	2600	6000	23000	56500	135000	
				3.0 V	935	2450	9400	23000	56500	2650	6200	23500	58000	140000	
				3.3 V	955	2550	9600	23500	57000	2700	6300	24000	59000	145000	
				3.6 V	995	2600	9800	24000	58500	2750	6550	24500	60000	145000	
			EN_ULP = 0 LPCAL = 0	1.8 V	985	2500	9050	22000	53000	2450	6250	22500	55500	130000	
				2.4 V	1100	2600	9350	22500	54500	2750	6550	23500	56500	135000	
				3.0 V	1250	2750	9650	23000	56500	3100	6950	24000	58000	140000	
				3.3 V	1300	2850	9850	23500	57500	3250	7150	24500	59000	145000	
				3.6 V	1400	3000	10000	24000	58500	3500	7500	25000	60500	145000	
		RTC clocked by LSE quartz in low-drive mode, LCD disabled	EN_ULP = 0 LPCAL = 0	1.8 V	840	2550	9850	22500	54500	2100	6450	24500	57000	135000	
				2.4 V	1100	2750	10000	23500	57000	2800	6900	25500	59000	140000	
				3.0 V	1250	3000	11000	24500	59000	3100	7500	27000	61000	150000	
				3.3 V	1300	3150	11000	25000	60500	3300	7850	28000	62000	150000	
				3.6 V	1400	3350	11500	25500	61500	3550	8400	28500	63500	155000	
			EN_ULP = 0 LPCAL = 1	1.8 V	890	2400	9000	22000	52500	2200	6050	22500	54500	130000	
				2.4 V	945	2450	9200	22500	54000	2350	6150	23000	56000	135000	
				3.0 V	985	2500	9400	23000	56000	2450	6300	23500	57500	140000	
				3.3 V	1000	2550	9550	23000	56500	2550	6450	24000	58000	140000	
				3.6 V	1050	2650	9750	24000	57500	2650	6600	24500	59500	145000	
			EN_ULP = 1 LPCAL = 1	1.8 V	825	2400	9700	22500	54000	2050	6050	24000	56500	135000	
				2.4 V	885	2500	10000	23000	56000	2200	6300	25000	58000	140000	
				3.0 V	940	2700	10500	24000	58500	2350	6750	26000	60000	145000	

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Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Stop\ 2)}$	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSE quartz in low-drive mode, LCD disabled	EN_ULP = 1 LPCAL = 1	3.3 V	975	2800	10500	24500	59500	2450	7000	27000	61500	150000	nA
				3.6 V	1050	2900	11000	25000	60500	2600	7250	27500	62500	150000	
		RTC clocked by LSE quartz in low-drive mode, LCD enabled	-	1.8 V	890	2400	9050	22000	52500	2200	6050	22500	54500	130000	
				2.4 V	945	2450	9150	22500	54000	2350	6150	23000	56000	135000	
				3.0 V	985	2500	9400	23000	56000	2450	6300	23500	57500	140000	
				3.3 V	1000	2550	9500	23500	56500	2550	6450	23500	58500	140000	
				3.6 V	1050	2650	9750	23500	57500	2650	6600	24500	59500	145000	

Table 41. Current consumption in Standby mode

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Standby)}$	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog	EN_ULP = 0	1.8 V	30.5	195	1200	3700	9400	77.5	485	3050	9300	23500	nA
				2.4 V	48.0	260	1550	4300	11000	120	650	3900	11000	27000	
				3.0 V	68.5	345	2000	5050	12000	170	865	5050	12500	30500	
				3.3 V	82.0	395	2250	5450	13000	205	990	5650	13500	32500	
				3.6 V	105	460	2550	5750	14000	260	1150	6400	14500	34500	
			EN_ULP = 1	1.8 V	100	235	1050	3050	8750	250	585	2600	7600	22000	
				2.4 V	115	265	1200	3450	10000	285	665	2950	8600	25000	
				3.0 V	130	305	1350	3900	11000	320	765	3400	9800	28000	
				3.3 V	135	330	1450	4250	12000	345	830	3600	10500	29500	
				3.6 V	150	370	1550	4500	12500	380	925	3900	11000	31500	
		Independent watchdog	EN_ULP = 0	1.8 V	195	335	1150	3150	8800	490	835	2850	7850	22000	
				2.4 V	215	375	1300	3600	10000	545	945	3250	8950	25500	
				3.0 V	240	425	1500	4000	11500	605	1050	3700	10000	28500	
				3.3 V	260	460	1600	4350	12000	650	1150	4000	11000	30000	
				3.6 V	280	505	1700	4700	13000	700	1250	4300	11500	32000	
$I_{DD\ (Standby\ with\ RTC)}$	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	EN_ULP = 0	1.8 V	195	335	1150	3150	8750	490	840	2850	7850	22000	
				2.4 V	220	380	1300	3600	10000	545	945	3250	8950	25500	
				3.0 V	245	430	1500	4050	11500	610	1050	3700	10000	28500	

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Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	EN_ULP = 0	3.3 V	260	460	1600	4350	12000	655	1150	4000	11000	30000	nA
				3.6 V	285	505	1700	4650	13000	710	1250	4250	11500	32000	
		RTC clocked by LSI, independent watchdog	EN_ULP = 0	1.8 V	200	340	1150	3150	8850	500	850	2850	7900	22000	
				2.4 V	225	385	1300	3600	10000	560	960	3250	9000	25500	
				3.0 V	245	435	1500	4050	11500	620	1100	3700	10000	28500	
				3.3 V	265	465	1600	4350	12000	665	1150	4000	11000	30000	
				3.6 V	290	515	1750	4700	13000	720	1300	4350	11500	32000	
		RTC clocked by LSE, bypassed at 32768 Hz	LPCAL = 0	1.8 V	155	290	1100	3150	8800	385	725	2750	7850	22000	
				2.4 V	195	355	1300	3600	10000	495	885	3200	9000	25500	
				3.0 V	245	430	1500	4100	11500	615	1050	3750	10500	28500	
				3.3 V	280	475	1600	4500	12000	695	1200	4050	11000	30500	
				3.6 V	315	540	1750	4800	13000	785	1350	4400	12000	33000	
		RTC clocked by LSE quartz in low-drive mode	EN_ULP = 0 LPCAL = 0	1.8 V	245	565	1400	3400	9550	620	1400	3450	8550	24000	
				2.4 V	510	680	1600	3900	11000	1250	1700	4050	9750	28000	
				3.0 V	625	820	1900	4550	12500	1550	2050	4750	11500	31500	
				3.3 V	690	905	2050	4900	13500	1750	2250	5150	12000	33500	
				3.6 V	770	1000	2250	5200	14000	1900	2500	5600	13000	35500	
			EN_ULP = 0 LPCAL = 1	1.8 V	230	400	1200	3250	9050	580	1000	3050	8100	22500	
				2.4 V	280	450	1400	3700	10500	705	1100	3450	9200	26000	
				3.0 V	320	510	1600	4200	11500	800	1300	3950	10500	29000	
				3.3 V	345	555	1650	4550	12500	865	1400	4200	11500	31000	
				3.6 V	380	615	1850	4800	13000	955	1550	4600	12000	33000	
			EN_ULP = 1 LPCAL = 1	1.8 V	160	360	1400	3900	11000	400	900	3500	9800	27500	
				2.4 V	215	440	1750	4550	13000	540	1100	4400	11500	32500	
				3.0 V	260	550	2250	5300	14500	650	1350	5600	13000	37000	
				3.3 V	285	620	2500	5700	15500	720	1550	6250	14000	39000	
				3.6 V	330	700	2800	6050	16500	825	1750	7000	15000	41500	
I_{DD} (SRAM2)	Supply current to be added in Standby mode when SRAM2 is retained		-	1.8 V	89.0	190	605	1400	3200	225	470	1500	3550	8050	
				2.4 V	90.0	190	605	1400	3250	225	470	1500	3550	8050	
				3.0 V	90.0	190	610	1450	3250	225	475	1500	3550	8100	

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Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (SRAM2)}$	Supply current to be added in Standby mode when SRAM2 is retained	-		3.3 V	90.0	190	620	1450	3300	225	475	1550	3500	8250	nA
				3.6 V	90.5	190	640	1500	3400	225	480	1600	3550	8500	

Table 42. Current consumption in Shutdown mode

Symbol	Parameter	Conditions			Typ					Max					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (Shutdown)}$	Supply current in Shutdown mode (backup registers retained), RTC disabled	-	EN_ULP = 0	1.8 V	10.0	92.5	595	1950	5950	42	280	2000	7050	25500	nA
				2.4 V	41.5	135	725	2250	7100	105	400	2400	8200	28500	
				3.0 V	52.5	165	840	2600	7900	145	495	2850	9500	32000	
				3.3 V	53.5	175	910	2800	8450	160	540	3100	10000	34000	
				3.6 V	65.0	205	1000	3050	9100	190	620	3350	11000	36500	
$I_{DD\ (Shutdown\ with\ RTC)}$	Supply current in Shutdown mode (backup registers retained), RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	-	1.8 V	67.0	150	660	2050	6150	195	370	1650	5100	15500	
				2.4 V	120	220	820	2400	7350	305	550	2050	5950	18500	
				3.0 V	165	285	980	2750	8200	420	710	2450	6950	20500	
				3.3 V	195	320	1050	3000	8850	485	800	2700	7500	22000	
				3.6 V	225	370	1200	3200	9550	565	930	3000	8050	24000	
		RTC clocked by LSE quartz	EN_ULP = 0 LPCAL = 0	1.8 V	160	425	955	2300	12000	400	1050	2400	5800	30000	
				2.4 V	425	535	1150	2700	13000	1050	1350	2850	6750	32500	
				3.0 V	535	665	1350	3150	14000	1350	1650	3400	7850	35000	
				3.3V	600	740	1500	3400	15500	1500	1850	3750	8550	38500	
				3.6 V	675	835	1650	3650	17000	1700	2100	4100	9200	42500	
			EN_ULP = 0 LPCAL = 1	1.8 V	145	260	785	2150	12000	360	655	1950	5400	30000	
				2.4 V	200	310	915	2450	13500	500	770	2300	6150	33500	
				3.0 V	235	360	1050	2850	14500	585	900	2650	7100	36000	
				3.3 V	255	395	1150	3050	16000	640	985	2850	7650	40000	
				3.6 V	290	445	1250	3250	17000	720	1100	3150	8200	42500	

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Table 43. Current consumption in VBAT mode

Symbol	Parameter	Conditions			TYP					MAX					Unit
		-	-	VBAT	25 °C	55 °C	85 °C	105 °C	125 °C	30 °C	55 °C	85 °C	105 °C	130 °C	
$I_{DD\ (VBAT)}$	Supply current in VBAT mode	RTC disabled	-	1.8 V	9.00	22.5	190	700	2600	25.5	56.5	470	1750	6550	nA
				2.4 V	10.5	36.5	230	815	2950	27.5	91.5	570	2050	7450	
				3.0 V	13	44	270	945	3350	33.5	110	675	2350	8450	
				3.3 V	13	47.5	295	100	3600	33.5	120	735	2550	9000	
				3.6 V	15.5	56	330	110	3850	40.5	140	820	2800	9650	
		RTC clocked by LSE, bypassed at 32768 Hz	-	1.8 V	53	73.5	200	535	1550	13.5	185	505	1350	3900	
				2.4 V	86	110	260	645	1800	21.5	275	655	1600	4550	
				3.0 V	120	150	330	775	2100	305	380	820	1950	5300	
				3.3 V	140	175	370	860	2300	355	440	930	2150	5750	
				3.6 V	165	205	430	960	2500	415	520	1050	2400	6300	
		RTC clocked by LSE quartz in low-drive mode	LPCAL = 0	1.8 V	130	190	380	905	2900	320	475	950	2250	7200	
				2.4 V	165	215	435	100	3250	415	545	1100	2550	8100	
				3.0 V	205	250	500	115	3650	510	625	1250	2950	9150	
				3.3 V	220	270	540	125	3900	550	675	1350	3150	9750	
				3.6 V	240	300	595	1350	4200	605	745	1500	3450	10500	
			LPCAL = 1	1.8 V	130	355	545	905	2900	320	885	1350	2250	7200	
				2.4 V	300	445	665	100	3250	750	1100	1650	2550	8100	
				3.0 V	505	555	810	115	3650	1250	1400	2050	2950	9150	
				3.3 V	565	620	895	125	3900	1400	1550	2250	3150	9800	
				3.6 V	630	690	995	1350	4200	1550	1750	2500	3450	10500	

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6.3.5.1 *I/O system current consumption*

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull resistors generate a current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in Table 64. I/O static characteristics.

For the output pins, any internal or external pull-up or pull-down resistor and external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see Table 44. Peripheral current consumption), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the internal or external capacitive load connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

6.3.5.2 *On-chip peripheral current consumption*

The current consumption of the on-chip peripherals is given in Table 44. Peripheral current consumption. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in Table 19. Voltage characteristics
- The power consumption of the digital part of the on-chip peripherals is given in Table 44. Peripheral current consumption. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

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Table 44. Peripheral current consumption

Peripheral		Range 1	Range 2	Unit
AHB	Bus matrix(1)	0.40	0.40	µA/MHz
	ADC	1.90	0.40	
	CRC	0.50	0.42	
	DMA1	5.44	4.52	
	DMA2	5.28	4.39	
	DMA1+DMA2	6.76	5.63	
	GPIOA(2)	0.08	0.07	
	GPIOB(2)	0.08	0.07	
	GPIOC(2)	0.07	0.06	
	GPIOD(2)	0.06	0.04	
	GPIOE(2)	0.05	0.04	
	GPIOF(2)	0.05	0.04	
	AES	0.05	0.01	
	RNG	1.21	NA	
	TSC	2.72	2.26	
	ALL AHB bridges	**18.1**	**15.1**	
APB	AHB to APB bridge(3)	0.27	0.21	
	RTCA	4.12	3.41	
	I2C1(4)	0.80	0.65	
	I2C1(5)	2.63	0.73	
	I2C2	0.94	0.77	
	I2C3(4)	0.66	0.54	
	I2C3(5)	2.20	0.61	
	I2C4	0.89	0.73	
	USART1(4)	8.64	7.19	
	USART1(5)	2.46	2.06	
	USART2(4)	2.23	1.85	
	USART2(5)	2.30	1.92	
	USART3(4)	2.32	1.93	
	USART3(5)	2.32	1.93	
	USART4	2.30	1.90	
	LPUART1(4)	1.47	1.22	
	LPUART1(5)	1.55	1.30	
	LPUART2(4)	5.01	4.18	
	LPUART2(5)	2.06	1.72	
	LPUART3(4)	1.92	1.58	
	LPUART3(5)	1.99	1.65	
	LPTIM1(4)	2.06	1.71	
	LPTIM1(5)	2.13	1.78	

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Peripheral		Range 1	Range 2	Unit
APB	LPTIM2(4)	1.37	1.13	µA/MHz
	LPTIM2(5)	1.44	1.21	
	LPTIM3(4)	2.02	1.67	
	LPTIM3(5)	2.10	1.75	
	OPAMP	0.27	0.21	
	DAC	1.02	0.83	
	PWR	0.66	0.54	
	SPI1	1.75	1.45	
	SPI2	1.74	1.44	
	SPI3	1.71	1.41	
	TIM1	0.64	0.54	
	TIM2	5.36	4.45	
	TIM3	4.23	3.52	
	TIM6	0.86	0.71	
	TIM7	0.86	0.70	
	TIM15	0.49	0.41	
	TIM16	2.46	2.05	
	WWDG	0.38	0.29	
	SYSCFG	0.32	0.27	
	USB	3.67	NA	
	LCD	0.55	0.45	
	ALL APB bridges	**46.0**	**38.5**	

1. *The BusMatrix is automatically active when at least one master is ON (CPU, DMA).*
2. *The GPIOx (x= A…F) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).*
3. *The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.*
4. *Independent clock domain.*
5. *Clock domain.*

6.3.6 Wake-up time from low-power modes and voltage scaling transition times

The wake-up times given in Table 45 are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait for event) instruction.

Table 45. Low-power mode wake-up timings

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wake-up time from Low-power sleep mode to Low-power run mode	Wake-up in flash with flash in power-down during low-power sleep mode (SLEEP_PD = 1 in FLASH_ACR) and with clock MSI = 2 MHz		6	8.3	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in flash	Range 1 or range 2	Wake-up clock MSI = 24 MHz	6.3	6.7	µs

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Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in flash	Range 1 or range 2	Wake-up clock HSI16 = 16 MHz	6.5	6.7	µs
			Wake-up clock MSI = 1 MHz	33.0	36.0	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1 or range 2	Wake-up clock MSI = 24 MHz	1.92	2.30	
			Wake-up clock HSI16 = 16 MHz	1.90	2.00	
			Wake-up clock MSI = 1 MHz	19.0	22.0	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in flash	Range 1 or range 2	Wake-up clock MSI = 24 MHz	11.5	17.5	µs
			Wake-up clock HSI16 = 16 MHz	11.0	13.5	
			Wake-up clock MSI = 1 MHz	35.0	38.4	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1 or range 2	Wake-up clock MSI = 24 MHz	7.2	13.0	
			Wake-up clock HSI16 = 16 MHz	6.9	8.8	
			Wake-up clock MSI = 1 MHz	21.9	25.0	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in flash	Range 1 or range 2	Wake-up clock MSI = 24 MHz	12.0	16.5	µs
			Wake-up clock HSI16 = 16 MHz	13.4	17.0	
			Wake-up clock MSI = 1 MHz	40.0	43.5	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1 or range 2	Wake-up clock MSI = 24 MHz	7.67	12.0	
			Wake-up clock HSI16 = 16 MHz	11.0	17.0	
			Wake-up clock MSI = 1 MHz	26.0	29.0	
t_{WUSTBY}	Wake-up time from Standby mode to Run mode	Range 1	Wake-up clock MSI = 4 MHz	62.0	67.0	µs
			Wake-up clock MSI = 1 MHz	63.0	67.0	
t_{WUSHDN}	Wake-up time from Shutdown mode to Run mode	Range 1	Wake-up clock MSI = 4 MHz	292	360	µs

Table 46. Regulator mode transition times

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wake-up time from Low-power run mode to Run mode(1)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(2)	Code run with MSI 16 MHz	20	40	

1. *Time until REGLPF flag is cleared in PWR_SR2.*
2. *Time until VOSF flag is cleared in PWR_SR2.*

Table 47. Wake-up time using USART/LPUART

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wake-up time needed to calculate the maximum USART/LPUART baud rate allowing to wake up up from stop mode when USART/LPUART clock source is HSI	Stop 0 mode	-	1.7	µs
		Stop 1 mode and Stop 2 mode	-	8.5	

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6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

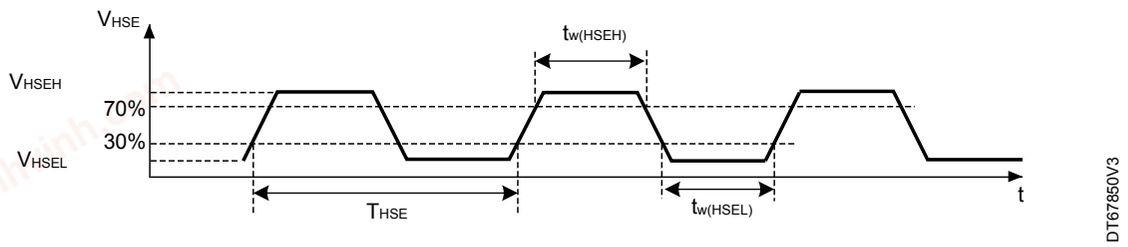
The external clock signal has to respect the I/O characteristics in Section 6.3.14: I/O port characteristics. However, the recommended clock input waveform is shown in Figure 16. AC timing diagram for high-speed external clock source .

Table 48. High-speed external user clock characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	19	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

Figure 16. AC timing diagram for high-speed external clock source



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in Section 6.3.14: I/O port characteristics. However, the recommended clock input waveform is shown in Figure 17. AC timing diagram for low-speed external clock source.

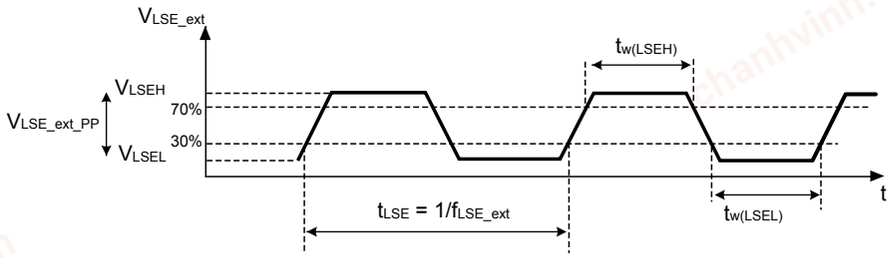
Table 49. Low-speed external user clock characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

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Figure 17. **AC timing diagram for low-speed external clock source**



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in Table 50. HSE oscillator characteristics. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 50. **HSE oscillator characteristics**

Specified by design, not tested in production.

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup[2]	-	-	5.5	mA
		V_{DD} = 3 V, R_m = 30 Ω, C_L = 10 pF @ 8 MHz	-	0.58	-	
		V_{DD} = 3 V, R_m = 45 Ω, C_L = 10 pF @ 8 MHz	-	0.59	-	
		V_{DD} = 3 V, R_m = 30 Ω, C = 5 pF @ 48 MHz	-	0.89	-	
		V_{DD} = 3 V, R_m = 30 Ω, C_L = 10 pF @ 48 MHz	-	1.14	-	
		V_{DD} = 3 V, R_m = 30 Ω, C_L = 20 pF @ 48 MHz	-	1.94	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$[3]	Startup time	V_{DD} is stabilized	-	2	-	ms

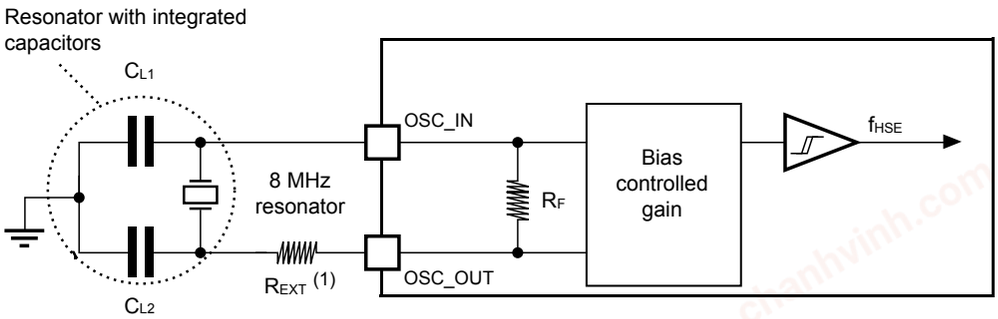
1. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*
2. *This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time*
3. *$t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer*

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For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 18. Typical application with an 8 MHz crystal). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with an 8 MHz crystal



1. *R_{EXT} value depends on the crystal characteristics.*

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in Table 51. LSE oscillator characteristics (f_{LSE} = 32.768 kHz). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 51. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Specified by design, not tested in production.

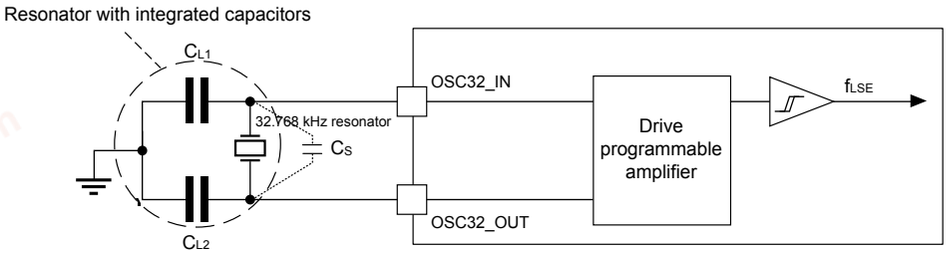
Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00, low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01, medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10, medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11, high drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, high drive capability	-	-	2.7	
$t_{SU(LSE)}$[2]	Startup time	V_{DD} is stabilized	-	2	-	s

1. *Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".*
2. *$t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer*

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Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 19. Typical application with a 32.768 kHz crystal



Note: CL1 and CL2 are external load capacitances. Cs (stray capacitance) is the sum of the device OSC32_IN/OSC32_OUT pins equivalent parasitic capacitance (C_{S_PARA}), and the PCB parasitic capacitance.

Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in Table 52. HSI16 oscillator characteristics are derived from tests performed under ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions. The provided curves are evaluated by characterization, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 52. HSI16 oscillator characteristics

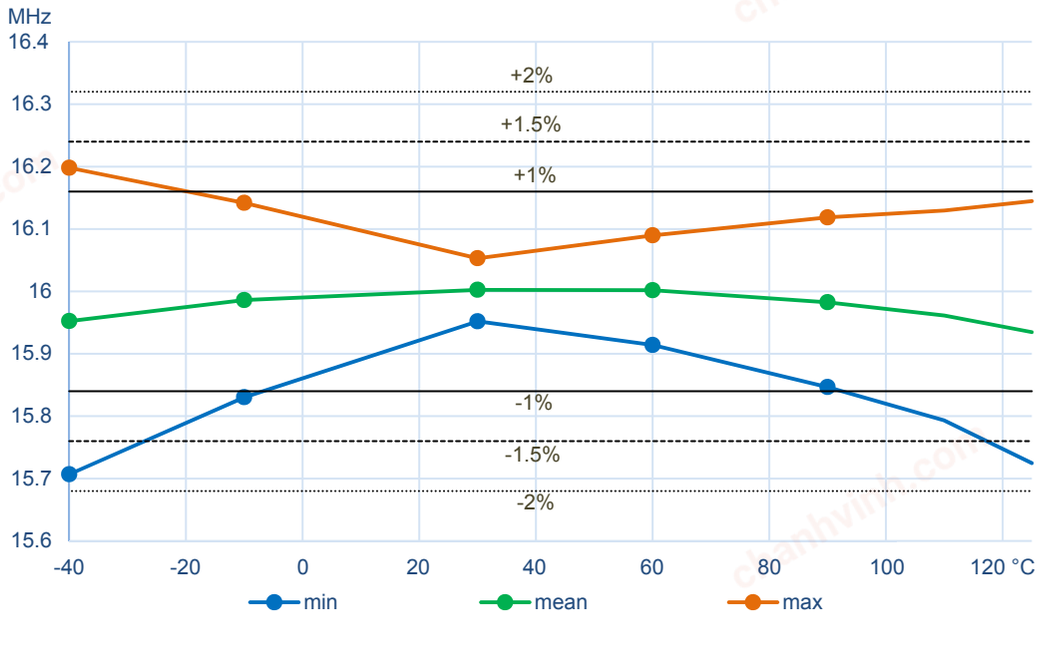
Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	From code 127 to 128	-8	-6	-4	%
		From code 63 to 64 From code 191 to 192	-5.8	-3.8	–1.8	
		For all other code increments	0.2	0.3	0.4	
DuCy(HSI16)(1)	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)(1)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(1)	HSI16 oscillator stabilization time	-	-	3	5	µs
I_{DD}(HSI16)(1)	HSI16 oscillator power consumption	-	-	155	190	µA

1. *Specified by design, not tested in production.*

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Figure 20. **HSI16 frequency versus temperature**



Multi-speed internal (MSI) RC oscillator

Table 53. **MSI oscillator characteristics**

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD} = 3 V and T_A = 30 °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	789.6	800	810.4	
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL = 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD} = 3 V and T_A = 30 °C	PLL mode XTAL = 32.768 kHz	Range 6		-	3.998	-	MHz
			Range 7		-	7.995	-	
			Range 8		-	15.991	-	
			Range 9		-	23.986	-	
			Range 10		-	32.014	-	
			Range 11		-	48.005	-	
$\Delta_{TEMP}(MSI)$[1]	MSI oscillator frequency drift over temperature	MSI mode	T_A = 0 to 85 °C		-3.5	-	3	%
			T_A = -40 to 125 °C		-8	-	6	
$\Delta_{VDD}(MSI)$[1]	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD} = 1.62 V to 3.6 V	-1.2	-	0.5	%
				V_{DD} = 2.4 V to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD} = 1.62 V to 3.6 V	-2.5	-	0.7	
				V_{DD} = 2.4 V to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD} = 1.62 V to 3.6 V	-5	-	1.2	
				V_{DD} = 2.4 V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}$ (MSI)[1][5]	Frequency variation in sampling mode[2]	MSI mode	T_A = -40 to 85 °C		-	1	2	%
			T_A = -40 to 125 °C		-	2	4	
P_USB Jitter(MSI)[5]	Period jitter for USB clock[3]	PLL mode Range 11	for next transition	-	-	-	3.458	ns
			for paired transition	-	-	-	3.916	
MT_USB Jitter(MSI)[5]	Medium term jitter for USB clock[4]	PLL mode Range 11	for next transition	-	-	-	2	ns
			for paired transition	-	-	-	1	
CC jitter(MSI)[5]	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)[5]	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)$[5]	MSI oscillator start-up time	Range 0		-	-	10	20	µs
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)$[5]	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	
$I_{DD}(MSI)$[5]	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA

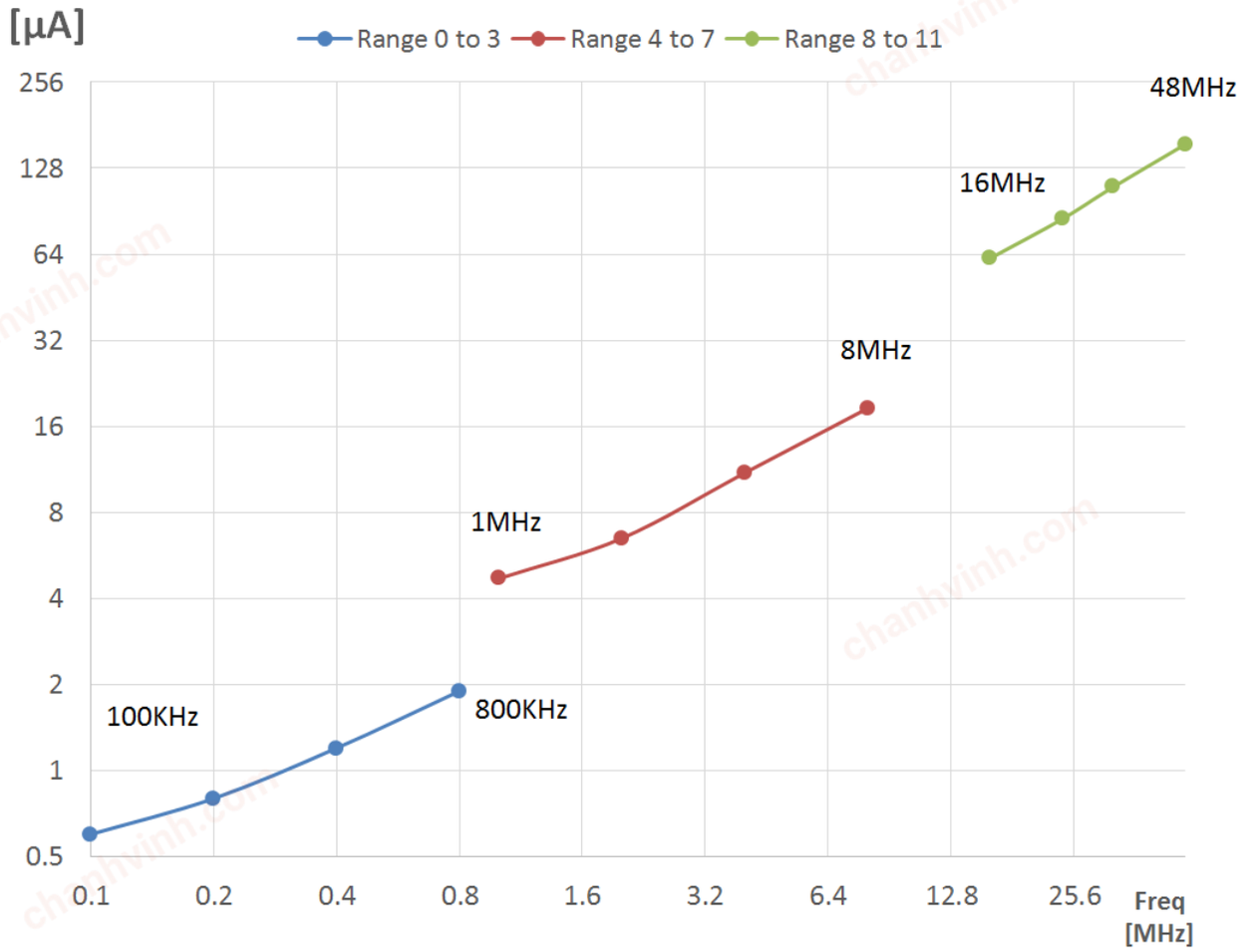
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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{DD}(MSI)(5)	MSI oscillator power consumption	MSI and PLL mode	Range 1	-	-	0.8	1.2	µA
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. *This is a deviation for an individual part once the initial frequency has been measured.*
2. *Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.*
3. *Average period of MSI @48 MHz is compared to a real 48 MHz clock over 28 cycles. It includes frequency tolerance + jitter of MSI @48 MHz clock.*
4. *Only accumulated jitter of MSI @48 MHz is extracted over 28 cycles.*
   For next transition: min. and max. jitter of 2 consecutive frame of 28 cycles of the MSI @48 MHz, for 1000 captures over 28 cycles.
   For paired transitions: min. and max. jitter of 2 consecutive frame of 56 cycles of the MSI @48 MHz, for 1000 captures over 56 cycles.
5. *Specified by design, not tested in production.*

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Figure 21. **Typical current consumption versus MSI frequency**



High-speed internal 48 MHz (HSI48) RC oscillator

Table 54. **HSI48 oscillator characteristics**

V_{DD} = 3 V, T_A = -40 to 125 °C unless otherwise specified.

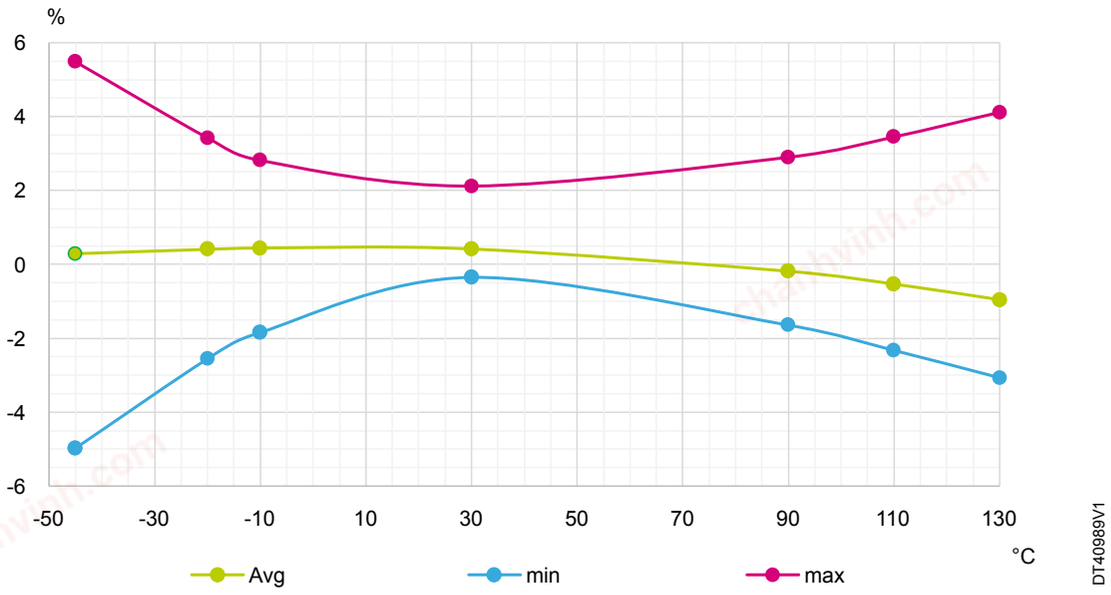
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD} = 3.0 V, T_A = 30 °C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(1)	0.18(1)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±64 steps	±6(2)	±7(2)	-	%
DuCy(HSI48)	Duty Cycle	-	45(1)	-	55(1)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = -15 to 85 °C	-	-	±3(2)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C	-	-	±4.5(2)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(2)	0.05(2)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(2)	0.1(2)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(1)	6(1)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(1)	380(1)	µA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(3)	-	-	+/-0.15(1)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(3)	-	-	+/-0.25(1)	-	ns

1. *Specified by design, not tested in production.*
2. *Evaluated by characterization, not tested in production.*
3. *Jitter measurement are performed without clock source activated in parallel.*

Figure 22. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 55. LSI oscillator characteristics

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)$(1)	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI)$(1)	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD}(LSI)$(1)	LSI oscillator power consumption	-	-	110	180	nA

1. *Specified by design, not tested in production.*

6.3.9 PLL characteristics

The parameters given in Table 56. PLL characteristics are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Table 56. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock frequency(1)	-	2.66	-	16	MHz

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
D_{PLL_IN}	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	3.09	-	122	MHz
		Voltage scaling Range 2	3.09	-	40	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	12	-	128	MHz
		Voltage scaling Range 2	12	-	33	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	12	-	64	MHz
		Voltage scaling Range 2	12	-	16	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	MHz
		Voltage scaling Range 2	96	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 56 MHz	-	50	-	±ps
	RMS period jitter		-	40	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}not found	VCO freq = 96 MHz	-	200	260	µA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. *Make sure to use the appropriate division factor M to obtain the specified PLL input clock values.*

6.3.10 Flash memory characteristics

Table 57. Flash memory characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	85	125	µs
		Burst mode	48	48	
t_{prog_row}	Row (32 double word) programming time	Normal programming	2.7	4.6	ms
		Fast programming	1.7	2.8	
t_{prog_page}	Page (2 Kbytes) programming time	Normal programming	21.8	36.6	
		Fast programming	13.7	22.4	
t_{ERASE}	Page (2 Kbytes) erase time	-	22.0	40.0	
t_{prog_bank}	One 256-Kbyte bank programming time(1)	Normal programming	1.4	2.4	s
		Fast programming	0.9	1.5	
t_{ME}	Mass erase time	-	22.1	40.1	ms
$I_{DD(Flash\ A)}$	Average consumption from V_{DD}	Programming	3	-	mA
		Page erase	3	-	
		Mass erase	5		
$I_{DD(Flash\ P)}$	Maximum current (peak)	Programming, 2 µs peak duration	7	-	
		Erase, 41 µs peak duration	7	-	

1. *The values provided also apply to devices with less flash memory than one 256-Kbyte bank.*

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Table 58. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. *Evaluated by characterization, not tested in production.*
2. *Cycling performed over the whole temperature range.*

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 59. EMS characteristics. They are based on the EMS levels and classes defined in application note AN1709.

Table 59. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 54 MHz, LPQF80 conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, TA = +25 °C, f_{HCLK} = 54 MHz, LPQF80 conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

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Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 60. EMI characteristics for f_{HSE} = 8 MHz and f_{HCLK} = 54 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak	V_{DD} = 3.6 V, T_A = 25 °C, LQFP80 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	5	dBµV
			30 MHz to 130 MHz	2	
			130 MHz to 1 GHz	1	
			1 GHz to 2 GHz	8	
	Level		0.1 MHz to 2 GHz	2	-

1. *Refer to AN1709 “EMI radiated test” section.*
2. *Refer to AN1709 “EMI level classification” section.*

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 61. ESD absolute maximum ratings

TBD stands for "to be defined".

Symbol	Ratings	Conditions	Package	Class	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	All	2D	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESDA/ JEDEC-002	WLCSP42	TBD	TBD	
			All others	C2a	500	

1. *Evaluated by characterization, not tested in production.*

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

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Table 62. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +130 °C conforming to JESD78A	II

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the 5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in Table 63. I/O current injection susceptibility.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 63. I/O current injection susceptibility

Evaluated by characterization, not tested in production.

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PA4, PA5	-5	N/A(1)	mA
	Injected current on PA4, PA5 pins	-5	0	

1. *Injection is not possible.*

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 64. I/O static characteristics are derived from tests performed under the conditions summarized in Section 6.3.1: General operating conditions. All I/Os are designed as CMOS- and TTL-compliant.

Note: For information on GPIO configuration, refer to the application note AN4899 "STM32 GPIO configuration for hardware settings and low-pow er consumption" available from the ST website www.st.com.

Table 64. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	1.62 V < V_{DDIOx} < 3.6 V	-	-	0.3 x V_{DDIOx} (2)	V
	I/O input low level voltage	1.62 V < V_{DDIOx} < 3.6 V	-	-	0.39 x V_{DDIOx} - 0.06(3)	
V_{IH}(1)	I/O input high level voltage	1.62 V < V_{DDIOx} < 3.6 V	0.7 x V_{DDIOx} (2)	-	-	V
	I/O input high level voltage	1.62 V < V_{DDIOx} < 3.6 V	0.49 x V_{DDIOX} + 0.26 (3)	-	-	
V_{hys}(3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V < V_{DDIOx} < 3.6 V	-	200	-	mV
I_{lkg}(4)	FT_xx input leakage current(3)(5)	V_{IN} ≤ Max(V_{DDXXX})(6)(7)	-	-	±100	nA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}[4]	FT_xx input leakage current[3][5]	$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX}) + 1\ V$[6][7]	-	-	650	nA
		$Max(V_{DDXXX}) + 1\ V < V_{IN} \le 5.5\ V$[6][7]	-	-	200	
	PC3 I/O	$V_{IN} \le Max(V_{DDXXX})$[6][7]	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX}) + 1\ V$[6][7]	-	-	2500[3]	
		$Max(V_{DDXXX}) + 1\ V < V_{IN} \le 5.5\ V$[6][7]	-	-	250	
	TT_xx input leakage current	$V_{IN} \le Max(V_{DDXXX})$[6]	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN} < 3.6V$[6]	-	-	2000[3]	
R_{PU}	Weak pull-up equivalent resistor[8]	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor[8]	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

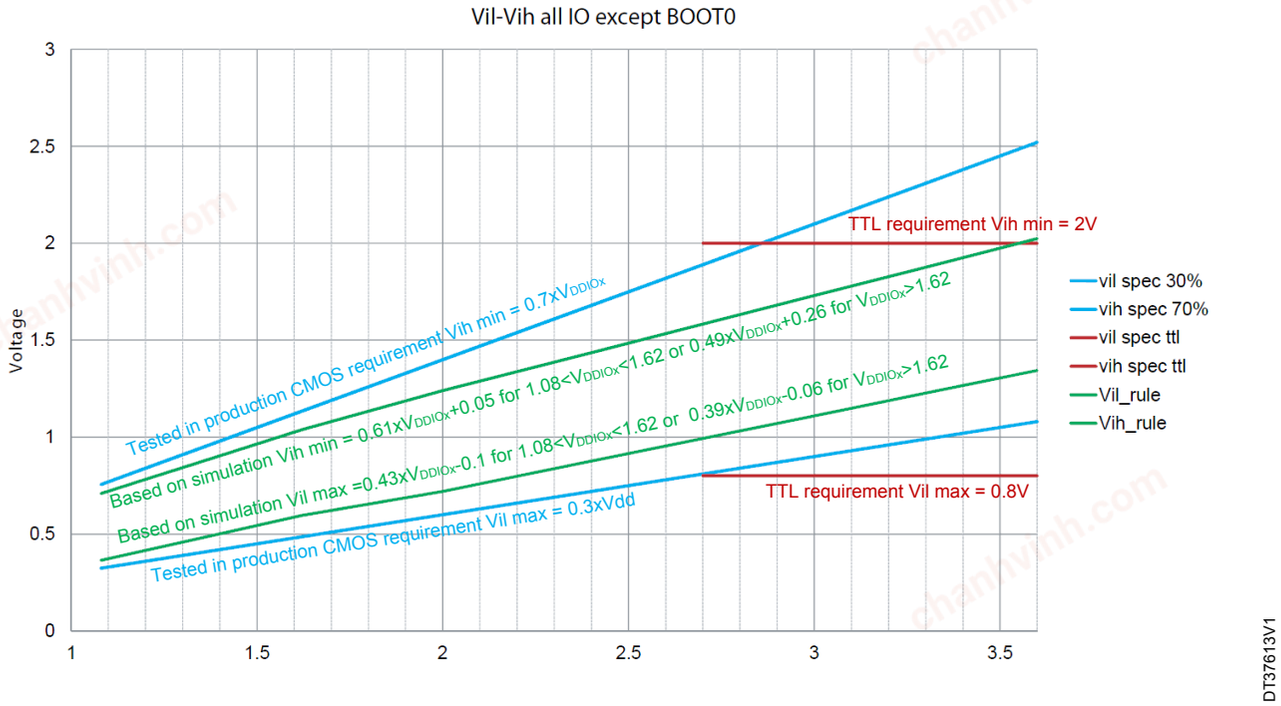
1. *Refer to Figure 23. I/O input characteristics.*
2. *Tested in production.*
3. *Specified by design, not tested in production.*
4. *This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula:*

   $I_{Total_Ileak_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] × $I_{lkg}(Max)$.
5. *All FT_xx GPIOs except FT_u and PC3 I/O.*
6. *$Max(V_{DDXXX})$ is the maximum value of all the I/O supplies. Refer to Table: Legend/Abbreviations used in the pinout table.*
7. *To sustain a voltage higher than $Min(V_{DD}, V_{DDA}, V_{DDUSB})$ + 0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.*
8. *Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).*

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in Figure 23. I/O input characteristics.

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Figure 23. **I/O input characteristics**



Current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

GPIOs PC13, PC14 and PC15 are supplied through the power switch, limiting source capability up to 3 mA only.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section 6.2: Absolute maximum ratings:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see Table 19. Voltage characteristics).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 19. Voltage characteristics).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions. All I/Os are CMOS- and TTL-compliant (FT or TT unless otherwise specified).

Table 65. **Output voltage characteristics**

The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 19. Voltage characteristics, , and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port (1) $\|I_{IO}\|$ = 8 mA(2) V_{DDIOx} ≥ 2.7 V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx} - 0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(1) $\|I_{IO}\|$ = 8 mA(4) V_{DDIOx} ≥ 2.7 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	

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Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (3)	Output low level voltage for an I/O pin	PC13, PC14 and PC15 $\|I_{IO}\|$ = 3 mA $V_{DDIOx} \geq 2.7$ V	-	0.07	V
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DDIOx} - 0.35	-	
V_{OL} (3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA (4) $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DDIOx} - 1.3	-	
V_{OL} (3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA (2) $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DDIOx} - 0.45	-	
V_{OLFM+} (3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	0.4	

1. *TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*
2. *PC13, PC14 and PC15 are tested/characterized at their maximum current of 3 mA.*
3. *Specified by design, not tested in production.*
4. *Not applicable to PC13, PC14 and PC15.*

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in Figure 24. I/O AC characteristics definition and Table 66. I/O AC characteristics, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Table 66. I/O AC characteristics

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0503 reference manual for a description of GPIO Port configuration register.
2. Specified by design, not tested in production.

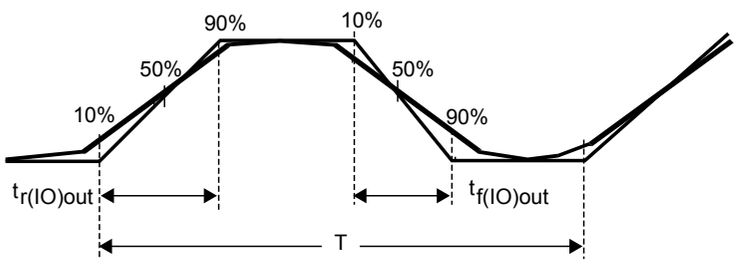
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	

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Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(1)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(1)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(1)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.62 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(2)		-	5	ns

1. *This value represents the I/O capability but the maximum system frequency is limited to 56 MHz.*
2. *The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.*

Figure 24. I/O AC characteristics definition



Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

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1. *Refer to Table 66. I/O AC characteristics.*

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Table 67. NRST pin characteristics

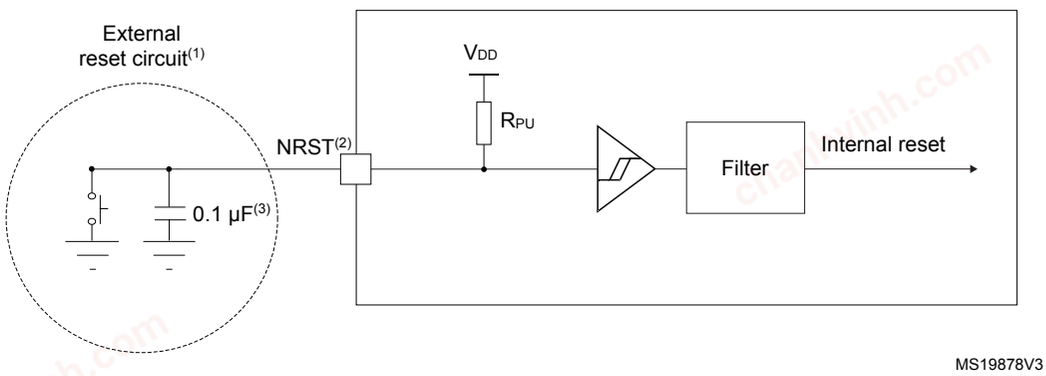
Specified by design, not tested in production.

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 × V_{DDIOx}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7 × V_{DDIOx}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(1)	V_{IN} = V_{SS}	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. *The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).*

Figure 25. Recommended NRST pin protection



1. *The reset network protects the device against parasitic resets.*
2. *The user must ensure that the voltage level on the NRST pin can go above the $V_{IH(NRST)}$ minimum level specified in Table 67. NRST pin characteristics during each power on, otherwise the device does not exit from reset. This is applicable to all NRST configurations selected through the NRST_MODE[1:0] bitfield of the FLASH_OPTR register, including GPIO mode.*
3. *The external capacitor on NRST must be placed as close as possible to the device.*

6.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 68. EXTI Input Characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

6.3.17 Analog switches booster

Table 69. Analog switches booster characteristics

Specified by design, not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs

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Symbol	Parameter	Min	Typ	Max	Unit
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

6.3.18 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in Table 70. ADC characteristics are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in Section 6.3.1: General operating conditions.

Note: It is recommended to perform a calibration after each power-up.

Table 70. ADC characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	V_{DDA} ≥ 2 V	2	-	V_{DDA}	
		V_{DDA} < 2 V	V_{DDA}			
f_{ADC}	ADC clock frequency	Range 1	0.14	-	35	MHz
		Range 2	0.14	-	16	
f_s	Sampling rate	12 bits	-	-	2.50	MSps
		10 bits	-	-	2.92	
		8 bits	-	-	3.50	
		6 bits	-	-	4.38	
f_{TRIG}	External trigger frequency	f_{ADC} = 35 MHz; 12 bits	-	-	2.33	MHz
		12 bits	-	-	f_{ADC}/15	
V_{AIN}(2)	Conversion voltage range	-	V_{SSA}	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	ADC power-up time	-	2			Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 35 MHz	2.35			µs
		-	82			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency	CKMODE = 00	2	-	3	$1/f_{ADC}$
		CKMODE = 01	6.5			$1/f_{PCLK}$
		CKMODE = 10	12.5			
		CKMODE = 11	3.5			
ts	Sampling time	f_{ADC} = 35 MHz; V_{DDA} > 2V	0.043	-	4.59	µs
			1.5	-	160.5	$1/f_{ADC}$
		f_{ADC} = 35 MHz; V_{DDA} < 2V	0.1	-	4.59	µs
			3.5	-	160.5	$1/f_{ADC}$

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Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 35 MHz Resolution = 12 bits	0.40	-	4.95	µs
		Resolution = 12 bits	t_s + 12.5 cycles for successive approximation = 14 to 173			$1/f_{ADC}$
t_{IDLE}	Laps of time allowed between two conversions without rearm	-	-	-	100	µs
$I_{DDA(ADC)}$	ADC consumption from V_{DDA}	f_s = 2.5 MSps	-	410	-	µA
		f_s = 1 MSps	-	164	-	
		f_s = 10 kSps	-	17	-	
$I_{DDV(ADC)}$	ADC consumption from V_{REF+}	f_s = 2.5 MSps	-	65	-	µA
		f_s = 1 MSps	-	26	-	
		f_s = 10 kSps	-	0.26	-	

1. *I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when V_{DDA} ≥ 2.4 V.*
2. *V_{REF+} is internally connected to V_{DDA} on some packages. Refer to Section 4: Pinouts/ballouts, pin description, and alternate functions for further details.*

Table 71. Maximum ADC R_{AIN}

Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN} [1][2] (Ω)
12 bits	1.5[3]	43	50
	3.5	100	680
	7.5	214	2200
	12.5	357	4700
	19.5	557	8200
	39.5	1129	15000
	79.5	2271	33000
	160.5	4586	50000
10 bits	1.5[3]	43	68
	3.5	100	820
	7.5	214	3300
	12.5	357	5600
	19.5	557	10000
	39.5	1129	22000
	79.5	2271	39000
	160.5	4586	50000
8 bits	1.5[3]	43	82
	3.5	100	1500
	7.5	214	3900
	12.5	357	6800

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Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN} (1)(2) (Ω)
8 bits	19.5	557	12000
	39.5	1129	27000
	79.5	2271	50000
	160.5	4586	50000
6 bits	1.5(3)	43	390
	3.5	100	2200
	7.5	214	5600
	12.5	357	10000
	19.5	557	15000
	39.5	1129	33000
	79.5	2271	50000
	160.5	4586	50000

1. *I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when V_{DDA} ≥ 2.4 V.*
2. *Specified by design, not tested in production.*
3. *Only allowed with V_{DDA} > 2 V*

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Table 72. ADC accuracy

1. Evaluated by characterization, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. Injecting negative current on any analog input pin significantly reduces the accuracy of A-to-D conversion of signal on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins susceptible to receive negative current.

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
ET	Total unadjusted error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	3	6	LSB
		$2\ V < V_{DDA}=V_{REF+} < 3.6$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; T_A = entire range	-	3	6.5	
		$1.65\ V < V_{DDA}=V_{REF+} < 3.6$ V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \le 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \le 1.1$ MSps;	-	3	7.5	
EO	Offset error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	1.5	5	LSB
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; T_A = entire range	-	1.5	5.5	
		$1.65\ V < V_{DDA}=V_{REF+} < 3.6$ V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \le 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \le 1.1$ MSps;	-	1.5	6	
EG	Gain error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	3	3.5	LSB
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; T_A = entire range	-	3	5	
		$1.65\ V < V_{DDA} = V_{REF+} < 3.6$ V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \le 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \le 1.1$ MSps;	-	3	6.5	
ED	Differential linearity error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	1.2	2.5	LSB
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; T_A = entire range	-	1.2	2.5	
		$1.65\ V < V_{DDA} = V_{REF+} < 3.6$ V; T_A = entire range Range 1: $f_{ADC} = 35$ MHz; $f_s \le 2.2$ MSps; Range 2: $f_{ADC} = 16$ MHz; $f_s \le 1.1$ MSps;	-	1.2	2.5	
EL	Integral linearity error	$V_{DDA} = V_{REF+} = 3$ V; $f_{ADC} = 35$ MHz; $f_s \le 2.5$ MSps; $T_A = 25$ °C	-	2.5	3	LSB

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Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
EL	Integral linearity error	2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	2.5	3.5	LSB
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	-	2.5	3.5	
ENOB	Effective number of bits	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	10.1	10.2	-	bit
		2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	9.6	10.2	-	
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	9.5	10.2	-	
SINAD	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	62.5	63	-	dB
		2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	59.5	63	-	
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	59	63	-	
SNR	Signal-to-noise ratio	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	63	64	-	dB
		2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	60	64	-	
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	60	64	-	
THD	Total harmonic distortion	V_{DDA} = V_{REF+} = 3 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = 25 °C	-	-74	-73	dB
		2 V < V_{DDA} = V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	-74	-70	
		1.65 V < V_{DDA} = V_{REF+} < 3.6 V; T_A = entire range Range 1: f_{ADC} = 35 MHz; f_s ≤ 2.2 MSps; Range 2: f_{ADC} = 16 MHz; f_s ≤ 1.1 MSps;	-	-74	-70	

1. *I/O analog switch voltage booster enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when V_{DDA} ≥ 2.4 V.*

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Figure 26. ADC accuracy characteristics

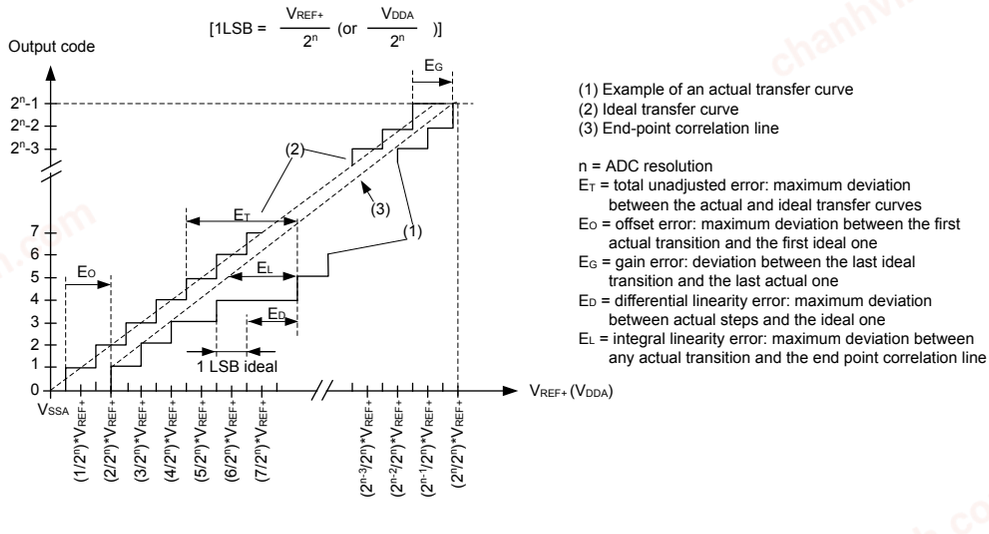
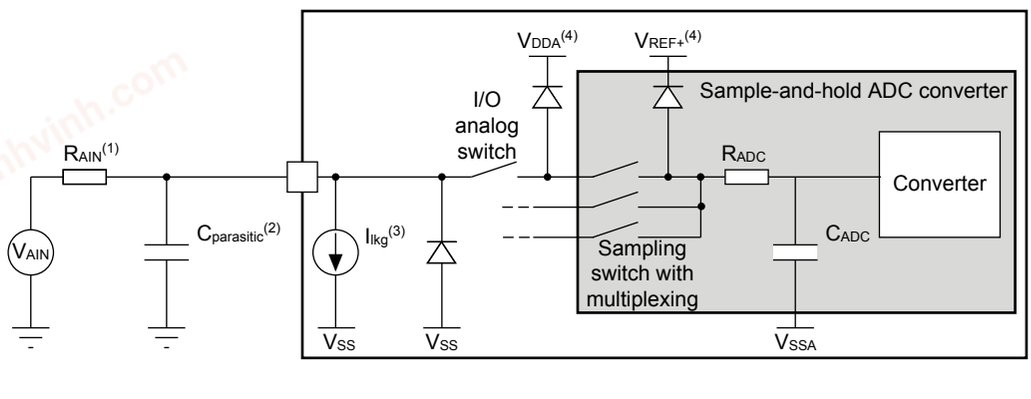


Figure 27. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



1. *Refer to Table 70. ADC characteristics for the values of R_{AIN} and C_{ADC}.*
2. *$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Table 64. I/O static characteristics for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.*
3. *Refer to Table 64. I/O static characteristics for the values of I_{lkg}.*
4. *Refer to Section 3.6.1: Power supply schemes.*

6.3.18.1 General PCB design guidelines

Power supply decoupling should be performed as shown in Figure 13. Power supply scheme. The 100 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

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6.3.19 Temperature sensor characteristics

Table 73. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope (2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C) (3)	0.742	0.76	0.785	V
$t_{START(TS_BUF)}$ (1)	Sensor Buffer Start-up time in continuous mode (4)	-	8	15	µs
t_{START} (1)	Start-up time when entering in continuous mode (4)	-	70	120	µs
t_{S_temp} (1)	ADC sampling time when reading the temperature	5	-	-	µs
$I_{DD(TS)}$ (1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. *Specified by design, not tested in production.*
2. *Evaluated by characterization, not tested in production.*
3. *Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.*
4. *Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.*

6.3.20 V_{BAT} monitoring characteristics

Table 74. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	3×39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er (1)	Error on Q	-10	-	10	%
t_{S_vbat} (1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. *Specified by design, not tested in production.*

Table 75. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.21 Digital-to-analog converter characteristics

Table 76. DAC characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	V_{DDA}	
		Other modes		1.80	-		
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ

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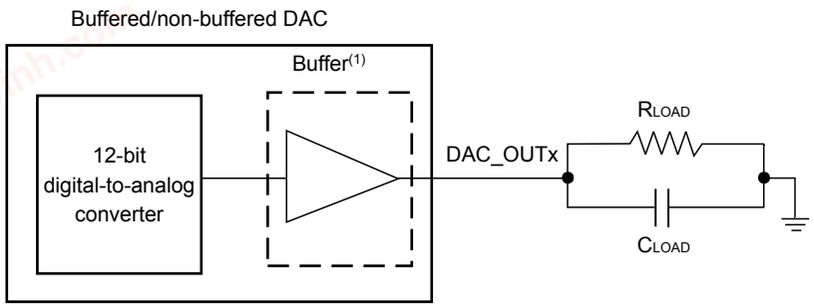
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_L	Resistive load	DAC output buffer ON	connected to V_{DDA}	25	-	-	kΩ
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} - 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(1)	Wake-up time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB
$T_{W_to_W}$	Minimum time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB)	DAC_MCR:MODEx[2:0] = 000 or 001 CL ≤ 50 pF; RL ≥ 5 kΩ		1	-	-	µs
		DAC_MCR:MODEx[2:0] = 010 or 011 CL ≤ 10 pF		1.4	-	-	
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(2)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
$I_{DDA(DAC)}$	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDA(DAC)}$	DAC consumption from V_{DDA}	DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	µA
		Sample and hold mode, C_{SH} = 100 nF		-	315 x T_{on}/ (T_{on}+T_{off})(3)	670 x T_{on}/ (T_{on}+T_{off})(3)	
$I_{DDV(DAC)}$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x T_{on}/ (T_{on}+T_{off})(3)	400 x T_{on}/ (T_{on}+T_{off})(3)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x T_{on}/ (T_{on}+T_{off})(3)	205 x T_{on}/ (T_{on}+T_{off})(3)	

1. *In buffered mode, the output can overshoot above the final value for low input code (starting from min value).*
2. *Refer to Table 64. I/O static characteristics.*
3. *T_{on} is the Refresh phase duration. T_{off} is the Hold phase duration. Refer to RM0503 reference manual for more details.*

Figure 28. 12-bit buffered / non-buffered DAC



(1) The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

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1. *The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.*

.

Table 77. DAC accuracy

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non linearity(1)	DAC output buffer ON	-	-	±2	LSB
		DAC output buffer OFF	-	-	±2	
-	monotonicity	10 bits	guaranteed			
INL	Integral non linearity(2)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL	-	-	±4	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Offset	Offset error at code 0x800(2)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	LSB
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(3)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(4)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	11.5	-	

1. *Difference between two consecutive codes - 1 LSB.*
2. *Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.*
3. *Difference between the value measured at Code (0x001) and the ideal value.*
4. *Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2) V when buffer is ON.*

6.3.22 Voltage reference buffer characteristics

Table 78. VREFBUF characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 1	2.8	-	3.6	V
		Degraded mode(1)	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	I_{load} = 100 µA T = 30 °C	V_{RS} = 0	2.038	2.042	2.046	
			V_{RS} = 1	2.497	2.5	2.503	
			V_{RS} = 0	V_{DDA}-150 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of C_{load}	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
$T_{Coeff_vrefbuf}$	Temperature coefficient of VREFBUF(2)	-40 °C < T_J < +125 °C		-	-	50	ppm/ °C
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(3)		-	300	350	µs
		CL = 1.1 µF(3)		-	500	650	
		CL = 1.5 µF(3)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase(4)	-		-	8	-	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA		-	16	25	µA
		I_{load} = 500 µA		-	18	30	
		I_{load} = 4 mA		-	35	50	

1. *In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).*
2. *The temperature coefficient at VREF+ output is the sum of $T_{Coeff_vrefint}$ and $T_{Coeff_vrefbuf}$.*
3. *The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.*
4. *To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.*

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6.3.23 Comparator characteristics

Table 79. COMP characteristics

Specified by design, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG} (1)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D (2)	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		4	8	16	
		Medium hysteresis		8	15	30	
		High hysteresis		15	27	52	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	
I_{bias}	Comparator input bias current	-		-	-	-(3)	nA

1. *Refer to Table 25. Embedded internal voltage reference.*
2. *Evaluated by characterization, not tested in production.*
3. *Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in Table 64. I/O static characteristics.*

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6.3.24 Operational amplifiers characteristics

Table 80. OPAMP characteristics

Evaluated by characterization, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage(1)	-		1.8	-	3.6	V
CMIR	Common mode input range	-		0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	25 °C, No Load on output.		-	-	±1.5	mV
		All voltage/temperature		-	-	±3	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode		-	±5	-	µV/°C
		Low-power mode		-	±10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-		-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-		-	1	1.35	
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(2)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AO	Open loop gain	Low-power mode		45	110	-	dB
V_{OHSAT}[2]	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} -100	-	-	mV
		Low-power mode		V_{DDA} -50	-	-	
V_{OLSAT}[2]	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	-	5	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input		-	-	-[3]	nA
PGA gain[2]	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	
$R_{network}$	R2/R1 internal resistance values in PGA mode[4]	PGA Gain = 2		-	80/80	-	kΩ/kΩ
		PGA Gain = 4		-	120/ 40	-	
		PGA Gain = 8		-	140/ 20	-	
		PGA Gain = 16		-	150/ 10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/2	-	MHz
		Gain = 4	-	-	GBW/4	-	
		Gain = 8	-	-	GBW/8	-	
		Gain = 16	-	-	GBW/16	-	
en	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	-	500	-	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	-	600	-	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	-	180	-	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	-	290	-	
I_{DDA}(OPAMP)[2]	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode	-	120	260	µA

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}(OPAMP)(2)	OPAMP consumption from V_{DDA}	Low-power mode	no Load, quiescent mode	-	45	100	µA

1. *The temperature range is limited to 0 °C-125 °C when V_{DDA} is below 2 V*
2. *Evaluated by characterization, not tested in production.*
3. *Mostly I/O leakage, when used in analog mode. Refer to I_{lkg} parameter in Table 64. I/O static characteristics.*
4. *R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1*

6.3.25 LCD controller characteristics

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the VLCD pin to decouple this converter.

Table 81. LCD controller characteristics

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage		-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0		-	2.62	-	
V_{LCD1}	LCD internal reference voltage 1		-	2.76	-	
V_{LCD2}	LCD internal reference voltage 2		-	2.89	-	
V_{LCD3}	LCD internal reference voltage 3		-	3.04	-	
V_{LCD4}	LCD internal reference voltage 4		-	3.19	-	
V_{LCD5}	LCD internal reference voltage 5		-	3.32	-	
V_{LCD6}	LCD internal reference voltage 6		-	3.46	-	
V_{LCD7}	LCD internal reference voltage 7		-	3.62	-	
C_{ext}	V_{LCD} external capacitance	Buffer OFF (BUFEN=0 is LCD_CR register)	0.2	-	2	µF
		Buffer ON (BUFEN=1 is LCD_CR register)	1	-	2	
I_{LCD}(1)	Supply current from V_{DD} at V_{DD} = 2.2 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	3	-	µA
	Supply current from V_{DD} at V_{DD} = 3.0 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	1.5	-	
I_{VLCD}	Supply current from V_{LCD} (V_{LCD} = 3 V)	Buffer OFF (BUFFEN = 0, PON = 0)	-	0.5	-	µA
		Buffer ON (BUFFEN = 1, 1/2 Bias)	-	0.6	-	
		Buffer ON (BUFFEN = 1, 1/3 Bias)	-	0.8	-	
		Buffer ON (BUFFEN = 1, 1/4 Bias)	-	1	-	
R_{HN}	Total High Resistor value for Low drive resistive network		-	5.5	-	MΩ
R_{LN}	Total Low Resistor value for High drive resistive network		-	240	-	kΩ
V_{44}	Segment/Common highest level voltage		-	V_{LCD}	-	V
V_{34}	Segment/Common 3/4 level voltage		-	3/4 V_{LCD}	-	
V_{23}	Segment/Common 2/3 level voltage		-	2/3 V_{LCD}	-	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{12}	Segment/Common 1/2 level voltage		-	1/2 V_{LCD}	-	V
V_{13}	Segment/Common 1/3 level voltage		-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage		-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage		-	0	-	

1. *LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.*

6.3.26 Timer characteristics

The parameters given in the following tables are specified by design, and not tested in production.

Refer to Section 6.3.14: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 82. TIMx characteristics

TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.8	-	ns
fEXT	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
ResTIM	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1363.1	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.34	s

Table 83. IWDG min/max timeout period at 32 kHz (LSI)

The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

Table 84. WWDG min/max timeout at 56 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0358	2.2938	ms
2	1	0.0717	4.5875	
4	2	0.1434	9.1750	

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Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
8	3	0.2867	18.3501	ms

6.3.27 I²C-bus interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

When the I2C peripheral is properly configured, the I2C timings requirements are specified by design, and not tested in production (refer to RM0503 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to Section 6.3.14: I/O port characteristics for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 85. I2C analog filter characteristics

Specified by design, not tested in production.

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(1)	205(2)	ns

1. *Spikes with widths below $t_{AF(min)}$ are filtered.*
2. *Spikes with widths above $t_{AF(max)}$ are not filtered*

6.3.28 USART characteristics

Unless otherwise specified, the parameters given in Table 86 are derived from tests performed under the ambient temperature, f_{PCLK} frequency and supply voltage conditions summarized in Section 6.3.1: General operating conditions. The additional general conditions are:

- Output speed is set to OSPEEDRy[1:0] = 11 (output speed)
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- Voltage scale is set to VOS[1:0] = 01

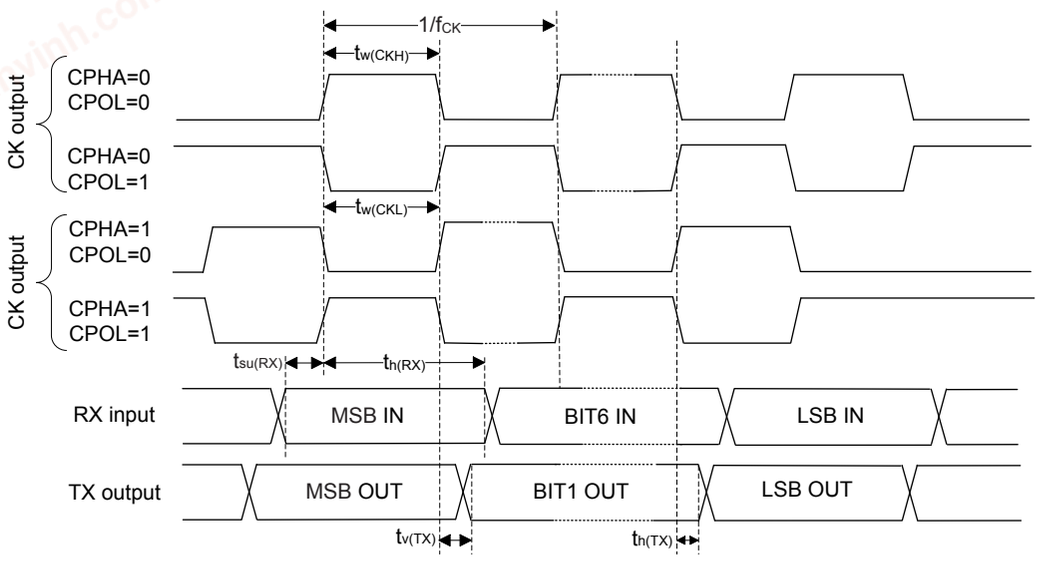
Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternatefunction characteristics (NSS, CK, TX, and RX for USART).

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Table 86. USART characteristics

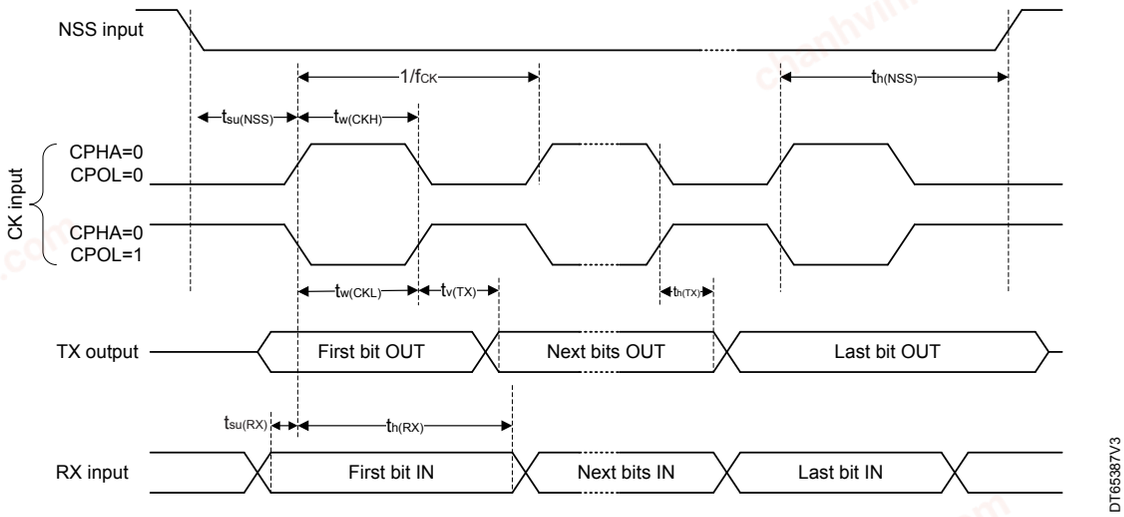
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	6.75	MHz
		Slave mode	-	-	18	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker} + 2	-	-	nsnsns
$t_{h(NSS)}$	NSS hold time		0.5	-	-	
$t_{w(CKH)}$	SCK high time	Master mode	1 / f_{CK} / 2 - 1	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1	
$t_{w(CKL)}$	SCK low time					
$t_{su(RX)}$	Data input setup time	Master mode	22	-	-	
		Slave mode	5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	
		Slave mode	0.5	-	-	
$t_{v(TX)}$	Data output valid time,	Master mode	0	0.5	1	
		Slave mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	16	-	19.5	
		Slave mode, 1.71 V ≤ V_{DD} ≤ 3.6 V	16	-	27.5	
$t_{h(TX)}$	Data output hold time	Master mode	0	-	-	
		Master mode	10	-	-	

Figure 29. USART timing diagram in SPI master mode



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Figure 30. **USART timing diagram in SPI slave mode**



6.3.29 SPI characteristics

Unless otherwise specified, the parameters given in Table 87 for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in Section 6.3.1: General operating conditions.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

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Table 87. SPI characteristics

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode receiver/full duplex 1.71 < V_{DD} < 3.6 V Voltage Range 1	-	-	27	MHz
		Master mode transmitter 1.71 < V_{DD} < 3.6 V Voltage Range 1			27	
		Slave mode receiver 1.71 < V_{DD} < 3.6 V Voltage Range 1			27	
		Slave mode transmitter/full duplex 2.7 < V_{DD} < 3.6 V Voltage Range 1			27(1)	
		Slave mode transmitter/full duplex 1.71 < V_{DD} < 3.6 V Voltage Range 1			21.5(1)	
		Voltage Range 2			9.5	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	4	-	-	T_{PCLK}
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	2	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{SCK2} - 1.5(2)	T_{SCK2}(2)	T_{SCK2} + 1.5(2)	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	ns
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2.5	-	-	ns
$t_{h(SI)}$		Slave mode	2.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	12.5	20	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	6	7.5	18	ns
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 < V_{DD} < 3.6 V Voltage Range 1	-	15	18	ns
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 1	-	15	23	
		Slave mode 1.71 < V_{DD} < 3.6 V Voltage Range 2	-	22	30	
$t_{v(MO)}$		Master mode	-	3	5.5	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	ns
$t_{h(MO)}$		Master mode	1	-	-	

1. *Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.*
2. *$T_{SCK2} = T_{PCLK} \times$ prescaler / 2*

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Figure 31. **SPI timing diagram - slave mode and CPHA = 0**

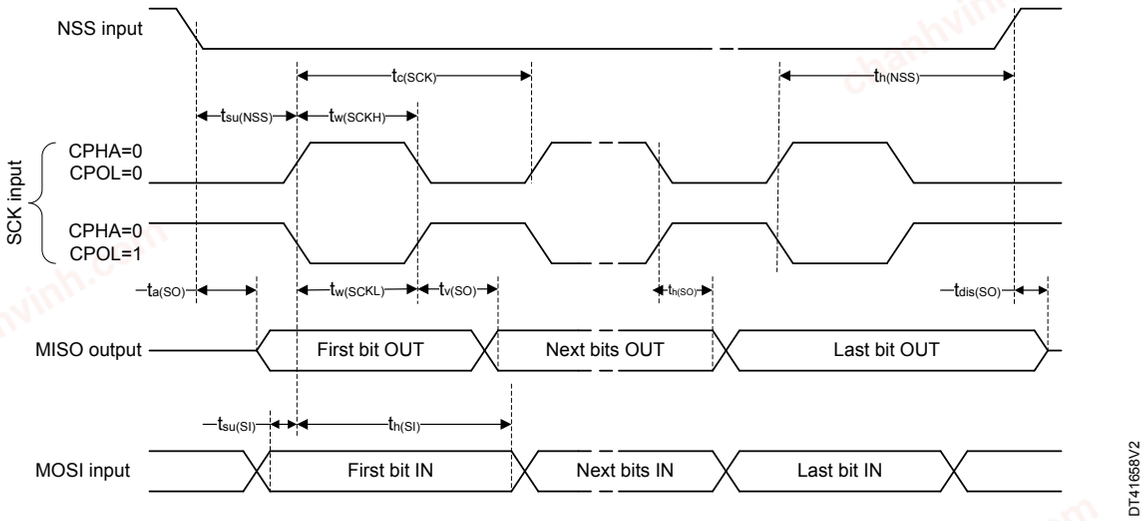
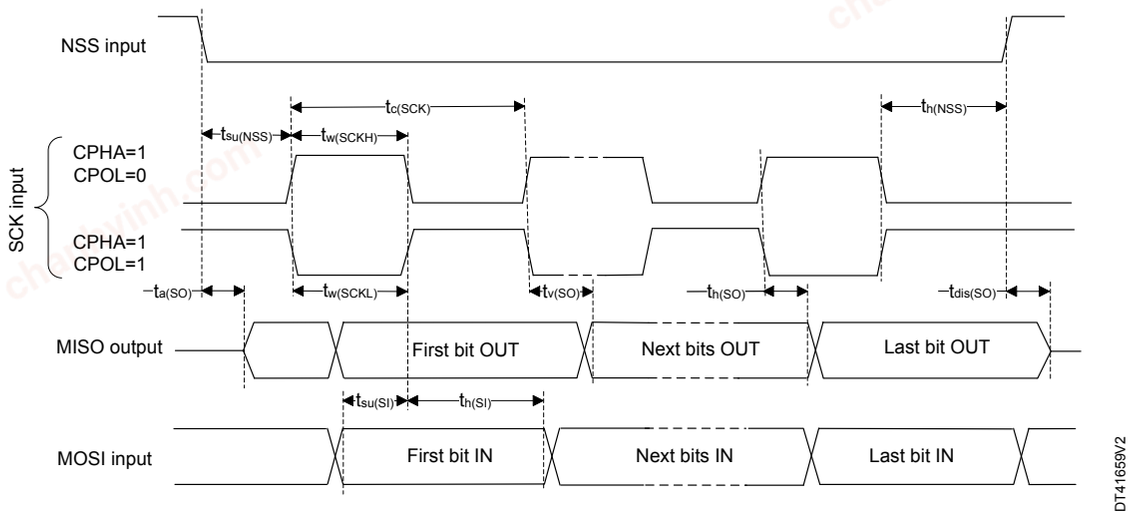


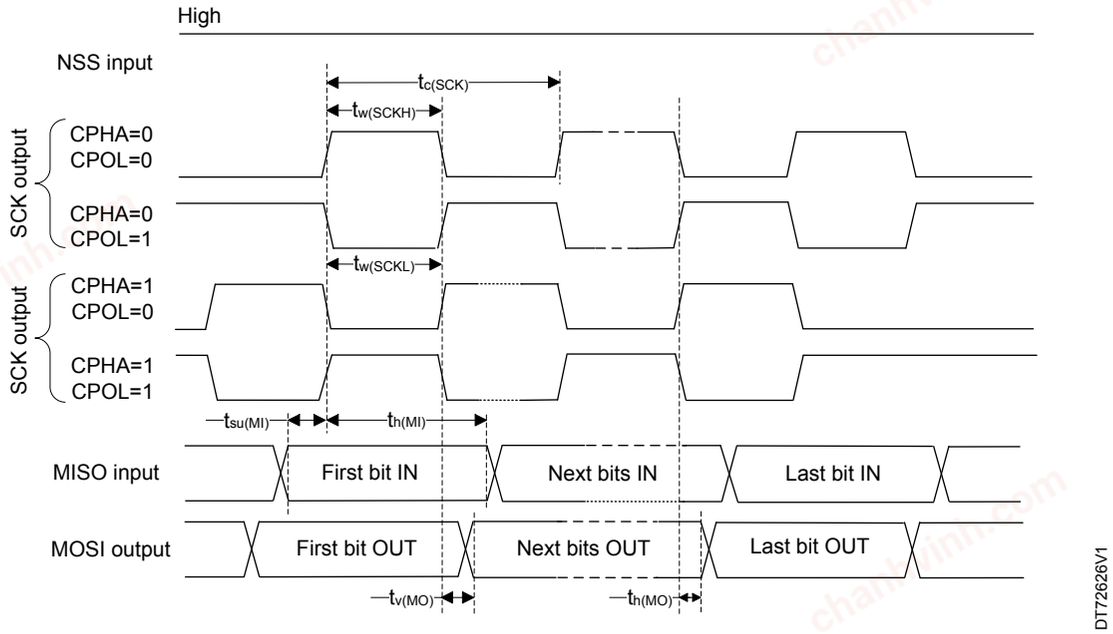
Figure 32. **SPI timing diagram - slave mode and CPHA = 1**



1. *Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.*

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Figure 33. **SPI timing diagram - master mode**



1. *Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.*

6.3.30 USB characteristics

The USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 88. **USB electrical characteristics**

T_A = -40 to 125 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage	-	3.0(1)	-	3.6	V
$T_{crystall_less}$	USB crystal-less operation temperature	-	-15	-	85	°C
$t_{STARTUP}$(2)	USB transceiver startup time	-	-	-	1.0	µs
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}(2)	Output driver impedance(3)	High and low driver	28	36	44	

1. *USB functionality is ensured down to 2.7 V, but some USB electrical characteristics are degraded in 2.7 to 3.0 V range.*
2. *Specified by design, not tested in production.*
3. *No external termination series resistors are required on USB_DP (D+) and USB_DM (D-). The matching impedance is already included in the embedded driver.*

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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

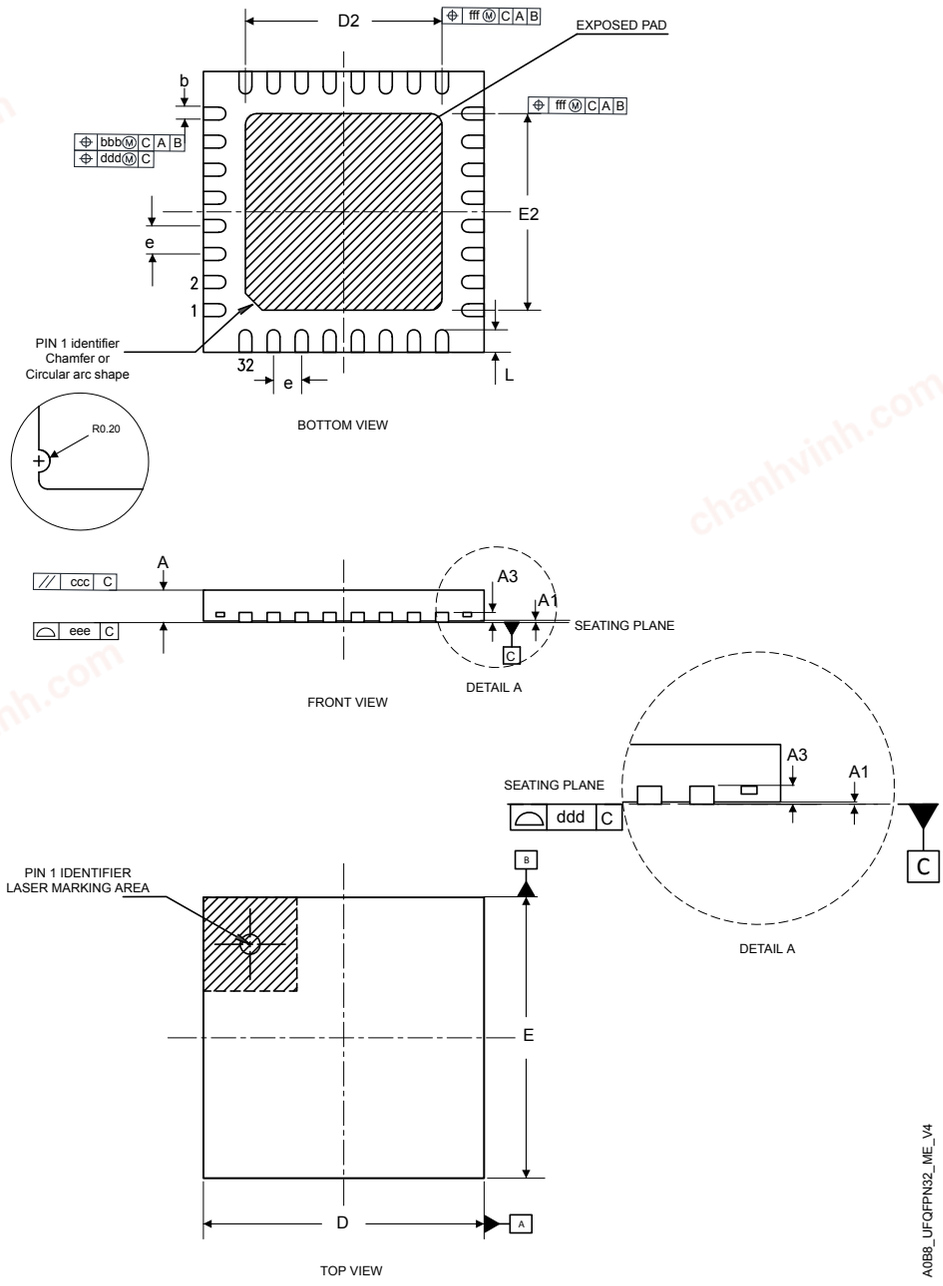
A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

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7.2 UFQFPN32 package information (A0B8)

This UFQFPN is a 32 pins, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package.

Figure 34. UFQFPN32 - Outline



1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.*

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Table 89. UFQFPN32 - Mechanical data

Symbol	millimeters[1]			inches[2]		
	Min	Typ	Max	Min	Typ	Max
A[3][4]	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1[5]	0.00	-	0.05	0.000	-	0.0020
A3[6]	-	0.15	-	-	0.0060	-
b[7]	0.18	0.25	0.30	0.0071	0.010	0.0118
D[8][9]	5.00 BSC			0.1969 BSC		
D2	3.50	3.60	3.70	0.139	0.143	0.147
E[8][9]	5.00 BSC			0.1969 BSC		
E2	3.50	3.60	3.70	0.139	0.143	0.147
e[9]	-	0.50	-	-	0.02	-
N[10]	32					
K	0.15	-	-	0.006	-	-
L	0.30	-	0.50	0.0119	-	0.0199
R	0.09	-	-	0.004	-	-

1. *All dimensions are in millimetres. Dimensioning and tolerancing schemes are conform to ASME Y14.5M-2018 except European .*
2. *Values in inches are converted from mm and rounded to 4 decimal digits.*
3. *UFQFPN stands for Ultra thin Fine pitch Quad Flat Package No lead: A ≤ 0.60mm / Fine pitch e ≤ 1.00mm.*
4. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
5. *A1 is the vertical distance from the bottom surface of the plastic body to the nearest metallized package feature.*
6. *A3 is the distance from the seating plane to the upper surface of the terminals.*
7. *Dimension b applies to metallized terminal. If the terminal has the optional radius on the other end of the terminal, the dimension b must not be measured in that radius area.*
8. *Dimensions D and E do not include mold protrusion, not to exceed 0,15mm.*
9. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to Table 90*
10. *N represents the total number of terminals.*

Table 90. Tolerance of form and position

Symbol[1]	Tolerance of form and position[2] In millimeters	Tolerance of form and position[3] In inches
aaa	0.15	0.006
bbb	0.10	0.004
ccc	0.10	0.004
ddd	0.05	0.002
eee	0.10	0.004
fff	0.10	0.004

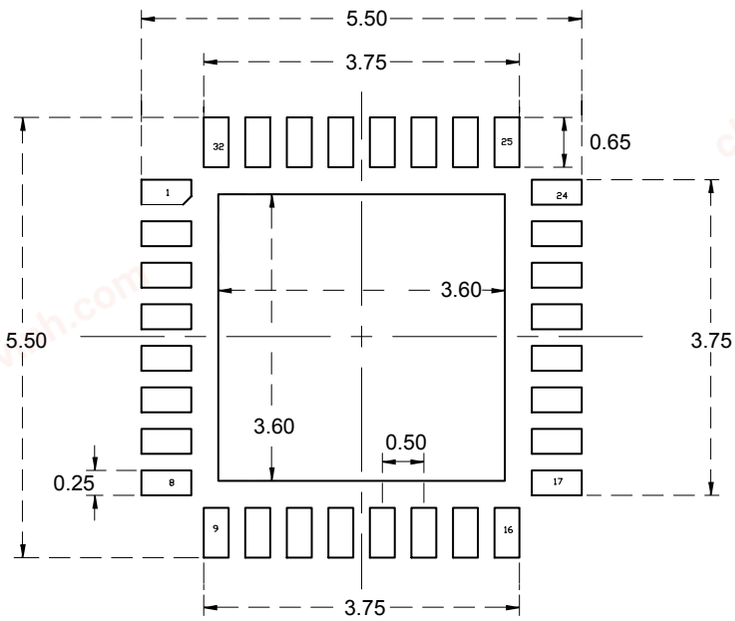
1. *For the tolerance of form and position definitions see Table 91.*
2. *All dimensions are in millimetres. Dimensioning and tolerancing schemes are conform to ASME Y14.5M-2018 except European .*
3. *Values in inches are converted from mm and rounded to 4 decimal digits.*

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Table 91. Tolerance of form and position symbol definition

Symbol	Definition
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centres of the profile zones are defined by the basic dimensions D and E.
bbb	The tolerance that controls the position of the terminals with respect to Datums A and B. The centre of the tolerance zone for each terminal is defined by basic dimension e as related to datums A and B.
ccc	The tolerance located parallel to the seating plane in which the top surface of the package must be located.
ddd	The tolerance that controls the position of the terminals to each other. The centres of the profile zones are defined by basic dimension e.
eee	The unilateral tolerance located above the seating plane wherein the bottom surface of all terminals must be located = coplanarity
fff	The tolerance that controls the position of the exposed metal heat feature. The centre of the tolerance zone is the data defined by the centrelines of the package body

Figure 35. UFQFPN32 - Footprint example



A0B8_UFQFPN32_FP_V1

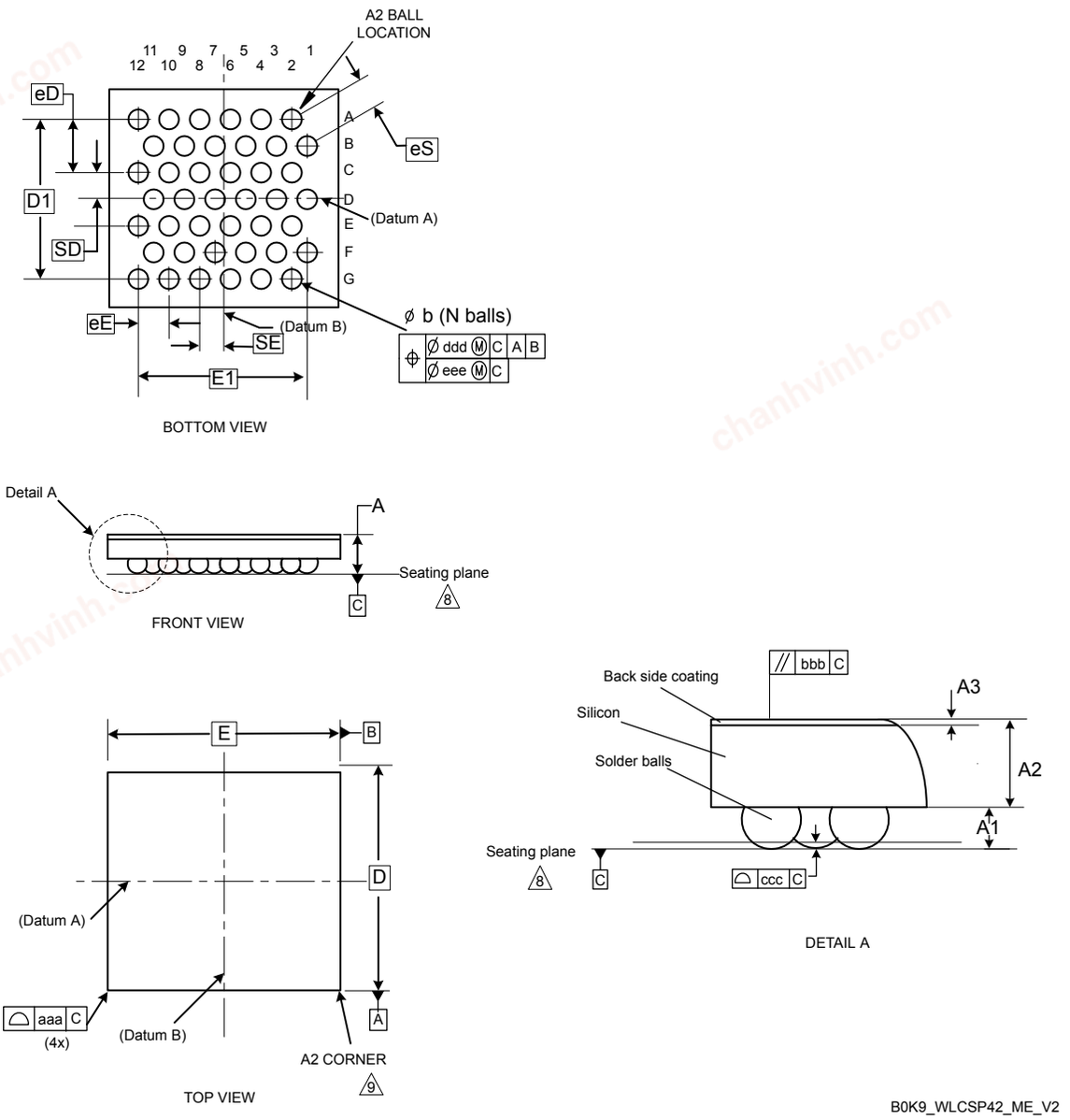
1. *Dimensions are expressed in millimeters.*

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7.3 WLCSP42 package information (B0K9)

This WLCSP is a 42-ball, 2.82 x 2.93 mm, 0.40 mm pitch, wafer level chip scale package.

Figure 36. WLCSP42 - Outline



1. *Drawing is not to scale*

Table 92. WLCSP42 - Mechanical data

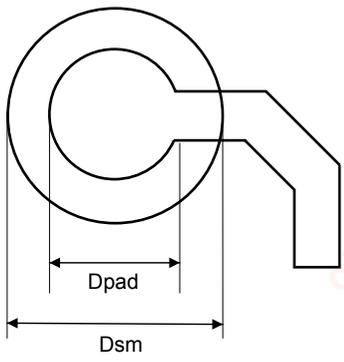
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	-	-	0.58	-	-	0.0228
A1(3)	-	0.17	-	-	0.0067	-

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Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A2	-	0.38	-	-	0.0150	-
A3 (if applicable)	-	0.025	-	-	0.0010	-
b[4]	0.23	0.25	0.28	0.0090	0.0098	0.0110
D[5]	2.82 BSC			0.1110 BSC		
D1[5]	2.078 BSC			0.0818 BSC		
E[5]	2.93 BSC			0.1153 BSC		
E1[5]	2.200 BSC			0.0866 BSC		
eD[5][6]	0.693 BSC			0.0273 BSC		
eE[5][6]	0.400 BSC			0.0157 BSC		
eS[5][6]	0.400 BSC			0.0157 BSC		
N[7]	42					
SD[5][8]	0.346 BSC			0.0136 BSC		
SE[5][8]	0.300 BSC			0.0118 BSC		
aaa[9]	0.030			0.0012		
bbb[9]	0.060			0.0023		
ccc[9]	0.030			0.0012		
ddd[9]	0.015			0.0006		
eee[9]	0.050			0.0020		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height A is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to Datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances, refer to form and position table. On the drawing, these dimensions are framed. For the tolerances, refer to form and position values.*
6. *e represents the solder balls grid pitch(es).*
7. *N represents the total number of balls.*
8. *Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.*
9. *Tolerance of form and position drawing*

Figure 37. WLCSP42 - Footprint example



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1. *Dimensions are expressed in millimeters.*

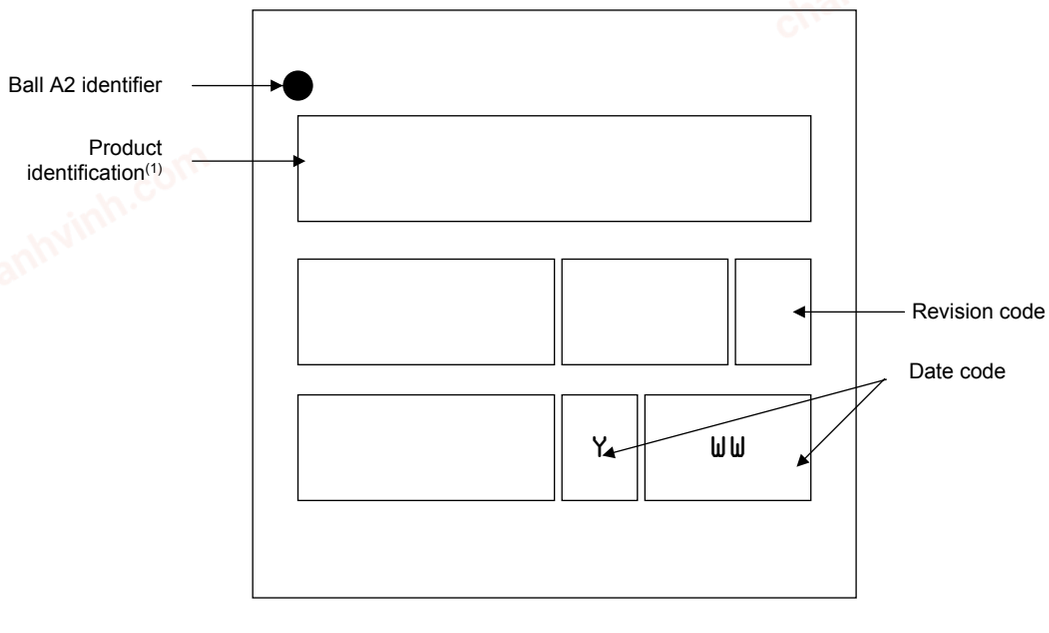
Table 93. WLCSP42 - Example of PCB design rules

Dimension	Values
Pitch	0.400 mm
Dpad	0,250 mm
Dsm	0.325 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.325 mm
Stencil thickness	0.100 mm

7.3.1 Device marking for WLCSP42

The following figure gives an example of topside marking versus ball A2 position identifier location.
The printed markings may differ depending on the supply chain.
Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 38. WLCSP42 marking example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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7.4 LQFP48 package information (5B)

This LQFP is a 48-pins, 7 x 7 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 39. LQFP48- Outline(15.)

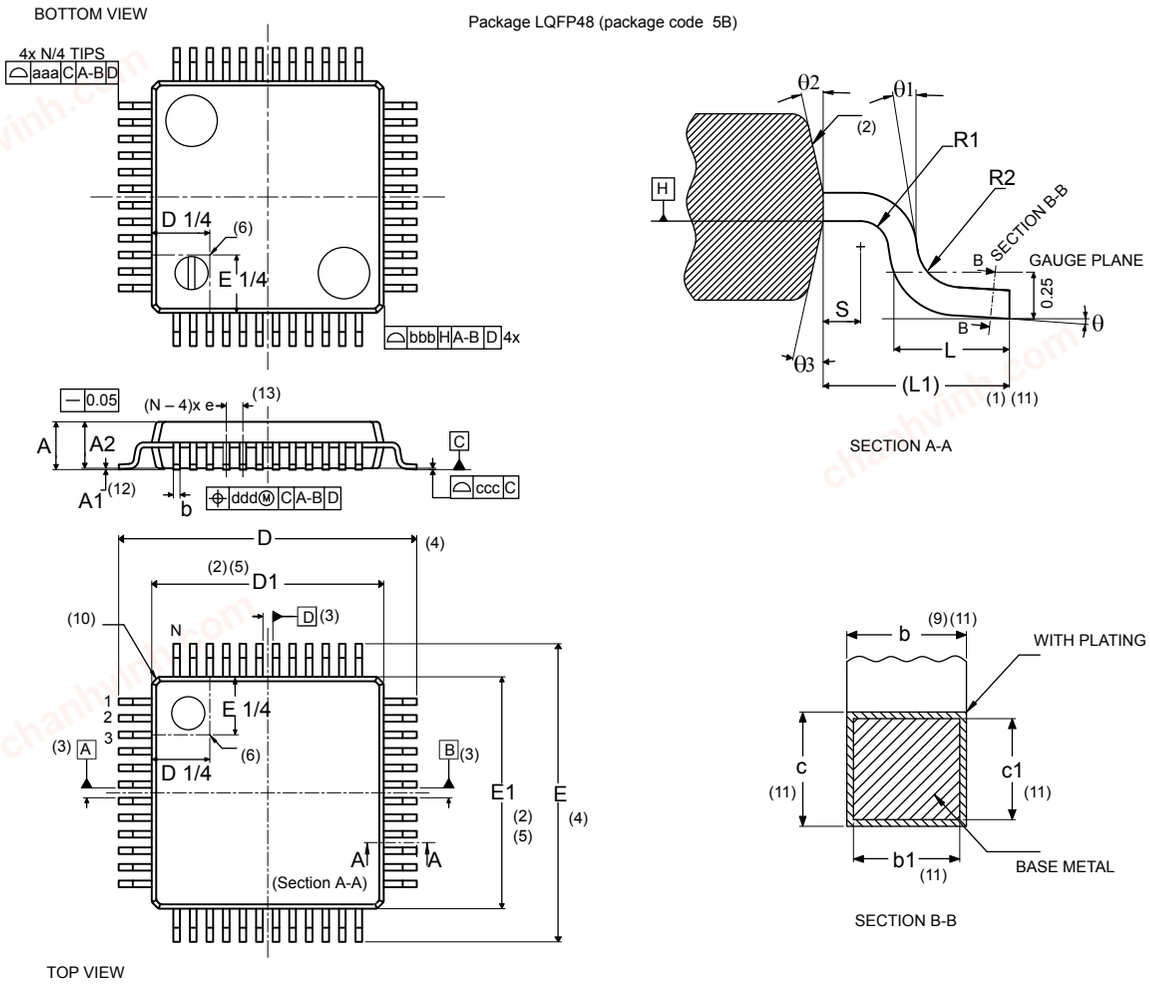


Table 94. LQFP48 - Mechanical data

Symbol	millimeters			inches(14.)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1(12.)	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b(9.)(11.)	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1(11.)	0.17	0.20	0.23	0.0067	0.0079	0.0090
c(11.)	0.09	-	0.20	0.0035	-	0.0079
c1(11.)	0.09	-	0.16	0.0035	-	0.0063

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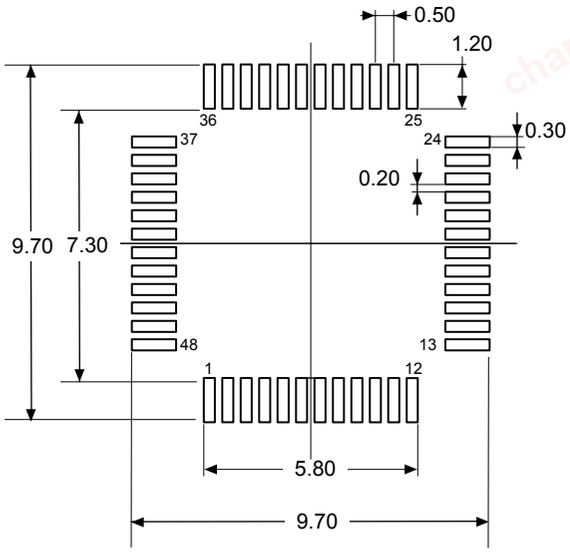
Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
D[4.]		9.00 BSC			0.3543 BSC	
D1[4.][5.]		7.00 BSC			0.2756 BSC	
E[4.]		9.00 BSC			0.3543 BSC	
E1[4.][5.]		7.00 BSC			0.2756 BSC	
e		0.50 BSC			0.1970 BSC	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00 REF			0.0394 REF	
N[13.]		48				
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.][7.]		0.20			0.0079	
bbb[1.][7.]		0.20			0.0079	
ccc[1.][7.]		0.08			0.0031	
ddd[1.][7.]		0.08			0.0031	

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits
15. Drawing is not to scale.

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Figure 40. **LQFP48 - Footprint example**



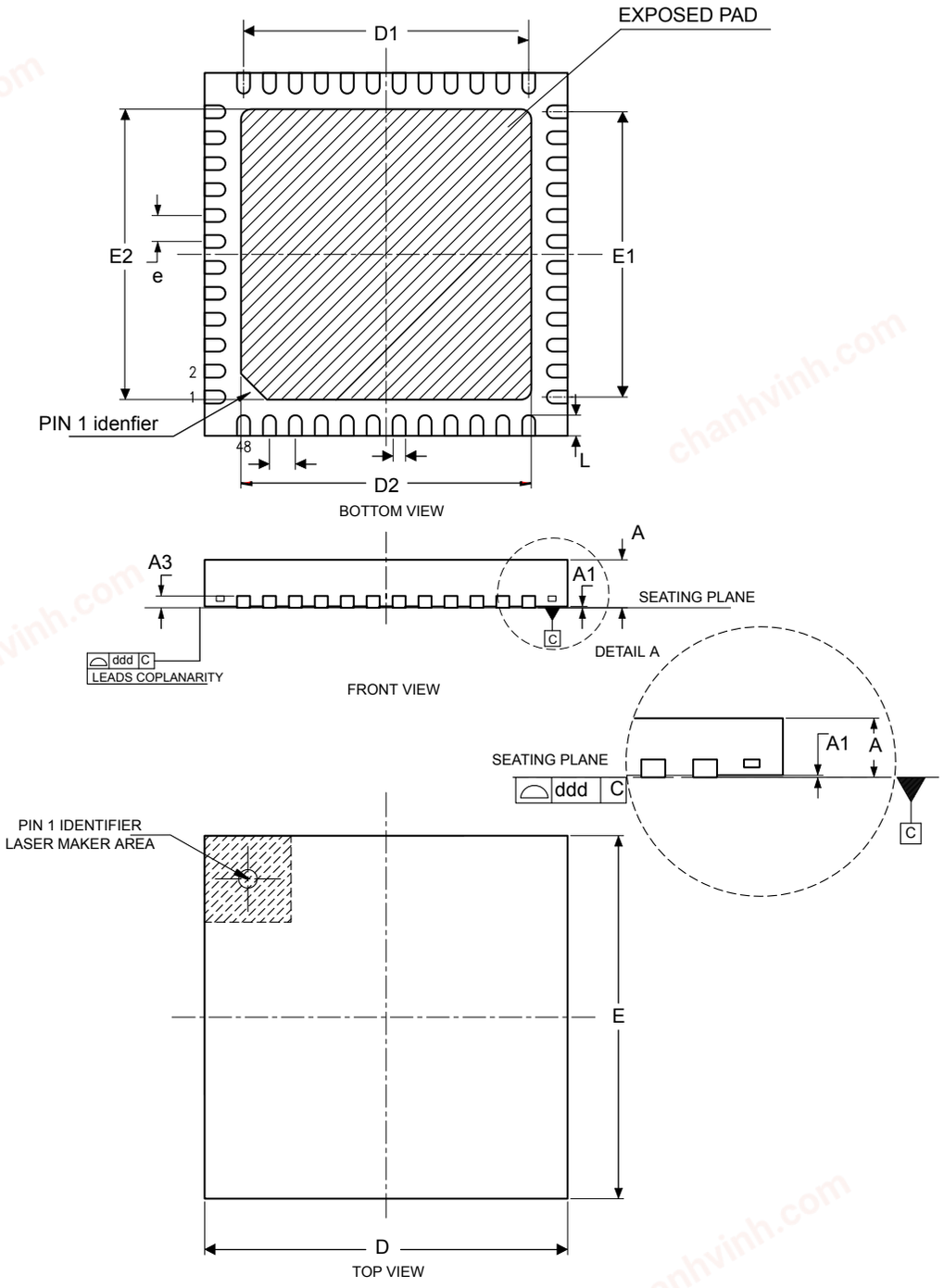
1. *Dimensions are expressed in millimeters.*

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7.5 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 41. UFQFPN48 - Outline



1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the under side of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.*

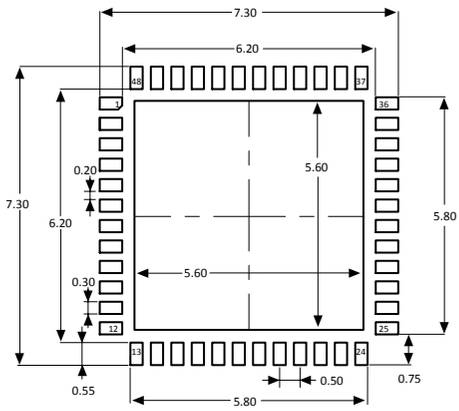
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Table 95. UFQFPN48 - Mechanical data

Symbol	Millimeters			Inches (1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D(2)	6.900	7.000	7.100	0.2717	0.2756	0.2795
D1	5.400	5.500	5.600	0.2126	0.2165	0.2205
D2(3)	5.500	5.600	5.700	0.2165	0.2205	0.2244
E(2)	6.900	7.000	7.100	0.2717	0.2756	0.2795
E1	5.400	5.500	5.600	0.2126	0.2165	0.2205
E2(3)	5.500	5.600	5.700	0.2165	0.2205	0.2244
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.*
3. *Dimensions D2 and E2 are not in accordance with JEDEC.*

Figure 42. UFQFPN48 - Footprint example



DT_A0B9_UFQFPN48_FP_V3

1. *Dimensions are expressed in millimeters.*

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7.6 LQFP64 package information (5W)

This is a 64-pins, 10 x 10 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 43. LQFP64 - Outline(15.)

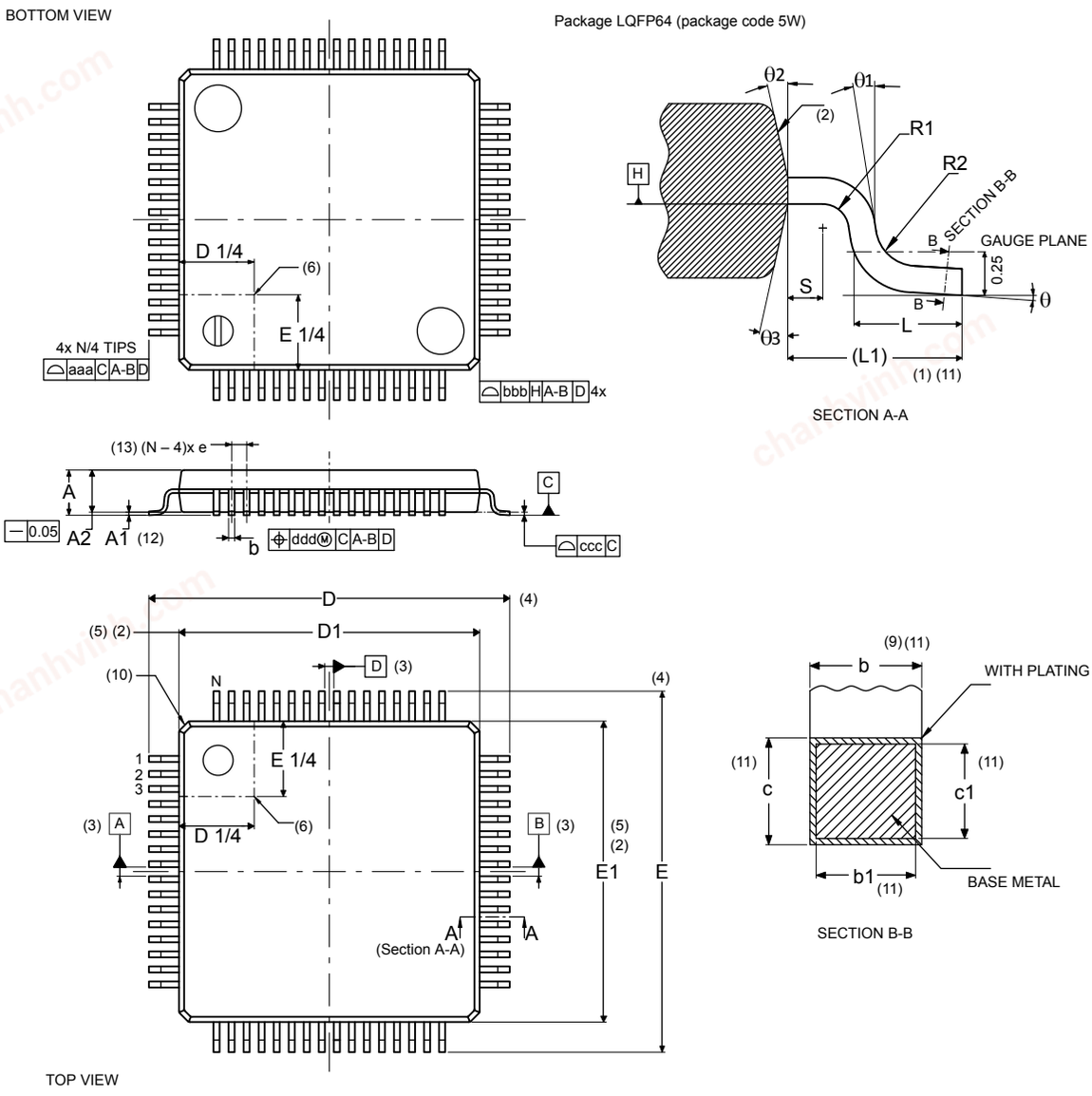


Table 96. LQFP64 - Mechanical data

Symbol	millimeters			inches(14.)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1(12.)	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b(9.)(11.)	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1(11.)	0.17	0.20	0.23	00067	0.0079	0.0091

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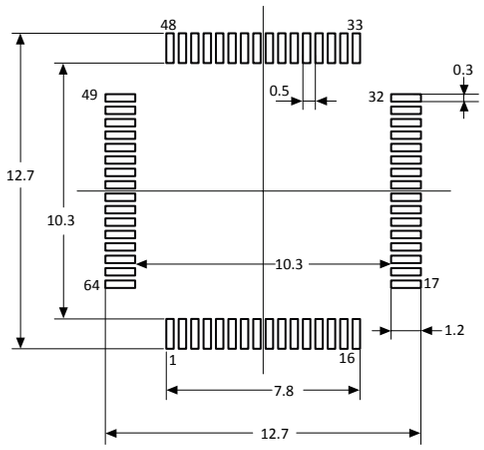
Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]		12.00 BSC			0.4724 BSC	
D1[2.][5.]		10.00 BSC			0.3937 BSC	
E[4.]		12.00 BSC			0.4724 BSC	
E1[2.][5.]		10.00 BSC			0.3937 BSC	
e		0.500 BSC			0.0197 BSC	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
N[13.]		64				
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]		0.20			0.0079	
bbb[1.]		0.20			0.0079	
ccc[1.]		0.08			0.0031	
ddd[1.]		0.08			0.0031	

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

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Figure 44. **LQFP64 - Footprint example**



1. *Dimensions are expressed in millimeters.*

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7.7 UFBGA64 package information (A019)

This UFBGA is a 64-ball, 5 x 5 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 45. UFBGA64 - Outline(13.)

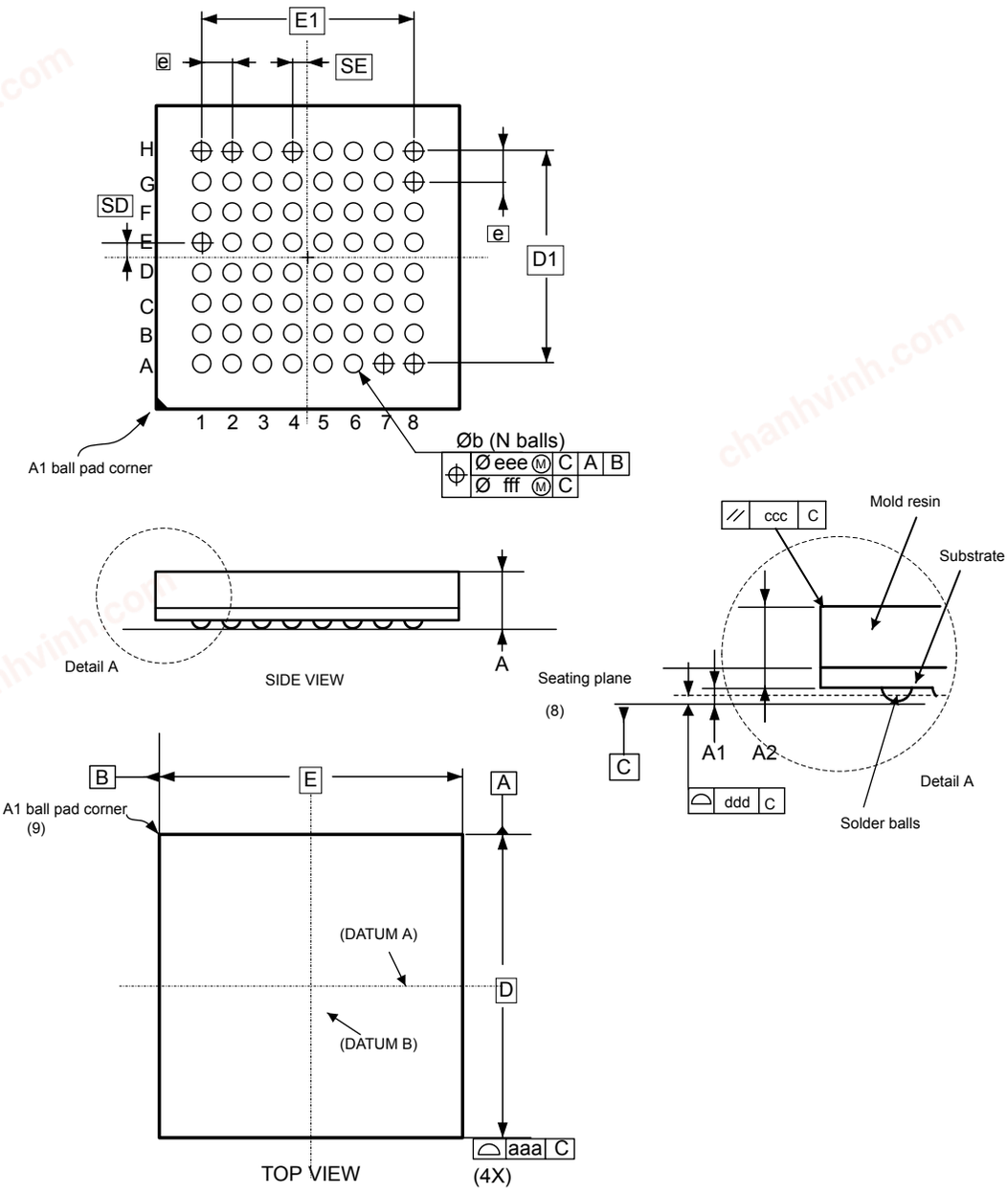


Table 97. UFBGA64 - Mechanical data

Symbol	millimeters(1.)			inches (12.)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A(2.)(3.)	-	-	0.60	-	-	0.0236
A1(4.)	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-

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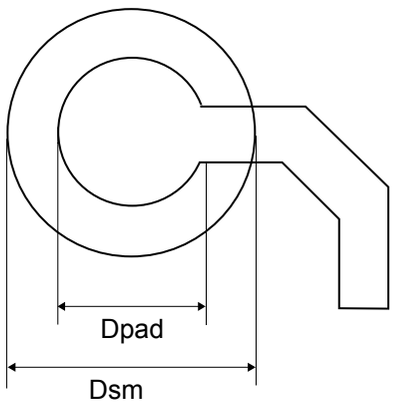
Symbol	millimeters[1.]			inches [12.]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b[5.]	0.23	0.28	0.33	0.0090	0.0110	0.0130
D[6.]		5.00 BSC			0.1969 BSC	
D1		3.50 BSC			0.1378 BSC	
E		5.00 BSC			0.1969 BSC	
E1		3.50 BSC			0.1378 BSC	
e[9.]		0.50 BSC			0.0197 BSC	
N[10.]		64				
SD[11.]		0.25 BSC			0.0098 BSC	
SE[11.]		0.25 BSC			0.0098 BSC	
aaa		0.15			0.0059	
ccc		0.20			0.0079	
ddd		0.08			0.0031	
eee		0.15			0.0059	
fff		0.05			0.0020	

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ultra profile fine pitch ball grid array: 0.50 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale

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Figure 46. **UFBGA64 - Footprint example**



DT_BGA_WLCSP_FT_V1

Table 98. **UFBGA64 - Recommended PCB design rules (0.50 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm aperture diameter
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

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7.8 LQFP80 package information (9X)

This is a 80-pins, 12 x 12 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 47. **LQFP80 - Outline(15.)**

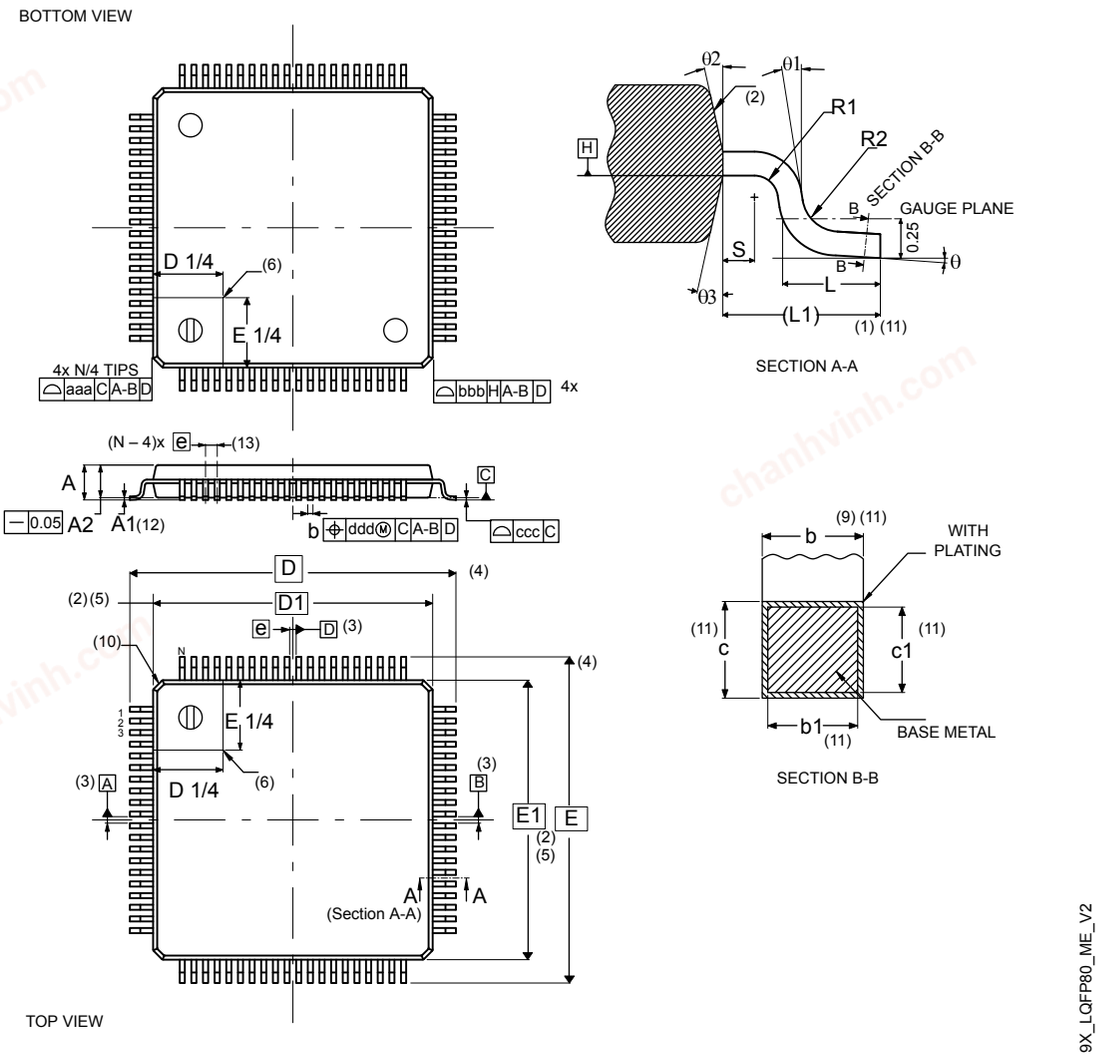


Table 99. **LQFP80 - Mechanical data**

Symbol	millimeters			inches(14.)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1(12.)	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b(9.)(11.)	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1(11.)	0.17	0.20	0.23	00067	0.0079	0.0091
c(11.)	0.09	-	0.20	0.0035	-	0.0079
c1(11.)	0.09	-	0.16	0.0035	-	0.0063

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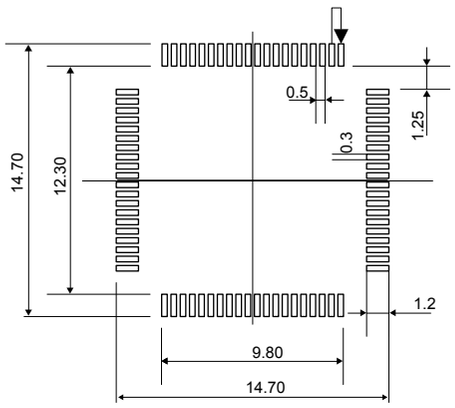
Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
D[4.]		14.00 BSC			0.5512 BSC	
D1[2.][5.]		12.00 BSC			0.4724 BSC	
E[4.]		14.00 BSC			0.5512 BSC	
E1[2.][5.]		12.00 BSC			0.4724 BSC	
e		0.50 BSC			0.0197 BSC	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
N[13.]		80				
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]		0.20			0.0079	
bbb[1.]		0.20			0.0079	
ccc[1.]		0.08			0.0031	
ddd[1.]		0.08			0.0031	

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

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Figure 48. **LQFP80 - Footprint example**



1. *Dimensions are expressed in millimeters.*

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7.9 UFBGA81 package information (B0B8)

This UFBGA is a 81-ball, 5 x 5 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 49. **UFBGA81 - Outline(13.)**

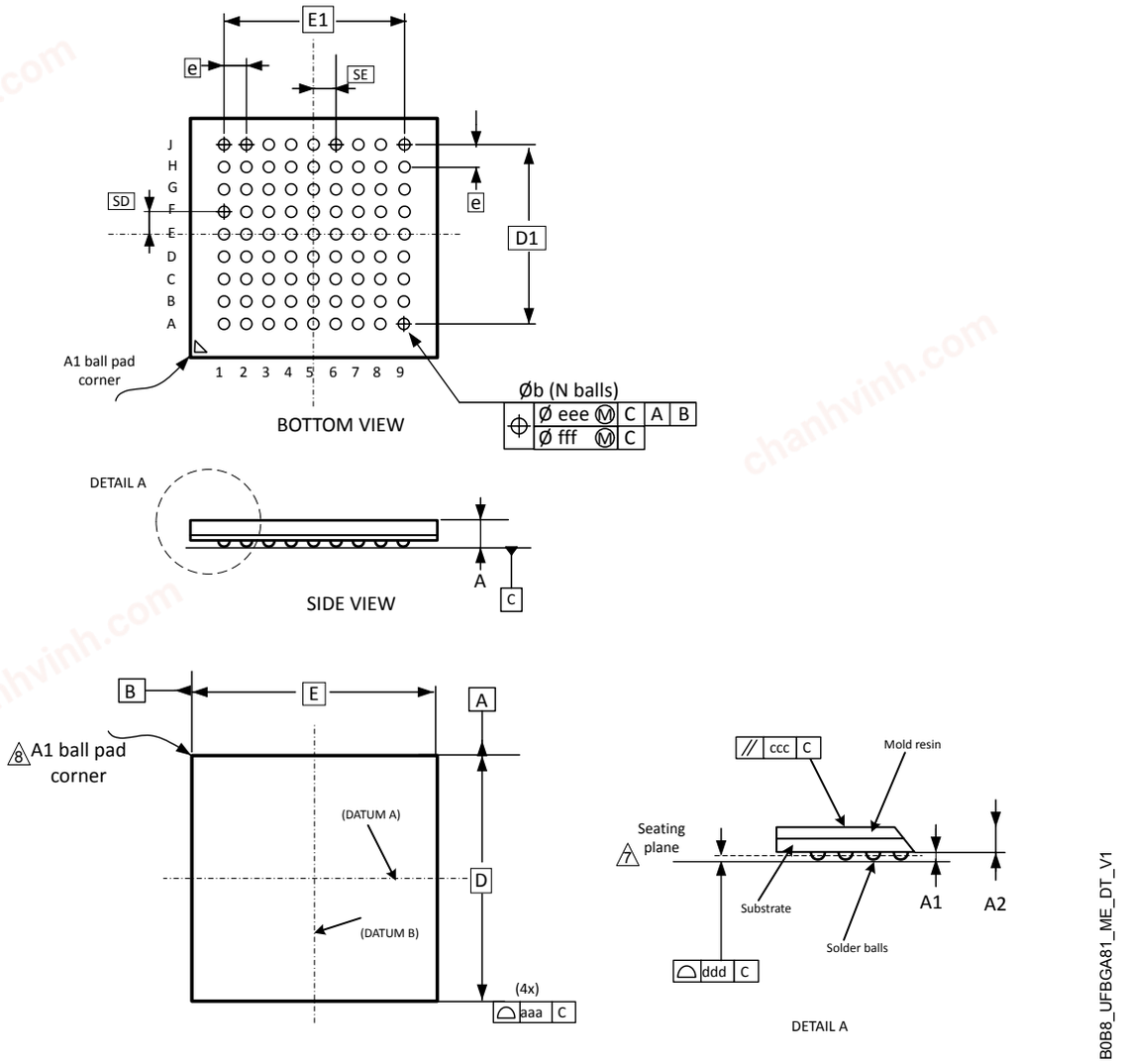


Table 100. **UFBGA81 - Mechanical data**

Symbol	millimeters(1.)			inches (12.)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A(2.)(3.)	-	-	0.60	-	-	0.0236
A1(4.)	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-
b(5.)	0.23	0.28	0.33	0.0090	0.0110	0.0130
D(6.)	5.00 BSC			0.1969 BSC		
D1	3.50 BSC			0.1378 BSC		

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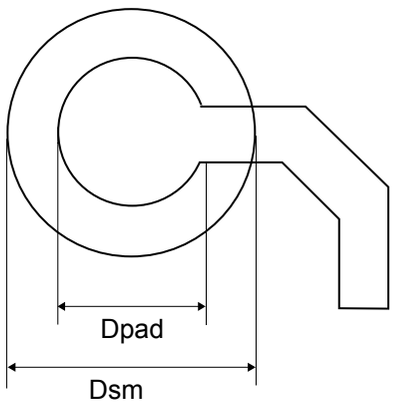
Symbol	millimeters[1.]			inches [12.]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E		5.00 BSC			0.1969 BSC	
E1		3.50 BSC			0.1378 BSC	
e[9.]		0.50 BSC			0.0197 BSC	
N[10.]			81			
SD[11.]		0.25 BSC			0.0098 BSC	
SE[11.]		0.25 BSC			0.0098 BSC	
aaa		0.15			0.0059	
ccc		0.20			0.0079	
ddd		0.08			0.0031	
eee		0.15			0.0059	
fff		0.05			0.0020	

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ultra profile fine pitch ball grid array: 0.50 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale

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Figure 50. **UFBGA81 - Footprint example**



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Table 101. **UFBGA81 - Example of PCB design rules (0.50 mm pitch BGA)**

Dimension	Values
Pitch	0.50 mm
Dpad	0.250 mm
Dsm	0.300 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.356 mm aperture diameter
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

7.10 Package thermal characteristics

The operating junction temperature, T_J, must never exceed the maximum given in Section 6.3.1: General operating conditions.

The maximum junction temperature in °C that the device can reach if respecting the operating conditions, is: operating conditions, is:

$$T_J \max = T_A \max + \left(P_D \max \times \Theta_{JA}\right)$$

where:

- T_{Amax} is the maximum ambient temperature, in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.
- $P_D = P_{INT} + P_{I/O}$
  - P_{INT} is the power dissipation contribution from product to I_{DD} and V_{DD}, expressed in Watts.
  - $P_{I/O}$ is the power dissipation contribution from output ports where: $P_{I/O} = \sum\left(V_{OL} \times I_{OL}\right) + \sum\left(\left(V_{DDIOx} - V_{OH}\right)\right) \times I_{OH}$ taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 102. **Package thermal characteristics**

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	UFQFPN32	39.9	°C/W
		WLCSP42	62.9	
		LQFP48	53.2	
		UFQFPN48	29.5	

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Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	LQFP64	43.9	°C/W
		UFBGA64	54.2	
		LQFP80	42.4	
		UFBGA81	51.5	
Θ_{JB}	Thermal resistance junction-board	UFQFPN32	21.8	
		WLCSP42	38.2	
		LQFP48	28.1	
		UFQFPN48	13.8	
		LQFP64	28.6	
		UFBGA64	37.3	
		LQFP80	26.7	
		UFBGA81	34.4	
Θ_{JC}	Thermal resistance junction-top case	UFQFPN32	16.8	
		WLCSP42	3.9	
		LQFP48	16.5	
		UFQFPN48	10.3	
		LQFP64	13.9	
		UFBGA64	15.4	
		LQFP80	13.6	
		UFBGA81	15.4	

7.10.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air) available on www.jedec.org.
- For information on thermal management, refer to application note *"Guidelines for thermal management on STM32 applications" (AN5036)* available on www.st.com.

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8 Ordering information

Example: STM32 U 083 M C T 6 TR

Device family

STM32 = Arm®-based 32-bit microcontroller

Product type

U = Ultra-low-power

Device subfamily

083 = STM32U083xx

Pin count

K = 32 pins

H = 42 ball

C = 48 pins

R = 64 pins/balls

M = 80/81 pins/balls

Flash memory size

C = 256 Kbytes of flash memory

Package

T = LQFP ECOPACK2

U = UFQFPN ECOPACK2

I = UFBGA ECOPACK2

Y = WLCSP ECOPACK2

Temperature range

3 = Industrial temperature range, –40 to 125 °C (130 °C junction)

6 = Industrial temperature range, –40 to 85°C (105 °C junction)

Packing

TR = Tape and reel

xxx = Programmed parts

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

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Revision history

Table 103. **Document revision history**

Date	Revision	Changes
01-Mar-2024	1	Initial release.
18-Mar-2024	2	Updated ULPMark™-CP value on cover page. Added Section 3.22: Touch sensing controller (TSC). Updated Table 39. Current consumption in Stop 1 mode. Added $I_{DD\ (Stop\ 2)}$ maximum values in Table 40. Current consumption in Stop 2 mode. Added $I_{DD\ (SRAM2)}$ maximum values in Table 41. Current consumption in Standby mode.

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