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STM32N647xx STM32N657xx

Arm® Cortex®-M55, ST Neural-ART Accelerator, H264 encoder, Neo-Chrom 2.5D GPU, 4.2 Mbyte-contiguous SRAM

Datasheet - production data

Features

- Includes ST state-of-the-art patented technology

Core

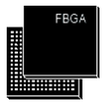
- Arm® 32-bit Cortex®-M55, 3360 CoreMark®, frequency up to 800 MHz, 1280 DMIPS, 32-Kbyte ICACHE, 32-Kbyte DCACHE
- Arm® MVE (M-Profile vector extension)
- Arm® Helium™ technology
- Arm® TrustZone® MPU, NVIC
- Single and half-precision floating point unit

Neural processing unit

- ST Neural-ART Accelerator, frequency up to 1 GHz, 600 Gops, 288 MAC/cycle
- Specialized hardware units for DNN (deep-neural network) inference functions
- Flexible dedicated stream processing engine
- Real-time encryption/decryption
- On-the-fly weight decompression

Memories

- 4.2-Mbyte contiguous SRAM
- 128-Kbyte TCM (tightly-coupled memory) RAM with ECC for critical real-time data + 64-Kbyte instruction TCM RAM with ECC for critical real-time routines
- 8-Kbyte backup SRAM active in V_{BAT} mode
- Flexible external memory controller with cypher engine supporting up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- XSPI with support for serial PSRAM, NAND, NOR, HyperRAM™/ HyperFlash™ frame formats
- 2 ports: XSPIM 8- and 16-bit configuration up to 200 MHz



VFBGA142 (8 x 8 mm) pitch 0.5 mm
VFBGA169 (6 x 6 mm) pitch 0.4 mm
VFBGA178 (12 x 12 mm) pitch 0.8 mm
VFBGA198 (10 x 10 mm) pitch 0.65 mm
VFBGA223 (10 x 10 mm) pitch 0.5 mm
VFBGA264 (14 x 14 mm) pitch 0.8 mm

Graphics

- Neo-Chrom 2.5D GPU: scaling, rotation, alpha blending, texture mapping, perspective transformation
- Chrom-ART Accelerator (DMA2D)
- Hardware JPEG codec with MJPEG
- LCD-TFT controller up to XGA resolution

Video

- Parallel and 2-lane CSI-2 camera interfaces
- ISP (image signal processor) with three parallel pipes on the same input stream: bad pixel, decimation, black level, exposure, de-mosaic, column conversion, contrast, crop, downsize, ROI, gamma, YUV convention, pixel packer
- H264 video encoding acceleration: baseline profile, main profile, high profile level 1 to level 5.2, 1080p30 and 720p60

Security and cryptography

- Arm® TrustZone® and securable I/Os memories and peripherals
- SESIP Level 3 (security evaluation standard for IoT platforms), Arm® PSA (platform security architecture) certified
- Flexible life-cycle scheme with RDP and password-protected debug
- Secure provisioning of customer keys in OTP (one-time programmable) fuses
- Secure boot code in ROM, decrypting and authenticating customer uRoT (updatable root-of-trust)
- Secure data storage with hardware-unique key (HUK)

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- Secure firmware upgrade support with TF-M (trusted firmware-M)
- Two AES coprocessors, including one with DPA (differential power analysis) resistance
- Public key accelerator (PKA), DPA resistant
- On-the-fly encryption/decryption of external memories
- HASH hardware accelerator
- True random number generator (RNG), NIST SP800-90B compliant
- 96-bit unique ID
- 1.5-Kbyte OTP fuses
- Active tampers

Communication peripherals

- 2x USB 2.0 high-speed/full-speed device/host OTG controllers (one with UCPD USB Type-C® Power Delivery)
- 10-Mbit, 100-Mbit, and 1-Gbit Ethernet with TSN (time-sensitive networking)
- 4x I2C Fm+ interfaces (SMBus/PMBus®) + 2x I3C
- 6x SPI, of which four I2S-capable
- 2x SAI, with four DMIC support
- 5x USART, 5x UART (ISO78916 interface, LIN, IrDA, up to 12.5 Mbit/s) + 1x LPUART
- 2x SDMMC: MMC version 4.0, CE-ATA version 1.0, and SD version 1.0.1
- 3x FDCAN with TTCAN capability

Low power

- Sleep, Stop and Standby modes
- V_{BAT} supply for RTC, 32x 32-bit backup registers + 8-Kbyte backup SRAM

Timers and watchdogs

- 1x high-resolution timer
- 4x 32-bit timers with up to four IC/OC/PWM or pulse counters and quadrature (incremental) encoder input (up to 240 MHz)
- 2x 16-bit advanced motor control timers (up to 240 MHz)
- 13x 16-bit general-purpose and 5x 16-bit low-power timers (up to 240 MHz)
- 2x watchdogs (independent and window)
- 1x SysTick timer
- RTC with subsecond accuracy and hardware calendar

Debug

- Development support: serial-wire debug (SWD), JTAG
- Embedded Trace Macrocell™ (ETM)

General-purpose I/Os

- Up to 165 pins

Analog peripherals

- 1x temperature sensor
- 2x ADCs with 12-bit maximum resolution (up to 5 Msps), up to 20 channels
- 1x ADF filter with SAD and 1x MDF (six filters)

Reset and power management

- POR, PDR, PBVD, and BOR
- Embedded SMPS step-down converter providing V_{DDCORE}
- 1.71 to 3.6 V application supply and I/Os
- Dedicated power for USB and XSPI I/Os
- Backup regulator (~0.9 V)
- Voltage reference for analog peripheral (V_{REF+})

Clock management

- Internal oscillators: 64 MHz HSI, 4 MHz MSI, 32 kHz LSI
- External oscillators: 16 to 48 MHz HSE, 32.768 kHz LSE
- 4x PLL (one for the system clock, one for the ST Neural-ART Accelerator, two for kernel clocks) with fractional mode

ECOPACK2 compliant packages

Table 1. Device summary

Reference	Part numbers
STM32N647xx	STM32N647A0, STM32N647B0, STM32N647I0, STM32N647L0, STM32N647X0, STM32N647Z0
STM32N657xx	STM32N657A0, STM32N657B0, STM32N657I0, STM32N657L0, STM32N657X0, STM32N657Z0

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32N647xx and STM32N657xx (hereafter referred to as STM32N6x7xx) MCUs.

For information on the device errata with respect to the datasheet and reference manual (RM0486) refer to the errata sheet ES0620.

For information on the Arm®(a) Cortex®-M55 core, refer to the Cortex®-M55 Technical Reference Manual, available from the www.arm.com website.

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2 Description

The STM32N6x7xx devices are based on the high-performance Arm® Cortex®-M55, operating at a frequency up to 800 MHz.

The Cortex®-M55 core features the Arm® Helium™ vector processing technology. On top of standard microcontroller tasks, this core enables energy-efficient digital signal processing. The Cortex®-M55 is equipped with a floating-point unit (FPU) that supports single- and half-precision (IEEE 754 compliant) data-processing. The Cortex®-M55 includes a 32-Kbyte ICACHE, a 32-Kbyte DCACHE, as well as 128-Kbyte data TCM RAM and 64-Kbyte instruction TCM RAM with ECC for critical real-time routines.

These microcontrollers have TrustZone®-aware support and a memory protection unit (MPU) for enhanced application security. A secure boot ROM ensures secure booting from external interfaces.

The devices embed a 4.2-Mbyte contiguous SRAM organized in several banks, an 8-Kbyte backup SRAM active in V_{BAT} mode, and a flexible external memory controller (FMC) for static memories, XSPI 8-/16-bit configurations.

The ST Neural-ART accelerator, running at up to 1 GHz and providing 600 Gops using optimized hardware units for DNN (deep-neural network) inference functions. optimizes power efficiency. Dedicated streaming engines are integrated into it to optimize data flow and minimize internal buffer usage and power. The accelerator supports on-the-fly weight decompression and real-time data encryption and decryption.

The Neo-Chrom graphic accelerator ensures efficient 2.5D graphic processing, by providing hardware acceleration for functions like scaling, using high-quality interpolation, free rotation, alpha blending, texture mapping, and perspective transformation.

For camera applications, a parallel and CSI interface together with an integrated hardware ISP is foreseen. The ISP provides processing of three parallel pipes on the same input stream. Supported algorithms are bad pixel, decimation, black-level tuning, exposure control, de-mosaicking, column conversion, contrast, cropping, downsizing, ROI isolation, gamma correction, YUV conversion, and pixel packer. The ISP output can be directly fed via a DMA to the NPU.

Optionally, the devices embed a hardware H264 encoding block supporting baseline profile, main profile and high profile level 1 to level 5.2, supporting frame rates of up to 30 frames per second for 1080p resolution.

A dedicated hardware accelerator ensures fast and simple JPEG and motion JPEG compression and decompression.

The devices offer an extensive range of enhanced I/Os and peripherals, and operate in the -40 to +125 °C temperature range, from 1.71 to 3.6 V power supply. A comprehensive set of low-power modes (Sleep, Stop, and Standby) allows the design of low-power applications.

The STM32N6x7xx devices are offered in six VFBGA packages, ranging from 142 to 264 pins.

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Table 2. STM32N647xx features and peripheral counts

Feature / Peripheral		STM32 N647X0	STM32 N647L0	STM32 N647B0	STM32 N647I0	STM32 N647A0	STM32 N647Z0
SRAM	System (Mbytes)	4.2					
	Backup (Kbytes)	8					
XSPI	16 bits	1		1[(1)]	0		
	8 bits	1					
Timers	Advanced control	2	1				0
	General purpose	10				7	
	Basic	3				2	1
	Low-power	5	4		2	1	
Communication interfaces	I2S	3				1	0
	SPI	6					5
	I2C	4				3	
	I3C	2					
	USART	5		4		3	2
	UART	5			4	3	
	LPUART	1					
	SAI	2					
	FDCAN	3					
	OTG HS	2					
	UCPD	Yes					
	SDMMC	2		1		0	
	CSI	Yes					
	PSSI	Yes					
	LTDC	Yes					
FMC	FMC_NOR32	Yes		No			
	FMC_NOR16						
	FMC_NORMUX			Yes			No
	FMC SDRAM32			No			
	FMC SDRAM16			Yes		No	
	FMC_NAND16						
Multi-function digital filter (MDF)		6 filters					2 filters
Audio digital filter (ADF)		Yes					

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Table 2. STM32N647xx features and peripheral counts (continued)

Feature / Peripheral		STM32 N647X0	STM32 N647L0	STM32 N647B0	STM32 N647I0	STM32 N647A0	STM32 N647Z0
Crypto	SAES	No					
	CRYPT	No					
	PKA	No					
	MCE1.4	No					
Accelerator	Neural-ART	Yes					
Real time clock (RTC)		Yes					
RNG		Yes					
ADC (12 bits)		2					
Digital temperature sensor (DTS)		Yes					
Internal voltage reference buffer		Yes					
Maximum CPU frequency		600 MHz, 800 MHz with overdrive mode					
Operating voltage		1.71 to 3.6 V					
Operating temperature	Ambient	-40 to 125 °C					
Package	Name	VFBGA264	VFBGA223	VFBGA198	VFBGA178	VFBGA169	VFBGA142
	Size	14 x 14 mm	10 x 10 mm	10 x 10 mm	12 x 12 mm	6 x 6 mm	8 x 8 mm
	Pitch	0.8 mm	0.5 mm	0.65 mm	0.8 mm	0.4 mm	0.5 mm
Number of IOs		165	144	126	106	90	75

1. Operates only in 8-bit mode.

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Table 3. STM32N657xx features and peripheral counts

Feature / Peripheral		STM32 N657X0	STM32 N657L0	STM32 N657B0	STM32 N657I0	STM32 N657A0	STM32 N657Z0
SRAM	System (Mbytes)	4.2					
	Backup (Kbytes)	8					
XSPI	16 bits	1		1[(1)]	0		
	8 bits	1					
Timers	Advanced control	2	1				0
	General purpose	10				7	
	Basic	3				2	1
	Low-power	5	4		2	1	
Communication interfaces	I2S	3				1	0
	SPI	6					5
	I2C	4				3	
	I3C	2					
	USART	5		4		3	2
	UART	5			4	3	
	LPUART	1					
	SAI	2					
	FDCAN	3					
	OTG HS	2					
	UCPD	Yes					
	SDMMC	2		1		0	
	CSI	Yes					
	PSSI	Yes					
	LTDC	Yes					
FMC	FMC_NOR32	Yes		No			
	FMC_NOR16						
	FMC_NORMUX			Yes			No
	FMC SDRAM32			No			
	FMC SDRAM16			Yes		No	
	FMC_NAND16						
Crypto	SAES	Yes					
	CRYPT	Yes					
	PKA	Yes					
	MCE1.4	Yes					
Accelerator	Neural-ART	Yes					

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Table 3. STM32N657xx features and peripheral counts (continued)

Feature / Peripheral		STM32 N657X0	STM32 N657L0	STM32 N657B0	STM32 N657I0	STM32 N657A0	STM32 N657Z0
Multi-function digital filter (MDF)		6 filters					2 filters
Audio digital filter (ADF)		Yes					
Real time clock (RTC)		Yes					
RNG		Yes					
ADC (12 bits)		2					
Digital temperature sensor (DTS)		Yes					
Internal voltage reference buffer		Yes					
Maximum CPU frequency		600 MHz, 800 MHz with overdrive mode					
Operating voltage		1.71 to 3.6 V					
Operating temperature	Ambient	-40 to 125 °C					
Package	Name	VFBGA264	VFBGA223	VFBGA198	VFBGA178	VFBGA169	VFBGA142
	Size	14 x 14 mm	10 x 10 mm	10 x 10 mm	12 x 12 mm	6 x 6 mm	8 x 8 mm
	Pitch	0.8 mm	0.5 mm	0.65 mm	0.8 mm	0.4 mm	0.5 mm
Number of IOs		165	144	126	106	90	75

1. Operates only in 8-bit mode.

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3 Functional overview

3.1 Arm Cortex-M55 core with TrustZone, FPU, NVIC

The device architecture relies on an Arm Cortex-M55 core optimized for execution:

- Main controllers:
  - Cortex-M55 with Arm TrustZone mainline, with two controller ports
    - M-AXI: provides access to the memory and to the peripherals
    - P-AHB: provides access to the peripherals
  - NPU (neural processor unit), including two controller AXI ports
- Memories:
  - AHB and APB peripherals
  - 4.2 Mbytes of SRAM
  - 128-Kbyte data TCM RAM with ECC for critical real-time data, and 64-Kbytes of instruction TCM RAM with ECC for critical real-time routines (TCMs case not extended)
  - 8 Kbytes of backup SRAM (BKPSRAM) active in VBAT mode
  - 2 x 16-Kbyte AHB RAMs
  - Flexible external memory controller (FLEXMEM) with cypher engine supporting up to 32-bit data bus: SRAM, PSRAM, SDRAM, LPSDR SDRAM, NOR/NAND memories
  - XSPI 8-bit configuration with cypher engine
  - XSPI 16-bit configuration with cypher engine (only on STM32N657X0H3Q, STM32N657L0H3Q, and STM32N657B0H3Q)

3.2 SRAM configuration

AHBSRAM1/2, AXISRAM1 to 6, BKPSRAM, FLEXRAM, and VENCRAM, with the following features:

- Error code correction (ECC):
  - Single-error detection and correction with interrupt generation
  - Double-error detection with interrupt generation
  - Status with failing address
- Hardware erase: on reset or dedicated event, the RAM content is automatically erased (written as 0)
- Software erase: the software can trigger an SRAM erase through RAMCFG registers

3.3 AXI cache configuration

The AXI cache (CACHEAXI) is introduced on the AXI interconnect driven by the NPU (neural network) peripheral, to improve the performance of data traffic, by caching the NPU data accessed in the external memories.

When configured as an SRAM, the CACHEAXI can be accessed by the NPU, and also by the Cortex-M55 processor or by any AXI controller peripheral.

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Main features:

- Bus interface
- Optionally, the CACHEAXI can be configured to behave as an SRAM
- Cache access
- Replacement and refill
- System compartments support:
- TrustZone security support
- Maintenance operations
- Performance counters
- Error management

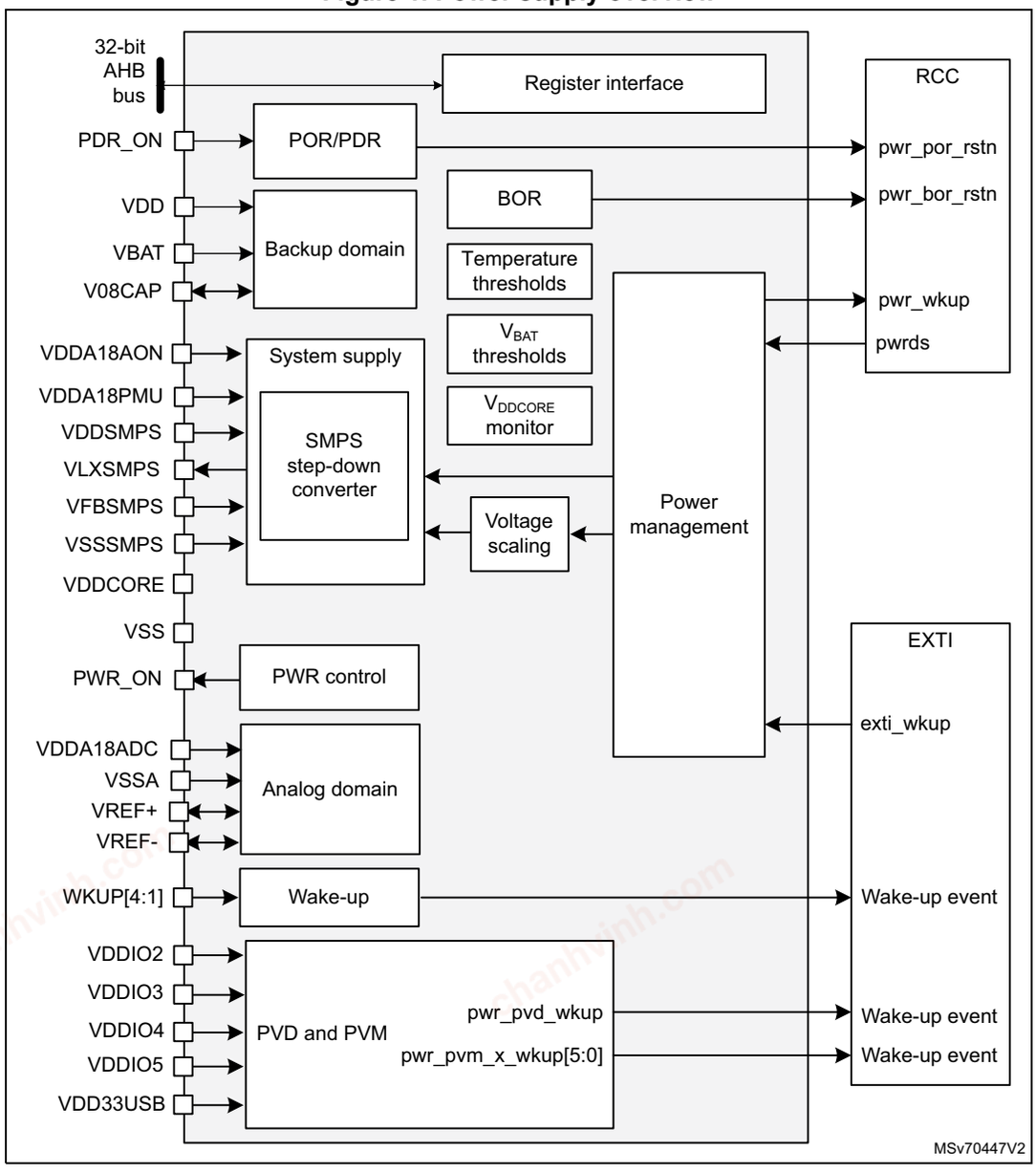
3.4 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domain (V_{CORE} = V_{DDCORE})
  - V_{DD} domain (V_{RET})
  - Backup domain (V_{SW}, V_{BAT})
  - Analog domain ($V_{DDA18ADC}$)
- System supply voltage regulation
  - Switched-mode power supply power-efficient voltage down-converter (SMPS step-down converter)
  - 0.8 V backup regulator (external to the PWR)
- Power supply supervision
  - POR/PDR monitor
  - BOR monitor
  - $V_{DDA18PMU}$ monitor
  - PVD monitor
  - PVM monitor (V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, V_{DDIO5}, $V_{DD33USB}$, $V_{DDA18ADC}$)
  - V_{BAT} thresholds
  - Temperature thresholds
  - V_{DDCORE} monitor
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes

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Figure 1. Power supply overview



3.4.1 Voltage scaling

The V_{CORE} domain is supplied from a single voltage regulator that supports voltage scaling with the following features:

- Run mode voltage scaling
  - VOS low
  - VOS high
- Stop mode voltage scaling
  - SVOS low
  - SVOS high

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3.4.2 Power supply schemes

3.4.3 Core domain

The core domain supply can be provided by the SMPS step-down converter, or by an external supply (VDDCORE). V_{CORE} supplies all the digital circuitries, except for the backup domain, and the retention domain in Standby mode. When a system reset occurs, the SMPS step-down converter is enabled to deliver 0.81 V, hence the system can start up in any supply configuration.

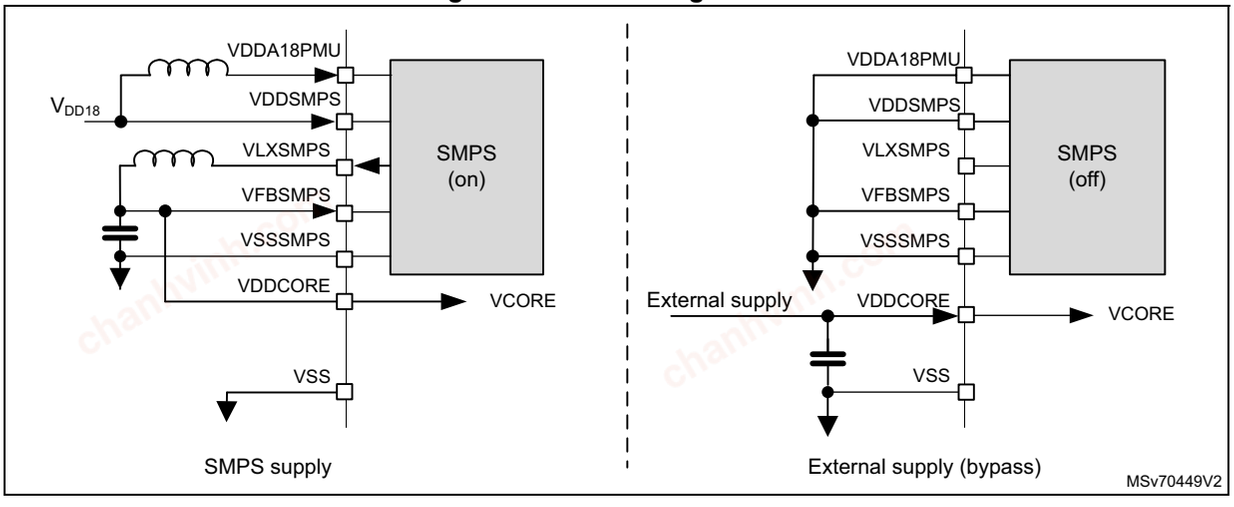
The system startup sequence from power-on in different supply configurations is controlled through power management.

3.4.4 SMPS usage

The devices embed an SMPS to provide the V_{CORE} supply. The SMPS generates this voltage on VLXSMPS, with a total external capacitor of 88 (4x 22) µF (typical). The SMPS requires an external coil of 1 µH (typical).

Two configurations exist, namely SMPS step-down converter supply on and off (bypass mode). In the latter the step-down converter supply is disabled.

Figure 2. SMPS configurations



3.4.5 Backup domain

To retain the content of the backup domain (RTC, backup registers, and backup RAM) when V_{DD} is turned off, the VBAT pin can be connected to an optional voltage supplied from a battery or another source. The switching to V_{BAT} is controlled by the power-down reset (PDR) embedded in the block that monitors the V_{DD} supply.

3.4.6 Analog supply

The analog supply domain is powered by dedicated VDDA18ADC and VSSA pins, which allow the supply to be filtered and shielded from noise on the PCB, thus improving ADC conversion accuracy.

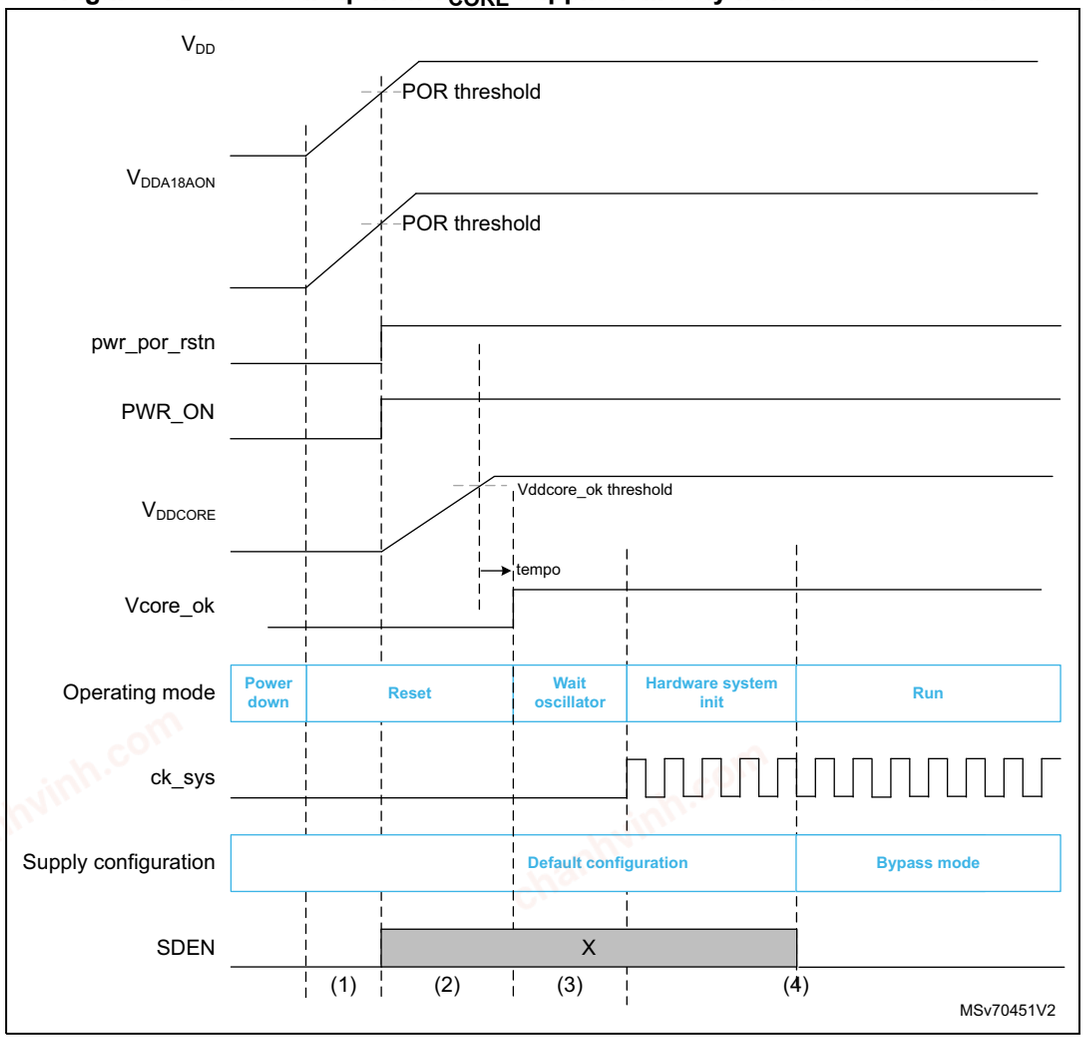
The analog supply voltage input is available on a separate VDDA18ADC pin, and an isolated supply ground connection is provided on VSSA pin.

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3.4.7 System supply startup

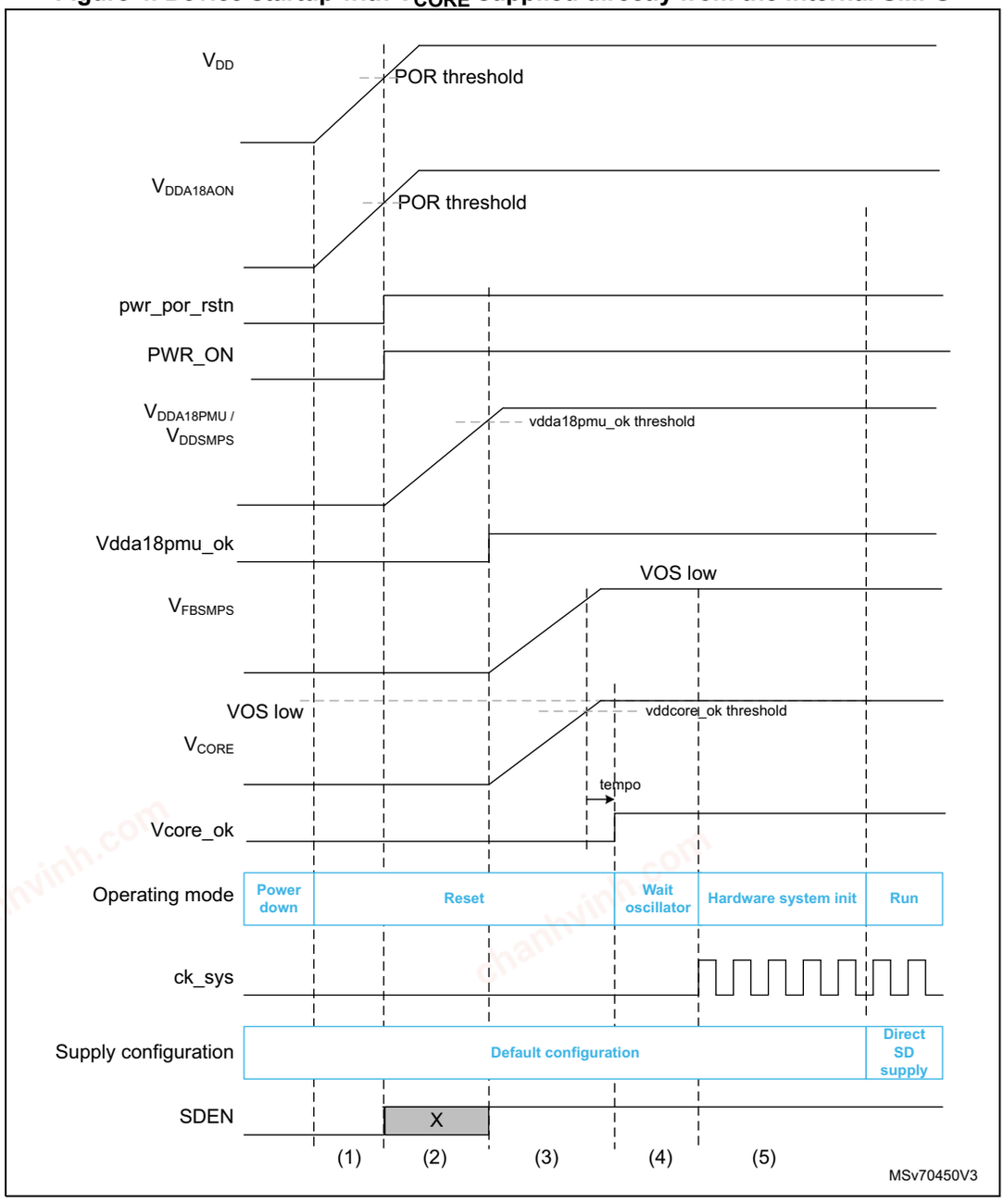
The system startup sequence from power-on has different supply configurations (see *Figure 3* and *Figure 4*), according to the usage of the SMPS.

Figure 3. Device startup with V_{CORE} supplied directly from an external SMPS



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Figure 4. Device startup with V_{CORE} supplied directly from the internal SMPS



3.4.8 Operation modes

Several system operating modes are available to tune the system according to the required performance. The user can select the operating mode that gives the best compromise between power consumption, start-up time, and available wake-up sources.

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Table 4. Operating mode summary

System	Entry	Wake-up	System oscillator	System clock	Peripheral clock	CPU clock	Voltage regulator	PWR_ON
Run	-	-	ON	ON	ON	ON(1)	ON (VOS low/high)	1
Sleep	WFI or return from ISR or WFE(2)	See *Table 5*			ON/OFF(3)			
Stop SVOS high	SVOS + SLEEPDEEP + WFI or return from ISR, WFE, or wake-up source cleared(4)		ON/OFF(5)	OFF		OFF	ON (SVOS high)	
Stop SVOS low	SLEEPDEEP + WFI or return from ISR, WFE, or wake-up source cleared(3)		OFF		OFF		ON (SVOS low)	
Standby	PDDS + SLEEPDEEP + WFI or return from ISR, WFE, or wake-up source cleared(3)	WKUP pins rising or falling edge, RTC alarm (A or B), RTC wake-up event, RTC tamper events, RTC timestamp event, external reset in NRST pin, IWDG reset	OFF	OFF	OFF	OFF	OFF	0(6)

1. The clock is gated in the core in Sleep mode.
2. WFI = wait for interrupt, ISR = interrupt service routine, WFE = wait for event.
3. The CPU subsystem peripherals with a PERxLPEN bit operate accordingly.
4. When the CPU is in Stop mode, the last EXTI wake-up source must be cleared by software.
5. When HSI or MSI is used, the state is controlled by HSISTOPEN and MSISTOPEN, otherwise the system oscillator is off.
6. A guaranteed minimum PWR_ON pulse low time can be defined by POPL bits in PWR_CR1.

Table 5. Functionalities depending on system operating mode

Peripheral(1)	Run mode	Stop mode SVOS high		Stop mode SVOS low		Standby mode		V_{BAT} mode
		-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
CPU	Y	R	-	R	-	-	-	-
NPU	O	O	-	R	-	-	-	-
Debug	O	O	O	R	-	-	-	-
ROM	Y	R	-	R	-	-	-	-

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Table 5. Functionalities depending on system operating mode (continued)

Peripheral[1]	Run mode	Stop mode SVOS high		Stop mode SVOS low		Standby mode		V_{BAT} mode
		-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
RAMCFG	O	R	-	R	-	-	-	-
I-TCM	O	R	-	R	-	R	-	-
I-TCM FLEXMEM	O	R	-	R	-	R	-	-
D-TCM	O	R	-	R	-	R	-	-
AXISRAM1	O	R	-	R	-	R[2]	-	-
AXISRAMx (x = 2, 3, 4)	O	O	-	R	-	-	-	-
I-TCM FLEXMEM extension	O	O	-	R	-	R[3]	-	-
D-TCM FLEXMEM extension	O	O	-	R	-	-	-	-
CACHEAXI1	O	O	-	R	-	-	-	-
VENCRAM	O	O	-	R	-	-	-	-
GPU RAM	O	O	-	R	-	-	-	-
BKPSRAM	O	R	-	R	-	O	-	O
AHBSRAMx (x = 1, 2)	O	O	-	R	-	-	-	-
XSPIx (x = 1, 2, 3)	O	R	-	R	-	-	-	-
XSPIM	O	R	-	R	-	-	-	-
MCEx (x = 1, 2, 3, 4)	O	R	-	R	-	-	-	-
FMC	O	R	-	R	-	-	-	-
Backup registers	Y	R	-	R	-	R	-	R
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	-
Programmable voltage detector (PVD)	O	O	O	O	O	-	-	-
Peripheral voltage monitor (PVM)	O	O	O	O	O	-	-	-
VBATH/VBATL monitoring	O	O	O	O	O	O	O	O
TEMPH/TEMPL monitoring	O	O	O	O	O	O	O	O
GPDMA1	O	R	-	R	-	-	-	-
HPDMA1	O	R	-	R	-	-	-	-
High speed internal (HSI)	O	O	-	-	-	-	-	-
High speed external (HSE)	O	-	-	-	-	-	-	-
Low speed internal (LSI)	O	O	-	O	-	O	-	-
Low speed external (LSE)	O	O	-	O	-	O	-	O
Multi speed internal (MSI)	O	O	-	-	-	-	-	-
HSE CSS (clock security system)	O	-	-	-	-	-	-	-
LSE CSS	O	O	O	O	O	O	O	O

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Table 5. Functionalities depending on system operating mode (continued)

Peripheral[1]	Run mode	Stop mode SVOS high		Stop mode SVOS low		Standby mode		V_{BAT} mode
		-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
RTC/auto wake-up	O	O	O	O	O	O	O	O
TAMP, number of tamper pins	7	7	O	4	O	4	O	4
OTG1 HS	O	R	O	R	-	-	-	-
OTG2 HS	O	R	O	R	-	-	-	-
UCPD1	O	R	O	R	-	-	-	-
SDMMCx (x = 1, 2)	O	R	-	R	-	-	-	-
FDCAN	O	R	-	R	-	-	-	-
MDIOS	O	R	O	R	-	-	-	-
ETH1	O	R	O	R	-	-	-	-
LPUART1	O	O	O	R	-	-	-	-
U(S)ARTx (x = 1 to 10)	O	O	O	R	-	-	-	-
I2Cx (x = 1, 2, 3, 4)	O	O	O	R	-	-	-	-
I3Cx (x = 1, 2)	O	O	O	R	-	-	-	-
SPIx (x = 1 to 6)	O	O	O	R	-	-	-	-
SAIx (x = 1, 2)	O	R	-	R	-	-	-	-
ADF1	O	O	O	R	-	-	-	-
MDF1	O	O	O	R	-	-	-	-
DCMI	O	R	-	R	-	-	-	-
PSSI	O	R	-	R	-	-	-	-
DCMIPP	O	R	-	R	-	-	-	-
GPU	O	R	-	R	-	-	-	-
DMA2D	O	R	-	R	-	-	-	-
GFXTIM	O	R	-	R	-	-	-	-
GFXMMU	O	R	-	R	-	-	-	-
JPEG	O	R	-	R	-	-	-	-
VENC	O	R	-	R	-	-	-	-
LTDC	O	R	-	R	-	-	-	-
ADCx (x = 1, 2)	O	R	-	R	-	-	-	-
VREFBUF	O	R	-	R	-	-	-	-
DTS	O	R	O	R	-	-	-	-
TIMx (x = 1 to 18)	O	R	-	R	-	-	-	-
LPTIMx (x = 1 to 5)	O	O	O	R	-	-	-	-

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Table 5. Functionalities depending on system operating mode (continued)

Peripheral[1]	Run mode	Stop mode SVOS high		Stop mode SVOS low		Standby mode		V_{BAT} mode
		-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	
IWDG	O	O	O	O	O	O	O	-
WWDG	O	R	-	R	-	-	-	-
RNG	O	R	-	R	-	-	-	-
SAES	O	R	-	R	-	-	-	-
CRYP	O	R	-	R	-	-	-	-
HASH	O	R	-	R	-	-	-	-
CRC	O	R	-	R	-	-	-	-
GPIOs	O	O	O	O	O 4 pins	O	O 4 pins	-

1. Legend: Y = Yes (enable). O = Optional (disable by default. Can be enabled by software). R = data/state retained. -= not available.
2. Only the first 80 Kbytes can optionally be retained (see the dedicated section of RM0486 for details).
3. Only the first 64 Kbytes can optionally be retained (see the dedicated section of RM0486 for details).

3.4.9 Low-power modes

Several low-power modes are available to save power when the CPU does not need to execute code (when waiting for an external event). The user must select the mode that gives the best compromise between low-power consumption, short start-up time, and available wake-up sources:

- Low-power modes
  - Sleep (CPU clock stopped and still in Run mode)
  - Stop (system clock stopped)
  - Standby (system powered down)
- Reset mode
  - To improve the consumption under reset, the I/O state under and after reset is “analog state” (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.5 Convolution neural network accelerator (NPU)

The neural processing unit (NPU) core is the design time parametric and runtime reconfigurable neural network inference engine. It can accelerate a wide range of neural network architectures in hardware.

The NPU is considered as an accelerator subsystem with several specialized hardware accelerators supporting various inference kernels connected via a reconfigurable data flow fabric. The specific instantiation can vary from a low-end version for low-cost microcontrollers designed with two convolution accelerators (CA).

The NPU subsystem connects to the host system and the shared system memory.

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The host configures the NPU subsystem through an AHB/AXI lite target port, connected to one of the ports of the system bus matrix/interconnect. The two controller ports of NPU are 64-bit wide controller AXI-4 interfaces that connect to the system bus matrix/Interconnect. The system memory is shared between the host subsystem and the NPU subsystem.

The used memory is configurable by software, it depends upon the complexity and target performance of the selected neural network workload.

3.6 Boot modes

The BootROM is the first code executed after any system reset. The boot mode is determined by BOOT0 and BOOT1 pins, one OTP word (flash source selection), and one TAMP backup register.

- BOOT0 is a dedicated pin latched upon reset release
- BOOT1 is a non-dedicated boot pin. The BOOT1 value comes from BOOT1 pin (default pin), or any other pin defined by system

Depending the configuration of these signals, there are two boot modes, namely serial boot, and external flash boot.

3.6.1 External flash boot

The firmware is loaded from an external flash memory. The BootROM code supports following types of boot memory devices:

- XSPI serial NOR (in SPI mode, single)
- XSPI HyperFlash™ (8-bit)
- e.MMC™ SDMMC1 or e.MMC™ SDMMC2 (up to JEDEC v5.1)
- SD-Card SDMMC1 (up to SD standard v6.0)

3.6.2 Serial boot

The image is loaded from a serial interface. The BootROM code supports following types of serial boot interfaces:

- USB boot: USB 2.0 OTG HS
- UART boot

3.6.3 Development boot

If BOOT1 is selected, the BootROM code finishes in an endless loop after having reopened debug in a secure way.

This boot mode is available only when the device is in development.

Secure installation

The ROM code is the root-of-trust of secure firmware installation.

3.7 General-purpose inputs/outputs (GPIOs)

Each general-purpose I/O port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, and GPIOx_PUPDR), two 32-bit data registers

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(GPIOx_IDR and GPIOx_ODR), a 16-bit reset register (GPIOx_BRR), and a 32-bit set/reset register (GPIOx_BSRR).

In addition, all GPIOs have a 32-bit locking register (GPIOx_LCKR), two couples of 32-bit advanced configuration registers (GPIOx_DELAYRL/H, GPIOx_ADVCFGRL/H), and two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL).

Access to each general-purpose I/O configuration bit can be restricted to secure-only and/or privileged-only.

The main features are:

- Multiple choice of configurations per I/O port:
  - Input configuration in floating, pull-up/down, or analog state
  - Analog configuration (output buffer and Schmitt trigger input disabled)
  - Output configuration, or alternate function configuration, in push-pull or open drain state, with pull-up or pull-down activated
- Data present on the I/O pin sampled to the input data register GPIOx_IDR (input configuration) or to the peripheral (alternate function configuration)
- Output buffer on the I/O pin driven by the output data register GPIOx_ODR (output configuration) or by the peripheral (alternate function configuration)
- I/O data output atomic read/modify through GPIOx_ BSRR and GPIOx_BRR
- Speed selection for each I/O (GPIOx_OSPEEDR)
- Lock mechanism (GPIOx_LCKR) to selectively freeze the I/O port configurations
- Highly-flexible pin multiplexing, enabling the use of I/O pins as GPIOs, or as one of several possible peripheral functions
- Programmable delay to the input or the output path (GPIOx_DELAYR)
- Double edge selection, clock inversion, and optional retime (GPIOx_ADVCFGR)
- Possibility to restrict each I/O control to secure-only and/or privileged-only

3.8 System configuration controller (SYSCFG)

The devices feature a set of configuration registers. The SYSCFG manages:

- Cortex-M55 internal settings (such as TCM, CACHE, or vectors)
- Iterconnect, security, and memory settings
- I/O compensation cells

3.9 General purpose direct memory access controller (GPDMA)

The GPDMA controller is a bus controller and system peripheral, used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

The GPDMA main features are:

- Dual bidirectional AHB controller
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral

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  - Memory-to-memory
  - Peripheral-to-peripheral
- Transfer arbitration based on a 4-grade programmed priority at channel level:
  - One high priority traffic class, for time-sensitive channels (queue 3)
  - Three low priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)
- Per channel event generation, on any of the following events: transfer complete, half transfer complete, data transfer error, user setting error, link transfer error, completed suspension, and trigger overrun
- Per channel interrupt generation, with separately programmed interrupt enable per event
- 16 concurrent GPDMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intra-channel GPDMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode.
  - Intra-channel and inter-channel GPDMA transfers chaining via programmable GPDMA input triggers connection to GPDMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive burst transfers
  - 2D source and destination addressing: programmable signed address offsets between successive burst transfers (non-contiguous addressing within a block, combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level, for a reduced set of channels
  - Support for scatter-gather (multi-buffer transfers), data interleaving and deinterleaving via 2D addressing
  - Programmable GPDMA request and trigger selection
  - Programmable GPDMA half transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the GPDMA linked-list control registers
  - Channel abort and restart
- Debug:
  - Channel suspend and resume support
  - Channel status reporting, including FIFO level, and event flags
- TrustZone support:
  - Support for secure and non-secure GPDMA transfers, independently at a first channel level, and independently at a source/destination and link sublevels.

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  - Secure and non-secure interrupts reporting, resulting from any of the respectively secure and non-secure channels.
  - TrustZone-aware AHB target port, protecting any GPDMA secure resource (register, register field) from a non-secure access.
- Privileged/unprivileged support:
  - Support for privileged and unprivileged GPDMA transfers, independently at a channel level
  - Privileged-aware AHB target port

Table 6. GPDMA1 channel implementation

Channel x	Hardware parameters		Features	Comment
	dma_fifo_size[x]	dma_addressing[x]		
0 to 11	2	0	– 8 bytes, 2 words FIFO – Fixed/contiguously incremented addressing	Typically allocated for GPDMA transfers between an APB/AHB peripheral and SRAM.
12 to 15	4	1	– 32 bytes, 8 words FIFO – 2D addressing	Can be used for GPDMA transfers, between a demanding AHB peripheral and SRAM, or for transfers from/to external memories.

3.10 High performance direct memory access controller (HPDMA)

The HPDMA is used to perform programmable data transfers between memory-mapped peripherals, and/or memories via linked-lists, upon the control of an off-loaded CPU.

Main features:

- Single bidirectional AXI controller and single bidirectional AHB controller
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Transfer arbitration based on a 4-grade programmed priority at channel level:
  - One high priority traffic class, for time-sensitive channels (queue 3)
  - Three low priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)
- Per channel event generation, on any of the following events:
  - Transfer complete, half transfer complete
  - Data transfer error, user setting error, link transfer error
  - Completed suspension
  - Trigger overrun
- Per channel interrupt generation, with separately programmed interrupt enable per event
- 16 concurrent HPDMA channels:
  - Per channel FIFO for queuing source and destination transfers

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  - Intra-channel HPDMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode.
  - Intra-channel and inter-channel HPDMA transfers chaining via programmable HPDMA input triggers connection to HPDMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing, or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing either fixed or contiguously incremented addressing, programmed at block level, between successive burst transfers
  - 2D source and destination addressing programmable signed address offsets between successive burst transfers (non-contiguous addressing within a block, combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level, for a reduced set of channels
  - Support for scatter-gather (multi-buffer transfers), data interleaving and de-interleaving via 2D addressing
  - Selection of programmable HPDMA request and trigger
  - Generation of programmable HPDMA half-transfer and transfer-complete event
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the HPDMA linked-list control registers
  - Channel abort and restart
- Debug:
  - Channel suspend and resume support
  - Channel status reporting, including FIFO level, and event flags
- TrustZone support:
  - Support for secure and non-secure HPDMA transfers, independently at a first channel level, and independently at a source/destination and link sublevels
  - Secure and non-secure interrupts reporting, resulting from any of the respectively secure and non-secure channels
  - TrustZone-aware AHB target port, protecting any HPDMA secure resource (register, bitfield) from a non-secure access
- Privileged/unprivileged support:
  - Support for privileged and unprivileged HPDMA transfers, independently at channel level
  - Privileged-aware AHB target port
- Channel isolation support:
  - Support for compartmented DMA transfers, independently at channel level, via compartment IDs (named CIDs)
  - CID-aware interrupts reporting
  - CID-aware AHB target port, with integrated semaphores for a concurrent control from any of the CPUs

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Table 7. Implementation of HPDMA1 channels

Channel x	Hardware parameters		Features
	dma_fifo_size[x]	dma_addressing[x]	
x = 0 to 11	3	0	Channel x (x = 0 to 11) is implemented with: – a FIFO of 16 bytes, 4 words, 2 double-words – fixed/contiguously incremented addressing These channels can be used for HPDMA transfers between an APB or AHB peripheral, an AHB/AXI SRAM, or CPU TCM.
x = 12 to 15	5	1	Channel x (x = 12 to 15) is implemented with: – a FIFO of 64 bytes, 8 double-words – 2D addressing These channels can be also used for HPDMA transfers, including AXI external memories.

Table 8. HPDMA1 in low-power modes

Feature	Low-power modes
Wake-up	HPDMA1 in Sleep mode

3.11 Chrom-ART Accelerator controller (DMA2D)

The Chrom-ART Accelerator (DMA2D) is a specialized DMA dedicated to image manipulation. It can perform the following operations:

- Fill a part or the whole of a destination image with a specific color
- Copy a part or the whole of a source image into a part or the whole of a destination image
- Copy a part or the whole of a source image into a part or the whole of a destination image with a pixel format conversion
- Blend a part and/or two complete source images with different pixel format and copy the result into a part or the whole of a destination image with a different color format

All the classical color coding schemes are supported, from 4- up to 32-bit per pixel with indexed or direct color mode, including block based YCbCr to handle JPEG decoder output.

The DMA2D has its own dedicated memories for CLUTs (color look-up tables).

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The main DMA2D features are:

- Single AXI controller bus architecture
- AHB target programming interface supporting 8-,16-,32-bit accesses (except for CLUT accesses which are 32-bit)
- User-programmable working area size
- User-programmable offset for sources and destination areas expressed in pixels or bytes
- User-programmable sources and destination addresses on the whole memory space
- Up to two sources with blending operation
- Alpha value that can be modified (source value, fixed value, or modulated value)
- User programmable source and destination color format
- Up to 12 color formats supported from 4-bit up to 32-bit per pixel with indirect or direct color coding
- Block based (8x8) YCbCr support with 4:4:4, 4:2:2 and 4:2:0 chroma sub-sampling factors
- Two internal memories for CLUT storage in indirect color mode
- Automatic CLUT loading or CLUT programming via the CPU
- User programmable CLUT size
- Internal timer to control AXI bandwidth
- Operating modes:
  - Register-to-memory
  - Memory-to-memory
  - Memory-to-memory with pixel format conversion
  - Memory-to-memory with pixel format conversion and blending
  - Memory-to memory with pixel format conversion, blending, and fixed color foreground
  - Memory-to memory with pixel format conversion, blending, and fixed color background
- Area filling with a fixed color
- Copy from an area to another
- Copy with pixel format conversion between source and destination images
- Copy from two sources with independent color format and blending
- Output buffer byte swapping to support refresh of displays through parallel interface
- Abort and suspend of DMA2D operations
- Watermark interrupt on a user programmable destination line
- Interrupt generation on bus error or access conflict
- Interrupt generation on process completion

3.12 Chrom-GRC (GFXMMU)

The Chrom-GRC (GFXMMU) is a graphical oriented memory management unit aimed to optimize memory usage according to the display shape. Main features are:

- Fully programmable display shape to physically store only the visible pixel

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- Up to four virtual buffers
- Each virtual buffer has 3072 or 4096 bytes per line and 1024 lines
- Each virtual buffer can be physically mapped to any system memory
- Packing and unpacking operation to store 32-bit pixel data into 24-bit packed
- Interrupt in case of buffer overflow (one per buffer)
- Interrupt in case of memory transfer error

3.13 Graphic timer (GFXTIM)

The graphic timer (GFXTIM) is a graphic oriented timer for smart management of graphical events for frame or line counting. Its main features are:

- Integrated frame and line clock generation
- One absolute frame counter with one compare channel
- Two auto-reload relative frame counters
- One line timer with two compare channels
- External tearing-effect line management and synchronization
- Four programmable event generators with external trigger generation
- One watchdog counter

3.14 Interrupts and events

3.14.1 Nested vectored interrupt controller (NVIC)

The NVIC includes the following features:

- Up to 196 maskable interrupt channels (not including the Cortex-M55 interrupt lines)
- 16 programmable priority levels (using four bits of interrupt priority)
- Low latency exception and interrupt handling
- Power management control
- Implementation of system control registers

The NVIC and the processor core interface are closely coupled, which enables low latency interrupt processing and efficient processing of late arriving interrupts. All interrupts, including the core exceptions, are managed by the NVIC.

3.14.2 Extended interrupt/event controller (EXTI)

The EXTI manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control, and generates interrupt requests to the CPU NVIC and events to the CPU event input. For the CPU an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop modes, and the CPU to be woken up from CStop and CStandby modes.

The interrupt request and event request generation can also be used in Run modes.

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The EXTI main features are the following:

- 73 input events supported
- Most event inputs allow to wake up the system, some can be used only to generate a CPU wake-up
- Events without an associated wake-up flag in the peripheral have a flag in the EXTI, and generate a combined secure/non-secure interrupt to the CPUs from the EXTI
- Events can be used to generate a CPU wake-up event
- The asynchronous event inputs are classified in two groups:
  - Configurable events (signals from I/Os or peripherals able to generate a pulse), with the following features:
    - Selectable active trigger edge
    - Interrupt pending status register bits independent for the rising and falling edge
    - Individual interrupt and event generation mask, used to condition the CPU wake-up, interrupt, and event generation
    - Individual interrupt lines per CPU
    - Software trigger possibility
  - Direct events (interrupt and wake-up sources from peripherals with an associated flag, which must be cleared in the peripheral), with the following features:
    - Fixed rising edge active trigger
    - No interrupt pending status register bit in the EXTI (the interrupt pending status flag is provided by the peripheral generating the event)
    - No interrupt pending status register bit in the EXTI (the interrupt pending status flag is provided by the peripheral generating the event)
    - No software trigger possibility
- Secure events
  - The access to control and configuration bits of secure input events can be made secure and or privileged
- EXTI I/O port selection

3.15 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from 8-, 16- or 32-bit data word and a generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

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Main features are:

- Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7
  ($x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$)
- Alternatively, uses fully programmable polynomial with programmable size (7, 8, 16, 32 bits)
- Handles 8-,16-, 32-bit data size
- Programmable CRC initial value
- Single input/output 32-bit data register
- • Input buffer to avoid bus stall during calculation
- CRC computation done in four AHB clock cycles (HCLK) for the 32-bit data size
- General-purpose 8-bit register (can be used for temporary storage)
- Reversibility options on I/O data
- Accessed through AHB target peripheral by 32-bit words only, with the exception of CRC_DR register, which can be accessed by words, right-aligned half-words, and right-aligned bytes

3.16 Flexible memory controller (FMC)

The FMC includes three memory controllers, namely the NOR/PSRAM, the NAND, and the synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller. Its main features are:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (four memory subregions)
  - Ferroelectric RAM (FRAM, FeRAM)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- Burst mode support for faster access to synchronous devices such as NOR flash memory, PSRAM and SDRAM)
- Programmable continuous clock output for asynchronous and synchronous accesses
- 8-,16- or 32-bit wide data bus
- Independent chip-select control for each memory region
- Independent configuration for each memory region
- Write enable and byte lane select outputs for use with PSRAM, SRAM and SDRAM devices
- External asynchronous wait control

At startup the FMC pins must be configured by the user application. The FMC input/output pins not used by the application can be used for other purposes.

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3.17 XSPI interface

3.17.1 Extended-SPI interface (XSPI)

The XSPI supports most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, HyperRAM™ and HyperFlash™ memories, with the following functional modes:

- Indirect: all the operations are performed using the XSPI registers to preset commands, addresses, data and transfer parameters.
- Automatic status-polling (available only in regular command protocol): the external memory status register is periodically read and an interrupt can be generated in case of flag setting.
- Memory-mapped mode: the external memory is memory mapped and it is seen by the system as if it was an internal memory, supporting both read and write operations.

The XSPI supports the following protocols with associated frame formats:

- regular-command frame format with the command, address, alternate byte, dummy cycles and data phase
- HyperBus™ frame format

Main features:

- Functional modes: indirect, automatic status-polling, and memory-mapped
- Read and write support in memory-mapped mode
- Support for single, dual, quad, and octal communication
- Dual-memory configuration, where 8 bits can be sent/received simultaneously by accessing two quad or octal memories in parallel
- XSPI mode accessing a single 16-bit memory
- SDR (single-data rate) and DTR (double-transfer rate) support
- Data strobe support
- Fully programmable opcode
- Fully programmable frame format
- Support wrapped-type access to memory in read direction
- HyperBus support
- Integrated FIFO for reception and transmission
- 8-, 16-, and 32-bit data accesses allowed
- DMA protocol support
- DMA channel for indirect mode operations
- Interrupt generation on FIFO threshold, timeout, operation complete, and access error
- AXI acceptance 2: acceptance is offered based on a read transaction followed by a second write or read request (acknowledged on the bus), while the first one is being processed
- Dual chip select support (NCS1 and NCS2)
- Extended external memory support: if two same size external memories (extmem1 and extmem2) are connected to the same I/O port, contiguously in the memory map and driven by a single XSPI. This XSPI automatically switches CS to extmem1 or extmem2, according to the address on interconnect side.

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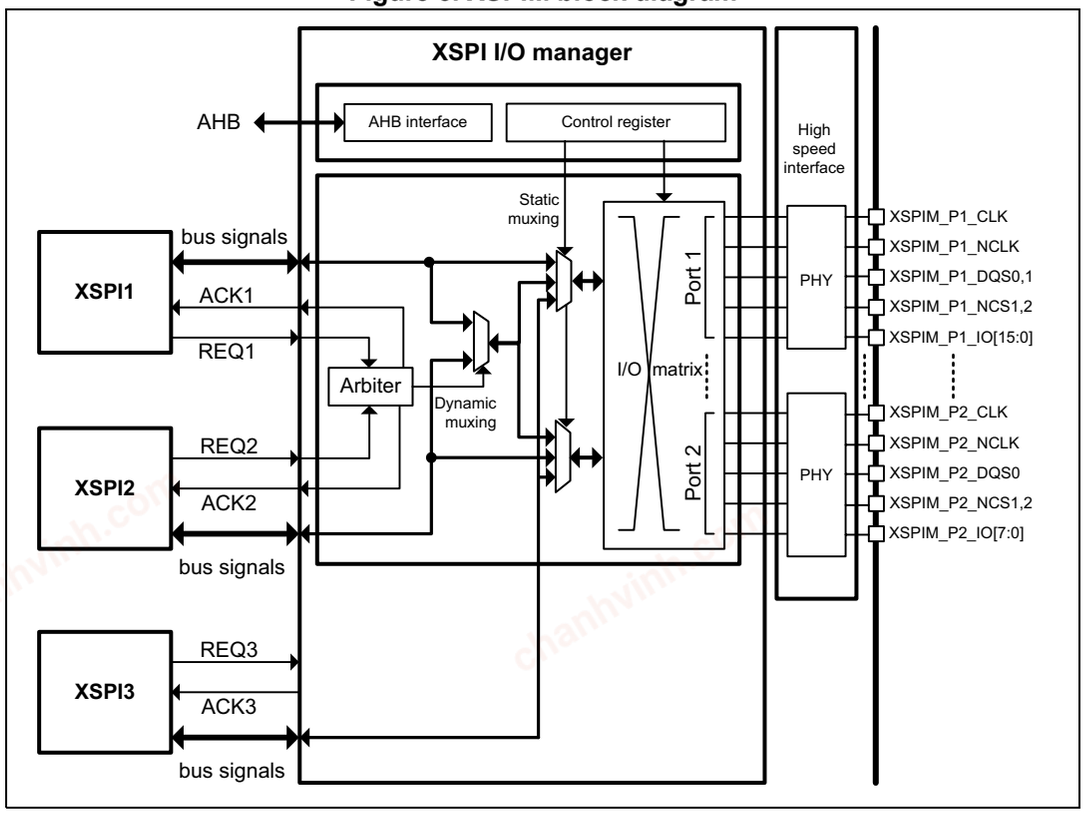
3.17.2 XSPI I/O manager (XSPIM)

The XSPI I/O manager is a low level interface, enabling efficient XSPI pin assignment with a full I/O matrix (before alternate function map), and multiplex of single/dual/quad/octal/16-bit SPI interfaces over the same bus.

Main features:

- Supports up to two single/dual/quad/octal/16-bit SPI interfaces
- Supports up to two ports for pin assignment
- Supports high-speed interfaces
- Manages up to three XSPIs

Figure 5. XSPIM block diagram



3.18 Secure digital input/output MultiMediaCard interface (SDMMC)

The SD/SDIO, embedded MultiMediaCard (eMMC™) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and eMMC devices.

The MultiMediaCard system specifications are available through the MultiMediaCard Association website at www.jedec.org, published by the MMCA technical committee. The SD memory card and SD I/O card system specifications are available through the SD Association website at www.sdcard.org.

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Main SDMMC features:

- Compliance with Embedded MultiMediaCard System Specification Version 5.1. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit. HS200 SDMMC_CK speed limited to maximum allowed I/O speed, HS400 is not supported.
- Full compatibility with previous versions of MultiMediaCards (backward compatibility).
- Full compliance with SD memory card specification version 6.0 (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Full compliance with SDIO card specification version 4.0. Card support for 1-bit (default) and 4-bit databus modes. SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported.
- Data transfer up to 208 Mbyte/s for the 8-bit mode, depending upon maximum allowed I/O speed.
- Data and command output enable signals to control external bidirectional drivers.
- IDMA linked list support.

The MultiMediaCard/SD bus connects cards to the host.

The current version of the SDMMC supports only one SD/SDIO/eMMC card at any one time, and a stack of eMMCs.

3.19 SDMMC delay block (DLYB)

This block is used to generate two output clocks dephased from two input clocks. The phase of each output clock must be programmed by the user application. The output clocks are then used to clock the data transmitted/received by another peripheral such as an SDMMC.

The delay block has the following features:

- Frequency for Lock mode in the 50 to 208 MHz range
- 32 phases (delay taps)
- Bypass mode for operation below 50 MHz

3.20 Analog-to-digital converters (ADC)

The devices embed two ADCs (ADC1, ADC2) tightly coupled, which can operate in Dual mode (ADC1 is controller).

Each ADC consists of one 12-bit successive approximation analog-to-digital converter, and has up to 20 multiplexed channels. The conversions can be performed in Single, Continuous, Scan, or Discontinuous mode. The result is stored in a left- or right-aligned (default configuration) 32-bit data register. The ADCs are mapped on the AHB bus for fast data handling.

The analog watchdog features allow the application to detect if the input voltage goes outside the user-defined high or low thresholds.

A built-in hardware oversampler improves analog performance, while off-loading the related computational burden from the CPU.

An efficient low-power mode is implemented for very low consumption at low frequencies.

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The ADCs main features are:

  - 12-, 10-, 8- or 6-bit configurable resolution
  - Conversion time independent from the AHB bus clock frequency
  - Faster conversion time by lowering resolution
  - Management of single-ended or differential inputs (programmable per channels)
  - AHB target bus interface to allow fast data handling
  - Offset calibration support
  - Channel-wise programmable sampling time
  - Flexible sampling time control
  - Up to four injected channels (analog inputs assignment to regular or injected channels is fully configurable)
  - Data alignment with in-built data coherency
  - Data can be managed by DMA for regular channel conversions
  - Data can be routed to MDF for post processing
  - Four dedicated data registers for the injected channels
- Low-power features
  - Speed adaptive low-power mode to reduce ADC consumption when operating at low frequency
  - Allows slow bus frequency application while keeping optimum ADC performance
  - Provides automatic control to avoid ADC overrun in low AHB bus clock frequency application (Auto-delay mode)
- Oversampler
  - 32-bit data register
  - Ratio adjustable from 2 to 1024
  - Programmable data right shift
- Data preconditioning
  - Gain compensation
  - Offset compensation
- Analog input channels
  - External analog inputs (per ADC): up to 17 GPIO pads
  - One channel for the internal reference voltage (VREFINT)
  - One channel for monitoring the external VBAT power supply pin
  - One channel connected to the analog positive reference voltage VREF+
  - One channel for monitoring V_{DDCORE} internal voltage
- Start-of-conversion can be initiated:
  - By software for both regular and injected conversions
  - By hardware triggers with configurable polarity (internal timers events or GPIO input events) for both regular and injected conversions
- Conversion modes
  - Each ADC can convert a single channel or can scan a sequence of channels
  - Single mode converts selected inputs once per trigger
  - Continuous mode converts selected inputs continuously
  - Discontinuous mode

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- Interrupt generation at ADC ready, the end of sampling, the end of conversion (regular or injected), end of sequence conversion (regular or injected), analog watchdog 1, 2 or three or overrun events
- Three analog watchdogs per ADC
- Input range: $V_{SSA} \leq V_{IN} \leq V_{REF+}$

3.21 Digital temperature sensor (DTS)

The DTS is a high precision low-power junction temperature sensor (TS), composed of a configurable controller plus two embedded temperature sensors (TS0 and TS1). The controller features a generic interface that enables the DTS to be accessed in read and write modes, through the APB bus.

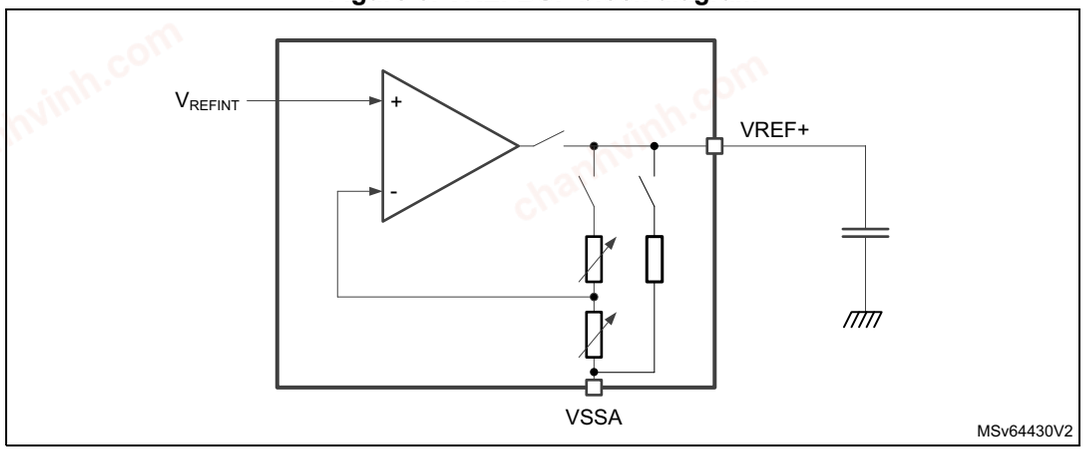
The main features are:

- For each temperature sensor, two programmable (rise or fall) hardware alarms incorporating hysteresis and status registers recording the minimum and maximum data values received
- A power-up timer with IRQ to support manual operation

3.22 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer supporting 1.21 and 1.5 V, which can be used as reference for ADCs and for external components through the VREF+ pin.

Figure 6. VREFBUF block diagram



3.23 Multi-function digital filter (MDF)

The multi-function digital filter (MDF) is a high performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators, mainly for audio capture signals, motor control, and metering.

The MDF features six digital serial interfaces (SITFx) and digital filters (DFLTx) with flexible digital processing options to offer up to 24-bit final resolution.

The DFLTx of the MDF also include the filters of the audio digital filter (ADF).

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The MDF can receive, via its serial interfaces, streams coming from various digital sensors. It supports SPI, Manchester coded 1-wire, and PDM interface standards.

Main features:

- AHB interface
- Six serial digital inputs
  - configurable SPI interface to connect digital sensors
  - configurable Manchester coded interface support
  - compatible with PDM interface to support digital microphones
- Two common clocks input/output for ΣΔ modulators
- Flexible matrix (BSMX) for connection between filters and digital inputs
- Two inputs to connect the internal ADCs
- Six flexible digital filter paths, including:
  - A configurable CIC filter:
    - Can be split into two CIC filters: high-resolution filter and out-off limit detector
    - Can be configured in Sinc4 and Sinc5 filters
    - Adjustable decimation ratio
  - A reshape filter to improve the out-off band rejection and in-band ripple
  - A high-pass filter to cancel the DC offset
  - An offset error cancellation
  - Gain control
  - Saturation blocks
  - An out-off limit detector
- Short-circuit detector
- Clock absence detector
- 16- or 24-bit signed output data resolution
- Continuous or single conversion
- Possibility to delay independently each bitstream
- Various trigger possibilities
- Break generation on out-of limit or short-circuit detector events
- Autonomous functionality in Stop modes
- DMA can be used to read the conversion data
- Interrupts services

3.24 Audio digital filter (ADF)

The audio digital filter (ADF) is a high performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators, mainly for audio capture signals and metering.

The ADF features one digital serial interface (SITF0) and one digital filter (DFLT0) with flexible digital processing options in order to offer up to 24-bit final resolution.

The ADF serial interface supports SPI, Manchester coded 1-wire, and PDM interface standards.

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Main features:

- AHB interface
- One serial digital input:
  - Configurable SPI interface to connect various digital sensors
  - Configurable Manchester coded interface support
  - Compatible with PDM interface to support digital microphones
- Two common clocks input/output for ΣΔ modulators
- One flexible digital filter path including:
  - An MCIC filter configurable in Sinc4 or Sinc5 filter with adjustable decimation ratio
  - A reshape filter to improve the out-off band rejection and in-band ripple
  - A high-pass filter to cancel the DC offset
  - Gain control
  - Saturation blocks
- • Clock absence detector
- • Sound activity detector
- • 24-bit signed output data resolution
- • Continuous or single conversion
- • Possibility to delay the selected bitstream
- • One trigger input
- • Autonomous functionality in Stop modes
- • DMA can be used to read the conversion data
- • Interrupts services

3.25 Camera subsystem

The camera subsystem is built around a double path:

- a low resolution path, with the DCMI and a low-frequency parallel interface, supporting sensors up to 24 Mpixel/s
- a high resolution path, with the DCMIPP and a high frequency parallel interface or serial CSI-2 interface (RGB or rawBayer), targeting sensors up to 5 Mpixels at 30 fps

For the connection of a camera sensor, it is recommended to use the DCMIPP. The DCMI is recommended only in two noticeable cases:

- to get backward compatibility with former platforms that embed also the DCMI
- to input the pixels from a second camera sensor

Note: The DCMIPP inputs pixels from one sensor via the CSI-2 interface, while the DCMI gets pixels from the second sensor via the parallel interface.

The DCMI path offers the following summarized maximum features:

- Target sensor: 24 Mpixel/s 16 bpp (limited by the DMA)
- Parallel input: 80 MHz on 14-bit input capability
- Central DMA to extract and dump its pixels
- Software extraction of its pixel data

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The DCMIPP path offers the following summarized maximum features:

- Target sensors: 5 Mpixel at 30 fps max
- Parallel input: 120 MHz on 16-bit input capability
- Serial input: CSI-2 at 2.5 Gbps/lane on two data lanes
- ISP (image signal processor): demosaicing, exposure, white-balance, contrast, bad-pixel
- Application pipes: two pipes with crop, downsize, gamma, YUV conversion, YUV420

Some over-target use cases are possible, but with specific constraints:

- sensors with resolution above 5 Mpixels
- sensors with pixel rate above 150 Mpixel/s
- double sensors in parallel

3.25.1 Digital camera interface (DCMI)

The digital camera is a synchronous parallel interface able to receive a high speed data flow from an external 8-, 10-, 12- or 14-bit CMOS camera module. It supports different data formats: YCbCr4:2:2/RGB565 progressive video and compressed data (JPEG).

DCMI main features are:

- 8-, 10-, 12- or 14-bit parallel interface at 80 MHz (no I/O ReTime)
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature
- Supports the following data formats:
  - 8/10/12/14-bit progressive video: either monochrome or raw Bayer
  - YCbCr 4:2:2 progressive video
  - RGB 565 progressive video
  - Compressed data: JPEG (any default/byte data)

3.25.2 Digital camera interface pixel pipeline (DCMIPP)

The DCMIPP path groups the DCMIPP pixel pipeline block, its included parallel interface, and the abutted CSI-2-Host and PHY.

The parallel interface has the following features:

- Input rate: 120 MHz up to 16-bit capability (with I/O ReTime)
- Pixel format: RGB565, 888, YUV422, RawBayer/Mono 8/10/12/14
- Synchronization: embedded versus external line and frame synchronization

The CSI-2 serial interface has the following features:

- Standard: MIPI CSI2 v1.3
- Input rate: two data lanes at 2.5 Gbps/lane
- Pixel rate: up to 200 Mpixel/s for RGB888, up to 333 Mpixel/s for rawBayer 10
- Pixel format: any MIPI CSI2 v1.3 (RGB565, 888, YUV422, rawBayer)
- Miscellaneous: interlaced video, interleaved packets, virtual channels

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3.26 CSI-2 Host (CSI)

The camera serial interface 2 (CSI-2) is a part of a group of communication protocols defined by the MIPI® Alliance. The MIPI CSI-2 Host controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification. It provides an interface between the system and the MIPI D-PHY, allowing communication with a CSI-2 compliant camera.

Standard and references:

- MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2) v1.3 - 29 May 2014
- MIPI Alliance Specification for D-PHY v1.2 - 01 August 2014

Main features:

- Compliant with MIPI Alliance standard
- Interface with MIPI D-PHY
- Up to two D-PHY data lanes supported
  - Up to 2.5 Gbit/s per lane in high-speed (HS) mode
  - 10 Mbit/s in low-power (LP) mode
- Data transmission in HS and LP modes supported by the D-PHY
- Escape mode (ESC) and ultra-low-power state mode (ULPS) supported
- CSI-2 lane management layer connected to the D-PHY_RX to merge 1 or 2 data lanes in a single 32-bit ISB-Byte bus
- ECC and error correction capabilities
- CRC check capability
- CSI-2 virtual channel and data type filtering supporting interleaved data
  - Up to four virtual channels
  - Support the data formats specified into the MIPI Alliance standard for CSI-2 v1.3 (18 data formats, plus the user defined ones)
- Up to seven independent data types
- Programmable interrupts:
  - Four timer interrupts mapped on a selected virtual channel with starting point from SOF (start of frame) or EOF (end of frame)
  - Four line/byte counter interrupts mapped on a selected virtual channel to trigger an event
- ISB-Byte header generation for internal connection with the DCMIPP peripheral

3.27 Parallel synchronous target interface (PSSI)

The PSSI and the DCMI use the same circuitry. As a result, these two peripherals cannot be used at the same time: when using the PSSI, the DCMI registers cannot be accessed, and vice versa. In addition, the PSSI and the DCMI share the same alternate functions and the same interrupt vector.

The PSSI is a generic synchronous 8-/16-bit parallel data input/output target interface. It enables the transmitter to send a data valid signal that indicates when the data is valid, and the receiver to output a flow control signal that indicates when it is ready to sample the data.

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The PSSI peripheral main features are the following:

- Target mode operation
- 8- or 16-bit parallel data input or output
- 8-word (32-byte) FIFO
- Data enable (PSSI_DE) and Ready (PSSI_RDY) alternate function. When selected, these signals can either enable the transmitter to indicate when the data is valid, allow the receiver to indicate when it is ready to sample the data, or both.
- Clock out mode

3.28 Display subsystem

The display subsystem is targeted to drive up to 1080p60 display panels, through a parallel interface. It supports some on-the-fly compositions to offload the GPU and optimize the use of the system bandwidth: up to two layers, color conversion, blend, mirror, and a final YUV conversion.

The display subsystem can display a secure layer with data that cannot be read by nonsecure application, and with the display guaranteed stable.

The display subsystem is built around LTDC:

- LTDC: handles display composition and rotation
  - Composition: 2 layers
  - Input pixel format: flexible format, including YUV420 full-planar on layer L1
  - Secure layer: protected access to buffer and configuration registers.
  - Mirror: horizontal and vertical
  - Miscellaneous: color lookup-table, color keying, Gamma
  - 1080p60 max performance
- LTDC parallel interface (integrated inside the LTDC):
  - Standard: 24 bpp + Hs, Vs, De (DataEnable) synchronization signals with ReTime
  - Output rate: 150 Mpixel/s
  - Resolution: 1920x1080 at 60 fps max, with HDMI blankings
  - Pixel formats: RGB888, 666, 565, YUV422-16 bits/BT601/709

3.29 LCD-TFT display controller (LTDC)

The LTDC (liquid crystal display - thin film transistor) display controller provides a parallel digital RGB (Red, Green, Blue) and signals for horizontal, vertical synchronization, pixel clock and data enable as output to interface directly to a variety of LCD-TFT panels.

LTDC main features are:

- Two input layers blended together to compose the display
- Cropping of layers from any input size and location
- Multiple input pixel formats:
  - Predefined ARGB, with 7 formats: ARGB8888, ABGR8888, RGBA8888, BGRA8888, RGB565, BGR565, RGB888packed
  - Flexible ARGB, allowing any width and location for A,R,G,B components

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  - Predefined YUV, with 3 formats: YUV422-1L (FourCC: YUYV, Interleaved), YUV420-2L (FourCC: NV12, semi planar), YUV420-3L (FourCC: Yxx I420, full planar) with some flexibility on the sequence of the component
- Color look-up table (CLUT) up to 256 colors (256x24 bits) per layer
- Color transparency keying
- Composition with flexible window position and size versus output display
- Blending with flexible layer order and alpha value (per pixel or constant)
- Background underlying color
- Gamma with non-linear configurable table
- Dithering for output with less bits per component (pseudo-random on 2 bits)
- Polarity inversion for HSync, VSync, and DataEnable outputs
- Output as RGB888 24 bpp or YUV422 16 bpp
- Secure layer (using layer2) capability, with grouped regs and additional interrupt set
- Interrupts based on seven different events
- AXI controller interface with long efficient bursts (64 or 128 bytes)

3.30 Neo-Chrom graphic processor (GPU2D)

The GPU2D is a dedicated graphics processing unit accelerating numerous 2.5D graphics applications such as graphical user interface (GUI), menu display or animations. The GPU2D works together with an optimized software stack designed for state of the art graphic rendering.

- GPU2D main features
  - Multi-threaded fragment (pixel) processing core with a VLIW (very-long instruction word) instruction set.
  - Fixed point functional units
  - Command list based DMAs to minimize CPU overhead
  - Two 64-bit AXI controller interfaces for texture and framebuffer access
  - Dedicated 64-bit AXI controller interface for command list
  - 32-bit AHB target interface for register bank access
  - Up to four general-purpose flags for system-level synchronization
  - Texture decompression unit with TSC™4 and TSC™6/TSC™6a support
- 2D drawing features
  - Pixel/line drawing
  - Filled rectangles
  - Triangles, quadrilateral drawing
  - Anti-aliasing 8xMSAA (multi-sample anti-aliasing)
- Image transformations
  - 3D perspective correct projections
  - Texture mapping with bilinear filtering or point sampling
- Blit support
  - Rotation, mirroring, stretching (independently on x and y axis)
  - Source and/or destination color keying

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  - Pixel format conversions
- Text rendering support
  - A1, A2, A4, and A8 bitmap anti-aliased
  - Subsampled anti-aliased
- Color formats
  - ABGR8888, ARGB8888, BGRA8888, RGBA8888
  - xBGR8888, xRGB8888, BGRx8888, RGBx8888, RGB888, BGR888
  - BGR565, RGB565
  - RGB322, BGR322
  - TSC4, TSC6, TSC6A
  - L1, L2, L4, L8 (gray scale)
  - A1, A2, A4, A8
- Full alpha blending with hardware blender
  - Programmable blending modes
  - Source/destination color keying

3.31 Video encoder (VENC)

The video encoder (VENC) provides a hardware acceleration to encode a 1080p30 video stream in H264 (= MPEG4_Part10/AVC). The VENC also provides hardware acceleration to encode still images (JPEG) of up to 300 Mpixel/s. The VENC implementation embeds a large 128-Kbyte video RAM (VENCRAM). When the VENC is disabled, the VENCRAM is unused for video purposes, and is accessible by the system as a contiguous extension of the system SRAM.

The VENC supports the following features:

- Video encode:
  - codecs: H264 (MPEG4_Part10/AVC, baseline/Main/High up to 5.2)
  - performance: 1080p30 for H264
- Still-image encode:
  - codecs: JPEG (baseline interleaved)
  - performance: 300 Mpixel/s for JPEG
- VENCRAM:
  - size: 128 Kbytes
  - access: can be statically assigned to the system by SYSCFG settings
- Security via RIF:
  - the VENC is protected by a default target and controller control (RISUP and RIMU)
  - by default, the VENC works in non-protected mode
  - the VENC can be set in protected mode, for instance to handle DRM tasks with a secure datapath. In such cases, the drivers must run in a protected process.
- Synchronization from an upstream peripheral: pixels can be streamed from an upstream peripheral (such as the camera) directly to the VENC, without writing to a full frame buffer, nor requiring external bandwidth.

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- Encode with multiple codecs on a same system: the VENC hardware processes the encode tasks sequentially, interleaved at frame level. Performance is shared across all the tasks.

3.32 JPEG codec (JPEG)

The hardware 8-bit JPEG codec encodes uncompressed image data stream or decodes JPEG-compressed image data stream. It also fully manages JPEG headers.

JPEG codec main features are:

- High-speed fully-synchronous operation
- Configurable as encoder or decoder
- Single-clock-per-pixel encode/decode
- RGB, YCbCr, YCMK and BW (grayscale) image color space support
- 8-bit depth per image component at encode/decode
- JPEG header generator/parser with enable/disable
- Four programmable quantization tables
- Single-clock Huffman coding and decoding
- Fully-programmable Huffman tables (two AC and two DC)
- Fully-programmable minimum coded unit (MCU)
- Concurrent input and output data stream interfaces

3.33 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a nondeterministic random bit generator (NDRBG).

The RNG true random number generator has been precertified NIST SP800-90B. It has also been tested using the German BSI statistical tests of AIS-31 (T0 to T8).

RNG main features:

- Delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage.
- Entropy source to construct a nondeterministic random bit generator (NDRBG).
- Embeds startup and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- Can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration).
- AMBA® AHB target peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored).

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3.34 Secure AES coprocessor (SAES)

The SAES encrypts or decrypts data in compliance with the advanced encryption standard (AES) defined by NIST. It incorporates a protection against side-channel attacks (SCA), including differential power analysis (DPA), certified SESIP and PSA security assurance level 3.

SAES supports ECB, CBC, CTR, GCM, GMAC, and CCM chaining modes for key sizes of 128 or 256 bits, and special modes such as hardware secret key encryption/decryption (Wrapped-key mode) and key sharing with faster CRYP peripheral (Shared-key mode).

SAES has the possibility to load STM32 hardware secret controller keys (boot hardware key BHK and derived hardware unique key DHUK), usable but not readable by application.

The peripheral supports DMA single transfers for incoming and outgoing data (two DMA channels are required). It is hardware-linked with the true random number generator (TRNG) and with the CRYP peripheral.

SAES main features:

- Compliant with NIST FIPS publication 197 “Advanced encryption standard (AES)” (November 2001)
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- Protection against side-channel attacks (SCA), incl. differential power analysis (DPA), certified SESIP and PSA security assurance level 3
- 128-bit data block processing, supporting cipher key lengths of 128-bit and 256-bit
- 480 or 680 clock cycle latency in ECB mode for processing one 128-bit block with, respectively, 128-bit or 256-bit key
- Hardware secret key encryption/ decryption (Wrapped-key mode)
- Using dedicated key bus, optional key sharing with faster CRYP peripheral (Sharedkey mode), controlled by SAES
- Integrated key scheduler to compute the last round key for ECB/CBC decryption
- 256-bit of write-only registers for storing cryptographic keys (eight 32-bit registers)
- Optional 128-bit or 256-bit hardware loading of two hardware secret keys (BHK, DHUK) that can be XOR-ed together
- Security context enforcement for keys
- 128-bit of registers for storing initialization vectors (four 32-bit registers)
- 32-bit buffer for data input and output
- Automatic data flow control supporting two direct memory access (DMA) channels, one for incoming data, one for processed data. Only single transfers are supported.
- Data-swapping logic to support 1-, 8-, 16-, or 32-bit data
- AMBA AHB target peripheral, accessible through 32-bit word single accesses only. Other access types generate an AHB error, and other than 32-bit writes may corrupt the register content.

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- Possibility for software to suspend a message if SAES needs to process another message with a higher priority, then resume the original message

3.35 Cryptographic processor (CRYP)

The cryptographic processor (CRYP) encrypts or decrypts data in compliance with the advanced encryption standard (AES) defined by NIST.

CRYP supports ECB, CBC, CTR, GCM, GMAC, and CCM chaining modes for key sizes of 128, 192, or 256 bits. CRYP has the possibility to load by hardware the key stored in SAES peripheral, under SAES control.

The peripheral supports both single and fixed DMA burst transfers for incoming and outgoing data (two DMA channels are required). CRYP also includes input and output FIFOs for better performance.

CRYP main features are:

- Compliant with NIST FIPS publication 197 “Advanced encryption standard (AES)” (November 2001)
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- 16-byte data block processing, supporting cipher key lengths of 128, 192 and 256 bits
- 14 or 18 clock cycle latency in ECB mode for processing one 16-byte block with 128-bit or 256-bit key, respectively
- Using dedicated key bus, optional key sharing with side-channel resistant SAES peripheral (shared-key mode), controlled by SAES
- Integrated key scheduler to compute the last round key for ECB/CBC decryption
- 256-bit of write-only registers for storing the cryptographic keys (eight 32-bit registers)
- 128-bit of registers for storing initialization vectors (four 32-bit registers)
- 32-bit input buffer associated with an internal input FIFO of eight 32-bit words, corresponding to two AES blocks
- 32-bit output buffer associated with an internal output FIFO of eight 32-bit words, corresponding to two AES blocks
- Automatic data flow control supporting two direct memory access (DMA) channels, one for incoming data, one for processed data. The output FIFO supports both single and burst transfers, while the input FIFO supports only burst transfers.
- Data swapping logic to support 1-, 8-, 16- or 32-bit data
- AMBA AHB target peripheral, accessible through 32-bit word single accesses only. Other access types generates an AHB error, and write accesses are ignored.
- Possibility for software to suspend a message if CRYP needs to process another message with a higher priority, then resume the original message

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3.36 Hash processor (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-2 family) and the HMAC (keyed-hash message authentication code) algorithm. HMAC is suitable for applications requiring message authentication.

The hash processor computes FIPS (Federal Information Processing Standards) approved digests of length of 160, 224, 256 bits, for messages of any length less than 264 bits (for SHA-1, SHA-224 and SHA-256) or less than 2128 bits (for SHA-384, SHA-512).

HASH main features are:

- Suitable for data authentication applications, compliant with:
  - Federal Information Processing Standards Publication FIPS PUB 180-4, Secure Hash Standard (SHA-1 and SHA-2 family)
  - Federal Information Processing Standards Publication FIPS PUB 186-4, Digital Signature Standard (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, HMAC: Keyed-Hashing for Message Authentication and Federal Information Processing Standards Publication FIPS PUB 198-1, The Keyed-Hash Message Authentication Code (HMAC)
- Fast computation of SHA-1, SHA2-224, SHA2-256, SHA2-384, and SHA2-512
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
  - 98 clock cycles for processing one 1024-bit block of data using either SHA2-384 or SHA2-512 algorithm
  - Support for SHA-2 truncated outputs (SHA2-512/224, SHA2-512/256)
  - Support for HMAC mode with all supported algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit-string
  - Supported word swapping format: bits, bytes, half-words and 32-bit words
- Single 32-bit, write-only, input register associated to an internal input FIFO, corresponding to a 64-byte block size (16 x 32 bits)
- Automatic padding to complete the input bit string to fit digest minimum block size
- AHB target peripheral, accessible by 32-bit words only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H15) for output message digest
- Automatic data flow control supporting direct memory access (DMA) using one channel.
- Support for both single and fixed DMA burst transfers of four words.
- Interruptible message digest computation, on a per-block basis
  - Re-loadable digest registers
  - Hashing computation suspend/resume mechanism, including DMA

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3.37 Memory cipher engine (MCE)

Memory cipher engine (MCE) defines, in a given address space, multiple regions with specific security setup (encryption). All system bus traffic going through an encrypted region is managed on-the-fly by the MCE, automatically decrypting reads and encrypting writes if authorized.

Multiple ciphering option (stream, block, fast block) are available to offer the best security versus performance trade-off.

MCE main features are:

- System bus in-line encryption (for writes) and decryption (for reads), based on embedded firewall programming
  - Four encryption modes per region (maximum 4 regions available): no encryption (bypass mode), stream cipher, block cipher and fast block cipher modes
  - Start and end of regions defined with 4-Kbytes granularity
  - Default filtering (region 0): any access granted
  - Regions 1 to 4 access filtering criteria: none
- Supported block ciphers: AES-128, AES-256 or Noekeon (12 round version), selected at boot
- Supported chaining modes: block and stream
  - Block mode with AES cipher is compatible with ECB mode specified in NIST FIPS publication 197 Advanced encryption standard (AES) (normal or fast).
  - Stream mode with AES cipher is compliant with CTR mode specified in NIST SP800-38A Recommendation for Block Cipher Modes of Operation.
  - Includes a leakage resilient mode of operation as defense against side channel attacks (SCA).
- One set of write-only and lockable 256-bit controller key registers per block cipher (normal, fast)
- Two sets of lockable cipher contexts (128-bit key, IV), usable for stream and block ciphers
- Optimization for XSPI data pre-fetching mechanism (stream cipher only)
- Read-write arbitration scheme, for better read performances
- AHB configuration port
- AXI system bus controller/target interfaces (64-bit)
  - Support for any AXI-64bit read transactions
  - When encryption is enabled, support for AXI-64bit INCRx (x = 1 to 8) and WRAPx (x = 4) write transactions

3.38 Public key accelerator (PKA)

PKA (public key accelerator) is intended for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann or ECC (elliptic curve cryptography) over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

For a given operation, all needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

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When manipulating secrets, the PKA incorporates a protection against side-channel attacks (SCA), including differential power analysis (DPA), certified SESIP and PSA security assurance level 3.

PKA main features are:

- Acceleration of RSA, DH and ECC over GF(p) operations, based on the Montgomery method for fast modular multiplications:
  - RSA modular exponentiation, RSA chinese remainder theorem (CRT) exponentiation
  - ECC scalar multiplication, point on curve check, complete addition, double base ladder, projective to affine
  - ECDSA signature generation and verification
- Capability to handle operands up to 4160 bits for RSA/DH and 640 bits for ECC
- When manipulating secrets: protection against side-channel attacks (SCA), including differential power analysis (DPA), certified SESIP and PSA security assurance level 3
- Applicable to modular exponentiation, ECC scalar multiplication and ECDSA signature generation
- Arithmetic and modular operations such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication
- Built-in Montgomery domain inward and outward transformations
- AMBA AHB target peripheral, accessible through 32-bit word single accesses only (otherwise an AHB bus error is generated, and write accesses are ignored)

3.39 Timers (TIMx)

The devices contain 15 timers and 5 low-power timers.

3.39.1 Basic timers (TIM6/TIM7/TIM18)

These timers consist in a 16-bit autoreload counter driven by a programmable prescaler. They can be used as generic timers for time-base generation. The timers are completely independent, and do not share any resources.

Main features:

- 16-bit autoreload upcounter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- Interrupt/DMA generation on the update event: counter overflow
- ADC synchronization for jitter-free sampling points

3.39.2 Advanced control timers (TIM1/TIM8)

The devices embed two advanced control timers that consist in a 16-bit auto-reload counter driven by a programmable prescaler. These timers can be used for a variety of purposes, such as measuring the pulse length of input signals (input capture) or generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

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The advanced control timers are completely independent from the general purpose ones, and do not share any resources. They can be synchronized together.

Advanced control timers main features are:

- 16-bit up, down, up/down auto-reload counter.
- 16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536.
- Up to six independent channels for:
  - Input capture (except channels 5 and 6)
  - Output compares
  - PWM generation (edge- and center-aligned mode)
  - One pulse mode output
- Complementary outputs with programmable dead-time
- Synchronization circuit to control the timer with external signals and to interconnect several timers together.
- Repetition counter to update the timer registers only after a given number of cycles of the counter.
- Two break inputs to put the timer’s output signals in a safe user selectable configuration.
- Interrupt/DMA generation on the following events:
  - Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output compare
- Support of incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes
- Trigger input for external clock or cycle-by-cycle current management
- ADC synchronization for jitter-free sampling points

3.39.3 General purpose timers (TIM2/TIM3/TIM4/TIM5)

These four timers consist of a 16- or 32-bit auto-reload counter driven by a programmable prescaler. They can be used for a variety of purposes, such as measuring the pulse length of input signals (input capture), or generating output waveforms (output compare and PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

The timers are completely independent, and do not share any resources. They can be synchronized together.

Main features:

- 16- or 32-bit up, down, up/down auto-reload counter.
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535.
- Up to four independent channels for:
  - Input capture
  - Output compare

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  - PWM generation (edge- and center-aligned modes)
  - One-pulse mode output
- Synchronization circuit to control the timer with external signals and to interconnect several timers.
- Interrupt/DMA generation on the following events:
  - Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output compare
- Support of incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes
- Trigger input for external clock or cycle-by-cycle current management
- ADC synchronization for jitter-free sampling points

3.39.4 General purpose timers (TIM9/TIM10/TIM11/TIM12/TIM13/TIM14)

These six timers consist in a 16-bit auto-reload counter driven by a programmable prescaler. They may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

The timers are completely independent, and do not share any resources. They can be synchronized together.

Main features:

- 16-bit auto-reload upcounter
- 16-bit programmable prescaler used to divide the counter clock frequency by any factor between 1 and 65536 (can be changed “on the fly”)
- Independent channel (up to two independent channels with TIM9/TIM12) for:
  - Input capture
  - Output compare
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Synchronization circuit to control the timer with external signals and to interconnect several timers together (TIM9/TIM12 only)
- Interrupt generation on the following events:
  - Update: counter overflow, counter initialization (by software or internal trigger)
  - Trigger event: counter start, stop, initialization, or count by internal trigger (TIM9/TIM12 only)
  - Input capture
  - Output compare
- ADC synchronization for jitter-free sampling points (TIM9/TIM12 only)

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3.39.5 General purpose timers (TIM15/TIM16/TIM17)

These timers consist of a 16-bit auto-reload counter driven by a programmable prescaler. They can be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

The timers are completely independent, and do not share any resources.

TIM15 can be synchronized. It includes the following features:

- 16-bit auto-reload upcounter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- Up to two independent channels for:
  - Input capture
  - Output compare
  - PWM generation (edge mode)
  - One-pulse mode output
- Complementary outputs with programmable dead-time (for channel 1 only)
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Break input to put the timer’s output signals in the reset state or a known state
- Interrupt/DMA generation on the following events:
  - Update: counter overflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output compares
  - Break input (interrupt request)
- ADC synchronization for jitter-free sampling points

TIM16/TIM17 main features:

- 16-bit auto-reload upcounter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- One channel for:
  - Input capture
  - Output compare
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Complementary outputs with programmable dead-time
- Repetition counter to update the timer registers only after a given number of cycles of the counter

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- Break input to put the timer's output signals in the reset state or a known state
- Interrupt/DMA generation on the following events:
  - Update: counter overflow
  - Input capture
  - Output compare
  - Break input

3.39.6 Low-power timer (LPTIM)

The LPTIM is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. Thanks to the diversity of its clock sources, the LPTIM is able to keep running in all power modes except for Standby mode. Given its capability to run even with no internal clock source, the LPTIM can be used as a pulse counter. The capability to wake up the system from low-power modes makes it suitable for timeout functions with extremely low consumption.

The LPTIM introduces a flexible clock scheme that provides the needed functionalities and performance, while minimizing the power consumption. Its main features are:

- 16 bit upcounter
- 3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, and 128)
- Selectable clock
  - Internal clock sources: configurable internal clock source (see RCC section)
  - External clock source over LPTIM input (working with no LP oscillator running, used by pulse counter application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
  - Update event
  - Input capture

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3.40 Independent watchdog (IWDG)

This peripheral offers a high safety level, thanks to its capability to detect malfunctions due to software or hardware failures. The IWDG is clocked by an independent clock, and stays active even if the main clock fails. In addition, the watchdog function is performed in the V_{DD} voltage domain, allowing the IWDG to remain functional even in low-power modes. Refer to the dedicated section of the reference manual to check its capabilities in this product.

The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, making it very reliable to detect any unexpected behavior. Its main features are:

- 12-bit down-counter
- Dual voltage domain, enabling operation in low-power modes
- Independent clock
- Early wake-up interrupt generation
- Reset generation in case of timeout and of refresh outside the expected window

3.41 System window watchdog (WWDG)

The WWDG is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence.

The watchdog circuit generates a reset on expiry of a programmed time period, unless the program refreshes the contents of the down-counter before bit T6 is cleared. A reset is also generated if the 7-bit down-counter value (in the control register) is refreshed before the down-counter reaches the window register value. This implies that the counter must be refreshed in a limited window.

The WWDG clock is prescaled from the APB clock, and has a configurable time-window that can be programmed to detect abnormally late or early application behavior.

The WWDG is best suited for applications requiring the watchdog to react within an accurate timing window. The WWDG main features are:

- Programmable free-running down-counter
- Conditional reset (if watchdog activated)
  - When the down-counter value becomes lower than 0x40
  - If the down-counter is reloaded outside the window
- Early wake-up interrupt (EWI): triggered (if enabled and the watchdog activated) when the down-counter is equal to 0x40

3.42 Real-time clock (RTC)

The RTC is an independent BCD timer/counter that provides an automatic wake-up to manage all low-power modes.

The RTC provides a time of- day clock/calendar with programmable alarm interrupts. As long as the supply voltage remains in the operating range, it never stops, regardless of the device status (Run mode, low-power mode or under reset). The RTC is functional in VBAT mode.

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Its main features are:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Binary mode with 32-bit free-running counter.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. (can be used to synchronize it with a controller clock).
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Timestamp, which can be used to save the calendar content: can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period.
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or non-secure configuration
- Alarm A, alarm B, wake-up timer and timestamp individual privilege protection
- The RTC is supplied through a switch that takes power either from the V_{DD} supply when present, or from the VBAT pin.
- The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE.
- All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes.

3.43 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks.

32 32-bit backup registers are retained in all low-power modes and in VBAT mode. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with eight tamper pins and ten internal tampers. The external tamper pins can be configured for edge or level detection with or without filtering, or active tamper, which increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- A tamper detection can erase the backup registers, backup SRAM, SRAM2, cryptographic peripherals. The protected resources are named “device secrets”.
- 32 32-bit backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the backup domain that remains powered-on by VBAT when the VDD power is switched off.
- Up to seven tamper pins for seven external tamper detection events:

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  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks.
  - Flexible active tamper I/O management: from four meshes (each input associated to its own exclusive output) to 7 meshes (single output shared for up to seven tamper inputs)
  - Passive tampers: ultra-low power edge or level detection with internal pull-up hardware management.
  - Configurable digital filter.
- Ten internal tamper events to protect against transient or environmental perturbation attacks
- Each tamper can be configured in two modes:
  - Confirmed mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Potential mode: most of the secrets erase following a tamper detection are launched by software
- Any tamper detection can generate a RTC timestamp event.
- TrustZone support:
  - Tamper secure or non-secure configuration
  - Backup registers configuration in three configurable-size areas:
- One read/write secure area
- One write secure/read non-secure area
- Put configurable-size areas in a menu
- One read/write non-secure area
  - Boot hardware key for secure AES, stored in backup registers, protected against read and write access
- Tamper configuration and backup registers privilege protection
- Monotonic counter

3.44 Inter-integrated circuit (I2C) interface

The devices contain four Inter integrated circuit (I2C1 to I2C4)

The I2C (inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I2C bus. It provides multicontroller capability, and controls all I2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode Plus (Fm+). It is also SMBus (system management bus) and PMBus® (power management bus) compatible.

DMA can be used to reduce CPU overload.

I2C main features are:

- I2C bus specification rev03 compatibility:
  - Target (formerly known as slave) and controller (formerly known as master) modes
  - Multicontroller capability
  - Standard-mode (up to 100 kHz)
  - Fast-mode (up to 400 kHz)
  - Fast-mode Plus (up to 1 MHz)

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  - 7- and 10-bit addressing mode
  - Multiple 7-bit target addresses (two addresses, one with configurable mask)
  - All 7-bit addresses acknowledge mode
  - General call
  - Programmable setup and hold times
  - Easy to use event management
  - Optional clock stretching
  - Software reset
- 1-byte buffer with DMA capability
- Programmable analog and digital noise filters

The following additional features are also available, depending upon product implementation

- SMBus specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Command and data acknowledge control
  - Address resolution protocol (ARP) support
  - Host and device support
  - SMBus alert
  - Timeouts and idle condition detection
- PMBus rev 1.3 standard compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the i2c_pclk reprogramming
- Wake-up from Stop mode on address match

Table 9. I2C implementation

I2C features[1]	I2C1	I2C2	I2C3	I2C4
7-bit addressing mode	X	X	X	X
10-bit addressing mode	X	X	X	X
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Independent clock	X	X	X	X
Wake-up from Stop mode	X[2]	X[2]	X[2]	X[2]
SMBus/PMBus	X	X	X	X

1. X = supported.
2. Supported only from Stop SVOS high.

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3.45 Improved inter-integrated circuit (I3C)

The I3C interface handles communication between this device and others, such as sensors and host processor, connected on an I3C bus. An I3C bus is a two-wire, serial single-ended, multidrop bus, intended to improve a legacy I2C bus.

The I3C SDR-only peripheral implements all the features required by the MIPI® I3C specification v1.1. It can control all I3C bus-specific sequencing, protocol, arbitration, and timing, and can act as controller, or as target.

When acting as controller, the I3C peripheral improves the features of the I2C interface preserving some backward compatibility: it allows an I2C target to operate on an I3C bus in legacy I2C fast-mode (Fm) or legacy I2C fast-mode plus (Fm+), provided that the latter does not perform clock stretching.

The I3C peripheral can be used with DMA, to off-load the CPU. Its main features are:

- MIPI® I3C specification v1.1, as:
  - I3C SDR-only primary controller
  - I3C SDR-only secondary controller
  - I3C SDR-only target
- I3C SCL bus clock frequency up to 12.5 MHz
- Registers configuration from the host application via the APB target port
- Queued data transfers:
  - Transmit FIFO (TX-FIFO) for data bytes/words to be transmitted on the I3C bus
  - Receive FIFO (RX-FIFO) for received data bytes/words on the I3C bus
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Queued control/status transfers, when controller:
  - Control FIFO (C-FIFO) for control words to be sent on the I3C bus
  - Optional status FIFO (S-FIFO) for status words as received on the I3C bus
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Messages:
  - Legacy I2C read/write messages to legacy I2C targets in Fm/Fm+
  - I3C SDR read/write private messages
  - I3C SDR broadcast CCC messages
  - I3C SDR read/write direct CCC messages
- Frame-level management, when controller:
  - Optional C-FIFO and TX-FIFO preload
  - Multiple messages encapsulation
  - Optional arbitrable header generation on the I3C bus
  - HDR exit pattern generation on the I3C bus for error recovery
- Programmable bus timing, when controller:
  - SCL high and low period
  - SDA hold time
  - Bus free (minimum) time
  - Bus available/idle condition time

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  - Clock stall time
- Target-initiated requests management:
  - Simultaneous support up to four targets, when controller
  - In-band interrupts, with programmable IBI payload (up to four bytes), with pending read notification support
  - Bus control request, with recovery flow support and hand-off delay
  - Hot-join mechanism
- HDR exit pattern detection when target
- Bus error management:
  - CEx with x = 0, 1, 2, 3 when controller
  - TEx with x = 0, 1, ..., 6 when target
  - Bus control switch error and recovery
  - Target reset
- Individual programmable event-based management:
  - Per-event identification with flag reporting and clear control
  - Host application notification via flag polling, and/or via interrupt with a per-event programmable enable
  - Error type identification
- Wake-up from low-power mode(s):
  - Acknowledged target request completion, when controller
  - Missed start detection, when target
  - Reset pattern detection, when target
- Wake-up from Stop mode(s), as controller:
  - On an in-band interrupt without payload
  - On a hot-join request
  - On a controller-role request
- • Wake-up from Stop mode(s), as target:
  - On a reset pattern
  - On a missed start
- Multiclock domain management:
  - Separate APB clock and kernel clock, driven from independently programmed clock sources via the RCC, in addition to SCL clock
  - Minimum operating frequency for the kernel clock and the APB clock vs. the application-driven SCL clock

3.46 Universal synchronous/asynchronous receiver transmitter (USART/UART/LPUART)

USART offers a flexible way to perform Full-duplex data exchange with external equipments requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

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3.46.1 USART/UART

The USART supports both synchronous one-way and Half-duplex Single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and Modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications are possible by using the DMA (direct memory access) for multibuffer configuration.

USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data. Each FIFO can be enabled/disabled by software and come with a status flag.
- A common programmable transmit and receive baud rate
- Dual clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection
- Programmable data word length (7, 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous target/controller mode and clock output/input for synchronous communications
- SPI target transmission underrun error flag
- Single-wire Half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA.
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop mode

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USART extended features are:

- LIN controller synchronous break send capability and LIN target break detection capability
- 13-bit break generation and 10/11 bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16 bit duration for Normal mode
- Smartcard mode
- Support of T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
- 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

3.46.2 LPUART

The LPUART is an UART that enables bidirectional UART communications with a limited power consumption.

Only 32.768 kHz LSE clock is required to enable UART communications up to 9600 bauds. Higher baud rates can be reached when the LPUART is clocked by other clock sources.

Even when the microcontroller is in low-power mode, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption.

The LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption. It supports Half-duplex, Single-wire communications, and modem operations (CTS/RTS). It also supports multiprocessor communications. DMA can be used for data transmission/reception

LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 to 9600 bauds using a 32.768 kHz clock source.
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data. Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual clock domain with dedicated kernel clock for peripherals independent from PCLK.
- Programmable data word length (7, 8, or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (one or two stop bits)
- Single-wire Half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA.
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration

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- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wake up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop mode

Table 10. Instance implementation

Instance	STM32N6xx
USART1	Full
USART2	Full
USART3	Full
USART6	Full
USART10	Full
UART4	Basic
UART5	Basic
UART7	Basic
UART8	Basic
UART9	Basic
LPUART1	Low-power

Table 11. USART/LPUART features

Mode or feature(1)	Full feature	Basic feature	Low-power feature
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode (target/controller)	X	-	-
Smartcard mode	X	-	-
Single-wire half-duplex communication	X	X	X

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Table 11. USART/LPUART features (continued)

Mode or feature[1]	Full feature	Basic feature	Low-power feature
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual-clock domain	X	X	X
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Auto baud rate detection	X	X	-
Driver enable	X	X	X
USART data length	7, 8 and 9 bits		
Tx/Rx FIFO	X	X	X
Tx/Rx FIFO size (bytes)	16		
Wake-up from low-power mode	X[2]	X[2]	X[2]

1. X = supported.
2. Wake-up supported from Stop mode.

3.47 Serial peripheral interface (SPI)

The devices embed three serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices.

The interface can be configured as controller or target and can operate in multitarget or multicontroller configurations. The device configured as controller provides communication clock (SCK) to the target device. The target select (SS) and ready (RDY) signals can be applied optionally just to setup communication with concrete target and to assure it handles the data flow properly. The Motorola® data format is used by default, but some other specific modes are supported as well.

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The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- From 4- to 32-bit data size selection
- Multicontroller or multitarget mode capability
- Dual-clock domain (the peripheral kernel clock is independent from the APB bus clock)
- Baud rate prescaler up to kernel frequency divided by two, or bypass from RCC in controller mode
- Protection of configuration and setting
- Hardware or software management of SS for both controller and target
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO x MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- Support of SPI Motorola® and Texas Instruments® formats
- Hardware CRC feature can verify the integrity of the communication at the end of transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun, the mode fault, and frame error, depending upon the operating mode
- Two 8-bit width embedded Rx and Tx FIFOs, whose size depends upon the instance
- Configurable FIFO thresholds (data packing)
- Configurable behavior at target underrun condition (support of cascaded circular buffers)
- Configurable behavior at target underrun condition (support of cascaded circular buffers)
- Optional status pin RDY signaling that the target device is ready to handle the data flow

Table 12. SPI features

Feature	SPI1, SPI2, SPI3, SPI6	SPI4, SPI5
Data and CRC size	Configurable from 4 to 32 bits	Configurable from 4 to 16 bits
CRC computation	CRC polynomial length, configurable from 5 to 33 bits	CRC polynomial length, configurable from 5 to 17 bits
Size of FIFOs	16x8 bits	8x8 bits
Number of data control (TSIZE)	Up to 65536	
I2S feature	Yes	No

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Table 12. SPI features (continued)

Feature	SPI1, SPI2, SPI3, SPI6	SPI4, SPI5
Autonomous in Stop modes with wake-up capability	No	
Autonomous in Standby mode	No	

3.48 Serial audio interface (SAI)

The SAI offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications can be targeted. I2S standards, LSB or MSB-justified, PCM/DSP, TDM, and AC'97 protocols can be addressed. SPDIF output is offered when the audio block is configured as a transmitter.

The SAI contains two independent audio sub-blocks, each has its own clock generator and I/O line controller.

The SAI works in controller or target configuration. The audio sub-blocks act as receiver or transmitter, and work synchronously or not (with respect to the other one).

The SAI can be connected with other SAIs, to work synchronously.

SAI main features are:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO
- 8-word integrated FIFOs for each audio sub-block
- Synchronous or asynchronous mode between the audio sub-blocks
- Possible synchronization between multiple SAIs
- Target or controller configuration independent for both audio sub-blocks
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in controller mode
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit
- Audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97
- PDM interface, supporting up to four microphone pairs
- SPDIF output available if required
- Up to 16 slots available with configurable size
- Number of bits by frame can be configurable
- Frame synchronization active level configurable (offset, bit length, level)
- First active bit position in the slot is configurable
- LSB first or MSB first for data transfer
- Mute mode
- Stereo/Mono audio frame capability
- Communication clock strobing edge configurable (SCK)
- Error flags with associated interrupts if enabled respectively
  - Overrun and underrun detection
  - Anticipated frame synchronization signal detection in target mode
  - Late frame synchronization signal detection in target mode

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  - Codec not ready for the AC’97 mode in reception
- Interrupt sources when enabled:
  - Errors
  - FIFO requests
- 2-channel DMA interface

Table 13. SAI features(1)

Feature	SAI1	SAI2
I2S, LSB- or MSB-justified, PCM/DSP, TDM, AC’97	X	X
FIFO size	8 words	
SPDIF	X	X
PDM	X(2)	-

1. ‘X’ = supported, ‘-’ = not supported.
2. Only signals D[3:1] and CK[2:1] are available.

3.49 SPDIF receiver interface (SPDIFRX)

The SPDIFRX interface handles S/PDIF audio protocol. Its main features are:

- Up to four inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 8 to 192 kHz supported
- Supports audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

3.50 Management data input/output (MDIOS)

An MDIO bus can be useful in systems where a controller chip needs to manage (configure and get status data from) one or multiple target chips.

The bus protocol uses only two signals, namely MDC (management data clock), and MDIO, the data line carrying the opcode (write or read), the target (port) address, the MDIOS register address, and the data.

In each transaction, the controller either reads the contents of an MDIOS register in one of its targets, or it writes data to an MDIOS register in one of its targets.

The MDIOS peripheral serves as a target interface to an MDIO bus. An MDIO controller can use the MDC/MDIO lines to write and read 32 16-bit registers held in the MDIOS. These registers are managed by the firmware. This allows the MDIO controller to configure the application running on the device and get status information from it.

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The MDIOS can operate in Stop mode, optionally waking up the device if the MDIO controller performs a read or a write to one of its MDIOS registers.

The MDIOS includes the following features:

- 32 MDIOS register addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIOS read-only output data registers
  - 32 x 16-bit firmware read-only, MDIOS write-only input data registers
- Configurable target (port) address
- Independently maskable interrupts/events:
  - MDIOS register write
  - MDIOS register read
  - MDIOS protocol error
- Able to operate in and to wake up from Stop mode

3.51 Controller area network with flexible data rate (FDCAN)

The controller area network (CAN) subsystem consists of three CAN modules, a shared message RAM and a clock calibration unit. Refer to the product memory organization for the base address of each of them.

FDCAN modules are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

In addition, the first CAN module FDCAN1 supports time triggered CAN (TTCAN), specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10 Kbyte message RAM implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TTCAN). This message RAM is shared between the FDCAN modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for each FDCAN from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

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The main features are:

- Conform with CAN protocol version 2.0 part A, B, and ISO 11898-1: 2015, -4
- CAN FD with max. 64 data bytes supported
- TTCAN protocol level 1 and level 2 completely in hardware (FDCAN1 only)
- Event synchronized time-triggered communication supported (FDCAN1 only)
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering
- Two configurable receive FIFOs
- Separate signaling on reception of high priority messages
- Up to 64 dedicated receive buffers
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO / queue
- Configurable transmit event FIFO
- FDCAN modules share the same message RAM
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains: APB bus interface and CAN core kernel clock
- Power-down support

3.52 USB on-the-go high speed (OTG)

Reference is made to the following documents:

- USB On-The-Go Supplement, Revision 2.0
- Universal Serial Bus Revision 2.0 Specification
- USB 2.0 Link Power Management Addendum Engineering Change Notice to the USB 2.0 specification, July 16, 2007
- Errata for USB 2.0 ECN: Link Power Management (LPM) - 7/2007
- Battery Charging Specification, Revision 1.2

The USB OTG is a dual-role device (DRD) controller that supports both device and host functions and is fully compliant with the On-The-Go Supplement to the USB 2.0 Specification. It can also be configured as a host-only or device-only controller, fully compliant with the USB 2.0 Specification. OTG supports the speeds defined in *Table 14*.

Table 14. Supported OTG speeds

Mode	HS (480 Mbit/s)	FS (12 Mbit/s)	LS (1.5 Mbit/s)
Host mode	X	X	X
Device mode	X	X	-

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3.53 USB HS PHY controller (USBPHYC)

There are two near-identical instances, namely USBPHYC1 (associated with OTG1), and USBPHYC2 (associated with OTG2) including one additional control bit for hardware debug (HDP).

For a more complete system view of the USB controllers and PHYs, refer to the block diagram of the main OTG controller. This controller handles general and miscellaneous control of the OTG PHYs.

The main features are:

- PLL configuration
- Trimming of the electrical parameters (if required)

3.54 USB Type-C / USB Power Delivery controller (UCPD)

The device embeds one controller (UCPD) compliant with USB Type-C Cable and Connector Specification release 2.0 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB power delivery requirements, featuring:

- Compliance with USB Type-C specification release 2.3
- Compliance with USB Power Delivery specifications revision 2.0 and 3.2
  - Enabling advanced applications such as PPS (programmable power supply)
- Stop mode low-power operation support
- Built-in analog PHY
  - USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
  - USB Power Delivery message transmission and reception

The digital controller handles:

- USB Type-C level detection with debounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB power delivery payload, generating interrupts (DMA compatible)
- USB power delivery timing dividers (including a clock prescaler)
- BMC (bi-phase mark coding) encode and decode
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Clock recovery from incoming Rx stream

3.55 Ethernet (ETH): gigabit media access control (GMAC) with DMA controller

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The Ethernet peripheral enables to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2015 standard.

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The peripheral is configurable to meet the needs of a large variety of consumer and industrial applications, including AV nodes and TSN (time sensitive networking) nodes.

The Ethernet peripheral embeds a dedicated DMA for direct memory interface, a media access controller (MAC) and a PHY interface block supporting several formats.

The Ethernet peripheral is compliant with the following standards:

- IEEE 802.3-2015 for Ethernet MAC and media independent interface (MII)
- IEEE 1588-2008 for precision networked clock synchronization (PTP)
- IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic
- IEEE 802.3az-2010 for Energy Efficient Ethernet (EEE)
- AMBA 2.0 for AHB target port
- AMBA4 for AXI controller port
- RGMII specification version 2.6 from HP/Marvell
- RMII specification version 1.2 from RMII consortium

Caution: The gigabit media independent interface (GMII) is only available internally to supply the RGMII adapter. No GMII signals are available off-chip

3.56 Development support

3.56.1 Serial-wire/JTAG debug port (SWJ-DP)

This is a CoreSight component that implements an external access port for connecting debugging equipment. Two types of interface can be configured, namely a 5-pin standard JTAG interface (JTAG-DP), and a 2-pin (clock + data) serial-wire debug port (SW-DP).

The two modes are mutually exclusive, as they share the same I/O pins.

By default, the JTAG-DP is selected after a system or POR. The five I/O pins are configured by hardware in debug alternative function mode. The SWJ-DP incorporates pull-up resistors on JTDI, JTMS/SWDIO, and NJTRST, as well as a pull-down resistor on JTCK/SWCLK.

A debugger can select the SW-DP by transmitting the following serial data sequence on JTMS/SWDIO: ...(50 or more ones)...,0,1,1,1,1,0,0,1,1,1,1,0,0,1,1,1,...(50 or more ones)...

JTCK/SWCLK must be cycled for each data bit.

In SW-DP mode, the unused JTAG pins (JTDI, JTDO, and NJTRST) can be used for other functions.

Note: All SWJ port I/Os can be reconfigured to other functions by software, but debugging is no longer possible.

3.56.2 Embedded Trace Macrocell

The Cortex-M55 ETM is a CoreSight component closely coupled to the CPU. The ETM generates trace packets that allow to trace the execution of the Cortex-M55 core.

Note: Data accesses are not included in the trace information.

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The ETM receives information from the CPU over the processor trace interface, including:

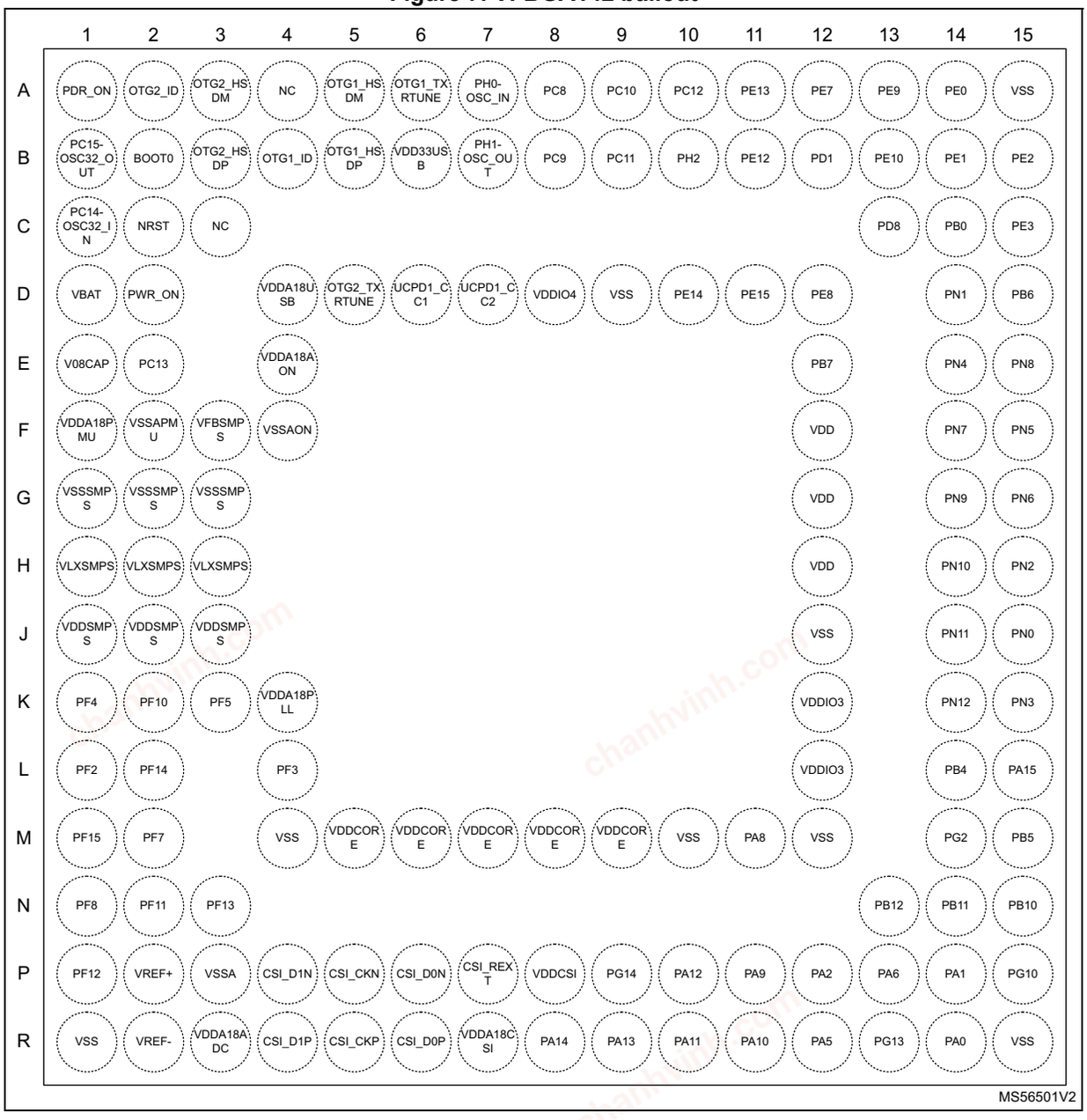
- the number of instructions executed in the same cycle
- changes in program flow
- the current processor instruction state
- addresses of memory locations accessed by load and store instructions
- type, direction and size of a transfer
- condition code information
- exception information
- wait for interrupt state information

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4 Pinout, pin description and alternate functions

4.1 Pinout/ballout schematics

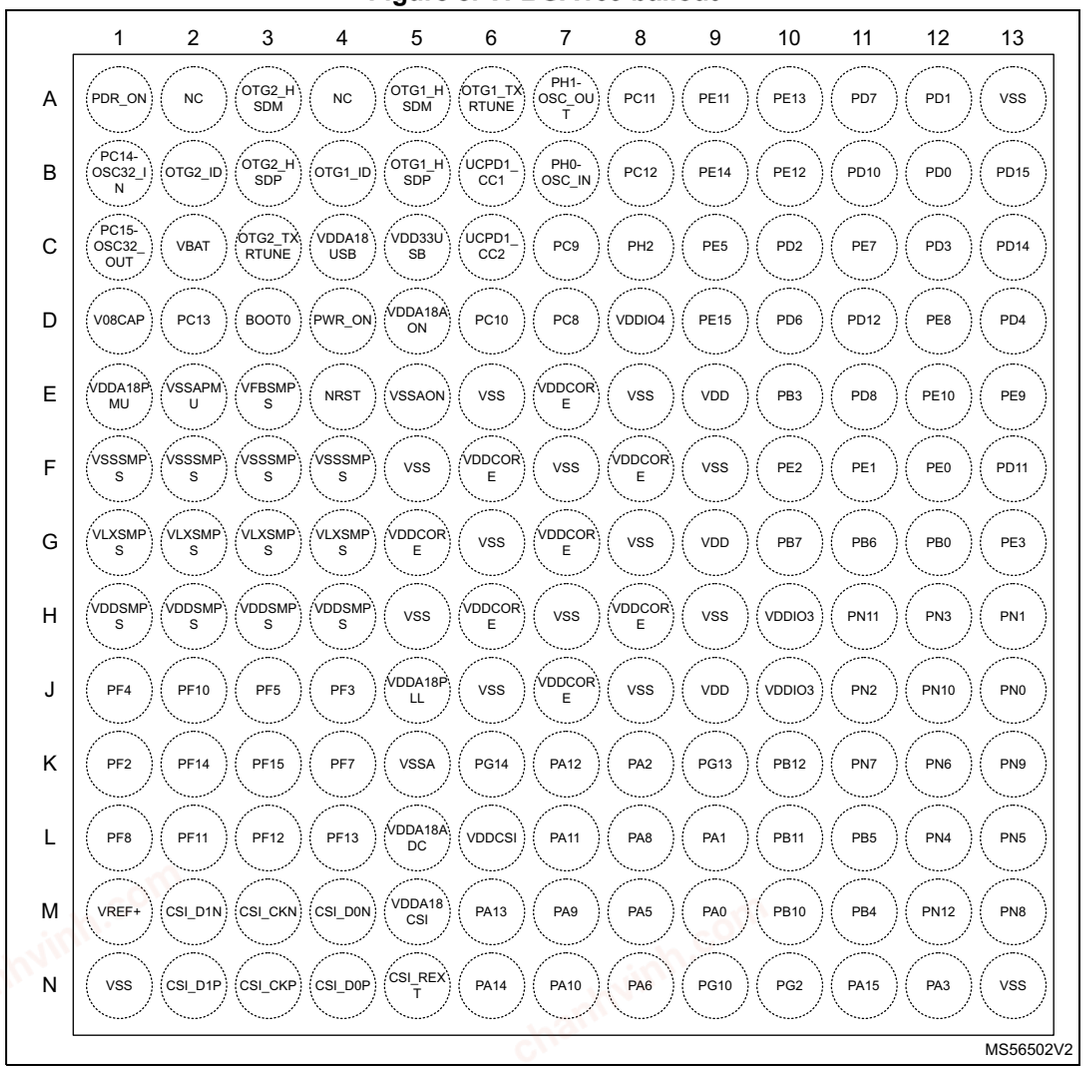
Figure 7. VFBGA142 ballout



1. The above figure shows the package top view.

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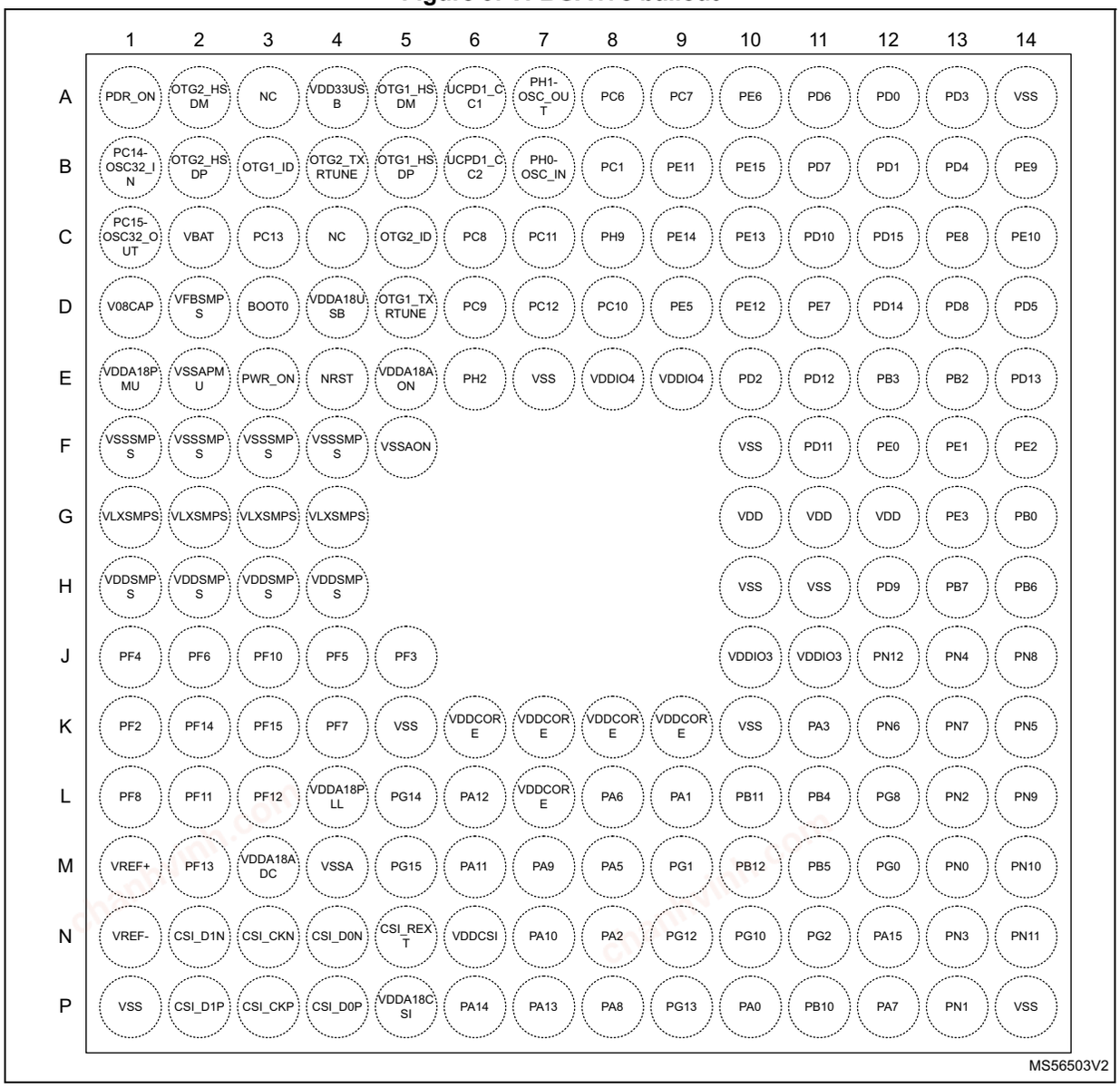
Figure 8. VFBGA169 ballout



1. The above figure shows the package top view.

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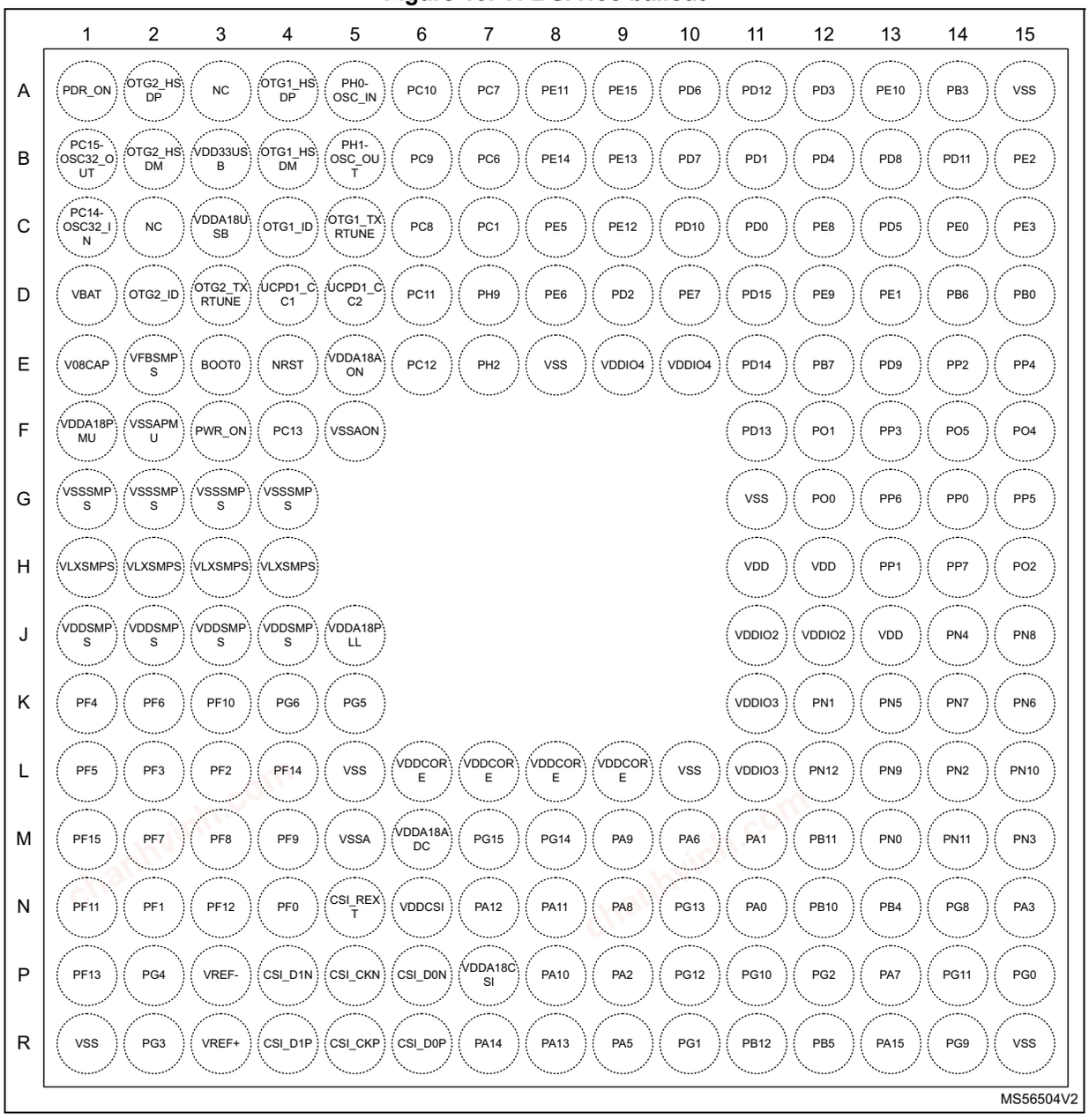
Figure 9. VFBGA178 ballout



1. The above figure shows the package top view.

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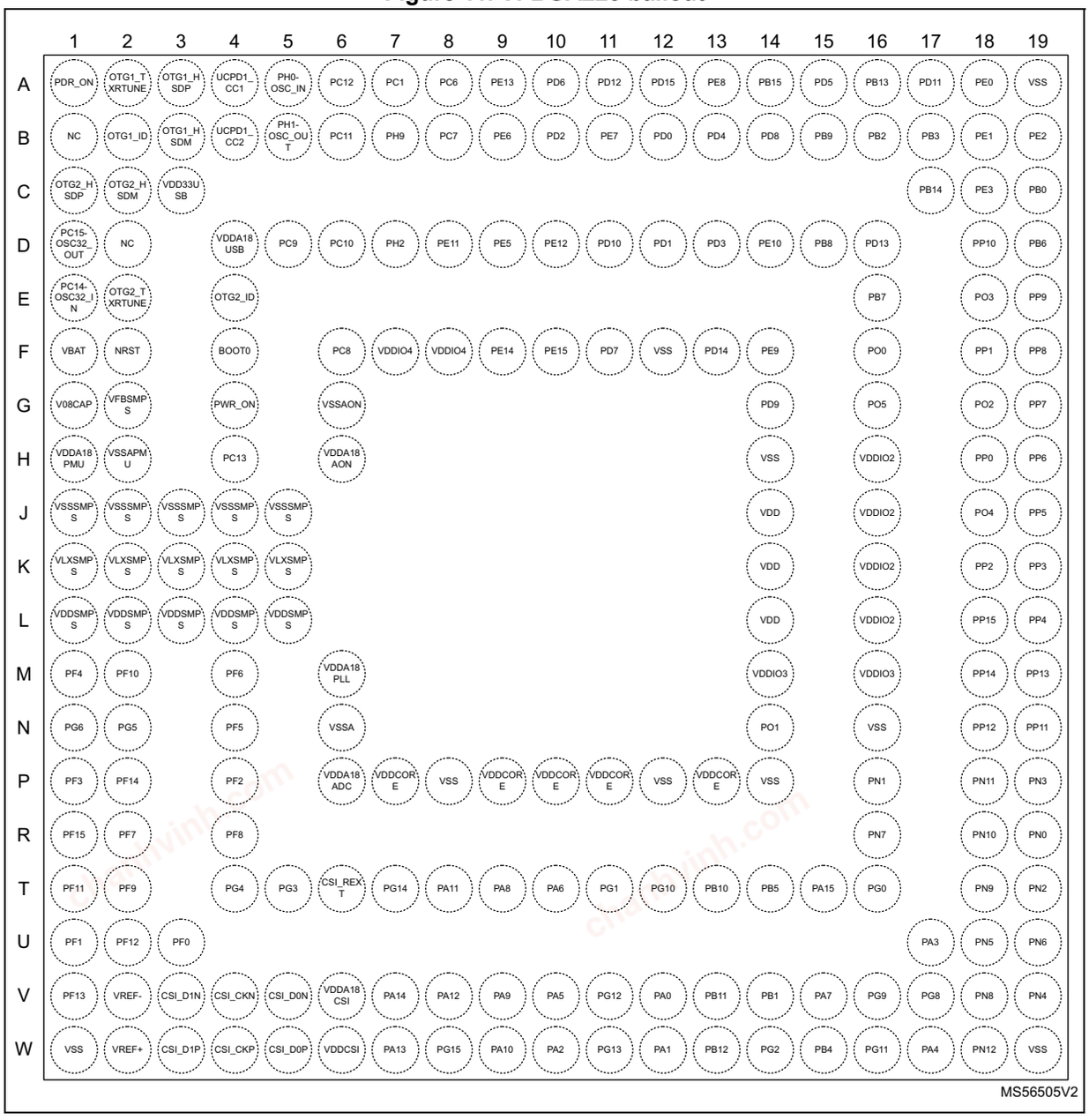
Figure 10. VFBGA198 ballout



1. The above figure shows the package top view.

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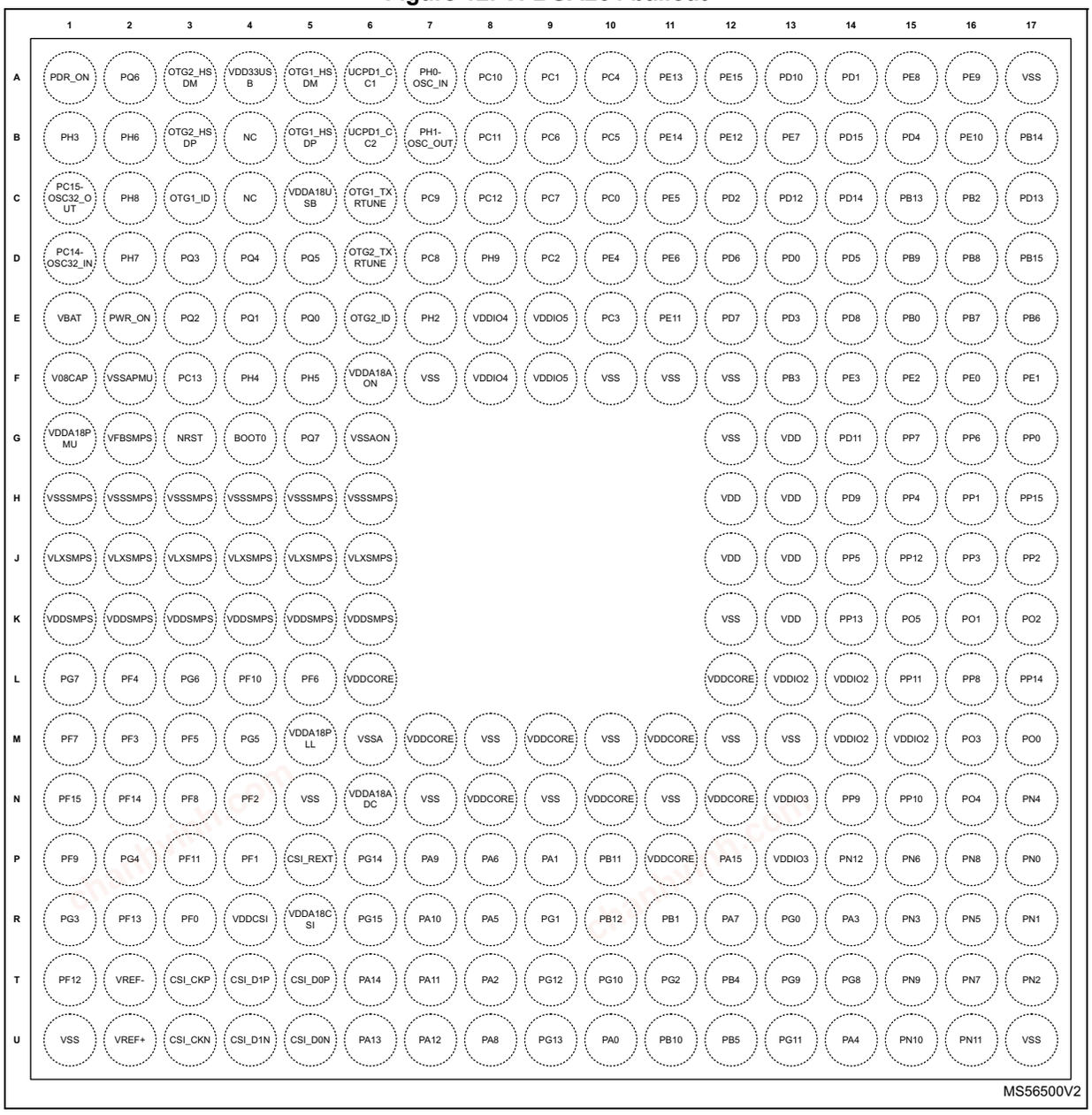
Figure 11. VFBGA223 ballout



1. The above figure shows the package top view.

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Figure 12. VFBGA264 ballout



1. The above figure shows the package top view.

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4.2 Pin description

Table 15. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input/output pin
I/O structure		TT	3.3 V-tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Options for TT I/Os(1)	
		_a	I/O, with analog switch function supplied by V_{DDA}
		_c	I/O with USB Type-C power delivery function
		_f	I/O, Fm+ capable
		_h	I/O with high speed low voltage mode
		_t	I/O with tamper function functional in VBAT mode
		_v	I/O very high-speed capable
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in the following table are a concatenation of various options. Examples: TT_a, TT_hat, TT_f.

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Table 16. Pin description

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
R2	-	N1	P3	V2	T2	VREF-	S	-	-	-	--
P2	M1	M1	R3	W2	U2	VREF+	S	-	-	-	-
D2	D4	E3	F3	G4	E2	PWR_ON	I	-	-	-	-
A1	A1	A1	A1	A1	A1	PDR_ON	I	-	-	-	-
B2	D3	D3	E3	F4	G4	BOOT0	I	-	-	-	-
C2	E4	E4	E4	F2	G3	NRST	I	-	-	-	-
P5	M3	N3	P5	V4	U3	CSI_CKN	I	-	-	-	-
R5	N3	P3	R5	W4	T3	CSI_CKP	I	-	-	-	-
P6	M4	N4	P6	V5	U5	CSI_D0N	I	-	-	-	-
R6	N4	P4	R6	W5	T5	CSI_D0P	I	-	-	-	-
P4	M2	N2	P4	V3	U4	CSI_D1N	I	-	-	-	-
R4	N2	P2	R4	W3	T4	CSI_D1P	I	-	-	-	-
P7	N5	N5	N5	T6	P5	CSI_REXT	I/O	-	-	-	-
A3	A3	A2	B2	C2	A3	OTG2_HSDM	I/O	-	-	-	-
B3	B3	B2	A2	C1	B3	OTG2_HSDP	I/O	-	-	-	-
A2	B2	C5	D2	E4	E6	OTG2_ID	I/O	-	-	-	-
C3	A2	C4	C2	D2	C4	NC	-	-	-	-	-
D5	C3	B4	D3	E2	D6	OTG2_TXRTUNE	I/O	-	-	-	-
A5	A5	A5	B4	B3	A5	OTG1_HSDM	I/O	-	-	-	-
B5	B5	B5	A4	A3	B5	OTG1_HSDP	I/O	-	-	-	-
B4	B4	B3	C4	B2	C3	OTG1_ID	I/O	-	-	-	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
A4	A4	A3	A3	B1	B4	NC	-	-	-	-	-
A6	A6	D5	C5	A2	C6	OTG1_TXRTUNE	I/O	-	-	-	-
D6	B6	A6	D4	A4	A6	UCPD1_CC1	I/O	-	-	-	-
D7	C6	B6	D5	B4	B6	UCPD1_CC2	I/O	-	-	-	-
F3	E3	D2	E2	G2	G2	VFBSMPS	S	-	-	-	-
R14	M9	P10	N11	V12	U10	PA0	I/O	-	-	TIM2_CH1, TIM5_CH1, TIM9_CH1, TIM15_BKIN, SPI6_NSS/I2S6_WS, USART2_CTS/USART2_NSS, UART4_TX, SAI2_SD_B, SDMMC2_CMD, FMC_AD7/FMC_D7, LCD_G3, HDP0	ADC1_INP0, ADC2_INP0, ADC1_INN1, ADC2_INN1, WKUP1
P14	L9	L9	M11	W12	P9	PA1	I/O	-	-	TIM2_CH2, TIM5_CH2, LPTIM3_IN1, TIM15_CH1N, USART2_RTS, UART4_RX, DCMIPP_D0/DCMI_D0/PSSI_D0, SAI2_MCLK_B, FMC_AD6/FMC_D6, LCD_G2, HDP1	ADC1_INP1, ADC2_INP1
P12	K8	N8	P9	W10	T8	PA2	I/O	-	-	TIM2_CH3, TIM5_CH3, LPTIM3_IN2, TIM15_CH1, USART2_TX, SAI2_SCK_B, MDIOS_MDIO, FMC_AD5/FMC_D5, LCD_B7, HDP2	ADC1_INP14, ADC2_INP14, WKUP2
-	N12	K11	N15	U17	R14	PA3	I/O	-	-	TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, FMC_A17/FMC_ALE, EVENTOUT	-
-	-	-	-	W17	U14	PA4	I/O	-	-	SPI5_MOSI, USART6_RX, DCMIPP_D3/DCMI_D3/PSSI_D3, FMC_A13, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
R12	M8	M8	R9	V10	R8	PA5	I/O	-	-	PWR_CSTOP, TIM2_CH1, TIM2_ETR, TIM9_CH2, I3C1_SCL, SPI1_SCK/I2S1_CK, SPI6_SCK/I2S6_CK, DCMIPP_D8/DCMI_D8/PSSI_D8, TIM10_CH1, FMC_NOE, LCD_CLK, HDP5	ADC2_INP18
P13	N8	L8	M10	T10	P8	PA6	I/O	-	-	BOOT1, TIM1_BKIN, TIM3_CH1, LPTIM3_ETR, I3C1_SDA, SPI1_MISO/I2S1_SDI, SPI6_MISO/I2S6_SDI, DCMIPP_PIXCLK/DCMI_PIXCLK/PSSI_PDCK, TIM13_CH1, MDIOS_MDC, LCD_B7, LCD_HSYNC, HDP6	ADC1_INP3, ADC2_INP3
-	-	P12	P13	V15	R12	PA7	I/O	-	-	TIM1_CH1N, TIM3_CH2, SPI1_MOSI/I2S1_SDO, USART1_RX, SPI6_MOSI/I2S6_SDO, LCD_R4, TIM14_CH1, FMC_RNB, LCD_B1, HDP7	ADC1_INP14, ADC2_INP14, WKUP2
M11	L8	P8	N9	T9	U8	PA8	I/O	-	-	MCO1, TIM1_CH1, I3C2_SCL, I2C3_SCL, USART1_CK, TIM11_CH1, UART7_RX, FMC_AD4/FMC_D4, LCD_B6, HDP0	ADC1_INP5, ADC2_INP5
P11	M7	M7	M9	V9	P7	PA9	I/O	-	-	TIM1_CH2, I3C2_SDA, LPUART1_TX, I2C3_SDA, SPI2_SCK/I2S2_CK, USART1_TX, DCMIPP_D0/DCMI_D0/PSSI_D0, FMC_AD3/FMC_D3, LCD_B5, HDP1	ADC1_INP10, ADC2_INP10
R11	N7	N7	P8	W9	R7	PA10	I/O	-	-	PWR_CSLEEP, TIM1_CH3, LPUART1_RX, USART1_RX, DCMIPP_D1/DCMI_D1/PSSI_D1, MDIOS_MDIO, FMC_AD2/FMC_D2, LCD_B4, HDP2	ADC1_INP11, ADC2_INP11, ADC1_INN10, ADC2_INN10
R10	L7	M6	N8	T8	T7	PA11	I/O	-	-	TIM1_CH4, LPUART1_CTS, SPI2_NSS/I2S2_WS, FDCAN1_RX, USART1_CTS/USART1_NSS, UART4_RX, FMC_AD1/FMC_D1, LCD_B3, HDP3	ADC1_INP12, ADC2_INP12, ADC1_INN11, ADC2_INN11

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
P10	K7	L6	N7	V8	U7	PA12	I/O	-	-	TIM1_ETR, LPUART1_RTS, SPI2_SCK/I2S2_CK, FDCAN1_TX, USART1_RTS, UART4_TX, SAI2_FS_B, FMC_AD0/FMC_D0, LCD_B2, HDP4	ADC1_INP13, ADC2_INP13, ADC1_INN12, ADC2_INN12
R9	M6	P7	R8	W7	U6	PA13 (JTMS/SWDIO)	I/O	-	-	JTMS/SWDIO, HDP5	-
R8	N6	P6	R7	V7	T6	PA14 (JTCK/SWCLK)	I/O	-	-	JTCK/SWCLK, HDP6	-
L15	N11	N12	R13	T15	P12	PA15(JTDI)	I/O	-	-	JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS/I2S6_WS, UART4_RTS, UART7_TX, FMC_D15/FMC_AD15, LCD_R5, HDP7	-
C14	G12	G14	D15	C19	E15	PB0	I/O	-	-	TRACED1, TIM1_CH4, SAI1_D2, ADF1_SDI0, MDF1_SDI2, SPI4_NSS, SAI1_FS_A, TIM15_CH1N, DCMIPP_D4/DCMI_D4/PSSI_D4, FMC_D13/FMC_AD13, EVENTOUT	-
-	-	-	-	V14	R11	PB1	I/O	-	-	TIM1_CH3N, TIM3_CH4, TIM9_CH2, FDCAN2_TX, USART2_TX, FMC_NOE, [RNG_S2], LCD_R1, HDP1	-
-	-	E13	-	B16	C16	PB2	I/O	-	-	RTC_OUT2, TIM1_CH1, SAI1_D1, ADF1_SDI0, MDF1_SDI1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, FMC_D2/FMC_AD2, LCD_B2, HDP2	-
-	E10	E12	A14	B17	F13	PB3	I/O	-	-	TRACECLK, TIM1_CH4N, GFXTIM_FCKCAL, MDF1_CKI1, USART1_CK, SAI2_FS_B, FMC_NBL1, GFXTIM_LCKCAL, FMC_A23, HDP0	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
L14	M11	L11	N13	W15	T12	PB4 (NJTRST)	I/O	-	-	NJTRST, TIM16_BKIN, TIM3_CH1, LPTIM4_ETR, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO/I2S6_SDI, DCMIPP_VSYNC/DCMI_VSYNC/PSSI_RDY, UART7_TX, SDMMC2_D3, FMC_D13/FMC_AD13, LCD_R3, HDP4	-
M15	L11	M11	R12	T14	U12	PB5 (JTDO/TRACESWO)	I/O	-	-	JTDO/TRACESWO, TIM17_BKIN, TIM3_CH2, LPTIM4_OUT, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, FDCAN2_RX, SPI3_MOSI/I2S3_SDO, SPI6_MOSI/I2S6_SDO, DCMIPP_D10/DCMI_D10/PSSI_D10, UART5_RX, FMC_D12/FMC_AD12, LCD_R2, HDP5	-
D15	G11	H14	D14	D19	E17	PB6	I/O	-	-	TRACED2, SAI1_CK2, ADF1_CCK1, MDF1_CCK1, SPI4_MISO, SAI1_SCK_A, TIM15_CH1, DCMIPP_D6/DCMI_D6/PSSI_D6, FMC_D14/FMC_AD14, EVENTOUT	-
E12	G10	H13	E12	E16	E16	PB7	I/O	-	-	TRACED3, TIM1_BKIN2, SAI1_D1, ADF1_SDI0, MDF1_SDI1, SPI4_MOSI, SAI1_SD_A, TIM15_CH2, DCMIPP_D7/DCMI_D7/PSSI_D7, SAI2_MCLK_B, FMC_D15/FMC_AD15, EVENTOUT	-
-	-	-	-	D15	D16	PB8	I/O	-	-	SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX1_IN3, DCMIPP_VSYNC/DCMI_VSYNC/PSSI_RDY, SAI2_FS_B, SDMMC2_D0, FMC_D1/FMC_AD1, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	-	-	-	B15	D15	PB9	I/O	-	-	LPTIM1_IN2, SPI1_SCK/I2S1_CK, USART10_TX, SPDIFRX1_IN0, DCMIPP_D3/DCMI_D3/PSSI_D3, SDMMC2_D2, FMC_D3/FMC_AD3, EVENTOUT	-
N15	M10	P11	N12	T13	U11	PB10	I/O	-	-	TIM2_CH3, I3C2_SCL, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, FMC_D11/FMC_AD11, LCD_G7, HDP2	ADC1_INP8, ADC2_INP8, ADC1_INN4, ADC2_INN4
N14	L10	L10	M12	V13	P10	PB11	I/O	-	-	TIM2_CH4, I3C2_SDA, LPTIM2_ETR, I2C2_SDA, USART3_RX, FMC_D10/FMC_AD10, LCD_G6, HDP3	ADC1_INP4, ADC2_INP4
N13	K10	M10	R11	W13	R10	PB12	I/O	-	-	TIM1_BKIN, LPTIM2_IN2, I2C2_SMBA, SPI2_NSS/I2S2_WS, FDCAN2_RX, USART3_CK, UART5_RX, FMC_D9/FMC_AD9, LCD_G5, HDP4	-
-	-	-	-	A16	C15	PB13	I/O	-	-	TRACED0, LPTIM1_CH1, TIM8_CH3N, SPI6_SCK/I2S6_CK, USART10_CTS/USART10_NSS, USART6_CTS/USART6_NSS, SDMMC2_D6, FMC_D5/FMC_AD5, LCD_CLK, EVENTOUT	-
-	-	-	-	C17	B17	PB14	I/O	-	-	LPTIM1_CH2, TIM8_CH4N, USART10_CK, USART6_CTS/USART6_NSS, DCMIPP_D10/DCMI_D10/PSSI_D10, FMC_D7/FMC_AD7, LCD_HSYNC, EVENTOUT	-
-	-	-	-	A14	D17	PB15	I/O	-	-	SPI6_NSS/I2S6_WS, USART6_RTS, SPDIFRX1_IN2, FMC_D0/FMC_AD0, LCD_G4, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	-	-	-	-	C10	PC0	I/O	-	-	TIM2_CH2, LPTIM4_IN1, MDF1_CKI1, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK/I2S6_CK, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, UART7_RX, SDMMC2_D2, FMC_D14/FMC_AD14, LCD_R4, HDP3	-
-	-	B8	C7	A7	A9	PC1	I/O	-	-	TIM17_CH1, TIM4_CH4, I2C1_SDA, SPI2_NSS/I2S2_WS, FDCAN1_TX, I3C1_SDA, UART4_TX, DCMIPP_D7/DCMI_D7/PSSI_D7, SDMMC1_D5, SDMMC2_D5, SDMMC1_CDIR, HDP1	-
-	-	-	-	-	D9	PC2	I/O	-	-	SAI1_D1, ADF1_SDI0, MDF1_SDI1, SPI3_MOSI/I2S3_SDO, SAI1_SCK_A, USART2_RX, DCMIPP_D13/DCMI_D13/PSSI_D13, SDMMC2_CK(boot), FMC_NE3, FMC_RNB, EVENTOUT	-
-	-	-	-	-	E10	PC3	I/O	-	-	SPI1_MOSI/I2S1_SDO, USART2_CK, SPDIFRX1_IN0, DCMIPP_D2/DCMI_D2/PSSI_D2, SDMMC2_CMD(boot), FMC_D8/FMC_AD8, EVENTOUT	-
-	-	-	-	-	A10	PC4	I/O	-	-	TIM1_CH2N, TIM12_CH1, LPTIM2_CH2, USART1_TX, SPI2_MISO/I2S2_SDI, USART3_RTS, UART4_RTS, LCD_VSYNC, SDMMC2_D0(boot), FMC_NE1, LCD_DE, HDP6	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	-	-	-	-	B10	PC5	I/O	-	-	SPI1_NSS/I2S1_WS, DCMIPP_D2/DCMI_D2/PSSI_D2, SAI2_SD_B, SDMMC2_D1, FMC_NWE, EVENTOUT	-
-	-	A8	B7	A8	B9	PC6	I/O	-	-	TIM1_CH1, TIM3_CH1, TIM9_CH1, I2S2_MCK, USART6_TX, DCMIPP_D1/DCMI_D1/PSSI_D1, SDMMC1_D6, SDMMC2_D6, SDMMC1_D0DIR, HDP6	-
-	-	A9	A7	B8	C9	PC7	I/O	-	-	DBTRGIO, TIM16_CH1N, TIM3_CH2, TIM9_CH2, I2S3_MCK, USART6_RX, DCMIPP_D1/DCMI_D1/PSSI_D1, SDMMC1_D7, SDMMC2_D7, SDMMC1_D123DIR, HDP7	-
A8	D7	C6	C6	F6	D7	PC8	I/O	-	-	TRACED1, TIM3_CH3, I2C3_SMBA, UCPD1_FRSTX1, USART6_CK, DCMIPP_D2/DCMI_D2/PSSI_D2, SDMMC1_D0(boot), UART5_RTS, FMC_NE4, LCD_B0, HDP0	-
B8	C7	D6	B6	D5	C7	PC9	I/O	-	-	MCO2, TIM3_CH4, I2C3_SDA, AUDIOCLK, UCPD1_FRSTX2, USART6_RX, DCMIPP_D3/DCMI_D3/PSSI_D3, SDMMC1_D1, UART5_CTS, LCD_B3, HDP1	-
A9	D6	D8	A6	D6	A8	PC10	I/O	-	-	TIM1_BKIN, I3C2_SCL, I2C4_SCL, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, DCMIPP_D14/PSSI_D14, SDMMC1_D2, FMC_CLK, HDP2	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
B9	A8	C7	D6	B6	B8	PC11	I/O	-	-	I3C2_SDA, I2C4_SDA, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, DCMIPP_D4/DCMI_D4/PSSI_D4, SDMMC1_D3, HDP3	-
A10	B8	D7	E6	A6	C8	PC12	I/O	-	-	TRACED3, TIM1_CH4, TIM15_CH1, SPI6_SCK/I2S6_CK, SPI3_MOSI/I2S3_SDO, USART3_CK, DCMIPP_D9/DCMI_D9/PSSI_D9, SDMMC1_CK(boot), UART5_TX, FMC_NL, HDP4	-
E2	D2	C3	F4	H4	F3	PC13	I/O	-	-	HDP5	TAMP_IN1/TAMP_OUT2, RTC_OUT1/RTC_TS, WKUP3
C1	B1	B1	C1	E1	D1	PC14-OSC32_IN (OSC32_IN)	I/O	-	-	-	OSC32_IN
B1	C1	C1	B1	D1	C1	PC15-OSC32_OUT (OSC32_OUT)	I/O	-	-		OSC32_OUT
-	B12	A12	C11	B12	D13	PD0	I/O	-	-	TIM1_ETR, FDCAN1_RX, UART9_CTS, UART4_RX, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, FMC_A6, FMC_A22, EVENTOUT	-
B12	A12	B12	B11	D12	A14	PD1	I/O	-	-	FDCAN1_TX, UART4_TX, ETH1_MDC, FMC_A7, FMC_A23, EVENTOUT	-
-	C10	E10	D9	B10	C12	PD2	I/O	-	-	TRACED0, TIM1_CH3, SAI1_D1, ADF1_SDI0, MDF1_SDI1, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, TIM15_CH1N, MDIOS_MDC, SDMMC2_CK, FMC_A0, FMC_A16/FMC_CLE, HDP1	WKUP4

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	C12	A13	A12	D13	E13	PD3	I/O	-	-	I2C2_SMBA, USART10_RX, USART6_CTS, DCMIPP_D14/PSSI_D14, ETH1_PHY_INTN, FMC_A10, EVENTOUT	-
-	D13	B13	B12	B13	B15	PD4	I/O	-	-	TIM1_BKIN2, I2C2_SDA, SPI5_MISO, USART6_RTS, DCMIPP_D9/DCMI_D9/PSSI_D9, FMC_A11, EVENTOUT	TAMP_IN7/TAMP_OUT8
-	-	D14	C13	A15	D14	PD5	I/O	-	-	TIM1_CH4N, USART2_TX, DCMIPP_PIXCLK/DCMI_PIXCLK/PSSI_PDCK, SDMMC2_D7, FMC_D6/FMC_AD6, EVENTOUT	-
-	D10	A11	A10	A10	D12	PD6	I/O	-	-	TIM1_CH1, TIM15_CH2, SPI2_MISO/I2S2_SDI, FMC_A1, FMC_A17/FMC_ALE, HDP2	-
-	A11	B11	B10	F11	E12	PD7	I/O	-	-	TIM1_CH2, TIM15_CH1N, SPI2_MOSI/I2S2_SDO, SPI3_NSS/I2S3_WS, DCMIPP_D0/DCMI_D0/PSSI_D0, FMC_A2, FMC_A18, HDP3	-
C13	E11	D13	B13	B14	E14	PD8	I/O	-	-	USART3_TX, SPDIFRX1_IN1, DCMIPP_D11/DCMI_D11/PSSI_D11, FMC_NBL0, LCD_R7, EVENTOUT	TAMP_IN3/TAMP_OUT4
-	-	H12	E13	G14	H14	PD9	I/O	-	-	USART3_RX, DCMIPP_D11/DCMI_D11/PSSI_D11, FMC_SDCLK, LCD_R1, EVENTOUT	TAMP_IN5/TAMP_OUT6
-	B11	C11	C10	D11	A13	PD10	I/O	-	-	TRACECLK, TIM1_ETR, MDF1_CKI3, I2S1_MCK, UCPD1_FRSTX1, SPDIFRX1_IN2, SAI2_FS_B, FMC_A3, GFXTIM_TE, FMC_A19, HDP4	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	F13	F11	B14	A17	G14	PD11	I/O	-	-	I2C4_SDA, SPI2_MISO/I2S2_SDI, UCPD1_FRSTX1, DCMIPP_D15/PSSI_D15, SDMMC1_D0, FMC_D8/FMC_AD8, EVENTOUT	-
-	D11	E11	A11	A11	C13	PD12	I/O	-	-	SAI1_D3, MDF1_SDI3, UCPD1_FRSTX2, SPDIFRX1_IN3, DCMIPP_D12/DCMI_D12/PSSI_D12, ETH1_MDIO, FMC_A5, FMC_A21, HDP5	-
-	-	E14	F11	D16	C17	PD13	I/O	-	-	LPTIM1_CH1, TIM4_CH2, UCPD1_FRSTX2, UART9_RTS, DCMIPP_D13/DCMI_D13/PSSI_D13, SAI2_SCK_A, FMC_D4/FMC_AD4, LCD_R6, EVENTOUT	-
-	C13	D12	E11	F13	C14	PD14	I/O	-	-	I2C2_SCL, USART10_RX, FMC_A9, EVENTOUT	-
-	B13	C12	D11	A12	B14	PD15	I/O	-	-	I2C2_SDA, USART10_TX, FMC_A8, LCD_R2, EVENTOUT	-
A14	F12	F12	C14	A18	F16	PE0	I/O	-	-	LPTIM1_ETR, TIM4_ETR, LPTIM2_ETR, USART3_RX, UART8_RX, DCMIPP_D2/DCMI_D2/PSSI_D2, SAI2_MCLK_A, FMC_D9/FMC_AD9, EVENTOUT	TAMP_IN6/TAMP_OUT5
B14	F11	F13	D13	B18	F17	PE1	I/O	-	-	LPTIM1_IN2, LPTIM2_CH2, USART3_TX, UART8_TX, DCMIPP_D8/DCMI_D8/PSSI_D8, FMC_D10/FMC_AD10, EVENTOUT	-
B15	F10	F14	B15	B19	F15	PE2	I/O	-	-	TRACECLK, LPTIM5_IN1, SAI1_CK1, ADF1_CCK0, MDF1_CCK0, SPI4_SCK, SAI1_MCLK_A, UCPD1_FRSTX1, FMC_D11/FMC_AD11, TIM1_CH2N, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
C15	G13	G13	C15	C18	F14	PE3	I/O	-	-	TRACED0, LPTIM5_ETR, MDF1_CKI2, SAI1_SD_B, TIM15_BKIN, FMC_D12/FMC_AD12, EVENTOUT	-
-	-	-	-	-	D10	PE4	I/O	-	-	LPTIM1_IN1, SPI6_MISO/I2S6_SDI, USART10_RX, USART6_RTS, SPDIFRX1_IN1, DCMIPP_D5/DCMI_D5/PSSI_D5, SDMMC2_D3, FMC_RNB, LCD_G1, EVENTOUT	-
-	C9	D9	C8	D9	C11	PE5	I/O	-	-	TIM16_CH1N, TIM4_CH1, LPUART1_TX, I2C1_SCL, I3C1_SCL, FDCAN2_TX, USART1_TX(boot), DCMIPP_D5/DCMI_D5/PSSI_D5, UART5_TX, FMC_SDNE1, HDP6	-
-	-	A10	D8	B9	D11	PE6	I/O	-	-	TIM17_CH1N, TIM4_CH2, LPUART1_RX, I2C1_SDA, I3C1_SDA, USART1_RX(boot), DCMIPP_VSYNC/DCMI_VSYNC/PSSI_RDY, DCMIPP_D1/DCMI_D1/PSSI_D1, UART5_TX, FMC_SDCKE1, HDP7	-
A12	C11	D11	D10	B11	B13	PE7	I/O	-	-	TIM1_ETR, MDF1_CKI0, UART7_RX, SAI2_SD_B, FMC_A4, FMC_A20, EVENTOUT	-
D12	D12	C13	C12	A13	A15	PE8	I/O	-	-	TIM1_CH1N, MDF1_SDI0, USART3_TX, UART7_TX, DCMIPP_D4/DCMI_D4/PSSI_D4, FMC_A12, EVENTOUT	-
A13	E13	B14	D12	F14	A16	PE9	I/O	-	-	TIM1_CH1, MDF1_CKI4, UART7_RTS, FMC_A14/FMC_BA0, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
B13	E12	C14	A13	D14	B16	PE10	I/O	-	-	TRACECLK, TIM1_CH2N, MDF1_SDI4, USART3_RX, UART7_CTS, DCMIPP_D3/DCMI_D3/PSSI_D3, FMC_A15/FMC_BA1, EVENTOUT	-
-	A9	B9	A8	D8	E11	PE11	I/O	-	-	TIM1_CH2, MDF1_CKI5, SPI4_NSS, FDCAN3_TX, SAI2_SD_B, FMC_SDNWE, LCD_VSYNC, EVENTOUT	-
B11	B10	D10	C9	D10	B12	PE12	I/O	-	-	TIM1_CH3N, MDF1_SDI5, SPI4_SCK, FDCAN3_RX, SAI2_SCK_B, FMC_NRAS, EVENTOUT	-
A11	A10	C10	B9	A9	A11	PE13	I/O	-	-	TIM1_CH3, ADF1_CCK0, I2C4_SCL, SPI4_MISO, SAI2_FS_B, FMC_NCAS, EVENTOUT	-
D10	B9	C9	B8	F9	B11	PE14	I/O	-	-	TIM1_CH4, GFXTIM_FCKCAL, ADF1_CCK1, I2C4_SDA, SPI4_MOSI, SAI2_MCLK_B, FMC_SDNE0, GFXTIM_LCKCAL, FMC_NWE, EVENTOUT	-
D11	D9	B10	A9	F10	A12	PE15	I/O	-	-	TIM1_BKIN, GFXTIM_LCKCAL, I2C4_SMBA, SPI5_SCK, USART10_CK, USART2_CK, SDMMC1_D0, FMC_SDCKE0, GFXTIM_FCKCAL, EVENTOUT	-
-	-	-	N4	U3	R3	PF0	I/O	-	-	LPTIM5_OUT, TIM4_CH4, UCPD1_FRSTX2, UART9_TX, UART8_RTS, DCMIPP_D9/DCMI_D9/PSSI_D9, ETH1_MII_TX_CLK, ETH1_RGMII_GTX_CLK, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	-	-	N2	U1	P4	PF1	I/O	-	-	LPTIM1_CH2, TIM4_CH3, LPTIM2_CH1, UCPD1_FRSTX1, UART9_RX, UART8_CTS, DCMIPP_D7/DCMI_D7/PSSI_D7, ETH1_TX_ER, EVENTOUT	-
L1	K1	K1	L3	P4	N4	PF2	I/O	-	-	TIM1_CH3N, SPI2_SCK/I2S2_CK, FDCAN3_TX, USART2_CTS/USART2_NSS, ETH1_RGMII_CLK125, FMC_NWAIT, LCD_B1, EVENTOUT	-
L4	J4	J5	L2	P1	M2	PF3	I/O	-	-	FDCAN3_RX, USART2_RTS, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, ETH1_PPS_OUT, FMC_NL, LCD_R4, EVENTOUT	ADC1_INP16
K1	J1	J1	K1	M1	L2	PF4	I/O	-	-	TIM5_ETR, LPTIM3_CH2, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS/I2S6_WS, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, ETH1_MDIO, LCD_R3, HDP4	ADC1_INP18
K3	J3	J4	L1	N4	M3	PF5	I/O	-	-	TIM1_ETR, LPTIM2_IN2, USART3_CTS/USART3_NSS, DCMIPP_D6/DCMI_D6/PSSI_D6, SAI2_SD_A, ETH1_CLK, FMC_NE3, LCD_G0, EVENTOUT	-
-	-	J2	K2	M4	L5	PF6	I/O	-	-	TIM2_CH4, TIM5_CH4, LPTIM3_CH1, TIM15_CH2, I2S6_MCK, SPI4_RDY, USART2_RX(boot), GFXTIM_LCKCAL, SPI5_RDY, SPI1_RDY, ETH1_MII_COL, GFXTIM_FCKCAL, TIM1_CH3, LCD_DE, HDP3	ADC1_INP15, ADC2_INP15

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
M2	K4	K4	M2	R2	M1	PF7	I/O	-	-	TIM1_CH2N, TIM3_CH3, TIM9_CH1, SPI1_SCK/I2S1_CK, UART4_CTS, ETH1_MII_RX_CLK/ETH1_RMII_REF_CLK/ETH1_RGMII_RX_CLK, GFXTIM_TE, [RNG_S1], LCD_VSYNC, HDP0	ADC1_INP9, ADC2_INP9, ADC1_INN5, ADC2_INN5
N1	L1	L1	M3	R4	N3	PF8	I/O	-	-	TRACECLK, UART9_TX, ETH1_MII_RXD2/ETH1_RGMII_RXD2, FMC_NWE, LCD_R6, EVENTOUT	-
-	-	-	M4	T2	P1	PF9	I/O	-	-	TRACED0, ETH1_MII_RXD3/ETH1_RGMII_RXD3, LCD_HSYNC, EVENTOUT	-
K2	J2	J3	K3	M2	L4	PF10	I/O	-	-	TIM16_BKIN, SAI1_D3, MDF1_SDI3, UCPD1_FRSTX1, UART7_RX, DCMIPP_D11/DCMI_D11/PSSI_D11, DCMIPP_D15/PSSI_D15, ETH1_MII_RX_DV/ETH1_RMII_CRS_DV/ETH1_RGMII_RX_CTL, LCD_R1, EVENTOUT	-
N2	L2	L2	N1	T1	P3	PF11	I/O		-	SPI5_MOSI, DCMIPP_D15/PSSI_D15, SAI2_SD_B, ETH1_MII_TX_EN/ETH1_RMII_TX_EN/ETH1_RGMII_TX_CTL, LCD_B0, EVENTOUT	ADC1_INP2
P1	L3	L3	N3	U2	T1	PF12	I/O	-	-	USART1_RX, SPI5_MISO, DCMIPP_D13/DCMI_D13/PSSI_D13, ETH1_MII_TXD0/ETH1_RMII_TXD0/ETH1_RGMII_TXD0, EVENTOUT	ADC1_INP6, ADC1_INN2
N3	L4	M2	P1	V1	R2	PF13	I/O	-	-	USART1_TX, SPI5_NSS, DCMIPP_D10/DCMI_D10/PSSI_D10, ETH1_MII_TXD1/ETH1_RMII_TXD1/ETH1_RGMII_TXD1, EVENTOUT	ADC2_INP2

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
L2	K2	K2	L4	P2	N2	PF14	I/O	-	-	TIM2_CH2, USART1_CTS, SPI5_MOSI, ETH1_MII_RXD0/ETH1_RMII_RXD0/ETH1_RGMII_RXD0, LCD_G0, EVENTOUT	ADC2_INP6, ADC2_INN2
M1	K3	K3	M1	R1	N1	PF15	I/O	-	-	USART1_RTS, SPI5_SCK, ETH1_MII_RXD1/ETH1_RMII_RXD1/ETH1_RGMII_RXD1, LCD_G1, EVENTOUT	-
-	-	M12	P15	T16	R13	PG0	I/O	-	-	TIM1_CH4N, TIM12_CH1, UART9_RX, LCD_VSYNC, ETH1_PHY_INTN, LCD_R0, EVENTOUT	-
-	-	M9	R10	T11	R9	PG1	I/O	-	-	TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS, DCMIPP_PIXCLK/DCMI_PIXCLK/PSSI_PDCK, TIM13_CH1, FMC_A19, LCD_G1, EVENTOUT	-
M14	N10	N11	P12	W14	T11	PG2	I/O	-	-	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, USART3_RTS, UART7_CTS, DCMIPP_D6/DCMI_D6/PSSI_D6, SAI2_MCLK_B, TIM14_CH1, FMC_A21, LCD_R0, EVENTOUT	-
-	-	-	R2	T5	R1	PG3	I/O	-	-	TRACED1, USART2_TX, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, ETH1_MII_TXD2/ETH1_RGMII_TXD2, EVENTOUT	-
-	-	-	P2	T4	P2	PG4	I/O	-	-	TIM1_BKIN2, ETH1_MII_TXD3/ETH1_RGMII_TXD3, LCD_B0, EVENTOUT	-
-	-	-	K5	N2	M4	PG5	I/O	-	-	TIM1_ETR, USART2_CTS/USART2_NSS, ETH1_MII_RX_ER, LCD_B1, EVENTOUT	-
-	-	-	K4	N1	L3	PG6	I/O	-	-	TIM17_BKIN, USART6_CK, DCMIPP_D12/DCMI_D12/PSSI_D12, ETH1_MII_CRS, LCD_B3, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	-	-	-	-	L1	PG7	I/O	-	-	TRACECLK, SAI1_MCLK_A, USART6_CK, DCMIPP_D13/DCMI_D13/PSSI_D13, ETH1_PHY_INTN, EVENTOUT	-
-	-	L12	N14	V17	T14	PG8	I/O	-	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, USART1_RX, SPI2_MOSI/I2S2_SDO, SAI1_SCK_B, UART4_CTS, SDMMC2_D1, FMC_A20, LCD_G7, HDP7	PVD_IN
-	-	-	R14	V16	T13	PG9	I/O	-	(1)	FMC_D8/FMC_AD8, LCD_R7, EVENTOUT	-
P15	N9	N10	P11	T12	T10	PG10	I/O	-	-	TIM1_CH1N, LPTIM2_CH1, SPI2_SCK/I2S2_CK, FDCAN2_TX, USART3_CTS/USART3_NSS, DCMIPP_D2/DCMI_D2/PSSI_D2, UART5_TX, FMC_A16/FMC_CLE, LCD_G4, HDP5	-
-	-	-	P14	W16	U13	PG11	I/O	-	(1)	UART7_RX, ETH1_MDC, LCD_R6, EVENTOUT	-
-	-	N9	P10	V11	T9	PG12	I/O	-	-	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, FMC_A18, LCD_G0, EVENTOUT	-
R13	K9	P9	N10	W11	U9	PG13	I/O	-	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, USART3_RTS, DCMIPP_D12/DCMI_D12/PSSI_D12, SAI2_FS_A, FMC_NE1, LCD_DE, EVENTOUT	-
P9	K6	L5	M8	T7	P6	PG14	I/O	-	-	TRACED1, LPTIM1_ETR, TIM8_CH4, SPI6_MOSI/I2S6_SDO, USART10_RTS, USART6_TX, USART2_RTS, DCMIPP_D11/DCMI_D11/PSSI_D11, FMC_NCE, FMC_NE2, LCD_B1, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	-	M5	M7	W8	R6	PG15	I/O	-	-	TIM1_CH4, SPI5_RDY, SPI4_RDY, USART3_CK, DCMIPP_D4/DCMI_D4/PSSI_D4, SPI1_RDY, ETH1_MII_RX_CLK/ETH1_RMII_REF_CLK, FMC_CLK, LCD_B0, EVENTOUT	ADC1_INP7, ADC2_INP7, ADC1_INN3, ADC2_INN3
A7	B7	B7	A5	A5	A7	PH0-OSC_IN(PH0)	I/O	-	-	EVENTOUT	OSC_IN
B7	A7	A7	B5	B5	B7	PH1-OSC_OUT(PH1)	I/O	-	-	EVENTOUT	OSC_OUT
B10	C8	E6	E7	D7	E7	PH2	I/O	-	-	TRACED2, TIM1_ETR, TIM3_ETR, TIM15_BKIN, FDCAN1_TX, DCMIPP_D11/DCMI_D11/PSSI_D11, SDMMC1_CMD(boot), UART5_RX, FMC_NE3, EVENTOUT	-
-	-	-	-	-	B1	PH3	I/O	-	(1)	TRACECLK, UART7_TX, LCD_B4, EVENTOUT	-
-	-	-	-	-	F4	PH4	I/O	-	(1)	UART7_TX, LCD_R4, EVENTOUT	TAMP_IN4/TAMP_OUT3
-	-	-	-	-	F5	PH5	I/O	-	-	SPI5_SCK, ETH1_MDC, EVENTOUT	-
-	-	-	-	-	B2	PH6	I/O	-	-	SPI5_NSS, LCD_B5, EVENTOUT	-
-	-	-	-	-	D2	PH7	I/O	-	(1)	I3C2_SCL, SPI5_MOSI, EVENTOUT	-
-	-	-	-	-	C2	PH8	I/O		(1)	I3C2_SDA, SPI5_MISO, EVENTOUT	-
-	-	C8	D7	B7	D8	PH9	I/O	-	-	TIM16_CH1, TIM4_CH3, USART3_CK, I2C1_SCL, FDCAN1_RX, I3C1_SCL, UART4_RX, DCMIPP_D6/DCMI_D6/PSSI_D6, SDMMC1_D4, SDMMC2_D4, SDMMC1_CKIN, FMC_D9/FMC_AD9, HDP0	-
J15	J13	M13	M13	R19	P17	PN0	I/O	-	-	XSPIM_P2_DQS0(boot), FMC_A25, EVENTOUT	-
D14	H13	P13	K12	P16	R17	PN1	I/O	-	-	XSPIM_P2_NCS1(boot), FMC_A24, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
H15	J11	L13	L14	T19	T17	PN2	I/O	-	-	XSPIM_P2_IO0(boot), FMC_A23, EVENTOUT	-
K15	H12	N13	M15	P19	R15	PN3	I/O	-	-	XSPIM_P2_IO1(boot), FMC_A22, EVENTOUT	-
E14	L12	J13	J14	V19	N17	PN4	I/O	-	-	XSPIM_P2_IO2(boot), EVENTOUT	-
F15	L13	K14	K13	U18	R16	PN5	I/O	-	-	XSPIM_P2_IO3(boot), EVENTOUT	-
G15	K12	K12	K15	U19	P15	PN6	I/O	-	-	XSPIM_P2_CLK(boot), EVENTOUT	-
F14	K11	K13	K14	R16	T16	PN7	I/O	-	-	XSPIM_P2_NCLK(boot), EVENTOUT	-
E15	M13	J14	J15	V18	P16	PN8	I/O	-	-	XSPIM_P2_IO4(boot), EVENTOUT	-
G14	K13	L14	L13	T18	T15	PN9	I/O	-	-	XSPIM_P2_IO5(boot), DCMIPP_D5/DCMI_D5/PSSI_D5, EVENTOUT	-
H14	J12	M14	L15	R18	U15	PN10	I/O	-	-	XSPIM_P2_IO6(boot), LCD_B4, EVENTOUT	-
J14	H11	N14	M14	P18	U16	PN11	I/O	-	-	XSPIM_P2_IO7(boot), LCD_B6, EVENTOUT	-
K14	M12	J12	L12	W18	P14	PN12	I/O	-	-	XSPIM_P2_NCS2, EVENTOUT	-
-	-	-	G12	F16	M17	PO0	I/O	-	-	XSPIM_P1_NCS1, FMC_A22, EVENTOUT	-
-	-	-	F12	N14	K16	PO1	I/O	-	-	XSPIM_P1_NCS2, FMC_A23, EVENTOUT	-
-	-	-	H15	G18	K17	PO2	I/O	-	-	XSPIM_P1_DQS0, FMC_A24, LCD_B7, EVENTOUT	-
-	-	-	-	E18	M16	PO3	I/O	-	-	XSPIM_P1_DQS1, FMC_A25, LCD_G3, EVENTOUT	-
-	-	-	F15	J18	N16	PO4	I/O	-	-	XSPIM_P1_CLK, LCD_B4, FMC_A24, FMC_NBL2, EVENTOUT	-
-	-	-	F14	G16	K15	PO5	I/O	-	-	XSPIM_P1_NCLK, FMC_A25, FMC_NBL3, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	-	-	G14	H18	G17	PP0	I/O	-	-	XSPIM_P1_IO0, FMC_D16, EVENTOUT	-
-	-	-	H13	F18	H16	PP1	I/O	-	-	XSPIM_P1_IO1, FMC_D17, EVENTOUT	-
-	-	-	E14	K18	J17	PP2	I/O	-	-	XSPIM_P1_IO2, FMC_D18, EVENTOUT	-
-	-	-	F13	K19	J16	PP3	I/O	-	-	XSPIM_P1_IO3, FMC_D19, EVENTOUT	-
-	-	-	E15	L19	H15	PP4	I/O	-	-	XSPIM_P1_IO4, FMC_D20, EVENTOUT	-
-	-	-	G15	J19	J14	PP5	I/O	-	-	XSPIM_P1_IO5, FMC_D21, EVENTOUT	-
-	-	-	G13	H19	G16	PP6	I/O	-	-	XSPIM_P1_IO6, FMC_D22, EVENTOUT	-
-	-	-	H14	G19	G15	PP7	I/O	-	-	XSPIM_P1_IO7, FMC_D23, EVENTOUT	-
-	-	-	-	F19	L16	PP8	I/O	-	-	SPI2_MISO, XSPIM_P1_IO8, FMC_D24, EVENTOUT	-
-	-	-	-	E19	N14	PP9	I/O	-	-	SPI2_MOSI, XSPIM_P1_IO9, FMC_D25, EVENTOUT	-
-	-	-	-	D18	N15	PP10	I/O	-	-	XSPIM_P1_IO10, ETH1_MDC, FMC_D26, EVENTOUT	-
-	-	-	-	N19	L15	PP11	I/O		-	XSPIM_P1_IO11, FMC_D27, EVENTOUT	-
-	-	-	-	N18	J15	PP12	I/O	-	-	XSPIM_P1_IO12, FMC_D28, EVENTOUT	-
-	-	-	-	M19	K14	PP13	I/O	-	-	XSPIM_P1_IO13, FMC_D29, EVENTOUT	-
-	-	-	-	M18	L17	PP14	I/O	-	-	XSPIM_P1_IO14, FMC_D30, EVENTOUT	-
-	-	-	-	L18	H17	PP15	I/O	-	-	XSPIM_P1_IO15, FMC_D31, LCD_B5, EVENTOUT	-
-	-	-	-	-	E5	PQ0	I/O	-	-	TRACECLK, TIM8_ETR, EVENTOUT	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	-	-	-	-	E4	PQ1	I/O	-	-	TIM8_BKIN, EVENTOUT	-
-	-	-	-	-	E3	PQ2	I/O	-	-	TIM8_BKIN2, SAI2_SCK_B, EVENTOUT	-
-	-	-	-	-	D3	PQ3	I/O	-	-	TIM8_CH1, EVENTOUT	-
-	-	-	-	-	D4	PQ4	I/O	-	-	TIM8_CH1N, EVENTOUT	-
-	-	-	-	-	D5	PQ5	I/O	-	-	TIM8_CH2, SAI2_FS_B, EVENTOUT	-
-	-	-	-	-	A2	PQ6	I/O	-	-	TIM8_CH2N, SAI2_SD_B, EVENTOUT	-
-	-	-	-	-	G5	PQ7	I/O	-	-	TIM8_CH3, SAI2_MCLK_B, EVENTOUT	TAMP_IN2/TAMP_OUT1
D1	C2	C2	D1	F1	E1	VBAT	S	-	-	-	-
K4	J5	L4	J5	M6	M5	VDDA18PLL	S	-	-	-	-
-	-	-	J11	H16	L13	VDDIO2	S	-	-	-	-
-	-	-	J12	J16	L14	VDDIO2	S	-	-	-	-
-	-	-	-	K16	M14	VDDIO2	S	-	-	-	-
-	-	-	-	L16	M15	VDDIO2	S	-	-	-	-
K12	H10	J10	K11	M14	N13	VDDIO3	S	-	-	-	-
L12	J10	J11	L11	M16	P13	VDDIO3	S	-	-	-	-
D8	D8	E8	E9	F7	E8	VDDIO4	S	-	-	-	-
-	-	E9	E10	F8	F8	VDDIO4	S	-	-	-	-
-	-	-	-	-	E9	VDDIO5	S	-	-	-	-
-	-	-	-	-	F9	VDDIO5	S	-	-	-	-
P8	L6	N6	N6	W6	R4	VDDCSI	S	-	-	-	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
R7	M5	P5	P7	V6	R5	VDDA18CSI	S	-	-	-	-
F1	E1	E1	F1	H1	G1	VDDA18PMU	S	-	-	-	-
F2	E2	E2	F2	H2	F2	VSSAPMU	S	-	-	-	-
J1	H1	H1	J1	L1	K1	VDDSMPS	S	-	-	-	-
G1	F1	F1	G1	J1	H1	VSSSMPS	S	-	-	-	-
J2	H2	H2	J2	L2	K2	VDDSMPS	S	-	-	-	-
G2	F2	F2	G2	J2	H2	VSSSMPS	S	-	-	-	-
J3	H3	H3	J3	L3	K3	VDDSMPS	S	-	-	-	-
G3	F3	F3	G3	J3	H3	VSSSMPS	S	-	-	-	-
-	H4	H4	J4	L4	K4	VDDSMPS	S	-	-	-	-
-	F4	F4	G4	J4	H4	VSSSMPS	S	-	-	-	-
-	-	-	-	L5	K5	VDDSMPS	S	-	-	-	-
-	-	-	-	J5	H5	VSSSMPS	S	-	-	-	-
-	-	-	-	-	K6	VDDSMPS	S	-	-	-	-
-	-	-	-	-	H6	VSSSMPS	S	-	-	-	-
E1	D1	D1	E1	G1	F1	V08CAP	S	-	-	-	-
H1	G1	G1	H1	K1	J1	VLXSMPS	S	-	-	-	-
H2	G2	G2	H2	K2	J2	VLXSMPS	S	-	-	-	-
H3	G3	G3	H3	K3	J3	VLXSMPS	S	-	-	-	-
-	G4	G4	H4	K4	J4	VLXSMPS	S	-	-	-	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	-	-	-	K5	J5	VLXSMPS	S	-	-	-	-
-	-	-	-	-	J6	VLXSMPS	S	-	-	-	-
D4	C4	D4	C3	D4	C5	VDDA18USB	S	-	-	-	-
B6	C5	A4	B3	C3	A4	VDD33USB	S	-	-	-	-
R3	L5	M3	M6	P6	N6	VDDA18ADC	S	-	-	-	-
P3	K5	M4	M5	N6	M6	VSSA	S	-	-	-	-
E4	D5	E5	E5	H6	F6	VDDA18AON	S	-	-	-	-
F4	E5	F5	F5	G6	G6	VSSAON	S	-	-	-	-
F12	E9	G10	H11	J14	G13	VDD	S	-	-	-	-
G12	G9	G11	H12	K14	H12	VDD	S	-	-	-	-
H12	J9	G12	J13	L14	H13	VDD	S	-	-	-	-
-	-	-	-	-	J12	VDD	S	-	-	-	-
-	-	-	-	-	J13	VDD	S	-	-	-	-
-	-	-	-	-	K13	VDD	S	-	-	-	-
M5	E7	K6	L6	P7	L6	VDDCORE	S	-	-	-	-
M6	F6	K7	L7	P9	L12	VDDCORE	S	-	-	-	-
M7	F8	K8	L8	P10	M7	VDDCORE	S	-	-	-	-
M8	G5	K9	L9	P11	M9	VDDCORE	S	-	-	-	-
M9	G7	L7	-	P13	M11	VDDCORE	S	-	-	-	-
-	H6	-	-	-	N8	VDDCORE	S	-	-	-	-

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Table 16. Pin description (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223	VFBGA264						
-	H8	-	-	-	N10	VDDCORE	S	-	-	-	-
-	J7	-	-	-	N12	VDDCORE	S	-	-	-	-
-	-	-	-	-	P11	VDDCORE	S	-	-	-	-
A15	A13	A14	A15	A19	A17	VSS	S	-	-	-	-
D9	E6	E7	E8	F12	F7	VSS	S	-	-	-	-
J12	E8	F10	G11	H14	F10	VSS	S	-	-	-	-
M4	F5	H10	L5	N16	F11	VSS	S	-	-	-	-
M10	F7	H11	L10	P8	F12	VSS	S	-	-	-	-
M12	F9	K5	R1	P12	G12	VSS	S	-	-	-	-
R1	G6	K10	R15	P14	K12	VSS	S	-	-	-	-
R15	G8	P1	-	W1	M8	VSS	S	-	-	-	-
-	H5	P14	-	W19	M10	VSS	S	-	-	-	-
-	H7	-	-	-	M12	VSS	S	-	-	-	-
-	H9	-	-	-	M13	VSS	S	-	-	-	-
-	J6	-	-	-	N5	VSS	S	-	-	-	-
-	J8	-	-	-	N7	VSS	S	-	-	-	-
-	N1	-	-	-	N9	VSS	S	-	-	-	-
-	N13	-	-	-	N11	VSS	S	-	-	-	-
-	-	-	-	-	U1	VSS	S	-	-	-	-
-	-	-	-	-	U17	VSS	S	-	-	-	-

1. Power supply is VDD.

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4.3 Alternate functions

Table 17. Alternate functions: AF0 to AF7

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM9_CH1	TIM15_BKIN	SPI6_NSS/I2S6_WS		USART2_CTS/U SART2_NSS
	PA1	-	TIM2_CH2	TIM5_CH2	LPTIM3_IN1	TIM15_CH1N	-	-	USART2_RTS
	PA2	-	TIM2_CH3	TIM5_CH3	LPTIM3_IN2	TIM15_CH1	-	-	USART2_TX
	PA3	-	TIM16_CH1	-	-	-	SPI5_NSS	SAI1_SD_B	-
	PA4	-	-	-	-	-	SPI5_MOSI	-	USART6_RX
	PA5	PWR_CSTOP	TIM2_CH1	TIM2_ETR	TIM9_CH2	I3C1_SCL	SPI1_SCK/I2S1_CK	-	-
	PA6	BOOT1	TIM1_BKIN	TIM3_CH1	LPTIM3_ETR	I3C1_SDA	SPI1_MISO/ I2S1_SDI	-	-
	PA7	-	TIM1_CH1N	TIM3_CH2	-	-	SPI1_MOSI/ I2S1_SDO	-	USART1_RX
	PA8	MCO1	TIM1_CH1	I3C2_SCL	-	I2C3_SCL	-	-	USART1_CK
	PA9	-	TIM1_CH2	I3C2_SDA	LPUART1_TX	I2C3_SDA	SPI2_SCK/I2S2_CK	-	USART1_TX
	PA10	PWR_CSLEEP	TIM1_CH3	-	LPUART1_RX	-	-	-	USART1_RX
	PA11	-	TIM1_CH4	-	LPUART1_CTS	-	SPI2_NSS/I2S2_WS	FDCAN1_RX	USART1_CTS/U SART1_NSS
	PA12	-	TIM1_ETR	-	LPUART1_RTS	-	SPI2_SCK/I2S2_CK	FDCAN1_TX	USART1_RTS
	PA13	JTMS/SWDIO	-	-	-	-	-	-	-
	PA14	JTCK/SWCLK	-	-	-	-	-	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/ I2S3_WS	SPI6_NSS/ I2S6_WS

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port B	PB0	TRACED1	TIM1_CH4	SAI1_D2	ADF1_SDI0	MDF1_SDI2	SPI4_NSS	SAI1_FS_A	TIM15_CH1N
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM9_CH2	-	-	FDCAN2_TX	USART2_TX
	PB2	RTC_OUT2	TIM1_CH1	SAI1_D1	ADF1_SDI0	MDF1_SDI1	-	SAI1_SD_A	SPI3_MOSI/ I2S3_SDO
	PB3	TRACECLK	TIM1_CH4N	GFXTIM_FCK CAL	-	MDF1_CKI1	-	-	USART1_CK
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	LPTIM4_ETR	-	SPI1_MISO/ I2S1_SDI	SPI3_MISO/ I2S3_SDI	SPI2_NSS/ I2S2_WS
	PB5	JTDO/ TRACESWO	TIM17_BKIN	TIM3_CH2	LPTIM4_OUT	I2C1_SMBA	SPI1_MOSI/ I2S1_SDO	FDCAN2_RX	SPI3_MOSI/ I2S3_SDO
	PB6	TRACED2	-	SAI1_CK2	ADF1_CCK1	MDF1_CCK1	SPI4_MISO	SAI1_SCK_A	TIM15_CH1
	PB7	TRACED3	TIM1_BKIN2	SAI1_D1	ADF1_SDI0	MDF1_SDI1	SPI4_MOSI	SAI1_SD_A	TIM15_CH2
	PB8	-	-	-	-	-	SPI1_MISO/ I2S1_SDI	-	USART6_RX
	PB9	-	LPTIM1_IN2	-	-	-	SPI1_SCK/I2S1_CK	USART10_TX	-
	PB10	-	TIM2_CH3	I3C2_SCL	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	-	USART3_TX
	PB11	-	TIM2_CH4	I3C2_SDA	LPTIM2_ETR	I2C2_SDA	-	-	USART3_RX
	PB12	-	TIM1_BKIN	-	LPTIM2_IN2	I2C2_SMBA	SPI2_NSS/I2S2_WS	FDCAN2_RX	USART3_CK
	PB13	TRACED0	LPTIM1_CH1	TIM8_CH3N	-	-	SPI6_SCK/I2S6_CK	USART10_CTS/ USART10_NSS	USART6_CTS/U SART6_NSS
	PB14	-	LPTIM1_CH2	TIM8_CH4N	-	-	-	USART10_CK	USART6_CTS/U SART6_NSS
	PB15	-	-	-	-	-	SPI6_NSS/I2S6_WS	-	USART6_RTS

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port C	PC0	-	TIM2_CH2	-	LPTIM4_IN1	MDF1_CKI1	SPI1_SCK/I2S1_CK	SPI3_SCK/ I2S3_CK	-
	PC1	-	TIM17_CH1	TIM4_CH4	-	I2C1_SDA	SPI2_NSS/I2S2_WS	FDCAN1_TX	I3C1_SDA
	PC2	-	-	SAI1_D1	ADF1_SDI0	MDF1_SDI1	SPI3_MOSI/ I2S3_SDO	SAI1_SCK_A	USART2_RX
	PC3	-	-	-	-	-	SPI1_MOSI/ I2S1_SDO	-	USART2_CK
	PC4	-	TIM1_CH2N	TIM12_CH1	LPTIM2_CH2	USART1_TX	SPI2_MISO/ I2S2_SDI	-	USART3_RTS
	PC5	-	-	-	-	-	SPI1_NSS/I2S1_WS	-	-
	PC6	-	TIM1_CH1	TIM3_CH1	TIM9_CH1	-	I2S2_MCK	-	USART6_TX
	PC7	DBTRGIO	TIM16_CH1N	TIM3_CH2	TIM9_CH2	-	-	I2S3_MCK	USART6_RX
	PC8	TRACED1	-	TIM3_CH3	-	I2C3_SMBA	-	UCPD1_FRSTX1	USART6_CK
	PC9	MCO2	-	TIM3_CH4	-	I2C3_SDA	AUDIOCLK	UCPD1_FRSTX2	USART6_RX
	PC10	-	TIM1_BKIN	I3C2_SCL	-	I2C4_SCL	-	SPI3_SCK/ I2S3_CK	USART3_TX
	PC11	-	-	I3C2_SDA	-	I2C4_SDA	-	SPI3_MISO/ I2S3_SDI	USART3_RX
	PC12	TRACED3	TIM1_CH4	-	-	TIM15_CH1	SPI6_SCK/I2S6_CK	SPI3_MOSI/ I2S3_SDO	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port D	PD0	-	TIM1_ETR	-	-	-	-	FDCAN1_RX	UART9_CTS
	PD1	-	-	-	-	-	-	FDCAN1_TX	-
	PD2	TRACED0	TIM1_CH3	SAI1_D1	ADF1_SDI0	MDF1_SDI1	SPI2_MOSI/ I2S2_SDO	SAI1_SD_A	TIM15_CH1N
	PD3	-	-	-	-	I2C2_SMBA	-	USART10_RX	USART6_CTS
	PD4	-	TIM1_BKIN2	-	-	I2C2_SDA	SPI5_MISO	-	USART6_RTS
	PD5	-	TIM1_CH4N	-	-	-	-	-	USART2_TX
	PD6	-	TIM1_CH1	-	-	TIM15_CH2	SPI2_MISO/ I2S2_SDI	-	-
	PD7	-	TIM1_CH2	-	-	TIM15_CH1N	SPI2_MOSI/ I2S2_SDO	SPI3_NSS/I2S3_ WS	-
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	TRACECLK	TIM1_ETR	-	-	MDF1_CKI3	I2S1_MCK	UCPD1_FRSTX1	-
	PD11	-	-	-	-	I2C4_SDA	SPI2_MISO/ I2S2_SDI	UCPD1_FRSTX1	-
	PD12	-	-	SAI1_D3	-	MDF1_SDI3	-	UCPD1_FRSTX2	-
	PD13	-	LPTIM1_CH1	TIM4_CH2	-	-	-	UCPD1_FRSTX2	UART9_RTS
	PD14	-	-	-	-	I2C2_SCL	-	USART10_RX	-
	PD15	-	-	-	-	I2C2_SDA	-	USART10_TX	-

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port E	PE0	-	LPTIM1_ETR	TIM4_ETR	LPTIM2_ETR	-	-	-	USART3_RX
	PE1	-	LPTIM1_IN2	-	LPTIM2_CH2	-	-	-	USART3_TX
	PE2	TRACECLK	LPTIM5_IN1	SAI1_CK1	ADF1_CCK0	MDF1_CCK0	SPI4_SCK	SAI1_MCLK_A	UCPD1_FRSTX1
	PE3	TRACED0	LPTIM5_ETR	-	-	MDF1_CKI2	-	SAI1_SD_B	TIM15_BKIN
	PE4	-	LPTIM1_IN1	-	-	-	SPI6_MISO/ I2S6_SDI	USART10_RX	USART6_RTS
	PE5	-	TIM16_CH1N	TIM4_CH1	LPUART1_TX	I2C1_SCL	I3C1_SCL	FDCAN2_TX	USART1_TX
	PE6	-	TIM17_CH1N	TIM4_CH2	LPUART1_RX	I2C1_SDA	I3C1_SDA	-	USART1_RX
	PE7	-	TIM1_ETR	-	-	MDF1_CKI0	-	-	-
	PE8	-	TIM1_CH1N	-	-	MDF1_SDI0	-	-	USART3_TX
	PE9	-	TIM1_CH1	-	-	MDF1_CKI4	-	-	-
	PE10	TRACECLK	TIM1_CH2N	-	-	MDF1_SDI4	-	-	USART3_RX
	PE11	-	TIM1_CH2	-	-	MDF1_CKI5	SPI4_NSS	FDCAN3_TX	-
	PE12	-	TIM1_CH3N	-	-	MDF1_SDI5	SPI4_SCK	FDCAN3_RX	-
	PE13	-	TIM1_CH3	-	ADF1_CCK0	I2C4_SCL	SPI4_MISO	-	-
	PE14	-	TIM1_CH4	GFXTIM_FCK CAL	ADF1_CCK1	I2C4_SDA	SPI4_MOSI	-	-
	PE15	-	TIM1_BKIN	GFXTIM_LCK CAL	-	I2C4_SMBA	SPI5_SCK	USART10_CK	USART2_CK

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port F	PF0	-	LPTIM5_OUT	TIM4_CH4	-	-	-	UCPD1_FRSTX2	UART9_TX
	PF1	-	LPTIM1_CH2	TIM4_CH3	LPTIM2_CH1	-	-	UCPD1_FRSTX1	UART9_RX
	PF2	-	TIM1_CH3N	-	-	-	SPI2_SCK/I2S2_CK	FDCAN3_TX	USART2_CTS/ USART2_NSS
	PF3	-	-	-	-	-	-	FDCAN3_RX	USART2_RTS
	PF4	-	-	TIM5_ETR	LPTIM3_CH2	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I 2S3_WS	USART2_CK
	PF5	-	TIM1_ETR	-	LPTIM2_IN2	-	-	-	USART3_CTS/ USART3_NSS
	PF6	-	TIM2_CH4	TIM5_CH4	LPTIM3_CH1	TIM15_CH2	I2S6_MCK	SPI4_RDY	USART2_RX
	PF7	-	TIM1_CH2N	TIM3_CH3	TIM9_CH1	-	SPI1_SCK/I2S1_CK	-	-
	PF8	TRACECLK	-	-	-	-	-	-	UART9_TX
	PF9	TRACED0	-	-	-	-	-	-	-
	PF10	-	TIM16_BKIN	SAI1_D3	-	MDF1_SDI3		UCPD1_FRSTX1	-
	PF11	-	-	-	-	-	SPI5_MOSI	-	-
	PF12	-	-	-	-	USART1_RX	SPI5_MISO	-	-
	PF13	-	-	-	-	USART1_TX	SPI5_NSS	-	-
	PF14	-	TIM2_CH2	-	-	USART1_CTS	SPI5_MOSI	-	-
	PF15	-	-	-	-	USART1_RTS	SPI5_SCK	-	-

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port G	PG0	-	TIM1_CH4N	TIM12_CH1	-	-	-	-	UART9_RX
	PG1	-	TIM16_CH1N	-	-	-	SPI5_MISO	SAI1_SCK_B	
	PG2	-	TIM17_CH1N	-	-	-	SPI5_MOSI	SAI1_FS_B	USART3_RTS
	PG3	TRACED1	-	-	-	-	-	-	USART2_TX
	PG4	-	TIM1_BKIN2	-	-	-	-	-	
	PG5	-	TIM1_ETR	-	-	-	-	-	USART2_CTS/ USART2_NSS
	PG6	-	TIM17_BKIN	-	-	-	-	-	USART6_CK
	PG7	TRACECLK		-	-	-	-	SAI1_MCLK_A	USART6_CK
	PG8	RTC_REFIN	TIM1_CH3N	TIM12_CH2	-	USART1_RX	SPI2_MOSI/ I2S2_SDO	SAI1_SCK_B	-
	PG9	-	-	-	-	-	-	-	-
	PG10	-	TIM1_CH1N		LPTIM2_CH1	-	SPI2_SCK/I2S2_CK	FDCAN2_TX	USART3_CTS/ USART3_NSS
	PG11	-	-	-	-	-	-	-	-
	PG12	-	TIM17_CH1	-	-	-	SPI5_SCK	SAI1_MCLK_B	
	PG13	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	-	-	-	USART3_RTS
	PG14	TRACED1	LPTIM1_ETR	TIM8_CH4	-	-	SPI6_MOSI/ I2S6_SDO	USART10_RTS	USART6_TX
	PG15	-	TIM1_CH4	-	-	-	SPI5_RDY	SPI4_RDY	USART3_CK

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH2	TRACED2	TIM1_ETR	TIM3_ETR	-	TIM15_BKIN	-	FDCAN1_TX	-
	PH3	TRACECLK	-	-	-	-	-	-	-
	PH4	-	-	-	-	-	-	-	-
	PH5	-	-	-	-	-	SPI5_SCK	-	-
	PH6	-	-	-	-	-	SPI5_NSS	-	-
	PH7	-	-	I3C2_SCL	-	-	SPI5_MOSI	-	-
	PH8	-	-	I3C2_SDA	-	-	SPI5_MISO	-	-
	PH9	-	TIM16_CH1	TIM4_CH3	USART3_CK	I2C1_SCL	-	FDCAN1_RX	I3C1_SCL
	PH10	-	-	-	-	-	-	-	-
	PH11	-	-	-	-	-	-	-	-
	PH12	-	-	-	-	-	-	-	-
	PH13	-	-	-	-	-	-	-	-
	PH14	-	-	-	-	-	-	-	-
	PH15	-	-	-	-	-	-	-	-

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port N	PN0	-	-	-	-	-	-	-	-
	PN1	-	-	-	-	-	-	-	-
	PN2	-	-	-	-	-	-	-	-
	PN3	-	-	-	-	-	-	-	-
	PN4	-	-	-	-	-	-	-	-
	PN5	-	-	-	-	-	-	-	-
	PN6	-	-	-	-	-	-	-	-
	PN7	-	-	-	-	-	-	-	-
	PN8	-	-	-	-	-	-	-	-
	PN9	-	-	-	-	-	-	-	-
	PN10	-	-	-	-	-	-	-	-
	PN11	-	-	-	-	-	-	-	-
	PN12	-	-	-	-	-	-	-	-
Port O	PO0	-	-	-	-	-	-	-	-
	PO1	-	-	-	-	-	-	-	-
	PO2	-	-	-	-	-	-	-	-
	PO3	-	-	-	-	-	-	-	-
	PO4	-	-	-	-	-	-	-	-
	PO5	-	-	-	-	-	-	-	-

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port P	PP0	-	-	-	-	-	-	-	-
	PP1	-	-	-	-	-	-	-	-
	PP2	-	-	-	-	-	-	-	-
	PP3	-	-	-	-	-	-	-	-
	PP4	-	-	-	-	-	-	-	-
	PP5	-	-	-	-	-	-	-	-
	PP6	-	-	-	-	-	-	-	-
	PP7	-	-	-	-	-	-	-	-
	PP8	-	-	-	-	-	SPI2_MISO	-	-
	PP9	-	-	-	-	-	SPI2_MOSI	-	-
	PP10	-	-	-	-	-	-	-	-
	PP11	-	-	-	-	-	-	-	-
	PP12	-	-	-	-	-	-	-	-
	PP13	-	-	-	-	-	-	-	-
	PP14	-	-	-	-	-	-	-	-
	PP15	-	-	-	-	-	-	-	-

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Table 17. Alternate functions: AF0 to AF7 (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2/16/17/ LPTIM1	PDM_SAI1/ TIM3/4/5/12/15	LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2	I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC	SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC	SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD	SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1
Port Q	PQ0	TRACECLK	-	TIM8_ETR	-	-	-	-	-
	PQ1	-	-	TIM8_BKIN	-	-	-	-	-
	PQ2	-	-	TIM8_BKIN2	-	-	-	-	-
	PQ3	-	-	TIM8_CH1	-	-	-	-	-
	PQ4	-	-	TIM8_CH1N	-	-	-	-	-
	PQ5	-	-	TIM8_CH2	-	-	-	-	-
	PQ6	-	-	TIM8_CH2N	-	-	-	-	-
	PQ7	-	-	TIM8_CH3	-	-	-	-	-

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Table 18. Alternate functions: AF8 to AF15

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port A	PA0	UART4_TX	-	SAI2_SD_B	SDMMC2_CMD	FMC_AD7/ FMC_D7	-	LCD_G3	HDP0
	PA1	UART4_RX	DCMIPP_D0/ DCMI_D0/PSSI_D0	SAI2_MCLK_B	-	FMC_AD6/ FMC_D6	-	-	LCD_G2
	PA2	-	-	SAI2_SCK_B	MDIOS_MDIO	FMC_AD5/ FMC_D5	-	-	LCD_B7
	PA3	UART7_RX	-	-	-	FMC_A17/ FMC_ALE	-	-	-
	PA4		DCMIPP_D3/ DCMI_D3/PSSI_D3	-	-	FMC_A13	-	-	-
	PA5	SPI6_SCK/ I2S6_CK	DCMIPP_D8/ DCMI_D8/PSSI_D8	TIM10_CH1	-	FMC_NOE	-	-	LCD_CLK
	PA6	SPI6_MISO/ I2S6_SDI	DCMIPP_PIXCLK/ DCMI_PIXCLK/ PSSI_PDCK	TIM13_CH1	MDIOS_MDC	LCD_B7	-	-	LCD_HSYNC
	PA7	SPI6_MOSI/ I2S6_SDO		LCD_R4	TIM14_CH1	FMC_RNB	-	-	LCD_B1
	PA8	-	TIM11_CH1	UART7_RX		FMC_AD4/ FMC_D4	-	-	LCD_B6
	PA9	-	DCMIPP_D0/ DCMI_D0/PSSI_D0	-		FMC_AD3/ FMC_D3	-	-	LCD_B5
	PA10	-	DCMIPP_D1/ DCMI_D1/PSSI_D1	-	MDIOS_MDIO	FMC_AD2/ FMC_D2	-	-	LCD_B4
	PA11	UART4_RX	-	-	-	FMC_AD1/ FMC_D1	-	-	LCD_B3
	PA12	UART4_TX	-	SAI2_FS_B	-	FMC_AD0/ FMC_D0	-		LCD_B2
	PA13	-	-	-	-	-	-	-	-
	PA14	-	-	-	-	-	-	-	-
	PA15	UART4_RTS	-	UART7_TX	-	FMC_D15/ FMC_AD15	-	-	LCD_R5

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Table 18. Alternate functions: AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port B	PB0	-	DCMIPP_D4/DCMI_D4/PSSI_D4	-	-	FMC_D13/ FMC_AD13	-	-	EVENTOUT
	PB1	-	-	-	-	FMC_NOE	[RNG_S2]	LCD_R1	HDP1
	PB2	-	-	-	-	FMC_D2/ FMC_AD2	-	LCD_B2	HDP2
	PB3	-	-	SAI2_FS_B	-	FMC_NBL1	GFXTIM_LCKCAL	FMC_A23	HDP0
	PB4	SPI6_MISO/ I2S6_SDI	DCMIPP_VSYNC/ DCMI_VSYNC/ PSSI_RDY	UART7_TX	SDMMC2_D3	FMC_D13/ FMC_AD13	-	LCD_R3	HDP4
	PB5	SPI6_MOSI/ I2S6_SDO	DCMIPP_D10/ DCMI_D10/PSSI_D10	-	UART5_RX	FMC_D12/ FMC_AD12	-	LCD_R2	HDP5
	PB6	-	DCMIPP_D6/DCMI_D6/PSSI_D6	-	-	FMC_D14/ FMC_AD14	-	-	EVENTOUT
	PB7	-	DCMIPP_D7/DCMI_D7/PSSI_D7	SAI2_MCLK_B	-	FMC_D15/ FMC_AD15	-	-	EVENTOUT
	PB8	SPDIFRX1_IN3	DCMIPP_VSYNC/ DCMI_VSYNC/ PSSI_RDY	SAI2_FS_B	SDMMC2_D0	FMC_D1/ FMC_AD1	-	-	EVENTOUT
	PB9	SPDIFRX1_IN0	DCMIPP_D3/DCMI_D3/PSSI_D3	-	SDMMC2_D2	FMC_D3/ FMC_AD3	-	-	EVENTOUT
	PB10	-	-	-	-	FMC_D11/ FMC_AD11	-	LCD_G7	HDP2
	PB11	-	-	-	-	FMC_D10/ FMC_AD10	-	LCD_G6	HDP3
	PB12	-	-	-	UART5_RX	FMC_D9/ FMC_AD9	-	LCD_G5	HDP4
	PB13	-	-	-	SDMMC2_D6	FMC_D5/ FMC_AD5	-	LCD_CLK	EVENTOUT
	PB14	-	DCMIPP_D10/ DCMI_D10/PSSI_D10	-	-	FMC_D7/ FMC_AD7	-	LCD_HSYNC	EVENTOUT
	PB15	SPDIFRX1_IN2	-	-	-	FMC_D0/ FMC_AD0	-	LCD_G4	EVENTOUT

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Table 18. Alternate functions: AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port C	PC0	SPI6_SCK/ I2S6_CK	DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE	UART7_RX	SDMMC2_D2	FMC_D14/ FMC_AD14	-	LCD_R4	HDP3
	PC1	UART4_TX	DCMIPP_D7/DCMI_D7/ PSSI_D7	SDMMC1_D5	SDMMC2_D5	SDMMC1_CDIR	-	-	HDP1
	PC2	-	DCMIPP_D13/ DCMI_D13/PSSI_D13	-	SDMMC2_CK	FMC_NE3	-	FMC_RNB	EVENTOUT
	PC3	SPDIFRX1_IN0	DCMIPP_D2/DCMI_D2/ PSSI_D2	-	SDMMC2_CMD	FMC_D8/ FMC_AD8	-	-	EVENTOUT
	PC4	UART4_RTS	-	LCD_VSYNC	SDMMC2_D0	FMC_NE1	-	LCD_DE	HDP6
	PC5	-	DCMIPP_D2/DCMI_D2/ PSSI_D2	SAI2_SD_B	SDMMC2_D1	FMC_NWE	-	-	EVENTOUT
	PC6	-	DCMIPP_D1/DCMI_D1/ PSSI_D1	SDMMC1_D6	SDMMC2_D6	SDMMC1_D0DIR	-	-	HDP6
	PC7	-	DCMIPP_D1/DCMI_D1/ PSSI_D1	SDMMC1_D7	SDMMC2_D7	SDMMC1_D123DIR	-	-	HDP7
	PC8	-	DCMIPP_D2/DCMI_D2/ PSSI_D2	SDMMC1_D0	UART5_RTS	FMC_NE4	-	LCD_B0	HDP0
	PC9	-	DCMIPP_D3/DCMI_D3/ PSSI_D3	SDMMC1_D1	UART5_CTS		-	LCD_B3	HDP1
	PC10	UART4_TX	DCMIPP_D14/PSSI_D14	SDMMC1_D2	-	FMC_CLK	-	-	HDP2
	PC11	UART4_RX	DCMIPP_D4/DCMI_D4/ PSSI_D4	SDMMC1_D3	-	-	-	-	HDP3
	PC12	-	DCMIPP_D9/DCMI_D9/ PSSI_D9	SDMMC1_CK	UART5_TX	FMC_NL	-	-	HDP4
	PC13	-	-	-	-	-	-	-	HDP5
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

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Table 18. Alternate functions: AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port D	PD0	UART4_RX	DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE	-	-	FMC_A6	-	FMC_A22	EVENTOUT
	PD1	UART4_TX	-	-	ETH1_MDC	FMC_A7	-	FMC_A23	EVENTOUT
	PD2	-	-	MDIOS_MDC	SDMMC2_CK	FMC_A0	-	FMC_A16/ FMC_CLE	HDP1
	PD3	-	DCMIPP_D14/PSSI_D14	-	ETH1_PHY_INTN	FMC_A10	-	-	EVENTOUT
	PD4	-	DCMIPP_D9/DCMI_D9/ PSSI_D9	-	-	FMC_A11	-	-	EVENTOUT
	PD5	-	DCMIPP_PIXCLK/ DCMI_PIXCLK/ PSSI_PDCK	-	SDMMC2_D7	FMC_D6/FMC_AD6	-	-	EVENTOUT
	PD6	-	-	-	-	FMC_A1	-	FMC_A17/ FMC_ALE	HDP2
	PD7	-	DCMIPP_D0/DCMI_D0/ PSSI_D0	-	-	FMC_A2	-	FMC_A18	HDP3
	PD8	SPDIFRX1_IN1	DCMIPP_D11/ DCMI_D11/PSSI_D11	-	-	FMC_NBL0	-	LCD_R7	EVENTOUT
	PD9	-	DCMIPP_D11/ DCMI_D11/PSSI_D11	-	-	FMC_SDCLK	-	LCD_R1	EVENTOUT
	PD10	SPDIFRX1_IN2	-	SAI2_FS_B	-	FMC_A3	GFXTIM_TE	FMC_A19	HDP4
	PD11	-	DCMIPP_D15/PSSI_D15	SDMMC1_D0	-	FMC_D8/FMC_AD8	-	-	EVENTOUT
	PD12	SPDIFRX1_IN3	DCMIPP_D12/ DCMI_D12/PSSI_D12	-	ETH1_MDIO	FMC_A5	-	FMC_A21	HDP5
	PD13	-	DCMIPP_D13/ DCMI_D13/PSSI_D13	SAI2_SCK_A	-	FMC_D4/FMC_AD4	-	LCD_R6	EVENTOUT
	PD14	-	-	-	-	FMC_A9	-	-	EVENTOUT
	PD15	-	-	-	-	FMC_A8	-	LCD_R2	EVENTOUT

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Table 18. Alternate functions: AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port E	PE0	UART8_RX	DCMIPP_D2/DCMI_D2/ PSSI_D2	SAI2_MCLK_A	-	FMC_D9/FMC_AD9	-	-	EVENTOUT
	PE1	UART8_TX	DCMIPP_D8/DCMI_D8/ PSSI_D8	-	-	FMC_D10/FMC_AD10	-	-	EVENTOUT
	PE2	-	-	-	-	FMC_D11/FMC_AD11	TIM1_CH2N	-	EVENTOUT
	PE3	-	-	-	-	FMC_D12/FMC_AD12	-	-	EVENTOUT
	PE4	SPDIFRX1_IN1	DCMIPP_D5/DCMI_D5/ PSSI_D5		SDMMC2_D3	FMC_RNB	-	LCD_G1	EVENTOUT
	PE5	-	DCMIPP_D5/DCMI_D5/ PSSI_D5		UART5_TX	FMC_SDNE1	-	-	HDP6
	PE6	-	DCMIPP_VSYNC/ DCMI_VSYNC/PSSI_RDY	DCMIPP_D1/DCMI_D1/ PSSI_D1	UART5_TX	FMC_SDCKE1	-	-	HDP7
	PE7	UART7_RX	-	SAI2_SD_B	-	FMC_A4	-	FMC_A20	EVENTOUT
	PE8	UART7_TX	DCMIPP_D4/DCMI_D4/ PSSI_D4	-	-	FMC_A12	-	-	EVENTOUT
	PE9	UART7_RTS	-	-	-	FMC_A14/FMC_BA0	-	-	EVENTOUT
	PE10	UART7_CTS	DCMIPP_D3/DCMI_D3/ PSSI_D3	-	-	FMC_A15/FMC_BA1	-	-	EVENTOUT
	PE11	-	-	SAI2_SD_B	-	FMC_SDNWE	-	LCD_VSYNC	EVENTOUT
	PE12	-	-	SAI2_SCK_B	-	FMC_NRAS	-	-	EVENTOUT
	PE13	-	-	SAI2_FS_B	-	FMC_NCAS	-	-	EVENTOUT
	PE14	-	-	SAI2_MCLK_B	-	FMC_SDNE0	GFXTIM_LCKCAL	FMC_NWE	EVENTOUT
	PE15	-	-	SDMMC1_D0	-	FMC_SDCKE0	GFXTIM_FCKCAL	-	EVENTOUT

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Table 18. Alternate functions: AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port F	PF0	UART8_RTS	DCMIPP_D9/DCMI_D9/ PSSI_D9	-	ETH1_MII_TX_CLK	ETH1_RGMII_GTX_CLK	-	-	EVENTOUT
	PF1	UART8_CTS	DCMIPP_D7/DCMI_D7/ PSSI_D7	-	ETH1_TX_ER	-	-	-	EVENTOUT
	PF2	-	-	-	ETH1_RGMII_CLK125	FMC_NWAIT	-	LCD_B1	EVENTOUT
	PF3	-	DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE	-	ETH1_PPS_OUT	FMC_NL	-	LCD_R4	EVENTOUT
	PF4	SPI6_NSS/ I2S6_WS	DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE	-	ETH1_MDIO	-	-	LCD_R3	HDP4
	PF5	-	DCMIPP_D6/DCMI_D6/ PSSI_D6	SAI2_SD_A	ETH1_CLK	FMC_NE3	-	LCD_G0	EVENTOUT
	PF6	-	SPI5_RDY	SPI1_RDY	ETH1_MII_COL	GFXTIM_FCKCAL	TIM1_CH3	LCD_DE	HDP3
	PF7	UART4_CTS	-	-	ETH1_MII_RX_CLK/ ETH1_RMII_REF_CLK/ ETH1_RGMII_RX_CLK	GFXTIM_TE	[RNG_S1]	LCD_VSYNC	HDP0
	PF8	-	-	-	ETH1_MII_RXD2/ ETH1_RGMII_RXD2	FMC_NWE	-	LCD_R6	EVENTOUT
	PF9	-	-	-	ETH1_MII_RXD3/ ETH1_RGMII_RXD3	-	-	LCD_HSYNC	EVENTOUT
	PF10	UART7_RX	DCMIPP_D11/DCMI_D11/ PSSI_D11	DCMIPP_D15/ PSSI_D15	ETH1_MII_RX_DV/ ETH1_RMII_CRS_DV/ ETH1_RGMII_RX_CTL	-	-	LCD_R1	EVENTOUT
	PF11	-	DCMIPP_D15/PSSI_D15	SAI2_SD_B	ETH1_MII_TX_EN/ ETH1_RMII_TX_EN/ ETH1_RGMII_TX_CTL	-	-	LCD_B0	EVENTOUT
	PF12	-	DCMIPP_D13/DCMI_D13/ PSSI_D13	-	ETH1_MII_TXD0/ ETH1_RMII_TXD0/ ETH1_RGMII_TXD0	-	-		EVENTOUT
	PF13	-	DCMIPP_D10/DCMI_D10/ PSSI_D10	-	ETH1_MII_TXD1/ ETH1_RMII_TXD1/ ETH1_RGMII_TXD1	-	-		EVENTOUT
	PF14	-	-	-	ETH1_MII_RXD0/ ETH1_RMII_RXD0/ ETH1_RGMII_RXD0	-	-	LCD_G0	EVENTOUT
	PF15	-	-	-	ETH1_MII_RXD1/ ETH1_RMII_RXD1/ ETH1_RGMII_RXD1	-	-	LCD_G1	EVENTOUT

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Table 18. Alternate functions: AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port G	PG0	-	-	LCD_VSYNC	ETH1_PHY_INTN	-	-	LCD_R0	EVENTOUT
	PG1	UART7_RTS	DCMIPP_PIXCLK/ DCMI_PIXCLK/ PSSI_PDCK	TIM13_CH1	-	FMC_A19	-	LCD_G1	EVENTOUT
	PG2	UART7_CTS	DCMIPP_D6/DCMI_D6/ PSSI_D6	SAI2_MCLK_B	TIM14_CH1	FMC_A21	-	LCD_R0	EVENTOUT
	PG3	-	DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE	-	ETH1_MII_TXD2/ ETH1_RGMII_TXD2	-	-	-	EVENTOUT
	PG4	-	-	-	ETH1_MII_TXD3/ ETH1_RGMII_TXD3	-	-	LCD_B0	EVENTOUT
	PG5	-	-	-	ETH1_MII_RX_ER	-	-	LCD_B1	EVENTOUT
	PG6	-	DCMIPP_D12/DCMI_D12/ PSSI_D12	-	ETH1_MII_CRS	-	-	LCD_B3	EVENTOUT
	PG7	-	DCMIPP_D13/DCMI_D13/ PSSI_D13	-	ETH1_PHY_INTN	-	-	-	EVENTOUT
	PG8	UART4_CTS	-	-	SDMMC2_D1	FMC_A20	-	LCD_G7	HDP7
	PG9	-	-	-	-	FMC_D8/FMC_AD8	-	LCD_R7	EVENTOUT
	PG10	-	DCMIPP_D2/DCMI_D2/ PSSI_D2	-	UART5_TX	FMC_A16/FMC_CLE	-	LCD_G4	HDP5
	PG11	UART7_RX	-	-	ETH1_MDC	-	-	LCD_R6	EVENTOUT
	PG12	UART7_TX	-	-	-	FMC_A18	-	LCD_G0	EVENTOUT
	PG13	-	DCMIPP_D12/DCMI_D12/ PSSI_D12	SAI2_FS_A	-	FMC_NE1	-	LCD_DE	EVENTOUT
	PG14	USART2_RTS	DCMIPP_D11/DCMI_D11/ PSSI_D11	FMC_NCE	-	FMC_NE2	-	LCD_B1	EVENTOUT
	PG15	-	DCMIPP_D4/DCMI_D4/ PSSI_D4	SPI1_RDY	ETH1_MII_RX_CLK/ ETH1_RMII_REF_CLK	FMC_CLK	-	LCD_B0	EVENTOUT

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Table 18. Alternate functions: AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	DCMIPP_D11/DCMI_D11/ PSSI_D11	SDMMC1_CMD	UART5_RX	FMC_NE3	-	-	EVENTOUT
	PH3	UART7_TX	-	-	-	-	-	LCD_B4	EVENTOUT
	PH4	UART7_TX	-	-	-	-	-	LCD_R4	EVENTOUT
	PH5	-	-	-	ETH1_MDC		-		EVENTOUT
	PH6	-	-	-	-	-	-	LCD_B5	EVENTOUT
	PH7	-	-	-	-	-	-		EVENTOUT
	PH8	-	-	-	-	-	-		EVENTOUT
	PH9	UART4_RX	DCMIPP_D6/DCMI_D6/ PSSI_D6	SDMMC1_D4	SDMMC2_D4	SDMMC1_CKIN	-	FMC_D9/ FMC_AD9	HDP0
	PH10	-	-	-	-	-	-	-	-
	PH11	-	-	-	-	-	-	-	-
	PH12	-	-	-	-	-	-	-	-
	PH13	-	-	-	-	-	-	-	-
	PH14	-	-	-	-	-	-	-	-
	PH15	-	-	-	-	-	-	-	-

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Table 18. Alternate functions: AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port N	PN0	-	XSPIM_P2_DQS0	-	-	FMC_A25	-	-	EVENTOUT
	PN1	-	XSPIM_P2_NCS1	-	-	FMC_A24	-	-	EVENTOUT
	PN2	-	XSPIM_P2_IO0	-	-	FMC_A23	-	-	EVENTOUT
	PN3	-	XSPIM_P2_IO1	-	-	FMC_A22	-	-	EVENTOUT
	PN4	-	XSPIM_P2_IO2	-	-	-	-	-	EVENTOUT
	PN5	-	XSPIM_P2_IO3	-	-	-	-	-	EVENTOUT
	PN6	-	XSPIM_P2_CLK	-	-	-	-	-	EVENTOUT
	PN7	-	XSPIM_P2_NCLK	-	-	-	-	-	EVENTOUT
	PN8	-	XSPIM_P2_IO4	-	-	-	-	-	EVENTOUT
	PN9	-	XSPIM_P2_IO5	DCMIPP_D5/DCMI_D5/ PSSI_D5	-	-	-	-	EVENTOUT
	PN10	-	XSPIM_P2_IO6	-	-	-	-	LCD_B4	EVENTOUT
	PN11	-	XSPIM_P2_IO7	-	-	-	-	LCD_B6	EVENTOUT
	PN12	-	XSPIM_P2_NCS2	-	-	-	-	-	EVENTOUT
Port O	PO0	-	XSPIM_P1_NCS1	-	-	FMC_A22	-	-	EVENTOUT
	PO1	-	XSPIM_P1_NCS2	-	-	FMC_A23	-	-	EVENTOUT
	PO2	-	XSPIM_P1_DQS0	-	-	FMC_A24	-	LCD_B7	EVENTOUT
	PO3	-	XSPIM_P1_DQS1	-	-	FMC_A25	-	LCD_G3	EVENTOUT
	PO4	-	XSPIM_P1_CLK	LCD_B4	-	FMC_A24	-	FMC_NBL2	EVENTOUT
	PO5	-	XSPIM_P1_NCLK	-	-	FMC_A25	-	FMC_NBL3	EVENTOUT

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Table 18. Alternate functions: AF8 to AF15 (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX	FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX	SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS	I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP	TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP	TIM1/DCMI/ PSSI/LCD/COMP	UART5/LCD	SYS
Port P	PP0	-	XSPIM_P1_IO0	-	-	FMC_D16	-	-	EVENTOUT
	PP1	-	XSPIM_P1_IO1	-	-	FMC_D17	-	-	EVENTOUT
	PP2	-	XSPIM_P1_IO2	-	-	FMC_D18	-	-	EVENTOUT
	PP3	-	XSPIM_P1_IO3	-	-	FMC_D19	-	-	EVENTOUT
	PP4	-	XSPIM_P1_IO4	-	-	FMC_D20	-	-	EVENTOUT
	PP5	-	XSPIM_P1_IO5	-	-	FMC_D21	-	-	EVENTOUT
	PP6	-	XSPIM_P1_IO6	-	-	FMC_D22	-	-	EVENTOUT
	PP7	-	XSPIM_P1_IO7	-	-	FMC_D23	-	-	EVENTOUT
	PP8	-	XSPIM_P1_IO8	-	-	FMC_D24	-	-	EVENTOUT
	PP9	-	XSPIM_P1_IO9	-	-	FMC_D25	-	-	EVENTOUT
	PP10	-	XSPIM_P1_IO1O	-	ETH1_MDC	FMC_D26	-	-	EVENTOUT
	PP11	-	XSPIM_P1_IO11	-	-	FMC_D27	-	-	EVENTOUT
	PP12	-	XSPIM_P1_IO12	-	-	FMC_D28	-	-	EVENTOUT
	PP13	-	XSPIM_P1_IO13	-	-	FMC_D29	-	-	EVENTOUT
	PP14	-	XSPIM_P1_IO14	-	-	FMC_D30	-	-	EVENTOUT
	PP15	-	XSPIM_P1_IO15	-	-	FMC_D31	-	LCD_B5	EVENTOUT
Port Q	PQ0	-	-	-	-	-	-	-	EVENTOUT
	PQ1	-	-	-	-	-	-	-	EVENTOUT
	PQ2	-	SAI2_SCK_B	-	-	-	-	-	EVENTOUT
	PQ3	-	-	-	-	-	-	-	EVENTOUT
	PQ4	-	-	-	-	-	-	-	EVENTOUT
	PQ5	-	SAI2_FS_B	-	-	-	-	-	EVENTOUT
	PQ6	-	SAI2_SD_B	-	-	-	-	-	EVENTOUT
	PQ7	-	SAI2_MCLK_B	-	-	-	-	-	EVENTOUT

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5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with junction temperature T_J = 25 °C and T_J = T_J max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, supply voltage V_{DD} = 3.3 V or 1.8 V (operating condition), $V_{DDA18ON}$ = 1.8 V, and nominal V_{DDCORE} = 0.81 V. They are only given as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error lower than or equal to the value indicated (mean ± 2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines, and are not tested.

5.1.4 Loading capacitor

Unless otherwise specified, the loading conditions used for pin parameter measurement are shown in *Figure 13*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 14*.

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Figure 13. Pin loading conditions

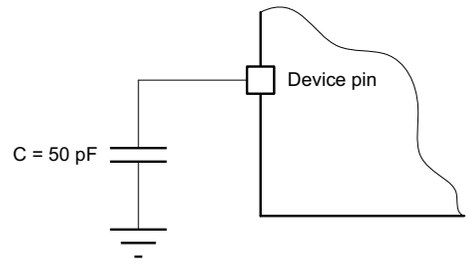
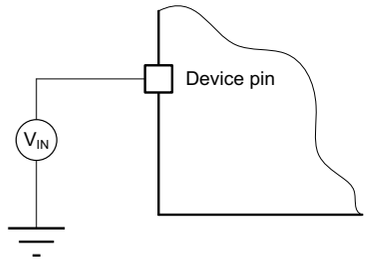


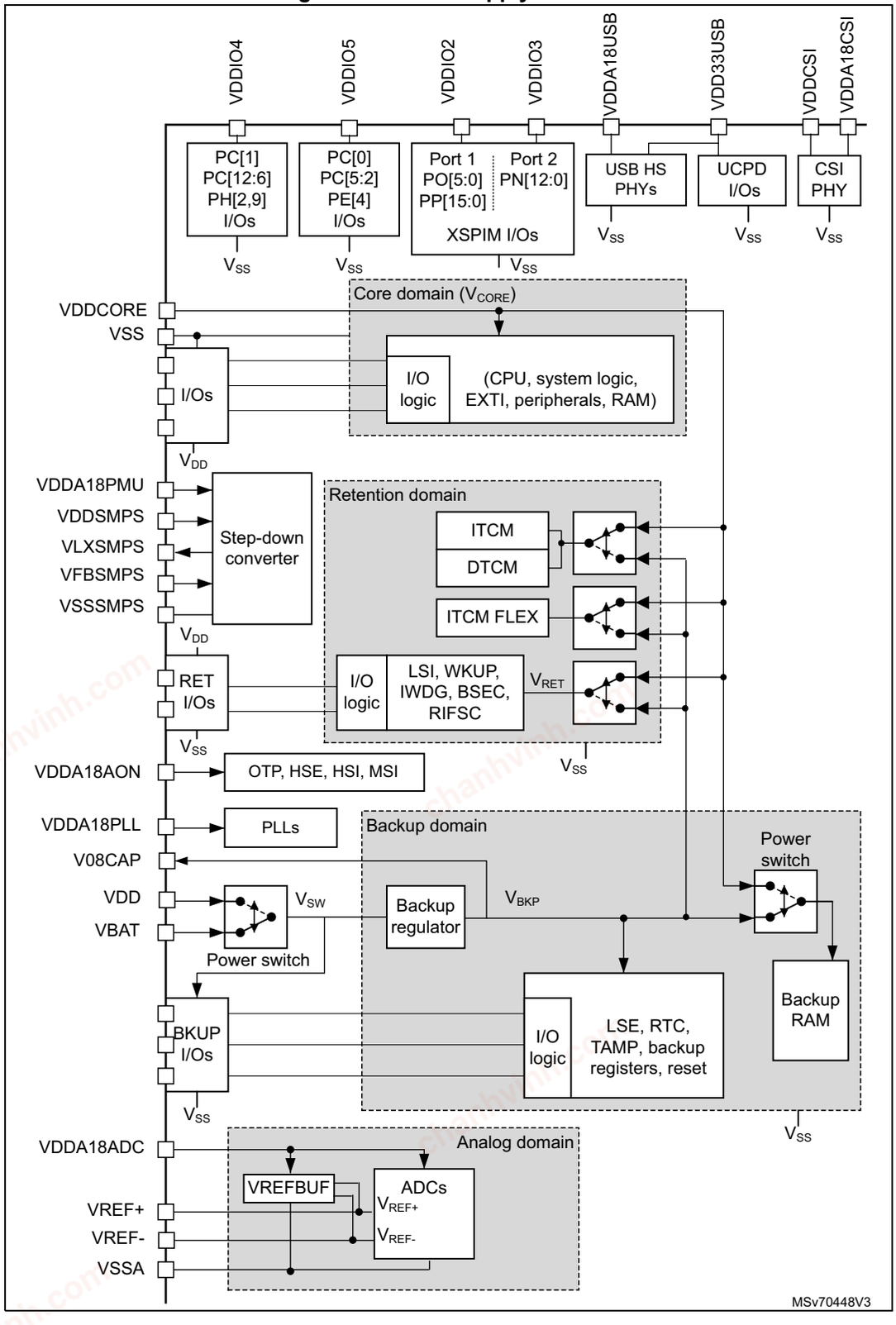
Figure 14. Pin input voltage



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5.1.6 Power supply scheme

Figure 15. Power supply scheme



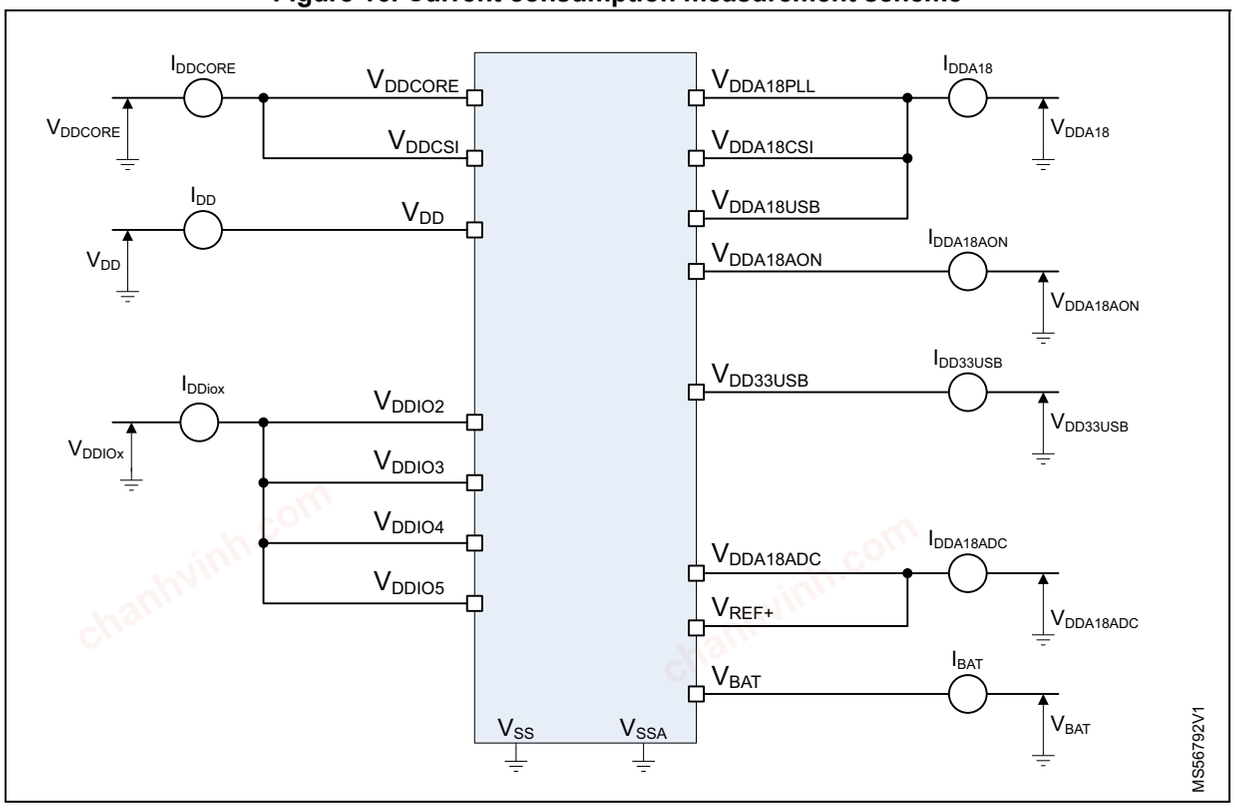
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Caution: Each power supply pair (V_{DD} / V_{SS}, V_{DDCORE} / V_{SS}, V_{DDA} / V_{SSA}) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to (or below) the appropriate pins to ensure correct device functionality. It is not recommended to remove them to reduce PCB size or cost, as this can cause incorrect operation of the device. The number of needed capacitors and their values are detailed in AN5967 "*Getting started with the hardware development for STM32N6 MCUs*", available on *www.st.com*.

5.1.7 Current consumption measurement

The I_{DD} parameters in the tables in the next sections represent the total MCU consumption, including the current supplying V_{DD}, V_{DDA}, and V_{DDCORE}.

Figure 16. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19*, *Table 20*, and *Table 21* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

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Table 19. Voltage characteristics(1)(2)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage for 1.8 V range (including V_{DD}, V_{DDIOx}, V_{BAT})	-0.3	2.0	V
V_{DDX} - V_{SS}	External main supply voltage for 3.3 V range (including V_{DD}, V_{DDIOx}, V_{BAT}, $V_{DD33USB}$)		3.7	
$V_{DD18OAON}$ - V_{SS}	1.8 V supply voltage		1.98	
V_{DDCORE} - V_{SS}	External core supply voltage (including V_{DDCORE}, V_{DDCSI})		0.99	
V_{DDA18} - V_{SS}	1.8 V supply voltage (including $V_{DDA18PLL}$, $V_{DDA18CSI}$, $V_{DDA18USB}$, $V_{DDA18ADC}$)		1.98	
V_{IN}	Input voltage on TT_xx pins (VDDIOxVRSEL = 0)	V_{SS} - 0.3	3.6	
	Input voltage on TT_xx pins (VDDIOxVRSEL = 1)		1.98	
	Input voltage on UCPD pins		$V_{DD33USB}$ + 1.935	
$\lvert\Delta V_{DDx}\rvert$	Variations between different VDDX power pins of the same domain	-	50.0	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-		

1. All main power and ground pins must always be connected to the external power supply, in the permitted range.
2. Specified by design, not tested in production.

Table 20. Current characteristics

Symbol	Ratings	Conditions	Max	Unit
I_{IO}	Output current sunk by any I/O and control pin	-40 °C < T_J ≤ 90 °C	20	mA
		90 °C < T_J ≤ 110 °C	10	
		T_J > 110 °C	4	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(1)		±25	

1. When several inputs are submitted to a current injection, the maximum $\sum\lvert I_{INJ(PIN)}\rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_{JMAX}	Maximum junction temperature	125	

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5.3 Operating conditions

5.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CPU}	Clock frequency of Cortex-CM55 (VOS low)	Base-TCM with 0 wait states Flex-TCM with 1 wait state	0	-	600	MHz
$F_{CPU\ overdrive}$	Clock frequency of Cortex-CM55 in overdrive (VOS high)		0	-	800	
F_{NPU}	Clock frequency of NPU/CNN		0	-	800	
$F_{NPU\ overdrive}$	Clock frequency of NPU/CNN in overdrive		0	-	1000	
$F_{ck_icn_hsl}$	Clock frequency of USB, ETH buses	-	0	-	400	
F_{HCLK}	Clock frequency of AHB bus	-	0	-	200	
$F_{ck_cpu_axi}$	Clock frequency of AXI CPU bus	-	0	-	400	
F_{PCLKx}	Clock frequency of APB buses (x = 1, 2, 3, 4, 5)	-	0	-	F_{HCLKx} / 4	
V_{DD}(1)	I/Os supply voltage	1.8 V range	1.62	1.8	1.98	V
		3.3 V range	3.0	3.3	3.6	
$V_{DDA18ON}$(1)	Internal analog supply voltage	-	1.71	1.8	1.935	
V_{DDIOx}	Specific I/Os supply voltage (x = 2, 3, 4, 5)	1.8 V range	1.71	1.8	1.935	
		3.3 V range	2.7	3.3	3.6	
V_{DDCORE}	Main digital logic supply voltage	SoC Run mode (VOS low)	0.782	0.81	0.842	
		SoC Run mode (VOS high)	0.858	0.89	0.921	
		Sleep mode (SoC Run mode, peripheral clock stopped, VOS low)	0.782	0.81	0.842	
		Sleep mode (SoC Run mode, peripheral clock stopped, VOS high)	0.858	0.89	0.921	
		Stop mode (SVOS low)	0.64	0.68	0.71	
		Stop mode (SVOS high)	0.782	0.81	0.842	
$V_{DDA18PLL}$	1.8 V analog supply for PLL	F_{NPU} range	1.62	1.8	1.98	
$V_{DDA18CSI}$	1.8 V analog supply for CSI	$F_{NPU\ overdrive}$ range	1.746	1.8	1.98	
V_{DDCSI}	CSI operating voltage	-	0.784	0.81	0.842	
$V_{DD18USB}$	1.8 V analog supply for USBPHY	-	1.746	1.8	1.935	
$V_{DD18ADCx}$	ADC operating voltage (x = 1, 2)	-	1.62	1.8	1.98	
V_{REF+}	ADC reference voltage	-	1.1	-	$V_{DD18ADC}$	
V_{BAT}	Backup operating voltage	-	TBD	-	3.6	

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Table 22. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD18SMPS}$	SMPS supply voltage	-	1.62	1.8	1.89	V
$V_{DD18PMU}$	SMPS analog supply voltage	-	1.62	1.8	1.89	
V_{08CAP}	Backup regulator output voltage (SMPS)	-	0.72	0.8	0.88	
V_{IN}	I/O input voltage	I/O TT_xx in the 1.8 V range	-0.3	-	Min V_{DDxx} + 0.3(2)	V
		I/O TT_xx in the 3.3 V range			Min(V_{DD}, V_{DDIOx}) + 0.3	
		I/O TT_a			$V_{DD18ADC}$ + 0.3	
PDR_ON	Power-down reset enable	-	1.62	1.8	1.98	V

1. Must be present before any other supply.
2. V_{DDxx} depends upon power ring on I/Os (V_{DD}, V_{DDIOx}, $V_{DDA18ADC}$, $V_{DDA18USB}$, $V_{DD33USB}$).

5.3.2 Operating conditions at power-up/power-down

The parameters in *Table 23* are evaluated by characterization under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 23. Operating conditions at power-up/power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD}/V_{DDIOx} transitions	Rise and fall time rates	20	1500	µs/V
$t_{VDDA18AON}$	$V_{DDA18AON}$ transitions				
$t_{VDDcore}$	V_{DDCORE} transitions				
t_{VDDCSI}	V_{DDCSI} transitions		10		
t_{VDDA18}	V_{DDAPLL}, $V_{DDA18CSI}$, $V_{DDA18USB}$, $V_{DDA18ADC}$ transitions				
t_{VDD33}	$V_{DD33USB}$ transitions				
t_{VBat}	V_{BAT} transitions				

1. Evaluated by characterization, not tested in production, unless otherwise specified.

5.3.3 Embedded reset and power control block characteristics

The parameters in *Table 24* are derived under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after POR released	-	200	-	-	µs

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Table 24. Embedded reset and power control block characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{POR}	Power-on reset threshold	V_{DD}	Rising edge	1.62	1.67	1.71	V
V_{PDR}	Power-down reset threshold		Falling edge	1.58	1.63	1.67	
$V_{hyst\ POR}$	Hysteresis voltage of POR/PDR		-	-	40	-	mV
V_{BOR0}	Brown-out reset threshold 0		Rising edge	-	-	-	V
			Falling edge	-	-	-	
V_{BOR1}	Brown-out reset threshold 1		Falling edge	-	-	-	
$V_{hyst\ BOR0}$	Hysteresis voltage of BOR0		-	-	40	-	mV
$V_{hyst\ BOR1}$	Hysteresis voltage of BOR1		-	-	80	-	
$V_{POR\ ANA}$	Power-on reset threshold	$V_{DDA18AON}$	Rising edge	1.62	1.67	1.71	V
$V_{PDR\ ANA}$	Power-down reset threshold		Falling edge	1.58	1.63	1.67	
$V_{hyst\ POR\ ANA}$	Hysteresis voltage of POR/PDR		-	-	40	-	mV
$V_{RDY\ VDDCORE}$	Threshold on rising edge	V_{DDCORE}	Normal modes	0.61	0.66	0.71	V
			LPLV modes	0.50	0.55	0.61	
$V_{hyst\ VDDCORE}$	Hysteresis on falling edge		-	-	21	-	mV
$T_{delay\ VDDCORE}$	Delay after detection		Rising edge	180	-	-	µs
			Falling edge	-	0	-	

1. Specified by design, not tested in production.

5.3.4 Embedded voltage reference

The parameters in *Table 25* are derived under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 25. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltage	-40 °C ≤ T_J ≤ +130 °C	0.792	0.8	0.808	V
$t_{S_vrefint}$(2)	ADC sampling time when reading the internal reference voltage	-	34	-	-	ns
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	-40 °C ≤ T_J ≤ +130 °C	-	-	11	mV
T_{Coeff}	Temperature coefficient		-	-	43	ppm/°C
$V_{DDCoeff}$	Voltage coefficient	1.71 V ≤ $V_{DDA18AON}$ ≤ 3.6 V	-	-	1250	ppm/V

1. Guaranteed by test in production.
2. Specified by design, not tested in production.

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Table 26. Embedded reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFINT_CAL}	Raw data acquired on ADC1 at 30 °C, $V_{DDA18ADC}$ = V_{REF+} = 1.8 V	0x4400 01B8[11:0](1)

1. BSEC_FVR110 register, not automatically shadowed with OTP content, so a fuse read sequence must be issued to get the register updated once (clear after reading). Refer to RM0486, BSEC section "*Operations on fuses*".

5.3.5 Supply current characteristics

The current consumption is measured as described in *Figure 16*. It depends upon several parameters, such as operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequency, I/O pin switching rate, program location in memory, and executed binary code. All the Run mode current consumption measurements are performed with a CoreMark code unless otherwise specified. Supply current characteristics are evaluated by characterization, not tested in production unless otherwise specified.

Typical and maximum current consumption

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled, except when otherwise mentioned
- RTC/LSE are disabled, unless otherwise specified
- BKPSRAM, backup supplies in low-power modes (such as Stop, Standby and VBAT modes) are disabled, unless otherwise specified
- Unless otherwise specified, the typical values are obtained for:
  - V_{DD}, V_{DDIOx} = 1.8 V
  - V_{BAT} = 3.3 V
  - V_{DDCORE} = 0.81 V
  - V_{DDA1V8}, $V_{DDA18AON}$ = 1.8 V

The parameters given in tables *27* to *33* are evaluated by characterization under ambient temperature and supply voltage conditions summarized in *Table 22*.

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Table 27. Current consumption in Run mode

Symbol	Conditions			frcc_c_ck (MHz)	Typ	Max(1) SMPS external				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD}	Code with data processing running from ITCM(2) HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(3)	0.3	0.3	0.3	0.3	0.4	mA
			VOS low	600(4)	0.3	0.3	0.3	0.3	0.4	
		All peripherals enabled	VOS high	800(2)	0.3	0.3	0.3	0.3	0.4	
			VOS low	600(3)	0.3	0.3	0.3	0.3	0.4	
	Code with data processing running from ITCM (2) HSE, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	0.3	0.3	0.3	0.4	0.4	
			VOS low	600(3)	0.3	0.3	0.3	0.4	0.4	
		All peripherals enabled	VOS high	800(2)	0.3	0.3	0.3	0.4	0.4	
			VOS low	600(3)	0.3	0.3	0.3	0.4	0.4	
	Code with data processing running from AXI-SRAM2, Cache ON (2) HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	0.3	0.3	0.3	0.3	0.4	
			VOS low	600(3)	0.3	0.3	0.3	0.3	0.4	
		All peripherals enabled	VOS high	800(2)	0.3	0.3	0.3	0.3	0.4	
			VOS low	600(3)	0.3	0.3	0.3	0.4	0.4	
	Code with data processing running from AXI-SRAM2, Cache OFF (2) HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	0.3	0.3	0.3	0.4	0.4	
			VOS low	600(3)	0.3	0.3	0.3	0.4	0.4	
		All peripherals enabled	VOS high	800(2)	0.3	0.3	0.3	0.4	0.4	
			VOS low	600(3)	0.3	0.3	0.3	0.4	0.4	

1. Guaranteed by characterization results unless otherwise specified.
2. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
3. cpu_overdrive range frequency.
4. cpu_nominal range frequency.

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Table 28. Current consumption (core) in Run mode

Symbol	Conditions			frcc_c_ck (MHz)	Typ	Max(1) SMPS external				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Code with data processing running from ITCM(2) HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(3)	88.0	113.3	321.0	474.9	741.8	mA
			VOS low	600(4)	68.0	90.8	287.7	431.9	694.7	
		All peripherals enabled	VOS high	800(2)	177.5	206.7	415.2	575.0	839.0	
			VOS low	600(3)	146.8	172.6	370.9	519.9	774.4	
	Code with data processing running from ITCM (2) HSE, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	87.6	110.8	319.6	474.8	742.6	
			VOS low	600(3)	64.6	86.3	284.5	429.8	692.7	
		All peripherals enabled	VOS high	800(2)	176.0	203.4	412.5	572.2	836.7	
			VOS low	600(3)	142.9	167.4	366.2	515.9	773.8	
	Code with data processing running from AXI-SRAM2, Cache ON (2) HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	90.4	115.7	323.3	477.8	747.6	
			VOS low	600(3)	69.8	92.7	289.6	434.4	695.2	
		All peripherals enabled	VOS high	800(2)	179.2	208.1	416.5	576.5	839.6	
			VOS low	600(3)	147.9	173.7	371.5	519.9	775.8	
	Code with data processing running from AXI-SRAM2, Cache OFF (2) HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	73.4	97.4	305.5	459.6	729.5	
			VOS low	600(3)	57.4	79.4	277.5	422.7	684.1	
		All peripherals enabled	VOS high	800(2)	164.7	189.1	397.2	556.4	820.2	
			VOS low	600(3)	135.5	159.9	358.5	507.6	763.2	

1. Guaranteed by characterization results unless otherwise specified.
2. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
3. cpu_overdrive range frequency.
4. cpu_nominal range frequency.

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Table 29. Current consumption (1V8) in Run mode

Symbol	Conditions			frcc_c_ck (MHz)	Typ	Max(1) SMPS external				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDA1V8}	Code with data processing running from ITCM(2) HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(3)	2.1	2.1	2.1	2.1	2.1	mA
			VOS low	600(4)	4.4	4.4	4.5	4.6	4.6	
		All peripherals enabled	VOS high	800(2)	2.1	2.1	2.1	2.1	2.1	
			VOS low	600(3)	4.4	4.4	4.5	4.6	4.6	
	Code with data processing running from ITCM (2) HSE, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	2.1	2.1	2.1	2.1	2.1	
			VOS low	600(3)	1.5	1.4	1.4	1.4	1.5	
		All peripherals enabled	VOS high	800(2)	2.1	2.1	2.1	2.1	2.1	
			VOS low	600(3)	1.5	1.4	1.4	1.4	1.5	
	Code with data processing running from AXI-SRAM2, Cache ON (2) HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	2.1	2.1	2.1	2.1	2.1	
			VOS low	600(3)	4.4	4.4	4.5	4.6	4.6	
		All peripherals enabled	VOS high	800(2)	2.1	2.1	2.1	2.1	2.1	
			VOS low	600(3)	4.4	4.4	4.5	4.6	4.6	
	Code with data processing running from AXI-SRAM2, Cache OFF (2) HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	2.1	2.1	2.1	2.1	2.1	
			VOS low	600(3)	1.5	1.4	1.4	1.4	1.5	
		All peripherals enabled	VOS high	800(2)	2.1	2.1	2.1	2.1	2.1	
			VOS low	600(3)	1.5	1.4	1.4	1.4	1.5	

1. Guaranteed by characterization results unless otherwise specified.
2. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
3. cpu_overdrive range frequency.
4. cpu_nominal range frequency.

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Table 30. Current consumption in Sleep mode

Symbol	Conditions			frcc_c_ck (MHz)	Typ	Max(1) SMPS external				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD}	HSI, V_{DD} = 1.8 V	All peripherals disabled	VOS high	800(2)	0.3	0.3	0.3	0.3	0.4	mA
			VOS low	600(3)	0.3	0.3	0.3	0.3	0.4	
			VOS high	800(2)	0.3	0.3	0.3	0.3	0.4	
			VOS low	600(3)	0.3	0.3	0.3	0.3	0.4	
I_{DDCORE}			VOS high	800(2)	48.9	75.1	284.5	438.7	713.9	
			VOS low	600(3)	41.8	66.0	265.4	413.5	677.4	
			VOS high	800(2)	136.4	171.1	382.3	542.8	809.4	
			VOS low	600(3)	118.8	149.9	349.2	500.1	760.0	
I_{DDA1V8}(4)			VOS high	800(2)	2.0	2.1	2.1	2.2	2.2	
			VOS low	600(3)	4.3	4.5	4.6	4.6	4.7	
			VOS high	800(2)	2.0	2.1	2.1	2.2	2.2	
			VOS low	600(3)	4.3	4.5	4.6	4.7	4.7	
$I_{DDA1V8ON}$			VOS high	800(2)	0.3	0.3	0.3	0.3	0.3	
			VOS low	600(3)	0.3	0.3	0.3	0.3	0.3	
			VOS high	800(2)	0.5	0.5	0.5	0.5	0.5	
			VOS low	600(3)	0.5	0.5	0.5	0.5	0.5	

1. Guaranteed by characterization results unless otherwise specified.
2. cpu_overdrive range frequency
3. cpu_nominal range frequency.
4. Sleep mode applies only to the CPU subsystem (CPU clock is stopped). PLL clock configuration changes.

Table 31. Current consumption in Stop mode

Symbol	Conditions		Typ	Max(1) SMPS external				Unit
				T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD}	SMPS external, V_{DD} = 1.8 V	SVOS high	9.1	27.5	191.4	314.8	524.8	mA
I_{DDCORE}			273.4	278.5	306.2	329.1	373.0	µA
I_{DDA1V8}			61.7	65.1	83.4	95.0	114.4	
$I_{DDA1V8ON}$			41.7	41.7	56.7	64.4	76.2	

1. Guaranteed by characterization results unless otherwise specified.

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Table 32. Current consumption in Standby mode

Symbol	Conditions		Typ	Max(1)				Unit
				T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD}	IWDG off, V_{DD} = 1.8 V	Backup RAM OFF RTC and LSE OFF	1.40	1.57	1.73	1.94	2.26	µA
		Backup RAM ON RTC and LSE OFF	1.40	1.58	1.77	2.01	2.39	
		Backup RAM OFF RTC and LSE OFF	1.40	1.57	1.73	1.94	2.26	
		Backup RAM ON RTC and LSE OFF	1.40	1.58	1.76	2.01	2.39	
	IWDG off, V_{DD} = 3.3 V	Backup RAM OFF RTC and LSE OFF	47	66	306	504	801	mA
		Backup RAM ON RTC and LSE OFF	48	69	339	571	927	
		Backup RAM OFF RTC and LSE OFF	48	66	306	503	800	
		Backup RAM ON RTC and LSE OFF	48	69	339	570	927	
$I_{DDA18ON}$	IWDG off	Backup RAM OFF RTC and LSE OFF	42	80	122	133	143	µA
		Backup RAM ON RTC and LSE OFF	42	80	122	133	143	
		Backup RAM OFF RTC and LSE OFF	42	80	122	133	143	
		Backup RAM ON RTC and LSE OFF	42	80	122	133	143	

1. Guaranteed by characterization, unless otherwise specified.

Table 33. Current consumption in V_{BAT} mode

Symbol	Conditions		Typ	Max(1)				Unit
				T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDVBAT}	V_{DD} = 3.3 V	Backup RAM OFF RTC and LSE(2)	-	36.5	41.2	62.7	89.8	µA
		Backup RAM ON RTC and LSE OFF	-	29.2	79.9	147.3	232.4	
		Backup RAM OFF RTC and LSE OFF	20.3	20.7	45.7	66.5	92.1	
		Backup RAM ON RTC and LSE OFF	21.6	23.7	85.60	145.9	233.5	

1. Guaranteed by characterization, unless otherwise specified.
2. LSE system modes Vsw domain only.

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I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up or pull-down generate current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Section 5.3.16*.

For the output pins, any internal or external pull-up or pull-down and external load must also be considered to estimate the current consumption.

An additional current consumption is due to I/Os configured as inputs when an intermediate voltage level is applied externally. This is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is the case of ADC input pins, which must be configured as analog inputs.

Caution: Any floating input pin can settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must be configured in analog mode, or forced internally to a definite digital value. This can be done by using pull-up/down resistors, or by configuring the pins in output mode.

I/O dynamic current consumption

The I/Os used in application contribute to the consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the pin circuitry, and to charge/discharge the capacitive load (internal and external) connected to it:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where:

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the I/O supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$
  - C_{INT} is the I/O pin capacitance
  - C_{EXT} is any connected external device pin capacitance

5.3.6 Wake-up time from low-power modes

The times given in *Table 34* are measured starting from the wake-up event trigger up to the first instruction executed by the CPU.

All timings are derived from tests performed under ambient temperature, V_{DD} and $V_{DDA18AON}$ = 1.8 V, V_{DDCORE} at nominal voltage.

General conditions unless otherwise noted:

- CM55 CPU software in SRAMx
- CPU goes to low power mode after WFI instruction.

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Table 34. Low-power mode wake-up timings(1)(2)

Symbol	Parameter	Conditions	Typ	Unit
$t_{WU(Sleep)}$	Wake-up time from Sleep	-	38	CPU clock cycles
$t_{WUDSTOP}$	Wake-up time from Stop	SVOS HIGH, HSI 64 MHz, clock disabled	10	µs
		SVOS HIGH, HSI 64 MHz, clock enabled	5	
		SVOS HIGH, MSI 4 MHz, clock disabled	65	
		SVOS HIGH, MSI 4 MHz, clock enabled	55	
t_{WUSTBY}	Wake-up time from Standby mode	-	400	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Measured from the wake-up event to the point in which the application code reads the first instruction.

5.3.7 External clock sources characteristics

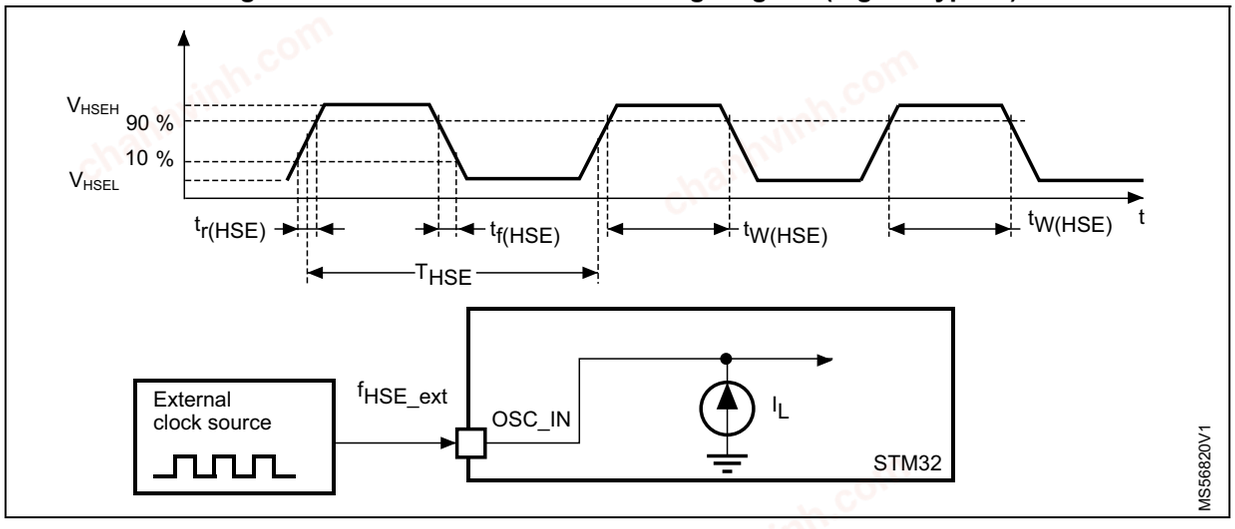
HSE clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

Digital and analog bypass modes are available.

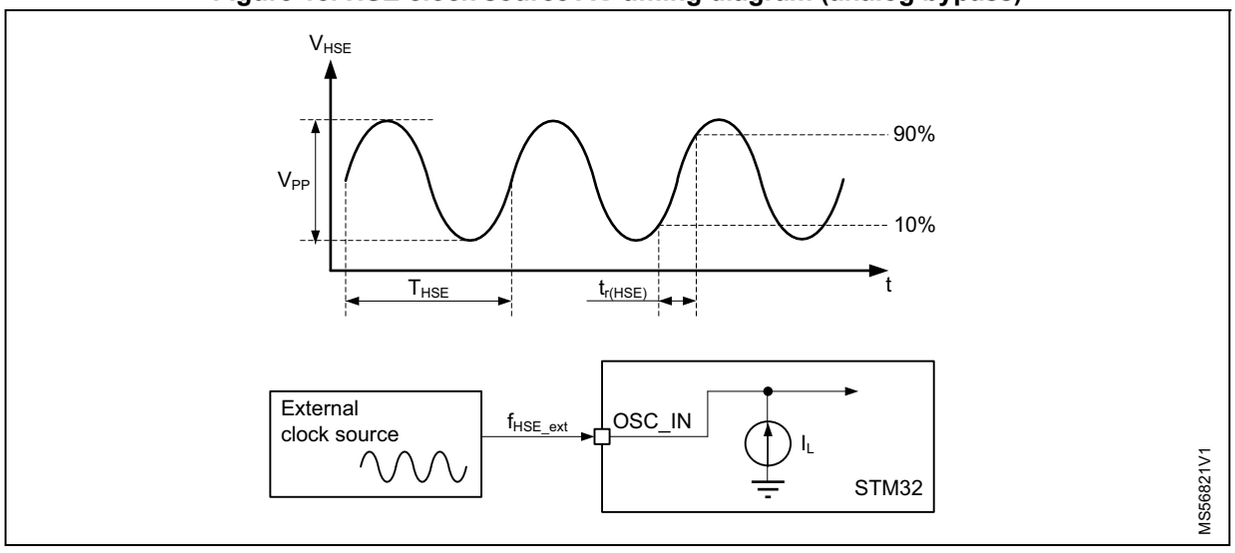
The external clock signal must respect the requirements specified in *Section 5.3.16*. The recommended clock input waveform is shown in *Figure 17* for digital bypass mode and in *Figure 18* for analog bypass mode. In the latter, the clock can be a sinusoidal waveform.

Figure 17. HSE clock source AC timing diagram (digital bypass)



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Figure 18. HSE clock source AC timing diagram (analog bypass)



The characteristics of digital and analog bypass are defined in the following tables.

Table 35. HSE clock characteristics (digital bypass)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source	1.8 V range	16	40	48	MHz
V_{HSEH}	OSC_IN high level voltage	1.8 V only	0.7 x $V_{DDA18AON}$	-	$V_{DDA18AON}$	V
V_{HSEL}	OSC_IN low level voltage		-	-	0.3 x $V_{DDA18AON}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	-	7	-	-	ns

1. Specified by design, not tested in production.

Table 36. HSE clock characteristics (analog bypass)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{HSE_ext}	User external clock source	1.8 V range	16	40	48	MHz
	Duty cycle		45	50	55	%
	Duty cycle deterioration		-	±10	±30	
V_{HSEH}	OSC_IN high level voltage	-	0.7 x $V_{DDA18AON}$	-	$V_{DDA18AON}$	V
V_{PP}	OSC_IN peak to peak amplitude	-	V_{SS}	-	0.67 x $V_{DDA18AON}$(2)	
$t_{SU(HSE)}$	Startup time	V_{DD} stabilized	-	1	10(3)	µs
$t_{r(HSE)}$ $t_{f(HSE)}$	Rise and fall time (10 to 90% threshold levels of the input peak to peak amplitude	-	0.05 x t_{HSE}	-	0.3 x t_{HSE}	ns

1. Specified by design, not tested in production.
2. Minimum peak-to-peak amplitude, 25 °C, 0.1 < V_{DC} < $V_{DDA18AON}$ - 0.1 V (V_{DC} is the DC component of the input signal).
3. Maximum start-up time is obtained with 200 mV peak-to-peak amplitude.

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HSE clock generated from a crystal/ceramic resonator

The clock can be supplied with a 16 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

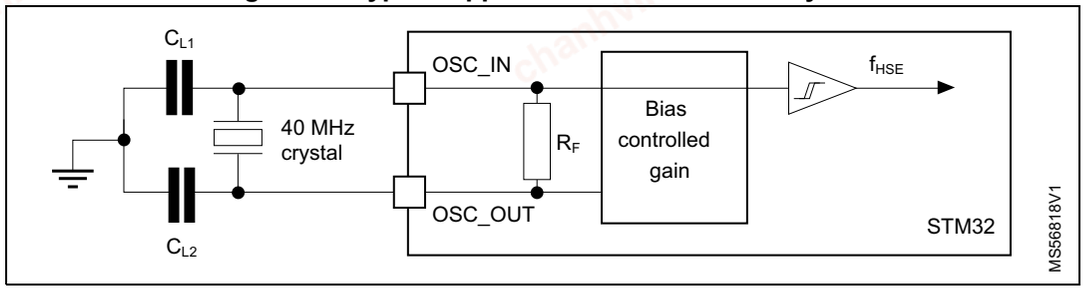
Table 37. HSE clock characteristics generated from crystal/ceramic resonator(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{HSE_ext}	User external clock source	1.8 V range	16	40	48	MHz
$G_{mcritmax}$	Maximum critical crystal gm	Startup	-	-	1.95	mA/V
$I_{DD(HSE)}$	Current consumption on $V_{DDA18AON}$	Startup	-	-	10	mA
		V_{DD} =1.8 V, R_m= 400 Ω, C_L = 6 pF, 48 MHz	-	4.8	-	
$t_{SU(HSE)}$	Startup time	V_{DD} stabilized	-	2	-	ms
R_F	Internal feedback equivalent resistor	-	-	250	-	kΩ

1. Specified by design, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 19*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance, which is the series combination of C_{L1} and C_{L2}. The PCB and pin capacitance must be included (4 pF can be used as a rough estimate of the combined pin and board capacitance).

Figure 19. Typical application with a 40 MHz crystal



Note: For information on selecting the crystal, refer to AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs", available from www.st.com.

LSE user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal must respect the values indicated in *Table 53*. The recommended clock input waveforms are shown in *Figure 20* for digital bypass and *Figure 21* for analog bypass.

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Figure 20. LSE clock source AC timing diagram (digital bypass)

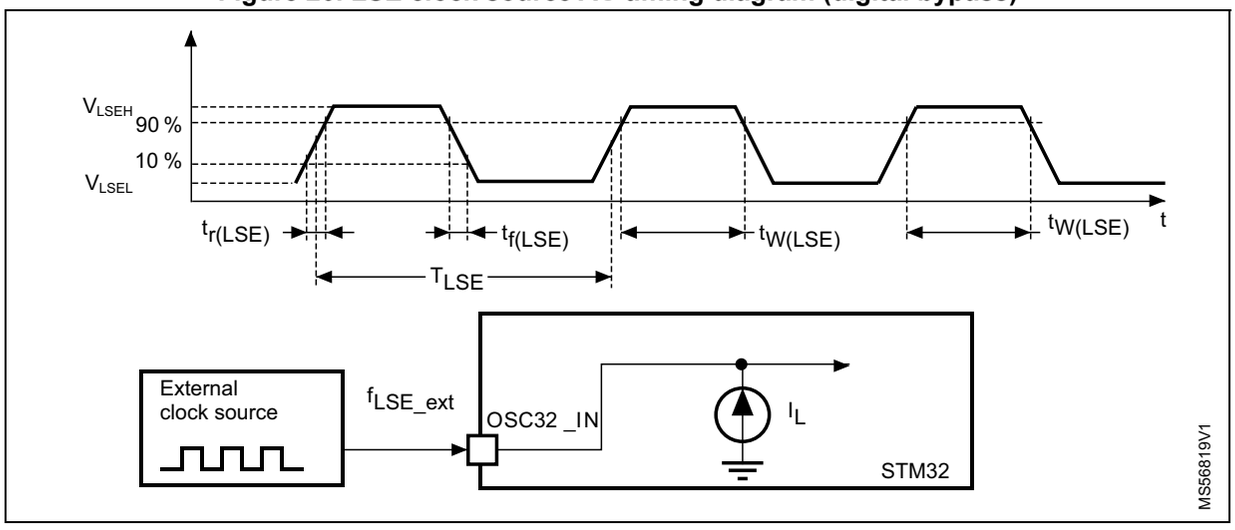
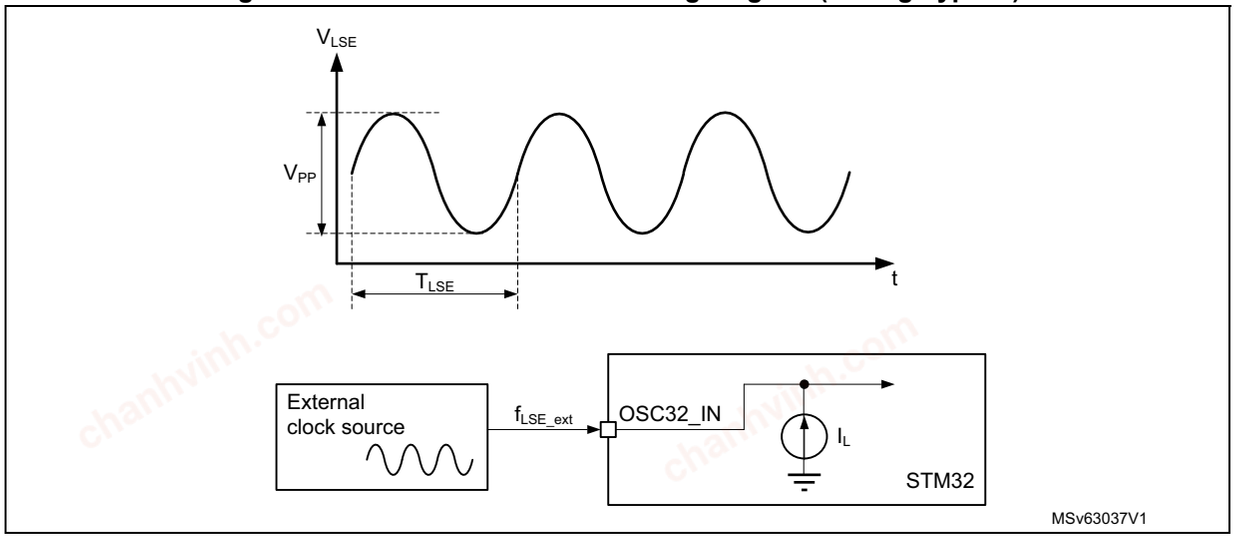


Figure 21. LSE clock source AC timing diagram (analog bypass)



The characteristics of digital and analog bypass are defined in the following tables.

Table 38. LSE clock characteristics (digital bypass)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source	-	-	32.768	-	kHz
V_{LSEH}	OSC_IN high level voltage	-	0.75 x V_{SW}	-	V_{SW}(2)	V
V_{LSEL}	OSC_IN low level voltage	-	-	-	0.25 x V_{SW}	
$t_{w(LSE}$	OSC_IN high or low time	-	250	-	-	ns

1. Specified by design, not tested in production.
2. V_{SW} is equal to V_{DD} when present, to V_{BAT} otherwise.

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Table 39. LSE clock characteristics (analog bypass)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source	-	-	32.768	-	kHz
V_{LSE}	Absolute input range	-	0	-	V_{SW}(2)	V
V_{PP}	OSC_IN peak to peak amplitude	-	0.2(3)	1	-	

1. Specified by design, not tested in production.
2. V_{SW} is equal to V_{DD} when present, to V_{BAT} otherwise.
3. Minimum peak-to-peak amplitude, 25 °C, 0.1 < V_{DC} < $V_{DDA18AON}$ - 0.1 V (V_{DC} is the DC component of the input signal).

LSE clock generated from a crystal/ceramic resonator

The low-speed external clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on its characteristics (frequency, package, accuracy).

Table 40. LSE clock characteristics generated from crystal/ceramic resonator(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{LSE}	Oscillator frequency	-	-	32.768	-	kHz
$G_{mcritmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, medium-low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, medium-high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, high drive capability	-	-	2.7	
t_{SU}(2)	Startup time	V_{SW} stabilized	-	2	-	s

1. Specified by design, not tested in production.
2. Startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator, it can vary significantly with the crystal manufacturer.

5.3.8 External clock source security characteristics

Table 41. High speed external user clock security system (HSE CSS)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DCM(HSE_CSS)}$	Time to detect clock missing	f_{HSE} = 48 MHz	-	1	2	µs

1. Specified by design, not tested in production.

Table 42. Low speed external user clock security system (LSE CSS)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DCM(LSE_CSS)}$	Time to detect clock missing	-	-	-	300	µs
$f_{MAX(LSE_CSS)}$	Cutoff frequency	-	-	-	2	MHz

1. Specified by design, not tested in production.

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5.3.9 Internal clock source characteristics

The parameters given in the following tables are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 43. 64 MHz high-speed internal (HSI) oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}(2)	Frequency	$V_{DDA18AON}$ = 1.8 V, T_J = 30 °C	63.68	64	64.32	MHz
TRIM	User trimming step	-	-	0.25	0.5	%
$DuCy_{HSI}$	Duty cycle	-	40	-	60	
$\Delta_{VDDA18AON(HSI)}$ + $\Delta_{TJ(HSI)}$	Oscillator frequency drift over voltage and temperature variation (after factory calibration)	T_J = -40 to 125 °C	-5	-	5	
$t_{su(HSI)}$	Startup time (from enable rise to first output clock edge)	-	-	-	3	µs
$t_{stab(HSI)}$	Stabilization time	1% of target frequency	-	-	5	
$I_{VDDCORE(HSI)}$	Supply current on V_{DDCORE}	-	-	-	10	µA
$I_{VDD18AON(HSI)}$	Supply current on $V_{DDA18AON}$	-	-	300	400	

1. Evaluated by characterization, not tested in production unless otherwise specified.
2. Guaranteed by test in production.

Table 44. Low power internal RC (MSI) oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	Frequency	V_{DDCORE} = 0.81 V, T_J = 30 °C	MSIFREQSEL = 0(2)	3.956	4	4.044	MHz
			MSIFREQSEL = 1	15.824	16	16.176	
TRIM	Trimming step	Trimming code is not a multiple of 32		-	0.8	1.1	%
		Trimming code is a multiple of 32		-	-2.5	-3.8	
$DuCy_{HSI}$	Duty cycle	At trimmed frequency		45	-	55	
$\Delta_{TJ(MSI)}$	Frequency drift over temperature	T_J = -40 to 125 °C		-7	-	+7	
$t_{su(HSI)}$	Start-up time	-		-	-	3.5	µs
$I_{VDDCORE(HSI)}$	Supply current on V_{DDCORE}	4 MHz	MSIFREQSEL = 0	-	20	22	µA
		16 MHz	MSIFREQSEL = 1	-	60	68	

1. Evaluated by characterization, not tested in production unless otherwise specified.
2. Guaranteed by test in production.

Table 45. 32 kHz low-speed internal (LSI) oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	T_J = 30 °C	30.5	32	33.5	kHz
		T_J = -40 to 125 °C	28.8	32	33.6	

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Table 45. 32 kHz low-speed internal (LSI) oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(LSI)}$	Start-up time (from enable rise to first output clock edge)	-	-	-	180	µs
$I_{VSW(LSI)}$	Supply current on V_{SW}	-	-	250	500	nA

1. Evaluated by characterization, not tested in production unless otherwise specified.

5.3.10 PLL characteristics

The parameters given in *Table 46* are derived from tests performed under temperature and supply voltage conditions summarized in *Table 22*.

Table 46. PLL1 to PLL4 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Normal mode	5	-	64	MHz
		Sigma delta mode	10	-	64	
f_{PFD}	PFD input clock	Normal mode	5	f_{PLL_IN} / FREFDIV	50	
		Sigma delta mode	10	-	min(50, f_{VCO} / 20)	
$f_{FOUTPOSTDIV}$	Divided output clock		16.32	-	3200	MHz
	Divided output clock duty cycle	Division by 1	48	50	52	%
		Even division	48	50	52	
		Odd division	47	50	53	
f_{VCO}	PLL VCO output		800	-	3200	MHz
t_{LOCK}	PLL lock time	Frequency lock	-	-	400	1 / f_{PFD} cycles
		f_{PFD} = 40 MHz (f_{PLL_IN} = 40 MHz, FREFDIV = 1)	-	-	10	µs
Jitter	RMS period jitter	f_{VCO} = 3200 MHz	-	-	±0.26	ps
	RMS integrated jitter (10 kHz - 20 MHz)	f_{VCO} = 3200 MHz, f_{PFD} = 25 MHz, integer divider	-	±2.7	±6.6	
		f_{VCO} = 3200 MHz, f_{PFD} = 25 MHz, fracN divider	-	-	±11.9	
$I_{VDDA18PLL}$	PLL supply current on $V_{DDA18PLL}$ (analog)	f_{VCO} = 3200 MHz, FBDIV < 256	-	5750	6850	µA
		f_{VCO} = 3200 MHz, FBDIV > 256	-	7050	8450	
		f_{VCO} = 800 MHz, FBDIV < 256	-	715	860	
$I_{VDDCORE(PLL)}$	PLL supply current on V_{DDCORE} (0.81 V)	f_{VCO} = 3200 MHz	-	1200	3650	
		f_{VCO} = 800 MHz	-	295	910	

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1. Specified by design, not tested in production unless otherwise specified.

5.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows the reduction of electromagnetic interferences (see *Section 5.3.13*). It is available only on PLL2 to PLL4.

Table 47. PLL2 to PLL4 SSCG constraints

Symbol	Parameter	Min	Typ	Max	Unit
f_{MOD}	Modulation frequency	5.2	-	391	kHz
M_D	Peak modulation depth	0.1	-	3.1	%

5.3.12 OTP characteristics

The characteristics are given at T_J = -40 to 125 °C, unless otherwise specified.

Table 48. OTP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OTP(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Programming	-	3.8	10	mA
		Reading	-	0.66	1.13	
		Power down	-	5	132	µA
$I_{OTP(VDDCORE)}$	Supply current on V_{DDCORE}	Programming	-	0.09	0.45	mA
		Reading	-	1.8	3.6	
		Power down	-	8	500	µA

1. Evaluated by characterization, not tested in production unless otherwise specified.

5.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs as follows:

- ESD (electrostatic discharge), positive and negative: applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB (fast transient voltage burst), positive and negative: applied to V_{DD} and V_{SS} pins through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 49*. They are based on the EMS levels and classes defined in AN1709 “*EMC design guide for STM8, STM32 and legacy MCUs*”.

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Table 49. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to apply on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{PLL1} = 1200 MHz, $f_{ck_icn_hs_mcu}$ = 600 MHz, VFBGA264 package, conforming to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to apply through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance		5A

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software.

Good EMC performance is highly dependent on the user application, and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the requested EMC level.

Software recommendations

The software flow must include the management of runaway conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or on the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specified values. When an unexpected behavior is detected, the software can be hardened to prevent the occurrence of unrecoverable errors. See AN1015 “*Software techniques for improving microcontrollers EMC performance*” for more details.

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with the IEC 61967-2 standard, which specifies the test board and the pin loading.

Table 50. EMI characteristics for f_{HSE} = 32 MHz and f_{HCLK} = 100 MHz(1)

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak level(2)	V_{DD} = 3.6 V, T_A = 25 °C, VFBGA264 package, SMPS on, $f_{ck_icn_hs_mcu}$ = 800 MHz, compliant with IEC 61967-2	0.1 MHz to 30 MHz	9	dBµV
			30 MHz to 130 MHz	13	
			130 MHz to 1 GHz	13	
			1 GHz to 2 GHz	7	
	Level(3)		EMI level	3	-

1. Evaluated by characterization, not tested in production.

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2. Refer to AN1709, “EMI radiated test” section.
3. Refer to AN1709, “EMI level classification” section.

5.3.14 Electrical sensitivity characteristics

Based on three different tests (ESD, latch-up) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 51. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions	Package	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to ANSI/ESDA/JEDEC JS-001	All	2	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to ANSI/ESDA/JEDEC JS-002		C1	250	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. 400 V for USB_PD_CC1 and USB_PD_CC2 pins.

Static latch-up

The following complementary static tests are required on three parts to assess the latch-up performance:

- a supply overvoltage is applied to each power supply pin
- a current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 52. Electrical sensitivity(1)

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_J = 130 °C conforming to JESD78	II.A

1. Evaluated by characterization, not tested in production, unless otherwise specified.

5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller if abnormal injection accidentally happens, some susceptibility tests are performed on a sample basis during device characterization.

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5.3.16 I/O port characteristics

General input/output characteristics

The parameters given in *Table 53* are derived from tests performed at ambient temperature and under the supply voltage conditions summarized in *Table 22*. All I/Os are designed as CMOS- and TTL-compliant. For additional informations see AN4899 “*STM32 microcontroller GPIO hardware settings and low-power consumption*”.

Table 53. I/O static characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	1.62 V ≤ V_{DDxx} ≤ 1.98 V	0.36 x V_{DDxx}	-	-	V
		2.7 V ≤ V_{DDxx} ≤ 3.6 V	0.4 x V_{DDxx} - 0.27	-	-	
V_{IH}	Input high level voltage	1.62 V ≤ V_{DDxx} ≤ 1.98 V	0.62 x V_{DDxx}	-	-	
		2.7 V ≤ V_{DDxx} ≤ 3.6 V	0.52 x V_{DDxx} - 0.11	-	-	
V_{hys}(2)	Input hysteresis	1.62 V ≤ V_{DDxx} ≤ 1.98 V	-	0.45	-	
		2.7 V ≤ V_{DDxx} ≤ 3.6 V	-	0.45	-	
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 5.5 mA, Speed 00, 1.62 V < V_{DDxx} < 1.98 V	-	-	0.45	V
		CMOS port, I_{IO} = 8 mA, Speed 01, 1.62 V < V_{DDxx} < 1.98 V	-	-	0.45	
		CMOS port, I_{IO} = 11 mA, Speed 10, 1.62 V < V_{DDxx} < 1.98 V	-	-	0.45	
		CMOS port, I_{IO} = 16 mA, Speed 11, 1.62 V < V_{DDxx} < 1.98 V	-	-	0.45	
		CMOS port, I_{IO} = 6.5 mA, Speed 00, 2.7 V < V_{DDxx} < 3.6 V	-	-	0.4	
		CMOS port, I_{IO} = 10 mA, Speed 01, 2.7 V < V_{DDxx} < 3.6 V	-	-	0.4	
		CMOS port, I_{IO} = 13 mA, Speed 10, 2.7 V < V_{DDxx} < 3.6 V	-	-	0.4	
		CMOS port, I_{IO} = 20 mA, Speed 11, 2.7 V < V_{DDxx} < 3.6 V	-	-	0.4	

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Table 53. I/O static characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	CMOS port, I_{IO} = 5.5 mA, Speed 00, 1.62 V < V_{DDxx} < 1.98 V	V_{DDxx} - 0.45	-	-	V
		CMOS port, I_{IO} = 8 mA, Speed 01, 1.62 V < V_{DDxx} < 1.98 V	V_{DDxx} - 0.45	-	-	
		CMOS port, I_{IO} = 11 mA, Speed 10, 1.62 V < V_{DDxx} < 1.98 V	V_{DDxx} - 0.45	-	-	
		CMOS port, I_{IO} = 16 mA, Speed 11, 1.62 V < V_{DDxx} < 1.98 V	V_{DDxx} - 0.45	-	-	
		CMOS port, I_{IO} = 6.5 mA, Speed 00, 2.7 V < V_{DDxx} < 3.6 V	V_{DDxx} - 0.4	-	-	
		CMOS port, I_{IO} = 10 mA, Speed 01, 2.7 V < V_{DDxx} < 3.6 V	V_{DDxx} - 0.4	-	-	
		CMOS port, I_{IO} = 13 mA, Speed 10, 2.7 V < V_{DDxx} < 3.6 V	V_{DDxx} - 0.4	-	-	
		CMOS port, I_{IO} = 20 mA, Speed 11, 2.7 V < V_{DDxx} < 3.6 V	V_{DDxx} - 0.4	-	-	

1. V_{DDxx} stands for V_{DD}, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, or V_{DDIO5}.
2. Specified by design, not tested in production.

Table 54. Leakage characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
I_{leak}	TT-x input leakage	-	-	1500	nA
C_{IO}	I/O pin capacitance	-	5	-	pF

1. Evaluated by characterization, not tested in production.

Table 55. R_{PU}/R_{PD} characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor	1.62 V < V_{DDIO} < 1.98 V	30	40	50	kΩ
		2.7 V < V_{DDIO} < 3.6 V				
R_{PU}	Weak pull-down equivalent resistor	1.62 V < V_{DDIO} < 1.98 V				
		2.7 V < V_{DDIO} < 3.6 V				

Output driving current

The GPIOs can sink or source up to ±20 mA (depending on speed setup, supply voltage range and temperature). In the application, I/O drive current must be limited to respect the absolute maximum ratings specified in *Section 5.2*, in particular:

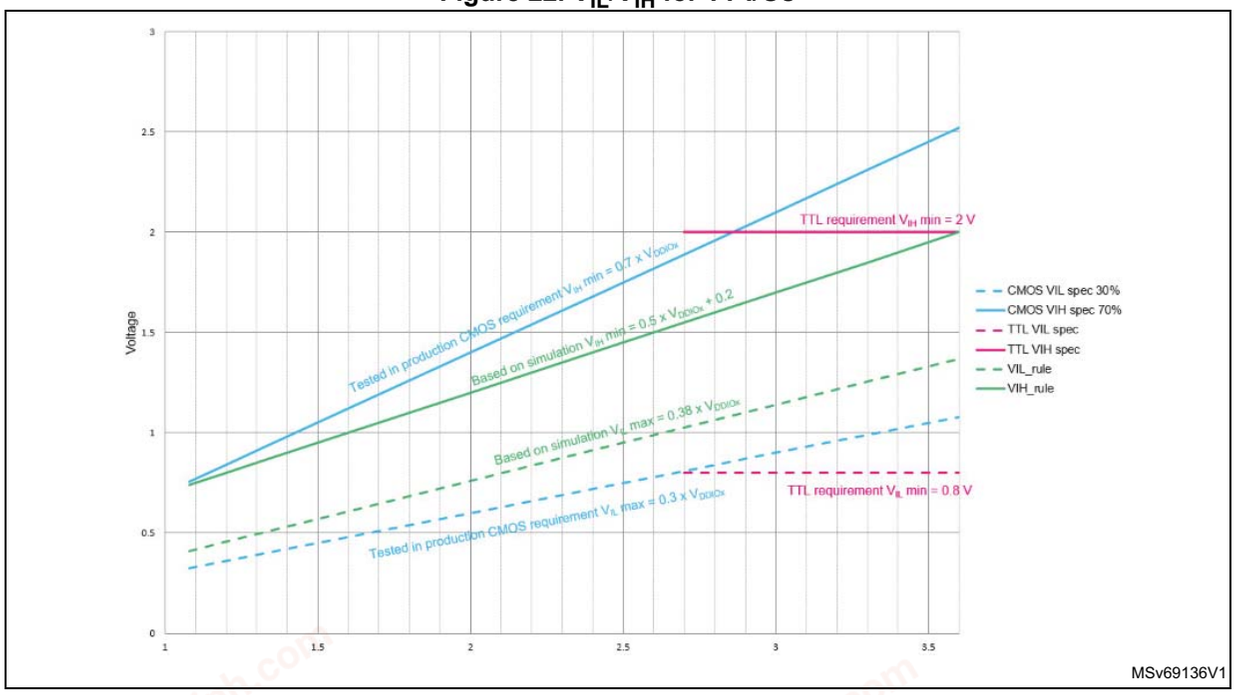
- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run mode consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 20*).

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- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run mode consumption of the MCU sink on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 20*).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22*.

Figure 22. V_{IL}/V_{IH} for TT I/Os



5.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 55*).

Unless otherwise specified, the parameters in *Table 56* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22*.

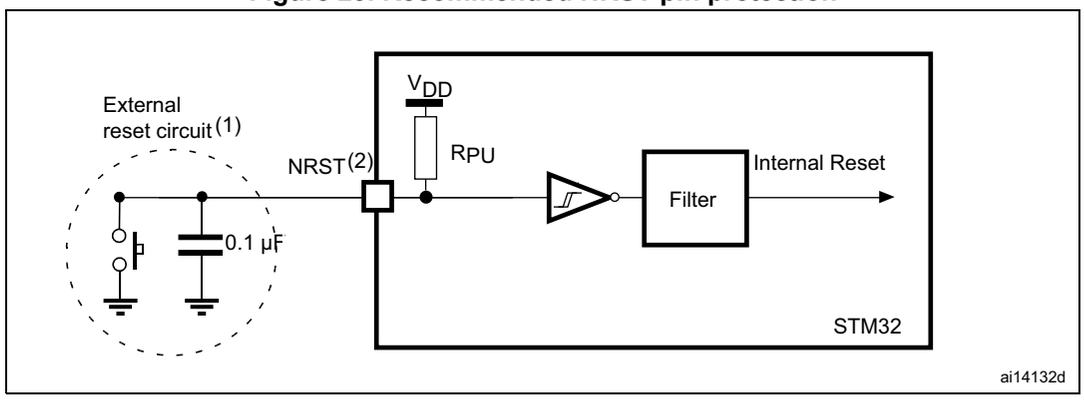
Table 56. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(1)	Weak pull-up equivalent resistor	-	30	40	50	kΩ
t_{GEN}	NRST minimum generated output pulse	-	17.5	-	-	µs
T_{FILT}	NRST input filtered pulse	-	-	-	50	ns
T_{NFILT}	NRST input not filtered pulse	-	150	-	-	
$V_{IL(NRST)}$	NRST input low-level voltage	-	-	-	0.65	V

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10%).

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Figure 23. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 56*. Otherwise, the reset is not taken into account by the device.

5.3.18 FMC characteristics

Unless otherwise specified, the parameters given in *Table 57* to *Table 74* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 × V_{DD}

Refer to *Section 5.3.16* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 24 to *Figure 27* represent asynchronous waveforms and *Table 57* to *Table 64* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime(ADDSET) = 0x1
- AddressHoldTime(ADDHLD) = 0x1
- DataSetupTime(DATAST) = 0x1 (except for asynchronous NWAIT mode for which DataSetupTime = 0x5)
- DataHoldTime(DATAHLD) = 0x1 (1 × $T_{fmc_ker_ck}$ for read operations and 2 × $T_{fmc_ker_ck}$ for write operations)
- ByteLaneSetup(NBLSET) = 0x1
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all timing tables, $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

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Table 57. Asynchronous non multiplexed SRAM/PSRAM/NOR read timings

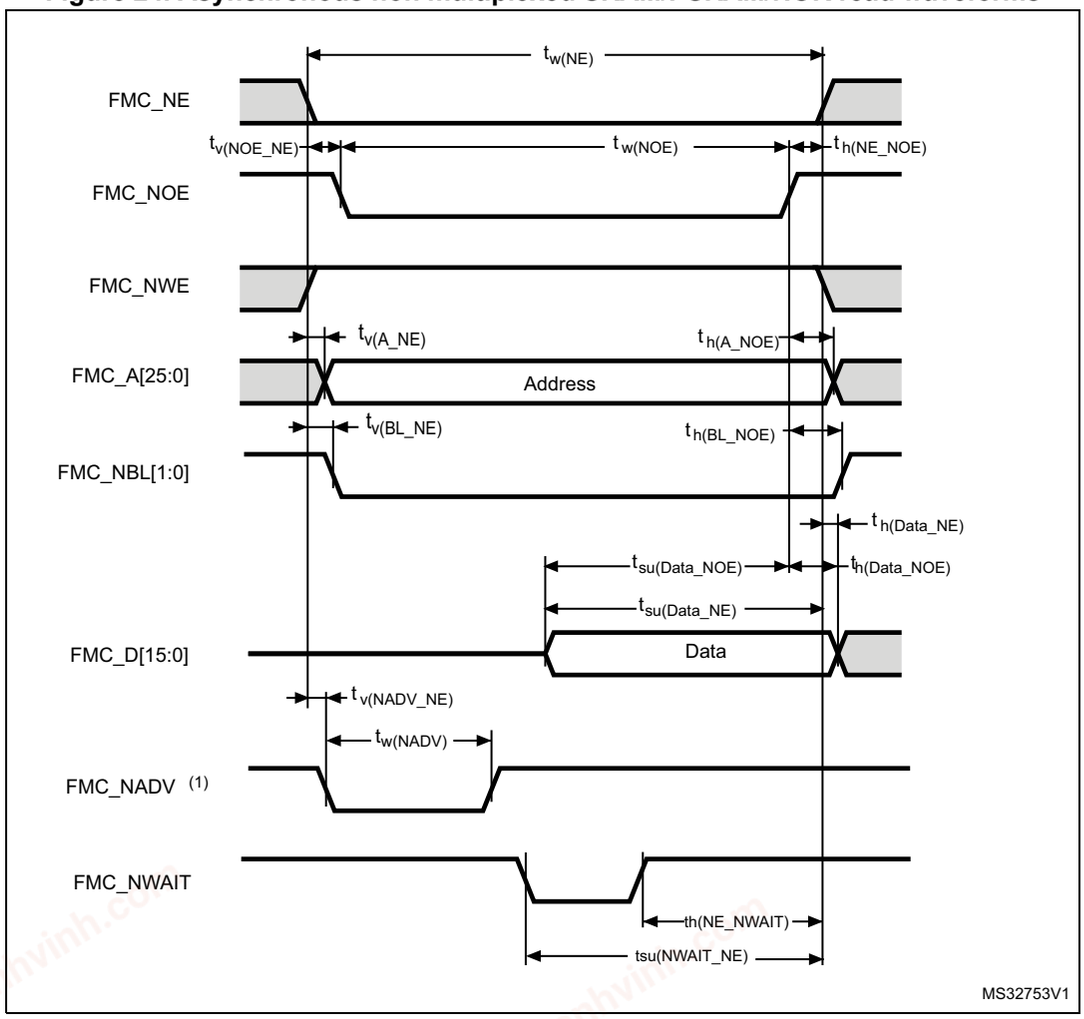
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3 \times T_{fmc_ker_ck} - 0.5$	$3 \times T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2 \times T_{fmc_ker_ck} - 0.5$	$2 \times T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	Address held until next read operation	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} + 17$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	16	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 1$	

Table 58. Asynchronous non multiplexed SRAM/PSRAM/NOR read-NWAIT timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8 \times T_{fmc_ker_ck} - 0.5$	$8 \times T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$7 \times T_{fmc_ker_ck} - 0.5$	$7 \times T_{fmc_ker_ck} + 1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck}$	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5 \times T_{fmc_ker_ck} + 15$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4 \times T_{fmc_ker_ck} + 12$	-	

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Figure 24. Asynchronous non multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C, and D only. In mode 1, FMC_NADV is not used.

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Table 59. Asynchronous non multiplexed SRAM/PSRAM/NOR write timings

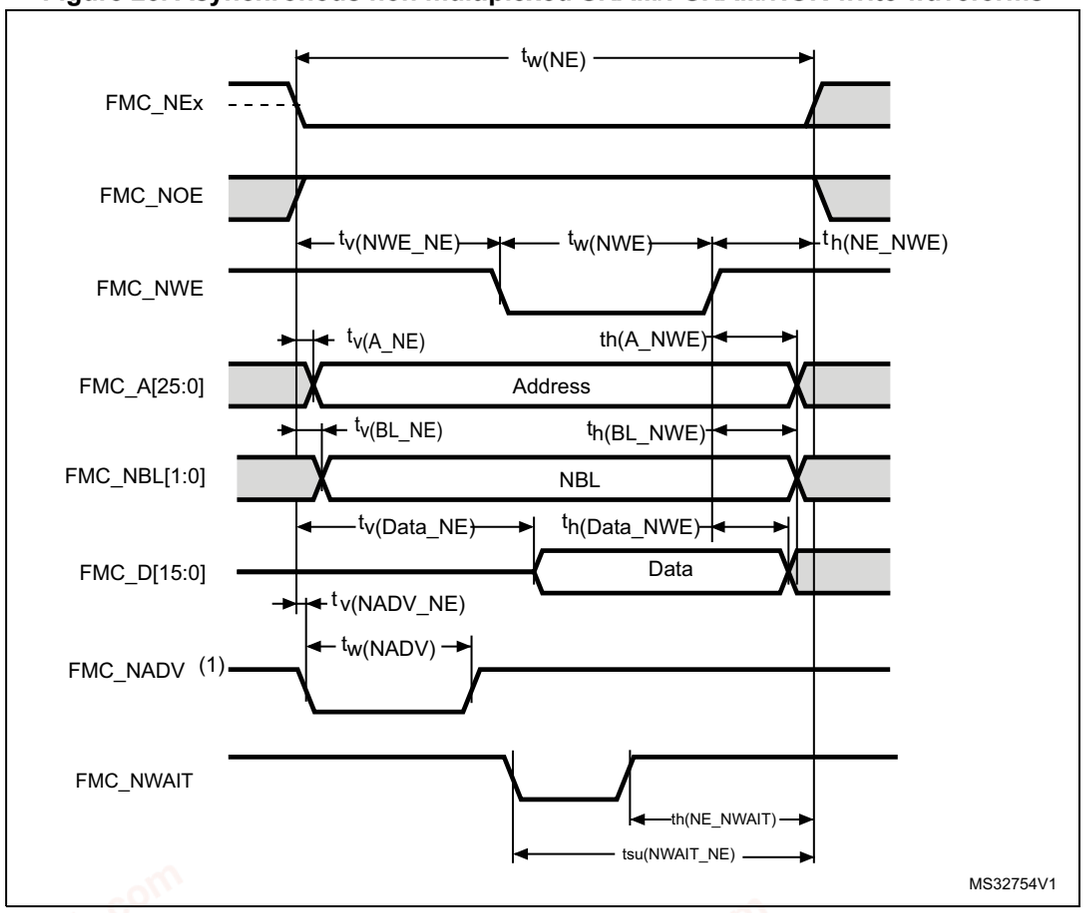
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3 \times T_{fmc_ker_ck} - 0.5$	$3 \times T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 4$	$T_{fmc_ker_ck} - 3$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} + 3$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$3 \times T_{fmc_ker_ck} - 1$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$3 \times T_{fmc_ker_ck} - 1.5$	-	
$t_{v(Data_NE)}$	FMC_NEx low to Data valid	-	2	
$t_{h(Data_NWE)}$	Data hold time after FMC_NEx high	$3 \times T_{fmc_ker_ck} - 1$	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 1$	

Table 60. Asynchronous non multiplexed SRAM/PSRAM/NOR write - NWAIT timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8 \times T_{fmc_ker_ck} - 0.5$	$8 \times T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$6 \times T_{fmc_ker_ck} - 0.5$	$6 \times T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5 \times T_{fmc_ker_ck} + 15$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4 \times T_{fmc_ker_ck} + 12$	-	

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Figure 25. Asynchronous non multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C, and D only. In mode 1, FMC_NADV is not used.

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Table 61. Asynchronous multiplexed PSRAM/NOR read timings

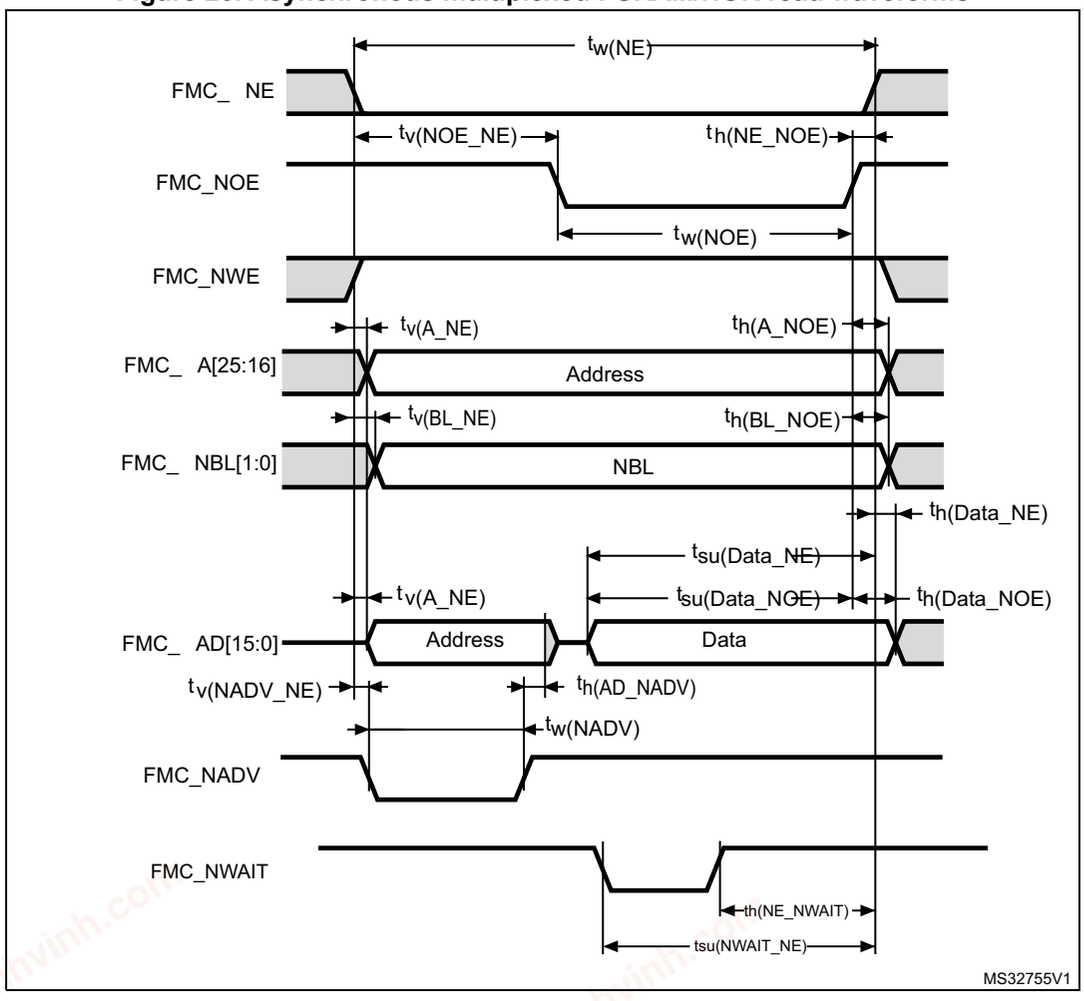
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4 \times T_{fmc_ker_ck} - 0.5$	$4 \times T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2 \times T_{fmc_ker_ck} - 1$	$2 \times T_{fmc_ker_ck} + 0.5$	
$t_{w(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 0.5$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck} - 1$	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	Address held until next read operation	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} + 17$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	16	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

Table 62. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9 \times T_{fmc_ker_ck} - 0.5$	$9 \times T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$6 \times T_{fmc_ker_ck} - 0.5$	$6 \times T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5 \times T_{fmc_ker_ck} + 15$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4 \times T_{fmc_ker_ck} + 12$	-	

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Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms



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Table 63. Asynchronous multiplexed PSRAM/NOR write timings

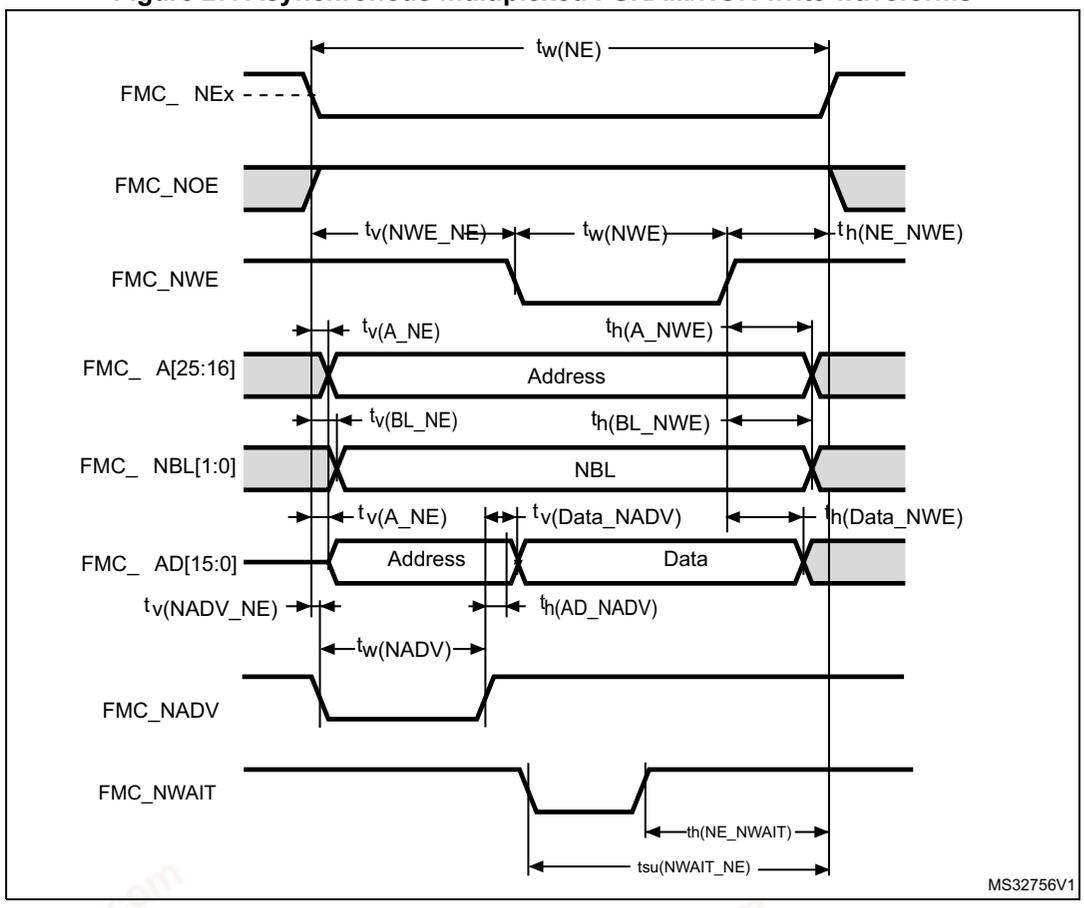
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4 \times T_{fmc_ker_ck} - 0.5$	$4 \times T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 4$	$T_{fmc_ker_ck} - 3$	
$t_{w(NWE)}$	FMC_NWE low time	$2 \times T_{fmc_ker_ck} - 0.5$	$2 \times T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} + 3$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	$T_{fmc_ker_ck} - 1.5$	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$3 \times T_{fmc_ker_ck} - 1$	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck} - 1.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0	
$t_{h(Data_NWE)}$	Data hold time after FMC_NEx high	-	$T_{fmc_ker_ck} + 2$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NEx high	$T_{fmc_ker_ck} - 1$	-	

Table 64. Asynchronous multiplexed PSRAM/NOR write - NWAIT timing

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9 \times T_{fmc_ker_ck} - 0.5$	$9 \times T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$7 \times T_{fmc_ker_ck} - 0.5$	$7 \times T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5 \times T_{fmc_ker_ck} + 15$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4 \times T_{fmc_ker_ck} + 12$	-	

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Figure 27. Asynchronous multiplexed PSRAM/NOR write waveforms



Synchronous waveforms and timings

Figure 28 to *Figure 31* represent synchronous waveforms and *Table 65* to *Table 68* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash memory; DataLatency = 0 for PSRAM

In all timing tables, $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period with the following FMC_CLK maximum values:

- For 1.65 V < V_{DD}< 3.6 V, FMC_CLK = 65 MHz at 20 pF (55 MHz when using NWAIT)

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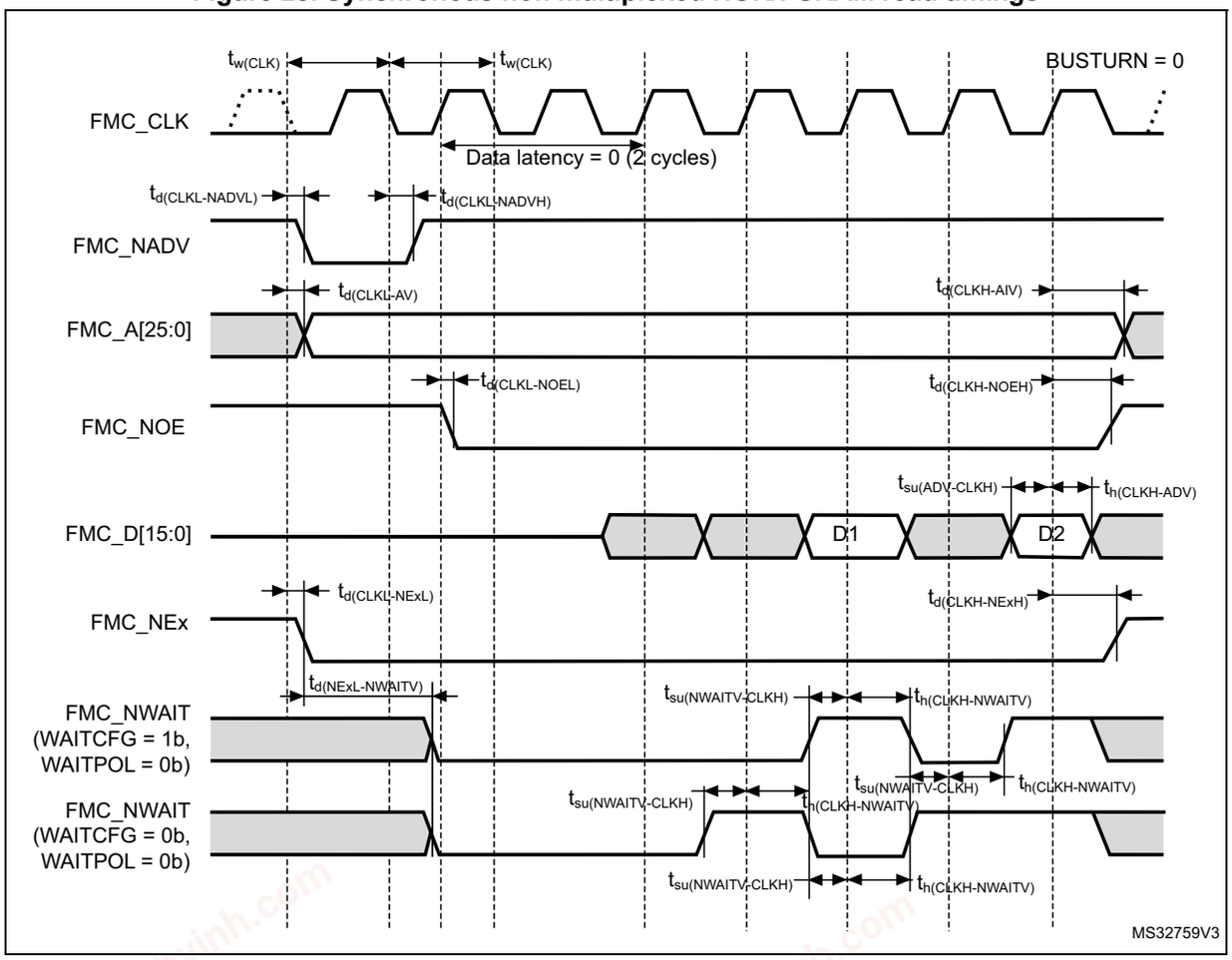
Table 65. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck} - 0.5$(2)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0…2)	-	5	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$R \times T_{fmc_ker_ck} / 2 + 5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16…25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16…25)	Address held until next read operation	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	0	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc_ker_ck} / 2 + 4$(2)	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0.5	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	4.5	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	0	-	
$T_{cew(NExL-NWAIT)}$	FMC_NWAIT valid after FMC_NEx low (x = 0…2)	-	(DATLAT + 2.5) × $T_{fmc_ker_ck}$ × R - 10.5	

1. Evaluated by characterization. Not tested in production.
2. Clock ratio R = FMC_CLK period / FMC_ker_CLK period.

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Figure 28. Synchronous non multiplexed NOR/PSRAM read timings



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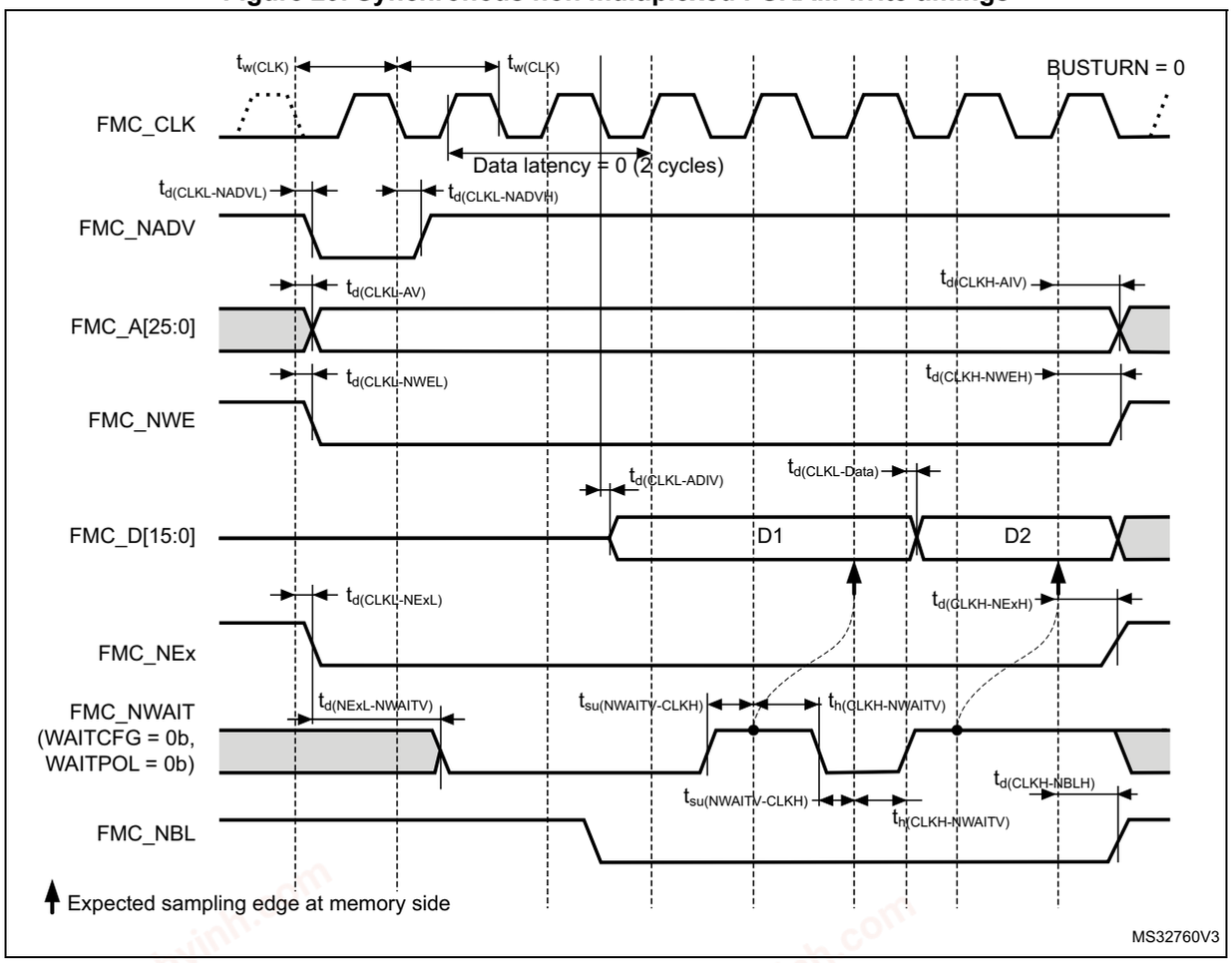
Table 66. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck} - 0.5$(2)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0…2)	-	5	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$R \times T_{fmc_ker_ck} / 2 + 5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16…25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16…25)	$R \times T_{fmc_ker_ck}$(2)	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R \times T_{fmc_ker_ck} / 2$(2)	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	0	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc_ker_ck} / 2$(2)	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	0	-	
$T_{cew(NExL-NWAIT)}$	FMC_NWAIT valid after FMC_NEx low (x = 0…2)	-	(DATLAT + 2.5) × $T_{fmc_ker_ck}$ × R - 10.5	-

1. Evaluated by characterization. Not tested in production.
2. Clock ratio R = FMC_CLK period / FMC_ker_CLK period.

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Figure 29. Synchronous non multiplexed PSRAM write timings



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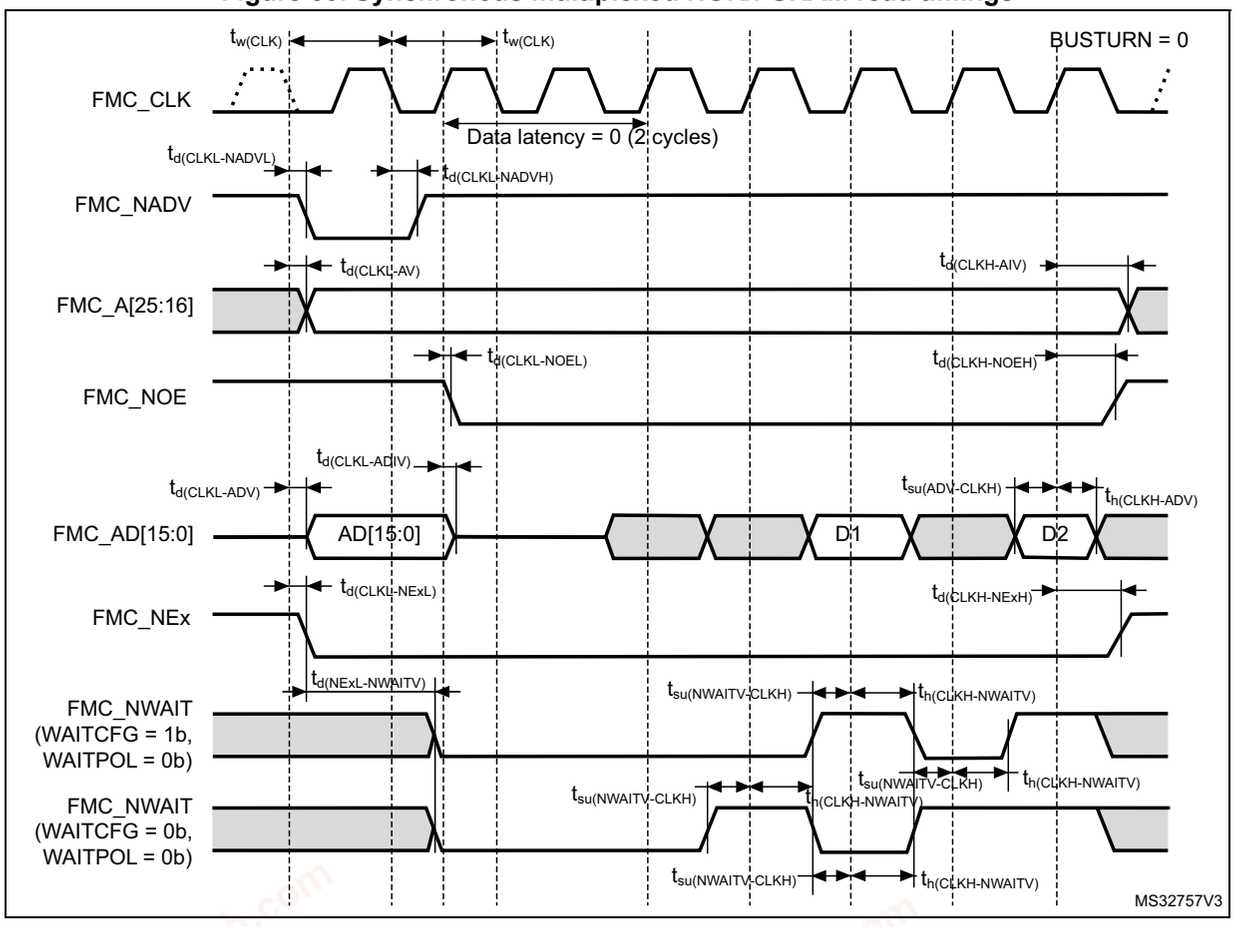
Table 67. Synchronous non multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck} - 0.5$(2)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0…2)	-	5	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$R \times T_{fmc_ker_ck}/2 + 5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x =16…25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x =16…25)	Address held until next read operation	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	0	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc_ker_ck}/2 + 4$(2)	-	
$t_{su(DV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	4.5	-	
$t_{h(CLKH-DV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	0	-	
$T_{cew(NExL-NWAIT)}$	FMC_NWAIT valid after FMC_NEx low (x = 0…2)	-	$(DATLAT + 2.5) \times T_{fmc_ker_ck} \times R - 10.5$	-

1. Evaluated by characterization. Not tested in production.
2. Clock ratio R = FMC_CLK period / FMC_ker_CLK period.

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Figure 30. Synchronous multiplexed NOR/PSRAM read timings



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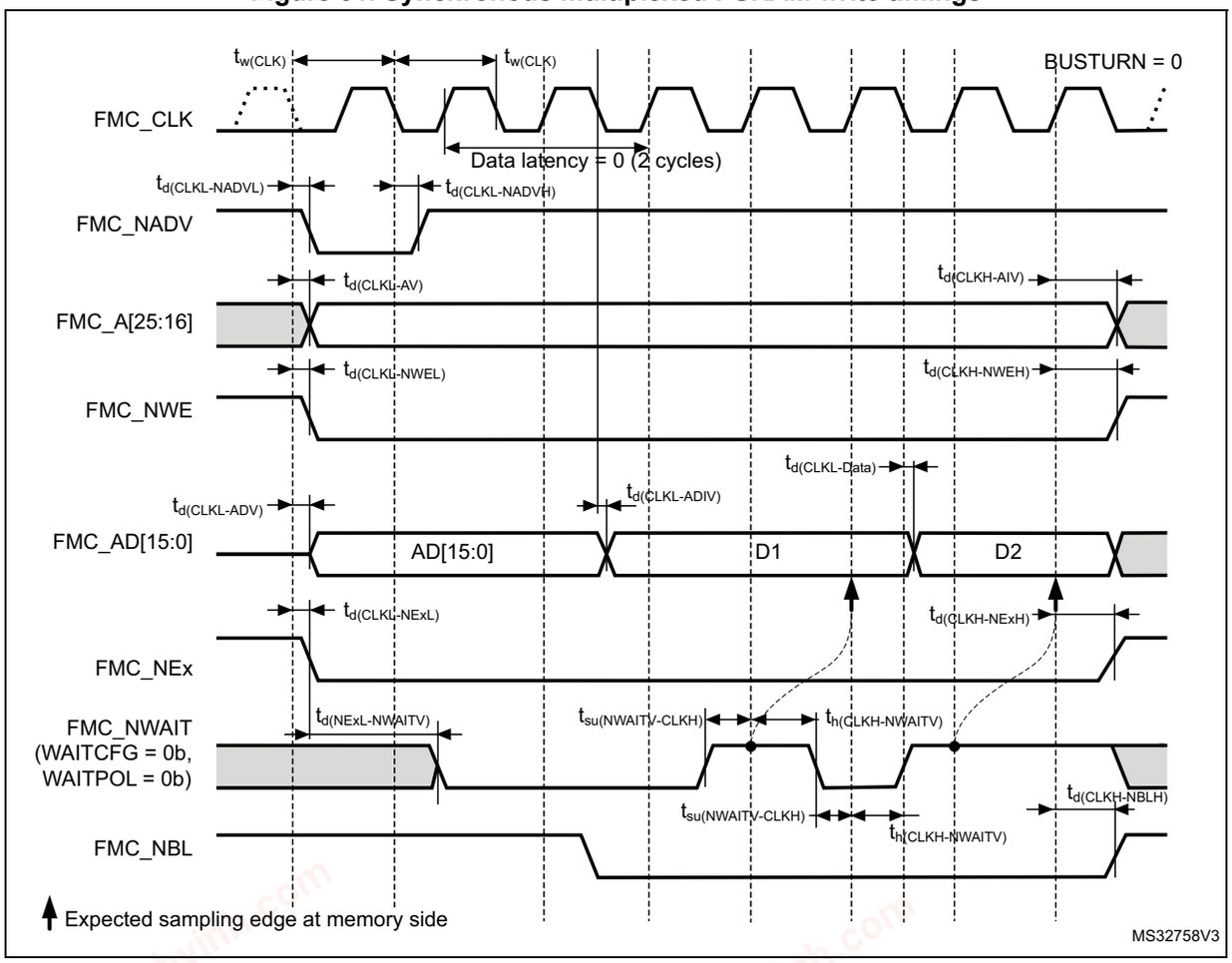
Table 68. Synchronous non multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck} - 0.5$(2)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0…2)	-	5	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$R \times T_{fmc_ker_ck}/2 + 5$(2)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x =16…25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x =16…25)	$R \times T_{fmc_ker_ck}$(2)	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R \times T_{fmc_ker_ck} / 2$(2)	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	0	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc_ker_ck} / 2$(2)	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	
$T_{cew(NExL - NWAIT)}$	FMC_NWAIT valid after FMC_NEx low (x = 0…2)	-	$(DATLAT + 2.5) \times T_{fmc_ker_ck} \times R - 10.5$	-

1. Evaluated by characterization. Not tested in production.
2. Clock ratio R = FMC_CLK period / FMC_ker_CLK period.

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Figure 31. Synchronous multiplexed PSRAM write timings



NAND flash memory controller waveforms and timings

Figure 32 and *Figure 33* represent synchronous waveforms, and *Table 69* and *Table 70* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- FMC_SetupTime = 0x01
- FMC_WaitSetupTime = 0x03
- FMC_HoldSetupTime = 0x02
- FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- Capacitive load C_L = 30 pF

In all timing tables, $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

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Table 69. NAND flash memory read cycles

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FMC_NOE low width	$4 \times T_{fmc_ker_ck} - 1$	$4 \times T_{fmc_ker_ck} + 1$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	15	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$2 \times T_{fmc_ker_ck} + 1.5$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3 \times T_{fmc_ker_ck} - 1$	-	

Figure 32. NAND controller waveforms for read access

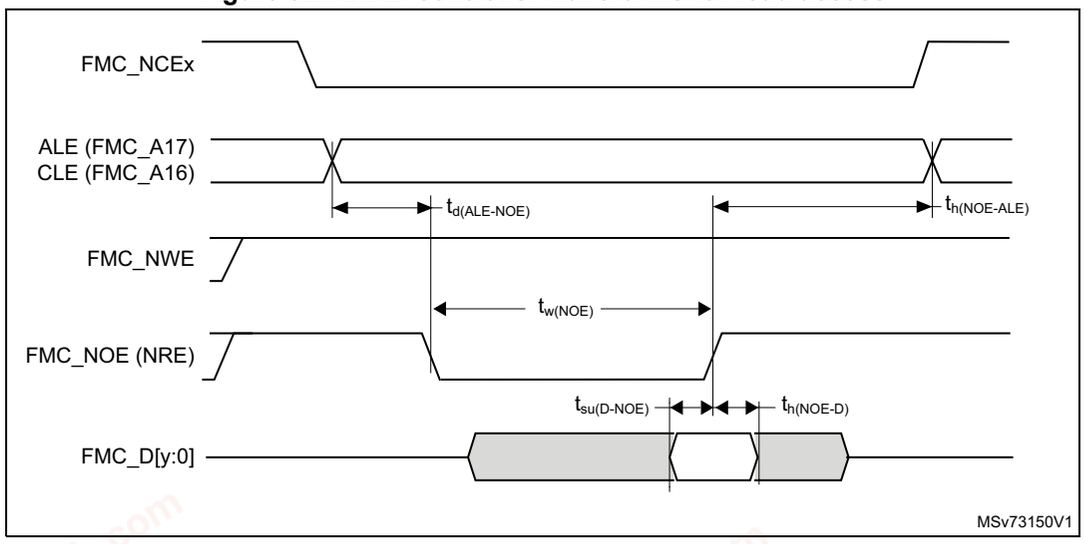
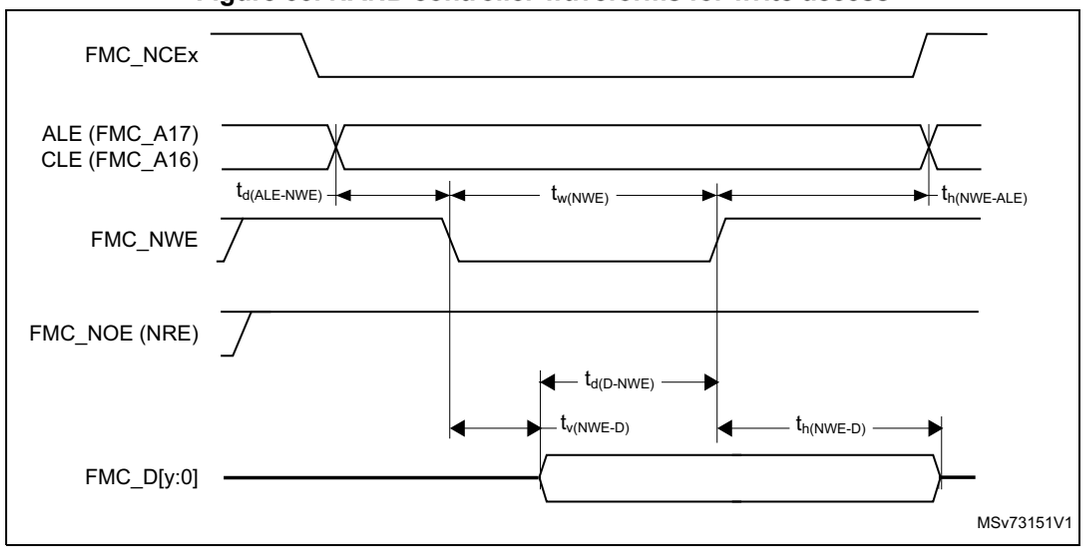


Table 70. NAND flash memory write cycles

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4 \times T_{fmc_ker_ck} - 1$	$4 \times T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	4	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$5 \times T_{fmc_ker_ck} - 1$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$4 \times T_{fmc_ker_ck} - 4.5$	-	
$t_{d(ALE_NWE)}$	FMC_ALE valid before FMC_NWE low	-	$2 \times T_{fmc_ker_ck} + 1.5$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3 \times T_{fmc_ker_ck} - 1$	-	

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Figure 33. NAND controller waveforms for write access



SDRAM waveforms and timings

In all timing tables, $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period, with primary interfaces and RETIME = 1:

- Maximum FMC_CLK = 166 MHz at 20 pF for 1.71 V < V_{DD} < 1.9 V
- Maximum FMC_CLK = 166 MHz at 20 pF for 2.7 V < V_{DD} < 3.6 V

Otherwise

- Maximum FMC_CLK = 70 MHz at 20 pF for 1.71 V < V_{DD}< 1.9 V
- Maximum FMC_CLK = 75 MHz at 20 pF for 2.7 V < V_{DD}< 3.6 V
- Maximum FMC_CLK = 80 MHz at 10 pF for 1.71 V < V_{DD} < 1.9 V

Table 71. SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2 × $T_{fmc_ker_ck}$ - 0.5	2 × $T_{fmc_ker_ck}$ + 0.5	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	1(2) / 5	-	
$t_{h(SDCLK\ H_Data)}$	Data input hold time	2(2) / 0.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1,5	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Evaluated by characterization. Not tested in production.
2. Primary interfaces used.

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Table 72. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2 $T_{fmc_ker_ck}$ - 0.5	2 $T_{fmc_ker_ck}$ + 0.5	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	1(2) / 5	-	
$t_{h(SDCLK\ H_Data)}$	Data input hold time	1.5(2) / 0.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1,5	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Evaluated by characterization. Not tested in production.
2. Primary interfaces used.

Table 73. SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2 $T_{fmc_ker_ck}$ - 0.5	2 $T_{fmc_ker_ck}$ + 0.5	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	1.5(2) / 5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	1	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Evaluated by characterization. Not tested in production.
2. Primary interfaces used.

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Table 74. LPSDR SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2 $T_{fmc_ker_ck}$ - 0.5	2 $T_{fmc_ker_ck}$ + 0.5	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	1.5(2) / 5.5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	1	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL-SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Evaluated by characterization. Not tested in production.
2. Primary interfaces used.

5.3.19 XSPI interface characteristics

Unless otherwise specified, the parameters given in *Table 75* for XSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V

Refer to *Section 5.3.16* for more details on the input/output alternate function characteristics.

The following table summarizes the parameters measured in SDR mode.

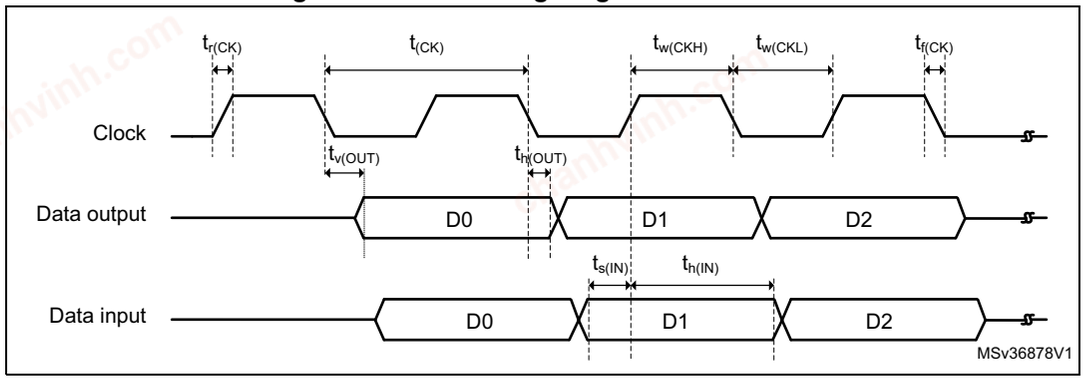
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Table 75. XSPI characteristics in SDR mode(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CLK}	XSPI clock frequency	1.65 V < V_{DD} < 1.98 V Voltage scaling VOS0 C_L = 15 pF	-	-	185	MHz
		2.7 V < V_{DD} < 3.6 V Voltage scaling VOS0 C_L = 15 pF	-	-	140	
$t_{w(CLKH)}$	XSPI clock high and low time Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$ / 2 + 1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$ / 2 - 1	-	$t_{(CLK)}$ / 2	
$t_{w(CLKH)}$	XSPI clock high and low time Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n / 2) × $t_{(CLK)}$ / (n + 1)	-	(n / 2) × $t_{(CLK)}$ / (n + 1) + 1	
$t_{w(CLKL)}$			(n / 2 + 1)*$t_{(CLK)}$/ (n + 1) - 1	-	(n / 2 + 1)*$t_{(CLK)}$/ (n + 1)	
$t_{s(DQ)}$	Data input setup time	-	1.5	-	-	
$t_{h(DQ)}$	Data input hold time	-	2	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0	0.5	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

1. Evaluated by characterization. Not tested in production.
2. Voltage scaling = VOS low.

Figure 34. XSPI timing diagram - SDR mode



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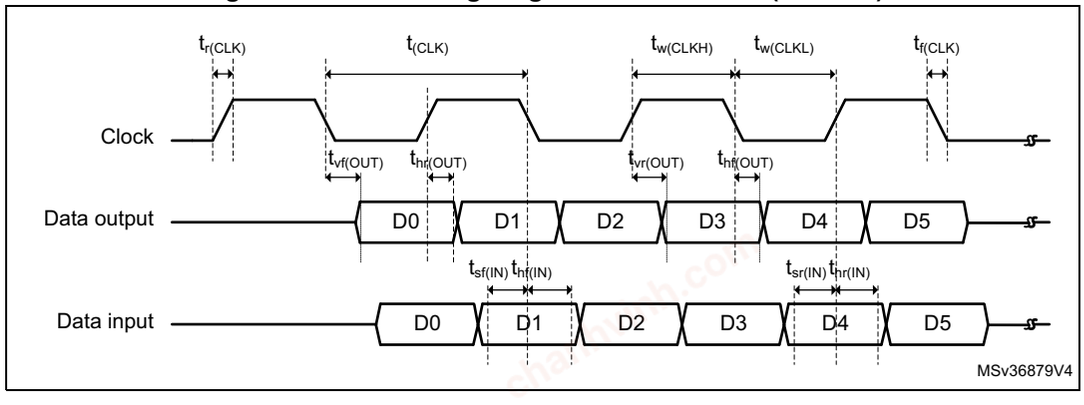
The following table summarizes the parameters measured in DTR mode (no DQS).

Table 76. XSPI characteristics in DTR mode without DQS(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	XSPI clock frequency	1.65 V < V_{DD} < 1.98 V Voltage scaling VOS0 C_L = 15 pF	-	-	180	MHz
		2.7 V < V_{DD} < 3.6 V Voltage scaling VOS0 C_L = 15 pF	-	-	140	
$t_{w(CLKH)}$	XSPI clock high and low time Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$ / 2 + 1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$ / 2 - 1	-	$t_{(CLK)}$ / 2	
$t_{w(CLKH)}$	XSPI clock high and low time Odd division	PRESCALER[:0] = n = 2,4,6,8	(n / 2) × $t_{(CLK)}$ / (n + 1)	-	-	
$t_{w(CLKL)}$			(n / 2 + 1) × $t_{(CLK)}$ / (n + 1) - 1	-	(n / 2 + 1) × $t_{(CLK)}$ / (n + 1)	
$t_{sr(DQ),tsf(DQ)}$	Data input setup time	-	2	-	-	ns
$t_{hr(DQ),thf(DQ)}$	Data input hold time	-	1	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	-	-	$t_{(CLK)}$ / 4 + 0.56(3)	$t_{(CLK)}$ / 4 + 1 6.5(3)	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	-	$t_{(CLK)}$ / 4 - 0.5 4.5(3)	-	-	

1. Evaluated by characterization. Not tested in production.
2. Voltage scaling = VOS low.
3. When Prescaler = 0 and $F_{(CLK)}$ < 40 MHz.

Figure 35. XSPI timing diagram – DTR mode (no DQS)



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The following table summarizes the parameters measured in DTR mode (with DQS).

Table 77. XSPI characteristics in DTR mode (with DQS or HyperBus)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	XSPI clock frequency	1.65 V < V_{DD} < 3.6 V Voltage scaling VOS0 C_L = 15 pF	-	-	200	MHz
$t_{w(CLKH)}$	XSPI clock high and low time Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$ / 2 + 1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$ / 2 - 1	-	$t_{(CLK)}$ / 2	
$t_{w(CLKH)}$	XSPI clock high and low time Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n / 2) × $t_{(CLK)}$ / (n + 1)	-	(n / 2) × $t_{(CLK)}$ / (n + 1) + 1	
$t_{w(CLKL)}$			(n / 2 + 1) × $t_{(CLK)}$ / (n + 1) - 1	-	(n / 2 + 1) × $t_{(CLK)}$ / (n + 1)	
$t_{w(CS)}$	Chip select high time	-	3 × $t_{(CLK)}$	-	-	
$t_{v(CK)}$	Clock valid time	-	-	-	$t_{(CLK)}$ + 1	
$t_{h(CK)}$	Clock hold time	-	$t_{(CLK)}$ / 2	-	-	
$V_{ODr(CK)}$	CLK, NCLK crossing level on CLK rising edge	V_{DD} = 1.8 V	1020	-	1138 / 1019(2)	mV
$V_{ODf(CK)}$	CLK, NCLK crossing level on CLK falling edge	V_{DD} = 1.8 V	908	-	1080	
$t_{sr(DQ)}$, $t_{sf(DQ)}$	Data input setup time	-	0.5 - $t_{(CLK)}$ / 4 3(3)	-	-	ns
$t_{hr(DQ)}$, $t_{hf(DQ)}$	Data input hold time	-	2 + $t_{(CLK)}$ / 4 7.5(3)	-	-	
$t_{v(DQ)}$	Data input valid time	-	0	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	3 × $t_{(CLK)}$	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	-	-	$t_{(CLK)}$/4 + 0.5 6(3)	$t_{(CLK)}$ / 4 + 1 6.5(3)	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	-	$t_{(CLK)}$ / 4 - 0.5 4.5(3)	-	-	

1. Evaluated by characterization. Not tested in production.
2. When using 33 Ω series termination on CLK and NCLK.
3. When Prescaler = 0 and $F_{(CLK)}$ < 40 MHz.

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Figure 36. XSPI HyperBus clock

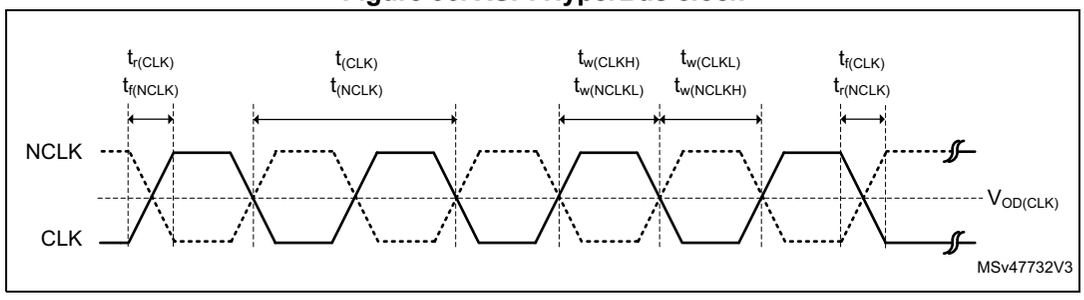


Figure 37. XSPI HyperBus read

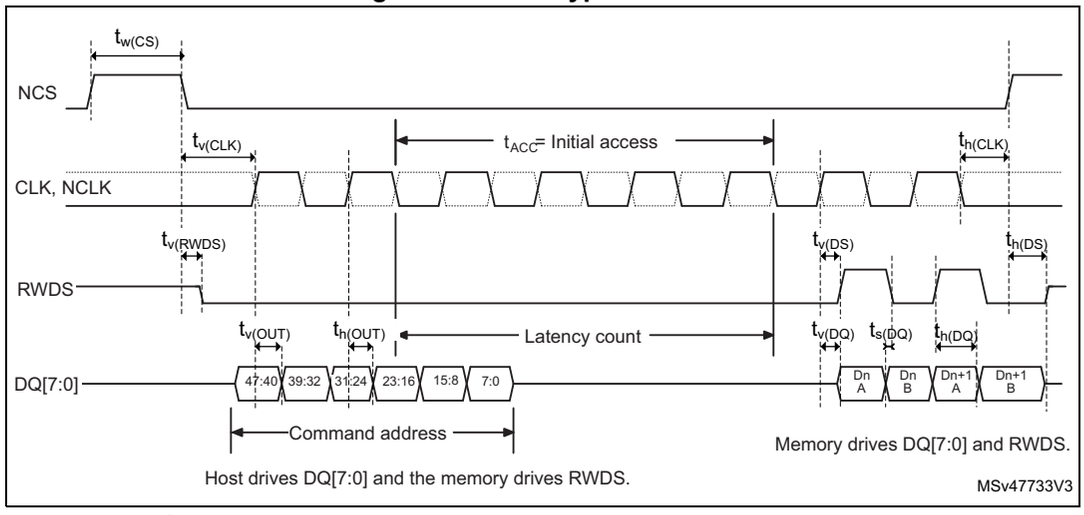
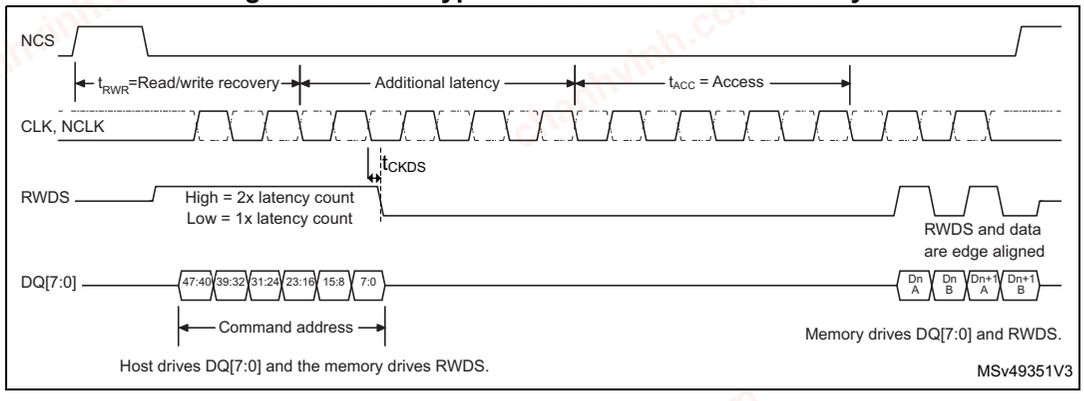
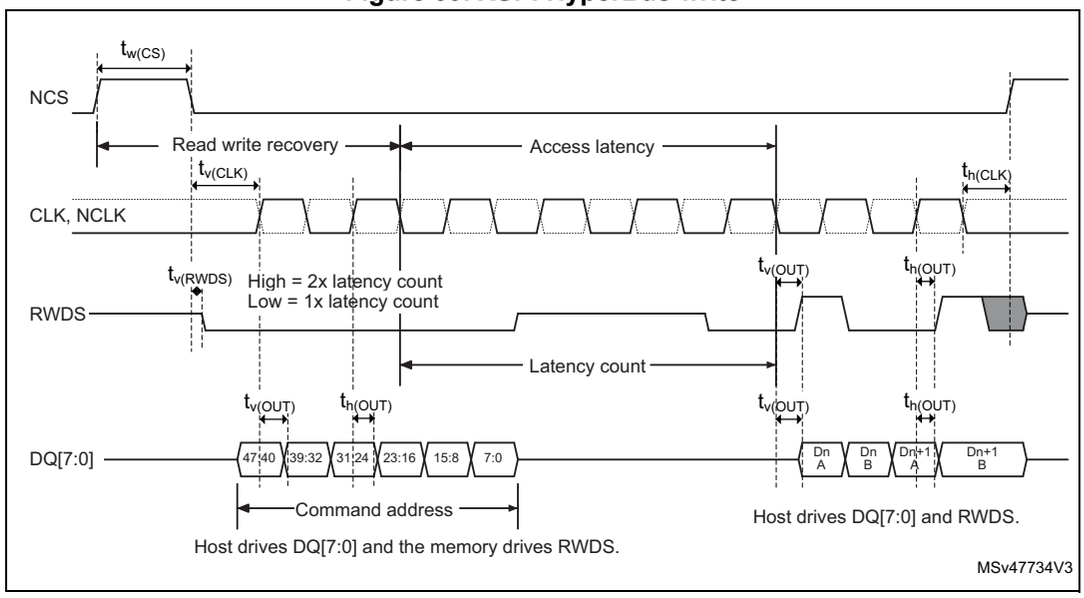


Figure 38. XSPI HyperBus read with double latency



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Figure 39. XSPI HyperBus write



5.3.20 SDMMC interface characteristics

Unless otherwise specified, the parameters given in *Table 79* to *Table 80* are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed set as shown in *Table 78*
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.5$ V

Refer to *Section 5.3.16* for more details on the input/output characteristics.

Table 78. Output speed settings versus voltage and clock frequency

Voltage range (V)	Max clock frequency (MHz)	OSPEEDRy[1:0]	
		Clock	Data
1.71 to 1.9 and 3.0 to 3.6	26/25	00	00
	52/50	01	00
	DDR 52/50	01	01
	100	01	00
3.0 to 3.6	145	11	10
1.71 to 1.9	200	11	10

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Table 79. Dynamic characteristics: SD, V_{DD} = 1.71 V to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	3.00 < V_{DD} < 3.6 V	-	-	145	MHz
		1.71 < V_{DD} < 1.9 V	-	-	200	
	SDIO_CK / f_{PCLK2} frequency ratio	1.71 < V_{DD} < 3.6 V	-	-	8 / 3	
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in SD HS/SDR(3)/DDR(3) mode						
t_{ISU}	Input setup time HS	-	3	-	-	ns
t_{IHD}	Input hold time HS	-	1.5	-	-	
T_{idw}(4)	Input valid window (variable window)	-	2.5	-	-	
CMD, D outputs (referenced to CK) in SD HS/SDR(3)/DDR(3) mode						
t_{OV}	Output valid time HS	-	-	6.5	6.5	ns
t_{OH}	Output hold time HS	-	4.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	2.5	-	-	ns
t_{IHD}	Input hold time SD	-	1.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	0.5	0.5	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. Evaluated by characterization. Not tested in production.
2. Above 100 MHz, C_L applied is 20 pF.
3. For SD 1.8 V support, an external voltage converter is needed.
4. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 80. Dynamic characteristics: eMMC, V_{DD} = 1.71 V to 3.6 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	3.00 < V_{DD} < 3.6 V	-	-	145	MHz
		1.71 < V_{DD} < 1.9 V	-	-	200	
	SDIO_CK / f_{PCLK2} frequency ratio	-	-	-	8 / 3	
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IH}	Input hold time HS	-	1.5	-	-	
T_{idw}(3)	Input valid window (variable window)	-	2.5	-	-	

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Table 80. Dynamic characteristics: eMMC, V_{DD} = 1.71 V to 3.6 V(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	-	-	6	6	ns
t_{OH}	Output hold time HS	-	4.5	-	-	

1. Evaluated by characterization. Not tested in production.
2. C_{load} = 20 pF
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Figure 40. SDIO high-speed mode

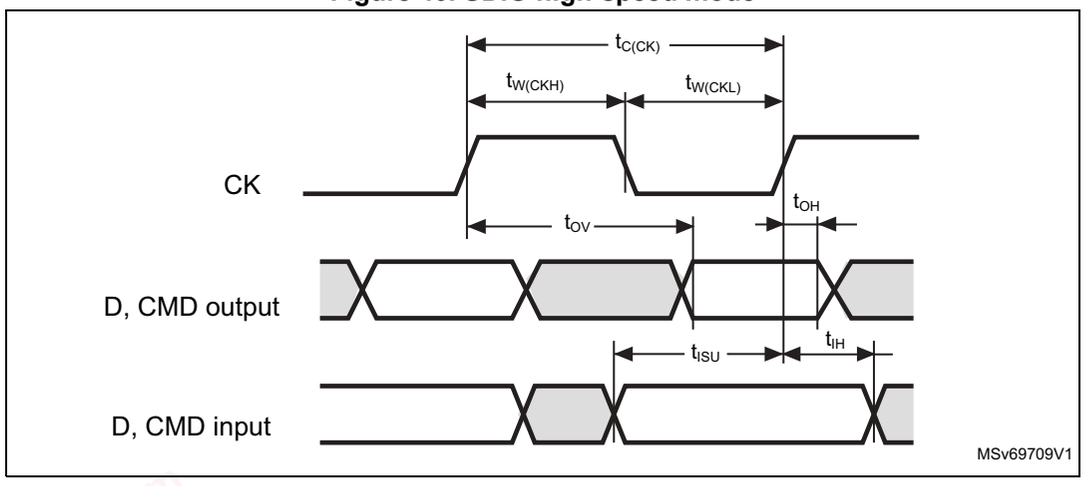


Figure 41. SD default mode

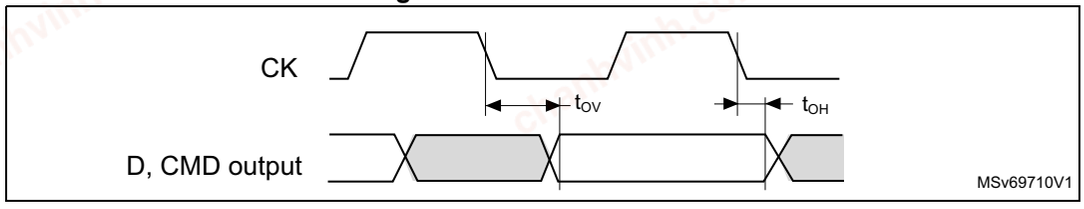
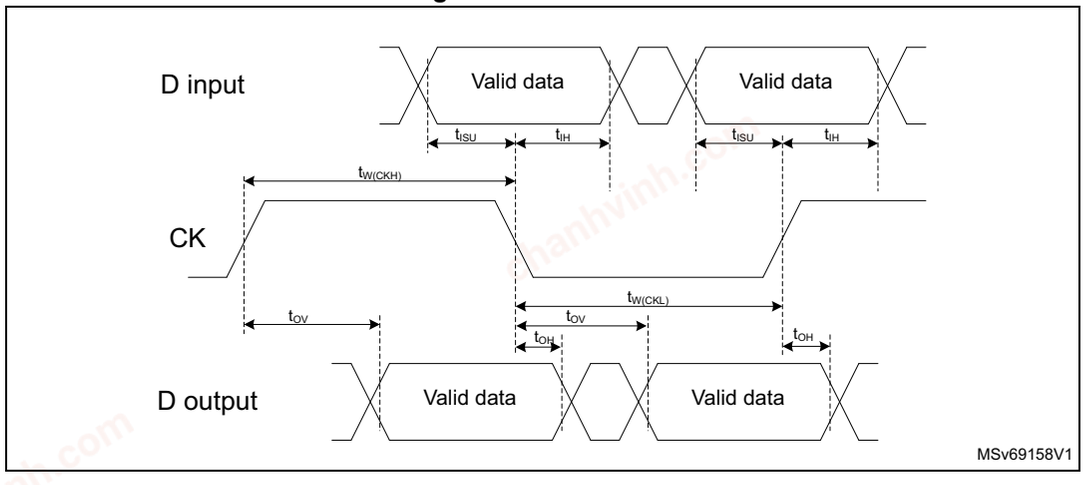


Figure 42. DDR mode



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5.3.21 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 81* are derived from tests performed under the ambient temperature, f_{HCLKx} frequency, and V_{DD} supply voltage summarized in *Table 22*.

Table 81. Delay block dynamic characteristics

Symbol	Parameter		Min	Typ	Max	Unit
t_{init}	Initial delay		150	250	350	ps
t_{Δ}	Unit delay	Bypass mode	30	40	50	
		Lock mode	$T^{(1)}$ / 32 - 10%	$T^{(1)}$ / 32	$T^{(1)}$ / 32 + 1%	

1. Period of the DLL clock.

5.3.22 12-bit ADC characteristics

Table 82. ADC characteristics(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	Clock frequency	-	0.7	-	70	MHz
f_s	Sampling rate	Resolution = 12 bits	0.0467	-	4.666	Msps
		Resolution = 10 bits	0.0538	-	5.384	
		Resolution = 8 bits	0.07	-	7	
		Resolution = 6 bits	0.0875	-	8.75	
t_C	Conversion cycle	Resolution = 12 bits	-	13.5	-	$1/f_{ADC}$
		Resolution = 10 bits	-	12	-	
		Resolution = 8 bits	-	10	-	
		Resolution = 6 bits	-	8	-	
f_{TRIG}	External trigger frequency	f_{ADC} = 70 MHz	-	-	TBD	MHz
		Resolution = 12 bits	-	-	TBD	$1 / f_{ADC}$
V_{AIN}	Conversion voltage range	Single ended	0	-	V_{REF+}	V
		Differential	$-V_{REF+}$	-	V_{REF+}	
V_{CMIV}	Common mode input voltage	Differential	-	V_{REF+} / 2	-	V
C_{ADC}	Internal sample and hold capacitor	-	-	2.56	-	pF
t_{STAB}	Start-up time	-	-	5	-	µs
t_{OFF_CAL}	Offset calibration time	-	-	TBD	-	$1 / f_{ADC}$
t_{LATR}	Trigger conversion latency regular and injected channels without conversion abort	CKMODE = 0	-	TBD	-	
		CKMODE = 1	-	TBD	-	
$t_{LATRINJ}$	Trigger conversion latency regular injected channels aborting a regular conversion	CKMODE = 0	-	TBD	-	
		CKMODE = 1	-	TBD	-	

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Table 82. ADC characteristics(1)(2)(3) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	-	2.5	-	1502	1 / f_{ADC}
$I_{ADC(VDDA18ADC)}$	ADC supply current on $V_{DDA18ADC}$	f_s = 5 Msps, resolution = 12 bits	-	315	-	µA
		f_s = 5.8 Msps, resolution = 10 bits	-	330	-	
		Power down, ADEN = 0	-	1.71	-	
		Deep power down, ADEN = 0, DEEPPWD = 1	-	1.53	-	

1. Evaluated by characterization and not tested in production, unless otherwise specified.
2. All analog inputs must be between V_{SSA} and $V_{DDA18ADC}$.
3. TBD stands for “to be defined”.

Table 83. ADC accuracy(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	-	3.52	-	LSB
		Differential	-	2.98	-	
ED	Differential linearity error (DNL)	Single ended	-	0.60	0.97	
		Differential	-	0.80	0.98	
EL	Integral linearity error (INL)	Single ended	-	2.60	3.60	
		Differential	-	2.10	3.80	
ENOB	Effective number of bits	Single ended	-	9.9	-	Bits
		Differential	-	10.5	-	
SINAD	Signal-to-noise and distortion ratio(3)	Single ended	-	62	-	dB
		Differential	-	65	-	
SNR	Signal-to-noise ratio	Single ended	-	62	-	
		Differential	-	65	-	
THD	Total harmonic distortion	Single ended	-	-76	-	
		Differential	-	-77	-	
EG	Gain error	Vs. V_{REF+} value	-1	-	1	% of full scale
EO	Offset error	Without calibration	-1	-	1	
		After calibration	TBD	-	TBD	LSB

1. Evaluated by characterization and not tested in production, unless otherwise specified.
2. TBD stands for “to be defined”.
3. Value measured with a -0.5 dBFS input signal and then extrapolated to full scale.

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Figure 43. ADC accuracy characteristics

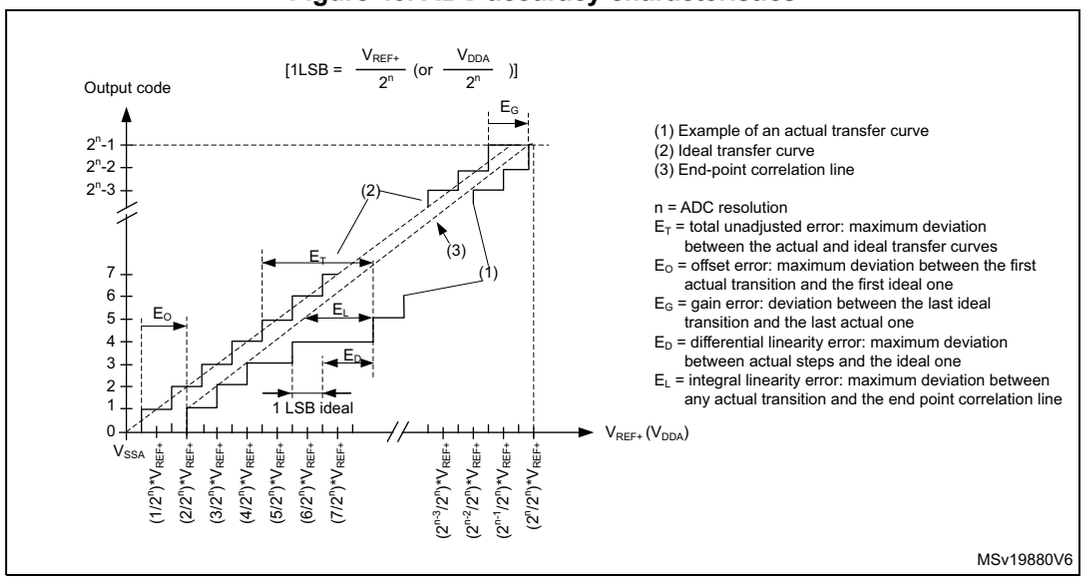
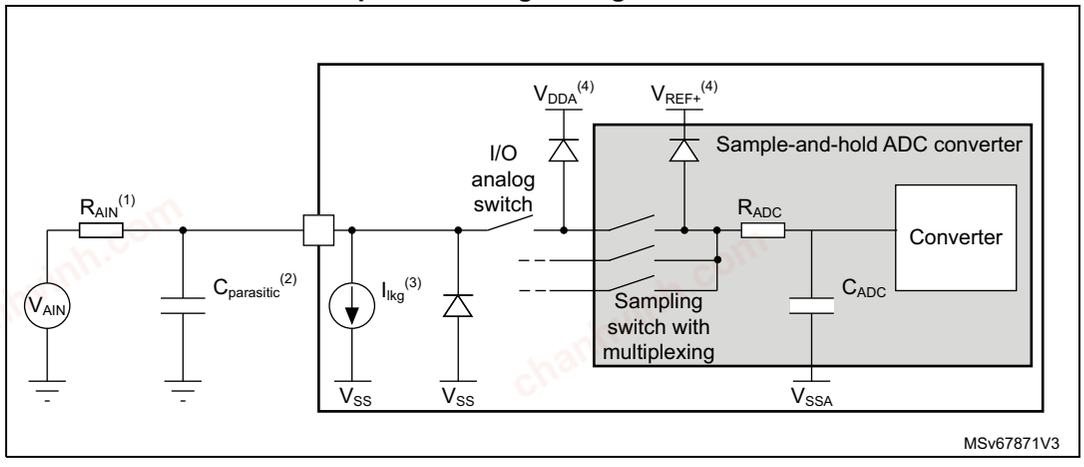


Figure 44. Typical connection diagram using the ADC with TT pins featuring analog switch function



1. Refer to *Table 82* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering R_{ADC}, and PCB layout quality) plus the pad capacitance (refer to *Table 53*). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 53* for the value of I_{lkg}.
4. Refer to *Figure 15* .

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Table 84. Minimum sampling time versus R_{AIN}(1)(2)

Symbol	Parameter	Conditions (R_{AIN} in ohms)		Min	Typ	Max	Unit
t_{s_min}	Minimum sampling time	12 bits	47	32	-	-	ns
			68	33	-	-	
			100	34	-	-	
			150	36	-	-	
			220	38	-	-	
			330	42	-	-	
			470	47	-	-	
			680	55	-	-	
			1000(3)	70	-	-	
t_{s_min}	Minimum sampling time	10 bits	47	23	-	-	ns
			68	24	-	-	
			100	25	-	-	
			150	26	-	-	
			220	28	-	-	
			330	30	-	-	
			470	33	-	-	
			680	38	-	-	
			1000	45	-	-	
			1500	55	-	-	
			2200	71	-	-	
			3300	97	-	-	
			4700(3)	133	-	-	

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Table 84. Minimum sampling time versus R_{AIN}[(1)(2)] (continued)

Symbol	Parameter	Conditions (Resolution / R_{AIN} in ohms)		Min	Typ	Max	Unit
t_{s_min}	Minimum sampling time	8 bits	47	17	-	-	ns
			68	17	-	-	
			100	18	-	-	
			150	19	-	-	
			220	20	-	-	
			330	22	-	-	
			470	25	-	-	
			680	28	-	-	
			1000	34	-	-	
			1500	42	-	-	
			2200	53	-	-	
			3300	70	-	-	
			4700	94	-	-	
			6800	128	-	-	
			10000	183	-	-	
			15000	277	-	-	
			22000[(3)]	435	-	-	
t_{s_min}	Minimum sampling time	6 bits	47	TBD	-	-	ns
			68	TBD	-	-	
			100	TBD	-	-	
			150	TBD	-	-	
			220	TBD	-	-	
			330	TBD	-	-	
			470	TBD	-	-	
			680	TBD	-	-	
			1000	TBD	-	-	
			1500	TBD	-	-	
			2200	TBD	-	-	
			3300	TBD	-	-	
			4700	TBD	-	-	
			6800	TBD	-	-	
			10000	TBD	-	-	
			15000	TBD	-	-	
			22000[(3)]	TBD	-	-	

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1. TBD stands for “to be defined”.
2. Specified by design. Not tested in production.
3. Maximum external input impedance value authorized for the given resolution.

5.3.23 Voltage reference buffer (VREFBUF) characteristics

Table 85. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DDA18ADC}$	Analog supply voltage	-	VRS = 000	1.62	1.8	1.98(2)	V
			VRS = 001	1.75	1.8	1.98(2)	
V_{REFBUF_OUT}	Voltage reference buffer output	I_{LOAD} = 10 µA, $V_{DDA18ADC}$ = 1.8 V, 30 °C	VRS = 000	1.209	1.210	1.211	
			VRS = 001	1.499	1.5	1.502	
TRIM	Trim step resolution	-		-	±0.05	±0.1	%
C_L	Load capacitor	-		0.5	1.1	1.5	µF
esr	Equivalent serial resistor of C_L	-		-	-	1	W
I_{LOAD}	External DC load current	ADC ON		-	-	0.8	mA
		ADC OFF		-	-	2	
I_{LINE_REG}	Line regulation	1.62 V ≤ $V_{DDA18ADC}$ ≤ 1.98 V, T_J = +30 °C		-	6463	10559	ppm / V
I_{LOAD_REG}	Load regulation	100 µA ≤ I_{LOAD} ≤ 800 µA, T_J = +30 °C		-	6276	6974	ppm / mA
T_{coeff}	Temperature coefficient	-40 °C < T_J < +25 °C		43	-	98	ppm / °C
		25 °C < T_J < +125 °C		64	-	139	
PSRR	Power supply rejection	DC		48	76	-	dB
		100 KHz		51	60	-	
t_{START}	Start-up time	-		-	300	800	µs
I_{INRUSH}	Control of max DC current drive on V_{REFBUF_OUT} during start-up phase			-	-	10	mA
$I_{VDDA18ADC(VREFBUF)}$	VREFBUF supply current $V_{DDA18ADC}$ (excluding internal and external load)	ENVR = 1	I_{LOAD} = 0.8 mA DC	-	9	17	µA
			Peak during 2× ADC conversions	-	48	60	
		ENVR = 0		-	5	26	µA

1. Evaluated by characterization and not tested in production, unless otherwise specified.
2. Static condition 1.98 V allowed during transients.

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5.3.24 Digital temperature sensor (DTS) characteristics

Table 86. DTS characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}	Operating frequency	-	4	-	8	MHz
Res	Resolution	-	8	10	12	Bits
Step	Step size	-	0.86	0.22	0.06	°C
t_{conv}	Conversion time	-	512	2048	8192	1 / f_{DTS}
t_{pwrup}	Power up time	-	-	-	256	
T_A	Accuracy	T_A = -20 °C to +130 °C	-	-	3	°C
		T_A = -40 °C to -20 °C	-	-	6	
G	G constant	Refer to reference manual for the formula	59.7			°C
H	H constant		204.4			°C
J	J constant		-0.16			°C / MHz
Cal5	Cal5 constant		4094			-
$I_{DTS(VDDA18AON)}$	DTS supply current on $V_{DDA18AON}$	f_{DTS} = 8 MHz, continuous measurements, single sensor	-	120	160	µA
		1 measurement/s	-	-	1	
		f_{DTS} clock stopped	-	-	1	
$I_{DTS(VDDCORE)}$	DTS supply current on V_{DDCORE}	f_{DTS} = 8 MHz	-	-	15	µA

5.3.25 V_{BAT}, V_{DDx}, V_{DDCORE}, $V_{DDA18AON}$, ADC measurement characteristics

Table 87. V_{BAT}, V_{DDx}, V_{DDCORE}, $V_{DDA18AON}$, ADC measurement characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-		130	-	kΩ
Q	Ratio on V_{BAT} measurement	-		4	-	-
E_r	Error on Q	-	TBD	-	TBD	%
t_{S_VBAT}	ADC sampling time when reading the V_{BAT}	-	TBD	-	-	µs
t_{S_VDD}	ADC sampling time when reading the V_{DD}	-	TBD	-	-	
$t_{S_VDDA18AON}$	ADC sampling time when reading the $V_{DDA18AON}$	-	TBD	-	-	
$t_{S_VDDCORE}$	ADC sampling time when reading the V_{DDCORE}	-	TBD	-	-	

1. Evaluated by characterization and not tested in production, unless otherwise specified.
2. TBD stands for “to be defined”.

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5.3.26 Temperature and V_{BAT} monitoring characteristics for tamper detection

Table 88. Temperature and V_{BAT} monitoring characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{EMPH}	High T_J temperature monitoring	-	110	-	125	°C
T_{EMPL}	Low T_j temperature monitoring	-	-40	-	-30	
V_{08CAPH}	High V_{08CAP}(2) supply monitoring	-	0.88	-	1	V
V_{08CAPL}	Low V_{08CAP}(2) supply monitoring	-	0.6	-	0.72	
V_{08CAP_filter}	V_{08CAP}(2) supply monitoring glitch filter	-	-	-	1	µs

1. Evaluated by characterization and not tested in production, unless otherwise specified.
2. V_{08CAP} is an internal regulator supplied by V_{SW}. V_{SW} is equal to V_{DD} when present. It is equals to V_{BAT} otherwise.

5.3.27 Compensation cell characteristics

Table 89. Compensation cell characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{COMPCELL}$	$V_{DDA18AON}$ current consumption during code calculation	Using a 8 MHz clock (HSI / 8)	-	250	-	µA
T_{ready}	Time needed to have the first code calculation after enabling		-	96	-	µs
$T_{measure}$	Time needed to update the code		-	832	-	

1. Evaluated by characterization and not tested in production, unless otherwise specified.

5.3.28 Multifunction digital filter (MDF) characteristics

Unless otherwise specified, the parameters given in *Table 90* for MDF are derived from tests performed under the ambient temperature, f_{AHB} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scale is set to VOS0

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Refer to *Section 5.3.16* for more details on the input/output alternate function characteristics.

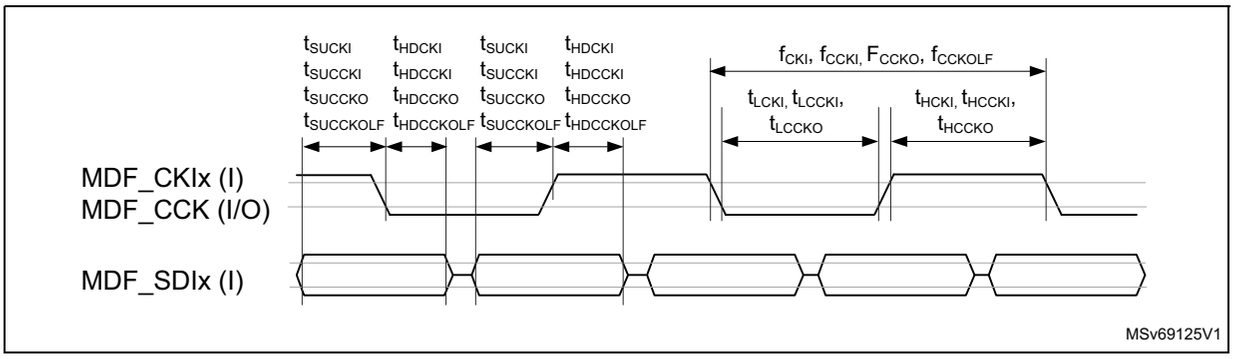
Table 90. MDF characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CKI}	Input clock frequency via MDF_CKIx pin, in target SPI mode	1.65 < V_{DD} < 3.6 V	-	-	25	MHz
f_{CCKI}	Input clock frequency via MDF_CCK[1:0] pin, in target SPI mode		-	-	25	
f_{CCKO}	Output clock frequency in controller SPI mode		-	-	25	
f_{CCKOLF}	Output clock frequency in LF_MASTER SPI mode		-	-	5	
f_{SYMB}	Input symbol rate in Manchester mode		-	-	20	
t_{HCKI}, t_{LCKI}	MDF_CKIx input clock high and low time	In target SPI mode	2 × $T_{mdf_proc_ck}$(2)	-	-	ns
t_{HCCKI}, t_{LCCKI}	MDF_CCK[1:0] input clock high and low time	In target SPI mode	2 × $T_{mdf_proc_c}$	-	-	
t_{HCCKO}, t_{LCCKO}	MDF_CCK[1:0] output clock high and low time	In controller SPI mode	2 × $T_{mdf_proc_ck}$	-	-	
$t_{HCCKOLF}$, $t_{LCCKOLF}$	MDF_CCK[1:0] output clock high and low time	In LF_MASTER SPI mode	$T_{mdf_proc_ck}$	-	-	
t_{SUCKI}	Data setup time w.r.t. MDF_CKIx input	In target SPI mode, measured on rising and falling edge	2.5	-	-	
t_{HDCKI}	Data hold time w.r.t. MDF_CKIx input		0	-	-	
t_{SUCCKI}	Data setup time w.r.t. MDF_CCK[1:0] input	In target SPI mode: MDF_CCK[1:0] configured in input, measured on rising and falling edge	3	-	-	
t_{HDCCKI}	Data hold time w.r.t. MDF_CCK[1:0] input		0	-	-	
t_{SUCCKO}	Data setup time w.r.t. MDF_CCK[1:0] output	In controller SPI mode: MDF_CCK[1:0] configured in output, measured on rising and falling edge	3	-	-	ns
t_{HDCCKO}	Data hold time w.r.t. MDF_CCK[1:0] output		0	-	-	
$t_{SUCCKOLF}$	Data setup time w.r.t. MDF_CCK[1:0] output	In LF_MASTER SPI mode, MDF_CCK[1:0] configured in output, measured on rising and falling edge	14	-	-	
$t_{HDCCKOLF}$	Data hold time w.r.t. MDF_CCK[1:0] output		0	-	-	

1. Evaluated by characterization. Not tested in production.
2. $T_{mdf_proc_ck}$ is the period of the MDF processing clock.

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Figure 45. MDF timing diagram



5.3.29 Audio digital filter (ADF) characteristics

Unless otherwise specified, the parameters given in *Table 91* are derived from tests performed under the ambient temperature, f_{AHB} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scale is set to VOS0

Refer to *Section 5.3.16* for more details on the input/output alternate function characteristics.

Table 91. ADF characteristics(1)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
F_{CCKI}	Input clock frequency via ADF_CCK[1:0] pin, in target SPI mode	1.65 < V_{DD} < 3.6 V	-	-	25	MHz
F_{CCKO}	Output clock frequency in controller SPI mode	1.65 < V_{DD} < 3.6 V	-	-	25	
F_{CCKOLF}	Output clock frequency in LF_MASTER SPI mode	1.65 < V_{DD} < 3.6 V	-	-	5	
F_{SYMB}	Input symbol rate in Manchester mode	1.65 < V_{DD} < 3.6 V	-	-	20	
T_{HCCKI}, T_{LCCKI}	ADF_CCK[1:0] input clock high and low time	In target SPI mode	2 × $T_{adf_proc_ck}$	-	-	ns
T_{HCCKO}, T_{LCCKO}	ADF_CCK[1:0] output clock high and low time	In controller SPI mode	2 × $T_{adf_proc_ck}$	-	-	
$T_{HCCKOLF}$, $T_{LCCKOLF}$	ADF_CCK[1:0] output clock high and low time	In LF_MASTER SPI mode	$T_{adf_proc_ck}$	-	-	

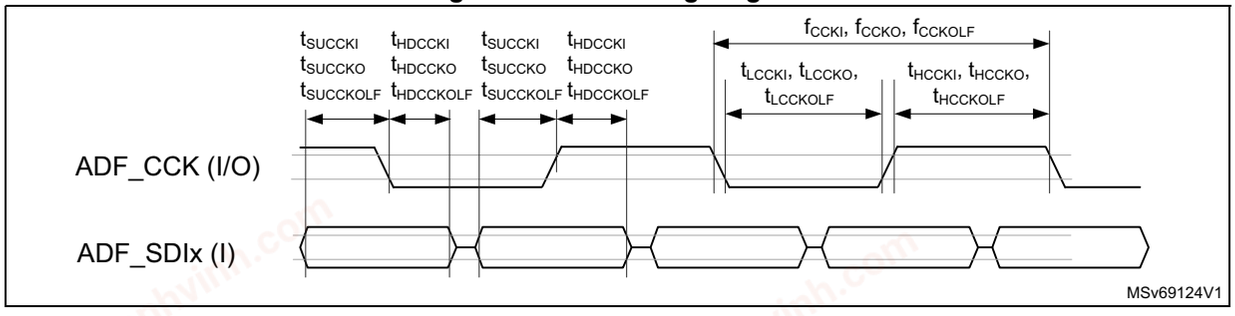
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Table 91. ADF characteristics(1) (continued)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
T_{SUCCKI}	Data setup time w.r.t. ADF_CCK[1:0] input	In target SPI mode: ADF_CCK[1:0] configured in input, measured on rising and falling edge	3	-	-	ns
T_{HDCCKI}	Data hold time w.r.t. ADF_CCK[1:0] input		0.5	-	-	
T_{SUCCKO}	Data setup time w.r.t. ADF_CCK[1:0] output	In controller SPImode: ADF_CCK[1:0] configured in output, measured on rising and falling edge	3	-	-	
T_{HDCCKO}	Data hold time w.r.t. ADF_CCK[1:0] output		0.5	-	-	
$T_{SUCCKOLF}$	Data setup time w.r.t. ADF_CCK[1:0] output	In LF_MASTER SPI mode: ADF_CCK[1:0] configured in output, measured on rising and falling edge	14	-	-	
$T_{HDCCKOLF}$	Data hold time w.r.t. ADF_CCK[1:0] output		0.5	-	-	

1. Evaluated by characterization. Not tested in production.

Figure 46. ADF timing diagram



5.3.30 Camera interface (DCMI) characteristics

Unless otherwise specified, the parameters given in *Table 92* are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage summarized in *Table 22*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scaling range 1

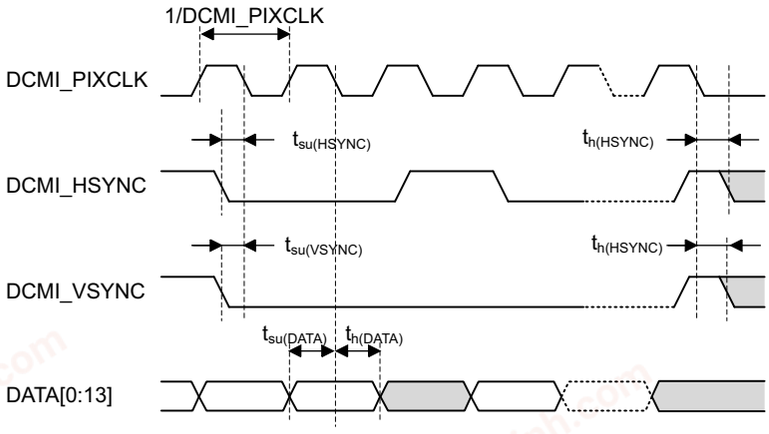
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Table 92. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	100	MHz
D_{PIXEL}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	3.5	-	ns
$t_{h(DATA)}$	Data hold time	0.5	-	
$t_{su(HSYNC)}t_{su(VSYNC)}$	DCMI_HSYNC and DCMI_VSYNC input setup times	3.5	-	
$t_{h(HSYNC)}t_{h(VSYNC)}$	DCMI_HSYNC and DCMI_VSYNC input hold times	1	-	

1. Evaluated by characterization. Not tested in production.

Figure 47. DCMI timing diagram



5.3.31 Camera interface pixel pipeline (DCMIPP) characteristics

Unless otherwise specified, the parameters given in *Table 93* are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage summarized in *Table 22*, with the following configuration:

- DCMIPP_PIXCLK polarity: falling
- DCMIPP_VSYNC and DCMIPP_HSYNC polarity: high
- Data formats: 16 bits
- Capacitive load C = 30 pF
- HSLV deactivated
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Table 93. DCMIPP characteristics(1)

Symbol	Parameter	Min	Max	Unit
DCMIPP_PIXCLK	Pixel clock input	-	120	MHz
D_{pixel}	Pixel clock input duty cycle	30	70	%

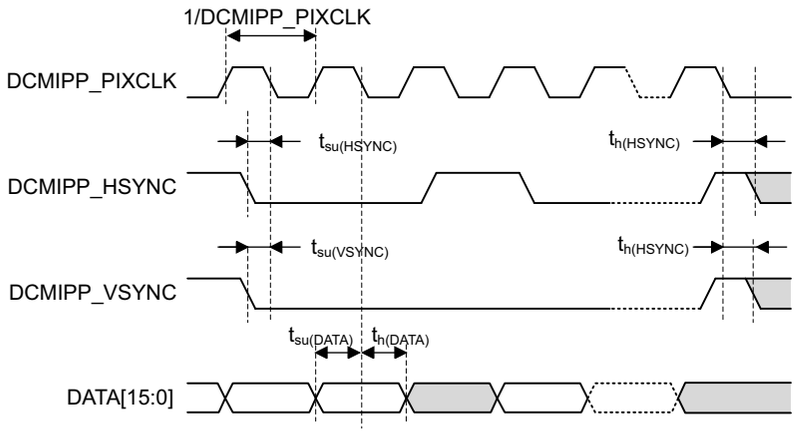
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Table 93. DCMIPP characteristics(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(DATA)}$	Data input setup time	2	-	ns
$t_{h(DATA)}$	Data hold time	3	-	
$t_{su(HSYNC)}$, $t_{su(VSYNC)}$	DCMI_HSYNC/ DCMI_VSYNC input setup time	2	-	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$	DCMI_HSYNC/ DCMI_VSYNC input hold time	3	-	

1. Evaluated by characterization. Not tested in production.

Figure 48. DCMIPP timing diagram



5.3.32 Parallel interface (PSSI) characteristics

Unless otherwise specified, the parameters given in *Table 94* and *Table 95* are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage summarized in *Table 22*, with the following configuration:

- PSSI_PDCK polarity: falling
- PSSI_RDY and PSSI_DE polarity: low
- Bus width: 16 lines
- Data width: 32 bits
- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scaling range 1

Table 94. PSSI transmit characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
-	Frequency ratio DCMI_PDCK/fHCLK	-	-	0.4	-
PSSI_PDCK	PSSI clock input	1.65 V ≤ V_{DD} ≤ 3.6 V	-	100(2)	MHz

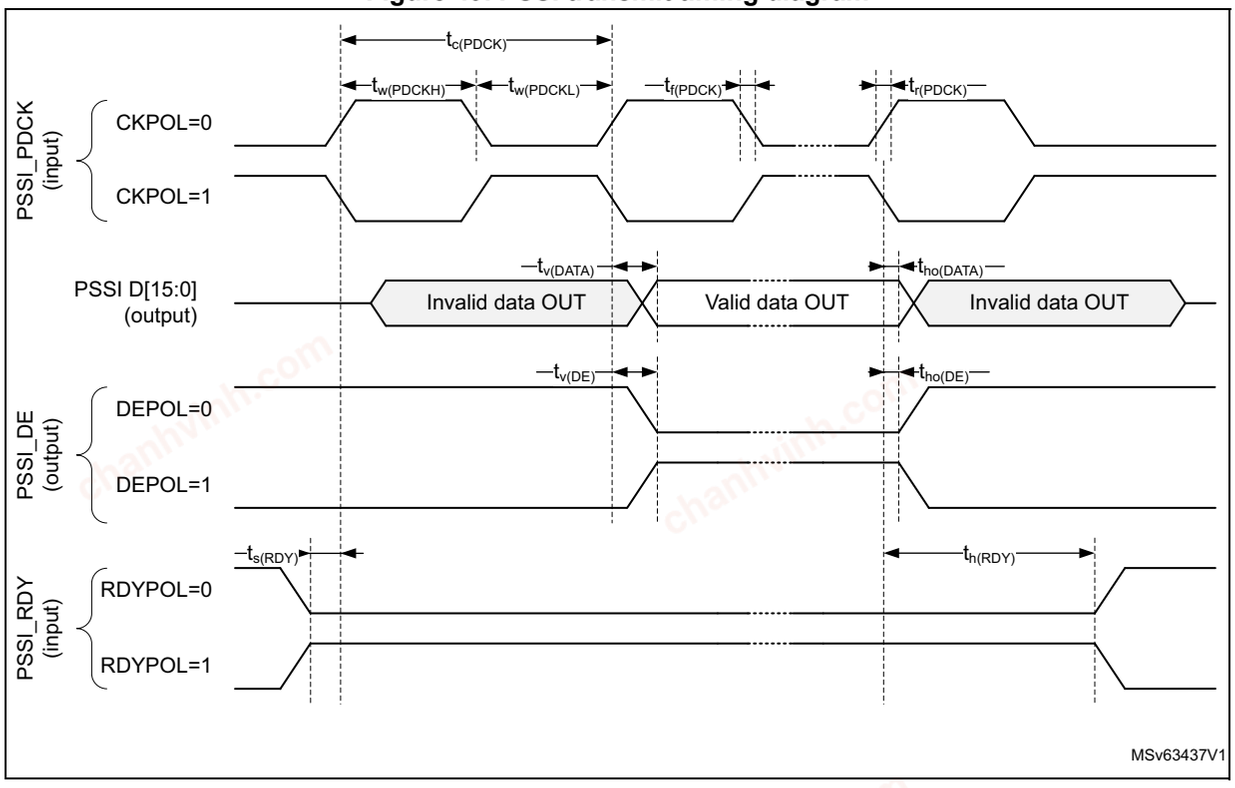
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Table 94. PSSI transmit characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
D_{PIXEL}	PSSI clock input duty cycle	-	30	70	%
$t_{SU(DATA)}$	Data output valid time	1.65 V ≤ V_{DD} ≤ 3.6 V	-	8	ns
$t_{H(DATA)}$	Data output hold time	1.65 V ≤ V_{DD} ≤ 3.6 V	5	-	
$t_{SU(DE)}$	DE output valid time		-	8	
$t_{H(DE)}$	DE output hold time		5	-	
$t_{OV(RDY)}$	RDY input setup time		0	-	
$t_{OH(RDY)}$	RDY input hold time		0	-	

1. Evaluated by characterization. Not tested in production.
2. This maximal frequency does not consider receiver setup and hold timings.

Figure 49. PSSI transmit timing diagram



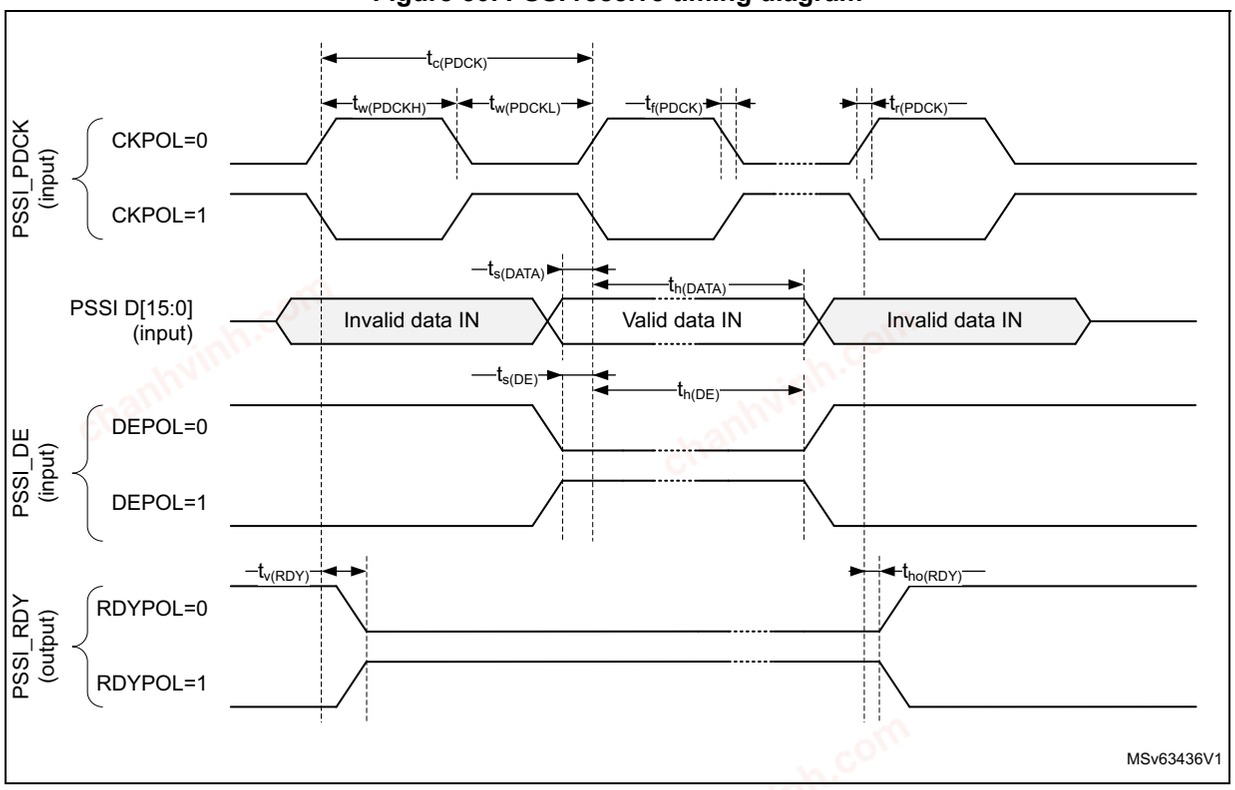
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Table 95. PSSI receive characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
-	Frequency ratio DCMI_PDCK/f_{HCLK}	-	-	0.4	-
PSSI_PDCK	PSSI clock input	1.65 V ≤ V_{DD} ≤ 3.6 V	-	100	MHz
D_{PIXEL}	PSSI clock input duty cycle	-	30	70	%
$t_{SU(DATA)}$	Data input setup time	1.65 V ≤ V_{DD} ≤ 3.6 V	3.5	-	ns
$t_{H(DATA)}$	Data input setup time		0.5	-	
$t_{SU(DE)}$	DE input setup time		3	-	
$t_{H(DE)}$	DE input setup time		1	-	
$t_{OV(RDY)}$	RDY output setup time		-	7	
$t_{OH(RDY)}$	RDY output hold time		6	-	

1. Evaluated by characterization. Not tested in production.

Figure 50. PSSI receive timing diagram



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5.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 96* for TFT-LCD are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage summarized in *Table 22*, with the following configuration:

- LCD_CLK polarity: low
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5VDD
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.5$ V
- Output speed is set to OSPEEDRy[1:0] = 11

Table 96. LCD-TFT characteristics(1)

Symbol	Parameter		Min	Max	Unit
f_{CLK}	LTDC clock output frequency	1.65 V ≤ V_{DD} ≤ 3.6 V, 30 pF	-	88	MHz
D_{CLK}	LTDC clock output duty cycle		45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock high time, low time		$t_{w(CLK)}$ /2 - 0.5	$t_{w(CLK)}$ /2 + 0.5	ns
$t_{v(DATA)}$	Data output valid time		-	3.5	
$t_{h(DATA)}$	Data output hold time		1.5	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$,	HSYNC/VSYNC/DE output valid time		-	-	ns
				1.5	
$t_{h(HSYNC)}$,	HSYNC/VSYNC/DE output hold time		0.5	-	
$t_{h(VSYNC)}$,					
$t_{h(DE)}$					

1. Evaluated by characterization. Not tested in production.

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Figure 51. LCD-TFT horizontal timing diagram

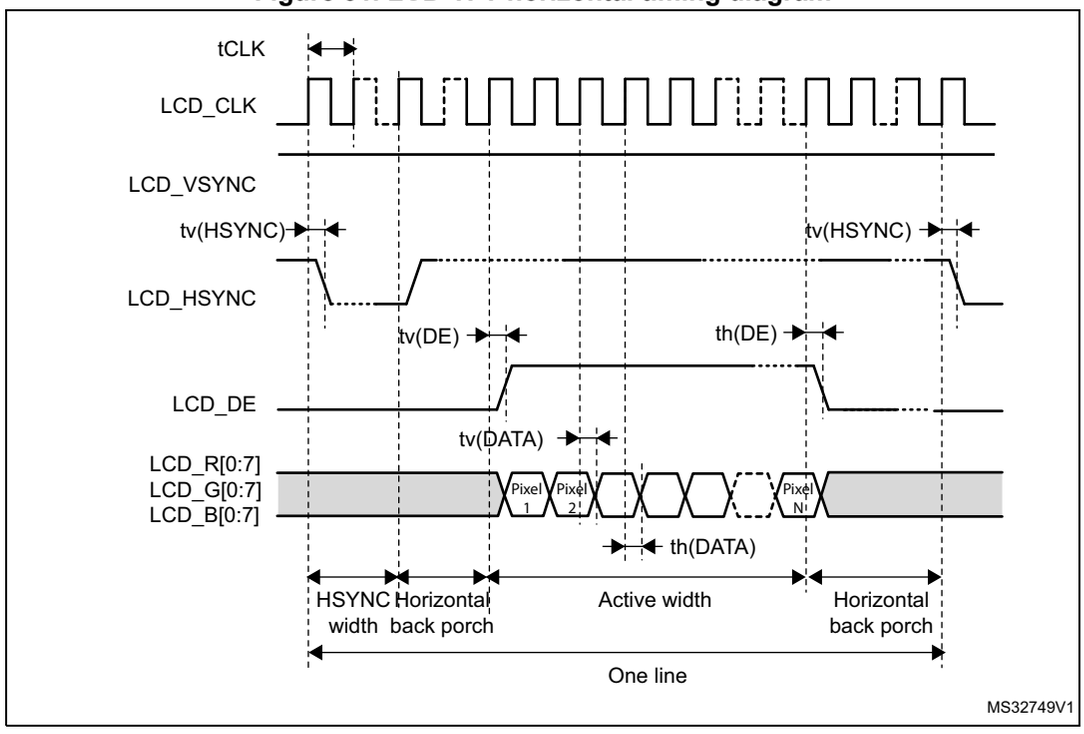
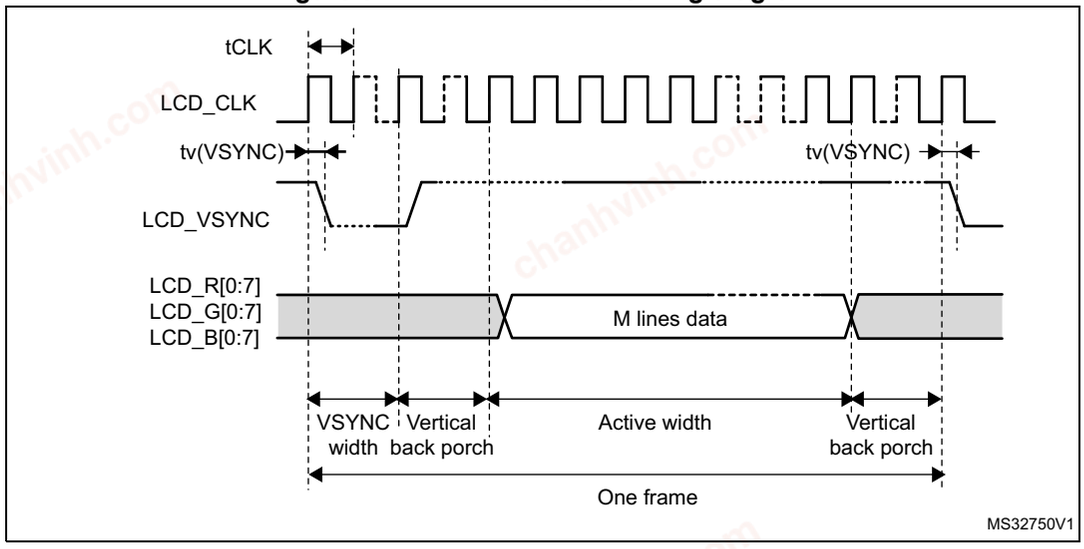


Figure 52. LCD-TFT vertical timing diagram



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5.3.34 Timer characteristics

The parameters given in *Table 97* and *Table 98* are specified by design, not tested in production.

Refer to *Table 5.3.16* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 97. TIMx characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{TIMxCLK}$	Timer kernel clock	0	200	MHz
f_{EXT}	Timer external clock frequency on CH1 to CH4	0	$f_{TIMxCLK}$ / 2	
Res_{TIM}	Timer resolution	-	16	bit
	Timer resolution (TIM2 to TIM5)	-	32	
t_{MAX_COUNT}	Maximum possible count with 16bit counters	-	65536	$t_{TIMxCLK}$
	Maximum possible count with 32-bit counter (TIM2 to TIM5)	-	65536 × 65536	

1. Specified by design. Not tested in production.
2. TIMx is used as a general term to refer to the TIM1 to TIMx timers.

Table 98. LPTIMx characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{res(LPTIM)}$	Timer resolution time	1	-	$t_{LPTIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	100	MHz
	Timer kernel clock (autonomous mode)	0	32768	Hz
f_{EXT}	Timer external clock frequency on IN1 and IN2	0	$f_{LPTIMxCLK}$ / 2	MHz
Res_{LPTIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$f_{LPTIMxCLK}$

1. Specified by design. Not tested in production.
2. LPTIMx is used as a general term to refer to the LPTIM1 to LPTIM5 timers.

5.3.35 Communications interfaces

SPI interface

Unless otherwise specified, the parameters given in *Table 99* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load: C = 3 0pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.5$ V

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Refer to *Section 5.3.16* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, and MISO for SPI).

Table 99. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Controller mode, 1.65 < V_{DD} < 1.98 V	-	-	115	MHz
		Controller mode, 3.00 < V_{DD} < 3.6 V			105	
		Target receiver mode			100	
		Target mode transmitter/full duplex			50(2)	
$t_{su(NSS)}$	NSS setup time	Target mode	4	-	-	ns
$t_{h(NSS)}$	NSS hold time	Target mode	1	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Controller mode	T_{pclk} - 1	T_{pclk}	T_{pclk} + 1	
$t_{su(MI)}$	Data input setup time	Controller mode	4.5	-	-	
$t_{su(SI)}$		Target mode	4.5	-	-	
$t_{h(MI)}$	Data input hold time	Controller mode	1	-	-	
$t_{h(SI)}$		Target mode	1	-	-	
$t_{a(SO)}$	Data output access time	Target mode	8	9	10.5	
$t_{dis(SO)}$	Data output disable time	Target mode	5.5	8	9	
$t_{v(SO)}$	Data output valid time	Target mode	-	8.5	10	
$t_{v(MO)}$		Controller mode	-	2.5	3	
$t_{h(SO)}$	Data output hold time	Target mode	7.5	-	-	
$t_{h(MO)}$		Controller mode	2	-	-	

1. Evaluated by characterization. Not tested in production.
2. Maximum frequency in target transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a controller having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%.

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Figure 53. SPI timing diagram - Controller mode

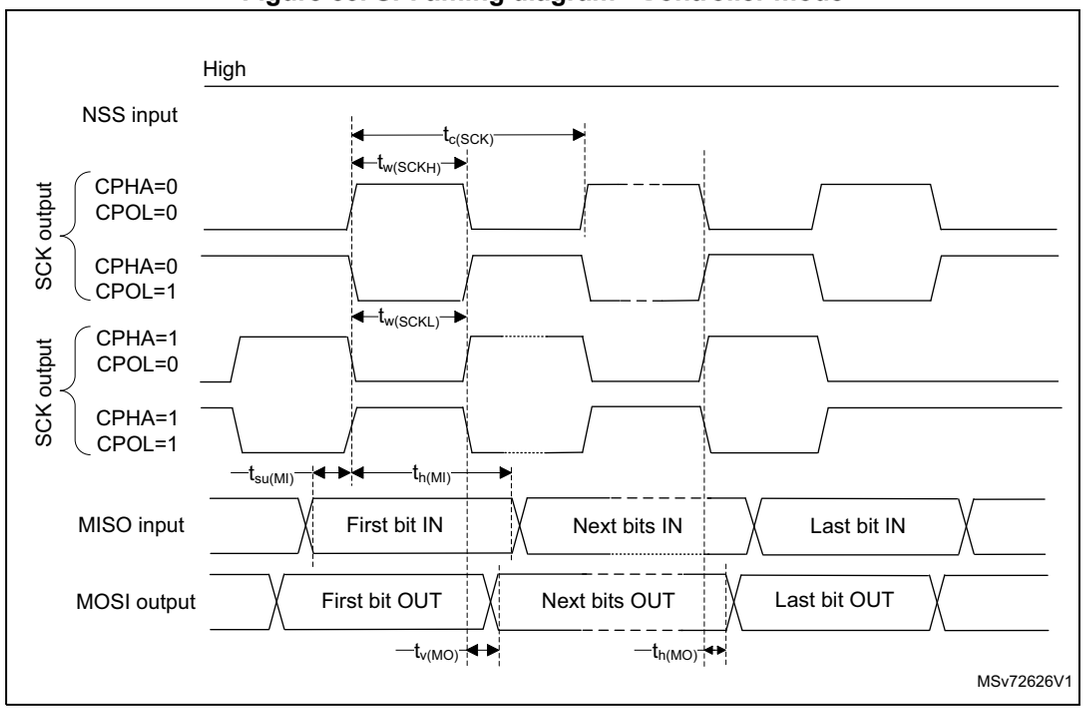
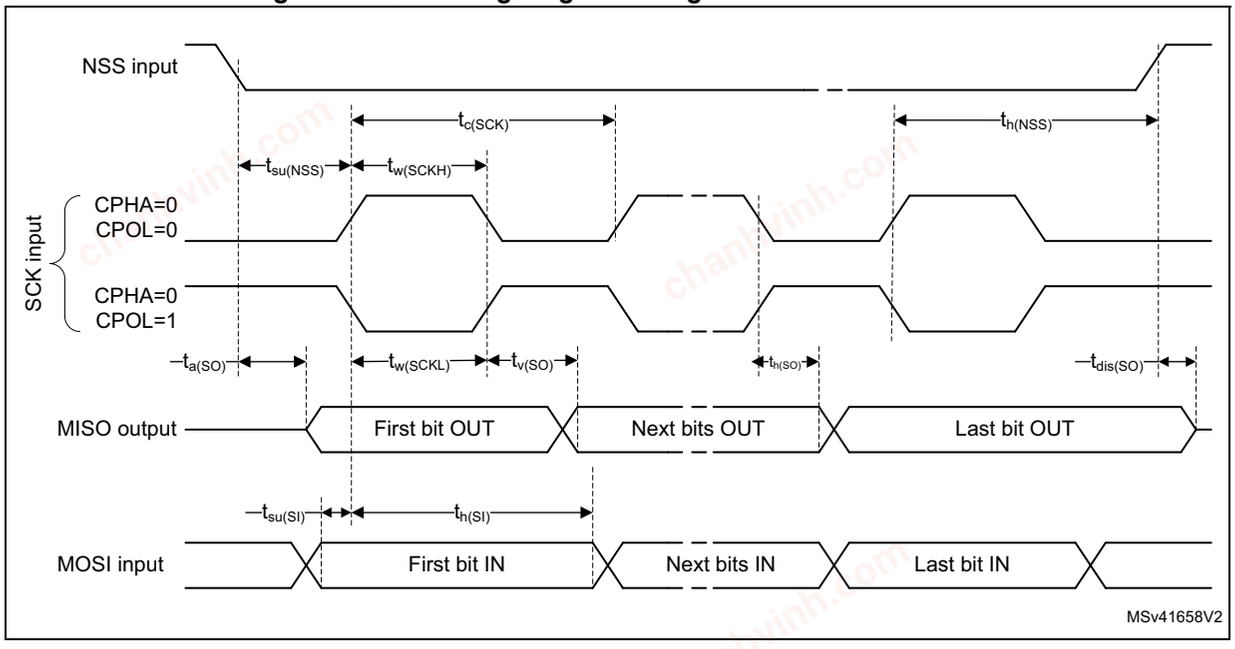
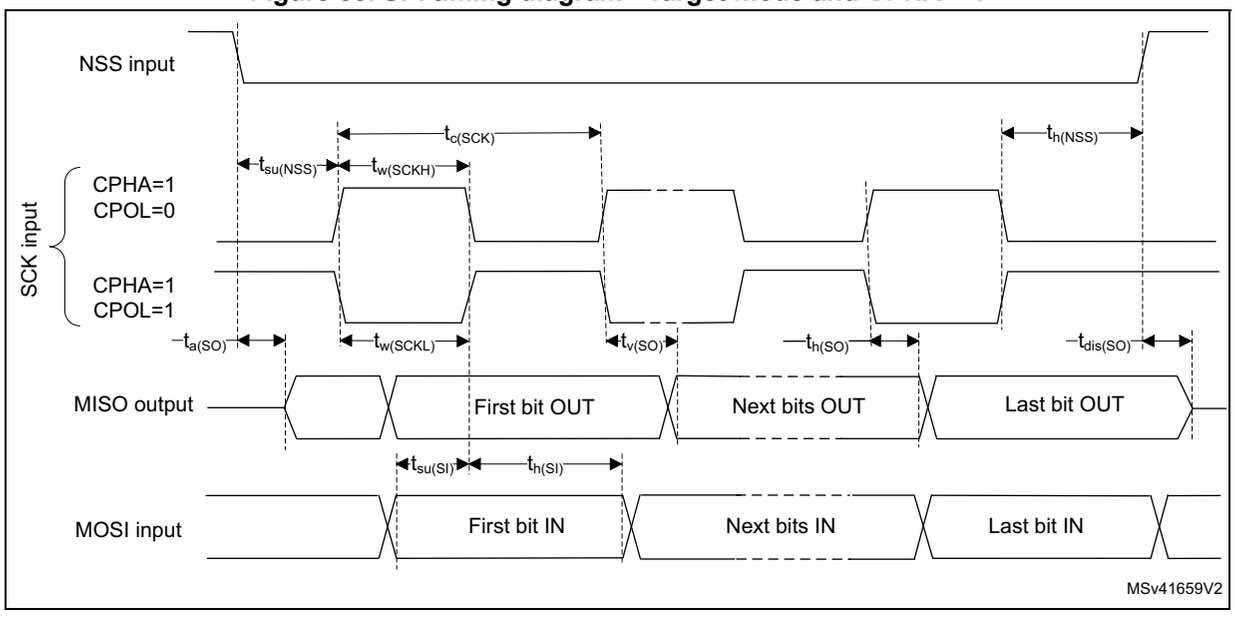


Figure 54. SPI timing diagram - Target mode and CPHA = 0



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Figure 55. SPI timing diagram - Target mode and CPHA = 1



I²C interface

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are specified by design, not tested in production, when the I2C peripheral is properly configured (refer to product reference manual).

Table 100. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes suppressed by analog filter	50(2)	230(3)	ns

1. Evaluated by characterization. Not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

I³C interface

The I³C interface meets the timings requirements of the MIPI® I3C specification v1.1.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

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The parameters given in *Table 101* are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V
- Voltage scale is set to VOS[0] = 1.

Table 101. I3C open-drain measured timing(1)

Symbol	Parameter	Conditions	I3C open drain mode		Timing measurements		Unit
			Min	Max	Min	Max	
t_{SU_OD}	SDA data setup time during open drain mode	Controller	3	-	20(2)	-	ns

1. Evaluated by characterization. Not tested in production.
2. This timing is not in line with minimal value in MIPI specification. This can be mitigated by adjusting the clock stall time on the Tbit phase through the I3C_TIMINGR2 register, and/or by increasing the SCL low duration in the TIMINGR0 register. For further details, refer to AN5879 "*Introduction to I3C for STM32 MCUs*".

Table 102. I3C push-pull measured timing(1)

Symbol	Parameter	Conditions	I3C push-pull mode		Timing measurements		Unit
			Min	Max	Min	Max	-
t_{SU_PP}	SDA signal data setup in push-pull mode	Controller	3	-	18(2)	-	ns

1. Evaluated by characterization. Not tested in production.
2. This timing is not in line with minimal value in MIPI specification. This can be mitigated by adjusting the clock stall time on the Tbit phase through the I3C_TIMINGR2 register, and/or by increasing the SCL low duration in the TIMINGR0 register. For further details, refer to AN5879 "*Introduction to I3C for STM32 MCUs*".

I2S interface

Unless otherwise specified, the parameters given in *Table 103* for I2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load: C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V

Refer to *Section 5.3.16* for more details on the input/output alternate function characteristics (CK,SDO,SDI,WS).

Table 103. I2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	-	-	50	MHz

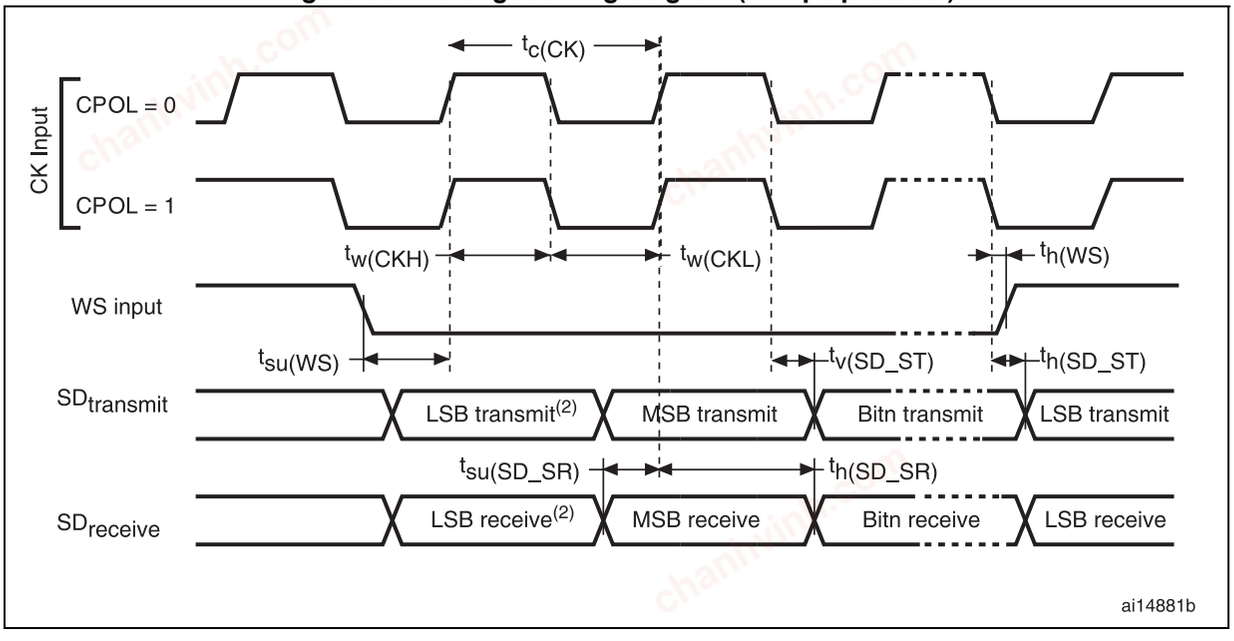
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Table 103. I2S characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK}	I2S clock frequency	Controller	-	50	MHz
		Target TX	-	27	
		Target RX	-	50	
$t_{v(WS)}$	WS valid time	Controller mode	-	3.5	ns
$t_{h(WS)}$	WS hold time	Controller mode	1.5	-	
$t_{su(WS)}$	WS setup time	Target mode	3	-	
$t_{h(WS)}$	WS hold time	Target mode	1	-	
$t_{su(SD_MR)}$	Data input setup time	Controller receiver	4	-	
$t_{su(SD_SR)}$		Target receiver	4.5	-	
$t_{h(SD_MR)}$	Data input hold time	Controller receiver	1	-	
$t_{h(SD_SR)}$		Target receiver	0	-	
$t_{v(SD_ST)}$	Data output valid time	Target transmitter (after enable edge)	-	11	
$t_{v(SD_MT)}$		Controller transmitter (after enable edge)	-	3.5	
$t_{h(SD_ST)}$	Data output hold time	Target transmitter (after enable edge)	8	-	
$t_{h(SD_MT)}$		Controller transmitter (after enable edge)	0.5	-	

1. Evaluated by characterization. Not tested in production.

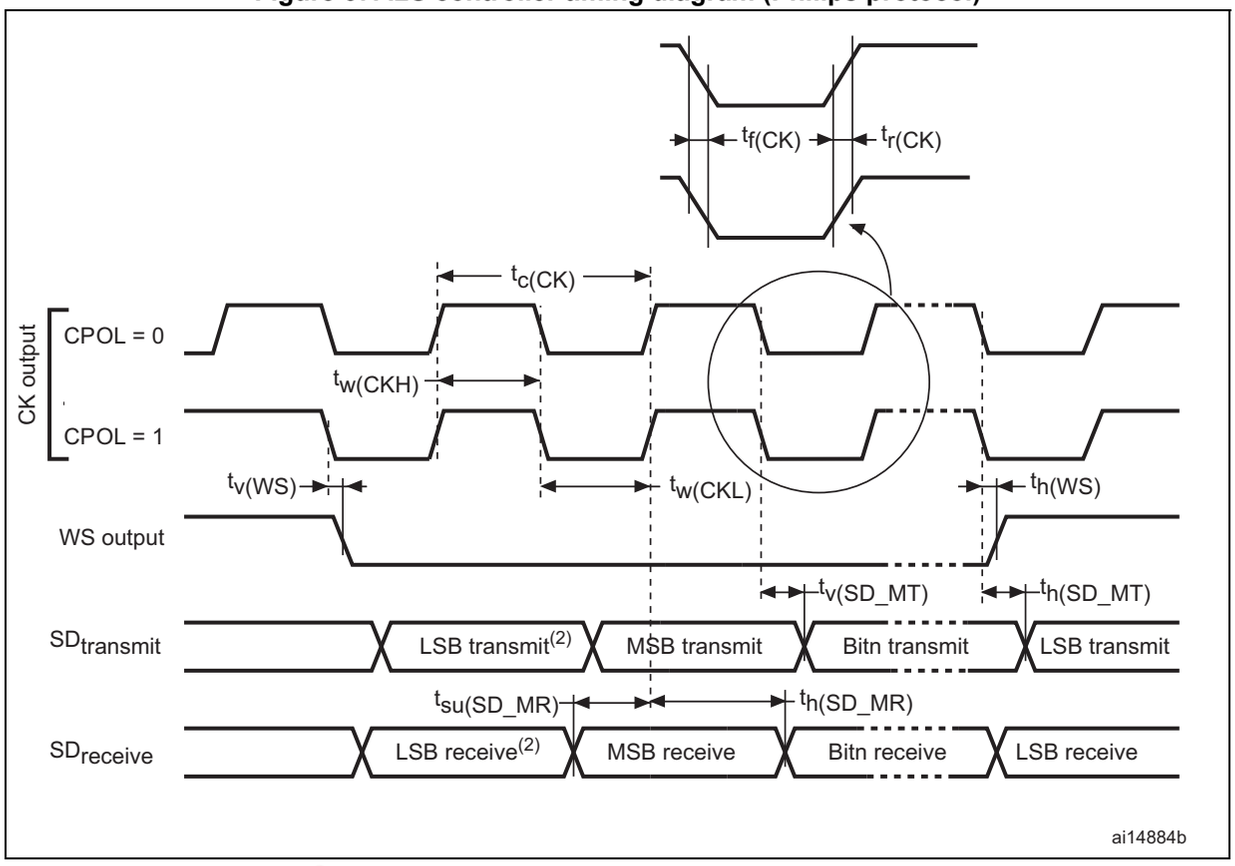
Figure 56. I2S target timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

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Figure 57. I2S controller timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SAI interface

Unless otherwise specified, the parameters given in *Table 104* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 5.3.16* for more details on the input/output alternate function characteristics (CK,SD,WS).

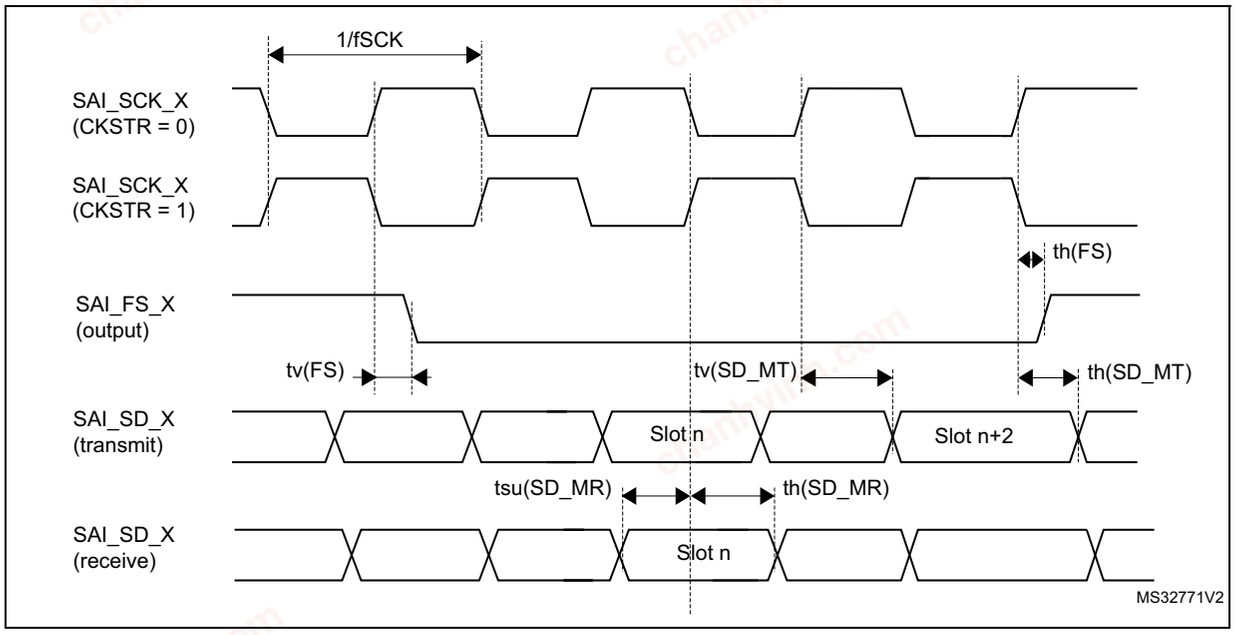
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Table 104. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Controller transmitter	-	38	
		Controller receiver	-	34	
		Target transmitter	-	40	
		Target receiver	-	50	
$t_{v(FS)}$	FS valid time	Controller mode	-	13	ns
$t_{h(FS)}$	FS hold time	Controller mode	9	-	
$t_{su(FS)}$	FS setup time	Target mode	3.5	-	
$t_{h(FS)}$	FS hold time	Target mode	1	-	
$t_{su(SD_A_MR)}$	Data input setup time	Controller receiver	4	-	
$t_{su(SD_B_SR)}$		Target receiver	4	-	
$t_{h(SD_A_MR)}$	Data input hold time	Controller receiver	1	-	
$t_{h(SD_B_SR)}$		Target receiver	1	-	
$t_{v(SD_B_ST)}$	Data output valid time	Target transmitter (after enable edge)	-	12.5	
$t_{h(SD_B_ST)}$	Data output hold time	Target transmitter (after enable edge)	8	-	
$t_{v(SD_A_MT)}$	Data output valid time	Controller transmitter (after enable edge)	-	12.5	
$t_{h(SD_A_MT)}$	Data output hold time	Controller transmitter (after enable edge)	8.5	-	

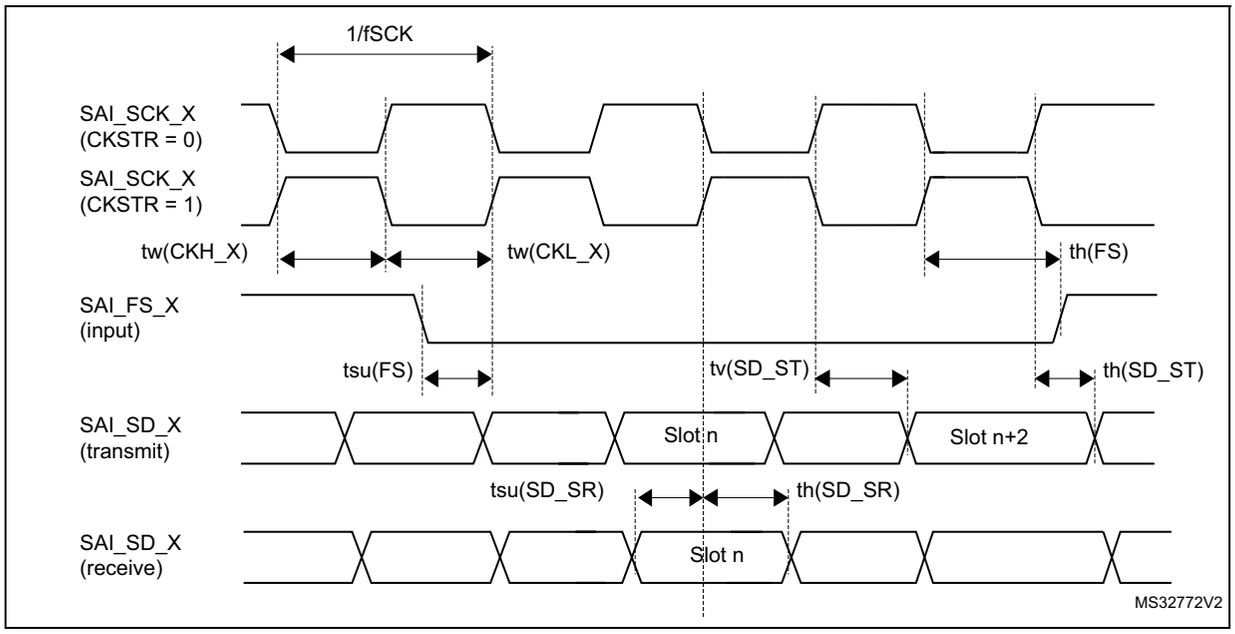
1. Evaluated by characterization. Not tested in production.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 58. SAI controller timing waveforms



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Figure 59. SAI target timing waveforms



Ethernet (ETH) interface

Unless otherwise specified, the parameters given in *Table 105* to *Table 108* for MDIO/SMA, RMII, MII, RGMII, and RGMII ID are derived from tests performed under the ambient temperature, f_{HCLKx} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 5.3.16* for more details on the input/output characteristics.

Table 105. Dynamic characteristics: Ethernet MAC signals for MDIO/SMA(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	399	400	401	ns
$T_{d(MDIO)}$	Write data valid time	3.5	4.5	5	
$t_{su(MDIO)}$	Read data setup time	16	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Evaluated by characterization. Not tested in production.

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Figure 60. Ethernet MDIO/SMA timing diagram

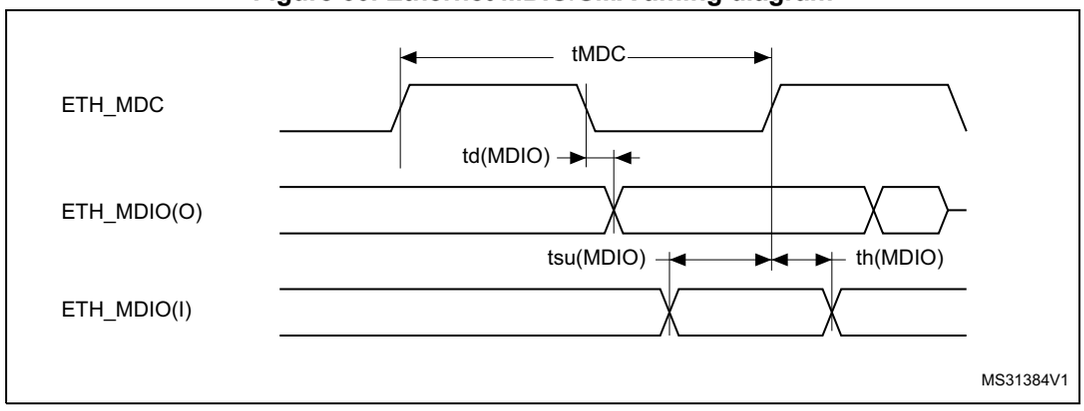
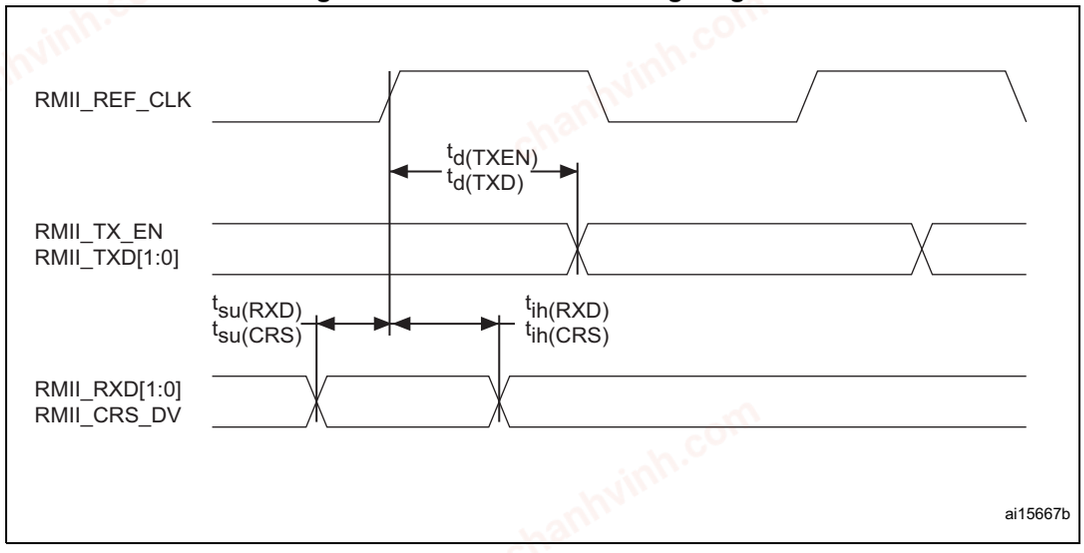


Table 106. Dynamic characteristics: Ethernet MAC signals for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1.5	-	-	
$t_{su(CRS)}$	Carrier sense setup time	2	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	1.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	4	5	6	
$t_{d(TXD)}$	Transmit data valid delay time	4	5	6	

1. Evaluated by characterization. Not tested in production.

Figure 61. Ethernet RMII timing diagram



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Table 107. Dynamic characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1.5	-	-	
$t_{su(DV)}$	Data valid setup time	1	-	-	
$t_{ih(DV)}$	Data valid hold time	1.5	-	-	
$t_{su(ER)}$	Error setup time	1.5	-	-	
$t_{ih(ER)}$	Error hold time	1	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	5	6	7.5	
$t_{d(TXD)}$	Transmit data valid delay time	5	6	7.5	

1. Evaluated by characterization. Not tested in production.

Figure 62. Ethernet MII timing diagram

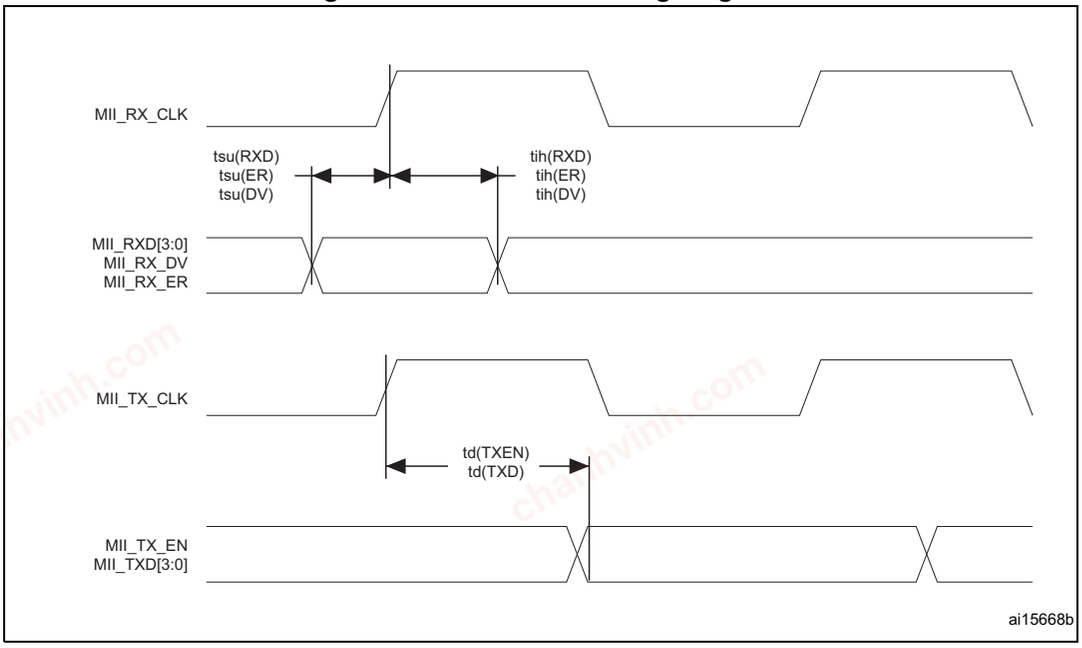


Table 108. Dynamic characteristics: Ethernet MAC signals for RGMII ID(1)(2)(3)

Symbol	Rating	Min	Typ	Max	Unit
T_{cyc}	Clock cycle duration	7.5	8	8.5	ns
$T_{skew_R\ (RXD)}$	Receive data skew time	-1(4)	-	0.5(4)	
$T_{skew\ R\ (DV)}$	Receive valid skew time	-1(4)	-	0.5(4)	
$T_{setup\ T\ (TXEN)}$	Transmit enable to clock output setup time	1.4(5)	-	-	
$T_{setupT(TXD)}$	Transmit data to clock output setup time	1.4(5)	-	-	
$T_{hold\ T\ (TXEN)}$	Transmit clock to transmit enable output hold time	1.4(5)	-	-	
$T_{hold\ T\ (TXD)}$	Transmit clock to data output hold time	1.4(5)	-	-	

1. Evaluated by characterization. Not tested in production.

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2. RGMII TX/RX data bits are retimed.
3. Test done at 100 MHz.
4. With delay on RGMII_RX_CLK (GPIOx_DELAYR) = 0b1110.
5. With delay on RGMII_TX_CLK (GPIOx_DELAYR) = 0b1010.

USART (SPI mode) interface

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 5.3.16* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 109. USART (SPI mode) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
f_{SCK}	Clock frequency	Controller mode, 1.65 V ≤ V_{DD} ≤ 3.6 V	-	-	12.5	MHz
		Target mode, 1.65 V ≤ V_{DD} ≤ 3.6 V	-	-	33	
$t_{su(NSS)}$	NSS setup time	Target mode	t_{ker}+3	-	-	ns
$t_{h(NSS)}$	NSS hold time	Target mode	0.5	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Controller mode	1 / f_{ck} / 2 - 1	1 / f_{ck} / 2	1 / f_{ck} / 2 + 1	
$t_{su(RX)}$	Data input setup time	Controller mode	13	-	-	
$t_{su(TX)}$		Target mode	6	-	-	
$t_{h(RX)}$	Data input hold time	Controller mode	0	-	-	
$t_{h(RX)}$		Target mode	0	-	-	
$t_{v(TX)}$	Data output valid time	Target mode	-	11.5	14	
$t_{v(TX)}$		Controller mode	-	4.5	5.5	
$t_{h(TX)}$	Data output hold time	Target mode	10	-	-	
$t_{h(TX)}$		Controller mode	3	-	-	

1. Evaluated by characterization. Not tested in production.

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Figure 63. USART timing diagram in SPI controller mode

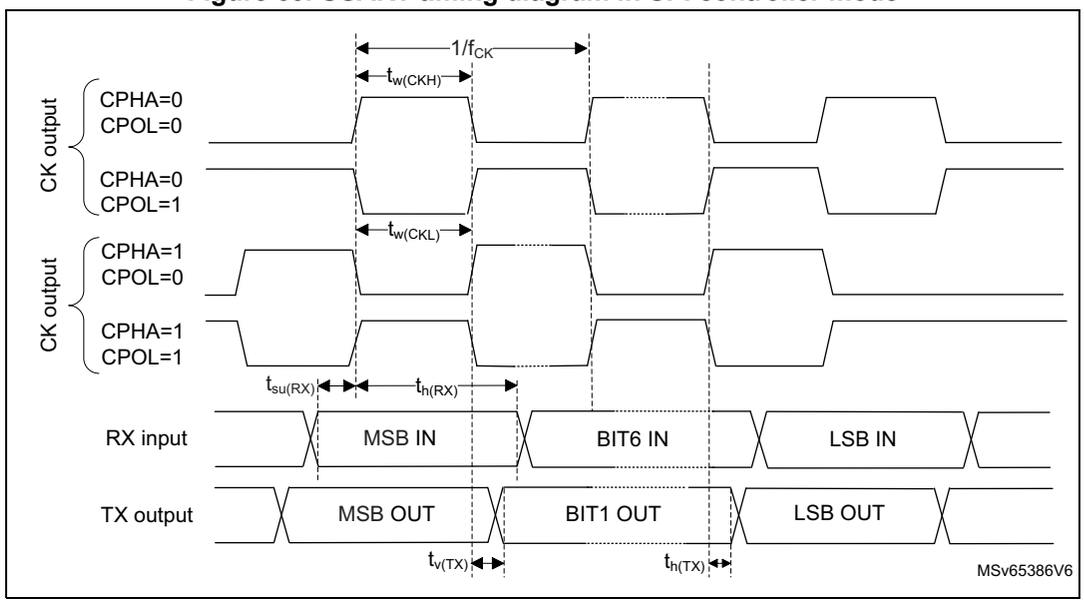
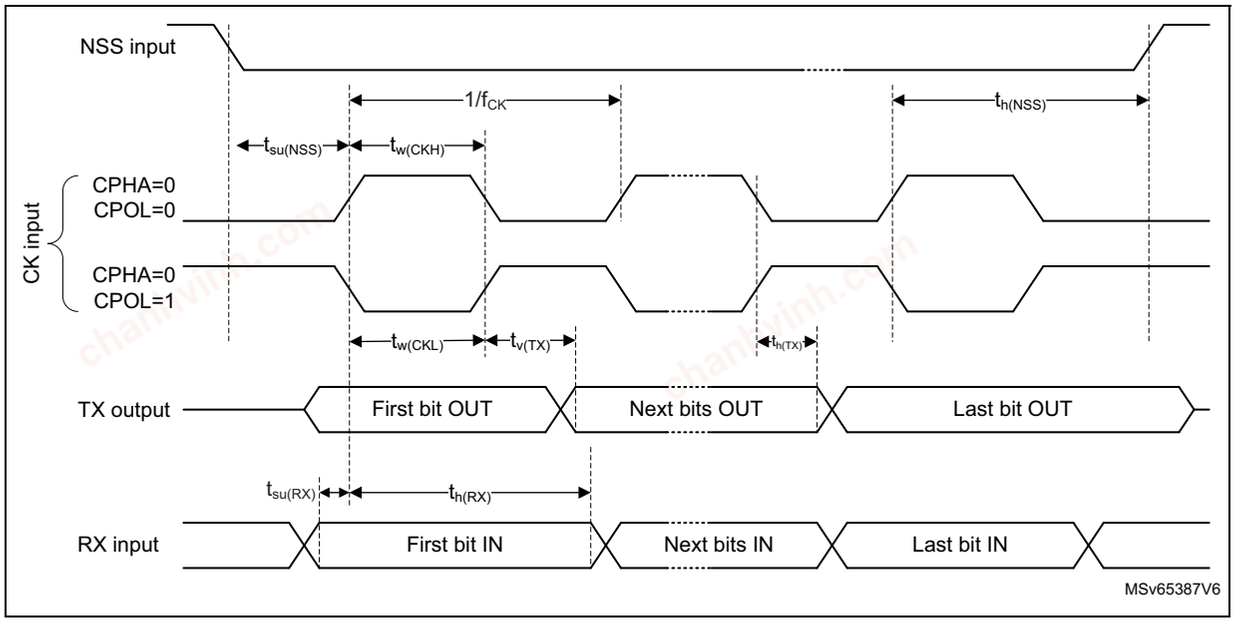


Figure 64. USART timing diagram in SPI target mode



FDCAN (controller area network) interface

Refer to *Section 5.3.16* for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).

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5.3.36 Embedded PHY characteristics

CSI PHY characteristics

Table 110. CSI PHY characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Typ	Unit
R_{EXT}	External resistor on R_{EXT}	Connected to ground		198	200	202	Ω
$I_{VDDCORE(CSIPHY)}$	Supply current on V_{DDCORE}	High-speed receive(2)	2 lanes at 1 Gbps	-	2.21	12.36	mA
			2 lanes at 1.5 Gbps	-	3.14	13.91	
			2 lanes at 2 Gbps	-	4.07	14.94	
			2 lanes at 2.5 Gbps	-	5.00	16.48	
		LP receive	Lane 0 at 10 Mbps	-	0.42	8.29	
		ULPS receive	ck_ker_csi2phy stopped	-	0.06	8.70	
$I_{VDDA18CSI}$	Supply current on $V_{DDA18CSI}$	High-speed receive(2)	2 lanes at 1 Gbps	2.19	2.23	2.84	mA
			2 lanes at 1.5 Gbps	2.31	2.36	3.00	
			2 lanes at 2 Gbps	2.55	2.65	3.35	
			2 lanes at 2.5 Gbps	2.54	2.64	3.35	
		LP receive	Lane 0 at 10 Mbps	1.53	1.72	2.25	
		ULPS receive	ck_ker_csi2phy stopped	0.01	0.01	0.02	
I_{VDDCSI}	Supply current on V_{DDCSI}	High-speed receive(2)	2 lanes at 1 Gbps	3.51	4.06	5.80	mA
			2 lanes at 1.5 Gbps	3.99	4.66	6.60	
			2 lanes at 2 Gbps	2.99	3.40	4.65	
			2 lanes at 2.5 Gbps	3.41	3.86	5.25	
		LP receive	Lane 0 at 10 Mbps	0.68	0.74	0.95	
		ULPS receive	ck_ker_csi2phy stopped	0.00	0.00	0.01	

1. Specified by design and not tested in production, unless otherwise specified.
2. The high-speed mode assumes PRBS9 pattern on data lanes and 100% occupation, that is continuous high speed.

USB PHY characteristics

Table 111. USB PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{TXRTUNE}$	External resistor on TXRTUNE	Connected to ground	198	200	202	Ω

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Table 111. USB PHY characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{VDDCORE(USB2PHY)}$	Supply current on V_{DDCORE}	HS transmit, maximum transition density(2)		-	7.52	23.72	mA
		HS transmit, minimum transition density(3)		-	7.35	23.88	
		HS idle(4)		-	8.21	23.91	
		FS transmit, maximum transition density(5)		-	6.53	23.22	
		LS transmit, maximum transition density(6)		-	6.45	24.70	
		Suspend(7)		-	1.25	11.75	
		Sleep(8)		-	1.24	11.52	
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1	-	3.17	17.26	
			VDATDETENB = 1, VDATSRCENB = 1(9)	-	5.82	23.80	
$I_{VDDA18USB}$	Supply current on $V_{DDA1V8USB}$	HS transmit, maximum transition density(2)		-	13.35	17.92	mA
		HS transmit, minimum transition density(3)		-	9.69	9.71	
		HS idle(4)		-	5.10	5.67	
		FS transmit, maximum transition density(5)		-	5.14	5.71	
		LS transmit, maximum transition density(6)		-	5.12	5.69	
		Suspend(7)		-	0.04	0.08	
		Sleep(8)		-	0.04	0.08	
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1	-	3.48	3.88	
			VDATDETENB = 1, VDATSRCENB = 1(9)	-	4.16	4.55	
$I_{VDD33USB}$	Supply current on $V_{DD33USB}$	HS transmit, maximum transition density(2)		-	3.39	3.64	mA
		HS transmit, minimum transition density(3)		-	2.32	2.53	
		HS idle(4)		-	2.15	2.34	
		FS transmit, maximum transition density(5)		-	16.84	16.84	
		LS transmit, maximum transition density(6)		-	13.39	14.81	
		Suspend(7)		-	0.07	0.17	
		Sleep(8)		-	0.07	0.17	
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1	-	2.15	2.35	
			VDATDETENB = 1, VDATSRCENB = 1(9)	-	2.15	2.34	

1. Evaluated by characterization and not tested in production, unless otherwise specified.
2. Packet transmission by one transceiver operating in device mode while driving all 0s data (constant JKJK on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.
3. Packet transmission by one transceiver operating in device mode while driving all 1s data (alternating 7-bit strings of J, then K on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.
4. HS receive mode with no traffic on the line.

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5. Packet transmission by one transceiver operating in device mode while driving all 0s data (constant JKJK on DP/DM). Loading of 50 pF. Transfers do not include any interpacket delay.
6. Packet transmission by one transceiver operating in host mode while driving all 0s data (constant JKJK on DP/DM). Loading of 600 pF. Transfers do not include any interpacket delay.
7. Suspend when operating in device mode with no far-side host termination on DP/DM during measurements. Measurements taken when COMMONONN (SYSCFG_USB2PHYxCR.USB2PHYxCMN) is deasserted.
8. Sleep mode when operating in device mode with no far-side host termination on DP/DM during measurements.
9. PHY is in suspend (with clocks turned OFF), nondriving mode and operating as a portable device in the “dead battery” condition.

UCPD PHY characteristics

Table 112. UCPDPHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{BITRATE}$	Bit rate (ensured by adequate RCC and UCPD settings)		270	300	330	Kbps
$C_{RECEIVER}$	Local capacitance added on PCB on each CC line		200	470	600	pF
Transmitter						
V_{SWING}	Voltage swing applies on CC pin to both no load condition and under the load condition.		1.05	1.125	1.2	V
Z_{DRIVER}	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750 kHz) while the source is driving the CC line.		33	-	75	Ω
T_r / T_f	Rise/fall time. 10% to 90% / 90% to 10% amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300	-	735	ns
DCYCLE	TX duty cycle at 0.5625 V (see Y5Tx, BMC Tx 'ONE' Mask and BMC Tx 'ZERO' Mask in the PD Specification)		47	-	53	%
Receiver						
V_{IL}	Rx receive input thresholds. The position of the center line of the inner mask is dependent on whether the receiver is sourcing or sinking power or is power neutral.	Sourcing power	-	-	0.4825	V
V_{IH}			0.8925	-	-	
V_{IL}		Sinking power	-	-	0.2325	V
V_{IH}			0.6425	-	-	
Hysteresis	Rx receive input hysteresis		0.15	-	-	
N_{COUNT}	Number of transitions for signal detection (number to count to detect non-idle bus).		3	-	-	-
$t_{TRANWIN}$	Time window for detecting non-idle bus		12	-	20	µs
Z_{BMCRX}	Receiver input impedance		1	-	-	MΩ

1. Evaluated by characterization and not tested in production, unless otherwise specified.

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5.3.37 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 113* are derived from tests performed under the ambient temperature, f_{HCLKx} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x01
- Capacitive load C = 30 pF
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.16* for more details on the input/output characteristics.

Table 113. Dynamic characteristics: JTAG

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp} $1 / t_{c(TCK)}$	TCK clock frequency	1.65 < V_{DD} < 3.6 V	-	-	40	MHz
$ti_{su(TMS)}$	TMS input setup time		4	-	-	ns
$ti_{h(TMS)}$	TMS input hold time		1	-	-	
$ti_{su(TDI)}$	TDI input setup time		4	-	-	
$ti_{h(TDI)}$	TDI input hold time		1	-	-	
$to_{v\ (TDO)}$	TDO output valid time		-	10	12	
$to_{h(TDO)}$	TDO output hold time		9.5	-	-	

Table 114. Dynamic characteristics: SWD

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp} $1 / t_{c(SWCLK)}$	SWCLK clock frequency	1.65 < V_{DD} < 3.6 V	-	-	80	MHz
$ti_{su(SWDIO)}$	SWDIO input setup time		4	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time		1	-	-	
$to_{v\ (SWDIO)}$	SWDIO output valid time		-	10	12	
$to_{h(SWDIO)}$	SWDIO output hold time		8	-	-	

MDIOS target interface

Unless otherwise specified, the parameters given in *Table 115* are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load: C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V

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Table 115. MDIO target timing parameters(1)

Symbol	Parameter	Min	Typ	Max	Unit
F_{MDC}	Clock	-	-	30	MHz
$t_{d(MDIO)}$	Input/output valid time	7	8	14	ns
$t_{su(MDIO)}$	Input/output setup time	2	-	-	
$t_{h(MDIO)}$	Input/output hold time	0.5	-	-	

1. Evaluated by characterization. Not tested in production.

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6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 Device marking

Refer to “*Reference device marking schematics for STM32 microcontrollers and microprocessors*” (TN1433), available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

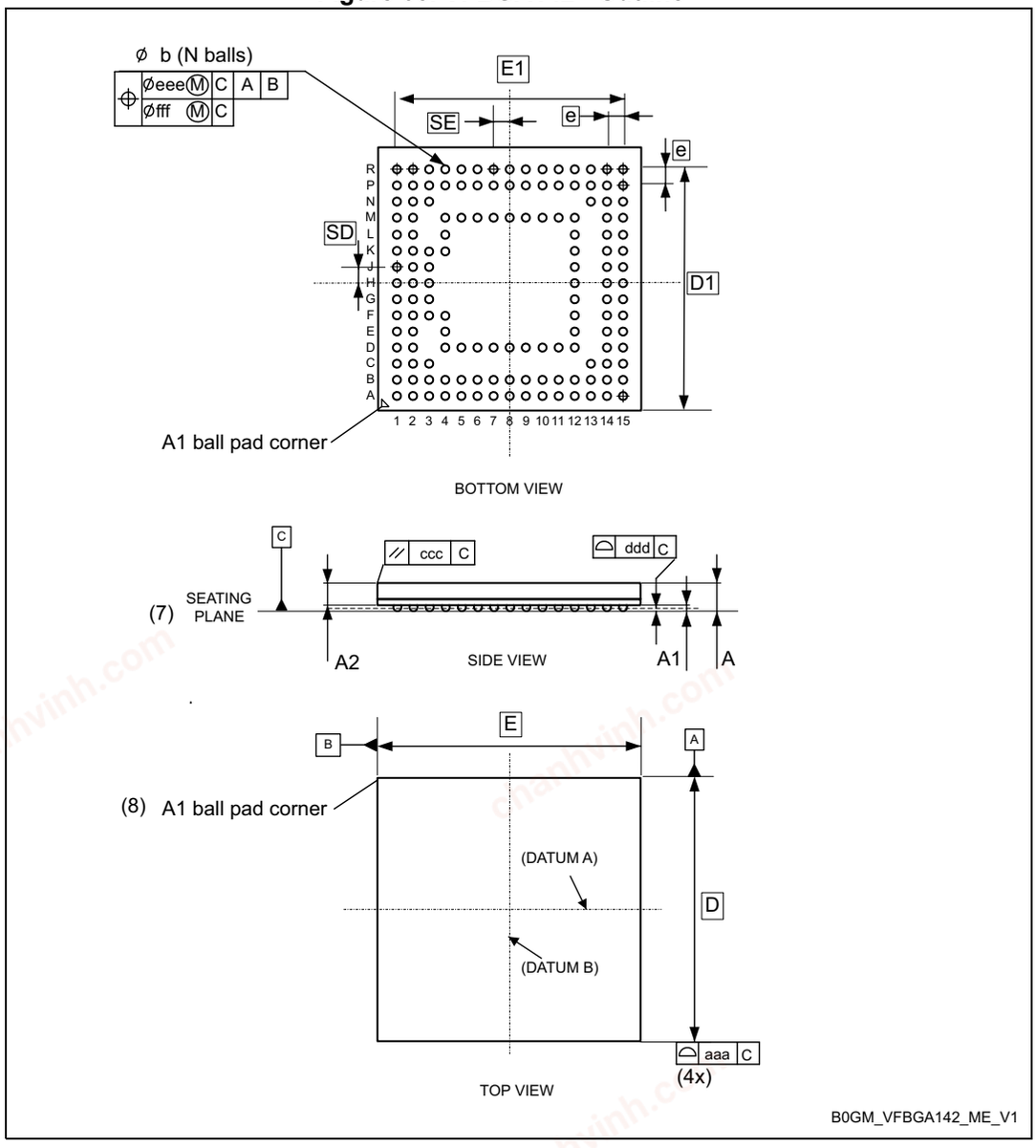
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6.2 VFBGA142 package information (B0GM)

This VFBGA is a 142-ball, 8 x 8 mm, 0.50 mm pitch, very thin fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 65. VFBGA142 - Outline(13)



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Table 116. VFBGA142 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	-	-	1.00	-	-	0.0394
A1[4]	0.13	-	-	0.0051	-	-
A2	-	0.59	-	-	0.0232	-
b[5]	0.26	0.31	0.36	0.0102	0.0122	0.0142
D[6]	8.00 BSC			0.3149 BSC		
D1	7.00 BSC			0.2756 BSC		
E	8.00 BSC			0.3149 BSC		
E1	7.00 BSC			0.2756 BSC		
e[9]	0.50 BSC			0.0197 BSC		
N[10]	142					
SD[11]	0.50 BSC			0.0197 BSC		
SE[11]	0.50 BSC			0.0197 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.05			0.0020		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.

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8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

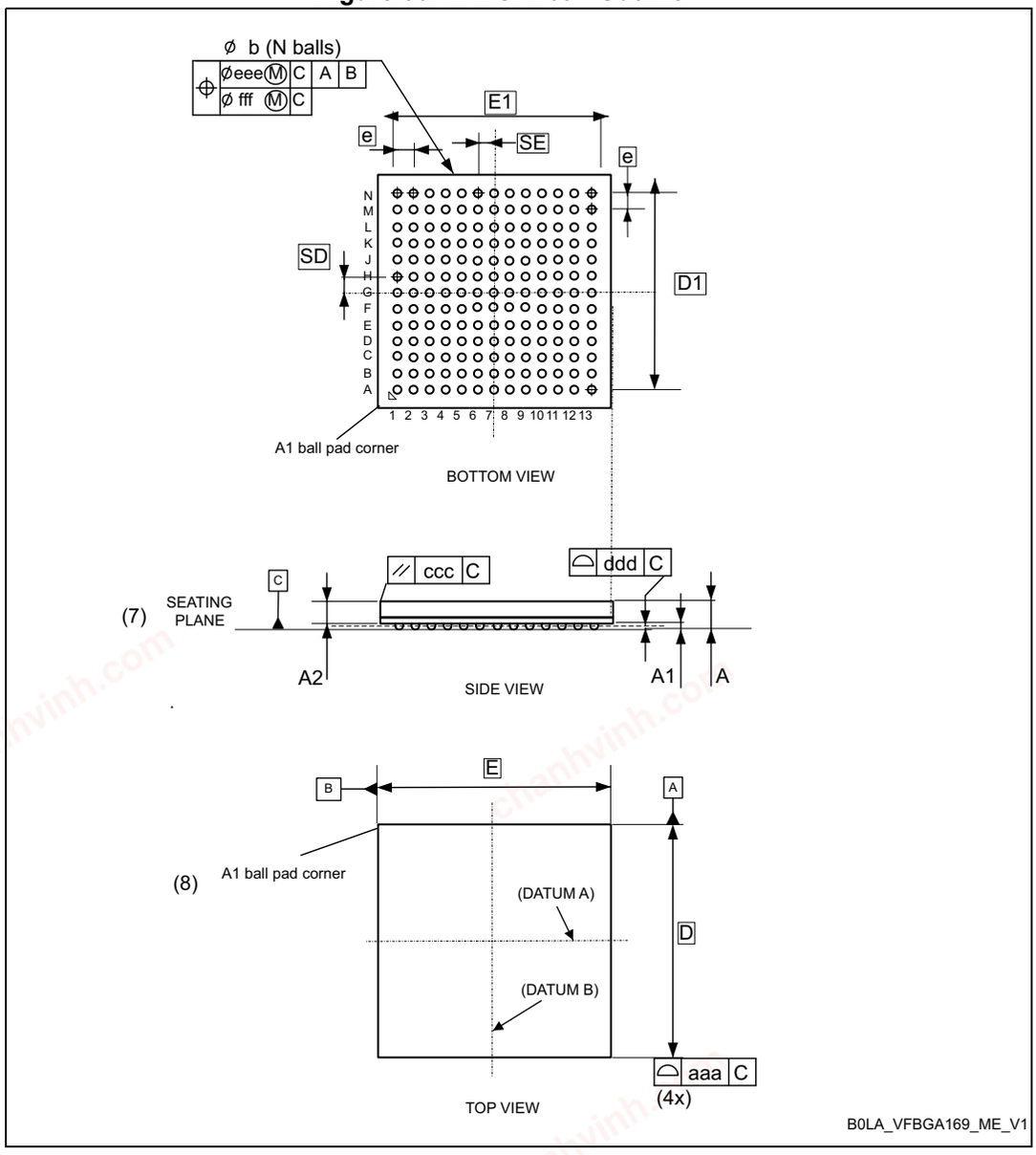
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6.3 VFBGA169 package information (B0LA)

This VFBGA is a 169-ball, 6 x 6 mm, 0.4 mm pitch, very thin fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 66. VFBGA169 - Outline(13)



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Table 117. VFBGA169 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	-	-	1.00	-	-	0.0394
A1[4]	0.11	-	-	0.0043	-	-
A2	-	0.62	-	-	0.0344	-
b[5]	0.22	0.26	0.30	0.0087	0.0102	0.0118
D[6]	6.00 BSC			0.2362 BSC		
D1	4.80 BSC			0.1890 BSC		
E	6.00 BSC			0.2362 BSC		
E1	4.80 BSC			0.1890 BSC		
e[9]	0.40 BSC			0.0157 BSC		
N[10]	169					
SD[11]	0.40 BSC			0.0157 BSC		
SE[11]	0.40 BSC			0.0157 BSC		
aaa	0,10			0.0039		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.05			0.0020		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2018.
2. VFBGA stands for very thin fine pitch ball grid array: 0.80 mm < A ≤ 1.00 mm / Fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or

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integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD & SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

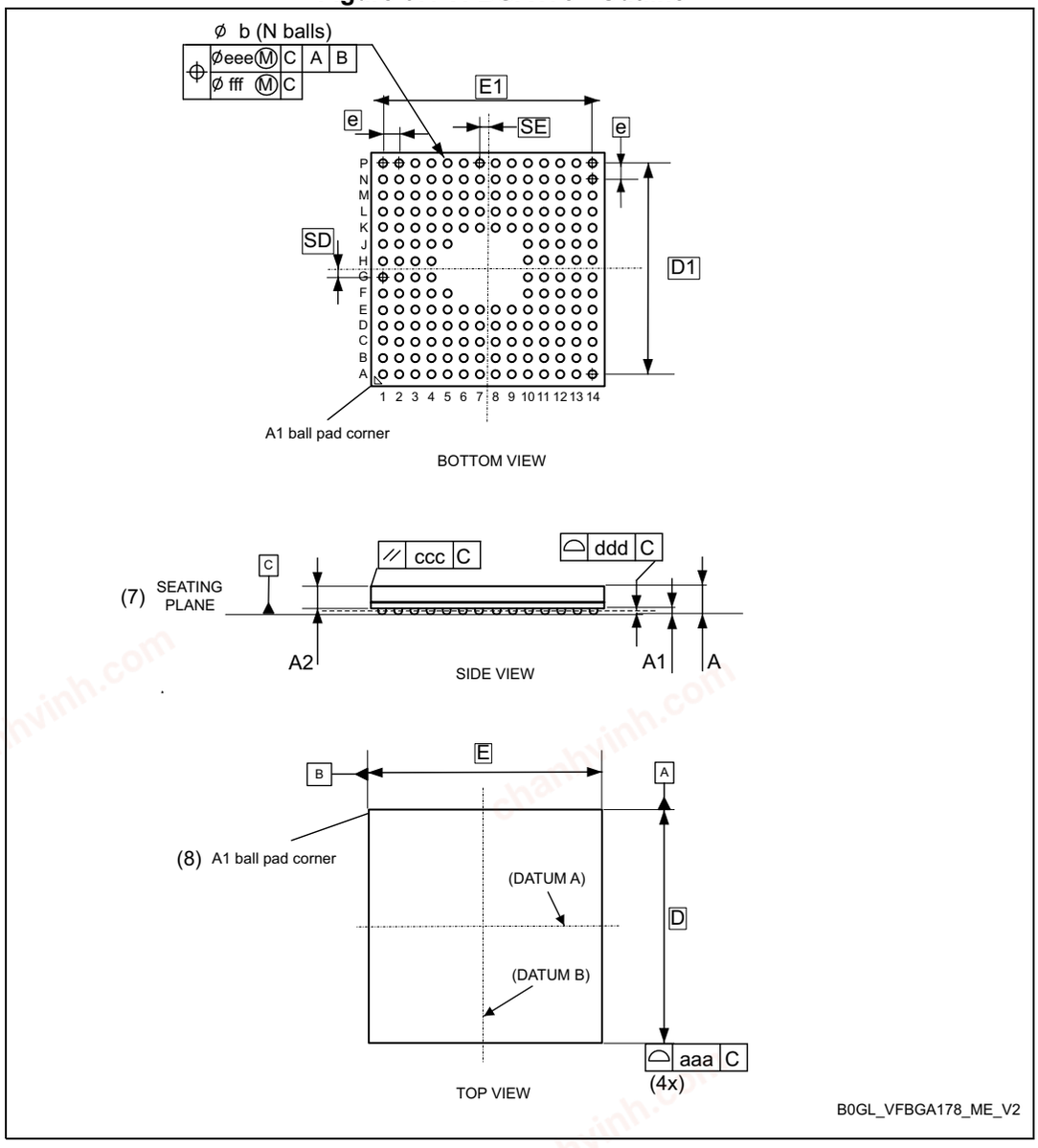
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6.4 VFBGA178 package information (B0GL)

This VFBGA is a 178-ball, 12 x 12 mm, 0.80 mm pitch, very thin fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 67. VFBGA178 - Outline(13)



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Table 118. VFBGA178 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	-	-	1.00	-	-	0.0394
A1[4]	0.21	-	-	0.0082	-	-
A2	-	0.51	-	-	0.0201	-
b[5]	0.38	0.43	0.48	0.150	0.0170	0.189
D[6]	12.00 BSC			0.4724 BSC		
D1	10.40 BSC			0.4094 BSC		
E	12.00 BSC			0.4724 BSC		
E1	10.40 BSC			0.4094 BSC		
e[9]	0.80 BSC			0.0315 BSC		
N[10]	178					
SD[11]	0.40 BSC			0.0157 BSC		
SE[11]	0.40 BSC			0.0157 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.0031		

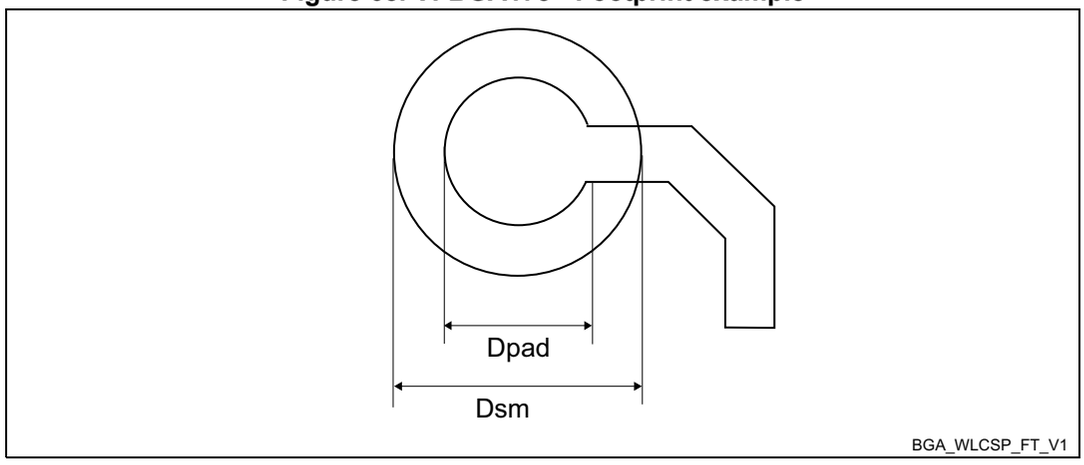
Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.

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8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

Figure 68. VFBGA178 - Footprint example



1. Dimensions are expressed in millimeters.

Table 119. VFBGA178 - Example of PCB design rules (0.80 mm pitch BGA)

Dimension	Values
Pitch	0.8 mm
Dpad	0.400 mm
Dsm	0.470 mm typ.
Stencil opening	0.400 mm
Stencil thickness	0.100 mm

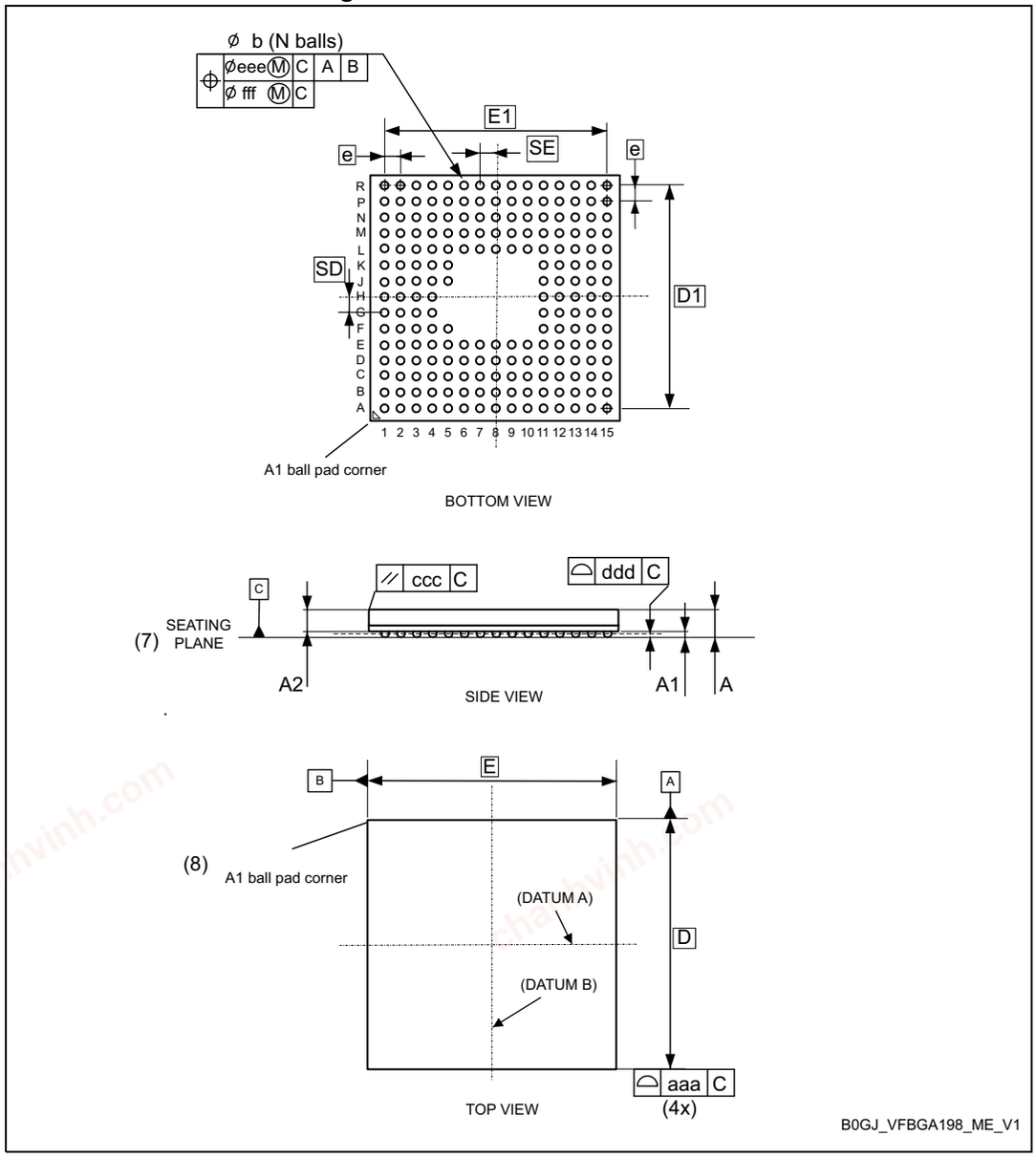
6.5 VFBGA198 package information (B0GJ)

This VFBGA is a 198-ball, 10 x 10 mm, 0.65 mm pitch, very thin fine pitch ball grid array package.

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Note: See list of notes in the notes section.

Figure 69. VFBGA198 - Outline(13)



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Table 120. VFBGA198 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	-	-	1.00	-	-	0.0394
A1[4]	0.21	-	-	0.0082	-	-
A2	-	0.51	-	-	0.0201	-
b[5]	0.35	0.40	0.45	0.0138	0.0157	0.0177
D[6]	10.00 BSC			0.3937BSC		
D1	9.10 BSC			0.3583 BSC		
E	10.00 BSC			0.3937BSC		
E1	9.10 BSC			0.3583 BSC		
e[9]	0.65 BSC			0.0256 BSC		
N[10]	198					
SD[11]	0.65 BSC			0.0256 BSC		
SE[11]	0.65 BSC			0.0256 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.00315		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.

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8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

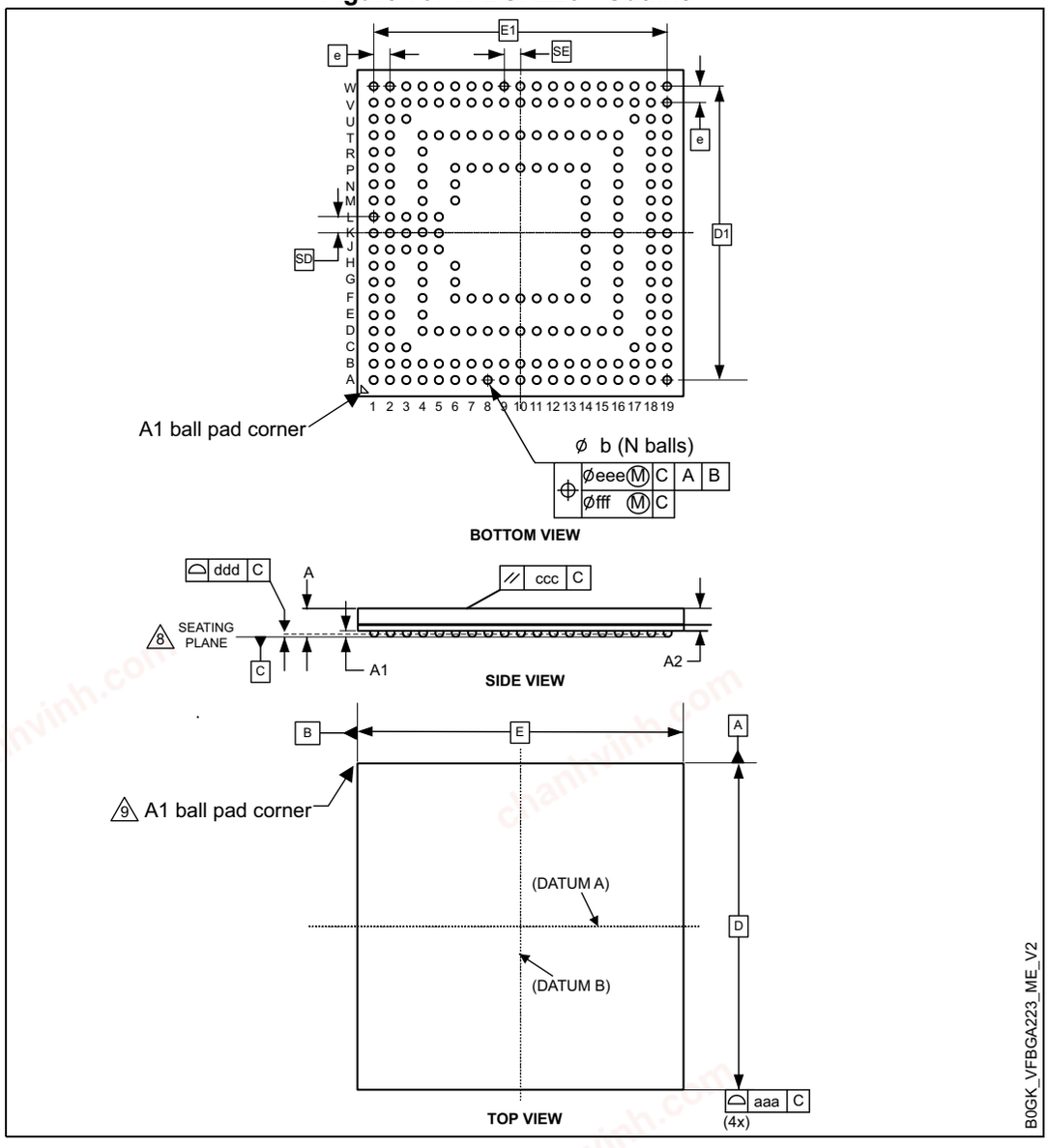
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6.6 VFBGA223 package information (B0GK)

This VFBGA is a 223-ball, 10 x 10 mm, 0.50 mm pitch, very thin fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 70. VFBGA223 - Outline(13)



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Table 121. VFBGA223 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	-	-	1.00	-	-	0.0394
A1[4]	0.13	-	-	0.0051	-	-
A2	-	0.51	-	-	0.0201	-
b[5]	0.26	0.31	0.36	0.0102	0.0122	0.0142
D[6]	10.00 BSC			0.3937BSC		
D1	9.00 BSC			0.3543 BSC		
E	10.00 BSC			0.3937BSC		
E1	9.00 BSC			0.3543 BSC		
e[9]	0.50 BSC			0.0197 BSC		
N[10]	223					
SD[11]	0.50 BSC			0.0197 BSC		
SE[11]	0.50 BSC			0.0197 BSC		
aaa[12]	0.15			0.0059		
ccc[12]	0.20			0.0079		
ddd[12]	0.08			0.0031		
eee[12]	0.15			0.0059		
fff[12]	0.05			0.0020		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or

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integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Tolerance of form and position drawing.
13. Values in inches are converted from mm and rounded to 4 decimal digits.
14. Drawing is not to scale.

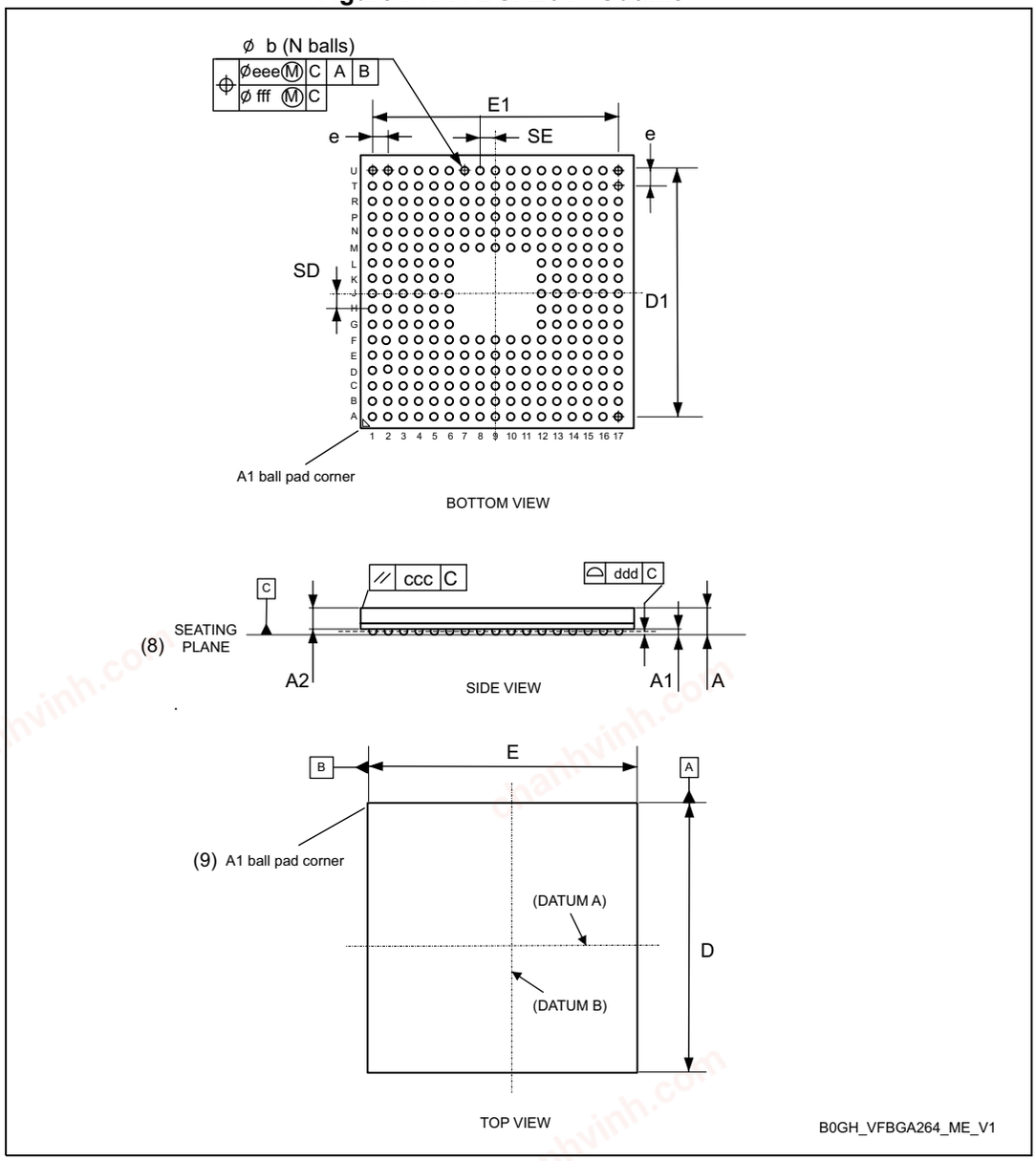
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6.7 VFBGA264 package information (B0GH)

This VFBGA is a 264-ball, 14 x 14 mm, 0.8 mm pitch, very thin fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 71. VFBGA264 - Outline(13)



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Table 122. VFBGA264 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	-	-	1.00	-	-	0.0394
A1[4]	0.21	-	-	0.0082	-	-
A2	-	0.59	-	-	0.0232	-
b[5]	0.38	0.43	0.48	0.150	0.0170	0.189
D[6]	14.00 BSC			0.5512 BSC		
D1	12.80 BSC			0.5039 BSC		
E	14.00 BSC			0.5512 BSC		
E1	12.80 BSC			0.5039 BSC		
e[9]	0.80 BSC			0.03149 BSC		
N[10]	264					
SD[11]	0.80 BSC			0.03149 BSC		
SE[11]	0.80 BSC			0.03149 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.00315		

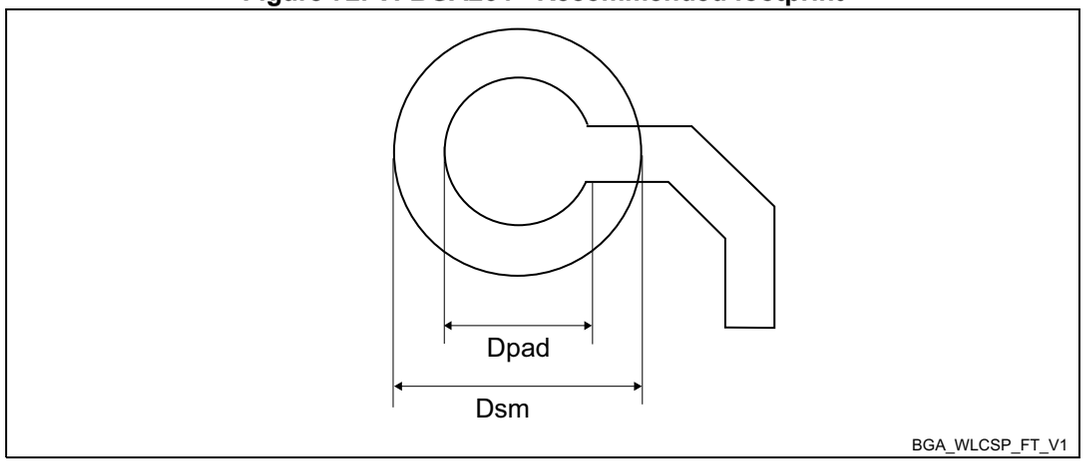
Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.

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8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

Figure 72. VFBGA264 - Recommended footprint



1. Dimensions are expressed in millimeters.

Table 123. VFBGA264 - Recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.400 mm
Dsm	0.470 mm typ.
Stencil opening	0.400 mm
Stencil thickness	0.100 mm

6.8 Package thermal characteristics

For package thermal characteristics, refer to AN5036 “*Guidelines for thermal management on STM32 applications*”, available on *www.st.com*.

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7 Ordering information

Example: STM32 N 6 5 7 X 0 H 3 Q U

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

N = neural

Device subfamily

6 = Cortex M55 core

Die

4 = Neural-ART, 4 Mbytes

5 = Neural-ART, 4 Mbytes, crypto

Line

7 = artificial intelligence

Pin/ball count

Z = 142
A = 169
I = 178
B = 198
L = 223
X = 264

Flash memory size

0 = 0-1 Kbytes

Package

H = VFBGA

Temperature range

3 = Industrial temperature range, -40 to 125 °C

Dedicated pinout

Q = Internal SMPS step-down converter

Packing

U = universal part (not for production, sampling, and tools)

For a list of available options (such as speed or package) or for further information on any aspect of this device, contact the nearest ST sales office.

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9 Revision history

Table 124. Document revision history

Date	Revision	Changes
28-Nov-2024	1	Initial release
18-Dec-2024	2	Updated *Table 2: STM32N647xx features and peripheral counts*, *Table 3: STM32N657xx features and peripheral counts*, *Table 16: Pin description*, *Table 19: Voltage characteristics*, *Table 22: General operating conditions*, *Table 30: Current consumption in Sleep mode*, *Table 48: OTP characteristics*, *Table 51: ESD absolute maximum ratings*, *Table 55: RPU/RPD characteristics*, and *Table 83: ADC accuracy*. Updated *Figure 3: Device startup with VCORE supplied directly from an external SMPS* and *Figure 4: Device startup with VCORE supplied directly from the internal SMPS*. Added *Section 6.8: Package thermal characteristics*. Minor text edits across the whole document.

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