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STM32H7S3x8 STM32H7S7x8

Arm® Cortex®-M7 32-bit 600 MHz MCU, 64 KB flash, 620 KB RAM, Ethernet, 2x USB, 2x FD-CAN, advanced graphics and security, 2x12-bit ADCs

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

Core

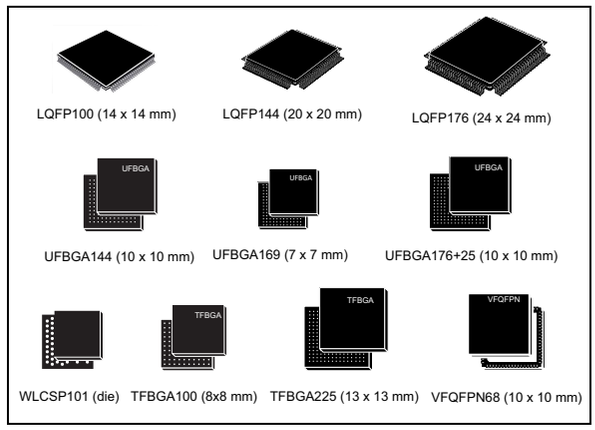
- 32-bit Arm® Cortex®-M7 CPU with MPU and DP-FPU, L1 cache: 32+32-Kbyte instruction and data cache allowing 0-wait state execution from embedded flash memory and external memories, frequency up to 600 MHz, 1284 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

- 64 Kbytes of user flash memory that can be used for user code and/or external memory configuration.
- SRAM: total 620 Kbytes (548 Kbytes with optional ECC activated) organized as follows:
  - 64+64 Kbytes minimum of instruction and data TCM RAM for critical real time instructions
  - 384 Kbytes AXI SRAM (128 Kbytes with optional remap to TCM RAM fully activated
  - 4 Kbytes of backup SRAM (available in the lowest-power modes)
- Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, FRAM, SDR/LPSDR SDRAM, NOR/NAND memories
- up to 2x Octo-SPI memory interfaces or 1 octo-SPI + 1 hexa-SPI with XiP, with support for serial PSRAM/NAND/NOR, HyperRAM™/ HyperFlash™ frame formats running at up to 200 MHz
- 2x SD/SDIO/MMC interfaces

2x DMA controllers to offload the CPU

- 2 × dual-port DMAs with FIFO and linked listed support



Security and cryptography

- PSA level 2 and SESIP level 3 certified (under certification)
- Flexible life cycle scheme with debug authentication based on certificate or password (debug reopening/regression support)
- Root of trust thanks to unique boot entry and secure hide protection area (HDP)
- Secure firmware installation / update (SFI/SFU) thanks to embedded root secure services (RSS)
- Secure data storage with hardware unique key (HUK)
- 2 AES coprocessors including one with DPA resistance
- Public key accelerator, DPA resistant
- On-the-fly encryption/decryption of serial and parallel external memories
- HASH hardware accelerator
- True random number generator, NIST SP800-90B compliant
- 96-bit unique ID
- 1 Kbyte OTP (one-time programmable)
- Active tampers

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- Hardware secure storage (dedicated secure flash area)

Graphics

- NeoChrom graphic processor (GPU2D) accelerating any angle rotation, scaling and perspective correct texture mapping
- Chrom-ART Accelerator (DMA2D) for enhanced graphic content creation
- Chrom-GRC (GFXMMU) allowing up to 20% of graphic resources optimization
- Hardware JPEG codec
- LCD-TFT controller supporting up to SVGA resolution
- Flexible memory controller FMC8/16 for parallel displays supporting up to WSVGA
- Digital camera parallel interface with pixel format conversion and cropping capabilities

Clock, reset and supply management

- 1.71 V to 3.6 V application supply and I/O
- POR, PVD and BOR
- Dedicated USB power embedding a 3.3 V internal regulator to supply the internal PHYs
- Embedded regulator LDO to supply the V_{CORE} and/or external circuitry
- High power-efficiency SMPS step-down converter regulator to directly supply V_{CORE} and/or external circuitry
- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-50 MHz HSE, 32.768 kHz LSE

Low power

- Sleep, Stop, and Standby modes
- V_{BAT} supply for RTC, 32×32-bit backup registers

Analog

- 2x12-bit ADC, up to 5 MSPS in 12-bit, up to 17 channels

Audio digital filters (ADF)

- 2 microphones /1 filter
- Voice activity detector (VAD) support

Up to 152 I/O ports with interrupt capability

Mathematical acceleration

- CORDIC for trigonometric functions acceleration

23 timers

- Sixteen 16-bit (including 5 x low power 16-bit timer available in stop mode, one graphic timer), four 32-bit timers, 2x watchdogs, 1x SysTick timer
- RTC with sub-second and hardware calendar with calibration (to be verified)

Debug mode

- Authenticated debug and flexible device lifecycle
- SWD and JTAG interfaces
- ETM with 2-Kbyte embedded trace buffer

Up to 35 communication interfaces

- 3× I2C FM+ (SMBus/PMBus™)
- 1x I^3C interface (muxed with one I^2C)
- Up to 3 USARTs/4 UARTs (ISO7816 interface, LIN, IrDA, modem control) and 2x LPUART
- 6 SPIs with 4 with muxed duplex I2S and 3x USART configured in synchronous mode (9 SPIs)
- 2x SAI (serial audio interface)
- 2× FD-CAN
- 16-bit parallel slave synchronous interface
- SPDIF-IN interface, HDMI-CEC
- Ethernet MAC interface with DMA controller
- 1 USB Type-C®/USB power delivery controller
- 1 USB OTG full-speed with embedded PHY
- 1 USB OTG high-speed with embedded PHY

ECOPACK2 compliant packages

Table 1. Device summary

Reference	Part numbers
STM32H7S3x8	STM32H7S3A8, STM32H7S3I8, STM32H7S3L8, STM32H7S3R8, STM32H7S3V8, STM32H7S3Z8
STM32H7S7x8	STM32H7S7A8, STM32H7S7I8, STM32H7S7L8, STM32H7S7Z8

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1 Introduction

This document provides information on STM32H7Sxx8 microcontrollers, such as description, functional overview, pin assignment and definition, packaging, and ordering information.

This document should be read in conjunction with the STM32H7Rx/7Sx reference manual (RM0477).

For information on the device errata with respect to the datasheet and reference manual, an errata sheet (ES0596) is available.

For information on the Arm®(a) Cortex®-M7 core, refer to the Cortex®-M7 Technical Reference Manual, available from the http://www.arm.com website.

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2 Description

STM32H7Sxx8 devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 600 MHz. The Cortex -M7 core features a floating point unit (FPU) which supports Arm double-precision (IEEE 754 compliant) and single-precision data-processing instructions and data types. The Cortex -M7 core includes 32 Kbytes of instruction cache and 32 Kbytes of data cache. STM32H7Sxx8 devices support a full set of DSP instructions and a memory protection unit (MPU) to enhance application security.

STM32H7Sxx8 devices incorporate high-speed embedded memories, 64 Kbytes of user flash memory and 128 Kbytes of system flash memory,and up to 620 Kbytes of RAM (including 128 Kbytes that can be shared between ITCM and AXI, including 64 Kbytes exclusively ITCM, including 128 Kbyte DTCM, including 64 Kbytes exclusively DTCM, including 32 Kbytes AHB and 4 Kbytes of backup RAM), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, 2x32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memory access. To improve application robustness, all memories feature error code correction (one error correction, two error detections).

The devices embed peripherals allowing mathematical/arithmetic function acceleration (CORDIC coprocessor for trigonometric functions). All the devices offer two ADCs, a low-power RTC, 4 general-purpose 32-bit timers, 7 general-purpose 16-bit timers including one PWM timer for motor control, five low-power timers, and a cryptographic acceleration cell (CRYP), Public key acceleration (PKA), a secure AES coprocessor (SAES) and a memory cipher engine (MCE) The devices support one digital filter for external sigma-delta modulators or digital microphone with voice activity detection. They also feature standard and advanced communication interfaces.

- Standard peripherals:
  - Three I^2Cs (One shared with I3C)
  - Three USARTs, four UARTs and one LPUART
  - Six SPIs, four I^2Ss in Half-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked by a dedicated internal audio PLL or by an external clock to allow synchronization (note that the five USARTs also provide SPI slave capability).
  - Two SAI serial audio interfaces
  - One SPDIFRX interface with four inputs
  - One SWPMI (Single Wire Protocol Master Interface)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces
  - A USB OTG high-speed interface with full-speed capability
  - A USB OTG full-speed interface
  - A USB Type-C/USB Power Delivery interface
  - Two FDCANs interface
  - An Ethernet interface
  - Chrom-ART Accelerator
  - HDMI-CEC

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- Advanced peripherals including:
  - A flexible memory control (FMC) interface
  - Two XSPI memory interfaces to support:
  a) one or two Octo-SPI memories
  b) one octo-SPI and one 16-bit SPI memory
  - on-the-fly encryption/decryption (MCE) for Octo-SPI/Hexa-SPI or FMC external memory. Two type of encryption are supported for best protection or best performance.
  - A camera interface for CMOS sensors
  - NeoChrom graphic processor
  - An LCD-TFT display controller
  - A camera interface for CMOS sensors

Refer to *Table 3: STM32H7Sxx8 features and peripheral counts* for the list of peripherals available on each part number.

The device security and graphics features bu product line are shown in *Table 2*.

Table 2. Security and graphics IP availability per product line

IP type	IP name	STM32H7R3 GP	STM32H7R7 GFx	STM32H7S3 GP	STM32H7S7 GFx
Graphics	Neo-Chrom (GPU2D)	N	Y	N	Y
	Chrom-Art (DMA2D)	Y			
	Chrom-GRC (GFXMMU)	Y			
	Hardware codec (JPEG)	Y			
	LCD-TFT	N	Y	N	Y
	Parallel display (FMC8/16)	Y			
Security	Life cycle support (TIL0/1/2)	Y			
	Root of trust (ST-iROT)	N	N	Y	Y
	Debug authentication	Y			
	Secure firmware install (SFI)	Y			
	Root secure service (RSS)	Y			
	HASH accelerator and PKA verification	Y			
	Crypto processor (Crypt, PKA, SAES)	N	N	Y	Y
	On-the-fly encryption/decryption (MCE)	N	N	Y	Y
	True random number generator (TRNG)	Y			

To reduce the power consumption some STM32H7Sxx8 devices include an optional step-down converter that can be used either for internal or external supply, or both.

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STM32H7Sxx8 devices operate in the –40 to +85°C[a] ambient temperature range from a 1.71 to 3.6 V power supply. The supply voltage can drop down to 1.71 V by using an external power supervisor the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Dedicated supply inputs for XSPI and USB are available to allow independent multiple voltage constraint and greater power supply choice.

A comprehensive set of power-saving modes allows the design of low-power applications.

STM32H7Sxx8 devices are offered in several packages ranging from 68 to 225 pins/balls. The set of included peripherals changes with the chosen device.

These features make STM32H7Sxx8 microcontrollers suitable for a wide range of applications:

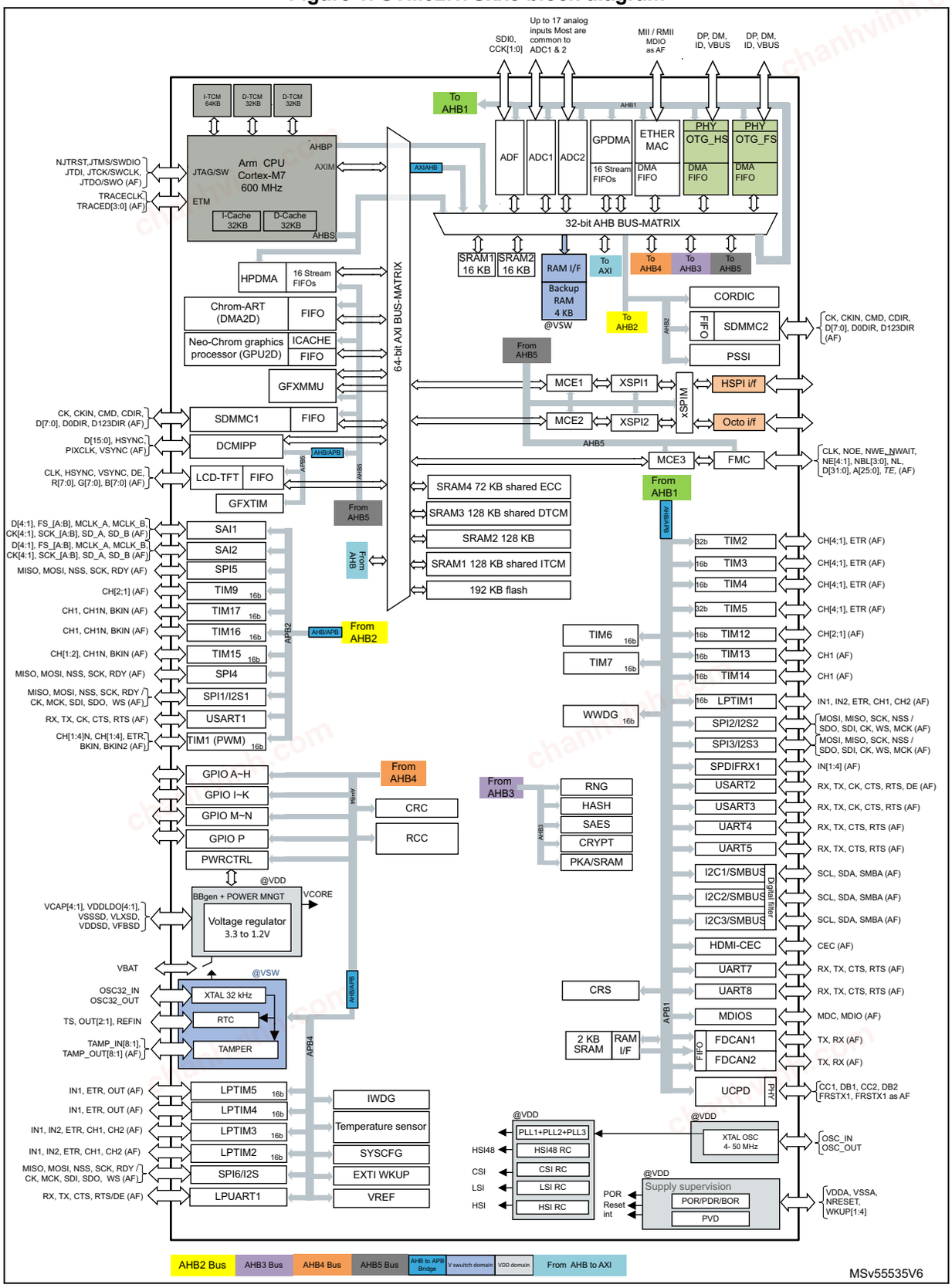
- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smart watches.

Figure 1 shows the device block diagram.

a. Under characterization

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Figure 1. STM32H7Sxx8 block diagram



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Table 3. STM32H7Sxx8 features and peripheral counts

Peripherals		STM32H7S3I8T6	STM32H7S3Z8J6	STM32H7S3A8I6	STM32H7S3I8K6	STM32H7S3L8H6	STM32H7S3L8H6H	STM32H7S3Z8T6	STM32H7S3V8T6	STM32H7S3V8H6	STM32H7S3V8Y6	STM32H7S3R8V6	STM32H7S7I8T6	STM32H7S7Z8J6	STM32H7S7A8I6	STM32H7S7I8K6	STM32H7S7L8H6	STM32H7S7L8H6H
Flash memory (Kbytes)		64																
SRAM in Kbytes	SRAM on AXI	456																
	SRAM on AHB	32																
TCM RAM in Kbytes	ITCM RAM (instruction)	64																
	DTCM RAM (data)	64																
Backup SRAM (Kbytes)		4																
FMC	Display Interface (bit)	FMC16										FMC8	FMC16					
	NOR flash memory/RAM controller	16	-	-	16(1)	32	16	-	-				16(2)	-	-	16(2)	32	16(3)
	Multiplexed I/O NOR flash memory	X(1)	-	X(1)	X(1)	X	X	X(1)	-				X(4)	X(5)	X(4)	X(4)	X	X
	16-bit NAND flash memory	X	-	X	X	X	X	-					X	-	-	X	X	X
	SDRAM controller	16	-	-	16	32	16	-					16	-	-	16	32	16
Octo-SPI /Hexa-SPI memories	-	1 / 0				2 / 0	1 / 1	1 / 0				1(6)/ 0	2 / 0	2 / 0	2 / 0	2 / 0	2 / 0	1 / 1
Timers	General-purpose 16/32 all	7/411	7/411	7/411	7/411	7/411	7/411	7/411	7/29	7/18	5/16	6/28	11	10	11	11	11	11
	Advanced-control (PWM)	1							1(7)				1					
	Basic	2											2					
	Low-power	5	5	5					5	3	3	3	4				5	
Window watchdog / independent watchdog	-	1/1																
Real-time clock (RTC)	-	1																

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Table 3. STM32H7Sxx8 features and peripheral counts (continued)

Peripherals		STM32H7S3I8T6	STM32H7S3Z8J6	STM32H7S3A8I6	STM32H7S3I8K6	STM32H7S3L8H6	STM32H7S3L8H6H	STM32H7S3Z8T6	STM32H7S3V8T6	STM32H7S3V8H6	STM32H7S3V8Y6	STM32H7S3R8V6	STM32H7S7I8T6	STM32H7S7Z8J6	STM32H7S7A8I6	STM32H7S7I8K6	STM32H7S7L8H6	STM32H7S7L8H6H
Tamper pins[8]	Passive	8	8	8	8	8	7	8	3	3	2	2	7	6	8	7	8	7
	Active	4	4	4	4	4	3	4	1	1	1	1	3	3	4	3	4	3
Random number generator	-	1																
Cryptographic accelerator	-	Yes																
Hash processor (HASH)	-	1																
On-the-fly encryption/decryption	For external Octo/Hexa-SPI memory and FMC	Yes																
Communication interfaces	SPI/I2S	6/4						6/4	5/4	5/4	5/4	4/3	6/4					
	I2C/I3C (Shared)	3/1																
	USART/UART/LPUART	3/4/1	3/4/1	3/4/1	3/4/1	3/4/1	3/4/1	3/4/1	3/3/1	2/3/1	2/3/1	3/3/1	3/4/1	3/3/1	3/4/1	3/4/1	3/4/1	3/4/1
	SAI/PDM	2/1							1/0	1/0	1/0	1/0	2/1					
	SPDIFRX	4 inputs	4 inputs	4 inputs	4 inputs	4 inputs	4 inputs	4 inputs	-	-	1 input	-	3 inputs	3 inputs	4 inputs	4 inputs	4 inputs	4 inputs
	MDIOS	1																
	SDMMC/EMMC	1 x(4 bit) + 1x 8 bit)							1 x(4 bit)			-	1x(4 bit) + 1x(8 bit)	1x(4 bit)	1x(4 bit) and 1x(8 bit)			
	FDCAN	2																
	OTG_HS / OTG_FS / UCPD	1/1/1										-/1/-	-/1/-	-/1/-	-/1/-	-/1/-	1/1/1	1/1/1
Digital camera interface/PSSI[9]	DCMIPP (bits)	16	16	16	16	16	16	16	-	-	-	-	12	8	12	12	16	16
	PSSI (bits)	16	16	16	16	16	16	16	-	-	-	-	8	8	8	8	16	16
LCD-TFT RGB24 display controller	-	0											1	1[10]	1			

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Table 3. STM32H7Sxx8 features and peripheral counts (continued)

Peripherals		STM32H7S3I8T6	STM32H7S3Z8J6	STM32H7S3A8I6	STM32H7S3I8K6	STM32H7S3L8H6	STM32H7S3L8H6H	STM32H7S3Z8T6	STM32H7S3V8T6	STM32H7S3V8H6	STM32H7S3V8Y6	STM32H7S3R8V6	STM32H7S7I8T6	STM32H7S7Z8J6	STM32H7S7A8I6	STM32H7S7I8K6	STM32H7S7L8H6	STM32H7S7L8H6H
JPEG codec	-	1																
ChromART Accelerator (DMA2D)	-	1																
Graphic memory management unit (GFXMMU)		1																
ICACHE	-	No											Yes					
HDMI CEC	-	1																
ADF number of filters	-	1							0				1					
ADCs (2 x 12bits)	Number of channels	17	17	16	18	20	20	16	12	11	11	10	17	16	17	18	20	20
ETH	-	RMII/MII	RMII	RMII	RMII/MII	RMII/MII	RMII/MII	RMII	-	-	-	-	RMII/MII	RMII	RMII	RMII/MII	RMII/MII	RMII/MII
GPIOs	-	119	94	116	122	152	150	98	67	63	65	45	118	93	117	122	152	150
	Wakeup pins	4																
Maximum CPU frequency (MHz)	-	600																
SMPS step-down converter	-	Yes						No		Yes		No	Yes					
USB internal regulator	-	Yes										No	Yes					

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Table 3. STM32H7Sxx8 features and peripheral counts (continued)

Peripherals		STM32H7S3I8T6	STM32H7S3Z8J6	STM32H7S3A8I6	STM32H7S3I8K6	STM32H7S3L8H6	STM32H7S3L8H6H	STM32H7S3Z8T6	STM32H7S3V8T6	STM32H7S3V8H6	STM32H7S3V8Y6	STM32H7S3R8V6	STM32H7S7I8T6	STM32H7S7Z8J6	STM32H7S7A8I6	STM32H7S7I8K6	STM32H7S7L8H6	STM32H7S7L8H6H
USB UCPD separate supply pad	-	Yes																
VREF+ separate pad and internal buffer	-	1																
Operating voltage	-	1.71 to 3.6 V																
Operating temperatures	-	Ambient temperature range: -40 to 85 °C																
	-	Junction temperature range: -40 to 125 °C(11)																
Packages	-	LQFP176	UFBGA 144	UFBGA 169	UFBGA 176+25	TFBGA 225	TFBGA 225	LQFP144	LQFP100	TFBGA 100	WLCSP101	VFQFPN68	LQFP176	UFBGA 144	UFBGA 169	UFBGA 176+25	TFBGA 225	TFBGA 225

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Table 3. STM32H7Sxx8 features and peripheral counts (continued)

Peripherals		STM32H7S3I8T6	STM32H7S3Z8J6	STM32H7S3A8I6	STM32H7S3I8K6	STM32H7S3L8H6	STM32H7S3L8H6H	STM32H7S3Z8T6	STM32H7S3V8T6	STM32H7S3V8H6	STM32H7S3V8Y6	STM32H7S3R8V6	STM32H7S7I8T6	STM32H7S7Z8J6	STM32H7S7A8I6	STM32H7S7I8K6	STM32H7S7L8H6	STM32H7S7L8H6H
Bootloader	-	USART, I2C, SPI, USB-DFU, FDCAN																

1. No NE4 A24/25.
2. No NBL2/3 A24/25
3. No NBL2/3
4. No A24/25
5. No A23/A24/25
6. Quad-SPI support only.
7. No BKIN2, CH4N.
8. A tamper pin can be configured either as passive or active (not both).
9. DCMIPP and PSSI cannot be used simultaneously since they share the same circuitry.
10. RGB 666
11. The junction temperature is limited to 105 °C in the VOS high-voltage range.

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3 Functional overview

3.1 Arm Cortex-M7 with FPU

The Arm Cortex-M7 with double-precision FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (32 Kbytes of instruction cache, and 32 Kbytes of data cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 1 shows the general block diagram of the STM32H7Sxx8 family.

Note: Cortex-M7 with FPU core is binary compatible with the Cortex-M4 core.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

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3.3 Memories

3.3.1 Embedded flash memory

The STM32H7Sxx8 devices embed a flash memory organized as follow:

- 64 Kbytes of user flash memory that can be used for storing programs and data.
  - The user flash contains 8 user sectors of 8 Kbytes each
  - 1 Kbyte of OTP (one-time programmable) memory containing option bytes for user configuration.
- 128 Kbytes of system flash memory from which the device can boot securely (but not available for user code).

The flash memory is organized as 137-bit flash words memory. Each word consists of:

- One flash word (4 words, 16 bytes or 128 bits)
- 9 ECC bits.

3.3.2 Secure access mode

In addition to other typical memory protection mechanism, STM32H7Sxx8 devices embed the Secure access mode, an enhanced security feature. This mode allows developing user-defined secure services by ensuring, on the one hand code and data protection and on the other hand code safe execution.

Two types of secure services are available:

- STMicroelectronics Root Secure Services:

  These services are embedded in System memory. They provide a secure solution for firmware and third-party modules installation. These services rely on cryptographic algorithms based on a device unique private key.
- User-defined secure services:

  These services are embedded in user flash memory. Examples of user secure services are proprietary user firmware update solution, secure flash integrity check or any other sensitive applications that require a high level of protection.

  The secure firmware is embedded in specific user flash memory areas configured through option bytes.

Secure services are executed just after a reset and preempt all other applications to guarantee protected and safe execution. Once executed, the corresponding code and data are no more accessible.

The above secure services are available only for Cortex-M7 core operating in Secure access mode. The other masters cannot access the option bytes involved in Secure access mode settings or the flash secured areas.

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3.3.3 Embedded SRAM

All devices feature:

- 456 Kbytes of AXI-SRAM mapped onto AXI bus matrix split into:
  - AXI-SRAM1: 128 Kbytes shared with ITCM
  - AXI-SRAM2: 128 Kbytes
  - AXI-SRAM3: 128 Kbytes shared with DTCM
  - AXI-SRAM4: 72 Kbytes shared with ECC
- 32 Kbytes of AHB-RAM mapped onto AHB bus matrix split into:
  - AHB-SRAM1: 16 Kbytes
  - AHB-SRAM2: 16 Kbytes
- 4 Kbytes of backup SRAM

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.
- RAM mapped to TCM interface (ITCM and DTCM):

  Both ITCM and DTCM RAMs are 0 wait state memories that are accessible from the CPU or the HPDMA (even in Sleep mode) through a specific AHB slave of the CPU(AHBS).
  - 64 Kbytes of ITCM-RAM (instruction RAM) which could be increased up to 192 Kbytes using the AXI-SRAM1 with a 32 Kbytes granularity.

    This RAM is connected to ITCM 64-bit interface designed for execution of critical real-times routines by the CPU.
  - 64 Kbytes of DTCM-RAM (2x 32 Kbyte DTCM-RAMs on 2x32-bit DTCM ports) which could be increased up to 192 Kbytes (2x96 Kbytes) using the AXI-SRAM3 with a 2x32 Kbytes granularity.

    The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex-M7 dual issue capability.

3.4 Boot modes

At startup, the boot memory space is selected by the BOOT0 pin and and the NVSTATE. For NVSTATE=OPEN the choice is made by the BOOT0 pin. For the NVSTATE=CLOSED the boot, from the RSS is the in the system flash:

- NVSTATE=OPEN and BOOT0 pin=0, boot from user flash at address 0x8000 0000
- NVSTATE=OPEN and BOOT0 pin=1, boot from bootloader.
- NVSTATE=CLOSED, boot from RSS in system flash memory at address 0x1FF0 0080

The boot loader is located in non-user System flash memory. It is used to reprogram the flash memory through a serial interface (USART, I2C, SPI, USB-DFU). Refer to *STM32 microcontroller system memory boot mode* application note (AN2606) for details.

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3.5 Power supply management

3.5.1 Power supply scheme

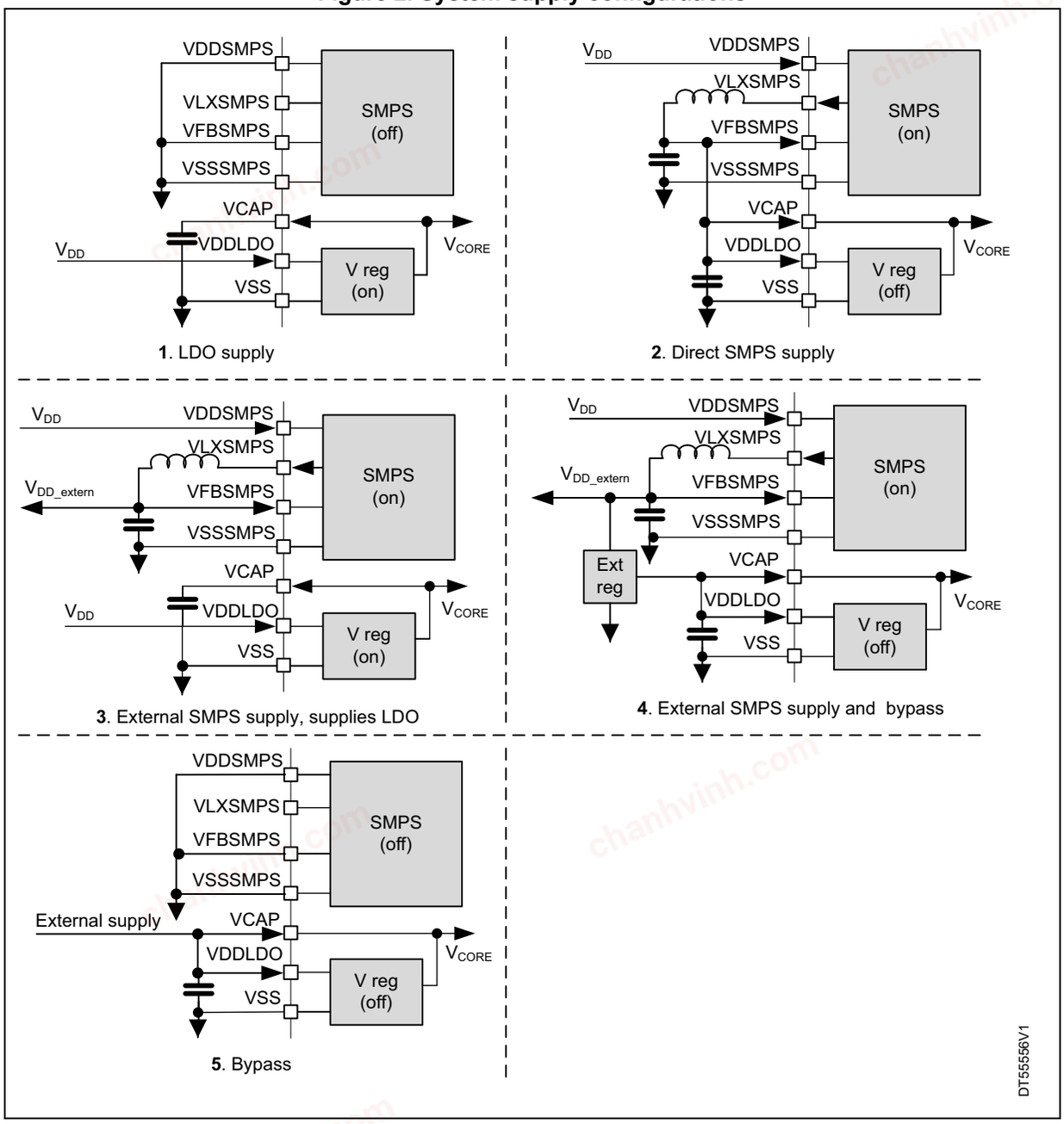
- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, provided externally through VDD pins.
- VDDLDO = 1.71 to 3.6 V: supply voltage for the internal regulator supplying V_{CORE}
- VDDA = 1.62 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL.
- $V_{DD33USB}$ and $V_{DD50USB}$: $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via the USB internal regulator. This allows supporting a V_{DD} supply different from 3.3 V.

  The USB regulator can be bypassed to supply directly $V_{DD33USB}$ if V_{DD} = 3.3 V.
- V_{BAT} = 1.2 to 3.6 V: power supply for the V_{SW} domain when V_{DD} is not present.
- V_{CAP}: V_{CORE} supply, which value depends on voltage scaling (SVOS low, SVOS high, VOS low, VOS high). It is configured through the VOS bits in the PWR_CSR4 and PWR_CR1 registers.
- V_{DDSMPS} = 1.71 to 3.6 V: step-down converter power supply
- V_{LXSMPS} = V_{CORE} or 1.8 V: external regulated step-down converter output
- V_{FBSMPS} = V_{CORE} or 1.8 V: external step-down converter feedback voltage sense input

Figure 2 gives the different power supply configurations.

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Figure 2. System supply configurations



Note: The features available on the device depend on the package refer to Table 3: STM32H7Sxx8 features and peripheral counts.

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3.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in reset mode when V_{DD} is below this threshold,
- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.
- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.
- Programmable voltage detector (PVD)

  The PVD monitors the V_{DD} power supply by comparing it with a threshold selected from a set of predefined values.

  It can also monitor the voltage level of the PVD_IN pin by comparing it with an internal V_{REFINT} voltage reference level.
- Analog voltage detector (AVD)

  The AVD monitors the V_{DDA} power supply by comparing it with a threshold selected from a set of predefined values.
- V_{BAT} threshold

  The V_{BAT} battery voltage level can be monitored by comparing it with two thresholds levels.
- Temperature threshold

  A dedicated temperature sensor monitors the junction temperature and compare it with two threshold levels.

3.5.3 Voltage regulator

Voltage regulator output can be adjusted according to application needs through four power supply levels:

- Run mode (VOS high and VOS low)
  - Scale HIGH : high performance
  - Scale LOW: optimized performance and low-power consumption
- Stop mode (SVOS high and SVOS low)
  - Scale HIGH: peripheral with wakeup from stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  - Scale LOW where the peripheral with wakeup from Stop mode is disabled

    The peripheral functionality is disabled but wakeup from Stop mode is possible through GPIO or asynchronous interrupt.

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3.5.4 SMPS step-down converter

The built-in SMPS step-down converter is a highly power-efficient DC/DC non-linear switching regulator that provides lower power consumption than a conventional voltage regulator (LDO).

The step-down converter can be used to:

- Directly supply the V_{CORE} domain
  - the SMPS step-down converter operating modes follow the device system operating modes (Run, Stop, Standby).
  - the SMPS step-down converter output voltage are set according to the selected VOS and SVOS bits (voltage scaling)
- Provide an external supply
  - The SMPS step-down converter is forced to High-performance mode
  - The SMPS step-down converter output equals 1.8 V according to the selected step-down level

The 1.8 V SMPS step-down converter output voltage imposes a minimum V_{DDSMPS} supply of 2.3 V to 3.6 V. It defines indirectly the minimum V_{DD} supply and I/O level.

3.6 Low-power modes

There are several ways to reduce power consumption on STM32H7Sxx8:

- Decrease dynamic power consumption by slowing down the system clocks even in Run mode and individually clock gating the peripherals that are not used.
- Save power consumption when the CPU is idle, by selecting among the available low-power mode according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wakeup sources. The low-power modes are:
  - Sleep (CPU clock stopped and still in RUN mode)
  - Stop (System clock stopped)
  - Standby (System powered down)

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Sleep and Stop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex-M7 core is set after returning from an interrupt service routine.

The CPU domain can enter low-power mode (Stop) when the processor, its subsystem and the peripherals allocated in the domain enter low-power mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared.

Table 4. Operating mode summary

System	System oscillator	System clock	Peripheral clock	CPU clock	Voltage regulator
Run	ON	ON	ON	ON	ON (VOS)
Sleep			ON/OFF	OFF	
Stop	ON/OFF	OFF			ON (SVOS)
Standby	OFF		OFF		OFF

Some GPIO pins can be used to monitor CPU and domain power states:

Table 5. Overview of low-power mode monitoring pins

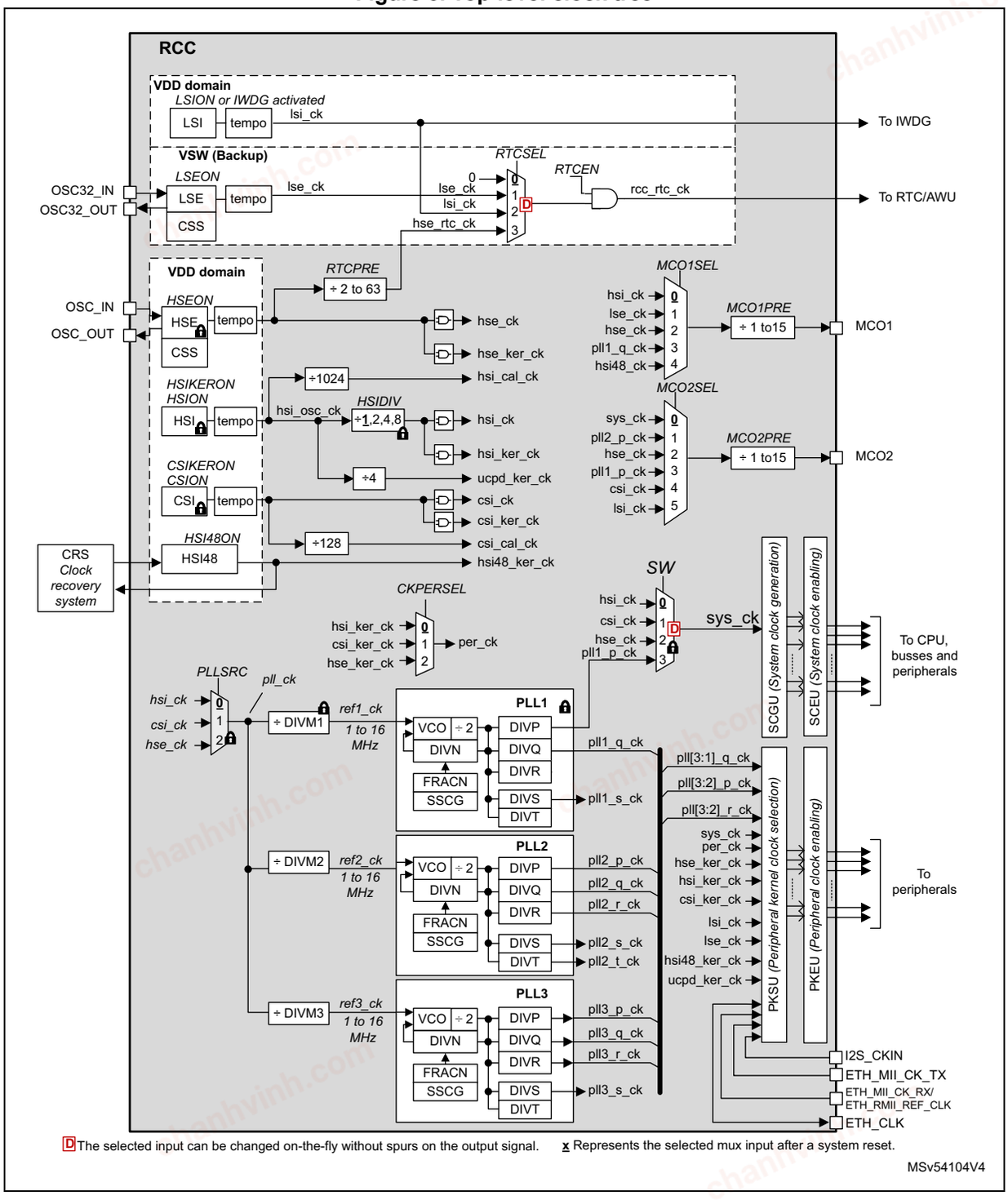
Power state monitoring pins	Description
PWR_CSLEEP	CPU clock OFF
PWR_CSTOP	CPU domain in low-power mode

3.7 Reset and clock controller (RCC)

The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baud rate.

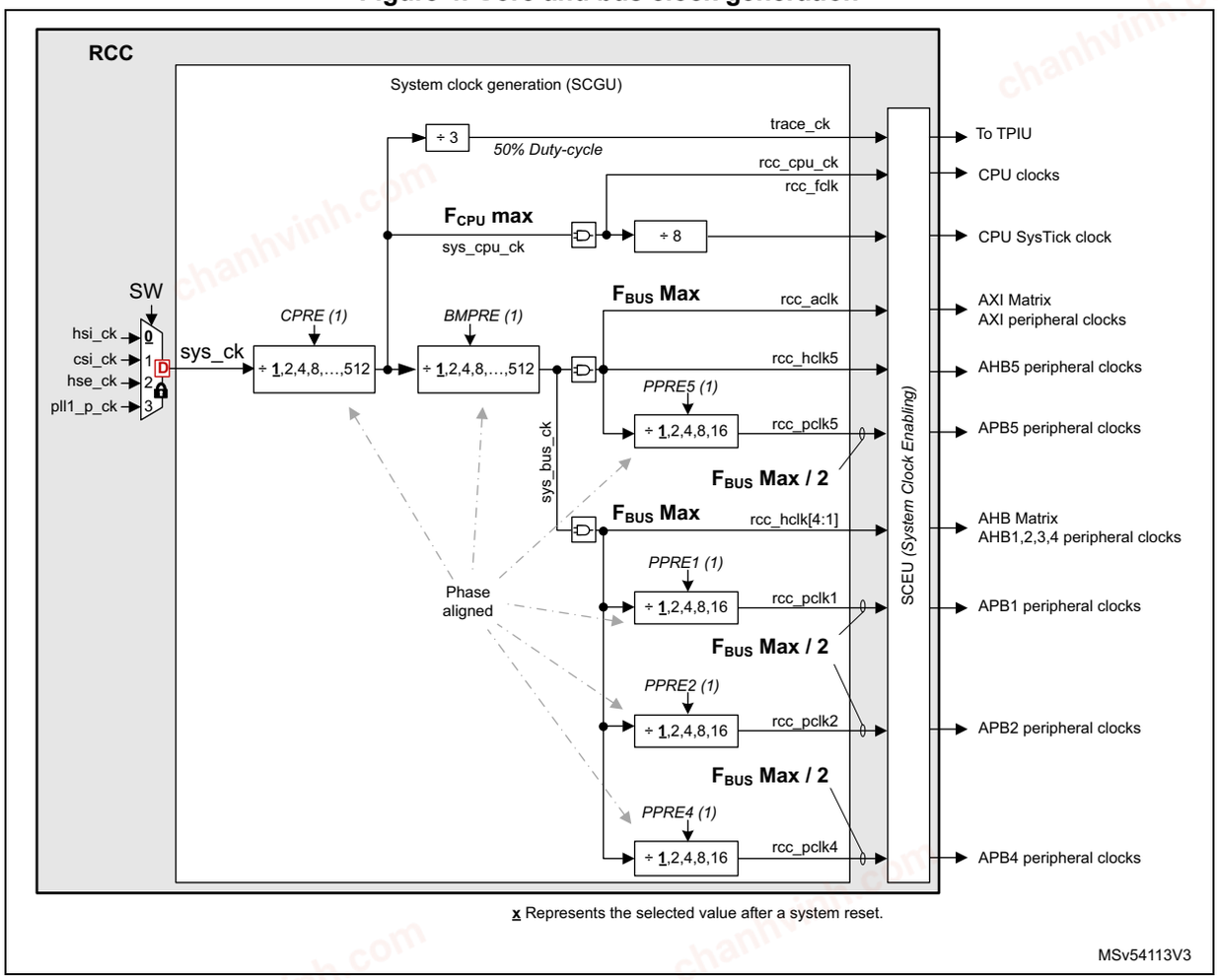
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Figure 3. Top-level clock tree



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Figure 4. Core and bus clock generation



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Table 6. Peripheral clock distribution summary

Peripherals	Clock types	Clock sources	Kernel clock MUX		Max Kernel clock freq. [MHz] (1)	Type (2)(3)
			Pos.	Control field		
ADF	Kernel	hclk1	**0**(4)	ADF1SEL	F_{MAX} / 2	A
		pll2_p_ck	1			
		pll3_p_ck	2			
		I2S_CKIN	3			
		csi_ker_ck	4			
		hsi_ker_ck	5			
	Bus	hclk1	-	-	F_{MAX} / 2	-
ADC12	Kernel	pll2_p_ck	**0**(4)	ADCSEL	125	A
		pll3_r_ck	1			
		per_ck	2			
	Bus	hclk1	-	-	F_{MAX} / 2	-
CORDIC	Bus	hclk2	-	-	F_{MAX} / 2	-
CRC	Bus	hclk4	-	-	F_{MAX} / 2	-
CRS	Bus	pclk1	-	-	F_{MAX} / 4	-
CRYP	Bus	hclk3	-	-	F_{MAX} / 2	-
DBG	Bus	sys_bus_ck	-	-	F_{MAX} / 2	-
	kernel	sys_cpu_ck/3	-	-	F_{MAX} / 3	-
DB_OCSPI1. DB_OCSPI2	Bus	hclk5	-	-	F_{MAX} / 2	-
DB_SDMMC1	Bus	hclk5	-	-	F_{MAX} / 2	-
DB_SDMMC2	Bus	hclk2	-	-	F_{MAX} / 2	-
DCMIPP	Bus	aclk	-	-	F_{MAX} / 2	-
		pclk5			F_{MAX} / 4	
GPDMA1	Bus	hclk1	-	-	F_{MAX} / 2	-
HPDMA1	Bus	hclk5	-	-	F_{MAX} / 2	-
		aclk				
DMA2D	Bus	hclk5	-	-	F_{MAX} / 2	-
		aclk				

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Table 6. Peripheral clock distribution summary (continued)

Peripherals	Clock types	Clock sources	Kernel clock MUX		Max Kernel clock freq. [MHz] (1)	Type (2)(3)
			Pos.	Control field		
ETH1	Kernel	ETH_MII_TX_CLK	-	-	25	A
		ETH_MII_TX_CLK/. ETH_RMII_REF_CLK	**0**(4)	ETH1REFCKSEL	25	A
		hse_ker_ck	1			
		eth_clk_fb	2			
		hse_ker_ck	**0**(4)	ETH1PHYCKSEL	50	A
		pll3_s_ck	1			
		clk_ptp_ref_i			F_{MAX} / 2	-
	Bus	hclk1	-	-	F_{MAX} / 2	-
EXTI	Bus	pclk4	-	-	F_{MAX} / 4	-
FLASH	Bus	hclk5	-	-	F_{MAX} / 2	-
FDCAN	Kernel	hse_ker_ck	**0**(4)	FDCANSEL	125	A
		pll1_q_ck	1			
		pll2_p_ck	2			
	Bus	pclk1	-	-	F_{MAX} / 4	-
FMC	Kernel	hclk5	**0**(4)	FMCSEL	F_{MAX} / 2	A
		pll1_q_ck	1			
		pll2_r_ck	2			
		hsi_ker_ck	3			
	Bus	hclk5	-	-	F_{MAX} / 2	-
		aclk				
GPIOA-H. GPIOM-P	Bus	hclk4	-	-	F_{MAX} / 2	-
GPU2D	Bus	hclk5	-	-	F_{MAX} / 2	-
		aclk				
GFXMMU	Bus	hclk5	-	-	F_{MAX} / 2	-
		aclk				
GFXTIM	Bus	pclk5	-	-	F_{MAX} / 4	-
HASH	Bus	hclk3	-	-	F_{MAX} / 2	-
HDMI-CEC	Kernel	lse_ck	**0**(4)	CECSEL	1	-
		lsi_ck	1			
		csi_ker_ck/122	2			
	Bus	pclk1	-	-	F_{MAX} / 4	

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Table 6. Peripheral clock distribution summary (continued)

Peripherals	Clock types	Clock sources	Kernel clock MUX		Max Kernel clock freq. [MHz] (1)	Type (2)(3)
			Pos.	Control field		
I2C2, I2C3	Kernel	pclk1	**0**(4)	I2C23SEL	F_{MAX} / 4	A
		pll3_r_ck	1			
		hsi_ker_ck	2			
		csi_ker_ck	3			
	Bus	pclk1	-	-	F_{MAX} / 4	-
I2C1/I3C1	Kernel	pclk1	**0**(4)	I2C1_I3C1SEL	F_{MAX} / 4	A
		pll3_r_ck	1			
		hsi_ker_ck	2			
		csi_ker_ck	3			
	Bus	pclk1	-	-	F_{MAX} / 4	-
XSPIM	Bus	hclk5	-	-	F_{MAX} / 2	-
IWDG	Kernel	lsi_ck	-	-	1	A
	Bus	pclk4	-	-	F_{MAX} / 4	-
JPEG	Bus	hclk5	-	-	F_{MAX} / 2	-
LPTIM1	Kernel	pclk1	**0**(4)	LPTIM1SEL	F_{MAX} / 4	A
		pll2_p_ck	1			
		pll3_r_ck	2			
		lse_ck	3			
		lsi_ck	4			
		per_ck	5			
	Bus	pclk1	-	-	F_{MAX} / 4	-
LPTIM2, LPTIM3	Kernel	pclk4	**0**(4)	LPTIM23SEL	F_{MAX} / 4	A
		pll2_p_ck	1			
		pll3_r_ck	2			
		lse_ck	3			
		lsi_ck	4			
		per_ck	5			
	Bus	pclk4	-	-	F_{MAX} / 4	-

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Table 6. Peripheral clock distribution summary (continued)

Peripherals	Clock types	Clock sources	Kernel clock MUX		Max Kernel clock freq. [MHz] (1)	Type (2)(3)
			Pos.	Control field		
LPTIM4, LPTIM5	Kernel	pclk4	**0**(4)	LPTIM45SEL	F_{MAX} / 4	A
		pll2_p_ck	1			
		pll3_r_ck	2			
		lse_ck	3			
		lsi_ck	4			
		per_ck	5			
	Bus	pclk4	-	-	F_{MAX} / 4	-
LPUART1	Kernel	pclk4	**0**(4)	LPUART1SEL	F_{MAX} / 4	A
		pll2_q_ck	1			
		pll3_q_ck	2			
		hsi_ker_ck	3			
		csi_ker_ck	4			
		lse_ck	5			
	Bus	pclk4	-	-	F_{MAX} / 4	-
LTDC	Kernel	pll3_r_ck	-	-	90	A
	Bus	pclk5	-		F_{MAX} / 4	-
		aclk	-		F_{MAX} / 2	
MCE1, MCE2, MCE3	Bus	aclk	-	-	F_{MAX} / 2	-
		hclk5	-			
MDIO	Bus	pclk1	-	-	F_{MAX} / 4	-
PKA	Bus	hclk3	-	-	F_{MAX} / 2	-
PWR	Bus	hclk4	-	-	F_{MAX} / 2	-
PSSI	Kernel	pll3_r_ck	**0**(4)	PSSISEL	100	-
		per_ck	1			-
	Bus	hclk2	-	-	F_{MAX} / 2	-
XSPI1	Kernel	hclk5	**0**(4)	XSPI1SEL	F_{MAX} / 2	A
		pll2_s_ck	1			
		pll2_t_ck	2			
	Bus	hclk5	-	-	F_{MAX} / 2	-
		aclk				

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Table 6. Peripheral clock distribution summary (continued)

Peripherals	Clock types	Clock sources	Kernel clock MUX		Max Kernel clock freq. [MHz] (1)	Type (2)(3)
			Pos.	Control field		
XSPI2	Kernel	hclk5	**0**(4)	XSPI2SEL	F_{MAX} / 2	A
		pll2_s_ck	1			
		pll2_t_ck	2			
	Bus	hclk5	-	-	F_{MAX} / 2	-
		aclk				
OTGFS	Kernel	hsi48_ker_ck	**0**(4)	OTGFSSEL	50	A
		pll3_q_ck	1			
		hse_ker_ck	2			
		clk48mohci	3			
	Bus	hclk1	-	-	F_{MAX} / 2	-
OTGHS	Kernel	phy60m_ck	-	-	60	A
	Bus	hclk1	-	-	F_{MAX} / 2	-
RCC	Bus	hclk4	-	-	F_{MAX} / 2	-
RNG	Kernel	hsi48_ker_ck	-	-	48	A
	Bus	hclk3	-	-	F_{MAX} / 2	-
RTC/AWU(5)	Kernel	no clock	**0**(4)	RTCSEL	4	A
		lse_ck	1			
		lsi_ck	2			
		hse_ker_ck / (RTCDIV+1)	3			
	Bus	pclk4	-	-	F_{MAX} / 4	-
SAES	Kernel	hclk3	-	-	F_{MAX} / 2	A
	Bus	hclk3	-	-	F_{MAX} / 2	-
SAI1	Kernel	pll1_q_ck	**0**(4)	SAI1SEL	133	A
		pll2_p_ck	1			
		pll3_p_ck	2			
		I2S_CKIN	3			
		per_ck	4			
	Bus	pclk2	-	-	F_{MAX} / 4	-

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Table 6. Peripheral clock distribution summary (continued)

Peripherals	Clock types	Clock sources	Kernel clock MUX		Max Kernel clock freq. [MHz] (1)	Type (2)(3)
			Pos.	Control field		
SAI2	Kernel	pll1_q_ck	**0**(4)	SAI2SEL	133	A
		pll2_p_ck	1			
		pll3_p_ck	2			
		I2S_CKIN	3			
		per_ck	4			
		spdif_symb_ck	5			
	Bus	pclk2	-	-	F_{MAX} / 4	-
SBS	Bus	pclk4	-	-	F_{MAX} / 4	-
SDMMC1	Kernel	pll2_s_ck	**0**(4)	SDMMC12SEL	200	A
		pll2_t_ck	1			
	Bus	hclk5	-	-	F_{MAX} / 2	-
SDMMC2	Kernel	pll2_s_ck	**0**(4)	SDMMC12SEL	200	A
		pll2_t_ck	1			
	Bus	hclk2	-	-	F_{MAX} / 2	-
SPDIFRX	Kernel	pll1_q_ck	**0**(4)	SPDIFRXSEL	200	A
		pll2_r_ck	1			
		pll3_r_ck	2			
		hsi_ker_ck	3			
	Bus	pclk1	-	-	F_{MAX} / 4	-
SPI/I2S6	Kernel	pclk4	**0**(4)	SPI6SEL	200	A
		pll2_q_ck	1			
		pll3_q_ck	2			
		hsi_ker_ck	3			
		csi_ker_ck	4			
		hse_ker_ck	5			
	Bus	pclk4	-	-	F_{MAX} / 4	-
SPI/I2S1	Kernel	pll1_q_ck	**0**(4)	SPI1SEL	130	A
		pll2_p_ck	1			
		pll3_p_ck	2			
		I2S_CKIN	3			
		per_ck	4			
	Bus	pclk2	-	-	F_{MAX} / 4	-

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Table 6. Peripheral clock distribution summary (continued)

Peripherals	Clock types	Clock sources	Kernel clock MUX		Max Kernel clock freq. [MHz] (1)	Type (2)(3)
			Pos.	Control field		
SPI4, SPI5	Kernel	pclk2	**0**(4)	SPI45SEL	200	A
		pll2_q_ck	1			
		pll3_q_ck	2			
		hsi_ker_ck	3			
		csi_ker_ck	4			
		hse_ker_ck	5			
	Bus	pclk2	-	-	F_{MAX} / 4	-
SPI/I2S3, SPI/I2S2	Kernel	pll1_q_ck	**0**(4)	SPI23SEL	200	A
		pll2_p_ck	1			
		pll3_p_ck	2			
		I2S_CKIN	3			
		per_ck	4			
	Bus	pclk1	-	-	F_{MAX} / 4	-
TAMPER	Kernel	no clock	**0**(4)	RTCSEL	4	A
		lse_ck	1			
		lsi_ck	2			
		hse_ker_ck/ (RTCDIV+1)	3			
	Bus	pclk4	-	-	F_{MAX} / 4	-
DTS	Kernel	lse_ck	-	-	10	A
	Bus	pclk4	-	-	F_{MAX} / 4	-
TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, TIM12, TIM13, TIM14	Kernel	timg1_ck	-	-	F_{MAX} / 2	S
	Bus	pclk1	-	-	F_{MAX} / 4	-
TIM1, TIM9, TIM15, TIM16, TIM17,	Kernel	timg2_ck	-	-	F_{MAX} / 2	S
	Bus	pclk2	-	-	F_{MAX} / 4	-
USART1,	Kernel	pclk2	**0**(4)	USART1SEL	F_{MAX} / 4	A
		pll2_q_ck	1			
		pll3_q_ck	2			
		hsi_ker_ck	3			
		csi_ker_ck	4			
		lse_ck	5			
	Bus	pclk2	-	-	F_{MAX} / 4	-

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Table 6. Peripheral clock distribution summary (continued)

Peripherals	Clock types	Clock sources	Kernel clock MUX		Max Kernel clock freq. [MHz] (1)	Type (2)(3)
			Pos.	Control field		
USART2, USART3, UART4, UART5, UART7, UART8	Kernel	pclk1	**0**(4)	UART234578SEL	F_{MAX} / 4	A
		pll2_q_ck	1			
		pll3_q_ck	2			
		hsi_ker_ck	3			
		csi_ker_ck	4			
		lse_ck	5			
	Bus	pclk1	-	-	F_{MAX} / 4	-
UCPD	Kernel	ucpd_ker_ck	-	-	25	A
	Bus	pclk1	-	-	F_{MAX} / 4	-
USBPHYC	Kernel	hse_ker_ck	**0**(4)	USBPHYCSEL	32	A
		hse_ker_ck / 2	1			
		pll3_q_ck	2			
VREFBUF	Bus	pclk4	-	-	F_{MAX} / 4	-
WWDG1	Bus	pclk1	-	-	F_{MAX} / 4	-

1. F_{MAX} value depends on the device reference and can be found on the datasheet of the product.
2. 'A' Means that the kernel clock is asynchronous with respect to bus interface clock.
3. 'S' Means that the kernel clock is synchronous with respect to bus interface clock.
4. Reset value
5. The RTC switch is in the VSW voltage domain

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3.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock (1% accuracy)
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - 4-50 MHz HSE clock
  - 32.768 kHz LSE clock

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

A high precision can be achieved for the 48 MHz clock by using the embedded clock recovery system (CRS). It uses the USB SOF signal, the LSE or an external signal (SYNC) to fine tune the oscillator frequency on-the- fly.

3.7.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC, the power controller status registers and part of the SBS, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Window watchdog
- Independent watchdog
- Software reset
- Low-power mode security reset
- Exit from Standby
- An option byte reload request from the flash interface (obl_rst)

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3.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) as analog, or as peripheral alternate functions. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs are in Analog mode to reduce power consumption (refer to GPIOs register reset values in the device reference manual).

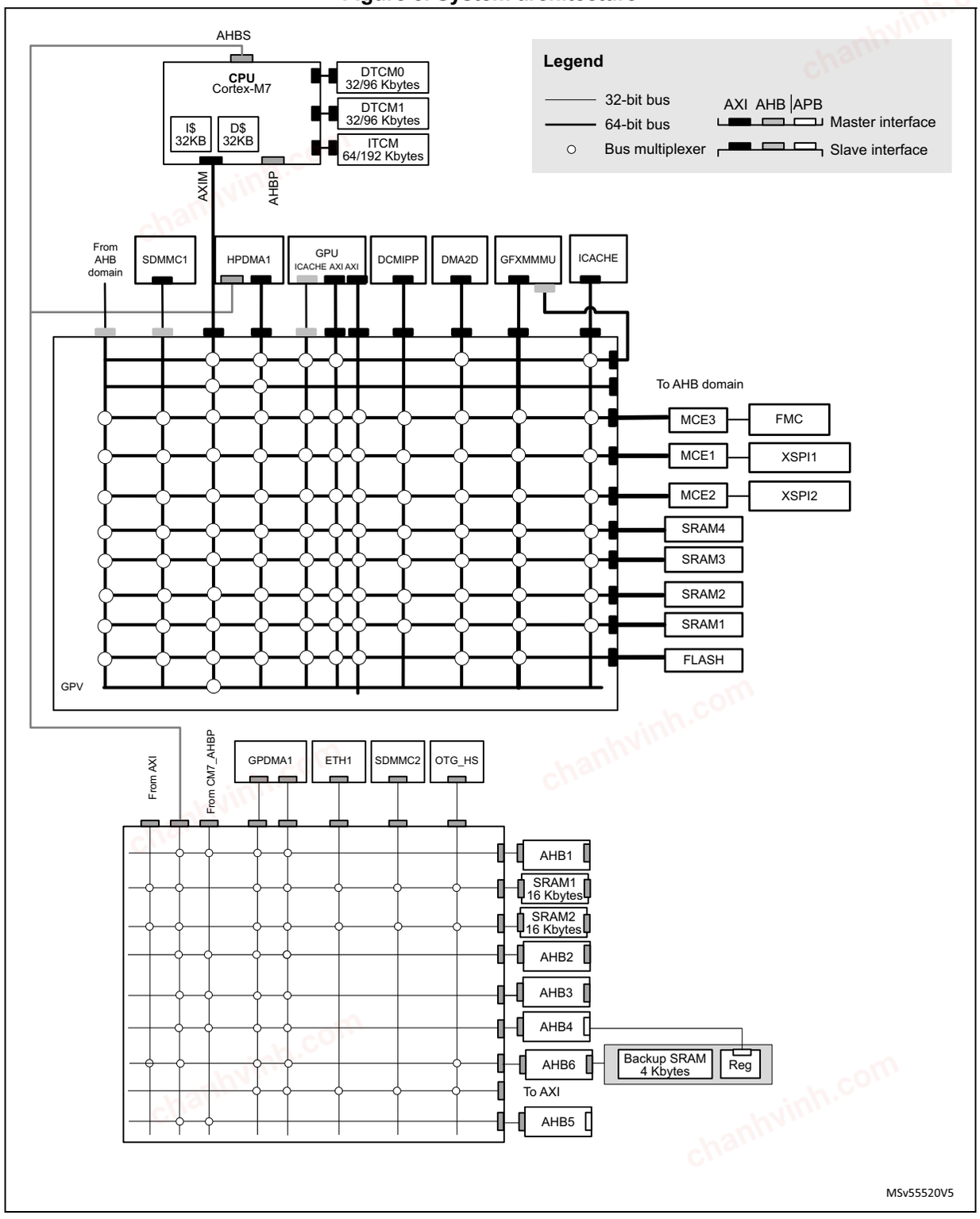
The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, an AHB bus matrices and bus bridges that allow interconnecting bus masters with bus slaves (see *Figure 5*).

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Figure 5. System architecture



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3.10 General purpose / high-performance direct memory access controller (GPDMA/HPDMA)

The general purpose direct memory access (GPDMA) controller and the high-performance direct memory access (HPDMA) controller are both bus master and system peripherals.

The GPDMA and HPDMA are used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

Their main features are:

- Dual bidirectional AXI master for HPDMA and AHB master for GPDMA
- Memory-mapped data transfers from a source to a destination:
  - peripheral-to-memory
  - memory-to-peripheral
  - memory-to-memory
  - peripheral-to-peripheral
- Transfers arbitration based on a four-grade programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)
- Per channel event generation, on any of the following events: transfer complete, half transfer complete, data transfer error, user setting error, link transfer error, completed suspension, or trigger overrun
- Per channel interrupt generation, with separately programmed interrupt enable per event
- 16 concurrent DMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intra-channel DMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intra-channel and inter-channel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - 2D source and destination addressing: programmable signed address offsets between successive burst transfers (non-contiguous addressing within a block,

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combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level)
  - Support for scatter-gather (multi-buffer transfers), data interleaving and deinterleaving via 2D addressing
  - Programmable DMA request and trigger selection
  - Programmable DMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting including FIFO level and event flags
- Privileged/unprivileged support:
  - Support for privileged and unprivileged GPDMA transfers, independently at a channel level
  - Privileged-aware AHB slave port.

3.11 Chrom-ART Accelerator (DMA2D)

The Chrom-Art Accelerator (DMA2D) is a graphical accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables. The DMA2D also supports block based YCbCr to handle JPEG decoder output.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.12 NeoChrom graphic processor (GPU2D)

The GPU2D is a dedicated graphics processing unit accelerating numerous 2.5D graphics applications such as graphical user interface (GUI), menu display or animations.

It works together with an optimized software stack designed for state of the art graphic rendering.

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Main features

- Multi-threaded fragment (pixel) processing core with a VLIW (very-long instruction word) instruction set
- Fixed point functional units
- Command list based DMAs to minimize CPU overhead
- Two 64-bit AXI master interfaces for texture, command list and framebuffer access
- Dedicated 64-bit AXI master interface for command list
- 32-bit AHB slave interface for register bank access
- Up to 4 general-purpose flags for system-level synchronization
- Texture decompression unit with TSC™4 and TSC™6/TSC™6a support
- 16 Kbyte texture cache (ICACHE)

2D drawing features

- Pixel/line drawing
- Filled rectangles
- Triangles, quadrilateral drawing
- Anti-aliasing 8xMSAA (multi-sample anti-aliasing)

Image transformations

- 3D perspective correct projections
- Texture mapping with bilinear filtering or point sampling

Blit support

- Rotation, mirroring, stretching (independently on x and y axis)
- Source and/or destination color keying
- Pixel format conversions

Text rendering support

- A1, A2, A4, and A8 bitmap anti-aliased
- Subsampled anti-aliased

Main color format

- RGB, grayscale
- 32, 24, 16 and 8 bits with/without alpha

Full alpha blending with hardware blender

- Programmable blending modes
- Source/destination color keying

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3.13 Chrom-GRC (GFXMMU)

The Chrom-GRC is a graphical oriented memory management unit aimed at optimizing memory usage according to the display shape.

GFXMMU main features:

- Fully programmable display shape to physically store only the visible pixel
- Up to 4 virtual buffers
- Each virtual buffer have 3072 or 4096 bytes per line and 1024 lines
- Each virtual buffer can be physically mapped to any system memory
- Packing and unpacking operation to store 32-bit pixel data into 24-bit packed
- Interrupt in case of buffer overflow (1 per buffer)
- Interrupt in case of memory transfer error

3.14 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and handle up to 140 maskable interrupt channels plus the 16 interrupt lines of the Cortex-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.15 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processor from Stop mode.

The EXTI handles up to 61 independent event/interrupt lines split as 27 configurable events and 34 direct events.

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

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3.16 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.17 CORDIC co-processor (CORDIC)

The CORDIC co-processor provides hardware acceleration of certain mathematical functions, notably trigonometric, commonly used in motor control, metering, signal processing and many other applications. It speeds up the calculation of these functions compared to a software implementation, allowing a lower operating frequency, or freeing up processor cycles in order to perform other tasks.

The CORDIC main features are:

- 24-bit CORDIC rotation engine
- Circular and hyperbolic modes
- Rotation and vectoring modes
- Functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural logarithm
- Programmable precision
- Low-latency AHB slave interface
- Results can be read as soon as ready without polling or interrupt
- DMA read and write channels
- Multiple register read/write by DMA

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3.18 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (4 memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by 2.

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3.19 Quad/Octo/Hexa-SPI memory interface

3.19.1 XSPI I/O manager (XSPIM)

The XSPI I/O manager is a low-level interface that enables an efficient XSPI pin assignment with a full I/O matrix (before alternate function map) and multiplex of single/dual/quad/octal/16-bit SPI interfaces over the same bus. up to 2 interfaces are available where one could be up to 16bits depending on the package.

it can support up to two single/dual/quad/octal/16-bit SPI interfaces (depending on the package option).

Table 7. XSPIM implementation

XSPIM features	i/f avaibility
Supports up to two single/dual/quad interfaces	Both
Fully I/O multiplexing capability	Both
Supports time-multiplexed mode	Both
Supports high-speed interface	Both
Chip select selection if XSPI provides dual chip select	Package dependent
Supports 16-bit data interface and dual-octal mode	Only a single i/f, package dependent

3.19.2 Extended-SPI interface (XSPI)

The XSPI supports most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, HyperRAM™ and HyperFlash™ memories, with the following functional modes:

- indirect mode: all the operations are performed using the XSPI registers to preset commands, addresses, data and transfer parameters.
- automatic status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting.
- memory-mapped mode: the external memory is memory mapped and it is seen by the system as if it was an internal memory, supporting both read and write operations.

The XSPI supports the following protocols with associated frame formats:

- the regular-command frame format with the command, address, alternate byte, dummy cycles and data phase
- the HyperBus™ frame format

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Table 8. XSPI implementation

Feature	XSPI1/2
HyperBus standard compliant	X
Xccela standard compliant	X
XSPI (JDES251C) standard compliant	X
AMBA® AXI compliant data interface	X
Asynchronous AHB clock versus kernel clock	X
Functional modes: indirect, automatic status-polling, and memory-mapped	X
Dual chip select support (NCS1 and NCS2)	X
Read and write support in memory-mapped mode	X
Dual-quad configuration	X
Dual-octal configuration	X
SDR (single-data rate) and DTR (double-transfer rate)	X
Data strobe (DS, DQS)	X
Fully programmable opcode	X
Fully programmable frame format	X
Integrated FIFO for reception and transmission	X
8, 16, and 32-bit data accesses	X
Interrupt on FIFO threshold, timeout, operation complete, and access error	X
Compliant with dual-XSPI arbiter (communication regulation)	X
Extended CSHT timeout	X
Memory-mapped write	X
Refresh counter	X
High-speed interface	X
GP/HPDMA interface	X
Prefetch disable	-
Prefetch hardware software	-

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3.20 Analog-to-digital converters (ADCs)

The STM32H7Sxx8 devices embed two analog-to-digital converters, which resolution can be configured to 12, 10, 8, or 6 bits. Each ADC shares up to 19 channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, thus allowing to automatically transfer ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6 TIM9, TIM12, and TIM15.

3.21 Analog temperature sensor

The temperature sensor generates a voltage V_{SENSE} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_INP16 input channel that is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity, but it must be calibrated to obtain a good accuracy of temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data is stored by STMicroelectronics in the system memory area, and is accessible in read-only mode.

Table 9. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	Temperature sensor 12-bit raw data acquired by ADC1 at 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.3 V (± 10 mV)	0x08FF F814 - 0x08FF F815
TS_CAL2	Temperature sensor 12-bit raw data acquired by ADC1 at 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.3 V (± 10 mV)	0x08FF F818 - 0x08FF F819

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3.22 Digital temperature sensor (DTS)

The STM32H7Sxx8 embeds a sensor that converts the temperature into a square wave which frequency is proportional to the temperature. The PCLK or the LSE clock can be used as reference clock for the measurements. A formula given in the product reference manual (RM0477) allows to calculate the temperature according to the measured frequency stored in the DTS_DR register.

3.23 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers and the backup SRAM.

To optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by V_{DD}, in which case, the V_{DD} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC, the backup registers and the backup SRAM.

The devices embed an internal V_{BAT} battery charging circuitry that can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

3.24 Voltage reference buffer (VREFBUF)

The built-in voltage reference buffer can be used as voltage reference for ADCs , as well as voltage reference for external components through the VREF+ pin.

Three different voltages are supported (refer to the reference manual for details).

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3.25 Audio digital filter (ADF)

The audio digital filter (ADF) is a high-performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators. The table below lists the set of features implemented into the ADF.

Table 10. ADF features (1)

Mode or feature	ADF1
Number of filters (DFLTx) and serial interfaces (SITFx)	1
ADF_CKI0 connected to pins	-
Sound activity detection (SAD)	X
RXFIFO depth (number of 24-bit words)	4
ADC connected to ADCITF1	ADC1
ADC connected to ADCITF2	ADC2
Motor dedicated features (SCD, OLD, OEC, INT, snapshot, break)	-
Main path with CIC4, CIC5	X
Main path with CIC1,2, 3 or FastSinc	-
RSFLT, HPF, SAT, SCALE, DLY, Discard functions	X
Autonomous in Stop modes	-

1. ‘X’ = supported, ‘-’ = not supported.

3.26 Digital camera interface (DCMIPP)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 16-bit parallel interface, to receive video data. The camera interface can achieve a data transfer rate up to 240 Mbyte/s using a 120 MHz pixel clock. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12-, 14- or 16-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

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3.27 Parallel synchronous slave interface (PSSI)

The PSSI is a generic synchronous 8-/16-bit parallel data input/output slave interface. It allows the transmitter to send a data valid signal to indicate when the data is valid, and the receiver to output a flow control signal to indicate when it is ready to sample the data.

The PSSI main features are:

- Slave mode operation
- 8- or 16-bit parallel data input or output
- 8-word (32-byte) FIFO
- Data enable (DE) alternate function input and Ready (RDY) alternate function output.

  When enabled, these signals can either allow the transmitter to indicate when the data is valid or the receiver to indicate when it is ready to sample the data, or both.

The PSSI shares most of the circuitry with the digital camera interface (DCMIPP). It thus cannot be used simultaneously with the DCMIPP.

3.28 LCD-TFT display controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

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3.29 JPEG codec (JPEG)

The JPEG codec can encode and decode a JPEG stream as defined in the ISO/IEC10918-1 specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Stallable design
- Support for single greyscale component
- Ability to enable/disable header processing
- Internal register interface
- Fully synchronous design
- Configuration for high-speed decode mode

3.30 Random number generator (RNG)

All the devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.31 Cryptographic acceleration (CRYP)

The devices implement state-of-the-art cryptographic algorithms featuring key sizes and computing protection as recommended by national security agencies. These agencies include: NIST for the U.S.A, BSI for Germany or ANSSI for France. The algorithms are used to support privacy, authentication, integrity, entropy and identity attestation.

The crypto engines embedded in STM32 reduce weaknesses in the implementation of critical cryptographic functions. They prevent, for example, the use of weak cryptographic algorithms and key sizes. They also enable shorter processing times and lower power consumption when performing cryptographic operations, by offloading those computations from Cortex-M7. This is especially true for asymmetric cryptography.

For product certification purposes, ST can provides certified device information on how these security functions are implemented and validated.

For more information on crypto engine processing times, refer to their respective sections in the reference manual.

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3.31.1 Crypto engines features

The table below lists the accelerated cryptographic operations available in the devices. Two AES accelerators are available. One is side-channel attack protected (SAES), while the second is more performance oriented (CRYP).

Note: Additional operations can be added using firmware.

The PKA can accelerate asymmetric crypto operations (like key pair generation, ECC scalar multiplication, point on curve check). See Section 40: Public key accelerator (PKA) for more details.

Table 11. Accelerated cryptographic operations

Operations	Algo-rithm	Specification	Key lengths (in bit)	Modes
Get entropy	RNG	NIST SP800-90B(1)	N/A	Software and hardware(2) modes running in parallel
Encryption, decryption	AES	FIPS PUB 197 NIST SP800-38A	128, 256	ECB, CBC, CTR(3)
Authenticated encryption or decryption		NIST SP800-38C NIST SP800-38D	128, 256	GCM, CCM
Cipher-based message authentication code		NIST SP800-38D	128, 256	GMAC
Checksum	SHA-1	FIPS PUB 180-4	N/A	Digest 160-bit
Cryptographic hash	SHA-2		-	SHA-224, SHA-256 SHA2-384, SHA2-512
Keyed-hashing for message authentication	HMAC	FIPS PUB 198-1 IETF RFC 2104	Short, long (>64 bytes)	-
Encryption/decryption key-pair generation(4)	RSA	IETF RFC 8017 NIST SP800-56B	Up to 4160	RSAES-OAEP
Signature(4) with hashing Signature verification	RSA	IETF RFC 8017 FIPS PUB 186-4	Up to 4160	PKCS1-v1_5, PSS
	ECDSA	ANSI X9.62 IETF RFC 7027 FIPS PUB 186-4	Up to 640	-
Key agreement	ECDH	ANSI X9.42		

1. Certifiable using STMicroelectronics reviewed documents.
2. Random numbers distribution to SAES and PKA using a dedicated hardware bus.
3. ECB and CBC chaining modes protected against side-channel and timing attacks in SAES.
4. Private key cryptography protected against side-channel and timing attacks.

Note: Binary curves, Edwards curves and Curve25519 are not supported by the PKA.

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3.32 Secure AES (SAES)

The devices provide an on-chip hardware AES encryption and decryption engine, which implements countermeasures and mitigations against power and electromagnetic side-channel attacks.

Clocked by the AHB bus clock, the SAES offers very good performance for a DPA resistant hardware accelerator. The SAES engine supports 128-bit or 256-bit keys in electronic code book (ECB), cipher block chaining (CBC), (CTR), (GCM), (CCM), (GMAC) modes.

The SAES can be used for extra-secure on-chip storage for sensitive information.

For more information, refer to the *Secure AES coprocessor (SAES)* section in reference manual RM0477.

3.33 Hash processor (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-2 family) and the HMAC (keyed-hash message authentication code) algorithm. HMAC is suitable for applications requiring message authentication.

The hash processor computes FIPS (Federal Information Processing Standards) approved digests of length of 160, 224, 256 bits, for messages of any length less than 264 bits (for SHA-1, SHA-224 and SHA-256) or less than 2^{128} bits (for SHA-384, SHA-512).

3.34 Public key accelerator (PKA)

The PKA (public key accelerator) is intended for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann or ECC (elliptic curve cryptography) over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

For a given operation, all needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

When manipulating secrets, the PKA incorporates a protection against side-channel attacks (SCA), including differential power analysis (DPA), certified SESIP and PSA security assurance level 3.

3.35 Memory cipher engine (MCE)

Memory cipher engine (MCE) defines, in a given address space, multiple regions with specific security setup (encryption, privilege, write). All system bus traffic going through an encrypted region is managed on-the-fly by the MCE, automatically decrypting reads and encrypting writes if authorized.

Multiple ciphering option (stream, block, fast block) are available to offer the best security / performance trade-off.

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3.35.1 Memory cipher features

the MCE embed a system bus in-line encryption (for writes) and decryption (for reads), based on embedded firewall programming. up to Four encryption modes per region (maximum 4 regions): no encryption (bypass mode), stream cipher, block cipher and fast block cipher modes.

The Start and end of regions are defined with 4 kBytes granularity

The block mode with AES cipher is compatible with ECB mode specified in NIST FIPS publication 197 Advanced encryption standard (AES) (normal or fast).

The stream mode with AES cipher is compliant with CTR mode specified in NIST SP800-38A Recommendation for Block Cipher Modes of Operation.

It Includes a leakage resilient mode of operation as defense against side channel attacks (SCA).

When encryption is enabled, support for AXI-64bit INCRx (x=1 to 8) and WRAPx (x=4) write transactions

3.35.2 Memory cipher implementation

Table 12. MCE implementation

MCE features	MCE1	MCE2/3
Number of regions	4	
Cipher engines	AES x 2	12 rounds Noekeon x2
Derive key function	normal, fast	
Master key	2	
Chaining modes (encryption mode)	block, stream	block
Cipher context(s)	2	0

Note: When MCE is used in conjunction with XSPI it is mandatory to access the flash memory using the memory map mode of the flash memory controller.

3.36 Timers and watchdogs

The devices include one advanced-control timers, eleven general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in Debug mode.

Table 13 compares the features of the advanced-control, general-purpose and basic timers.

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Table 13. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output
Advanced-control	TIM1	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	4
General purpose	TIM2,TIM3, TIM4 TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No
	TIM9,TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
	TIM13,TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No
Low-power timer	LPTIM1, LPTIM2, LPTIM3	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	Yes	2	No
	LPTIM4, LPTIM5		Up		No	0	No

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3.36.1 Advanced-control timers (TIM1)

The advanced-control timers (TIM1) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 - 100%)
- One-pulse mode output

In Debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 support independent DMA request generation.

3.36.2 General-purpose timers (TIMx)

There are up to elven synchronizable general-purpose timers embedded in the STM32H7Sxx8 devices (see *Table 13: Timer feature comparison* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  They are full-featured general-purpose timers with 32-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in Debug mode.

  All have independent DMA request generation and support quadrature encoders.

  They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

- **TIM9, TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel,

  TIM9, TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple time bases.

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3.36.3 Basic timers TIM6 and TIM7

These timers are mainly used for waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.36.4 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

The devices embed five low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wake up the system from Stop mode.

3.36.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 4-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.36.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.36.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.37 Real-time clock (RTC)

The RTC provides an automatic wakeup to manage all low-power modes.

The real-time clock (RTC) is an independent BCD timer/counter. The RTC provides a time-of-day clock/calendar with programmable alarm interrupts.

The RTC includes also a periodic programmable wakeup flag with interrupt capability.

After backup domain reset, all RTC registers are protected against possible parasitic write accesses except the one’s configured in privilege mode.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, Low-power mode or under reset).

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The RTC unit main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), day (day of week), date (day of month), month, and year.
- Daylight saving compensation programmable by software.
- Programmable alarm with interrupt function. The alarm can be triggered by any combination of the calendar fields.
- Automatic wakeup unit generating a periodic flag that triggers an automatic wakeup interrupt.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Accurate synchronization with an external clock using the subsecond shift feature.
- Digital calibration circuit (periodic counter correction): 0.95 ppm accuracy, obtained in a calibration window of several seconds
- Timestamp function for event saving
- Maskable interrupts/events:
  - Alarm A
  - Alarm B
  - Wakeup interrupt
  - Timestamp

3.38 Tamper and backup registers (TAMP)

32 x 32-bit backup registers are retained in all low-power modes and also in VBAT mode. They can be used to store sensitive data as their content is protected by an tamper detection circuit. 8 tamper pins (8 input or 8 outputs) and 12 internal tampers are available for anti-tamper detection. The 8 external tamper pins can be configured for edge detection, edge and level, level detection with filtering, or up to 4 active tamper which increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features

- 32 backup registers:
  - the backup registers (TAMP_BKPxR) are implemented in the RTC domain that remains powered-on by VBAT when the V_{DD} power is switched off.
- 8 external tamper detection events.
  - Each external event can be configured to be active (4 Tamper) or passive (8 Tamper).
  - External passive tampers with configurable filter and internal pull-up.
- 11 internal tamper events.
- Any tamper detection can generate a RTC timestamp event.
- Any tamper detection erases the backup registers.
- Monotonic counter.

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3.39 Inter-integrated circuit interface (I2C)

The STM32H7Sxx8 embeds three I^2C interfaces.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bit rate up to 100 kbit/s
  - Fast-mode (Fm), with a bit rate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match[a]
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.40 Improved inter-integrated circuit (I3C)

The I^3C interface handles communication between this device and others, such as sensors and host processor(s) that are connected to an I^3C bus.

- The I3C peripheral implements all the required features of the MIPI I3C specification v1.1. It can control all I^3C bus-specific sequencing, protocol, arbitration, and timing. It acts as a controller (formerly known as master) or as a target (formerly known as slave).
- The I3C peripheral, acting as controller, improves the features of the I2C interface, while preserving some backward compatibility; it allows an I2C target to operate on an I^3C bus in legacy I^2C fast-mode (Fm) or legacy I^2C fast-mode plus (Fm+), provided that the latter does not perform clock stretching.
- The I3C peripheral can be used with DMA in order to offload the CPU.

Refer to reference manual RM0477 for full details of the I3C controller features versus MIPI v1.1.

a. Under characterization.

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3.41 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The STM32H7Sxx8 has three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8) and one low-power universal asynchronous receiver transmitter (LPUART1). Refer to *Table 14* for a summary of USARTx UARTx and LPUART features.

Table 14. USART, UART and LPUART features

Modes/features(1)	Full feature set	Basic feature set	Low-power feature set
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode (master/slave)	X	-	-
Smartcard mode	X	-	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual clock domain	X	X	X
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Auto baud rate detection	X	X	-
Driver Enable	X	X	X
USART data length	7, 8 and 9 bits		
Tx/Rx FIFO	X	X	X
Tx/Rx FIFO size (bytes)	16		
Wake-up from low-power mode	X(2)	X(2)	X(2)

1. “X” = supported, “-” = not supported.
2. Wake-up supported from Stop mode.

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3.41.1 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The USART offers a flexible means to perform full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS).

Multiprocessor communications are also supported.

High-speed data communications are possible by using the DMA (direct memory access) for multibuffer configuration.

Table 15. Instance implementation on STM32H7Sxx8

Instance	STM32H7Sxx8
USART1	Full
USART2	Full
USART3	Full
UART4	Basic
UART5	Basic
UART7	Basic
UART8	Basic
LPUART1	Low-power

3.41.2 Low-power universal asynchronous receiver transmitter (LPUART)

The LPUART is an UART which enables bidirectional UART communications with a limited power consumption. Only 32.768 kHz LSE clock is required to enable UART communications up to 9600 baud. Higher baud rates can be reached when the LPUART is clocked by clock sources different from the LSE clock.

Even when the microcontroller is in low-power mode, the LPUART can wait for an incoming

UART frame while having an extremely low energy consumption. The LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption.

It supports half-duplex single-wire communications and modem operations (CTS/RTS). It also supports multiprocessor communications.

DMA (direct memory access) can be used for data transmission/reception.

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3.42 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

3.42.1 Introduction

The device embed six serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to setup communication with concrete slave and to assure it handles the data flow properly. The Motorola® data format is used by default, but some other specific modes are supported as well.

3.42.2 SPI main features

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- From 4-bit up to 32-bit data size selection or fixed to multiply of 8-bit
- Multi master or multi slave mode capability
- Dual clock domain, the peripheral kernel clock is independent of APB bus clock
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO x MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can verify integrity of the communication at the end of transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun, the mode fault and frame error at dependency on the operating mode
- Two multiply of 8-bit embedded Rx and Tx FIFOs (FIFO size depends on instance)

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- Configurable FIFO thresholds (data packing)
- Capability to handle data streams by system DMA controller
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- optional status pin RDY signalizing the slave device ready to handle the data flow

3.42.3 SPI implementation

Table 16 describes the SPI implementation. The instances are applied either with a full set or a limited set of features.

Table 16. SPI features

SPI feature	SPI2S1, SPI2S2, SPI2S3 and SPI2S6 (full feature set instances)	SPI4 and SPI5 (full feature set instances)
Data and CRC size	Configurable from 4 to 32- bit	Configurable from 4 to 16- bit
CRC computation	CRC polynomial length configurable from 5 to 33- bit	CRC polynomial length configurable from 5 to 17- bit
Size of FIFOs	16x8-bit	8x8-bit
Number of data control (TSIZE)	Up to 65536	Up to 65536
I2S feature	Yes	No
Autonomous in Stop modes with wakeup capability	No	No
Autonomous in LP-Stop and Standby modes with wakeup capability	No	No

Note: For detailed information about instances capabilities to exit from Stop and Standby modes refer to SPI wakeup and interrupt requests in reference manual RM0477.

3.43 Serial audio interfaces (SAI)

The devices embed two SAI. Refer to *Table 17: STM32H7Sxx8 SAI features* for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

3.43.1 SAI main features

The devices embed 2 SAIs that allow the design of many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC’97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.
Audio sampling frequencies up to 192 kHz are supported.
In addition, up to 4 microphones can be supported thanks to an embedded PDM interface.

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The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.43.2 SAI implementation

Table 17. STM32H7Sxx8 SAI features (1)

SAI features	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
FIFO size	8 words	8 words
SPDIF	X	X
PDM	X(2)	-

1. 'X' = supported, '-' = not supported.
2. Only signals D[3:1], and CK[2:1] are available.

3.44 SPDIFRX receiver interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal is available, the SPDIFRX resamples the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that is used to compute the exact sample rate for clock drift algorithms.

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3.45 Management data input/output (MDIO) slaves

The devices embed an MDIO slave interface it includes the following features:

- 32 MDIO register addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO register write
  - MDIO register read
  - MDIO protocol error
- Able to operate in and wake up from STOP mode

3.46 Secure digital input/output MultiMediaCard interface (SDMMC)

Two secure digital input/output MultiMediaCard interfaces (SDMMC) provide an interface between the AHB bus and SD memory cards, SDIO devices and e.MMC devices.

The SDMMC features include the following:

- Full compliance with *MultiMediaCard System Specification Version 5.1*.
  Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit.
  (HS200 speed limited by maximum allowed I/O speed, HS400 is not supported)
- Full compatibility with previous versions of MultiMediaCards (backward compatibility).
- Full compliance with *SD memory card specifications version 6.0*.
  (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Full compliance with SDIO card specification version 4.0.
  Card support for two different databus modes: 1-bit (default) and 4-bit.
  (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Data transfer up to 208 Mbyte/s for the 8-bit mode. (depending maximum allowed I/O speed).
- Data and command output enable signals to control external bidirectional drivers.
- The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.
- IDMA linked list support

Each SDMMC is coupled with a delay block (DLYB) allowing support of an external data frequency above 100 MHz.

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3.47 Controller area network (FDCAN1, FDCAN2)

The controller area network (CAN) subsystem consists of two CAN module, a shared message RAM memory and a configuration block.

The modules (FDCAN) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 2 Kbyte message RAM implements filters, receives FIFOs, transmits event FIFOs and transmits FIFOs.

The FDCAN main features are:

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015, -4
- CAN FD with maximum 64 data bytes supported
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering
- 2 receive FIFOs of three payloads each (up to 64 bytes per payload)
- Separate signaling on reception of high priority messages
- Transmit FIFO / queue of three payload (up to 64 bytes per payload)
- Configurable transmit Event FIFO
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains: APB bus interface and CAN core kernel clock
- Power-down support

3.48 Universal serial bus on-the-go full-speed (OTG_FS)

The main features support both host-mode and device-mode.It is compliant with the Universal Serial Bus Specification Rev 2.0. it includes an on-chip full-speed PHY.

It includes full support (PHY) for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Rev 2.0 specification. it support the A-B device identification (ID line) .It supports OTG monitoring of VBUS levels with internal comparators and the SOF pulse on PAD ALT function.

- SOF pulse internal connection to timer (TIM2 and.TIM5)

It includes power saving features such as system stop during USB suspend, switch-off of clock domains internal to the digital core, PHY and DFIFO power management. it includes a dedicated RAM of 1.25 Kbytes with advanced FIFO control as configurable partitioning of RAM space into different FIFOs for flexible and efficient use of RAM

It supports charging port detection as described in Battery Charging Specification Revision 1.2.

Table 18. OTG_FS speeds supported

Mode	HS (480 Mbit/s)	FS (12 Mbit/s)	LS (1.5 Mbit/s)
Host mode	-	X	X
Device mode	-	X	-

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3.49 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed one USB High Speed host/device (up to 480 Mbit/s) with one physical port. OTG_HS supports both low-speed, full-speed as well as high-speed modes. It integrates a physical interface (PHY) which can be used for either low-speed (1.5 Mbit/s), full-speed (12 Mbit/s) or high-speed operation (480 Mbit/s). it includes the SOF pulse on PAD ALT function.

- SOF pulse internal connection to timer (TIM2 and TIM5)

It includes power saving features such as system stop during USB suspend, switch-off of clock domains internal to the digital core, PHY and DFIFO power management. it includes a dedicated RAM of 1.25 Kbytes with advanced FIFO control as configurable partitioning of RAM space into different FIFOs for flexible and efficient use of RAM

It supports charging port detection as described in Battery Charging Specification Revision 1.2.

The OTG_HS uses a dedicaded digital power supply, DVDD. This should be connected to VCAP when used, and to GND when not used.

Table 19. OTG_HS speeds supported

Mode	HS (480 Mbit/s)	FS (12 Mbit/s)	LS (1.5 Mbit/s)
Host mode	X	X	X
Device mode	X	X	-

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3.50 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, and so on). The PHY is connected to the device MII port using 21 signals for MII or 12 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

3.51 USB Type-C power delivery controller (UCPD)

The devices embed one controllers compliant with USB Type-C Rev.2.1 and USB Power Delivery Rev. 3.1 specifications.

The controllers use specific I/Os supporting the USB Type-C and USB Power Delivery requirements, featuring the USB Type-C pull-up (Rp, current source) and pull-down (Rd, resistors) and the USB Power Delivery message transmission and reception

The digital controller handles embed the USB Type-C level detection with de-bounce, generating interrupts and FRS detection, generating an interrupt

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages and FRS signaling.

3.52 High-definition multimedia interface - consumer electronics control (HDMI-CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the consumer electronics control (CEC) protocol (supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory

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overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wake up the MCU from Stop mode on data reception.

3.53 Development support

3.53.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.53.2 Embedded Trace Macrocell

The Arm Embedded Trace Macrocell (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

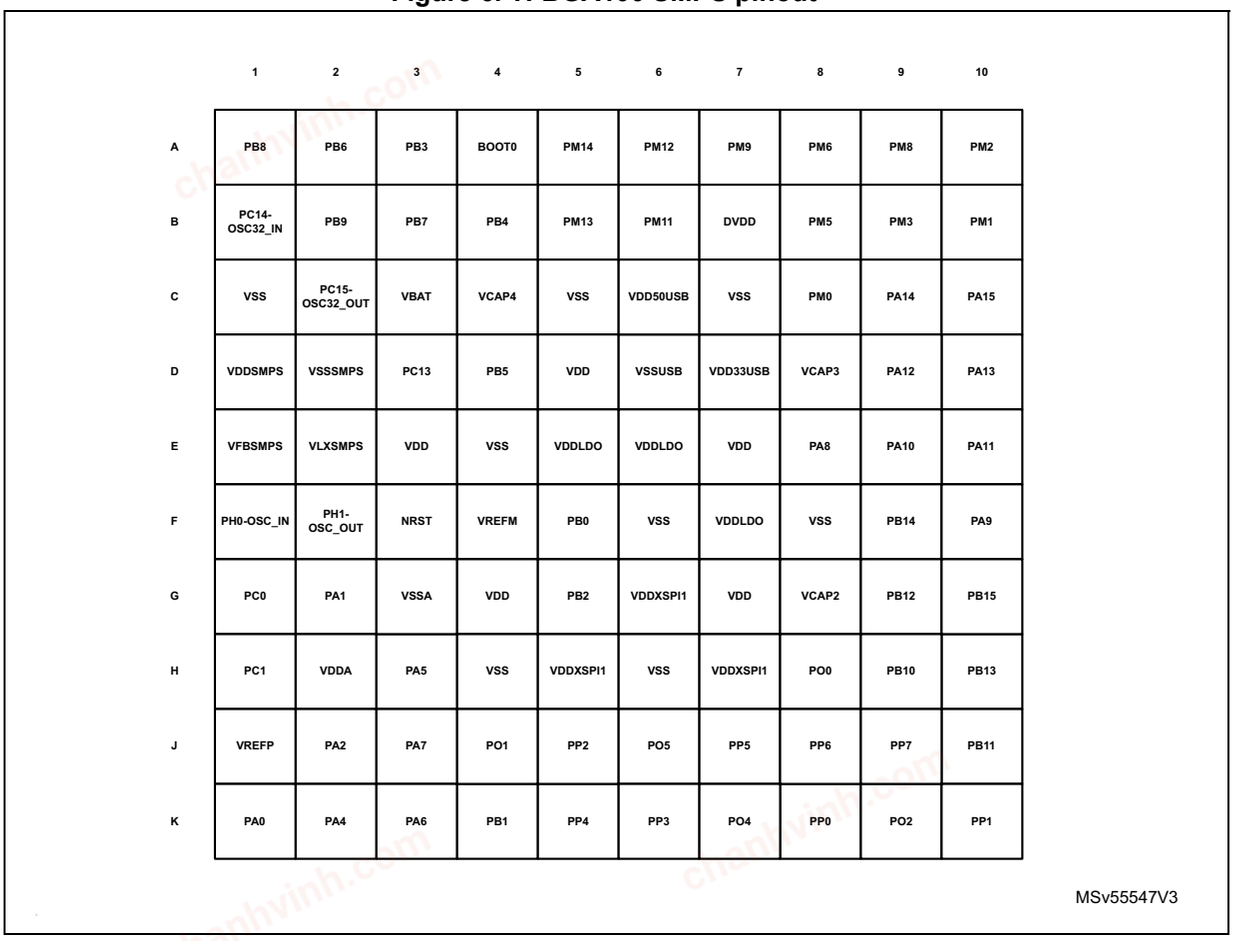
Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The ETM operates with third party debugger software tools.

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4 Pinouts, pin description and alternate functions

Figure 6. TFBGA100 SMPS pinout[(a)]



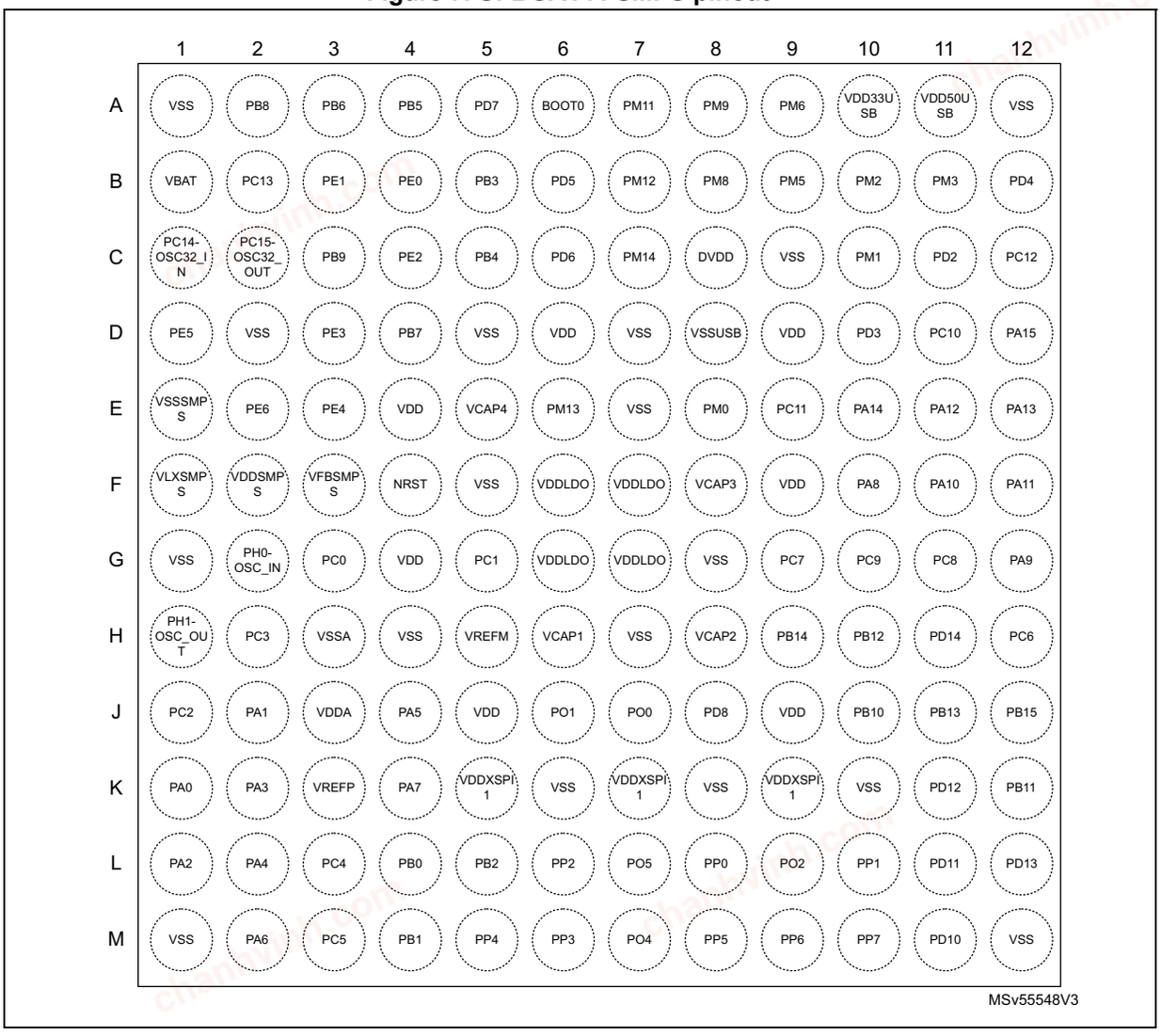
	1	2	3	4	5	6	7	8	9	10
A	PB8	PB6	PB3	BOOT0	PM14	PM12	PM9	PM6	PM8	PM2
B	PC14-OSC32_IN	PB9	PB7	PB4	PM13	PM11	DVDD	PM5	PM3	PM1
C	VSS	PC15-OSC32_OUT	VBAT	VCAP4	VSS	VDD50USB	VSS	PM0	PA14	PA15
D	VDDSMPS	VSSSMPS	PC13	PB5	VDD	VSSUSB	VDD33USB	VCAP3	PA12	PA13
E	VFBSMPS	VLXSMPS	VDD	VSS	VDDLDO	VDDLDO	VDD	PA8	PA10	PA11
F	PH0-OSC_IN	PH1-OSC_OUT	NRST	VREFM	PB0	VSS	VDDLDO	VSS	PB14	PA9
G	PC0	PA1	VSSA	VDD	PB2	VDDXSPI1	VDD	VCAP2	PB12	PB15
H	PC1	VDDA	PA5	VSS	VDDXSPI1	VSS	VDDXSPI1	PO0	PB10	PB13
J	VREFP	PA2	PA7	PO1	PP2	PO5	PP5	PP6	PP7	PB11
K	PA0	PA4	PA6	PB1	PP4	PP3	PO4	PP0	PO2	PP1

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a. The above figure shows the package top view.

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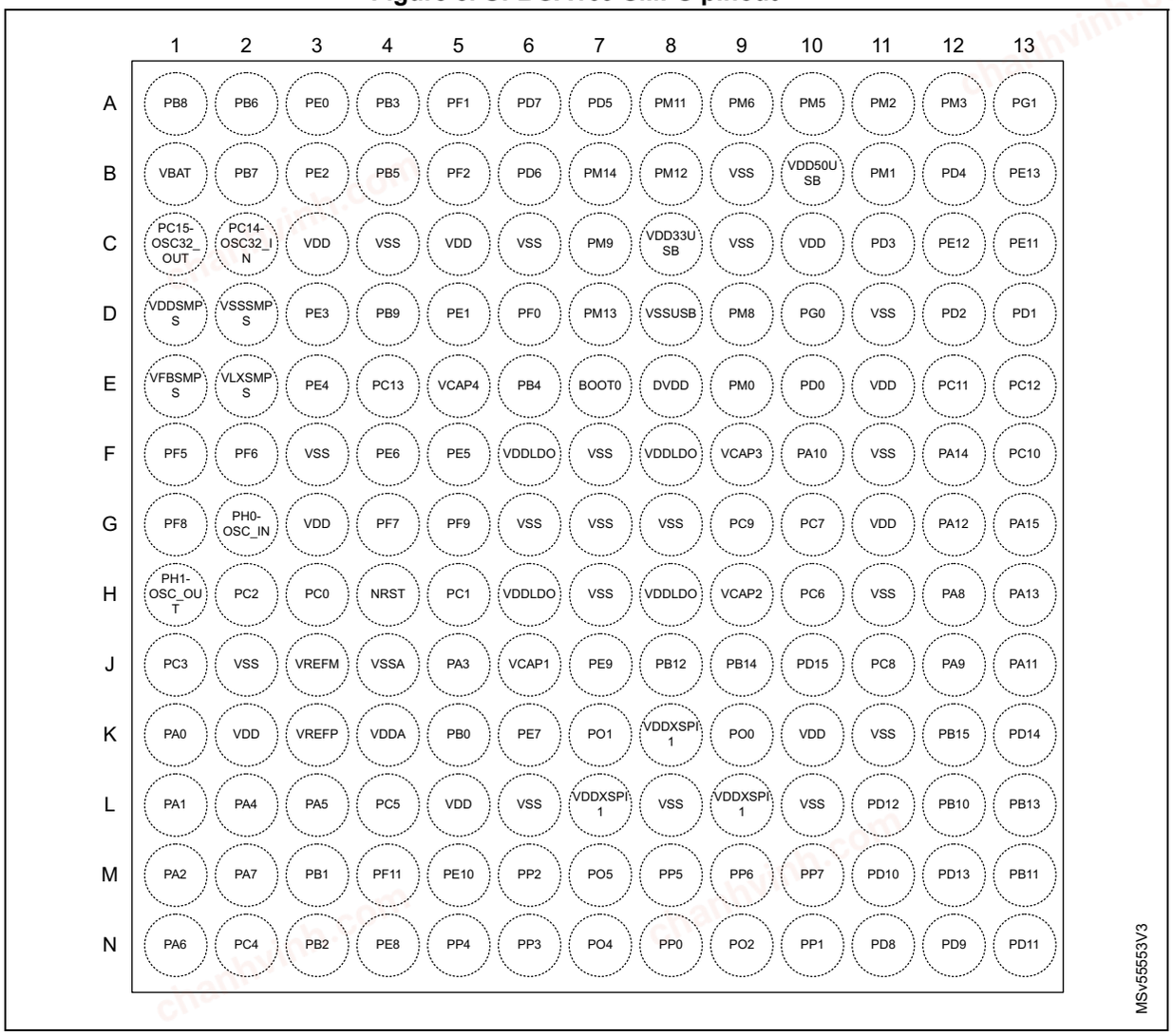
Figure 7. UFBGA144 SMPS pinout[a]



a. The above figure shows the package top view.

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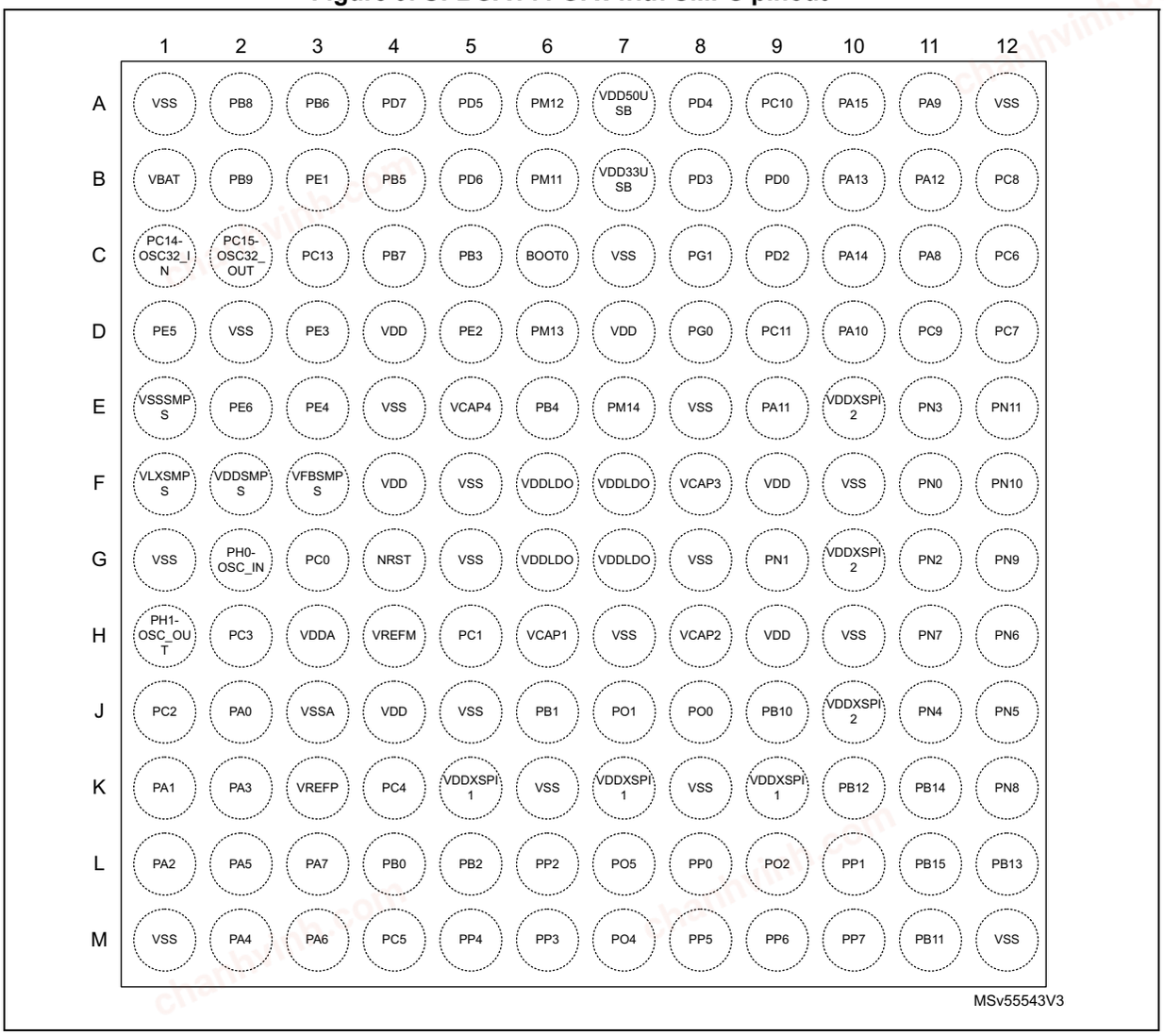
Figure 8. UFBGA169 SMPS pinout[a]



a. The above figure shows the package top view.

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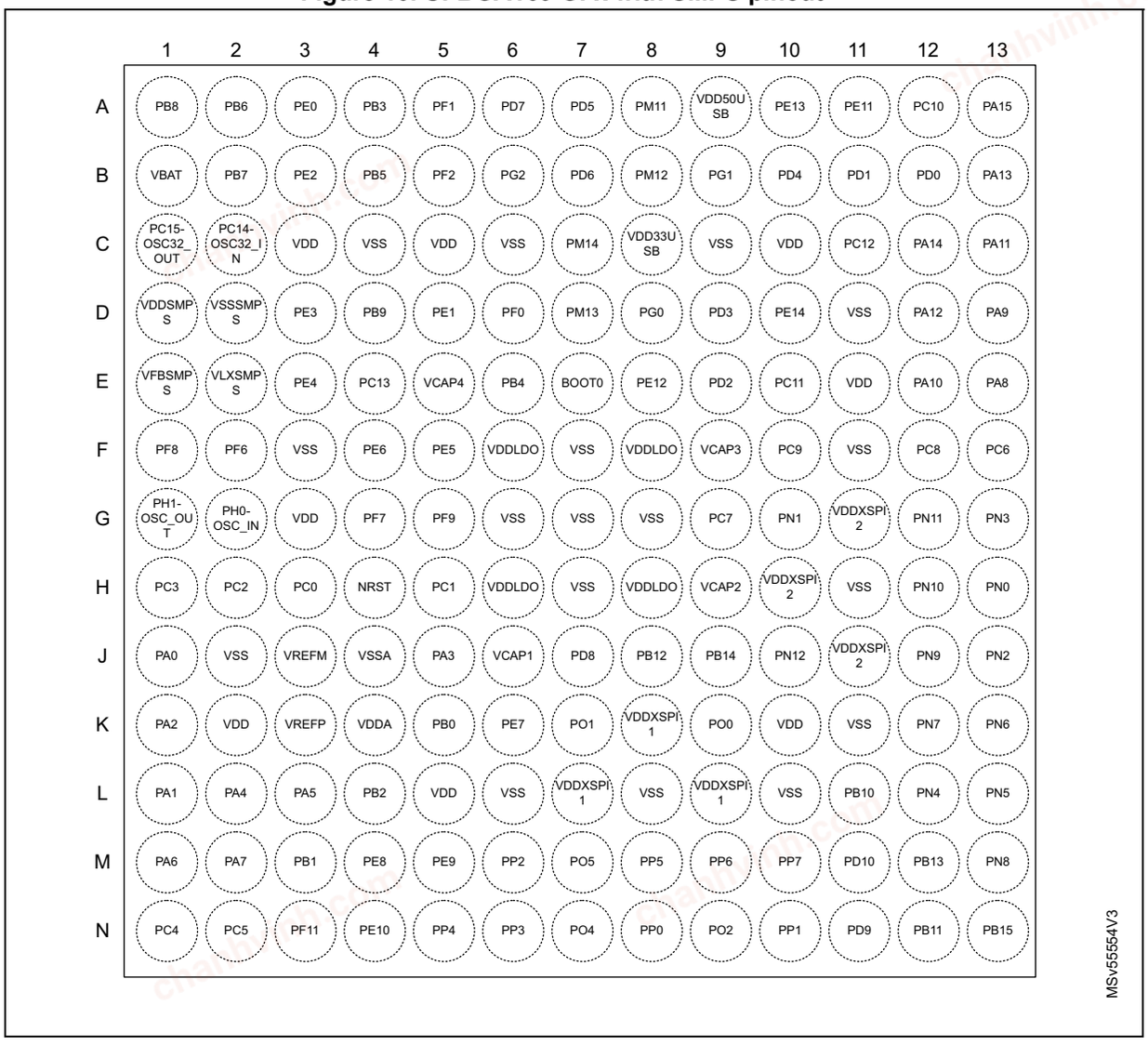
Figure 9. UFBGA144 GFx with SMPS pinout(a)



a. The above figure shows the package top view

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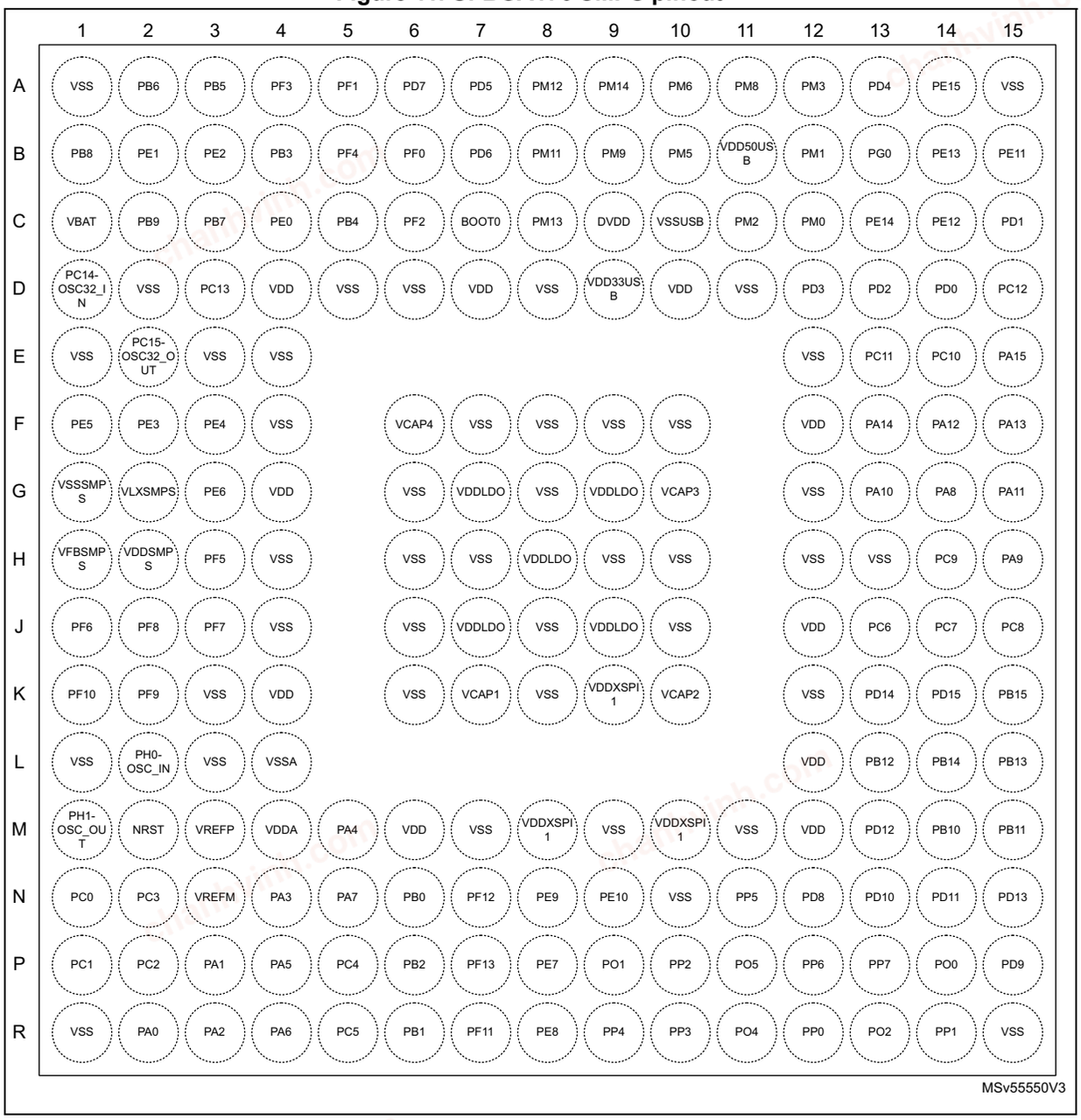
Figure 10. UFBGA169 GFx with SMPS pinout(a)



a. The above figure shows the package top view

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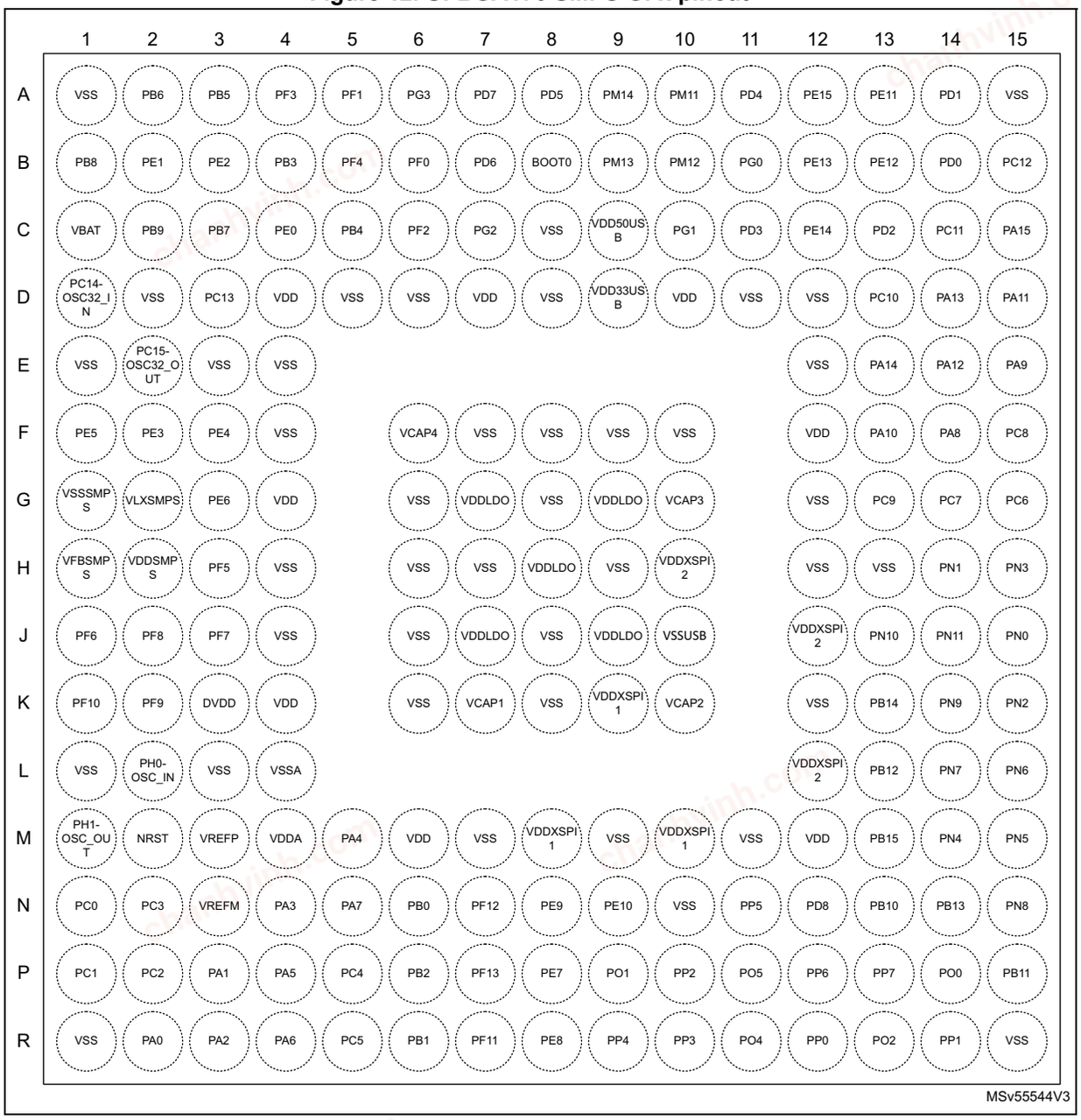
Figure 11. UFBGA176 SMPS pinout[(a)]



a. The above figure shows the package top view

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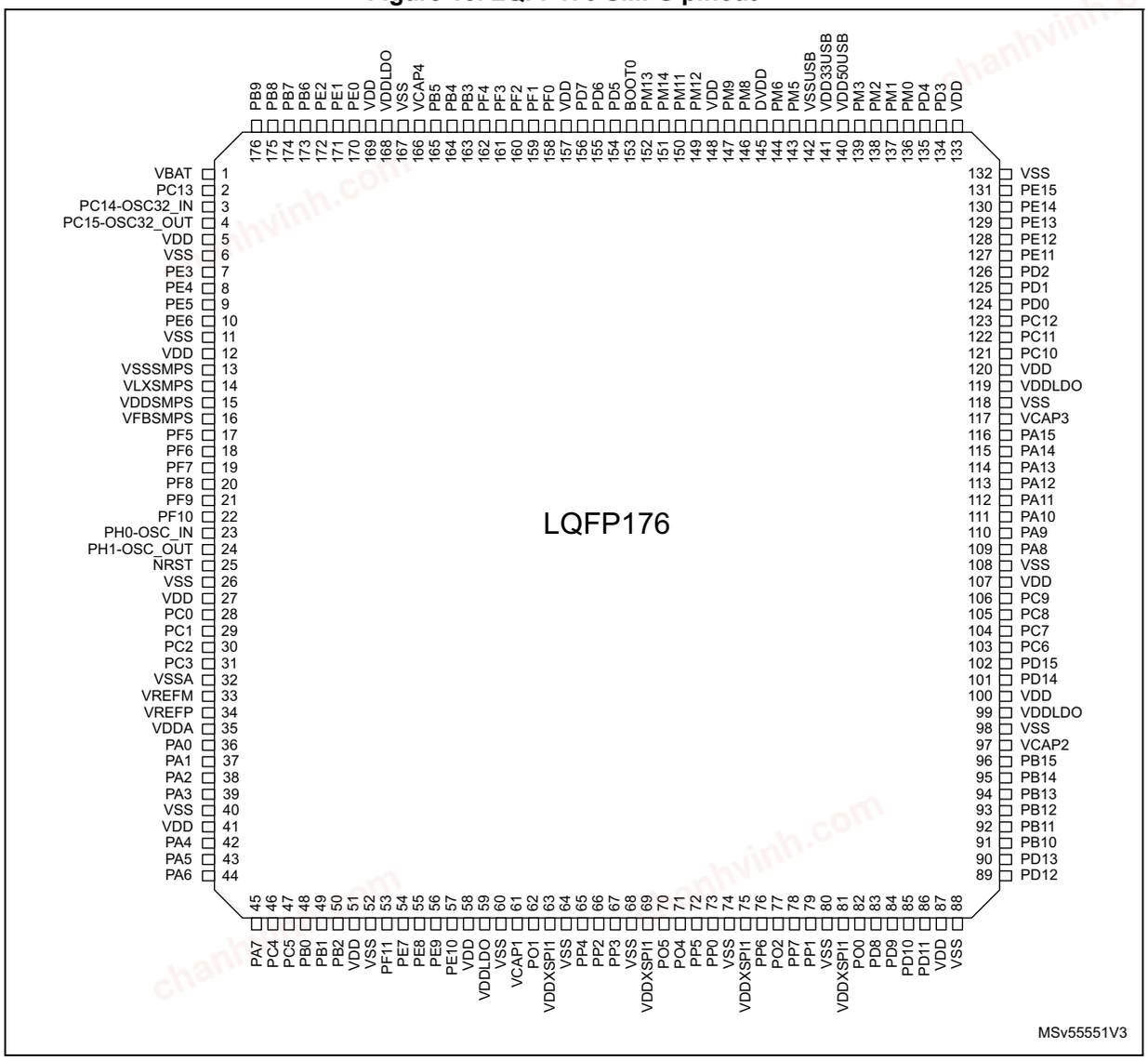
Figure 12. UFBGA176 SMPS GFx pinout[a]



a. The above figure shows the package top view

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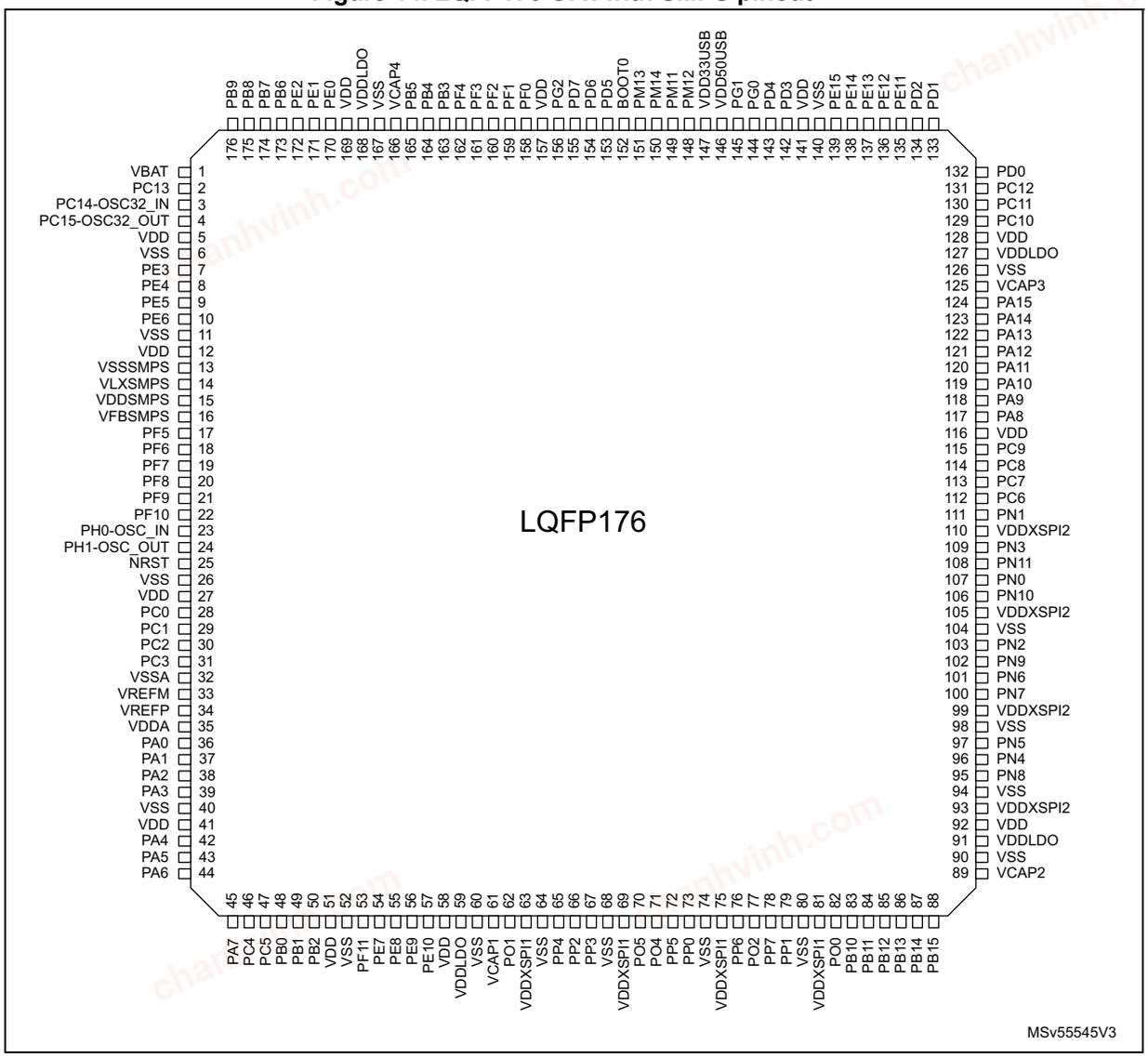
Figure 13. LQFP176 SMPS pinout[a]



a. The above figure shows the package top view

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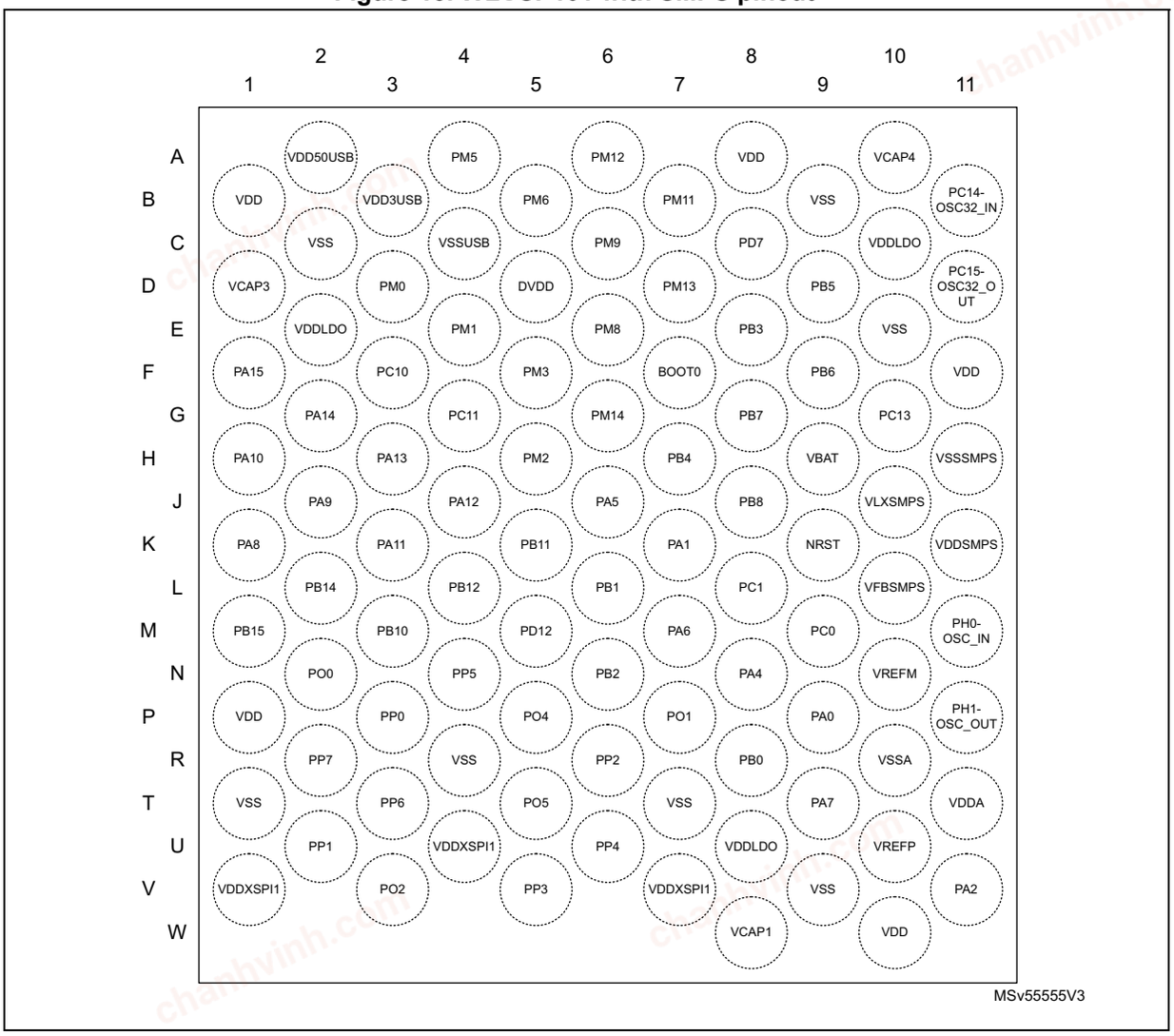
Figure 14. LQFP176 GFx with SMPS pinout(a)



a. The above figure shows the package top view

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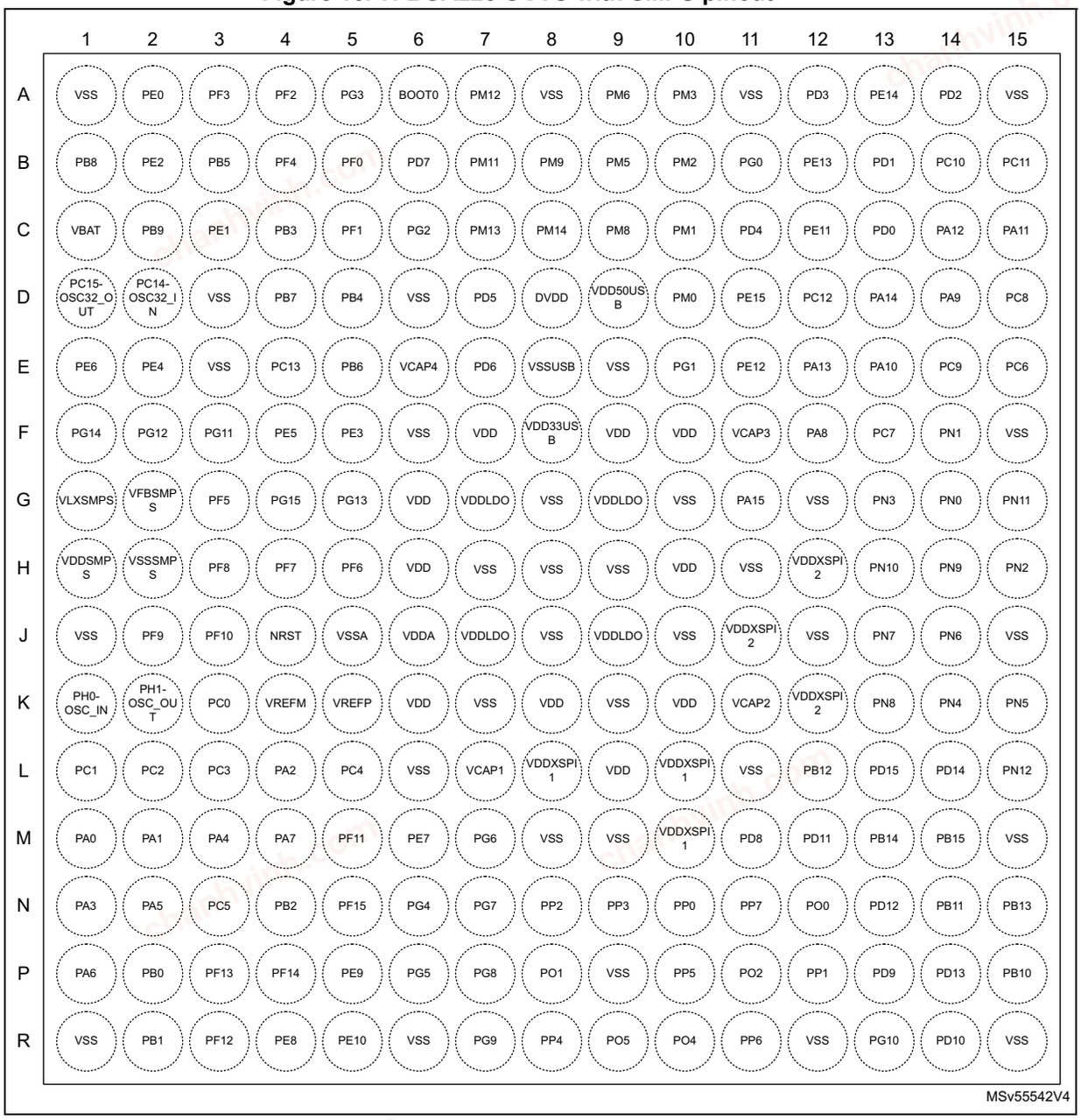
Figure 15. WLCSP101 with SMPS pinout(a)



a. The above figure shows the package top view

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Figure 16. TFBGA225 OCTO with SMPS pinout[a][b]

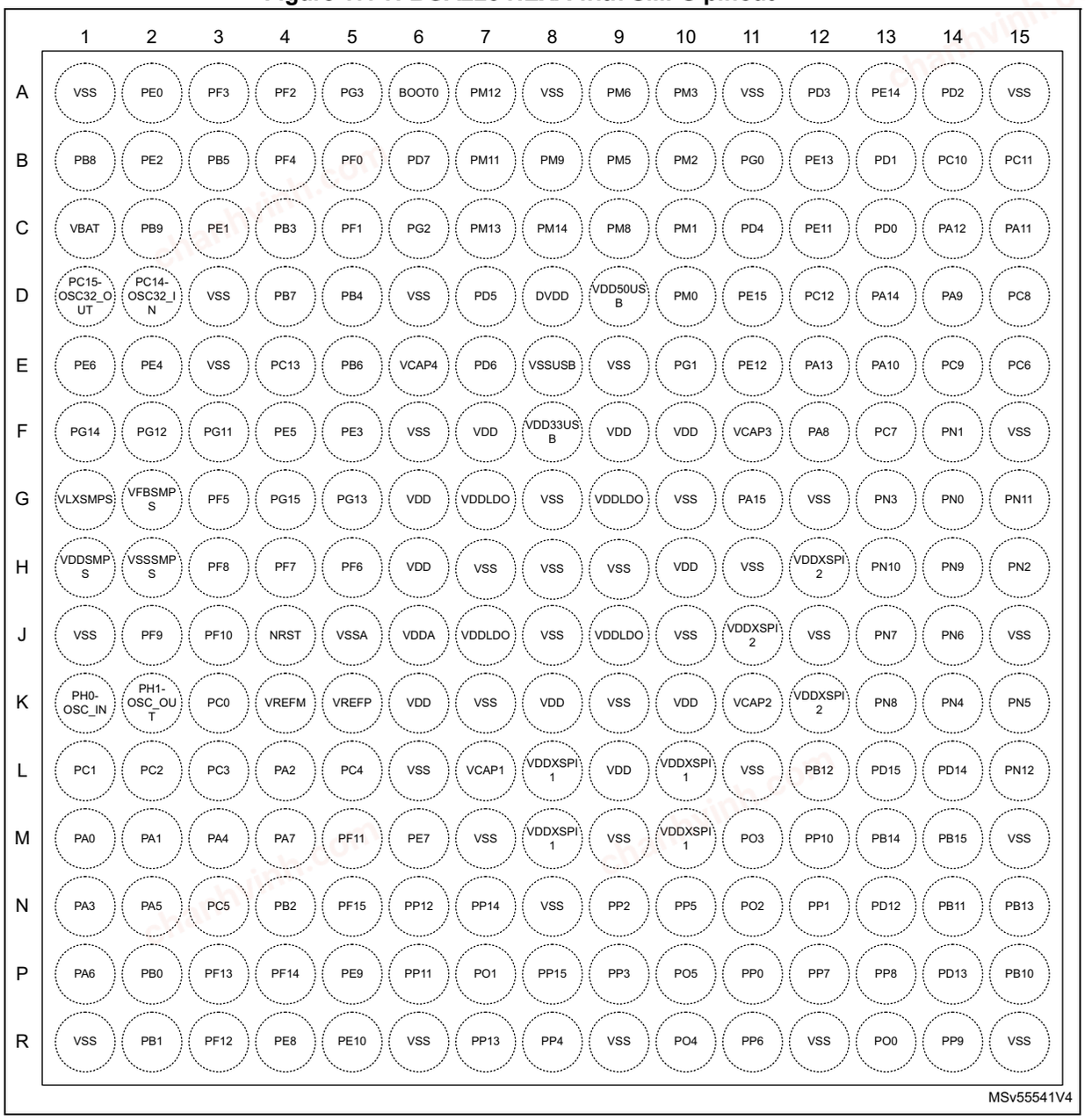


a. The above figure shows the package top view

b. The above figure shows the package top view

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Figure 17. TFBGA225 HEXA with SMPS pinout[a][b]

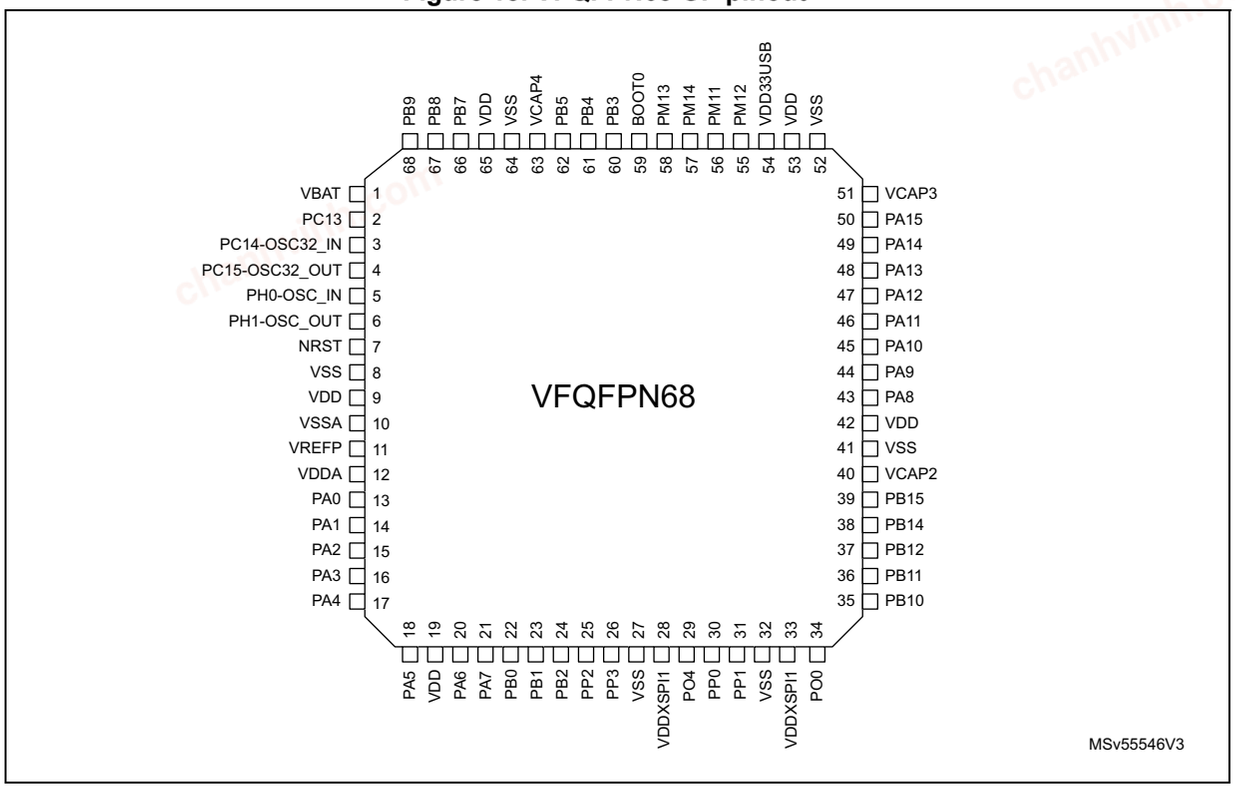


a. The above figure shows the package top view

b. The above figure shows the package top view

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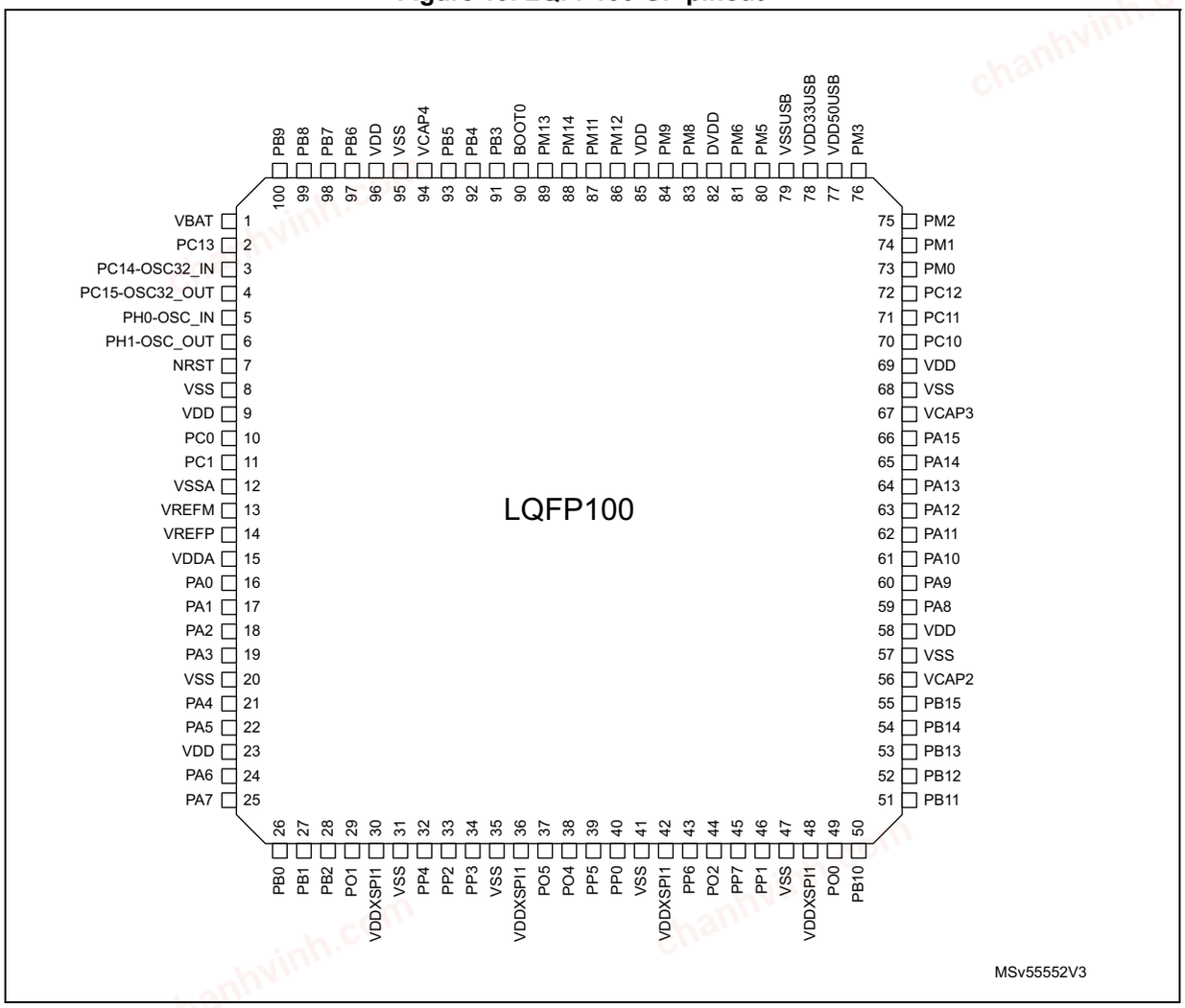
Figure 18. VFQFPN68 GP pinout[a]



a. The above figure shows the package top view

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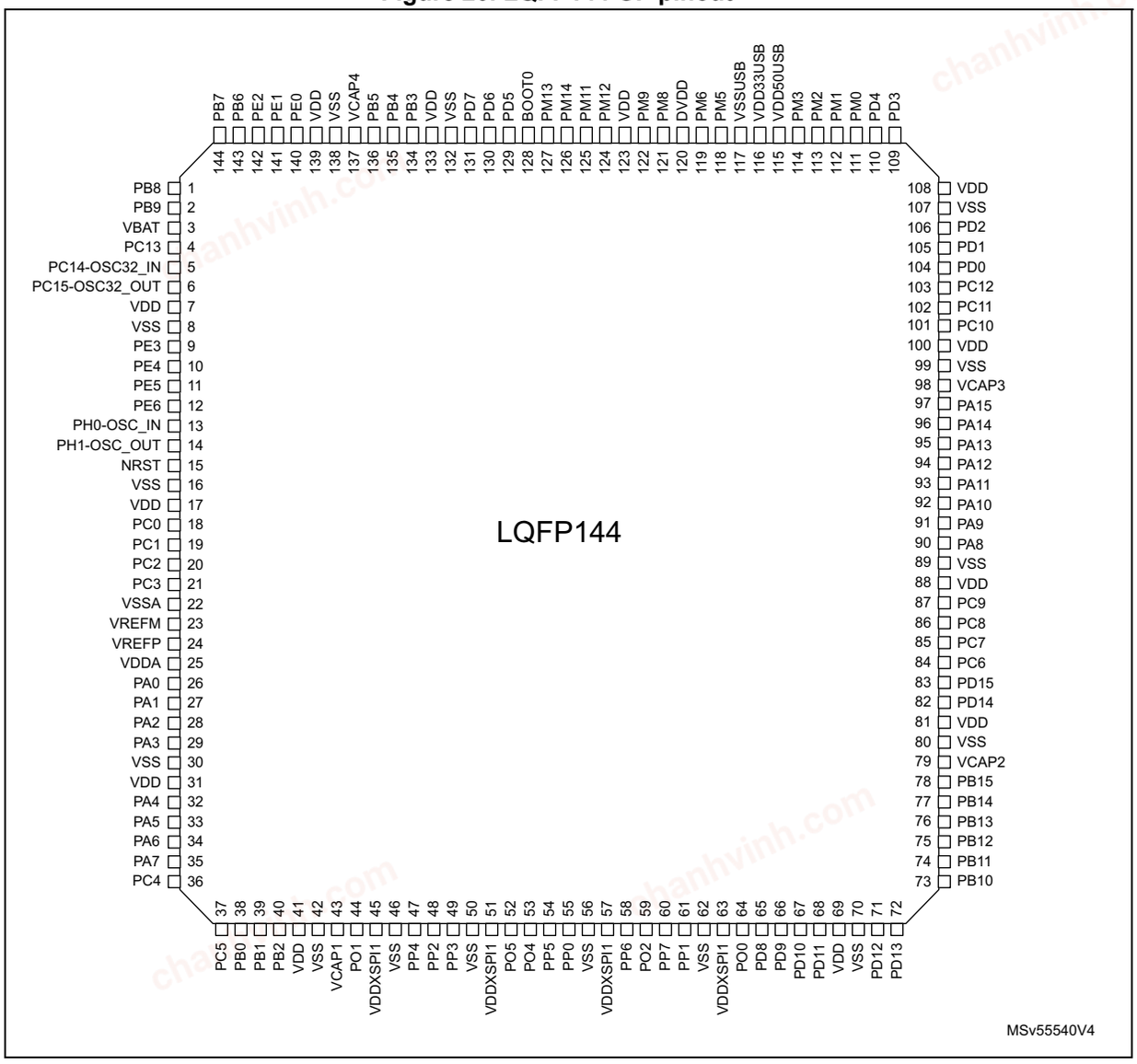
Figure 19. LQFP100 GP pinout[a]



a. The above figure shows the package top view

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Figure 20. LQFP144 GP pinout[(a)]



a. The above figure shows the package top view

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4.1 Pin description

Table 20. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input/output pin
I/O structure		FT	5V-tolerant I/O
		TT	3.6V-tolerant I/O
		B	Dedicated BOOT pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os(1)	
		_a	I/O, with analog switch function supplied by V_{DDA}
		_f	I/O, Fm+ capable
		_h	I/O with high-speed low-voltage mode (HSLV)
		_s	I/O supplied only by V_{DDIOx}(2)
		_t	I/O with tamper function functional in VBAT mode
		_c	I/O power delivery
		_d	I/O i/o dead battery
		_u	I/O USB
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in the table below are a concatenation of various options. Examples: FT_hat, FT_fs, TT_a.
2. VDDIOx represents VDD or VDDXSPIx.

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Table 21. STM32H7Sxx8 pin and ball descriptions

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
B2	C3	B2	D4	D4	C2	176	176	C2	-	C2	C2	68	100	2	PB9	I/O	FT_h	-	TIM17_CH1, TIM4_CH4, I2C1_SDA/I3C1_SDA, SPI2_NSS/I2S2_WS, PSSI_D7, SDMMC1_CDIR, UART4_TX, FDCAN1_TX, SDMMC2_D5, SDMMC1_D5, DCMIPP_D7, EVENTOUT	TAMP_IN2/ TAMP_OUT1
C3	B1	B1	B1	B1	C1	1	1	C1	H9	C1	C1	1	1	3	VBAT	S	-	-	-	-
C1	A1	A1	C4	B9	A1	-	-	A1	B9	A1	A1	-	-	-	VSS	S	-	-	-	-
D3	B2	C3	E4	E4	D3	2	2	D3	G10	E4	E4	2	2	4	PC13	I/O	-	-	EVENTOUT	TAMP_IN1/ TAMP_OUT2, RTC_OUT1/ RTC_TS, WKUP3

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
C5	A12	A12	C6	C4	A15	-	-	A15	C2	A8	A8	-	-	-	VSS	S	-	-	-	-
B1	C1	C1	C2	C2	D1	3	3	D1	B11	D2	D2	3	3	5	PC14-OSC32_IN(OSC32_IN)	I/O	-	-	EVENTOUT	OSC32_IN
C2	C2	C2	C1	C1	E2	4	4	E2	D11	D1	D1	4	4	6	PC15-OSC32_OUT(OSC32_OUT)	I/O	-	-	EVENTOUT	OSC32_OUT
D5	D6	D4	C3	C3	D4	5	5	D4	F11	F7	F7	-	-	7	VDD	S	-	-	-	-
C7	C9	C7	C9	C6	D2	6	6	C8	E10	A11	A11	-	-	8	VSS	S	-	-	-	-
-	D3	D3	D3	D3	F2	7	7	F2	-	F5	F5	-	-	9	PE3	I/O	FT_h	-	TRACED0, LPTIM5_ETR, TIM15_BKIN, SAI1_SD_B, ETH_MII_RXD3, FMC_D12/FMC_AD12, EVENTOUT	-
-	E3	E3	E3	E3	F3	8	8	F3	-	E2	E2	-	-	10	PE4	I/O	FT_h	-	TRACED1, SAI1_D2, ADF1_SDI0, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, PSSI_D4, FMC_D13/FMC_AD13, DCMIPP_D4, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	D1	D1	F5	F5	F1	9	9	F1	-	F4	F4	-	-	11	PE5	I/O	FT_h	-	TRACED2, ADF1_CCK1, SAI1_CK2, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, PSSI_D6, FMC_D14/FMC_AD14, DCMIPP_D6, EVENTOUT	-
-	E2	E2	F4	F4	G3	10	10	G3	-	E1	E1	-	-	12	PE6	I/O	FT_h	-	TRACED3, TIM1_BKIN2, SAI1_D1, ADF1_SDI0, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, PSSI_D7, SAI2_MCLK_B, FMC_D15/FMC_AD15, DCMIPP_D7, EVENTOUT	-
E3	D9	D7	C5	-	D7	-	-	D7	-	F9	F9	-	-	-	VDD	S	-	-	-	-
E4	D2	D2	D11	C9	D5	-	-	D2	R4	A15	A15	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	F3	F3	-	-	-	PG11	I/O	FT_h	-	LPTIM1_IN2, SPI1_SCK/I2S1_CK, SPDIFRX_IN0, PSSI_D3, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, FMC_D28, DCMIPP_D3, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	-	-	-	-	-	-	-	-	F2	F2	-	-	-	PG12	I/O	FT_h	-	LPTIM1_IN1, SPI6_MISO/I2S6_SDI, SPDIFRX_IN1, SDMMC2_D3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_D29, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	G5	G5	-	-	-	PG13	I/O	FT_h	-	TRACED0, LPTIM1_CH1, SPI6_SCK/I2S6_CK, SDMMC2_D6, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_D30, LCD_CLK, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F1	F1	-	-	-	PG14	I/O	FT_h	-	TRACED1, LPTIM1_ETR, SPI6_MOSI/I2S6_SDO, SDMMC2_D7, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_D31, LCD_B1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	G4	G4	-	-	-	PG15	I/O	FT_h	-	LPTIM1_CH2, PSSI_D13, FMC_NBL3, DCMIPP_D13, EVENTOUT	-
F6	D5	E4	F3	D11	D6	11	11	D5	T1	D3	D3	-	-	-	VSS	S	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
E7	E4	F4	C10	C5	D10	12	12	D10	-	F10	F10	-	-	-	VDD	S	-	-	-	-
D2	E1	E1	D2	D2	G1	13	13	G1	H11	H2	H2	-	-	-	VSSSMPS	S	-	-	-	-
E2	F1	F1	E2	E2	G2	14	14	G2	J10	G1	G1	-	-	-	VLXSMPS	S	-	-	-	-
D1	F2	F2	D1	D1	H2	15	15	H2	K11	H1	H1	-	-	-	VDDSMPS	S	-	-	-	-
E1	F3	F3	E1	E1	H1	16	16	H1	L10	G2	G2	-	-	-	VFBSMPS	S	-	-	-	-
-	-	-	-	F1	H3	17	17	H3	-	G3	G3	-	-	-	PF5	I/O	FT_h	-	DCMIPP_D15, UCPD_FRSTX1, PSSI_D15, FMC_CLE, ETH_MII_RXD2, FMC_A16, EVENTOUT	-
-	-	-	F2	F2	J1	18	18	J1	-	H5	H5	-	-	-	PF6	I/O	FT_h	-	TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, FMC_ALE, FMC_A17, EVENTOUT	-
-	-	-	G4	G4	J3	19	19	J3	-	H4	H4	-	-	-	PF7	I/O	FT_h	-	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, FMC_A18, LCD_G0, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	-	F1	G1	J2	20	20	J2	-	H3	H3	-	-	-	PF8	I/O	FT_h	-	TIM16_CH1N, DCMIPP_PIXCLK, SPI5_MISO, SAI1_SCK_B, UART7_RTS, PSSI_PDCK, TIM13_CH1, FMC_A19, LCD_G1, EVENTOUT	-
-	-	-	G5	G5	K2	21	21	K2	-	J2	J2	-	-	-	PF9	I/O	FT_h	-	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, FMC_A21, LCD_R0, EVENTOUT	-
-	-	-	-	-	K1	22	22	K1	-	J3	J3	-	-	-	PF10	I/O	FT_h	-	TIM16_BKIN, SAI1_D3, DCMIPP_D15, PSSI_D15, PSSI_D11, FMC_A22, DCMIPP_D11, LCD_R1, EVENTOUT	-
F1	G2	G2	G2	G2	L2	23	23	L2	M11	K1	K1	5	5	13	PH0-OSC_IN(PH0)	I/O	FT_h	-	EVENTOUT	OSC_IN
F2	H1	H1	G1	H1	M1	24	24	M1	P11	K2	K2	6	6	14	PH1-OSC_OUT(PH1)	I/O	FT_h	-	EVENTOUT	OSC_OUT
F3	F4	G4	H4	H4	M2	25	25	M2	K9	J4	J4	7	7	15	NRST	I/O	RST	-	-	-
F8	D7	E8	F7	F3	D8	-	-	D6	T7	D6	D6	-	-	-	VSS	-	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
H4	E7	F5	F11	F7	D11	26	26	D8	V9	E3	E3	8	8	16	VSS	S	-	-	-	-
G4	F9	F9	E11	C10	F12	27	27	F12	W10	G6	G6	9	9	17	VDD	S	-	-	-	-
G7	G4	H9	G3	E11	G4	-	-	G4	-	H6	H6	-	-	-	VDD	-	-	-	-	-
G1	G3	G3	H3	H3	N1	28	28	N1	M9	K3	K3	-	10	18	PC0	I/O	FT_h	-	GFXTIM_FCKCAL, SAI2_FS_B, FMC_NBL1, GFXTIM_LCKCAL, EVENTOUT	ADC12_INP10
H1	G5	H5	H5	H5	P1	29	29	P1	L8	L1	L1	-	11	19	PC1	I/O	FT_h	-	TRACED0, SAI1_D1, ADF1_SDI0, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, FMC_A16, SDMMC2_CK, ETH_MDC, FMC_A0, MDIOS_MDC, EVENTOUT	ADC12_INP11, ADC12_INN10, TAMP_IN7/TAMP_OUT8, WKUP4
-	J1	J1	H2	H2	P2	30	30	P2	-	L2	L2	-	-	20	PC2	I/O	FT_h	-	TIM1_CH1, SPI2_MISO/I2S2_SDI, FMC_A17, ETH_MII_TXD2, FMC_A1, EVENTOUT	ADC12_INP12, ADC12_INN11

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	H2	H2	H1	J1	N2	31	31	N2	-	L3	L3	-	-	21	PC3	I/O	FT_h	-	TIM1_CH2, SPI2_MOSI/I2S2_SDO, FMC_A18, ETH_MII_TX_CLK, FMC_A2, EVENTOUT	ADC12_INP13, ADC12_INN12
G3	H3	J3	J4	J4	L4	32	32	L4	R10	J5	J5	10	12	22	VSSA	S	-	-	-	-
F4	H5	H4	J3	J3	N3	33	33	N3	N10	K4	K4	-	13	23	VREFM	S	-	-	-	-
J1	K3	K3	K3	K3	M3	34	34	M3	U10	K5	K5	11	14	24	VREFP	S	-	-	-	-
H2	J3	H3	K4	K4	M4	35	35	M4	T11	J6	J6	12	15	25	VDDA	S	-	-	-	-
K1	K1	J2	J1	K1	R2	36	36	R2	P9	M1	M1	13	16	26	PA0	I/O	FT_h	-	TIM2_CH1, TIM5_CH1, TIM9_CH1, TIM15_BKIN, SPI6_NSS/I2S6_WS, USART2_CTS/USART2_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, FMC_AD7/FMC_D7, LCD_G3, EVENTOUT	ADC12_INP0, ADC12_INN1, WKUP1

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
G2	J2	K1	L1	L1	P3	37	37	P3	K7	M2	M2	14	17	27	PA1	I/O	FT_h	-	TIM2_CH2, TIM5_CH2, LPTIM3_IN1, TIM15_CH1N, DCMIPP_D0, PSSI_D0, USART2_RTS, UART4_RX, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, FMC_AD6/FMC_D6, LCD_G2, EVENTOUT	ADC12_INP1
J2	L1	L1	K1	M1	R3	38	38	R3	V11	L4	L4	15	18	28	PA2	I/O	FT_h	-	TIM2_CH3, TIM5_CH3, LPTIM3_IN2, TIM15_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, FMC_AD5/FMC_D5, LCD_B7, MDIOS_MDIO, EVENTOUT	ADC12_INP14, WKUP2
-	K2	K2	J5	J5	N4	39	39	N4	-	N1	N1	16	19	29	PA3	I/O	FT_h	-	TIM2_CH4, TIM5_CH4, LPTIM3_CH1, TIM15_CH2, I2S6_MCK, SPI4_RDY, USART2_RX, GFXTIM_LCKCAL, SPI5_RDY, SPI1_RDY, ETH_MII_COL, GFXTIM_FCKCAL, LCD_DE, TIM1_CH3, EVENTOUT	ADC12_INP15

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	G1	G1	G7	G6	E3	40	40	D12	-	F6	F6	-	20	30	VSS	S	-	-	-	-
-	J5	J4	K2	G3	J12	41	41	K4	-	H10	H10	-	-	31	VDD	S	-	-	-	-
K2	L2	M2	L2	L2	M5	42	42	M5	N8	M3	M3	17	21	32	PA4	I/O	FT_h	-	TIM5_ETR, LPTIM3_CH2, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS/I2S6_WS, PSSI_DE, OTG_HS_SOF, ETH_MDIO, LCD_R3, DCMIPP_HSYNC, EVENTOUT	ADC1_INP18
H3	J4	L2	L3	L3	P4	43	43	P4	J6	N2	N2	18	22	33	PA5	I/O	FT_h	-	PWR_CSTOP, TIM2_CH1, TIM2_ETR, TIM9_CH2, SPI1_SCK/I2S1_CK, PSSI_D8, SPI6_SCK/I2S6_CK, FMC_NOE, DCMIPP_D8, LCD_CLK, EVENTOUT	ADC2_INP18
-	G8	G5	G8	G7	E4	-	-	E1	-	F15	F15	-	-	-	VSS	S	-	-	-	-
-	J9	-	K10	G11	K4	-	-	M6	-	K6	K6	19	23	-	VDD	S	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
K3	M2	M3	M1	N1	R4	44	44	R4	M7	P1	P1	20	24	34	PA6	I/O	FT_h	-	PWR_CSLEEP, TIM1_BKIN, TIM3_CH1, LPTIM3_ETR, SPI1_MISO/I2S1_SDI, PSSI_PDCK, SPI6_MISO/I2S6_SDI, TIM13_CH1, MDIOS_MDC, LCD_B7, DCMIPP_PIXCLK, LCD_HSYNC, EVENTOUT	ADC12_INP3
J3	K4	L3	M2	M2	N5	45	45	N5	T9	M4	M4	21	25	35	PA7	I/O	FT_h	-	TIM1_CH1N, TIM3_CH2, SPI1_MOSI/I2S1_SDO, SPI6_MOSI/I2S6_SDO, TIM14_CH1, LCD_R4, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_INT, LCD_B1, EVENTOUT	ADC12_INP7, ADC12_INN3
-	L3	K4	N1	N2	P5	46	46	P5	-	L5	L5	-	-	36	PC4	I/O	FT_h	-	I2S1_MCK, FMC_A19, SPDIFRX_IN2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_A3, EVENTOUT	ADC12_INP4
-	M3	M4	N2	L4	R5	47	47	R5	-	N3	N3	-	-	37	PC5	I/O	FT_h	-	SAI1_D3, DCMIPP_D15, PSSI_D15, FMC_A21, SPDIFRX_IN3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_A5, EVENTOUT	ADC12_INP8, ADC12_INN4

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
F5	L4	L4	K5	K5	N6	48	48	N6	R8	P2	P2	22	26	38	PB0	I/O	FT_h	-	TIM1_CH2N, TIM3_CH3, TIM9_CH1, SPI1_SCK/I2S1_CK, UART4_CTS, ETH_MII_TXD0/ETH_RMII_TXD0, GFXTIM_TE, [RNG_S1], LCD_VSYNC, EVENTOUT	ADC12_INP9, ADC12_INN5
K4	M4	J6	M3	M3	R6	49	49	R6	L6	R2	R2	23	27	39	PB1	I/O	FT_h	-	TIM1_CH3N, TIM3_CH4, TIM9_CH2, FDCAN2_TX, LCD_G2, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_NOE, [RNG_S2], EVENTOUT	ADC12_INP5
G5	L5	L5	L4	N3	P6	50	50	P6	N6	N4	N4	24	28	40	PB2	I/O	FT_h	-	RTC_OUT2, SAI1_D1, ADF1_SDI0, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, LCD_B2, FMC_NWE, EVENTOUT	-
-	-	-	L5	K2	L12	51	51	M12	-	K8	K8	-	-	41	VDD	S	-	-	-	-
-	H4	G8	H7	G8	E12	52	52	E3	-	G8	G8	-	-	-	VSS	S	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	-	N3	M4	R7	53	53	R7	-	M5	M5	-	-	-	PF11	I/O	FT_h	-	SPI5_MOSI, PSSI_D12, SAI2_SD_B, FMC_A23, DCMIPP_D12, LCD_B0, EVENTOUT	ADC1_INP2
-	-	-	-	-	N7	-	-	N7	-	R3	R3	-	-	-	PF12	I/O	FT_h	-	USART1_RX, SPI5_MISO, FMC_D19, EVENTOUT	ADC1_INP6, ADC1_INN2
-	-	-	-	-	P7	-	-	P7	-	P3	P3	-	-	-	PF13	I/O	FT_h	-	USART1_TX, SPI5_NSS, PSSI_D10, FMC_D20, DCMIPP_D10, EVENTOUT	ADC2_INP2
-	-	-	-	-	-	-	-	-	-	P4	P4	-	-	-	PF14	I/O	FT_h	-	USART1_CTS, SPI5_MOSI, FMC_A24, LCD_G0, EVENTOUT	ADC2_INP6, ADC2_INN2
-	-	-	-	-	-	-	-	-	-	N5	N5	-	-	-	PF15	I/O	FT_h	-	USART1_RTS, SPI5_SCK, FMC_A25, LCD_G1, EVENTOUT	-
-	-	-	K6	K6	P8	54	54	P8	-	M6	M6	-	-	-	PE7	I/O	FT_h	-	TIM1_ETR, UART7_RX, FMC_A20, SAI2_SD_B, FMC_A4, EVENTOUT	-
-	-	-	M4	N4	R8	55	55	R8	-	R4	R4	-	-	-	PE8	I/O	FT_h	-	TIM1_CH1N, UART7_TX, FMC_A12, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	-	M5	J7	N8	56	56	N8	-	P5	P5	-	-	-	PE9	I/O	FT_h	-	TIM1_CH1, UART7_RTS, FMC_A14, FMC_BA0, EVENTOUT	-
-	-	-	N4	M5	N9	57	57	N9	-	R5	R5	-	-	-	PE10	I/O	FT_h	-	TIM1_CH2N, UART7_CTS, FMC_A15, FMC_BA1, EVENTOUT	-
-	-	-	-	K10	M6	58	58	-	-	K10	K10	-	-	41	VDD	S	-	-	-	-
-	G6	G6	H6	H6	J7	59	59	J7	U8	J7	J7	-	-	-	VDDLDO	S	-	-	-	-
-	H7	H7	H11	H7	F4	60	60	E4	-	G10	G10	-	-	42	VSS	S	-	-	-	-
-	H6	H6	J6	J6	K7	61	61	K7	W8	L7	L7	-	-	43	VCAP1	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	N6	-	-	-	-	PG4	I/O	FT_h	-	TIM1_BKIN2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_D22, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	P6	-	-	-	-	PG5	I/O	FT_h	-	TIM1_ETR, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_D23, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	M7	-	-	-	-	PG6	I/O	FT_h	-	TIM17_BKIN, PSSI_D12, ETH_MDC, FMC_NBL2, DCMIPP_D12, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	-	-	-	-	-	-	-	-	N7	-	-	-	-	PG7	I/O	FT_h	-	SAI1_MCLK_A, PSSI_D13, FMC_D24, DCMIPP_D13, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	P7	-	-	-	-	PG8	I/O	FT_h	-	SPI6_NSS/I2S6_WS, SPDIFRX_IN2, ETH_PPS_OUT, FMC_D25, LCD_G0, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	R7	-	-	-	-	PG9	I/O	FT_h	-	SPI1_MISO/I2S1_SDI, SPDIFRX_IN3, PSSI_RDY, SAI2_FS_B, SDMMC2_D0, FMC_D26, DCMIPP_VSYNC, EVENTOUT	-
-	-	-	-	-	-	-	-	-	U4	-	L8	-	-	-	VDDXSPI1	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	H7	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	N6	-	-	-	PP12	I/O	FT_h	-	XSPIM_P1_IO12	-
-	-	-	-	-	-	-	-	-	-	-	P6	-	-	-	PP11	I/O	FT_h	-	XSPIM_P1_IO11	-
-	-	-	-	-	-	-	-	-	-	-	N7	-	-	-	PP14	I/O	FT_h	-	XSPIM_P1_IO14	-
-	-	-	-	-	-	-	-	-	-	-	R7	-	-	-	PP13	I/O	FT_h	-	XSPIM_P1_IO13	-
J4	J6	J7	K7	K7	P9	62	62	P9	P7	P8	P7	-	29	44	PO1	I/O	FT_h	-	XSPIM_P1_NCS2	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
G6	K5	K5	K8	K8	K9	63	63	K9	V1	L8	L10	-	30	45	VDDXSPI1	S	-	-	-	-
-	K8	J5	K11	J2	F8	64	64	F4	-	H7	H8	-	31	46	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	P8	-	-	-	PP15	I/O	FT_h	-	XSPIM_P1_IO15	-
K5	M5	M5	N5	N5	R9	65	65	R9	U6	R8	R8	-	32	47	PP4	I/O	FT_h	-	XSPIM_P1_IO4	-
J5	L6	L6	M6	M6	P10	66	66	P10	R6	N8	N9	25	33	48	PP2	I/O	FT_h	-	XSPIM_P1_IO2	-
K6	M6	M6	N6	N6	R10	67	67	R10	V5	N9	P9	26	34	49	PP3	I/O	FT_h	-	XSPIM_P1_IO3	-
-	K10	K6	L6	K11	F9	68	68	F7	-	H8	H9	27	35	50	VSS	S	-	-	-	-
H5	K7	K7	L7	L7	M8	69	69	M8	V7	L10	M8	28	36	51	VDDXSPI1	S	-	-	-	-
J6	L7	L7	M7	M7	P11	70	70	P11	T5	R9	P10	-	37	52	PO5	I/O	FT_h	-	XSPIM_P1_NCLK	-
K7	M7	M7	N7	N7	R11	71	71	R11	P5	R10	R10	29	38	53	PO4	I/O	FT_h	-	XSPIM_P1_CLK	-
J7	M8	M8	M8	M8	N11	72	72	N11	N4	P10	N10	-	39	54	PP5	I/O	FT_h	-	XSPIM_P1_IO5	-
K8	L8	L8	N8	N8	R12	73	73	R12	P3	N10	P11	30	40	55	PP0	I/O	FT_h	-	XSPIM_P1_IO0	-
-	M1	K8	L8	L6	F10	74	74	F8	-	H9	H11	-	41	56	VSS	S	-	-	-	-
H7	K9	K9	L9	L9	M10	75	75	M10	-	M10	M10	-	42	57	VDDXSPI1	S	-	-	-	-
J8	M9	M9	M9	M9	P12	76	76	P12	T3	R11	R11	-	43	58	PP6	I/O	FT_h	-	XSPIM_P1_IO6	-
K9	L9	L9	N9	N9	R13	77	77	R13	V3	P11	N11	-	44	59	PO2	I/O	FT_h	-	XSPIM_P1_DQS0	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
J9	M10	M10	M10	M10	P13	78	78	P13	R2	N11	P12	-	45	60	PP7	I/O	FT_h	-	XSPIM_P1_IO7	-
K10	L10	L10	N10	N10	R14	79	79	R14	U2	P12	N12	31	46	61	PP1	I/O	FT_h	-	XSPIM_P1_IO1	-
-	M12	M1	L10	L8	G6	80	80	F9	-	H11	J1	32	47	62	VSS	S	-	-	-	-
-	-	-	-	-	-	81	81	-	-	-	-	33	48	63	VDDXSPI1	S	-	-	-	-
H8	J7	J8	K9	K9	P14	82	82	P14	N2	N12	R13	34	49	64	PO0	I/O	FT_h	-	XSPIM_P1_NCS1	-
-	-	-	-	-	-	-	-	-	-	-	P13	-	-	-	PP8	I/O	FT_h	-	XSPIM_P1_IO8	-
-	-	-	-	-	-	-	-	-	-	-	M11	-	-	-	PO3	I/O	FT_h	-	XSPIM_P1_DQS1	-
-	-	-	-	-	-	-	-	-	-	-	R14	-	-	-	PP9	I/O	FT_h	-	XSPIM_P1_IO9	-
-	-	-	-	-	-	-	-	-	-	-	M12	-	-	-	PP10	I/O	FT_h	-	XSPIM_P1_IO10	-
-	-	-	-	-	-	-	-	-	-	-	J8	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	R13	-	-	-	-	PG10	I/O	FT_h	-	SPI1_NSS/I2S1_WS, PSSI_D2, SAI2_SD_B, SDMMC2_D1, FMC_D27, DCMIPP_D2, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	J8	-	J7	N11	N12	83	-	N12	-	M11	-	-	-	65	PD8	I/O	FT_h	-	USART3_TX, SPDIFRX_IN1, ETH_MII_TX_EN/ETH_RMII_TX_EN, FMC_NBL0, LCD_R0, EVENTOUT	-
-	-	-	N11	N12	P15	84	-	-	-	P13	-	-	-	66	PD9	I/O	FT_h	-	USART3_RX, FMC_SDCLK, LCD_R1, EVENTOUT	-
-	M11	-	M11	M11	N13	85	-	-	-	R14	-	-	-	67	PD10	I/O	FT_h	-	TIM1_CH4, DCMIPP_D4, SPI4_RDY, USART3_CK, PSSI_D4, SPI5_RDY, SPI1_RDY, FMC_CLK, LCD_B0, EVENTOUT	TAMP_IN8/TAMP_OUT7
-	L11	-	-	N13	N14	86	-	-	-	M12	-	-	-	68	PD11	I/O	FT_h	-	TIM1_ETR, LPTIM2_IN2, DCMIPP_D6, USART3_CTS/USART3_NSS, PSSI_D6, SAI2_SD_A, FMC_D16, EVENTOUT	-
-	-	-	-	L5	M12	87	-	-	P1	L9	L9	-	-	69	VDD	S	-	-	-	-
-	-	M12	-	L10	G8	88	-	F10	-	J1	J10	-	-	70	VSS	S	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	K11	-	-	L11	M13	89	-	-	M5	N13	N13	-	-	71	PD12	I/O	FT_h	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, USART3_RTS, PSSI_D12, SAI2_FS_A, FMC_NE1, DCMIPP_D12, LCD_DE, EVENTOUT	-
-	L12	-	-	M12	N15	90	-	-	-	P14	P14	-	-	72	PD13	I/O	FT_h	-	LPTIM1_CH1, TIM4_CH2, UCPD_FRSTX2, SAI2_SCK_A, PSSI_D13, FMC_INT, DCMIPP_D13, EVENTOUT	-
H9	J10	J9	L11	L12	M14	91	83	N13	M3	P15	P15	35	50	73	PB10	I/O	FT_h	-	TIM2_CH3, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, ETH_MII_RX_ER, FMC_D11/FMC_AD11, LCD_G7, EVENTOUT	-
J10	K12	M11	N12	M13	M15	92	84	P15	K5	N14	N14	36	51	74	PB11	I/O	FT_h	-	TIM2_CH4, LPTIM2_ETR, I2C2_SDA, USART3_RX, ETH_MII_TX_EN/ETH_RMII_TX_EN, FMC_D10/FMC_AD10, LCD_G6, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
G9	H10	K10	J8	J8	L13	93	85	L13	L4	L12	L12	37	52	75	PB12	I/O	FT_h	-	TIM1_BKIN, LPTIM2_IN2, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, FDCAN2_RX, FMC_D9/FMC_AD9, LCD_G5, UART5_RX, EVENTOUT	-
H10	J11	L12	M12	L13	L15	94	86	N14	-	N15	N15	-	53	76	PB13	I/O	FT_h	-	TIM1_CH1N, LPTIM2_CH1, SPI2_SCK/I2S2_CK, SDMMC1_D0, USART3_CTS/USART3_NSS, PSSI_D2, FDCAN2_TX, LCD_G4, ETH_MII_RXD3, FMC_D8/FMC_AD8, DCMIPP_D2, UART5_TX, EVENTOUT	-
F9	H9	K11	J9	J9	L14	95	87	K13	L2	M13	M13	38	54	77	PB14	I/O	FT_h	-	TIM1_CH2N, TIM12_CH1, LPTIM2_CH2, USART1_TX, SPI2_MISO/I2S2_SDI, USART3_RTS, UART4_RTS, SDMMC2_D0, FMC_NE1, LCD_DE, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
G10	J12	L11	N13	K12	K15	96	88	M13	M1	M14	M14	39	55	78	PB15	I/O	FT_h	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, USART1_RX, SPI2_MOSI/I2S2_SDO, UART4_CTS, SDMMC2_D1, LCD_G7, FMC_A20, EVENTOUT	PVD_IN
G8	H8	H8	H9	H9	K10	97	89	K10	-	K11	K11	40	56	79	VCAP2	S	-	-	-	-
-	-	-	-	-	G12	98	90	G6	-	J8	J12	41	57	80	VSS	S	-	-	-	-
F7	G7	G7	H8	H8	H8	99	91	H8	-	J9	J9	-	-	-	VDDLDO	S	-	-	-	-
-	-	-	-	-	-	100	92	-	-	-	-	42	58	81	VDD	S	-	-	-	-
-	H11	-	-	K13	K13	101	-	-	-	L14	L14	-	-	82	PD14	I/O	FT_h	-	LPTIM1_CH2, TIM4_CH3, LPTIM2_CH1, DCMIPP_D7, UCPD_FRSTX1, UART8_CTS, PSSI_D7, FMC_D17, EVENTOUT	-
-	-	-	-	J10	K14	102	-	-	-	L13	L13	-	-	83	PD15	I/O	FT_h	-	TIM4_CH4, LPTIM5_OUT, DCMIPP_D9, UCPD_FRSTX2, UART8_RTS, PSSI_D9, FMC_D18, EVENTOUT	-
-	-	-	J10	-	-	-	-	-	-	L15	L15	-	-	-	PN12	I/O	FT_h	-	XSPIM_P2_NCS2	-
-	-	E10	G11	-	-	-	93	H10	-	H12	H12	-	-	-	VDDXSPI2	S	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	-	-	-	H6	-	94	G12	-	J12	K7	-	-	-	VSS	S	-	-	-	-
-	-	K12	M13	-	-	-	95	N15	-	K13	K13	-	-	-	PN8	I/O	FT_h	-	XSPIM_P2_IO4, FMC_D4/FMC_AD4	-
-	-	J11	L12	-	-	-	96	M14	-	K14	K14	-	-	-	PN4	I/O	FT_h	-	XSPIM_P2_IO2, FMC_D2/FMC_AD2	-
-	-	J12	L13	-	-	-	97	M15	-	K15	K15	-	-	-	PN5	I/O	FT_h	-	XSPIM_P2_IO3, FMC_D3/FMC_AD3	-
-	-	-	-	-	H7	-	98	H4	-	J15	K9	-	-	-	VSS	S	-	-	-	-
-	-	G10	H10	-	-	-	99	J12	-	J11	J11	-	-	-	VDDXSPI2	S	-	-	-	-
-	-	H11	K12	-	-	-	100	L14	-	J13	J13	-	-	-	PN7	I/O	FT_h	-	XSPIM_P2_NCLK, FMC_CLK	-
-	-	H12	K13	-	-	-	101	L15	-	J14	J14	-	-	-	PN6	I/O	FT_h	-	XSPIM_P2_CLK, FMC_SDCLK	-
-	-	G12	J12	-	-	-	102	K14	-	H14	H14	-	-	-	PN9	I/O	FT_h	-	XSPIM_P2_IO5, FMC_D5/FMC_AD5	-
-	-	G11	J13	-	-	-	103	K15	-	H15	H15	-	-	-	PN2	I/O	FT_h	-	XSPIM_P2_IO0, FMC_D0/FMC_AD0	-
-	-	-	-	-	H9	-	104	H6	-	K7	L6	-	-	-	VSS	S	-	-	-	-
-	-	J10	J11	-	-	-	105	L12	-	K12	K12	-	-	-	VDDXSPI2	S	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	F12	H12	-	-	-	106	J13	-	H13	H13	-	-	-	PN10	I/O	FT_h	-	XSPIM_P2_IO6, FMC_D6/FMC_AD6	-
-	-	F11	H13	-	-	-	107	J15	-	G14	G14	-	-	-	PN0	I/O	FT_h	-	XSPIM_P2_DQS0, FMC_NE4	-
-	-	E12	G12	-	-	-	108	J14	-	G15	G15	-	-	-	PN11	I/O	FT_h	-	XSPIM_P2_IO7, FMC_D7/FMC_AD7	-
-	-	E11	G13	-	-	-	109	H15	-	G13	G13	-	-	-	PN3	I/O	FT_h	-	XSPIM_P2_IO1, FMC_D1/FMC_AD1	-
-	-	-	-	-	H10	-	-	H7	-	K9	L11	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	110	-	-	-	-	-	-	-	VDDXSPI2	S	-	-	-	-
-	-	G9	G10	-	-	-	111	H14	-	F14	F14	-	-	-	PN1	I/O	FT_h	-	XSPIM_P2_NCS1, FMC_NBL0	-
-	H12	C12	F13	H10	J13	103	112	G15	-	E15	E15	-	-	84	PC6	I/O	FT_h	-	TIM3_CH1, TIM9_CH1, I2S2_MCK, SDMMC1_D0DIR, PSSI_D0, SDMMC2_D6, SDMMC1_D6, DCMIPP_D0, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	G9	D12	G9	G10	J14	104	113	G14	-	F13	F13	-	-	85	PC7	I/O	FT_h	-	TRGIO, TIM3_CH2, TIM9_CH2, I2S3_MCK, SDMMC1_D123DIR, PSSI_D1, SDMMC2_D7, SDMMC1_D7, DCMIPP_D1, EVENTOUT	-
-	G11	B12	F12	J11	J15	105	114	F15	-	D15	D15	-	-	86	PC8	I/O	FT_h	-	TRACED1, TIM3_CH3, I2C3_SMBA, UART5_RTS, PSSI_D2, SDMMC1_D0, DCMIPP_D2, EVENTOUT	-
-	G10	D11	F10	G9	H14	106	115	G13	-	E14	E14	-	-	87	PC9	I/O	FT_h	-	MCO2, TIM3_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, PSSI_D3, SDMMC1_D1, DCMIPP_D3, EVENTOUT	-
-	-	-	-	-	-	107	116	-	-	-	-	-	-	88	VDD	S	-	-	-	-
-	-	-	-	-	H12	108	-	H9	-	L6	M7	-	-	89	VSS	S	-	-	-	-
E8	F10	C11	E13	H12	G14	109	117	F14	K1	F12	F12	43	59	90	PA8	I/O	FT_h	-	MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, UART7_RX, FMC_AD4/FMC_D4, LCD_B6, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
F10	G12	A11	D13	J12	H15	110	118	E15	J2	D14	D14	44	60	91	PA9	I/O	FT_h	-	TIM1_CH2, LPUART1_TX, I2C3_SDA, SPI2_SCK/I2S2_CK, PSSI_D0, USART1_TX, FMC_AD3/FMC_D3, DCMIPP_D0, LCD_B5, EVENTOUT	-
E9	F11	D10	E12	F10	G13	111	119	F13	H1	E13	E13	45	61	92	PA10	I/O	FT_h	-	TIM1_CH3, LPUART1_RX, PSSI_D1, USART1_RX, MDIOS_MDIO, FMC_AD2/FMC_D2, DCMIPP_D1, LCD_B4, EVENTOUT	-
E10	F12	E9	C13	J13	G15	112	120	D15	K3	C15	C15	46	62	93	PA11	I/O	FT_h	-	TIM1_CH4, LPUART1_CTS, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS/USART1_NSS, FDCAN1_RX, FMC_AD1/FMC_D1, LCD_B3, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
D9	E11	B11	D12	G12	F14	113	121	E14	J4	C14	C14	47	63	94	PA12	I/O	FT_h	-	TIM1_ETR, LPUART1_RTS, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, SAI2_FS_B, FDCAN1_TX, FMC_AD0/FMC_D0, LCD_B2, EVENTOUT	-
D10	E12	B10	B13	H13	F15	114	122	D14	H3	E12	E12	48	64	95	PA13(JTMS/ SWDIO)	I/O	FT_h	-	JTMS-SWDIO, EVENTOUT	-
C9	E10	C10	C12	F12	F13	115	123	E13	G2	D13	D13	49	65	96	PA14(JTCK/ SWCLK)	I/O	FT_h	-	JTCK-SWCLK, EVENTOUT	-
C10	D12	A10	A13	G13	E15	116	124	C15	F1	G11	G11	50	66	97	PA15(JTDI)	I/O	FT_h	-	JTDI, TIM2_CH1, TIM2_ETR, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS/I2S6_WS, UART4_RTS, UART7_TX, FMC_D15/FMC_AD15, LCD_R5, EVENTOUT	-
D8	F8	F8	F9	F9	G10	117	125	G10	D1	F11	F11	51	67	98	VCAP3	S	-	-	-	-
-	-	-	-	-	H13	118	126	H12	-	L11	M9	52	68	99	VSS	S	-	-	-	-
E6	F7	F7	F8	F8	G9	119	127	G9	E2	G9	G9	-	-	-	VDDLDO	S	-	-	-	-
-	-	-	-	-	-	120	128	-	B1	-	-	53	69	100	VDD	S	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	D11	A9	A12	F13	E14	121	129	D13	F3	B14	B14	-	70	101	PC10	I/O	FT_h	-	TIM1_BKIN, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, PSSI_D14, SDMMC1_D2, DCMIPP_D14, EVENTOUT	-
-	E9	D9	E10	E12	E13	122	130	C14	G4	B15	B15	-	71	102	PC11	I/O	FT_h	-	SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, PSSI_D4, SDMMC1_D3, DCMIPP_D4, EVENTOUT	-
-	C12	-	C11	E13	D15	123	131	B15	-	D12	D12	-	72	103	PC12	I/O	FT_h	-	TRACED3, TIM1_CH4, TIM15_CH1, SPI6_SCK/I2S6_CK, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, PSSI_D9, SDMMC1_CK, DCMIPP_D9, EVENTOUT	-
-	-	B9	B12	E10	D14	124	132	B14	-	C13	C13	-	-	104	PD0	I/O	FT_h	-	PSSI_DE, FMC_A22, UART4_RX, FDCAN1_RX, FMC_A6, DCMIPP_HSYNC, EVENTOUT	-
-	-	-	B11	D13	C15	125	133	A14	-	B13	B13	-	-	105	PD1	I/O	FT_h	-	FMC_A23, UART4_TX, FDCAN1_TX, FMC_A7, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	C11	C9	E9	D12	D13	126	134	C13	-	A14	A14	-	-	106	PD2	I/O	FT_h	-	TRACED2, TIM1_ETR, TIM3_ETR, TIM15_BKIN, PSSI_D11, UART5_RX, SDMMC1_CMD, DCMIPP_D11, EVENTOUT	-
-	-	-	-	-	J6	-	-	J4	-	M9	N8	-	-	-	VSS	S	-	-	-	-
-	-	-	A11	C13	B15	127	135	A13	-	C12	C12	-	-	-	PE11	I/O	FT_h	-	TIM1_CH2, SPI4_NSS, SAI2_SD_B, LCD_VSYNC, FMC_SDNWE, EVENTOUT	-
-	-	-	E8	C12	C14	128	136	B13	-	E11	E11	-	-	-	PE12	I/O	FT_h	-	TIM1_CH3N, SPI4_SCK, SAI2_SCK_B, FMC_SDNRAS, EVENTOUT	-
-	-	-	A10	B13	B14	129	137	B12	-	B12	B12	-	-	-	PE13	I/O	FT_h	-	TIM1_CH3, SPI4_MISO, SAI2_FS_B, FMC_SDNCAS, EVENTOUT	-
-	-	-	D10	-	C13	130	138	C12	-	A13	A13	-	-	-	PE14	I/O	FT_h	-	TIM1_CH4, GFXTIM_FCKCAL, SPI4_MOSI, SAI2_MCLK_B, FMC_SDNE0, GFXTIM_LCKCAL, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	-	-	-	A14	131	139	A12	-	D11	D11	-	-	-	PE15	I/O	FT_h	-	TIM1_BKIN, GFXTIM_LCKCAL, FMC_SDCKE0, GFXTIM_FCKCAL, EVENTOUT	-
-	-	-	-	-	J8	132	140	J6	-	M15	R1	-	-	107	VSS	S	-	-	-	-
-	-	-	-	-	-	133	141	-	-	-	-	-	-	108	VDD	S	-	-	-	-
-	D10	B8	D9	C11	D12	134	142	C11	-	A12	A12	-	-	109	PD3	I/O	FT_h	-	TIM1_CH3N, SPI2_SCK/I2S2_CK, PSSI_D5, USART2_CTS/USART2_NSS, FMC_NWAIT, DCMIPP_D5, LCD_B1, EVENTOUT	-
-	B12	A8	B10	B12	A13	135	143	A11	-	C11	C11	-	-	110	PD4	I/O	FT_h	-	DCMIPP_HSYNC, PSSI_DE, USART2_RTS, ETH_PHY_INTN, FMC_NL, EVENTOUT	TAMP_IN6/TAMP_OUT3
-	-	D8	D8	D10	B13	-	144	B11	-	B11	B11	-	-	-	PG0	I/O	FT_h	-	TIM1_CH4N, LCD_R7, EVENTOUT	-
-	-	C8	B9	A13	-	-	145	C10	-	E10	E10	-	-	-	PG1	I/O	FT_h	-	LCD_R6, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
C8	E8	-	-	E9	C12	136	-	-	D3	D10	D10	-	73	111	PM0	I/O	FT_c	-	-	UCPD_CC1
B10	C10	-	-	B11	B12	137	-	-	E4	C10	C10	-	74	112	PM1	I/O	FT_c	-	-	UCPD_CC2
A10	B10	-	-	A11	C11	138	-	-	H5	B10	B10	-	75	113	PM2	I/O	FT_d	-	-	UCPD_DB1
B9	B11	-	-	A12	A12	139	-	-	F5	A10	A10	-	76	114	PM3	I/O	FT_d	-	-	UCPD_DB2
-	-	-	-	-	J10	-	-	J8	-	P9	R6	-	-	-	VSS	S	-	-	-	-
C6	A11	A7	A9	B10	B11	140	146	C9	A2	D9	D9	-	77	115	VDD50USB	S	-	-	-	-
-	-	-	-	-	-	141	147	-	-	-	-	54	78	116	VDD33USB	S	-	-	-	-
D6	D8	-	-	D8	C10	142	-	J10	C4	E8	E8	-	79	117	VSSUSB	S	-	-	-	-
B8	B9	-	-	A10	B10	143	-	-	A4	B9	B9	-	80	118	PM5	I/O	FT_u	-	-	OTG_HS_DM
A8	A9	-	-	A9	A10	144	-	-	B5	A9	A9	-	81	119	PM6	I/O	FT_u	-	-	OTG_HS_DP
B7	C8	-	-	E8	C9	145	-	K3	D5	D8	D8	-	82	120	DVDD	S	-	-	-	-
A9	B8	-	-	D9	A11	146	-	-	E6	C9	C9	-	83	121	PM8	I/O	FT_u	-	UART7_RX, OTG_HS_VBUS	-
A7	A8	-	-	C7	B9	147	-	-	C6	B8	B8	-	84	122	PM9	I/O	FT_u	-	UART7_TX, OTG_HS_ID	-
-	-	-	-	-	-	148	-	-	A8	-	-	-	85	123	VDD	S	-	-	-	-
-	-	-	-	-	K3	-	-	K6	-	R1	R9	-	-	-	VSS	S	-	-	-	-
A6	B7	A6	B8	B8	A8	149	148	B10	A6	A7	A7	55	86	124	PM12	I/O	FT_u	-	SPI5_NSS	OTG_FS_DM

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
B6	A7	B6	A8	A8	B8	150	149	A10	B7	B7	B7	56	87	125	PM11	I/O	FT_u	-	SPI5_SCK	OTG_FS_DP
A5	C7	E7	C7	B7	A9	151	150	A9	G6	C8	C8	57	88	126	PM14	I/O	FT_u	-	SPI5_MISO, OTG_FS_VBUS	-
B5	E6	D6	D7	D7	C8	152	151	B9	D7	C7	C7	58	89	127	PM13	I/O	FT_u	-	SPI5_MOSI, OTG_FS_ID	-
A4	A6	C6	E7	E7	C7	153	152	B8	F7	A6	A6	59	90	128	BOOT0	I	B	-	-	[VPP]
-	B6	A5	A7	A7	A7	154	153	A8	-	D7	D7	-	-	129	PD5	I/O	FT_h	-	TIM1_CH4N, DCMIPP_PIXCLK, PSSI_PDCK, USART2_TX, FMC_NCE, FMC_NE2, EVENTOUT	TAMP_IN5/TAMP_OUT4
-	C6	B5	B7	B6	B7	155	154	B7	-	E7	E7	-	-	130	PD6	I/O	FT_h	-	SAI1_D1, ADF1_SDI0, ETH_CLK, SPI3_MOSI/I2S3_SDO, SAI1_SCK_A, USART2_RX, PSSI_D10, FMC_INT, SDMMC2_CK, FMC_NE3, DCMIPP_D10, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	A5	A4	A6	A6	A6	156	155	A7	C8	B6	B6	-	-	131	PD7	I/O	FT_h	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK, SPI1_MOSI/I2S1_SDO, PSSI_D2, USART2_CK, SPDIFRX_IN0, SDMMC2_CMD, FMC_D8/FMC_AD8, DCMIPP_D2, EVENTOUT	-
-	-	-	B6	-	-	-	156	C7	-	C6	C6	-	-	-	PG2	I/O	FT_h	-	LCD_HSYNC, EVENTOUT	-
-	-	-	-	-	-	-	-	A6	-	A5	A5	-	-	-	PG3	I/O	FT_h	-	DCMIPP_HSYNC, PSSI_DE, ETH_PPS_OUT, FMC_D21, EVENTOUT	-
-	-	-	-	-	K6	-	-	K8	-	R6	R12	-	-	132	VSS	S	-	-	-	-
-	-	-	-	-	-	157	157	-	-	-	-	-	-	133	VDD	S	-	-	-	-
-	-	-	D6	D6	B6	158	158	B6	-	B5	B5	-	-	-	PF0	I/O	FT_h	-	I2C2_SDA, LCD_R2, FMC_A8, EVENTOUT	-
-	-	-	A5	A5	A5	159	159	A5	-	C5	C5	-	-	-	PF1	I/O	FT_h	-	I2C2_SCL, FMC_A9, EVENTOUT	-
-	-	-	B5	B5	C6	160	160	C6	-	A4	A4	-	-	-	PF2	I/O	FT_h	-	I2C2_SMBA, DCMIPP_D14, PSSI_D14, FMC_A10, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	-	-	-	A4	161	161	A4	-	A3	A3	-	-	-	PF3	I/O	FT_h	-	DCMIPP_D9, PSSI_D9, ETH_MII_CRS, FMC_A11, EVENTOUT	-
-	-	-	-	-	B5	162	162	B5	-	B4	B4	-	-	-	PF4	I/O	FT_h	-	DCMIPP_D8, PSSI_D8, ETH_MII_TX_ER, FMC_A13, EVENTOUT	-
A3	B5	C5	A4	A4	B4	163	163	B4	E8	C4	C4	60	91	134	PB3(JTDO/TRACESWO)	I/O	FT_h	-	JTDO-SWO, TIM2_CH2, LPTIM4_IN1, DCMIPP_HSYNC, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK/I2S6_CK, SDMMC2_D2, CRS_SYNC, UART7_RX, FMC_D14/FMC_AD14, LCD_R4, PSSI_DE, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
B4	C5	E6	E6	E6	C5	164	164	C5	H7	D5	D5	61	92	135	PB4(NJTRST)	I/O	FT_h	-	NJTRST, TIM16_BKIN, TIM3_CH1, LPTIM4_ETR, DCMIPP_VSYNC, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO/I2S6_SDI, SDMMC2_D3, UART7_TX, FMC_D13/FMC_AD13, LCD_R3, PSSI_RDY, EVENTOUT	-
D4	A4	B4	B4	B4	A3	165	165	A3	D9	B3	B3	62	93	136	PB5	I/O	FT_h	-	TIM17_BKIN, TIM3_CH2, LPTIM4_OUT, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, PSSI_D10, SPI3_MOSI/I2S3_SDO, SPI6_MOSI/I2S6_SDO, FDCAN2_RX, LCD_R2, ETH_PPS_OUT, FMC_D12/FMC_AD12, DCMIPP_D10, UART5_RX, EVENTOUT	-
C4	E5	E5	E5	E5	F6	166	166	F6	A10	E6	E6	63	94	137	VCAP4	S	-	-	-	-
-	-	-	-	-	K8	167	167	K12	-	R12	R15	64	95	138	VSS	S	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
E5	F6	F6	F6	F6	G7	168	168	G7	C10	G7	G7	-	-	-	VDDLDO	S	-	-	-	-
-	-	-	-	-	-	169	169	-	-	-	-	65	96	139	VDD	S	-	-	-	-
-	B4	-	A3	A3	C4	170	170	C4	-	A2	A2	-	-	140	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, LPTIM2_ETR, UART8_RX, PSSI_D2, SAI2_MCLK_A, FMC_D9/FMC_AD9, DCMIPP_D2, EVENTOUT	TAMP_IN4/TAMP_OUT5
-	B3	B3	D5	D5	B2	171	171	B2	-	C3	C3	-	-	141	PE1	I/O	FT_h	-	LPTIM1_IN2, LPTIM2_CH2, UART8_TX, PSSI_D3, FMC_D10/FMC_AD10, DCMIPP_D3, EVENTOUT	TAMP_IN3/TAMP_OUT6
-	C4	D5	B3	B3	B3	172	172	B3	-	B2	B2	-	-	142	PE2	I/O	FT_h	-	TRACECLK, ADF1_CCK0, SAI1_CK1, LPTIM5_IN1, SPI4_SCK, SAI1_MCLK_A, ETH_MII_TXD3, FMC_D11/FMC_AD11, TIM1_CH2N, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
A2	A3	A3	A2	A2	A2	173	173	A2	F9	E5	E5	-	97	143	PB6	I/O	FT_h	-	TIM16_CH1N, TIM4_CH1, I2C1_SCL/I3C1_SCL, HDMI_CEC, PSSI_D5, USART1_TX, LPUART1_TX, FDCAN2_TX, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, FMC_SDNE1, DCMIPP_D5, UART5_TX, EVENTOUT	-
B3	D4	C4	B2	B2	C3	174	174	C3	G8	D4	D4	66	98	144	PB7	I/O	FT_h	-	TIM17_CH1N, TIM4_CH2, I2C1_SDA/I3C1_SDA, DCMIPP_D1, PSSI_RDY, USART1_RX, LPUART1_RX, PSSI_D1, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_SDCKE1, DCMIPP_VSYNC, UART5_TX, EVENTOUT	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
A1	A2	A2	A1	A1	B1	175	175	B1	J8	B1	B1	67	99	1	PB8	I/O	FT_h	-	TIM16_CH1, TIM4_CH3, USART3_CK, I2C1_SCL/I3C1_SCL, PSSI_D6, SDMMC1_CKIN, UART4_RX, FDCAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMIPP_D6, FMC_D9/FMC_AD9, EVENTOUT	-
-	-	-	-	-	J9	-	-	J9	-	-	-	-	-	-	VDDLDO	S	-	-	-	-
D7	A10	B7	C8	C8	D9	-	-	D9	B3	F8	F8	-	-	-	VDD33USB	S	-	-	-	-
-	-	-	-	-	K12	-	-	L1	-	R15	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	J4	-	-	H13	-	M8	M15	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	H4	-	-	G8	-	J10	J15	-	-	-	VSS	S	-	-	-	-
-	K6	H10	J2	H11	F7	-	-	E12	-	G12	G12	-	-	-	VSS	S	-	-	-	-
H6	F5	F10	G6	F11	E1	-	-	D11	-	E9	E9	-	-	-	VSS	-	-	-	-	-
-	-	-	-	-	R15	-	-	R15	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	R1	-	-	R1	-	-	-	-	-	-	VSS	S	-	-	-	-

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Table 21. STM32H7Sxx8 pin and ball descriptions (continued)

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA100 SMPS GP	UFBGA144 SMPS GP	UFBGA144 SMPS GFx	UFBGA169 SMPS GFx	UFBGA169 SMPS GP	UFBGA176 SMPS GP	LQFP176 SMPS GP	LQFP176 SMPS GFx	UFBGA176 SMPS GFx	WLCSP101 SMPS GP	TFBGA225 OCTO SMPS	TFBGA225 HEXA SMPS	VFQFPN68 GP	LQFP100 GP	LQFP144 GP						
-	-	-	-	-	N10	-	-	N10	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	M11	-	-	M11	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	M9	-	-	M9	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	M7	-	-	M7	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	L3	-	-	L3	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	L1	-	-	-	-	-	-	-	-	-	VSS	S	-	-	-	-

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Table 22. STM32H7Sxx8 pin alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM9_CH1	TIM15_BKIN	SPI6_NSS/I2S6_WS	-	USART2_CTS/USART2_NSS	UART4_TX	SDMMC2_CMD	SAI2_SD_B	-	FMC_AD7/FMC_D7	LCD_G3	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	LPTIM3_IN1	TIM15_CH1N	DCMIPP_D0	PSSI_D0	USART2_RTS	UART4_RX	-	SAI2_MCLK_B	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	FMC_AD6/FMC_D6	LCD_G2	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	LPTIM3_IN2	TIM15_CH1	-	-	USART2_TX	SAI2_SCK_B	-		ETH_MDIO	FMC_AD5/FMC_D5	LCD_B7	MDIOS_MDIO	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	LPTIM3_CH1	TIM15_CH2	I2S6_MCK	SPI4_RDY	USART2_RX	GFXTIM_LCKCAL	SPI5_RDY	SPI1_RDY	ETH_MII_COL	GFXTIM_FCKCAL	LCD_DE	TIM1_CH3	EVENTOUT
	PA4	-	-	TIM5_ETR	LPTIM3_CH2	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	SPI6_NSS/I2S6_WS	PSSI_DE	OTG_HS_SOF	ETH_MDIO	LCD_R3	DCMIPP_HSYNC	-	EVENTOUT
	PA5	PWR_CSTOP	TIM2_CH1	TIM2_ETR	TIM9_CH2	-	SPI1_SCK/I2S1_CK	PSSI_D8	-	SPI6_SCK/I2S6_CK	-	-	-	FMC_NOE	DCMIPP_D8	LCD_CLK	EVENTOUT
	PA6	PWR_CSLEEP	TIM1_BKIN	TIM3_CH1	LPTIM3_ETR	-	SPI1_MISO/I2S1_SDI	PSSI_PDCK	-	SPI6_MISO/I2S6_SDI	TIM13_CH1	-	MDIOS_MDC	LCD_B7	DCMIPP_PIXCLK	LCD_HSYNC	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	-	-	SPI1_MOSI/I2S1_SDO	-	-	SPI6_MOSI/I2S6_SDO	TIM14_CH1	LCD_R4	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_INT	LCD_B1	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port A	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	UART7_RX	FMC_AD4/FMC_D4	LCD_B6	-	EVENTOUT
	PA9	-	TIM1_CH2	-	LPUART1_TX	I2C3_SDA	SPI2_SCK/I2S2_CK	PSSI_D0	USART1_TX	-	-	-	-	FMC_AD3/FMC_D3	DCMIPP_D0	LCD_B5	EVENTOUT
	PA10	-	TIM1_CH3	-	LPUART1_RX	-		PSSI_D1	USART1_RX	-	-	-	MDIOS_MDIO	FMC_AD2/FMC_D2	DCMIPP_D1	LCD_B4	EVENTOUT
	PA11	-	TIM1_CH4	-	LPUART1_CTS	-	SPI2_NSS/I2S2_WS	UART4_RX	USART1_CTS/USART1_NSS	-	FDCAN1_RX	-	-	FMC_AD1/FMC_D1	LCD_B3	-	EVENTOUT
	PA12	-	TIM1_ETR	-	LPUART1_RTS	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS	SAI2_FS_B	FDCAN1_TX	-	-	FMC_AD0/FMC_D0	LCD_B2	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	HDMI_CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS/I2S6_WS	UART4_RTS	-	-	UART7_TX	FMC_D15/FMC_AD15	LCD_R5	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM9_CH1	-	SPI1_SCK/I2S1_CK	-	-	UART4_CTS	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	GFXTIM_TE	-	LCD_VSYNC	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM9_CH2	-	-	-	-	-	FDCAN2_TX	LCD_G2	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_NOE	-	-	EVENTOUT
	PB2	RTC_OUT2	-	SAI1_D1	ADF1_SDI0	-	-	SAI1_SD_A	SPI3_MOSI/I2S3_SDO	-	-	LCD_B2		FMC_NWE	-	-	EVENTOUT
	PB3	JTDO-SWO	TIM2_CH2	-	LPTIM4_IN1	DCMIPP_HSYNC	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK/I2S6_CK	SDMMC2_D2	CRS_SYNC	UART7_RX	FMC_D14/FMC_AD14	LCD_R4	PSSI_DE	EVENTOUT
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	LPTIM4_ETR	DCMIPP_VSYNC	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/I2S2_WS	SPI6_MISO/I2S6_SDI	SDMMC2_D3	-	UART7_TX	FMC_D13/FMC_AD13	LCD_R3	PSSI_RDY	EVENTOUT
	PB5	-	TIM17_BKIN	TIM3_CH2	LPTIM4_OUT	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	PSSI_D10	SPI3_MOSI/I2S3_SDO	SPI6_MOSI/I2S6_SDO	FDCAN2_RX	LCD_R2	ETH_PPS_OUT	FMC_D12/FMC_AD12	DCMIPP_D10	UART5_RX	EVENTOUT
	PB6	-	TIM16_CH1N	TIM4_CH1	-	I2C1_SCL/I3C1_SCL	HDMI_CEC	PSSI_D5	USART1_TX	LPUART1_TX	FDCAN2_TX	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	FMC_SDNE1	DCMIPP_D5	UART5_TX	EVENTOUT
	PB7	-	TIM17_CH1N	TIM4_CH2	-	I2C1_SDA/I3C1_SDA	DCMIPP_D1	PSSI_RDY	USART1_RX	LPUART1_RX	PSSI_D1	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_SDCKE1	DCMIPP_VSYNC	UART5_TX	EVENTOUT
	PB8	-	TIM16_CH1	TIM4_CH3	USART3_CK	I2C1_SCL/I3C1_SCL	-	PSSI_D6	SDMMC1_CKIN	UART4_RX	FDCAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC1_D4	DCMIPP_D6	FMC_D9/FMC_AD9	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port B	PB9	-	TIM17_CH1	TIM4_CH4	-	I2C1_SDA/I3C1_SDA	SPI2_NSS/I2S2_WS	PSSI_D7	SDMMC1_CDIR	UART4_TX	FDCAN1_TX	SDMMC2_D5		SDMMC1_D5	DCMIPP_D7	-	EVENTOUT
	PB10	-	TIM2_CH3	-	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	-	USART3_TX	-	-	-	ETH_MII_RX_ER	FMC_D11/FMC_AD11	LCD_G7	-	EVENTOUT
	PB11	-	TIM2_CH4	-	LPTIM2_ETR	I2C2_SDA	-	-	USART3_RX	-	-	-	ETH_MII_TX_EN/ETH_RMII_TX_EN	FMC_D10/FMC_AD10	LCD_G6	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	LPTIM2_IN2	I2C2_SMBA	SPI2_NSS/I2S2_WS	-	USART3_CK	-	FDCAN2_RX	-	-	FMC_D9/FMC_AD9	LCD_G5	UART5_RX	EVENTOUT
	PB13	-	TIM1_CH1N	-	LPTIM2_CH1	-	SPI2_SCK/I2S2_CK	SDMMC1_D0	USART3_CTS/UART3_NSS	PSSI_D2	FDCAN2_TX	LCD_G4	ETH_MII_RXD3	FMC_D8/FMC_AD8	DCMIPP_D2	UART5_TX	EVENTOUT
	PB14	-	TIM1_CH2N	TIM12_CH1	LPTIM2_CH2	USART1_TX	SPI2_MISO/I2S2_SDI	-	USART3_RTS	UART4_RTS	SDMMC2_D0	-	-	FMC_NE1	LCD_DE	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	-	USART1_RX	SPI2_MOSI/I2S2_SDO	-	-	UART4_CTS	SDMMC2_D1	LCD_G7	-	FMC_A20	-	-	EVENTOUT
Port C	PC0	-	-	GFXTIM_FCKCAL	-	-	-	-	-	SAI2_FS_B	-	-	-	FMC_NBL1	GFXTIM_LCKCAL	-	EVENTOUT
	PC1	TRACED0	-	SAI1_D1	ADF1_SDI0	-	SPI2_MOSI/I2S2_SDO	SAI1_SD_A	FMC_A16	-	SDMMC2_CK	-	ETH_MDC	FMC_A0	-	MDIOS_MDC	EVENTOUT
	PC2	-	TIM1_CH1	-	-	-	SPI2_MISO/I2S2_SDI	-	-	-	FMC_A17	-	ETH_MII_TXD2	FMC_A1	-	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port C	PC3	-	TIM1_CH2	-	-	-	SPI2_MOSI/I2S2_SDO	-	FMC_A18	-	-	-	ETH_MII_TX_CLK	FMC_A2	-	-	EVENTOUT
	PC4	-	-	-	-	-	I2S1_MCK	-	FMC_A19	-	SPDIFRX_IN2	-	ETH_MII_RXD0/ETH_RMII_RXD0	FMC_A3	-	-	EVENTOUT
	PC5	-	-	SAI1_D3	-	DCMIPP_D15	-	PSSI_D15	FMC_A21	-	SPDIFRX_IN3	-	ETH_MII_RXD1/ETH_RMII_RXD1	FMC_A5	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM9_CH1	-	I2S2_MCK	-	-	SDMMC1_D0DIR	PSSI_D0	SDMMC2_D6	SDMMC1_D6	-	DCMIPP_D0	-	EVENTOUT
	PC7	TRGIO	-	TIM3_CH2	TIM9_CH2	-	-	I2S3_MCK	-	SDMMC1_D123DIR	PSSI_D1	SDMMC2_D7	SDMMC1_D7	-	DCMIPP_D1	-	EVENTOUT
	PC8	TRACED1	-	TIM3_CH3	-	I2C3_SMBA	-	-	-	UART5_RTS	PSSI_D2	-	SDMMC1_D0	-	DCMIPP_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	-	I2C3_SDA	I2S_CKIN	-	-	UART5_CTS	PSSI_D3	-	SDMMC1_D1	-	DCMIPP_D3	-	EVENTOUT
	PC10	-	TIM1_BKIN	-	-	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	PSSI_D14	-	-	SDMMC1_D2	DCMIPP_D14	-	EVENTOUT
	PC11	-		-	-	-	-	SPI3_MISO/I2S3_SDI	USART3_RX	UART4_RX	PSSI_D4	-	SDMMC1_D3	-	DCMIPP_D4	-	EVENTOUT
	PC12	TRACED3	TIM1_CH4	TIM15_CH1	-	-	SPI6_SCK/I2S6_CK	SPI3_MOSI/I2S3_SDO	USART3_CK	UART5_TX	PSSI_D9	-	SDMMC1_CK	-	DCMIPP_D9	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port C	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port D	PD0	-	-	-	-	-	-	PSSI_DE	FMC_A22	UART4_RX	FDCAN1_RX	-	-	FMC_A6	DCMIPP_HSYNC	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	FMC_A23	UART4_TX	FDCAN1_TX	-	-	FMC_A7	-	-	EVENTOUT
	PD2	TRACED2	TIM1_ETR	TIM3_ETR	-	TIM15_BKIN		PSSI_D11		UART5_RX			SDMMC1_CMD		DCMIPP_D11	-	EVENTOUT
	PD3	-	TIM1_CH3N	-	-	-	SPI2_SCK/I2S2_CK	PSSI_D5	USART2_CTS/USART2_NSS	-	-	-		FMC_NWAIT	DCMIPP_D5	LCD_B1	EVENTOUT
	PD4	-		-	-	-	DCMIPP_HSYNC	PSSI_DE	USART2_RTS	-	-	-	ETH_PHY_INTN	FMC_NL	-	-	EVENTOUT
	PD5	-	TIM1_CH4N	-	-	-	DCMIPP_PIXCLK	PSSI_PDCK	USART2_TX	-	-	FMC_NCE		FMC_NE2	-	-	EVENTOUT
	PD6	-	-	SAI1_D1	ADF1_SDI0	ETH_CLK	SPI3_MOSI/I2S3_SDO	SAI1_SCK_A	USART2_RX	-	PSSI_D10	FMC_INT	SDMMC2_CK	FMC_NE3	DCMIPP_D10	-	EVENTOUT
	PD7	-	-	-	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	SPI1_MOSI/I2S1_SDO	PSSI_D2	USART2_CK	-	SPDIFRX_IN0		SDMMC2_CMD	FMC_D8/FMC_AD8	DCMIPP_D2	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port D	PD8	-	-	-	-	-	-	-	USART3_TX	-	SPDIFRX_IN1	-	ETH_MII_TX_EN/ETH_RMII_TX_EN	FMC_NBL0	LCD_R0	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FMC_SDCLK	LCD_R1	-	EVENTOUT
	PD10	-	TIM1_CH4	-	-	-	DCMIPP_D4	SPI4_RDY	USART3_CK	PSSI_D4	SPI5_RDY	SPI1_RDY	-	FMC_CLK	LCD_B0	-	EVENTOUT
	PD11	-	TIM1_ETR	-	LPTIM2_IN2	-	DCMIPP_D6	-	USART3_CTS/USART3_NSS	PSSI_D6	-	SAI2_SD_A	-	FMC_D16	-	-	EVENTOUT
	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	-	-	-	USART3_RTS	-	PSSI_D12	SAI2_FS_A	-	FMC_NE1	DCMIPP_D12	LCD_DE	EVENTOUT
	PD13	-	LPTIM1_CH1	TIM4_CH2	-	-	-	UCPD_FRSTX2	-	SAI2_SCK_A	PSSI_D13	FMC_INT	-		DCMIPP_D13	-	EVENTOUT
	PD14	-	LPTIM1_CH2	TIM4_CH3	LPTIM2_CH1	-	DCMIPP_D7	UCPD_FRSTX1	-	UART8_CTS	PSSI_D7	-	-	FMC_D17	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	LPTIM5_OUT	-	DCMIPP_D9	UCPD_FRSTX2	-	UART8_RTS	PSSI_D9	-	-	FMC_D18	-	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port E	PE0	-	LPTIM1_ETR	TIM4_ETR	LPTIM2_ETR	-	-	-	-	UART8_RX	PSSI_D2	SAI2_MCLK_A	-	FMC_D9/FMC_AD9	DCMIPP_D2	-	EVENTOUT
	PE1	-	LPTIM1_IN2	-	LPTIM2_CH2	-	-	-	-	UART8_TX	PSSI_D3	-	-	FMC_D10/FMC_AD10	DCMIPP_D3	-	EVENTOUT
	PE2	TRACECLK	ADF1_CCK0	SAI1_CK1	LPTIM5_IN1	-	SPI4_SCK	SAI1_MCLK_A		-	-	-	ETH_MII_TXD3	FMC_D11/FMC_AD11	-	TIM1_CH2N	EVENTOUT
	PE3	TRACED0	-	-	LPTIM5_ETR	TIM15_BKIN		SAI1_SD_B	-	-	-	-	ETH_MII_RXD3	FMC_D12/FMC_AD12	-	-	EVENTOUT
	PE4	TRACED1	-	SAI1_D2	ADF1_SDI0	TIM15_CH1N	SPI4_NSS	SAI1_FS_A	-	-	PSSI_D4		-	FMC_D13/FMC_AD13	DCMIPP_D4	-	EVENTOUT
	PE5	TRACED2	ADF1_CCK1	SAI1_CK2		TIM15_CH1	SPI4_MISO	SAI1_SCK_A	-	-	PSSI_D6		-	FMC_D14/FMC_AD14	DCMIPP_D6	-	EVENTOUT
	PE6	TRACED3	TIM1_BKIN2	SAI1_D1	ADF1_SDI0	TIM15_CH2	SPI4_MOSI	SAI1_SD_A	-	-	PSSI_D7	SAI2_MCLK_B	-	FMC_D15/FMC_AD15	DCMIPP_D7	-	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	-	UART7_RX	-	FMC_A20	SAI2_SD_B	-	FMC_A4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	-	UART7_TX	-	-	-	-	FMC_A12	-	-	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	-	UART7_RTS	-	-	-	-	FMC_A14	-	FMC_BA0	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	UART7_CTS	-	-	-	-	FMC_A15	-	FMC_BA1	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS	-	-	-	-	SAI2_SD_B	LCD_VSYNC	FMC_SDNWE	-	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port E	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	-	-	-	-	SAI2_SCK_B	-	FMC_SDNRAS	-	-	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	-	-	-	-	SAI2_FS_B	-	FMC_SDNCAS	-	-	EVENTOUT
	PE14	-	TIM1_CH4	GFXTIM_FCKCAL	-	-	SPI4_MOSI	-	-	-	-	SAI2_MCLK_B	-	FMC_SDNE0	GFXTIM_LCKCAL	-	EVENTOUT
	PE15	-	TIM1_BKIN	GFXTIM_LCKCAL	-	-	-	-	-	-	-	-	-	FMC_SDCKE0	GFXTIM_FCKCAL	-	EVENTOUT
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	LCD_R2	FMC_A8	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-		FMC_A9	-	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port F	PF2	-	-	-	-	I2C2_SMBA	DCMIPP_D14	-	-	-	PSSI_D14	-	-	FMC_A10	-	-	EVENTOUT
	PF3	-	-	-	-	-	DCMIPP_D9	-	-	-	PSSI_D9	-	ETH_MII_CRS	FMC_A11	-	-	EVENTOUT
	PF4	-	-	-	-	-	DCMIPP_D8	-	-	-	PSSI_D8	-	ETH_MII_TX_ER	FMC_A13	-	-	EVENTOUT
	PF5	-	-	-	-	-	DCMIPP_D15	UCPD_FRSTX1	-	-	PSSI_D15	FMC_CLE	ETH_MII_RXD2	FMC_A16	-	-	EVENTOUT
	PF6	-	TIM16_CH1	-	-	-	SPI5_NSS	SAI1_SD_B	UART7_RX	-	-	FMC_ALE		FMC_A17	-	-	EVENTOUT
	PF7	-	TIM17_CH1	-	-	-	SPI5_SCK	SAI1_MCLK_B	UART7_TX	-	-	-	-	FMC_A18	LCD_G0	-	EVENTOUT
	PF8	-	TIM16_CH1N	-	-	DCMIPP_PIXCLK	SPI5_MISO	SAI1_SCK_B	UART7_RTS	PSSI_PDCK	TIM13_CH1	-	-	FMC_A19	LCD_G1	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port F	PF9	-	TIM17_CH1N	-	-	-	SPI5_MOSI	SAI1_FS_B	UART7_CTS	-	TIM14_CH1	-	-	FMC_A21	LCD_R0	-	EVENTOUT
	PF10	-	TIM16_BKIN	SAI1_D3	-	DCMIPP_D15	-	PSSI_D15	-	-	PSSI_D11	-	-	FMC_A22	DCMIPP_D11	LCD_R1	EVENTOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	PSSI_D12	SAI2_SD_B	-	FMC_A23	DCMIPP_D12	LCD_B0	EVENTOUT
	PF12	-	-	-	-	USART1_RX	SPI5_MISO	-	-	-	-	-	-	FMC_D19	-	-	EVENTOUT
	PF13	-	-	-	-	USART1_TX	SPI5_NSS	-	-	-	PSSI_D10	-	-	FMC_D20	DCMIPP_D10	-	EVENTOUT
	PF14	-	-	-	-	USART1_CTS	SPI5_MOSI	-	-	-	-	-	-	FMC_A24	LCD_G0	-	EVENTOUT
	PF15	-	-	-	-	USART1_RTS	SPI5_SCK	-	-	-	-	-	-	FMC_A25	LCD_G1	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port G	PG0	-	TIM1_CH4N	-	-	-	-	-	-	-	-	-	-	-	LCD_R7	-	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	-	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	-	EVENTOUT
	PG3	-	-	-	-	-	DCMIPP_HSYNC	-	-	-	PSSI_DE		ETH_PPS_OUT	FMC_D21	-	-	EVENTOUT
	PG4	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-	ETH_MII_RXD0/ETH_RMII_RXD0	FMC_D22	-	-	EVENTOUT
	PG5	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	ETH_MII_RXD1/ETH_RMII_RXD1	FMC_D23	-	-	EVENTOUT
	PG6	-	TIM17_BKIN	-	-	-	-				PSSI_D12	-	ETH_MDC	FMC_NBL2	DCMIPP_D12	-	EVENTOUT
	PG7	-	-	-	-	-	-	SAI1_MCLK_A	-	-	PSSI_D13	-		FMC_D24	DCMIPP_D13	-	EVENTOUT
	PG8	-	-	-	-	-	SPI6_NSS/I2S6_WS	-	-	SPDIFRX_IN2	-	-	ETH_PPS_OUT	FMC_D25	LCD_G0	-	EVENTOUT
	PG9	-	-	-	-	-	SPI1_MISO/I2S1_SDI	-	-	SPDIFRX_IN3	PSSI_RDY	SAI2_FS_B	SDMMC2_D0	FMC_D26	DCMIPP_VSYNC	-	EVENTOUT
	PG10	-	-	-	-	-	SPI1_NSS/I2S1_WS	-	-		PSSI_D2	SAI2_SD_B	SDMMC2_D1	FMC_D27	DCMIPP_D2	-	EVENTOUT

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port G	PG11	-	LPTIM1_IN2	-	-	-	SPI1_SCK/I2S1_CK	-	-	SPDIFRX_IN0	PSSI_D3	SDMMC2_D2	ETH_MII_TX_EN/ETH_RMII_TX_EN	FMC_D28	DCMIPP_D3	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port M	PM0	-	-	-	-	-	-	UCPD_CC1	-	-	-	-	-	-	-	-	-
	PM1	-	-	-	-	-	-	UCPD_CC2	-	-	-	-	-	-	-	-	-
	PM2	-	-	-	-	-	-	UCPD_DB1	-	-	-	-	-	-	-	-	-
	PM3	-	-	-	-	-	-	UCPD_DB2	-	-	-	-	-	-	-	-	-
	PM5	-	-	-	-	-	-	-	-	-	-	OTG_HS_DM	-	-	-	-	-
	PM6	-	-	-	-	-	-	-	-	-	-	OTG_HS_DP	-	-	-	-	-
	PM8	-	-	-	-	-	-	-	UART7_RX	-	-	OTG_HS_VBUS	-	-	-	-	-
	PM9	-	-	-	-	-	-	-	UART7_TX	-	-	OTG_HS_ID	-	-	-	-	-
	PM11	-	-	-	-	-	SPI5_SCK	-	-	-	-	OTG_FS_DP	-	-	-	-	-
	PM12	-	-	-	-	-	SPI5_NSS	-	-	-	-	OTG_FS_DM	-	-	-	-	-

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port M	PM13	-	-	-	-	-	SPI5_MOSI	-	-	-	-	OTG_FS_ID	-	-	-	-	-
	PM14	-	-	-	-	-	SPI5_MISO	-	-	-	-	OTG_FS_VBUS	-	-	-	-	-
Port N	PN0	-	-	-	-	-	-	-	-	-	XSPIM_P2_DQS0	-	-	FMC_NE4	-	-	-
	PN1	-	-	-	-	-	-	-	-	-	XSPIM_P2_NCS1	-	-	FMC_NBL0	-	-	-
	PN2	-	-	-	-	-	-	-	-	-	XSPIM_P2_IO0	-	-	FMC_D0/FMC_AD0	-	-	-
	PN3	-	-	-	-	-	-	-	-	-	XSPIM_P2_IO1	-	-	FMC_D1/FMC_AD1	-	-	-
	PN4	-	-	-	-	-	-	-	-	-	XSPIM_P2_IO2	-	-	FMC_D2/FMC_AD2	-	-	-
	PN5	-	-	-	-	-	-	-	-	-	XSPIM_P2_IO3	-	-	FMC_D3/FMC_AD3	-	-	-
	PN6	-	-	-	-	-	-	-	-	-	XSPIM_P2_CLK	-	-	FMC_SDCLK	-	-	-
	PN7	-	-	-	-	-	-	-	-	-	XSPIM_P2_NCLK	-	-	FMC_CLK	-	-	-
	PN8	-	-	-	-	-	-	-	-	-	XSPIM_P2_IO4	-	-	FMC_D4/FMC_AD4	-	-	-

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port N	PN9	-	-	-	-	-	-	-	-	-	XSPIM_P2_IO5	-	-	FMC_D5/FMC_AD5	-	-	-
	PN10	-	-	-	-	-	-	-	-	-	XSPIM_P2_IO6	-	-	FMC_D6/FMC_AD6	-	-	-
	PN11	-	-	-	-	-	-	-	-	-	XSPIM_P2_IO7	-	-	FMC_D7/FMC_AD7	-	-	-
	PN12	-	-	-	-	-	-	-	-	-	XSPIM_P2_NCS2	-	-	-	-	-	-
Port O	PO0	-	-	-	-	-	-	-	-	-	XSPIM_P1_NCS1	-	-	-	-	-	-
	PO1	-	-	-	-	-	-	-	-	-	XSPIM_P1_NCS2	-	-	-	-	-	-
	PO2	-	-	-	-	-	-	-	-	-	XSPIM_P1_DQS0	-	-	-	-	-	-
	PO3	-	-	-	-	-	-	-	-	-	XSPIM_P1_DQS1	-	-	-	-	-	-
	PO4	-	-	-	-	-	-	-	-	-	XSPIM_P1_CLK	-	-	-	-	-	-
	PO5	-	-	-	-	-	-	-	-	-	XSPIM_P1_NCLK	-	-	-	-	-	-

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port P	PP0	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO0	-	-	-	-	-	-
	PP1	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO1	-	-	-	-	-	-
	PP2	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO2	-	-	-	-	-	-
	PP3	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO3	-	-	-	-	-	-
	PP4	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO4	-	-	-	-	-	-
	PP5	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO5	-	-	-	-	-	-
	PP6	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO6	-	-	-	-	-	-
	PP7	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO7	-	-	-	-	-	-
	PP8	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO8	-	-	-	-	-	-
	PP9	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO9	-	-	-	-	-	-
	PP10	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO10	-	-	-	-	-	-
	PP11	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO11	-	-	-	-	-	-
	PP12	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO12	-	-	-	-	-	-
	PP13	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO13	-	-	-	-	-	-

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Table 22. STM32H7Sxx8 pin alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	ADF1/LPTIM1/TIM1/2/16/17	GFXTIM/PDM_SAI1/TIM2/3/4/5/12/15	ADF1/LPTIM2/3/4/5/LPUART1/TIM9/USART3	CEC/DCMIPP/ETH/I2C/I3C/I2C2/3/TIM15/USART1	CEC/DCMIPP/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/SPI6/I2S6	PSSI_/SAI1/SDMMC1/SPI3/I2S3/SPI4/UART4/UCPD	FMC/SDMMC1/SPI2/I2S2/SPI3/I2S3/SPI6/I2S6/UART7/USART1/2/3	GFXTIM/LPUART1/PSSI_/SAI2/SDMMC1/SPDIFRX/SPI6/I2S6/UART4/5/8	FDCAN1/2/FMC/OCTOSPIM_P1/2/PSSI_/SDMMC2/SPDIFRX/SPI5/TIM13/14	CRS/FMC/LCD/OTG1_FS/OTG1_HS/SAI2/SDMMC2/SPI1/I2S1	ETH/LCD/MDIOS/SDMMC1/2/UART7	FMC/GFXTIM/LCD/SDMMC1	DCMIPP/GFXTIM/LCD	FMC/LCD/MDIOS/PSSI_/TIM1/UART5	SYS
Port P	PP14	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO14	-	-	-	-	-	-
	PP15	-	-	-	-	-	-	-	-	-	XSPIM_P1_IO15	-	-	-	-	-	-

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5 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

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6 Electrical characteristics

The STM32H7Sxx8 uses a static voltage trimming mechanism to ensure that the maximum frequency is reached with the minimum power consumption.

This mechanism is automatically selected when using a internal power supply. The static voltage-trimming setting is die dependent, and cannot be modified. All values given in this document are derived and guaranteed for an internal supply with LDO or SMPS only, and not when a bypass mechanism is used.

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with a junction temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus four times the standard deviation (mean ±4σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.0 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±4σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 21*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 22*.

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Figure 21. Pin loading conditions

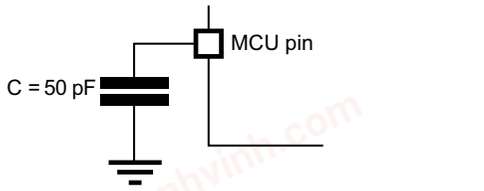
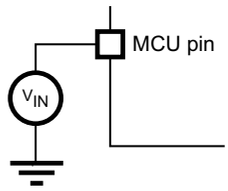


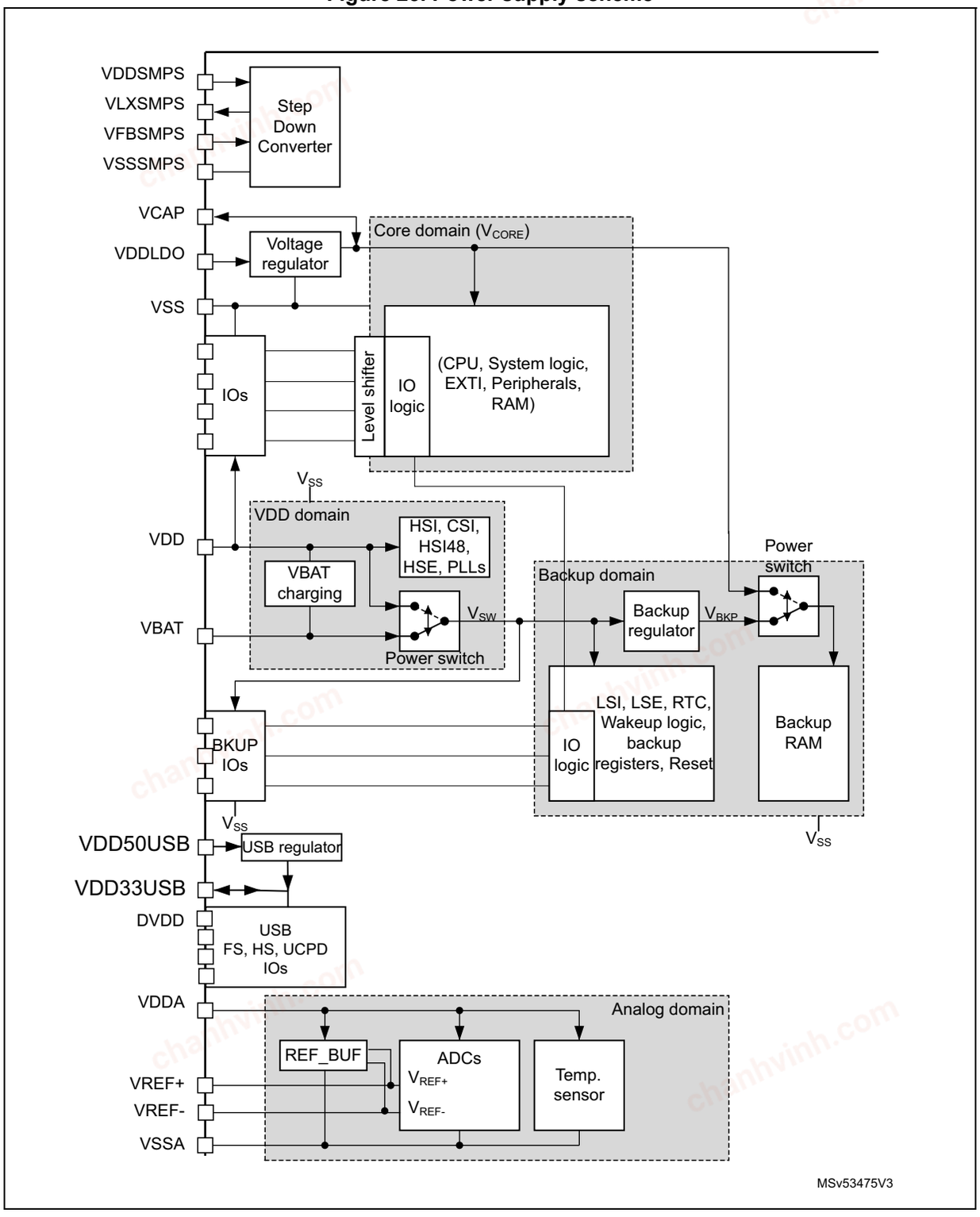
Figure 22. Pin input voltage



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6.1.6 Power supply scheme

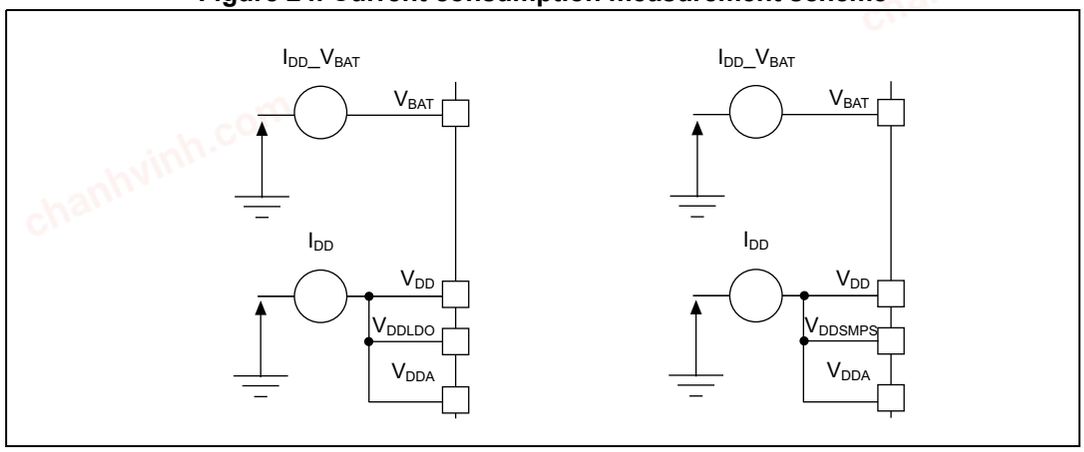
Figure 23. Power supply scheme



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6.1.7 Current consumption measurement

Figure 24. Current consumption measurement scheme



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6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 23: Voltage characteristics*, *Table 24: Current characteristics*, and *Table 25: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rat ing conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 23. Voltage characteristics

Symbols	Ratings	Min	Max	Unit
V_{DDX}-V_{SS}(1)	External main supply voltage (including V_{DD}(2)(3)(4), V_{DDSMPS}, V_{DDA}, V_{DDUSB}, $V_{DDXSPIx}$(2)(3)(4), V_{BAT}, V_{REF+})	-0.3	4.0	V
V_{DDX}-V_{SS}(3)	I/O supply when HSLV= 0	-0.3	4.0	
	I/O supply when HSLV= 1	-	2.8	
V_{IN}(5)	Input voltage on FT_xxx pins	V_{SS}−0.3	MIN (MIN (V_{DD}, V_{DDA}, V_{DDUSB}, V_{BAT}) + 4.0 V)(6)(7)	
	Input voltage on TT_xx pins	V_{SS}−0.3	4.0	
	Input voltage on BOOT0 pin	Vss	9.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\lvert\Delta V_{DDX}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50.0	mV
$\lvert V_{SSX}-V_{SS}\rvert$	Variations between all the different ground pins	-	50.0	mV
V_{ref}-V_{DDA}	Allowed voltage difference for V_{ref}+ > V_{DDA}	-	0.4	V

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{DDSMPS}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. If HSLV = 0.
3. V_{DD}, V_{DDXSP1}, or V_{DDXSP2}.
4. HSLV = High-speed low-voltage mode. Refer to General-purpose I/Os (GPIO) section of RM0477.
5. V_{IN} maximum must always be respected. Refer to Table xx: Current characteristics for the maximum allowed injected current values.
6. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
7. To sustain a voltage higher than 4V the internal pull-up/pull-down resistors must be disabled.

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Table 24. Current characteristics

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	620	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	620	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk or sourced by any I/O and control pin, except Pxy_C	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST and B pins	-5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 23: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 25. Thermal characteristics

Symbol	Ratings		Value	Unit
T_{STG}	Storage temperature range		-65 to +150	°C
T_J	Maximum junction temperature	Industrial temperature range 6	125(1)	

1. The junction temperature is limited to 105 °C in the VOS high voltage range.

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6.3 Operating conditions

6.3.1 General operating conditions

Table 26. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	HSLV=0	1.71(1)	-	3.6	V
		HSLV=1	1.71(1)	-	2.7	
V_{DDLDO}	Supply voltage for the internal regulator.	-	1.71(1)	-	3.6	
V_{DDSMPS}(2)	Supply voltage for the internal SMPS step-down converter		1.71(1)	-	3.6	
$V_{DDXSPIx}$	Octo and HexaSPI supply	HSLV=0	1.71	-	3.6	
		HSLV=1	1.08	-	2.7	
$V_{DD50USB}$(2)	USB suply voltage	USB regulator ON	4.0	5.0	5.5	
		USB regulator OFF	$V_{DD33USB}$			
$V_{DD33USB}$	USB suply voltage	USB used	3.0	-	3.6	
		USB not used	0	-	3.6	
V_{DDA}	Analog operating voltage	ADC used	1.62	-	3.6	
		VREFBUF used	2.10	-		
		ADC, VREFBUF not used	0	-		
V_{BAT}	Supply voltage for backup domain	-	1.2(3)	-	3.6	
V_{IN}	I/O Input voltage	BOOT0	-0.3	-	9.0	
		All IOs except BOOT0	-0.3	-	MIN (V_{DD}, V_{DDA}, $V_{DD33USB}$, $V_{DDXSPIx}$, 3.6 V) <, 5.5 V(4)(5)	
V_{CORE}	Internal regulator ON (LDO or SMPS)(6)	VOS low	1.1	1.21	1.26	
		VOS high	1.1	1.36	1.4	
	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on V_{CAP} pins	VOS low	1.2	-	1.26	
		VOS high	1.37	-	1.4	
		SVOS low(7)	0.7	0.74	0.8	
		SVOS high(7)	0.95	1	1.05	

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Table 26. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
f_{CPU}	CPU clock frequency	VOS low	-	-	400	MHz
		VOS high	-	-	600	
f_{ACLK}	AXI clock frequency	VOS low	-	-	200	
		VOS high	-	-	300	
f_{HCLK}	AHB clock frequency	VOS low	-	-	200	
		VOS high	-	-	300	
F_{pclk}	APB clock frequency	VOS low	-	-	100	
		VOS high	-	-	150	
T_A	Ambient temperature for temperature range(8)	Maximum power dissipation	-40	-	85	°C
T_J	Junction temperature	VOS high	-40	-	105	

1. When RESET is released, functionality is guaranteed down to BOR level 0 minimum voltage.
2. Not available on every package.
3. V_{BAT} minimum value can be reduced to 0 V if V_{DD} is present.
4. This formula has to be applied on power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between Min (VDD, VDDA, VDD33USB, VDDXSPIx) + 3.6 V < 5.5 V.
5. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDUSB}, and $V_{DDXSPIx}$) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
6. These values are factory trimmed per die.
7. Values for Regulator ON or OFF
8. The device junction temperature must be kept below maximum T_J indicated in *Table 27: Supply voltage and maximum temperature configuration* and *Section 7.12: Package thermal characteristics*).

Table 27. Supply voltage and maximum temperature configuration

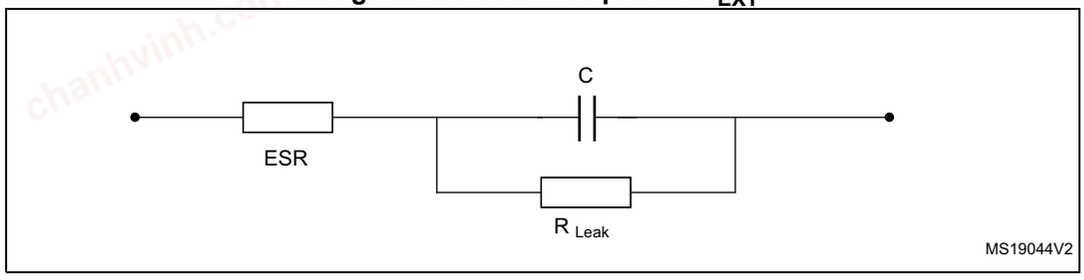
Power scale	V_{CORE} source	Max. T_J (°C)	Min. V_{DD}(V)	Min. V_{DDLDO} (V)
VOS high	LDO	105	1.71	1.71
	External (Bypass)		1.71	-
VOS low	LDO	125	1.71	1.71
	External (Bypass)		-	-
SVOS high/SVOS low	LDO	125	2	2
		105	1.71	1.71
	External (Bypass)	125	1.71	-

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6.3.2 VCAP external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP pin. C_{EXT} is specified in *Table 28*. Two external capacitors can be connected to VCAP pins.

Figure 25. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 28. VCAP operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF(2)(3)
ESR	ESR of external capacitor	< 100 mΩ

1. When bypassing the voltage regulator, the three 2.2 µF V_{CAP} capacitors are not required and should be replaced by three 100 nF decoupling capacitors.
2. This value corresponds to CEXT typical value. A variation of ±20% is tolerated.
3. If a fourth VCAP pin is available on the package, it must be connected to the other VCAP pins, but no additional capacitor is required.

6.3.3 SMPS step-down converter

The devices embed a high power efficiency SMPS step-down converter. SMPS characteristics for external usage are given in *Table 30*. The SMPS step-down converter requires external components that are fully described in AN5935 *"STM32H7R3/7S3 and STM32H7R7/7S7 MCU hardware development"*. The components used for datasheet characterization are specified in *Figure 26* and *Table 29*.

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Figure 26. External components for SMPS step-down converter

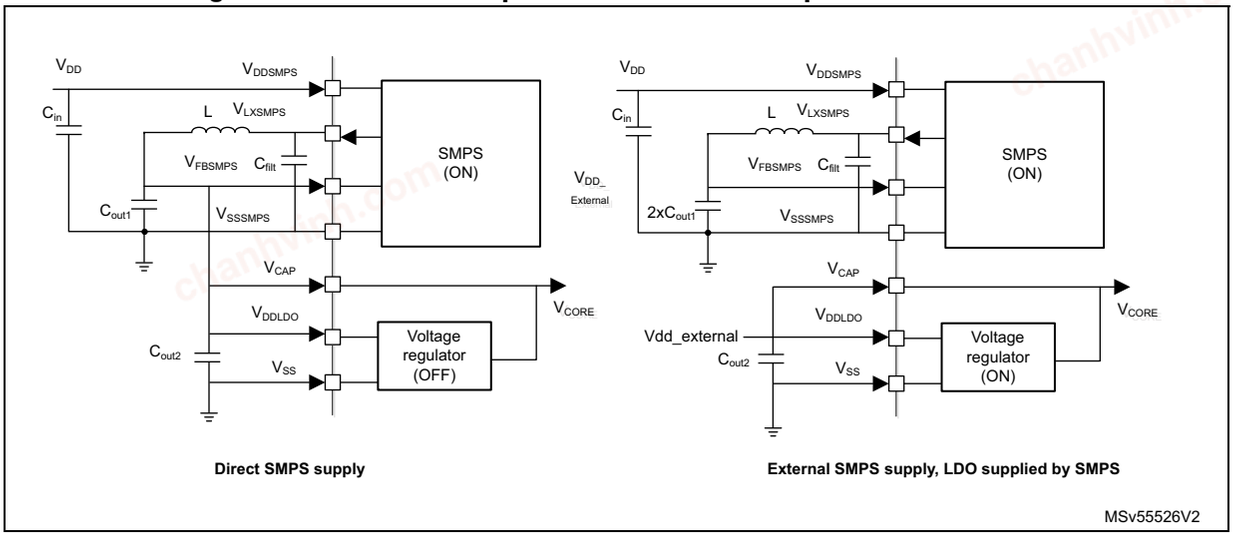


Table 29. Characteristics of SMPS step-down converter external components

Symbol	Parameter	Conditions
C_{in}	Capacitance of external capacitor on V_{DDSMPS}	4.7 µF
	ESR of external capacitor	100 mΩ
C_{filt}	Capacitance of external capacitor on V_{LXSMPS} pin	220 pF
C_{OUT}	Capacitance of external capacitor on V_{FBSMPS} pin	2x10 µF
	ESR of external capacitor	20 mΩ
L	Inductance of external Inductor on V_{LXSMPS} pin	2.2 µH
-	Serial DC resistor	150 mΩ
I_{SAT}	DC current at which the inductance drops 30% from its value without current.	1.7 A
I_{RMS}	Average current for a 40 °C rise: rated current for which the temperature of the inductor is raised 40°C by DC current	1.4 A

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Table 30. SMPS step-down converter characteristics for external usage

Parameters	Conditions	Min	Typ	Max	Unit
V_{DDSMPS}(1)	V_{OUT} = 1.8 V(2)	2.3	-	3.6	V
	V_{OUT} = 2.5 V(2)	3	-	3.6	
V_{OUT}(3)	Iout=600 mA	2.25	2.5	2.75	
		1.62	1.8	1.98	
I_{OUT}	External usage only(4)	-	-	600	mA
RDS_{ON}	-	-	100	120	mΩ
I_{DDSMPS_Q}	Quiescent current	-	220	-	µA
T_{SMPS_START}	V_{OUT} = 1.8 V	-	270	405	µs
	V_{OUT} = 2.5 V	-	360	540	

1. The switching frequency is 2.4 MHz±10%.
2. Only for bypass mode.
3. Including line transient and load transient.
4. These characteristics are given for SMPSEXTHP bit is set in the PWR_CR3 register.

Table 31. Inrush current and inrush electric charge characteristics for LDO and SMPS(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{RUSH}	Inrush current on voltage regulator power-on (POR or wakeup from Standby)	on V_{DDLDO}(3)	-	-	55	96(4)	mA
		on V_{DDSMPS}(5)	SMPS supplies the V_{DDCORE}	-	100	420(6)	
	Inrush current on voltage regulator power-on (POR)	on V_{DDSMPS}(5)	SMPS supplies external circuit, V_{OUT} = 1.8 V(7)	-	100	320(6)	
			SMPS supplies external circuit, V_{OUT} = 2.5 V(7)	-	-	240(6)	
Q_{RUSH}	Inrush charge on voltage regulator power-on (POR or wakeup from Standby)	on V_{DDLDO}(3)	-	-	4.4	5.3(4)	µC
		on V_{DDSMPS}(5)	SMPS supplies the V_{DDCORE}	-	7.3	18(6)	
	Inrush charge on voltage regulator power-on (POR)	on V_{DDSMPS}(5)	SMPS supplies external circuit, V_{OUT} = 1.8 V(7)	-	7.3	13.7(6)	
			SMPS supplies external circuit, V_{OUT} = 2.5 V(7)	-		10.5(6)	

1. The typical values are given for V_{DDLDO} = V_{DDSMPS} = 3.3 V and for typical decoupling capacitor values of C_{EXT} and C_{OUT}.
2. The product consumption (on V_{DDCORE}) is not taken into account in the inrush current and inrush electric charges.
3. The inrush current and inrush electric charge on V_{DDLDO} are not present in Bypass mode or when the SMPS supplies the V_{DDCORE}.
4. The maximum value is given for the maximum decoupling capacitor C_{EXT}.
5. The inrush current and inrush electric charges on V_{DDSMPS} are not present if the external component (L or C_{OUT}) is not present that is if the SMPS is not used.
6. The maximum value is given for the maximum decoupling capacitor C_{OUT} and the minimum V_{DDSMPS} voltage.
7. The inrush current due to transition from 1.2 V to the final V_{OUT} Value (1.8 V or 2.5 V) is not taken into account.

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Typical SMPS efficiency versus load current and temperature

Figure 27. SMPS efficiency in VOS mode T_j=25°C

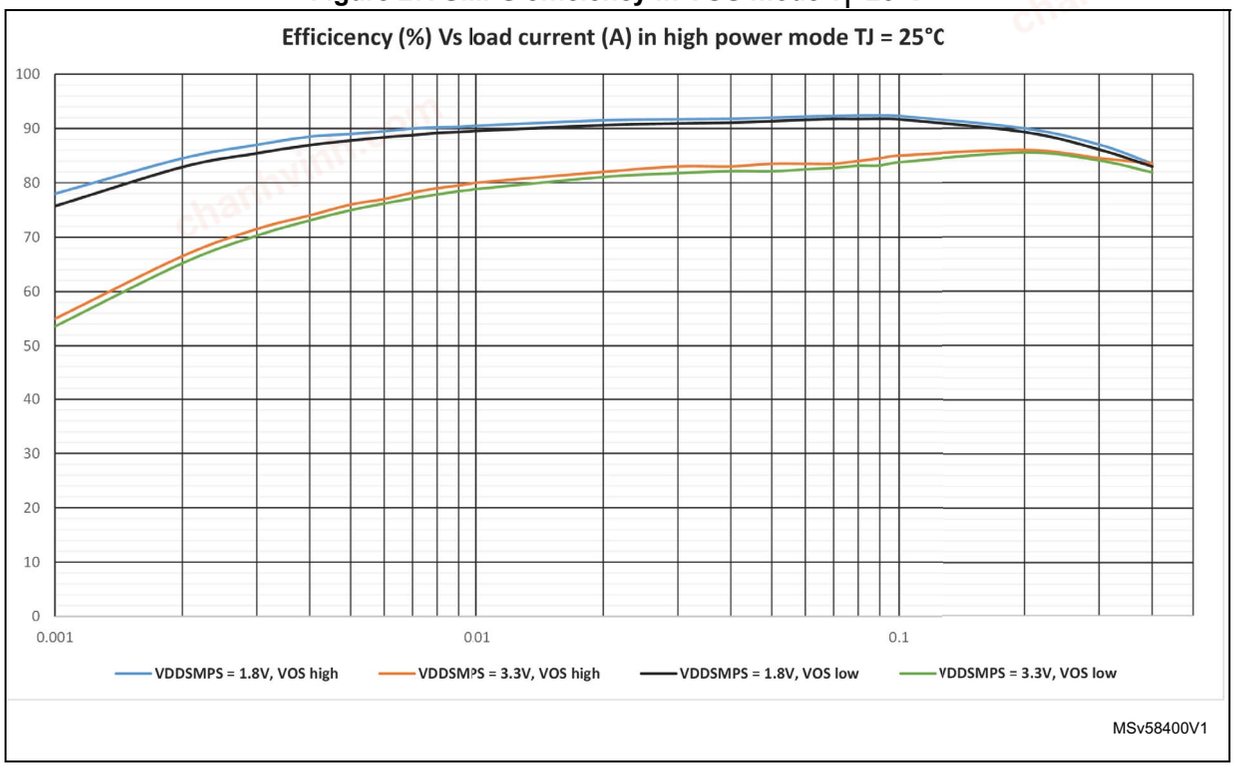
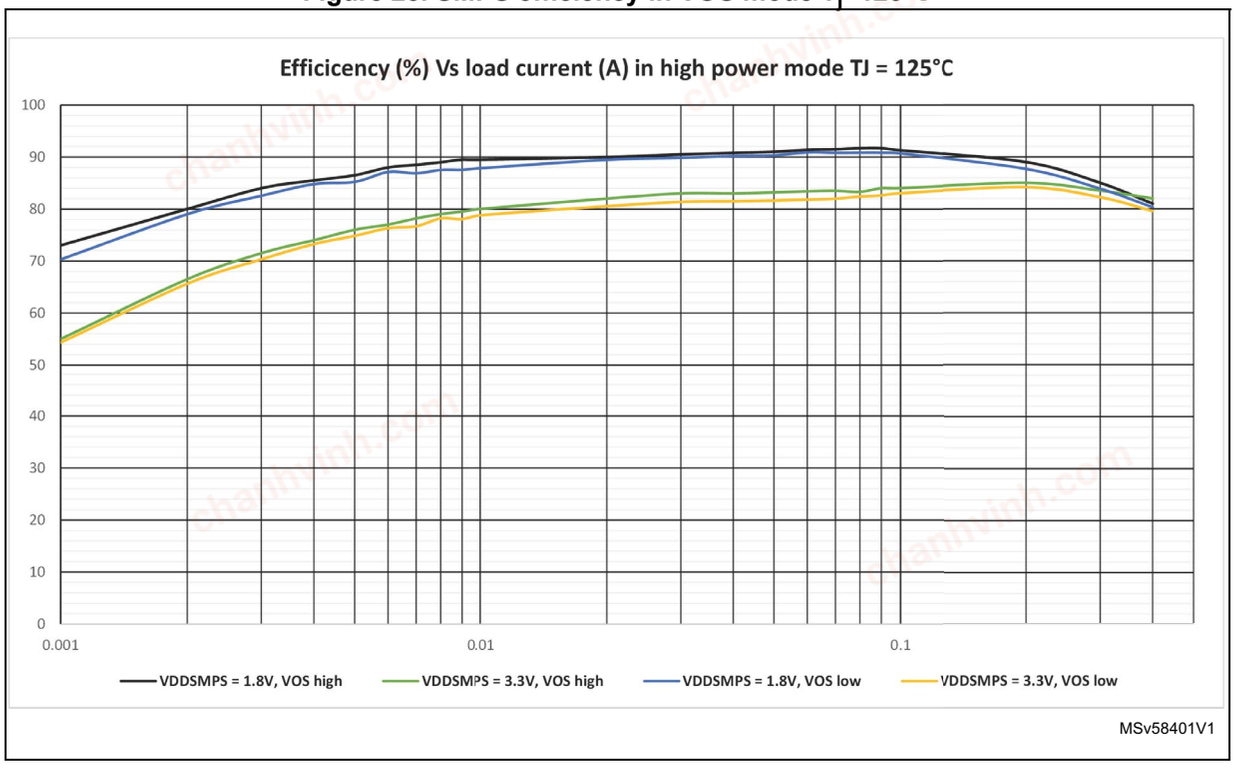


Figure 28. SMPS efficiency in VOS mode T_j=125°C



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Figure 29. SMPS efficiency in SVOS mode T_j=25°C

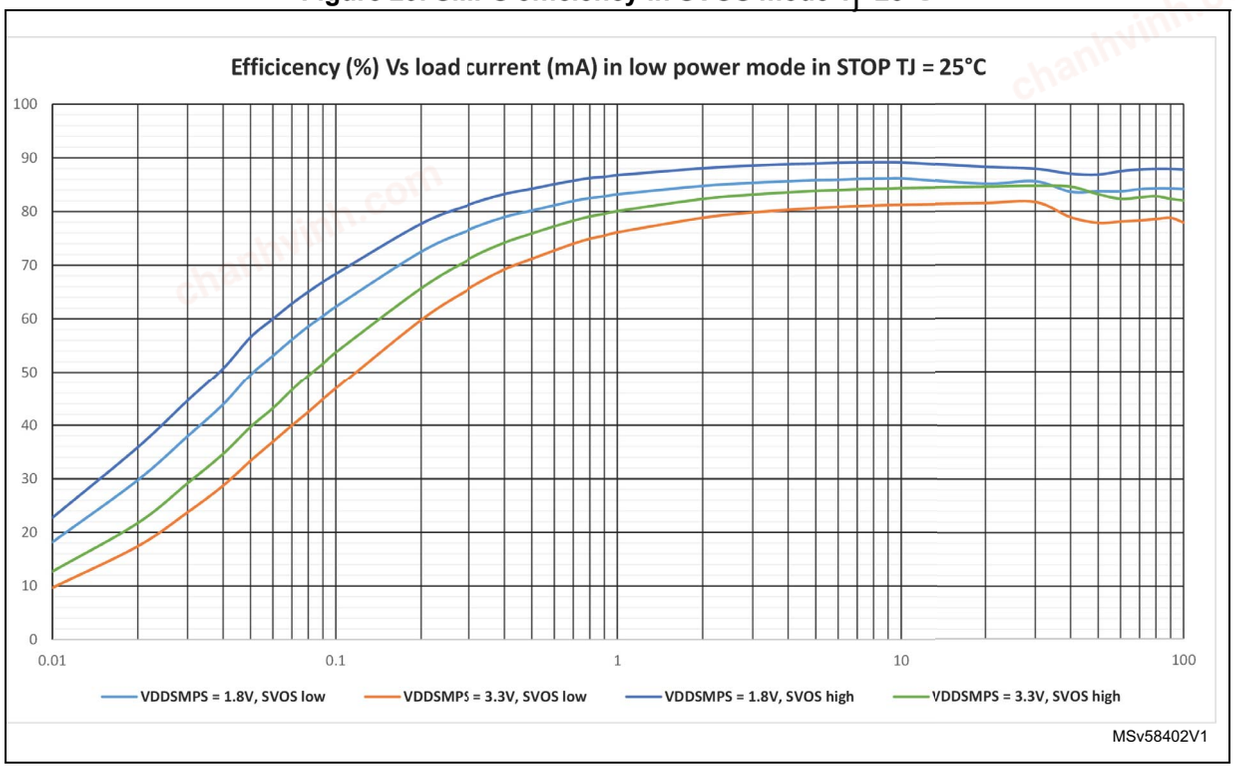
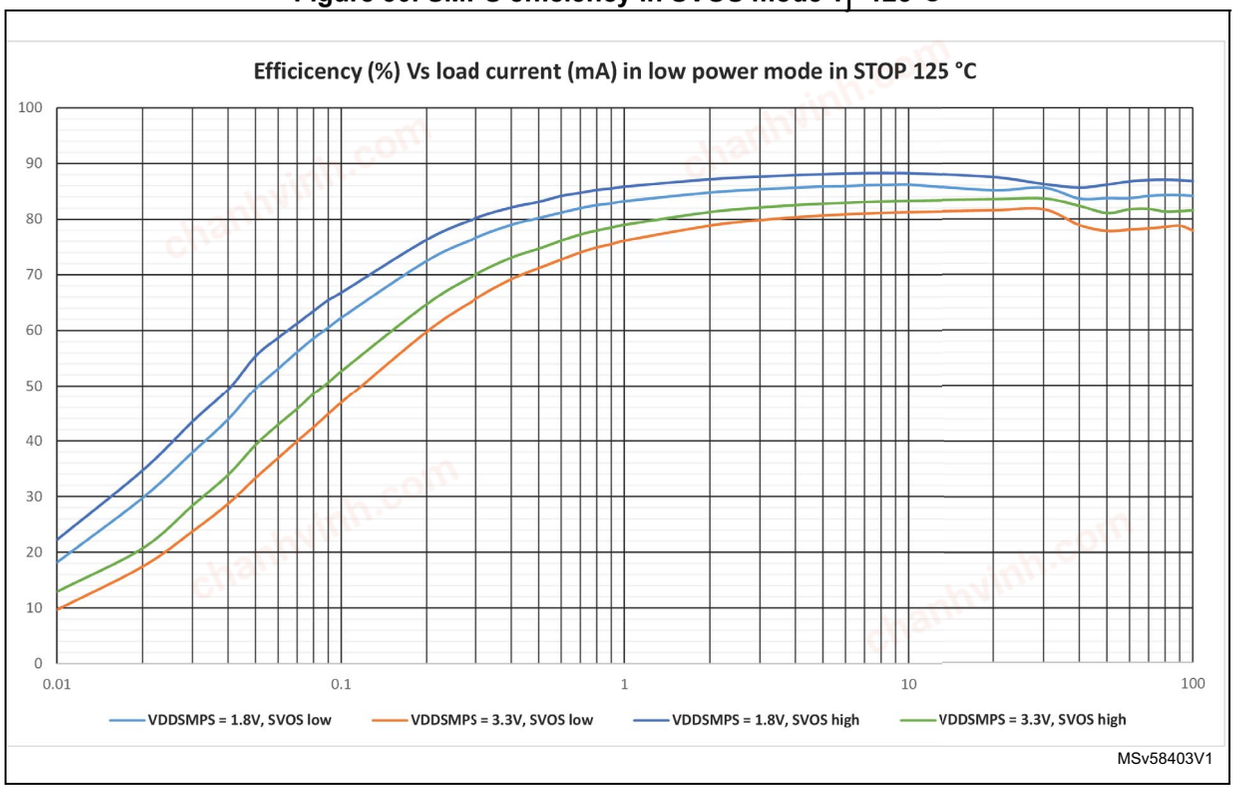


Figure 30. SMPS efficiency in SVOS mode T_j=125°C



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6.3.4 Operating conditions at power-up / power-down

These figures are subject to general operating conditions for T_A.

Table 32. Operating conditions at power-up/power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	0	∞	
	V_{DDUSB} fall time rate	10	∞	
t_{VCORE}(1)	V_{CORE} rise time rate(2)	0	285	
	V_{CORE} fall time rate	10	∞	

1. t_{VCORE} should be achieved when V_{CORE} is provided by an external supply voltage (bypass with $V_{DDLDO} = V_{CORE}$).
2. V_{CORE} rising slope must respect the above constraints. There are no constraints on the delay between V_{DD} rising and V_{CORE} rising.

6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 33* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*.

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Table 33. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after BOR0 released	-	-	377	550	µs
$V_{BOR0/POR/PDR}$	Power-on/power-down reset threshold	Rising edge(1)	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge in Run mode	2.69	2.76	2.83	
$V_{hyst_POR_PDR}$	Hysteresis voltage for Power-on/power-down reset (including BOR0)	Hysteresis in Run mode	-	43	-	mV
$V_{hyst_BOR_PVD}$	Hysteresis voltage for BOR (except BOR0)		-	100	-	
$I_{DD_BOR_PVD}$(1)	BOR and PVD consumption from V_{DD}	-	-	-	0.63	µA
$I_{DD_POR_PVD}$	POR and PVD consumption from V_{DD}	-	0.8	-	1.2	

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Table 33. Reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVM_0}	Analog voltage detector for V_{DDA} threshold 0	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVM_1}	Analog voltage detector for V_{DDA} threshold 1	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVM_2}	Analog voltage detector for V_{DDA} threshold 2	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVM_3}	Analog voltage detector for V_{DDA} threshold 3	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{hyst_VDDA}	Hysteresis of V_{DDA} voltage detector	-	-	100	-	mV
I_{DD_PVM}	PVM consumption from $V_{DD(1)}$	-	-	-	0.25	µA
I_{DD_VDDA}	Voltage detector consumption on V_{DDA}(1)	Resistor bridge	-	-	2.5	µA

1. Specified by design – not tested in production.

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6.3.6 Embedded reference voltage characteristics

The parameters given in *Table 34* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*.

Table 34. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltages	-40°C < T_J < T_{Jmax}	1.18	1.216	1.255	V
$t_{S_vrefint}$(1)(2)(3)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}(2)	VBAT sampling time when reading the internal VBAT reference voltage	-	9	-	-	
$t_{start_vrefint}$(2)	Start time of reference voltage buffer when ADC is enable	-	-	-	4.4	
I_{refbuf}(2)	Reference Buffer consumption for ADC	V_{DD} = 3.3 V	9	13.5	23	µA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	-40°C < T_J < T_{Jmax}	-	5	15	mV
T_{coeff}(2)	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$(2)	Average Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	10	1370	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	-	25	-	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage	-	-	50	-	
V_{REFINT_DIV3}	3/4 reference voltage	-	-	75	-	

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.
3. Guaranteed by design. and tested in production at 3.3 V.

Table 35. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = 3.3 V	0x08FF F810 - 0x08FF F811

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6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 24: Current consumption measurement scheme*.

All the Run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait states number, depending on the f_{ACLK} frequency (refer to the table “Number of wait states according to CPU clock ($f_{rcc_c_ck}$) frequency and V_{CORE} range” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.
- For typical values, the power supply is 3 V unless otherwise specified.
- For maximum values, the power supply is 3.6 V unless otherwise specified.

The parameters given in the below tables are derived from tests performed at supply voltage conditions summarized in *Table 26: General operating conditions*, and at ambient temperature unless otherwise specified.

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Table 36. Typical and maximum current consumption in Run mode, code with data processing running from ITCM(1)

Symbol	Parameter	Conditions		frcc_c_ck (MHz)	Typ LDO	Typ SMPS	Max(2) LDO				Unit
							TJ = 25°C	TJ = 85°C	TJ = 105°C	TJ = 125°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS high	600	125.0	65.5	135.0	235.0	310.0	-	mA
				400	84.5	45.0	95.0	195.0	275.0	-	
			VOS high(3)	400	90.0	48.0	100.0	200.0	280.0	-	
			VOS low	400	73.5	36.5	91.5	190.0	260.0	405.0	
				300	57.0	29.0	75.0	170.0	245.0	390.0	
		All peripherals enabled	VOS high	600	175.0	90.0	180.0	280.0	355.0	-	
				400	115.0	62.5	130.0	230.0	305.0	-	
			VOS high(3)	400	125.0	65.5	135.0	235.0	310.0	-	
			VOS low	400	105.0	50.5	125.0	220.0	290.0	435.0	
				300	79.5	39.5	98.0	195.0	265.0	410.0	

1. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
2. Guaranteed by characterization results unless otherwise specified. Refer to *Section 6.3.3: SMPS step-down converter* for the SMPS maximum consumption.
3. ECC is enabled.

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Table 37. Typical and maximum current consumption in Run mode, code with data processing running from AXISRAM3, cache ON (1)

Symbol	Parameter	Conditions		frcc_c_ck (MHz)	Typ LDO	Typ SMPS	Max(2) LDO				Unit
							TJ = 25°C	TJ = 85°C	TJ = 105°C	TJ = 125°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS high	600	130.0	69.0	140.0	240.0	315.0	-	mA
				400	89.5	47.5	99.5	200.0	275.0	-	
			VOS high(3)	400	92.0	49.0	105.0	205.0	280.0	-	
			VOS low	400	77.5	38.5	96.0	195.0	265.0	410.0	
				300	60.5	30.5	78.5	175.0	245.0	395.0	
		All peripherals enabled	VOS high	600	180.0	94.5	190.0	285.0	360.0	-	
				400	125.0	65.5	135.0	235.0	310.0	-	
			VOS high(3)	400	125.0	67.0	135.0	235.0	310.0	-	
			VOS low	400	105.0	52.5	130.0	225.0	295.0	440.0	
				300	82.5	41.0	105.0	200.0	270.0	415.0	

1. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
2. Guaranteed by characterization results unless otherwise specified. Refer to *Section 6.3.3: SMPS step-down converter* for the SMPS maximum consumption.
3. ECC is enabled.

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Table 38. Typical and maximum current consumption in Run mode, code with data processing running from AXISRAM3, cache OFF (1)

Symbol	Parameter	Conditions		frcc_c_ck (MHz)	Typ LDO	Typ SMPS	Max(2) LDO				Unit
							TJ = 25°C	TJ = 85°C	TJ = 105°C	TJ = 125°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS high	600	96.0	51.0	110.0	210.0	285.0	-	mA
				400	66.5	35.5	82.5	180.0	255.0	-	
			VOS high(3)	400	70.5	37.5	87.0	185.0	260.0	-	
			VOS low	400	57.5	28.5	79.5	175.0	245.0	390.0	
				300	46.0	23.5	66.5	160.0	235.0	380.0	
		All peripherals enabled	VOS high	600	145.0	77.5	160.0	255.0	330.0	-	
				400	99.5	53.0	115.0	215.0	290.0	-	
			VOS high(3)	400	105.0	55.5	120.0	215.0	290.0	-	
			VOS low	400	87.0	43.0	110.0	205.0	275.0	420.0	
				300	68.0	34.0	89.0	185.0	255.0	405.0	

1. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
2. Guaranteed by characterization results unless otherwise specified. Refer to *Section 6.3.3: SMPS step-down converter* for the SMPS maximum consumption.
3. ECC is enabled.

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Table 39. Typical and maximum current consumption in Run mode, code with data processing running from internal flash memory, cache ON(1)

Symbol	Parameter	Conditions		frcc_c_ck (MHz)	Typ LDO	Typ SMPS	Max(2) LDO				Unit
							TJ = 25°C	TJ = 85°C	TJ = 105°C	TJ = 125°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS high	600	130.0	67.5	140.0	235.0	315.0	-	mA
				400	87.0	46.5	97.0	200.0	275.0	-	
			VOS high(3)	400	89.5	48.0	99.5	200.0	280.0	-	
			VOS low	400	75.5	37.0	93.5	190.0	265.0	410.0	
				300	58.5	29.5	76.5	175.0	245.0	395.0	
		All peripherals enabled	VOS high	600	175.0	92.5	185.0	285.0	360.0	-	
				400	120.0	64.0	130.0	230.0	305.0	-	
			VOS high(3)	400	125.0	65.5	135.0	235.0	310.0	-	
			VOS low	400	105.0	51.5	125.0	220.0	295.0	440.0	
				300	81.0	40.5	99.5	195.0	270.0	415.0	

1. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
2. Guaranteed by characterization results unless otherwise specified. Refer to *Section 6.3.3: SMPS step-down converter* for the SMPS maximum consumption.
3. ECC is enabled.

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Table 40. Typical and maximum current consumption in Run mode, code with data processing running from internal flash memory, cache OFF(1)

Symbol	Parameter	Conditions		frcc_c_ck (MHz)	Typ LDO	Typ SMPS	Max(2) LDO				Unit
							TJ = 25°C	TJ = 85°C	TJ = 105°C	TJ = 125°C	
I_{DD}	Supply current in Run mode	All peripherals disabled	VOS high	600	78.5	43.5	91.5	195.0	270.0	-	mA
				400	59.0	33.0	73.5	175.0	250.0	-	
			VOS high(3)	400	60.5	34.0	75.0	175.0	250.0	-	
			VOS low	400	49.5	26.5	68.5	165.0	235.0	385.0	
				300	41.5	22.5	60.5	155.0	230.0	375.0	
		All peripherals enabled	VOS high	600	130.0	69.5	140.0	240.0	315.0	-	
				400	92.5	51.0	105.0	205.0	280.0	-	
			VOS high(3)	400	94.0	52.0	110.0	205.0	280.0	-	
			VOS low	400	78.5	40.5	98.5	195.0	265.0	415.0	
				300	64.0	33.0	83.0	180.0	250.0	400.0	

1. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
2. Guaranteed by characterization results unless otherwise specified. Refer to *Section 6.3.3: SMPS step-down converter* for the SMPS maximum consumption.
3. ECC is enabled.

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Table 41. Typical consumption in Run mode and corresponding performance versus code position

Symbol	Parameter	Conditions		frcc_c_ck (MHz)	Coremark	Typ LDO	Typ SMPS	Unit	LDO I_{DD} CoreMark	SMPS I_{DD} CoreMark	Unit
		Peripheral	Code								
I_{DD}	Supply current in Run mode	All peripherals disabled	ITCM	600	2976	125.0	65.5	mA	42.0	22.2	µA/ Core-Mark
		All peripherals disabled, cache ON	AXI SRAM3	600	2976	130.0	69.0		43.7	23.2	
			Internal flash	600	2976	130.0	67.5		43.7	22.7	
		All peripherals disabled, cache OFF	AXI SRAM3	600	1284	96.0	51.0		74.8	39.7	
			Internal flash	600	564	78.5	43.5		139.2	77.1	

Table 42. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions		frcc_c_ck (MHz)	Typ LDO	Typ SMPS	Max(1) LDO				Unit
							TJ = 25°C	TJ = 85°C	TJ = 105°C	TJ = 125°C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	All peripherals disabed	VOS high	600	34.5	20.0	49.0	150.0	225.0	-	mA
				400	24.5	14.5	39.5	140.0	215.0	-	
			VOS high(2)	400	24.5	14.5	40.0	140.0	220.0	-	
			VOS low	400	20.5	11.5	38.0	135.0	205.0	345.0	
				300	17.5	9.9	34.5	130.0	205.0	340.0	

1. Guaranteed by characterization results unless otherwise specified. Refer to *Section 6.3.3: SMPS step-down converter* for the SMPS maximum consumption.
2. ECC is enabled.

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Table 43. Typical and maximum current consumption in System Stop mode

Symbol	Parameter	Conditions		Typ LDO	Typ SMPS	Max(1) LDO				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DD(Stop)}$	Stop	Flash memory in low-power mode	SVOS high	1.450	0.700	11.0	66.5	115.0	200.0	mA
			SVOS low	0.605	0.265	4.3	32.5	56.0	105.0	
		Flash memory in normal mode	SVOS high	1.500	0.705	11.0	66.5	115.0	200.0	
			SVOS low	0.605	0.265	4.3	32.5	56.0	105.0	

1. Guaranteed by characterization results unless otherwise specified. Refer to *Section 6.3.3: SMPS step-down converter* for the SMPS maximum consumption.

Table 44. Typical and maximum current consumption in Standby mode

Smbol	Parameter	Conditions		Typ				Max (3.6 V)(1)				Unit
		Backup SRAM	RTC and LSE(2)	1.8 V	2.4 V	3 V	3.3 V	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD} (Standby)	Supply current in Standby mode, **IWDG OFF**	OFF	OFF	2.4	2.6	2.8	3.0	5.4	15.5	31.5	84.5	µA
		ON	OFF	3.9	4.2	4.5	4.7	8.6	40.5	97.0	160.0	
		OFF	ON	3.0	3.1	3.5	3.7	-	-	-	-	
		ON	ON	4.2	4.6	5.0	5.3	-	-	-	-	

1. Guaranteed by characterization results.
2. The LSE is in Low-drive mode.

Table 45. Typical and maximum current consumption in V_{BAT} mode

Sym-bol	Parameter	Conditions		Typ				Max (3.6 V)(1)				Unit
		Backup SRAM	RTC and LSE(2)	1.62 V	2.4 V	3 V	3.3 V	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD} (VBAT)	Supply current in VBAT mode	OFF	OFF	0.009	0.013	0.021	0.037	0.22	3.40	8.70	27.00	µA
		ON	OFF	1.5	1.8	1.8	1.9	2.85	19.00	41.00	87.00	
		OFF	ON	0.4	0.5	0.7	0.8	1.10	4.25	9.55	28.50	
		ON	ON	1.9	2.1	2.4	2.5	3.70	19.50	41.50	89.00	

1. Guaranteed by characterization results.
2. The LSE is in Low-drive mode.

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XSPI current consumption

All XSPI current consumption measurements given in this section are performed using the TFBGA225 SMPS HEXA product, which supports both 16-bit SPI and OCTO-SPI memories. A 16-bit SPI memory is connected to Port 1, while an Octo-SPI memory is connected to port 2.

The MCU is put under the following conditions:

- The external Octo and HexaSPI power supply ($V_{DDXSPI1}$, $V_{DDXSPI2}$) is 1.8 V
- All I/O pins of Hexa and Octo dedicated Power rail (XSPIM1 rail, XSPIM2 rail) are configured in HSLV mode .
- The Memory clock frequency is the CPU frequency divided by 2
- The MCU power supply is 3 V unless otherwise specified.

The parameters given in the below tables are derived from tests performed with :

- CoreMark code running from Octo SPI memory (*Table 46*), and 16-bit SPI memory (*Table 47*).
- Data write on 16-bit memory with 50%, 25%,12.5%, or 6.25% of toggling (*Table 48* to *Table 51*).

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Table 46. Typical and maximum current consumption in Run mode, code with data processing running from Octo flash memory(1), cache OFF(2)

Symbol	Parameter	Conditions	frcc_c_ck (MHz)	Memory frequency(MHz)	Typ	Max(3) TJ = 105°C	Unit
IDD_XSPI	XSPI current in Run mode	$V_{DDXSPIx}$ = 1.8 V	380	190	9.00	9.5	mA
			320	160	7.10	7.7	
			266	133	5.80	6.3	
			200	100	4.50	4.9	
			180	90	4.05	4.5	
			120	60	2.70	3.0	
			60	30	1.35	1.5	

1. MACRONIX_MX66UW1G45G.
2. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
3. Guaranteed by characterization results.

Table 47. Typical and maximum current consumption in Run mode, code with data processing running from 16-bit memory(1), cache OFF(2)

Symbol	Parameter	Conditions	frcc_c_ck (MHz)	Memory frequency(MHz)	Typ	Max(3) TJ = 105°C	Unit
IDD_XSPI	XSPI current in Run mode	$V_{DDXSPIx}$ = 1.8 V	380	190	4.55	5.0	mA
			320	160	3.70	4.1	
			266	133	3.10	3.4	
			200	100	2.35	2.6	
			180	90	2.10	2.4	
			120	60	1.45	1.6	
			60	30	0.76	0.8	

1. AP_Memory_Hexa-SPI_PSRAM_APS256XXN OBR-BG.
2. Data are in DTCM for best computation performance, cache has no influence on consumption in this case.
3. Guaranteed by characterization results.

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Table 48. Typical and maximum current consumption: data write 50% toggle on 16-bit memory(1)

Symbol	Parameter	Conditions	frcc_c_ck (MHz)	Memory frequency(MHz)	Typ	Max(2) TJ = 105°C	Unit
IDD_XSPI	XSPI current in Run mode	$V_{DDXSPIx}$ = 1.8 V	380	190	48.0	52.0	mA
			320	160	38.0	42.0	
			266	133	32.0	35.5	
			200	100	25.0	27.5	
			180	90	22.5	25.0	
			120	60	15.0	17.0	
			60	30	7.6	8.5	

1. AP_Memory_Hexa-SPI_PSRAM_APS256XXN OBR-BG
2. Guaranteed by characterization results.

Table 49. Typical and maximum current consumption: data write 25% toggle on 16-bit memory(1)

Symbol	Parameter	Conditions	frcc_c_ck (MHz)	Memory frequency(MHz)	Typ	Max(2) TJ = 105°C	Unit
IDD_XSPI	XSPI current in Run mode	$V_{DDXSPIx}$ = 1.8 V	380	190	26.50	29.0	mA
			320	160	21.50	23.5	
			266	133	18.00	20.0	
			200	100	14.00	15.5	
			180	90	12.50	14.0	
			120	60	8.50	9.4	
			60	30	4.25	4.8	

1. AP_Memory_Hexa-SPI_PSRAM_APS256XXN OBR-BG.
2. Guaranteed by characterization results.

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Table 50. Typical and maximum current consumption: data write 12.5% toggle on 16-bit memory(1)

Symbol	Parameter	Conditions	frcc_c_ck (MHz)	Memory frequency(MHz)	Typ	Max(2) TJ = 105°C	Unit
IDD_XSPI	XSPI current in Run mode	$V_{DDXSPIx}$ = 1.8 V	380	190	16.00	17.5	mA
			320	160	13.00	14.0	
			266	133	11.00	12.0	
			200	100	8.35	9.3	
			180	90	7.55	8.4	
			120	60	5.10	5.7	
			60	30	2.55	2.9	

1. AP_Memory_Hexa-SPI_PSRAM_APS256XXN OBR-BG.
2. Guaranteed by characterization results.

Table 51. Typical and maximum current consumption: data write 6.25% toggle on 16-bit memory(1)

Symbol	Parameter	Conditions	frcc_c_ck (MHz)	Memory frequency (MHz)	Typ	Max(2) TJ = 105°C	Unit
IDD_XSPI	XSPI current in Run mode	$V_{DDXSPIx}$ = 1.8 V	380	190	10.50	11.5	mA
			320	160	8.55	9.5	
			266	133	7.35	8.0	
			200	100	5.60	6.2	
			180	90	5.05	5.6	
			120	60	3.40	3.8	
			60	30	1.70	1.9	

1. AP_Memory_Hexa-SPI_PSRAM_APS256XXN OBR-BG.
2. Guaranteed by characterization results.

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I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as input with pull-up or pull-down generate a current consumption when the pin is externally held to the opposite level.

The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 71: I/O static characteristics*.

For the output pins, any internal or external pull-up or pull-down and external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal and external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

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On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc_c_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc_c_ck}/4$, and $f_{HCLK} = f_{rcc_c_ck}/2$.
  The given value is calculated by measuring the difference of current consumption
  – with all peripherals clocked off
  – with only one peripheral clocked on
- The ambient operating temperature is 25 °C and V_{DD}=3 V

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Table 52. Typical dynamic current consumption of peripherals

Bus	Peripheral	LDO		SMPS		Unit
		VOS high	VOS low	VOS high	VOS low	
AHB1	ADC1/2 registers	2.57	1.89	1.34	1.00	µA/MHz
	ADC1/2 kernel	0.55	0.49	0.35	0.34	
	ADF1 registers	1.19	1.06	0.59	0.52	
	ADF1 kernel	2.45	2.18	1.23	1.09	
	ETHERNET MAC registers	11.44	9.56	6.05	4.90	
	ETHERNET MAC kernel	2.38	2.12	1.19	1.06	
	ETHERNETRX	0.44	0.39	0.22	0.20	
	ETHERNETTX	0.50	0.44	0.25	0.22	
	GPDMA1	1.27	0.99	0.62	0.45	
	OTG_FS registers	7.06	5.97	3.82	3.07	
	OTG_FS kernel	0.27	0.24	0.14	0.12	
	OTG_HS	15.46	13.37	8.33	6.85	
	USBPHYC registers	0.23	0.20	0.08	0.07	
	USBPHYC kernel	1.10	0.98	0.40	0.36	
AHB2	CORDIC	0.33	0.29	0.21	0.19	
	PSSI registers	1.85	1.69	1.05	0.85	
	PSSI kernel	0.43	0.33	0.20	0.18	
	SDMMC2	7.63	6.76	4.19	3.43	
	SRAM1	0.37	0.33	0.25	0.22	
	SRAM2	0.46	0.42	0.30	0.27	
AHB3	CRYP	0.89	0.77	0.54	0.44	
	HASH	1.10	0.95	0.64	0.55	
	PKA	4.79	4.20	2.64	2.20	
	RNG	0.82	0.69	0.46	0.38	
	SAES	6.83	6.07	4.28	3.80	

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Table 52. Typical dynamic current consumption of peripherals (continued)

Bus	Peripheral	LDO		SMPS		Unit
		VOS high	VOS low	VOS high	VOS low	
AHB4	BKPRAM	1.34	1.17	0.84	0.75	µA/MHz
	CRC	0.25	0.22	0.13	0.10	
	GPIOA	0.14	0.12	0.09	0.07	
	GPIOB	0.14	0.14	0.10	0.08	
	GPIOC	0.16	0.14	0.12	0.10	
	GPIOD	0.12	0.11	0.07	0.06	
	GPIOE	0.12	0.11	0.07	0.06	
	GPIOF	0.16	0.14	0.08	0.06	
	GPIOG	0.13	0.12	0.09	0.08	
	GPIOH	0.15	0.13	0.08	0.07	
	GPIOM	0.17	0.16	0.09	0.08	
	GPION	0.17	0.15	0.09	0.08	
	GPIOO	0.31	0.28	0.21	0.18	
	GPIOP	0.30	0.27	0.22	0.19	

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Table 52. Typical dynamic current consumption of peripherals (continued)

Bus	Peripheral	LDO		SMPS		Unit
		VOS high	VOS low	VOS high	VOS low	
AHB5	DMA2D	1.29	1.15	0.78	0.65	µA/MHz
	FMC/MCE3 registers	2.47	2.21	1.39	1.13	
	FMC/MCE3 kernel	4.71	4.21	2.58	2.15	
	GFXMMU	0.63	0.59	0.41	0.29	
	GPU2D	6.00	5.37	3.37	2.73	
	HPDMA1	0.91	0.84	0.51	0.42	
	JPEG	1.47	1.38	0.86	0.68	
	SDMMC1	6.88	6.13	3.82	3.15	
	XSPI1/MCE1 registers	0.86	0.77	0.49	0.43	
	XSPI1/MCE1 kernel	1.02	0.99	0.57	0.51	
	XSPI2/MCE2 registers	0.74	0.71	0.46	0.37	
	XSPI2/MCE2 kernel	1.03	0.93	0.54	0.48	
	XSPIM	0.22	0.20	0.11	0.10	
	Flash	13.75	12.19	7.58	6.19	
	DTCM1	0.69	0.62	0.43	0.34	
	DTCM2	0.50	0.44	0.31	0.27	
	ITCM	0.72	0.64	0.44	0.37	
	AXI SRAM	10.02	8.95	5.56	4.52	
APB1	HDMI-CEC register	0.90	0.80	0.34	0.30	
	HDMI-CEC kernel	8.65	7.69	4.33	3.85	
	CRS	7.32	6.14	3.9	3.06	
	FDCAN1/2 register	6.53	5.54	3.4	2.75	
	FDCAN1/2 kernel	3.64	3.25	1.87	1.54	
	I2C1 register	1.34	1.19	0.59	0.52	
	I2C1 kernel	4.54	4.01	2.53	2.04	
	I2C2 register	1.27	1.13	0.49	0.44	
	I2C2 kernel	1.65	1.52	0.89	0.79	
	I2C3 register	1.36	1.21	0.51	0.45	

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Table 52. Typical dynamic current consumption of peripherals (continued)

Bus	Peripheral	LDO		SMPS		Unit
		VOS high	VOS low	VOS high	VOS low	
APB1	I2C3 kernel	2.14	1.87	1.22	0.96	µA/MHz
	LPTIM1 registers	1.33	1.18	0.63	0.50	
	LPTIM1 kernel	3.38	2.93	1.83	1.50	
	MDIOS	2.83	2.52	1.35	1.04	
	SPDIF-RX registers	0.99	0.71	0.37	0.33	
	SPDIF-RX kernel	2.34	2.21	1.33	1.10	
	SPI2 registers	1.84	1.35	0.87	0.67	
	SPI2 kernel	2.14	1.92	0.99	0.88	
	SPI3 registers	1.79	1.41	0.84	0.62	
	SPI3 kernel	1.91	1.78	1.07	0.98	
	TIM12	1.90	1.52	0.92	0.72	
	TIM13	1.39	1.04	0.59	0.42	
	TIM14	1.49	1.1	0.64	0.51	
	TIM2	3.40	2.97	1.83	1.49	
	TIM3	3.56	3.04	1.87	1.50	
	TIM4	3.58	3.11	1.85	1.49	

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Table 52. Typical dynamic current consumption of peripherals (continued)

Bus	Peripheral	LDO		SMPS		Unit
		VOS high	VOS low	VOS high	VOS low	
APB1	TIM5	3.48	3.01	1.81	1.45	µA/MHz
	TIM6	1.02	0.86	0.51	0.45	
	TIM7	0.91	0.74	0.45	0.4	
	UART4 registers	2.12	1.63	1.07	0.78	
	UART4 kernel	3.53	3.05	1.95	1.55	
	UART5 registers	2.13	1.59	1.10	0.98	
	UART5 kernel	3.62	3.14	1.94	1.61	
	UART7 registers	2.24	1.68	1.14	1.01	
	UART7 kernel	3.43	3.02	1.95	1.54	
	UART8 registers	2.27	1.71	1.16	1.03	
	UART8 kernel	3.61	3.17	1.96	1.58	
	UCPD1	2.61	2.21	1.25	1.06	
	USART2 registers	2.32	1.87	1.12	0.86	
	USART2 kernel	3.41	3.03	1.89	1.55	
	USART3 registers	2.07	1.66	1.04	0.79	
	USART3 kernel	4.02	3.60	2.20	1.82	
	WWDG	1.25	1.11	0.57	0.46	

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Table 52. Typical dynamic current consumption of peripherals (continued)

Bus	Peripheral	LDO		SMPS		Unit
		VOS high	VOS low	VOS high	VOS low	
APB2	SAI1 registers	1.17	1.01	0.56	0.41	µA/MHz
	SAI1 kernel	1.56	1.38	0.87	0.68	
	SAI2 registers	1.19	1.02	0.64	0.57	
	SAI2kernel	1.41	1.22	0.73	0.64	
	SPI1 registers	1.29	1.14	0.68	0.54	
	SPI1 kernel	2.15	1.87	1.08	0.95	
	SPI4 registers	1.25	1.11	0.66	0.53	
	SPI4 kernel	1.48	1.35	0.88	0.69	
	SPI5 registers	1.3	1.22	0.60	0.52	
	SPI5kernel	1.69	1.42	0.91	0.69	
	TIM1	4.50	3.97	2.43	1.98	
	TIM15	2.25	2.02	1.25	0.99	
	TIM16	1.54	1.45	0.88	0.69	
	TIM17	1.60	1.42	0.87	0.74	
	TIM9	1.39	1.24	0.67	0.58	
	USART1 registers	1.50	1.33	0.78	0.62	
	USART1 kernel	4.03	3.47	2.20	1.77	

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Table 52. Typical dynamic current consumption of peripherals (continued)

Bus	Peripheral	LDO		SMPS		Unit
		VOS high	VOS low	VOS high	VOS low	
APB4	DTS	2.10	1.63	1.01	0.89	µA/MHz
	LPTIM2 registers	1.24	1.1	0.57	0.49	
	LPTIM2 kernel	3.17	2.78	1.78	1.46	
	LPTIM3 registers	1.23	0.97	0.61	0.51	
	LPTIM3 kernel	3.35	2.99	1.84	1.5	
	LPTIM4 registers	0.69	0.56	0.35	0.26	
	LPTIM4 kernel	1.90	1.79	1.08	0.87	
	LPTIM5 registers	0.73	0.58	0.36	0.31	
	LPTIM5 kernel	2.24	1.92	1.25	1.04	
	LPUART1 registers	1.39	1.07	0.68	0.64	
	LPUART1 KERNEL	2.46	2.25	1.40	1.12	
	RTCAPB	1.85	1.51	0.93	0.80	
	SBS	0.71	0.63	0.33	0.29	
	SPI6 registers	1.58	1.16	0.74	0.68	
	SPI6 kernel	1.69	1.55	0.91	0.77	
	VREF	0.27	0.24	0.12	0.11	
APB5	DCMIPP	5.71	5.03	3.14	2.60	
	GFXTIM	1.12	1.03	0.67	0.56	
	LTDC	3.42	3.03	1.87	1.55	

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6.3.8 Wake-up time from low-power modes

The wake-up times given in *Table 53* are measured starting from the wake-up event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wake-up event is WFE.
- WKUP (PC1) pin is used to wake-up from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3 V.

Table 53. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)(2)(3)	Unit
$t_{WUSLEEP}$(4)	Wakeup from Sleep	-	15	16	CPU clock cycles
$t_{WUDSTOP}$(4)	Wakeup from Stop	SVOS low, HSI, Flash memory in normal mode	42.5	46.0	µs
		SVOS low, HSI, Flash memory in low-power mode	42.5	46.0	
		SVOS high, HSI, Flash memory in normal mode	16.0	17.5	
		SVOS high, HSI, Flash memory in low-power mode	20.0	21.0	
		SVOS low, CSI, Flash memory in normal mode	65.0	71.0	
		SVOS low, CSI, Flash memory in low power mode	71.5	77.5	
		SVOS high, CSI, Flash memory in normal mode	32.0	35.0	
		SVOS high, CSI, Flash memory in low-power mode	48.5	54.0	
$t_{WUSTDBY}$(4)	Wakeup from Standby mode	-	280.0	535.0	

1. Guaranteed by characterization results.
2. Measurements are made at -40°C under worst-case conditions.
3. Maximum values are for the LDO configuration.
4. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction..

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6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

The external clock signal has to respect the *Table 71: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 31*.

Table 54. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	External digital/ analog clock	4	25	50	MHz
V_{HSEH}	Digital OSC_IN input high-level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input low-level voltage	External digital cwlock	V_{SS}	-	0.3 V_{DD}	
$t_{W(HSE)}$(2)	OSC_IN high or low time(2)	External digital clock	7	-	-	ns
V_{lswHSE} (V_{HSEH} -V_{HSEL})(3)	Analog low swing OSC_IN peak-to-peak amplitud(3)e	External Analog Low Swing Clock	0.2	-	2/3 V_{DD}	V
DuCyHSE	Analog low swing OSC_IN duty cycle	External analog low-swing clock	45	50	55	%
t_{rHSE}/t_{fHSE}	Analog low swing OSC_IN rise and fall time(3)	External analog low -swing clock 10% to 90%	0.05 / f_{HSE_ext}	-	0.3 / f_{HSE_ext}	ns

1. Guaranteed by design.
2. No specified rise and fall time for a digital input signal but the VHSEH and VHSEL conditions must be fulfilled.
3. The DC component of the signal must insure that the signal peaks are located between V_{DD} and V_{SS}.

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Figure 31. High-speed external clock source AC timing diagram

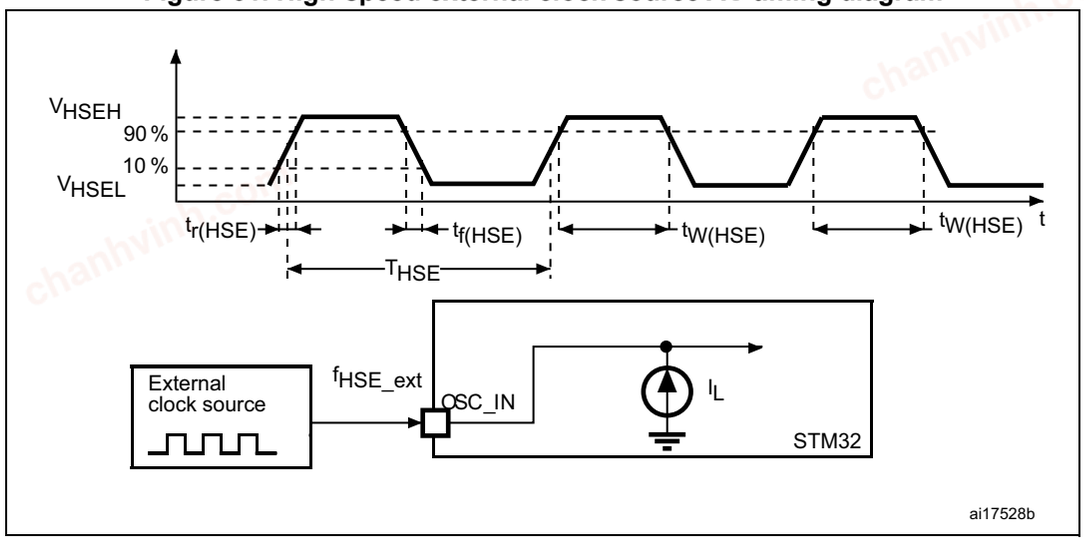


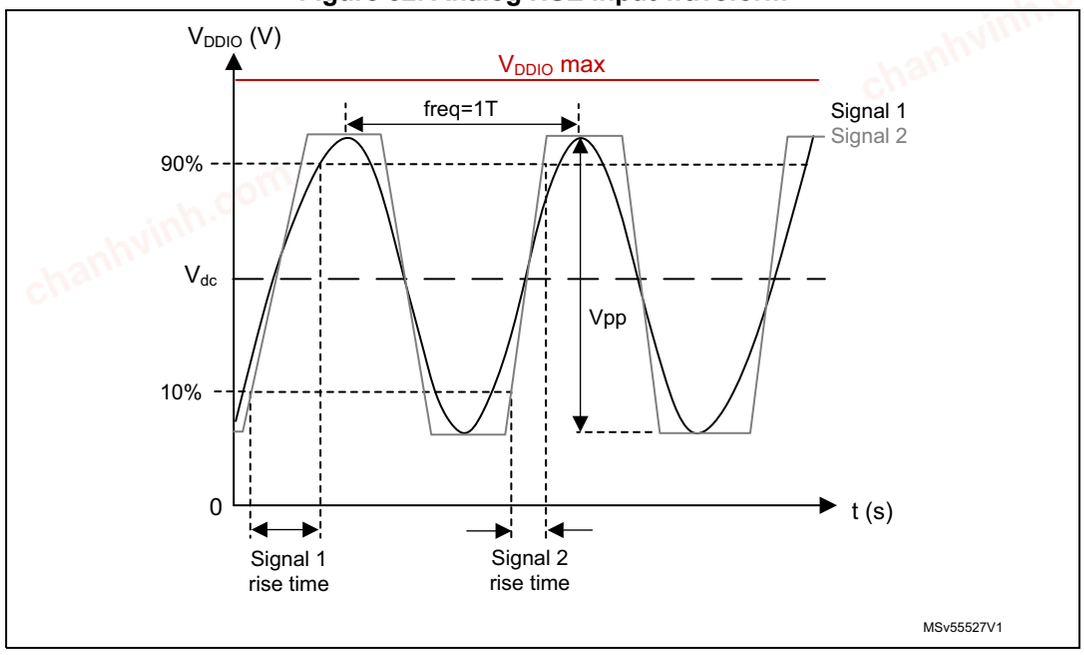
Table 55. Timing for analog HSE input

Parameter	Comment	Min	Typ	Max	KHz
IO power supply	V_{DDIO}	1.71	3.30	3.60	V
Temperature	-	-40	25	125	°C
Absolute input range	-	0.000	-	V_{DDIO}	V
Input peak-to peak amplitude	V pp	0.2(1)	-	2/3.V_{DDIO}	V
V_{DDIO} power consumption	-	-	150(2)	500(3)	µA
Input frequency	-	4	-	50(4)	MHz
Input duty cycle	Square wave	45	50	55	%
Duty cycle deterioration	-	0	±10(5)	±10(6)	
Time to start	-	1	-	10(7)	µs
Rise and fall time	10% to 90% threshold levels of the input peak-to-peak amplitude	0.05 / freq	-	0.3 / freq	-

1. 200 mV is the minimum peak-to-peak amplitude @25°C (0.1 V< V_{dc} < $V_{DD\ IO}$ -0.1 V where V_{dc} is the DC component of the input signal).
2. Power consumption with a sine wave signal at the input @25°C ($V_{DD\ IO}$ = 3.3 V / V pp = 400 mV / V dc = 0.4 V).
3. Power consumption with a sine wave signal at the input @125°C ($V_{DD\ IO}$ = 3.6 V / V pp = 800 mV / V dc =1.8 V).
4. The IP is functional up to 50 MHz for RMII applications.
5. Guaranteed by design with a square wave @25°C / $V_{DD\ IO}$ =3.3 V / V pp = 400 mV / V_{dc} =1 V.
6. Guaranteed by design with a square wave @25°C / $V_{DD\ IO}$ =1.6 V / V pp = 200 mV / V_{dc} =0.8 V.
7. Maximum start-up time value (slow corner @125°C with 200 mV peak-to-peak amplitude).

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Figure 32. Analog HSE input waveform



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Low-speed external user clock generated from an external source

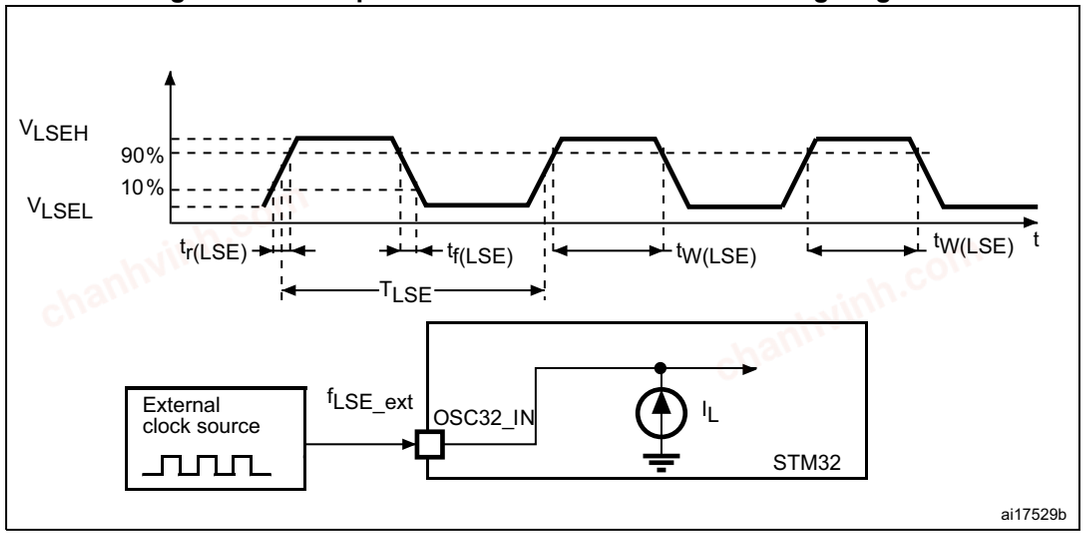
In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 71: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 33*.

Table 56. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	External digital / analog clock	-	32.768	1000	kHz
V_{LSEH}	Digital OSC_IN input high level	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	External digital clock	V_{SS}	-	0.3 V_{DD}	V
$t_{w(LSEH)}/t_{w(LSEL)}$	OSC32_IN high or low time	External digital clock	250	-	-	ns
V_{lsw_H}	Analog low-swing OSC_IN high level	External analog low swing clock	0.6		1.225	V
V_{lsw_L}	Analog low-swing OSC_IN low level	External Analog low swing clock	0.35		0.8	V
V_{lswLSE} (V_{LSEH} - V_{LSEL})	Analog low-swing OSC_IN peak-to-peak amplitude	External analog low swing clock	0.2		0.875	V
D_{uCyLSE}	Analog low-swing OSC_IN duty cycle	External analog low swing clock	45	50	55	%
t_{rLSE}/t_{fLSE}	Analog low -swing OSC_IN rise and fall time	External analog low swing clock 10% to 90%	-	100	200	ns

1. Specified by design - not tested in production.

Figure 33. Low-speed external clock source AC timing diagram



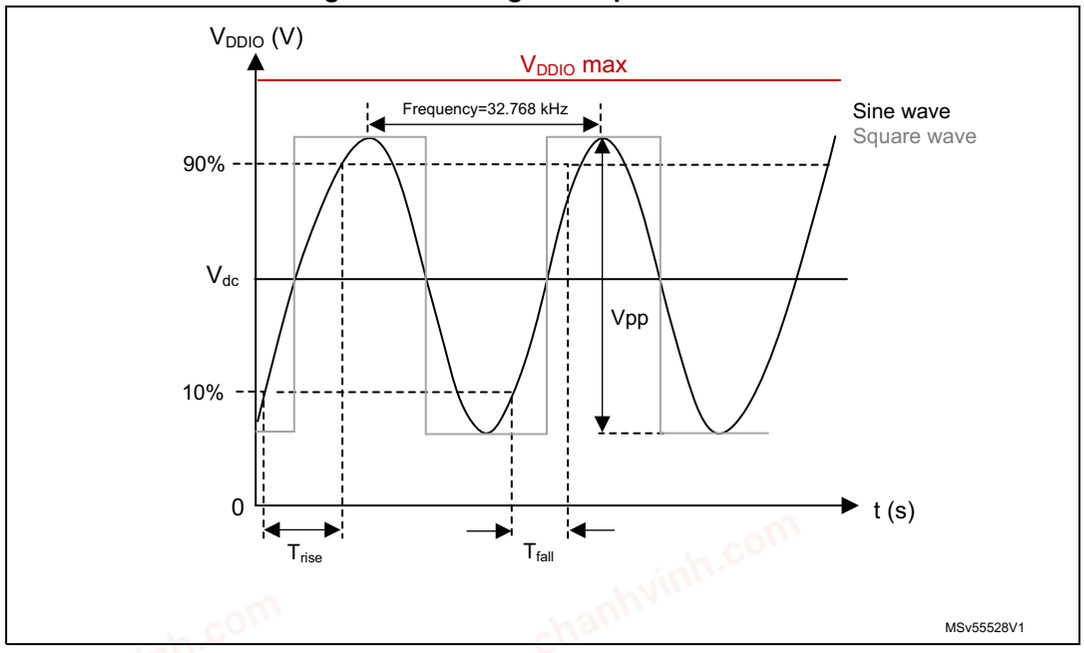
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Table 57. Timing for analog LSE input

Parameter	Comment	Min	Typ	Max	Unit
Input frequency	Fundamental frequency	32.768	32.768	32.768	kHz
Input peak-to-peak amplitude	Vpp	0.3(1)	-	V_{SW}	V
Absolute input range	-	-	-	V_{SW}	

1. 300 mV is the minimum peak-to-peak amplitude @25°C (0.1V<V_{dc} < V_{DDIO} -0.1V where V_{dc} is the DC component of the input signal).

Figure 34. Analog LSE input waveform



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High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 58*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 58. 4-50 MHz HSE oscillator characteristics(1)

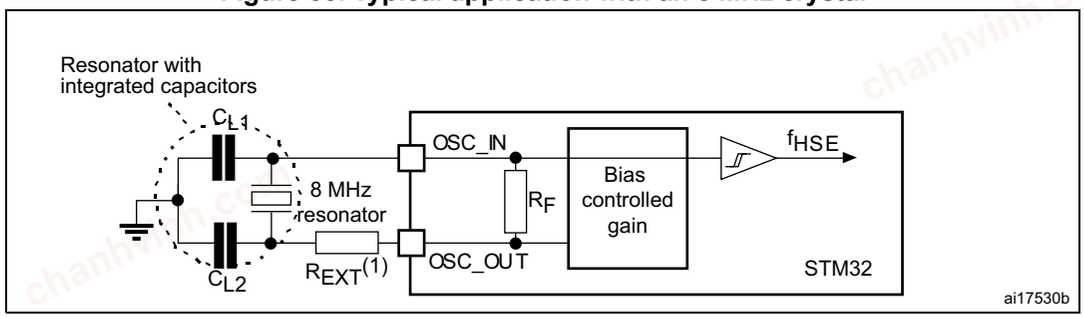
Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	50	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	10	mA
		V_{DD}=3 V, Rm=20 Ω C_L=10 pF at 4 MHz	-	0.44	-	
		V_{DD}=3 V, Rm=20 Ω C_L=10 pF at 8 MHz	-	0.44	-	
		V_{DD}=3 V, Rm=20 Ω C_L=10 pF at 16 MHz	-	0.55	-	
		V_{DD}=3 V, Rm=20 Ω C_L=10 pF at 32 MHz	-	0.67	-	
		V_{DD}=3 V, Rm=20 Ω C_L=10 pF at 48 MHz	-	1.17	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
t_{SU}(4)	Start-up time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to application note AN2867 “Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs” available from the ST website www.st.com.

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Figure 35. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 59*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 59. Low-speed external user clock characteristics(1)

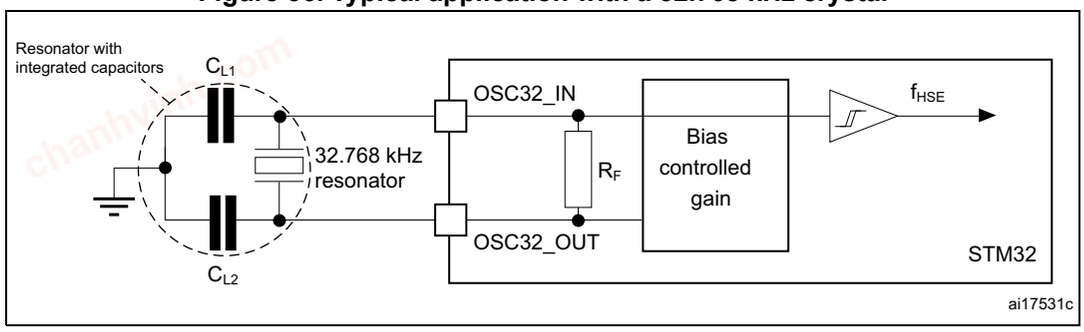
Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	246	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	333	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	462	-	
		LSEDRV[1:0] = 11, High drive capability	-	747	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	VDD is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 *"Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs"*.
3. t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

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Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs” available from the ST website www.st.com.

Figure 36. Typical application with a 32.768 kHz crystal



1. *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

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6.3.10 Internal clock source characteristics

The parameters given in *Table 60* to *Table 62* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*.

48 MHz high-speed internal RC oscillator (HSI48)

Table 60. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD}=3.3 V, TJ=30 °C	47.5(1)	48	48.5(1)	MHz
TRIM(2)	USER trimming step	-	-	0.175	0.250	%
USER TRIM COVERAGE(3)	USER trimming coverage	± 32 steps	±4.70	±5.6	-	%
$DuCy_{(HSI48)}$(2)	Duty cycle	-	45	-	55	%
ACCHSI48_REL(3)(4)	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	T_J=-40 to 125 °C	-4.5	-	3.5	%
$\Delta_{VDD}(HSI48)$(2)(4)	HSI48 oscillator frequency drift with V_{DD}(5) (the reference is 3.3 V)	V_{DD}=3 to 3.6 V	-	0.025	0.05	%
		V_{DD}=1.62 V to 3.6 V	-	0.05	0.1	
$t_{su(HSI48)}$(2)	HSI48 oscillator start-up time	-	-	2.1	4.0	µs
$I_{DD(HSI48)}$(2)	HSI48 oscillator power consumption	-	-	350	400	µA
N_T jitter(2)	Next transition jitter Accumulated jitter on 28 cycles(6)	-	-	± 0.15	-	ns
P_T jitter(2)	Paired transition jitter Accumulated jitter on 56 cycles(6)	-	-	± 0.25	-	ns

1. Guaranteed by test in production.
2. Guaranteed by design.
3. Guaranteed by characterization.
4. Δf_{HSI} = ACCHSI48_REL + Δ_{VDD}.
5. These values are obtained by using the formula: (Freq(3.6 V) - Freq(3.0 V)) / Freq(3.0 V) or (Freq(3.6 V) - Freq(1.62 V)) / Freq(1.62 V).
6. Jitter measurements are performed without clock source activated in parallel.

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64 MHz high-speed internal RC oscillator (HSI)

Table 61. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	V_{DD}=3.3 V, T_J=30 °C	63.7(2)	64	64.3(2)	MHz
TRIM	HSI user trimming step	Trimming is not a multiple of 32	-	0.24	0.32	%
		Trimming is 128, 256 and 384	-5.2	-1.8	-	
		Trimming is 64, 192, 320 and 448	-1.4	-0.8	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)	-0.6	-0.25	-	
DuCy(HSI)	Duty cycle	-	45	-	55	%
$\Delta_{VDD\ (HSI)}$	HSI oscillator frequency drift over V_{DD} (the reference is 3.3 V)	V_{DD}=1.71 to 3.6 V	-0.12	-	0.03	%
$\Delta_{TEMP(HSI)}$	HSI oscillator frequency drift over temperature (the reference is 64 MHz)	T_J=-20 to 105 °C	-1(3)	-	1(3)	%
		T_J=-40 to $T_J$max °C	-2(3)	-	1(3)	
t_{su}(HSI)	HSI oscillator start-up time	-	-	1.4	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1% of target frequency	-	4	8	
		at 5% of target frequency	-	-	4	
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by test in production.
3. Guaranteed by characterization.

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4 MHz low-power internal RC oscillator (CSI)

Table 62. CSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}	CSI frequency	V_{DD}=3.3 V, T_J=30 °C	3.96(2)	4	4.04(2)	MHz
TRIM	CSI trimming step	Trimming is not a multiple of 16	-	0.40	0.75	%
		Trimming is a multiple of 32	-4.75	-2.75	0.75	
		Other trimming values not multiple of 16 (excluding multiple of 32)	-0.43	0.00	0.75	
DuCy(CSI)	Duty cycle	-	45	-	55	%
Δ_{TEMP} (CSI)	CSI oscillator frequency drift over temperature	T_J = 0 to 85 °C	-3.7(3)	-	4.5(3)	%
		T_J = -40 to 125 °C	-11(3)	-	7.5(3)	
Δ_{VDD} (CSI)	CSI oscillator frequency drift over V_{DD}	V_{DD} = 1.71 to 3.6 V	-0.06	-	0.06	%
$t_{su(CSI)}$	CSI oscillator startup time	-	-	1	2	µs
$t_{stab(CSI)}$	CSI oscillator stabilization time (to reach ± 3% of f_{CSI})	-	-	-	4	cycle
$I_{DD(CSI)}$	CSI oscillator power consumption	-	-	23	30	µA

1. Guaranteed by design, unless otherwise specified.
2. Guaranteed by test in production.
3. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 63. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.3 V, T_J = 25 °C	31.4(1)	32	32.6(1)	kHz
		T_J = –40 to 110 °C, V_{DD} = 1.62 to 3.6 V	29.76(2)	-	33.6(2)	
		T_J = –40 to 125 °C, V_{DD} = 1.71 to 3.6 V	29.4(2)	-	33.6(2)	
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	80	130	µs
$t_{stab(LSI)}$(3)	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	-	130	280	nA

1. Guaranteed by test in production.
2. Guaranteed by characterization results.
3. Guaranteed by design.

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6.3.11 PLL characteristics

The parameters given in *Table 64* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*.

Table 64. PLL1 characteristics (wide VCO frequency range)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P, Q, R, S, T	VOS high		1.5	-	600(2)	MHz
		VOS low		1.5	-	400(2)	
f_{VCO_OUT}	PLL VCO output	-		192	-	836(3)	
t_{LOCK}	PLL lock time	Normal mode		15	50	150(3)	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)		25	65	170	
Jitter (RMS)	Cycle-to-cycle jitter multiplier output clock P, Q, R, S, T	f_{VCO_OUT} = 192 MHz		-	35	-	±ps
		f_{VCO_OUT} = 836 MHz		-	15	-	
	Period jitter multiplier output clock P, Q, R, S, T	f_{VCO_OUT} = 192 MHz		-	32	-	
		f_{VCO_OUT} = 836 MHz		-	10	-	
	Long term jitter multiplier output clock P, Q, R, S, T	Normal mode ($F_{PLL\ IN}$= 2 MHz), f_{VCO_OUT} = 192 MHz		-	±0.18	-	%(4)
		Normal mode ($F_{PLL\ IN}$= 16 MHz), f_{VCO_OUT} = 192 MHz		-	±0.5	-	
$I_{DD(PLL)}$	PLL power consumption	f_{VCO_OUT} = 192 MHz	V_{DDA}	-	390	548	µA
			V_{CORE}	-	590	3800	
		f_{VCO_OUT} = 836 MHz	V_{DDA}	-	1000	1100	
			V_{CORE}	-	3500	9020	

1. Guaranteed by design unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Guaranteed by characterization results.
4. Given as percent of input clock period.

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Table 65. PLL1 characteristics (narrow VCO frequency range)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P, Q, R, S, T	VOS high		1.17	-	210	MHz
		VOS low		1.17	-	210	
f_{VCO_OUT}	PLL VCO output	-		150	-	420	
t_{LOCK}	PLL lock time	Normal mode		-	60(2)	100(2)	µs
		Sigma-delta mode		Forbidden			
Jitter (RMS)	Cycle-to-cycle jitter multiplier output clock P, Q, R, S, T	f_{VCO_OUT} = 150 MHz		-	20	-	±ps
		f_{VCO_OUT} = 420 MHz		-	12	-	
	Period jitter multiplier output clock P, Q, R, S, T	f_{VCO_OUT} = 150 MHz		-	15	-	
		f_{VCO_OUT} = 420 MHz		-	8	-	
	Long-term jitter multiplier output clock P, Q, R, S, T	Normal mode (F_{PLL_IN} = 2 MHz) f_{VCO_OUT} = 150 MHz		-	±0.35	-	%(3)
		Normal mode (F_{PLL_IN} = 2 MHz) f_{VCO_OUT} = 420 MHz		-	±0.55	-	
$I_{DD(PLL)}$	PLL power consumption	f_{VCO_OUT} = 192 MHz	V_{DDA}	-	200	290	µA
			V_{CORE}	-	625	4880	
		f_{VCO_OUT} = 836 MHz	V_{DDA}	-	460	510	
			V_{CORE}	-	1690	640	

1. Guaranteed by design unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Given as percent of input clock period.

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6.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 66*. They are based on the EMS levels and classes defined in AN1709 "*EMC design guide for STM8, STM32 and Legacy MCUs*".

Table 66. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 600 MHz, BGA225 Hexa package conforming to IEC 61000-4-2	1B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 600 MHz, BGA225 Hexa package conforming to IEC 61000-4-4	5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (such as control registers)

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Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or on the oscillator pins for 1 s.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015 *"Software techniques for improving microcontrollers EMC performance").*

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 67. EMI characteristics for f_{HSE} = 8 MHz and f_{CPU} = 600 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/600 MHz	
S_{EMI}	Peak level(1)	V_{DD} = 3.6 V, T_A = 25 °C, BGA225 package, compliant with IEC61967-2	0.1 to 30 MHz	10	dBµV
			30 to 130 MHz	30	
			130 MHz to 1 GHz	22	
			1 GHz to 2 GHz	9	
	Level(2)		0.1 MHz to 2 GHz	4.0	-

1. Refer to AN1709 *EMI radiated test* chapter.
2. Refer to AN1709 *EMI level classification* chapter.

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6.3.13 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 68. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	All packages(2)	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All packages(2)	C2B	750	

1. Evaluated by characterization – not tested in production.
2. WLCSP not yet available.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 69. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	Conforming to JESD78, $T_J = T_{JMax}$	II level A

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6.3.14 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 70. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on pins: PB2, PC14, PC15, PF15, PM0, PM1, PM5 and PM6	0	0	mA
-	Injected current on all other pins	5	NA	

1. Evaluated by characterization results.

6.3.15 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 71* are derived from tests performed under the conditions summarized in *Table 26: General operating conditions*. All I/Os are CMOS and TTL compliant (except for BOOT0).

Note: For information on GPIO configuration, refer to AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption”, available from the ST website www.st.com.

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Table 71. I/O static characteristics(1)

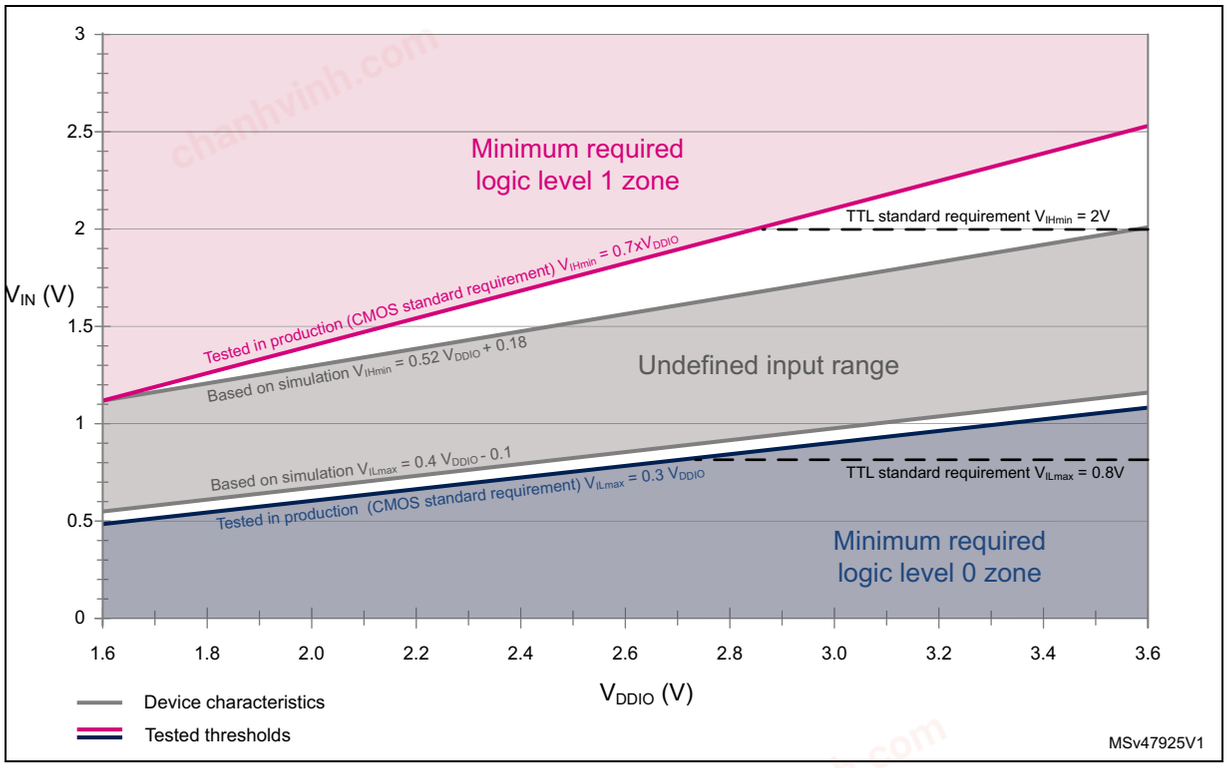
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage except BOOT0	1.08 V < V_{DD} < 3.6 V	-	-	0.3 V_{DDIOx}(2)	V
	I/O input low level voltage except BOOT0		-	-	0.4 V_{DDIOx} - 0.1(3)	
	BOOT0 I/O input low level voltage		-	-	0.19 V_{DDIOx} + 0.1(3)	
V_{IH}	I/O input high level voltage except BOOT0	1.08 V < V_{DD} < 3.6 V	0.7 V_{DDIOx}(2)	-	-	V
	I/O input high level voltage except BOOT0		0.52 V_{DDIOx} + 0.18(3)	-	-	
	BOOT0 I/O input high level voltage		0.17 V_{DDIOx} + 0.6(3)	-	-	
V_{HYS}(3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.08 V < V_{DD} < 3.6 V	-	250	-	mV
	BOOT0 I/O input hysteresis	1.71 V < V_{DD} < 3.6 V	-	200	-	
I_{leak}(4)	FT_xx Input leakage current(3)	0 < V_{IN} ≤ Max(V_{DDXXX})(7)	-	-	±250	nA
		Max(V_{DDXXX}) < V_{IN} ≤ Max(V_{DDXXX})+ 1 V) (5)(7)	-	-	2500	
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(7)	-	-	750	
	TT_xx Input leakage current	0< V_{IN} ≤ Max(V_{DDXXX}) (7)	-	-	±250	
	BOOT0	0< V_{IN} ≤ V_{DDOX}	-	-	15	µA
R_{PU}	Weak pull-up equivalent resistor(6)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	V_{IN} = V_{DD}(7)	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DDIOx} represents V_{DD} or $V_{DDXSPIx}$.
2. Compliant with CMOS requirements.
3. Specified by design - Not tested in production.
4. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_leak_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x $I_{lkg(Max)}$.
5. V_{IN} must be less than Max(V_{DDXXX}) + 3.6 V.
6. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10%).
7. Max(V_{DDXXX}) is the maximum value of all the I/O supplies.

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All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 37*.

Figure 37. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2: Absolute maximum ratings*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 24*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 24*).

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Output voltage levels

Unless otherwise specified, the parameters given in *Table 72* and *Table 73* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 72. Output voltage characteristics for all I/Os except PC13, PC14, and PC15

Symbol	Parameter	Conditions(1)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 8 mA 2.7 V≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -8 mA 2.7 V≤ V_{DD} ≤ 3.6 V	V_{DD}- 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 8 mA 2.7 V≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -8 mA 2.7 V≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}(3)	Output high level voltage	I_{IO} = -20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 1.3	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 4 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage	I_{IO} = -4 mA 1.71 V ≤ V_{DD} <3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 2 mA 1.08 V ≤ V_{DD} ≤ 1.32 V	-	0.3 $V_{DDXSPIx}$ 0.3	
V_{OH} (3)	Output high level voltage	I_{IO} = -2 mA 1.71 V ≤ V_{DD} < 1.32 V	0.7 $V_{DDXSPIx}$	-	
V_{OLFM+}(3)	Output low level voltage for an FTf I/O pin in (FT I/O with “f” option)	I_{IO} = 20 mA 2.3 V≤ V_{DD} ≤3.6 V	-	0.4	
		I_{IO} = 10 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 4.5 mA 1.08 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 24*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

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Table 73. Output voltage characteristics for PC13(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -3 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -3 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 1.5 mA 1.71 V≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	I_{IO} = −1.5 mA 1.71 V≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 24*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 74. Output voltage characteristics for PC14 and PC15(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 0.25 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	I_{IO} = -0.25 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 24*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

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Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of GPIOx_HSLVR register can be used to optimize the I/O speed when the product voltage is below 2.7 V.

Table 75. Output timing characteristics (HSLV OFF)(1)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F_{max}(2)(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	8	MHz
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	14	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	16	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
	t_r/t_f(4)(5)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	18.0	ns
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	36.0	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17.0	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	34.0	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	15.5	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	32.0	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	14.2	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	30.0	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.2	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	27	

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Table 75. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	F_{max}(2)(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V		40	MHz
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	12	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	45	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	14	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	16	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	18	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	60	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	20	
	t_r/t_f(4)(5)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	6.2	ns
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	11.4	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.7	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	10.5	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.1	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	9.5	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.5	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V		8.4	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V		3.7	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V		7.0	

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Table 75. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	F_{max}(2)(3)(6)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	80	MHz
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	30	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	90	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	35	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	40	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	110	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	45	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	133	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	50	
	t_r/t_f(4)(5)(6)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.8	ns
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	7.5	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.4	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	6.6	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.9	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5.7	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.5	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	4.7	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.9	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3.7	

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Table 75. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
11	F_{max}(2)(3)(6)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	MHz
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	40	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	120	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	50	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	140	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	60	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	166	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	70	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	200	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	80	
	t_r/t_f(4)(5)(6)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	6.3	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.8	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5.5	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.3	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	4.6	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.9	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3.7	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.4	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the conditions (t_r + t_f) ≤ 2/3 T, Skew ≤ 1/20 T, and 45% < Duty cycle < 55%.
3. When 2 V < V_{DD} < 2.7 V the maximum frequency is between values given for V_{DD} = 1.98 V and V_{DD} = 2.7 V.
4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
5. When 2 V<V_{DD}<2.7 V maximum frequency is between values given for V_{DD}=1.98 V and V_{DD}=2.7 V.
6. When 2 V<V_{DD}<2.7 V Max T_{rise}/T_{fall} is between values given for V_{DD}=1.98 V and Vdd=2.7 V.

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Output buffer timing characteristics (HSLV option enabled)

Table 76. Output timing characteristics (HSLV ON)(1)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD}≤2 V	-	8	MHz
			C = 40 pF, 1.71 V ≤ V_{DD}≤2 V	-	10	
			C = 30 pF, 1.71 V ≤ V_{DD}≤2 V	-	12	
			C = 20 pF, 1.71 V ≤ V_{DD}≤2 V	-	14	
			C = 10 pF, 1.71 V ≤ V_{DD}≤2 V	-	16	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD}≤2 V	-	17.8	ns
			C = 40 pF, 1.71 V ≤ V_{DD}≤2 V	-	15.8	
			C = 30 pF, 1.71 V ≤ V_{DD}≤2 V	-	14.4	
			C = 20 pF, 1.71 V ≤ V_{DD}≤2 V	-	13.1	
			C = 10 pF, 1.71 V ≤ V_{DD}≤2 V	-	11.4	
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD}≤2 V	-	40	MHz
			C = 40 pF, 1.71 V ≤ V_{DD}≤2 V	-	45	
			C = 30 pF, 1.71 V ≤ V_{DD}≤2 V	-	50	
			C = 20 pF, 1.71 V ≤ V_{DD}≤2 V	-	55	
			C = 10 pF, 1.71 V ≤ V_{DD}≤2 V	-	60	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD}≤2 V	-	7.2	ns
			C = 40 pF, 1.71 V ≤ V_{DD}≤2 V	-	6.5	
			C = 30 pF, 1.71 V ≤ V_{DD}≤2 V	-	5.6	
			C = 20 pF, 1.71 V ≤ V_{DD}≤2 V	-	4.8	
			C = 10 pF, 1.71 V ≤ V_{DD}≤2 V	-	3.8	
10	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD}≤2 V	-	60	MHz
			C = 40 pF, 1.71 V ≤ V_{DD}≤2 V	-	70	
			C = 30 pF, 1.71 V ≤ V_{DD}≤2 V	-	90	
			C = 20 pF, 1.71 V ≤ V_{DD}≤2 V	-	110	
			C = 10 pF, 1.71 V ≤ V_{DD}≤2 V	-	140	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD}≤2 V	-	5.3	ns
			C = 40 pF, 1.71 V ≤ V_{DD}≤2 V	-	4.6	
			C = 30 pF, 1.71 V ≤ V_{DD}≤2 V	-	3.8	
			C = 20 pF, 1.71 V ≤ V_{DD}≤2 V	-	3.0	
			C = 10 pF, 1.71 V ≤ V_{DD}≤2 V	-	2.2	

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Table 76. Output timing characteristics (HSLV ON)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
11	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD}≤2 V	-	67	MHz
			C = 40 pF, 1.71 V ≤ V_{DD}≤2 V	-	100	
			C = 30 pF, 1.71 V ≤ V_{DD}≤2 V	-	120	
			C = 20 pF, 1.71 V ≤ V_{DD}≤2 V	-	155	
			C = 10 pF, 1.71 V ≤ V_{DD}≤2 V	-	200	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD}≤2 V	-	5.0	ns
			C = 40 pF, 1.71 V ≤ V_{DD}≤2 V	-	4.1	
			C = 30 pF, 1.71 V ≤ V_{DD}≤2 V	-	3.3	
			C = 20 pF, 1.71 V ≤ V_{DD}≤2 V	-	2.5	
			C = 10 pF, 1.71 V ≤ V_{DD}≤2 V	-	1.8	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45% < Duty cycle < 55%
3. The fall and rise times are defined, respectively, between 90 and 10% and between 10 and 90% of the output waveform.
4. Compensation system enabled.

Table 77. Output timing characteristics $V_{DDXSPIx}$ 1.2 V range (HSLV OFF)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	1	MHz
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	1	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	1	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	1	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	1	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	83.0	ns
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	79.0	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	46.0	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	72.0	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	68.0	

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Table 77. Output timing characteristics $V_{DDXSPIx}$ 1.2 V range (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	MHz
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	24.5	ns
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	22.2	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	20.0	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	17.8	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	15.0	
10	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	10	MHz
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	10	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	10	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	10	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	10	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	16.2	ns
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	14.3	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	12.2	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	10.0	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	7.9	
11	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	20	MHz
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	23	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	25	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	28	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	30	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	14.0	ns
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	12.0	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	10.0	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	8.0	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	6.0	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the following conditions:
   $(t_r+t_f) \leq 2/3$ T
   Skew ≤ 1/20 T
   45% < Duty cycle < 55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

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Table 78. Output timing characteristics $V_{DDXSPIx}$ 1.2 V (HSLV ON)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	MHz
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	32.5	ns
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	30.0	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	27.5	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	25.0	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	22.5	
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	15.0	MHz
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	17.5	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	20.0	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	22.5	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	25.0	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	14.6	ns
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	12.9	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	11.2	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	9.3	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	7.3	
10	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	25	MHz
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	30	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	33	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	44	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	55	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	11.6	ns
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	9.7	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	7.8	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	6.1	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	4.3	

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Table 78. Output timing characteristics $V_{DDXSPIx}$ 1.2 V (HSLV ON)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
11	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	30	MHz
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	35	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	44	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	55	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	77	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	11.1	ns
			C = 40 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	9.2	
			C = 30 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	7.2	
			C = 20 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	5.4	
			C = 10 pF, 1.08 V ≤ $V_{DDXSPIx}$≤1.32 V	-	3.6	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the following conditions:
   $(t_r+t_f) \le 2/3$ T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

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6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 71: I/O static characteristics*).

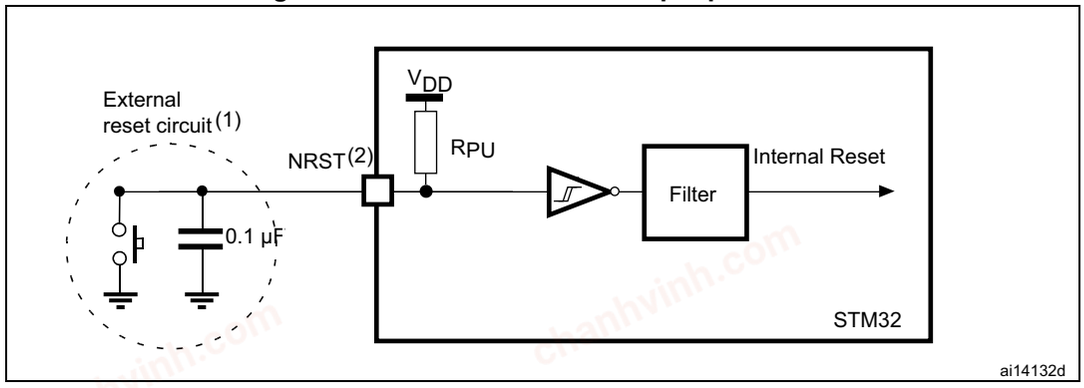
Unless otherwise specified, the parameters in *Table 79* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: Voltage characteristics*.

Table 79. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST input not filtered pulse	1.71 V < V_{DD} < 3.6 V	350	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. The PMOS contribution to the series resistance is minimum (~10 % order).
2. Specified by design - Not tested in production.

Figure 38. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 71*, otherwise the reset is not taken into account by the device.

6.3.17 FMC characteristics

Unless otherwise specified, the parameters given in *Table 80* to *Table 93* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS high.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics.

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Asynchronous waveforms and timings

Figure 39 through *Figure 41* represent asynchronous waveforms and *Table 80* through *Table 87* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all timing tables, the T_{KERCK} is the $f_{mc_ker_ck}$ clock period.

Table 80. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck}-1$	$3T_{fmc_ker_ck}+1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc_ker_ck}-1$	$2T_{fmc_ker_ck}+1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$2T_{fmc_ker_ck}-1$	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck}+12.5$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	12.5	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	1	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck}+1$	

1. Guaranteed by characterization results.

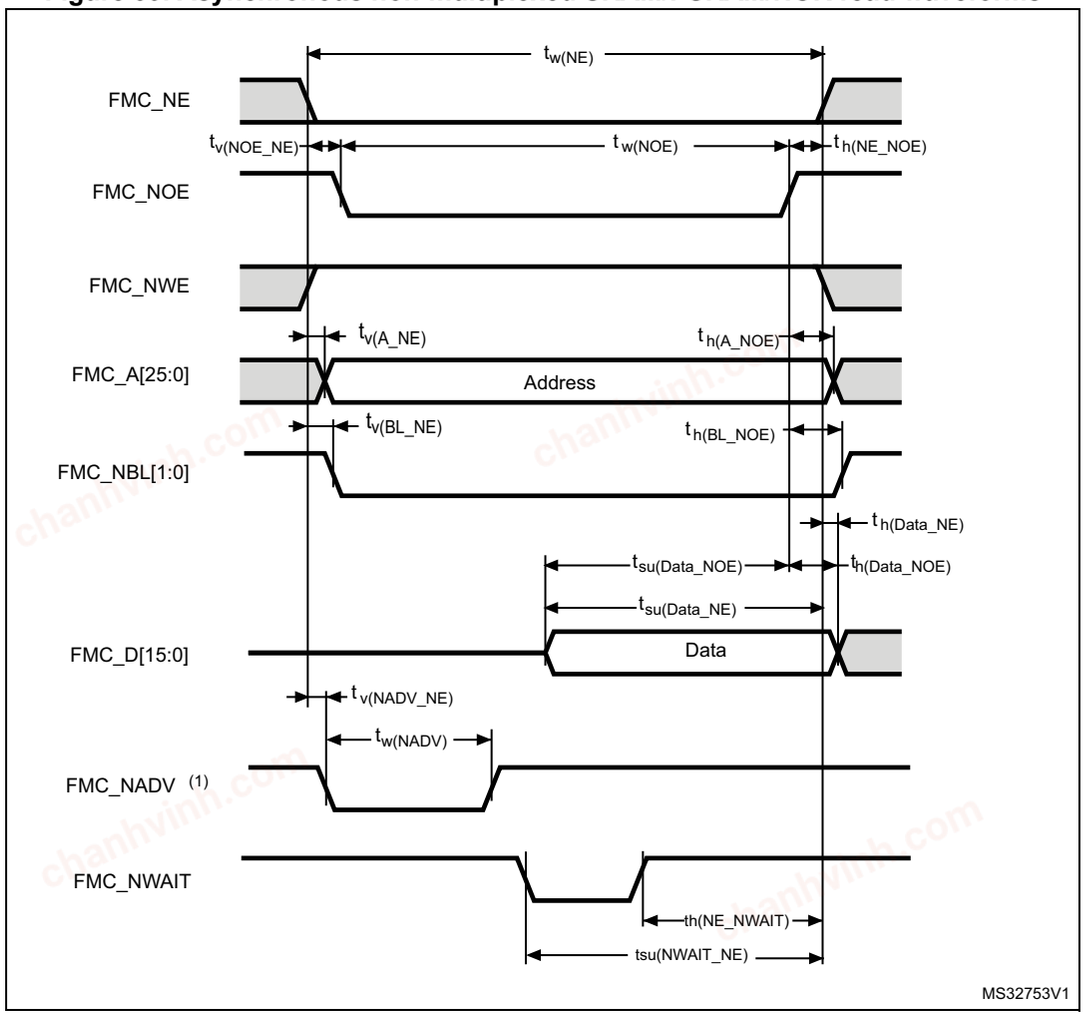
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Table 81. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck}-1$	$8T_{fmc_ker_ck}+1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$7T_{fmc_ker_ck}-1$	$7T_{fmc_ker_ck}+1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck}$	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck}+12$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}+12$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 fmc_ker_ck cycle.

Figure 39. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

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Table 82. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck} - 1$	$3T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} + 1$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck}$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{fmc_ker_ck} + 0.5$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck} + 2$	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 0.5$	

1. Guaranteed by characterization results.

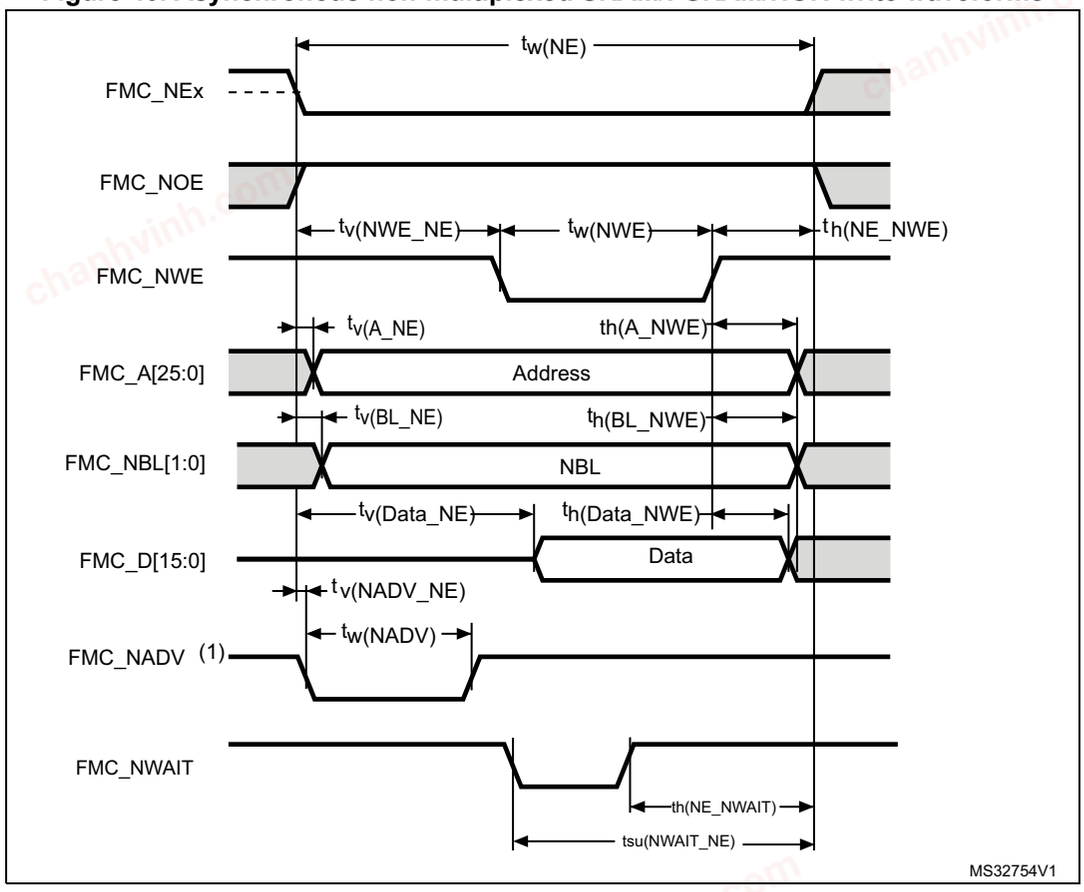
Table 83. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck} - 1$	$8T_{fmc_ker_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc_ker_ck} - 1$	$6T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 13$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck} + 13$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 fmc_ker_ck cycle.

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Figure 40. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

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Table 84. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck} - 1$	$4T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck} + 1$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	$T_{fmc_ker_ckk} - 3$	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$2T_{fmc_ker_ck} - 1$	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} + 12$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	12	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results.

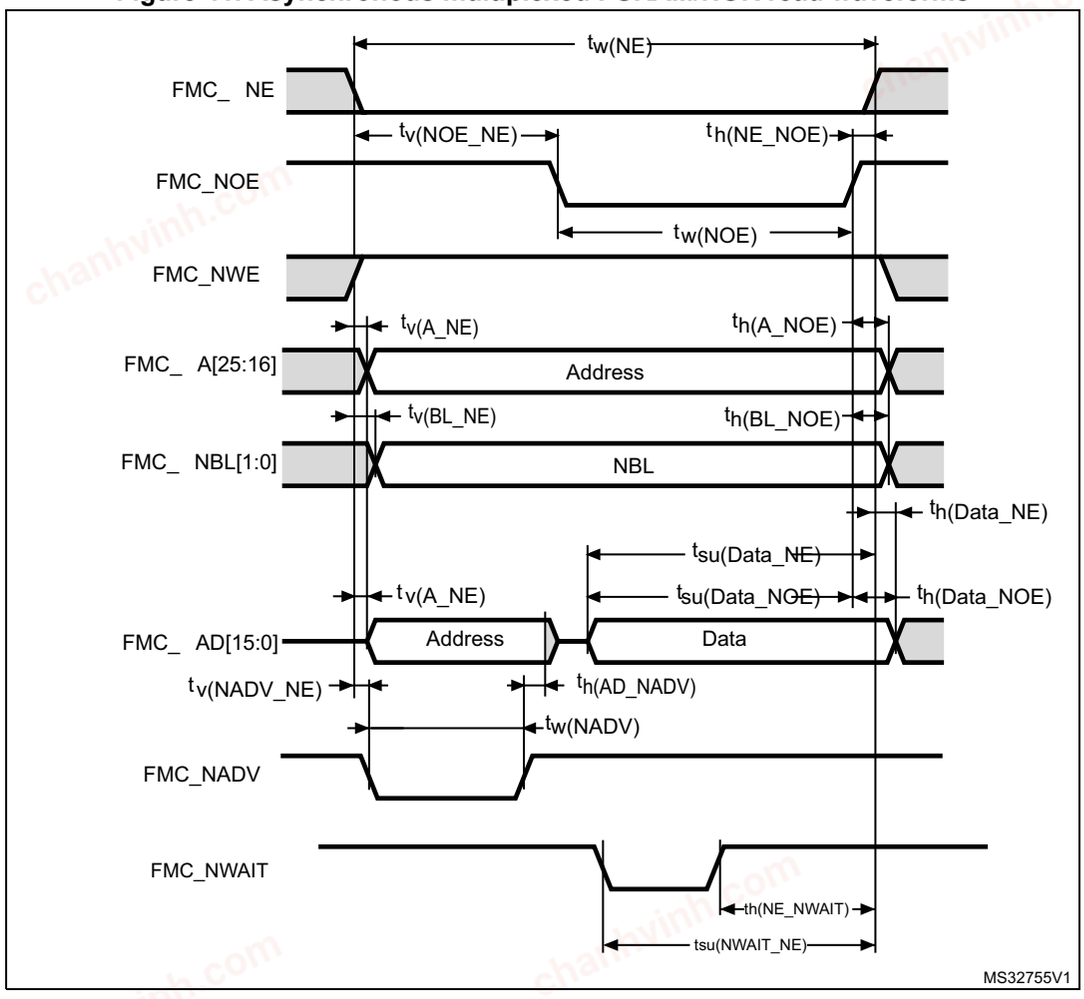
Table 85. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck} - 1$	$9T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$6T_{fmc_ker_ck} - 1$	$6T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 13$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck} + 13$	-	

1. Guaranteed by characterization results.

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Figure 41. Asynchronous multiplexed PSRAM/NOR read waveforms



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Table 86. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck} - 1$	$4T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} + 1$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 0.5$	
$t_{h(AD_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	$T_{fmc_ker_ck} - 1.5$	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck}$	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_c} + 0.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc_ker_ck} + 0.5$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck} + 2$	-	

1. Guaranteed by characterization results.

Table 87. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck} - 1$	$9T_{fmc_ker_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc_ker_ck} - 1$	$7T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 13$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck} + 13$	-	

1. Guaranteed by characterization results.
2. N_{WAIT} pulse width is equal to 1 fmc_ker_ck cycle.

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Synchronous waveforms and timings

Figure 44 through *Figure 43* represent synchronous waveforms and *Table 90* through *Table 89* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash, DataLatency = 0 for PSRAM, C_L = 30 pF

In all the timing tables, the $T_{fmc_ker_ck}$ is the $f_{mc_ker_ck}$ clock period, with the following FMC_CLK maximum values:

- For 2.7 V<V_{DD}<3.6 V: maximum FMC_CLK = 125 MHz at C_L = 20 pF
- For 2.7 V<V_{DD}<3.6 V: maximum FMC_CLK = 125 MHz at C_L = 15 pF
- For 1.71 V<V_{DD}<1.9 V: maximum FMC_CLK = 100 MHz at C_L = 20 pF
- For 1.71 V<V_{DD}<1.9 V: maximum FMC_CLK = 105 MHz at C_L = 15 pF

Note: At VOS low, the performance can be degraded by up to 7% compared to VOS high.

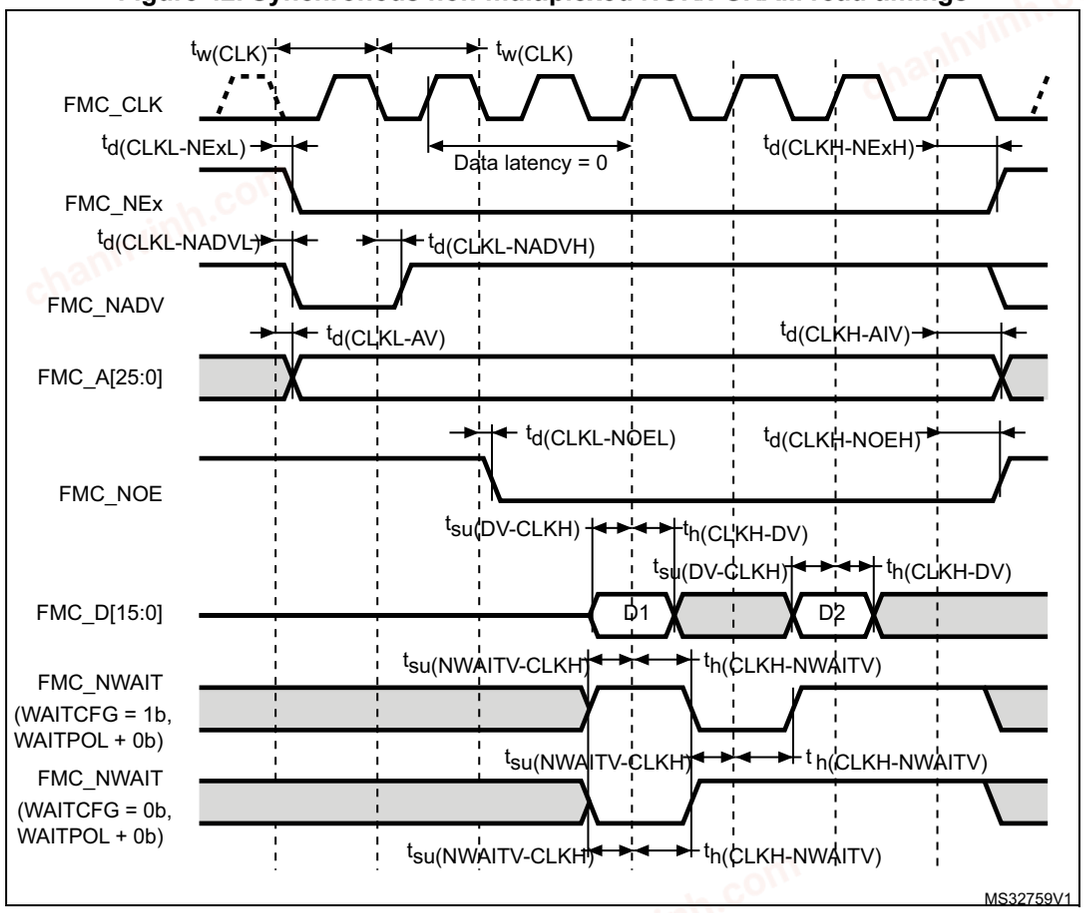
Table 88. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max(2)	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck}$ –0.5	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc_ker_ck}$+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK ow to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc_ker_ck}$	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	2.5	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	1.5	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

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Figure 42. Synchronous non-multiplexed NOR/PSRAM read timings



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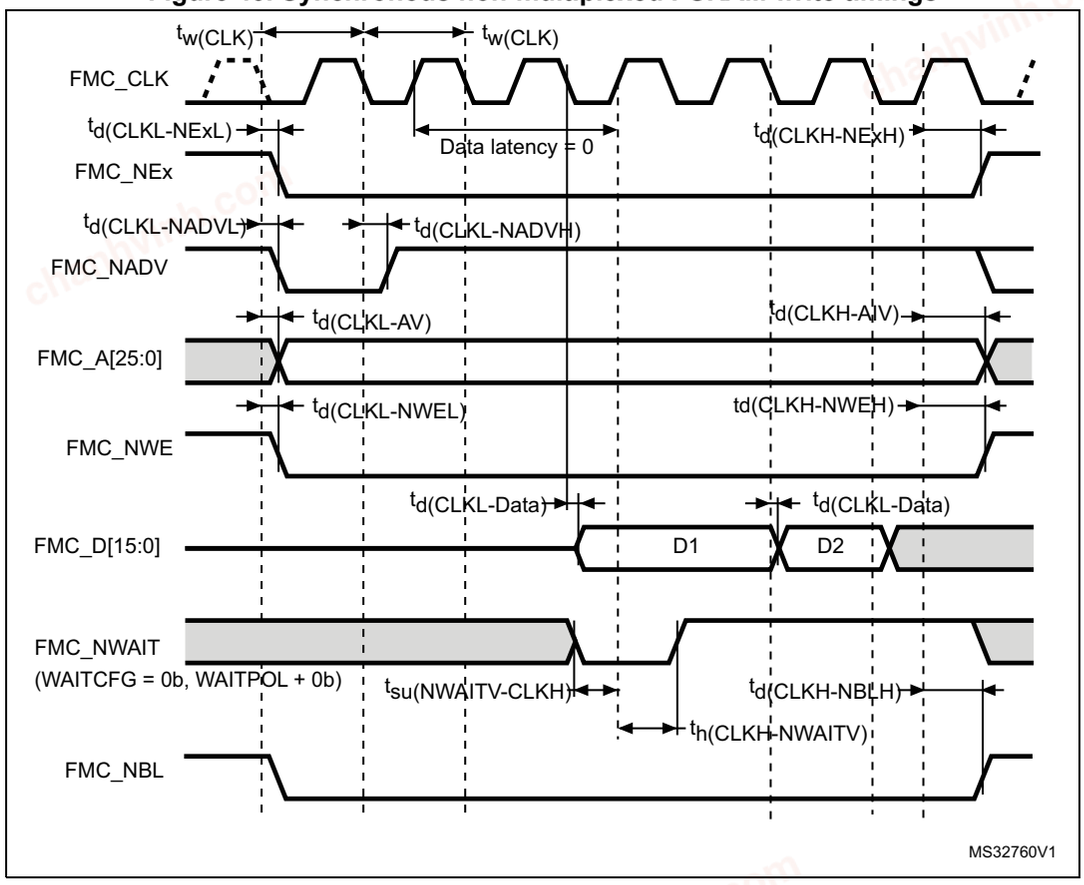
Table 89. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max(2)	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc_ker_ck}+1$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	2	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck}+0.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

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Figure 43. Synchronous non-multiplexed PSRAM write timings



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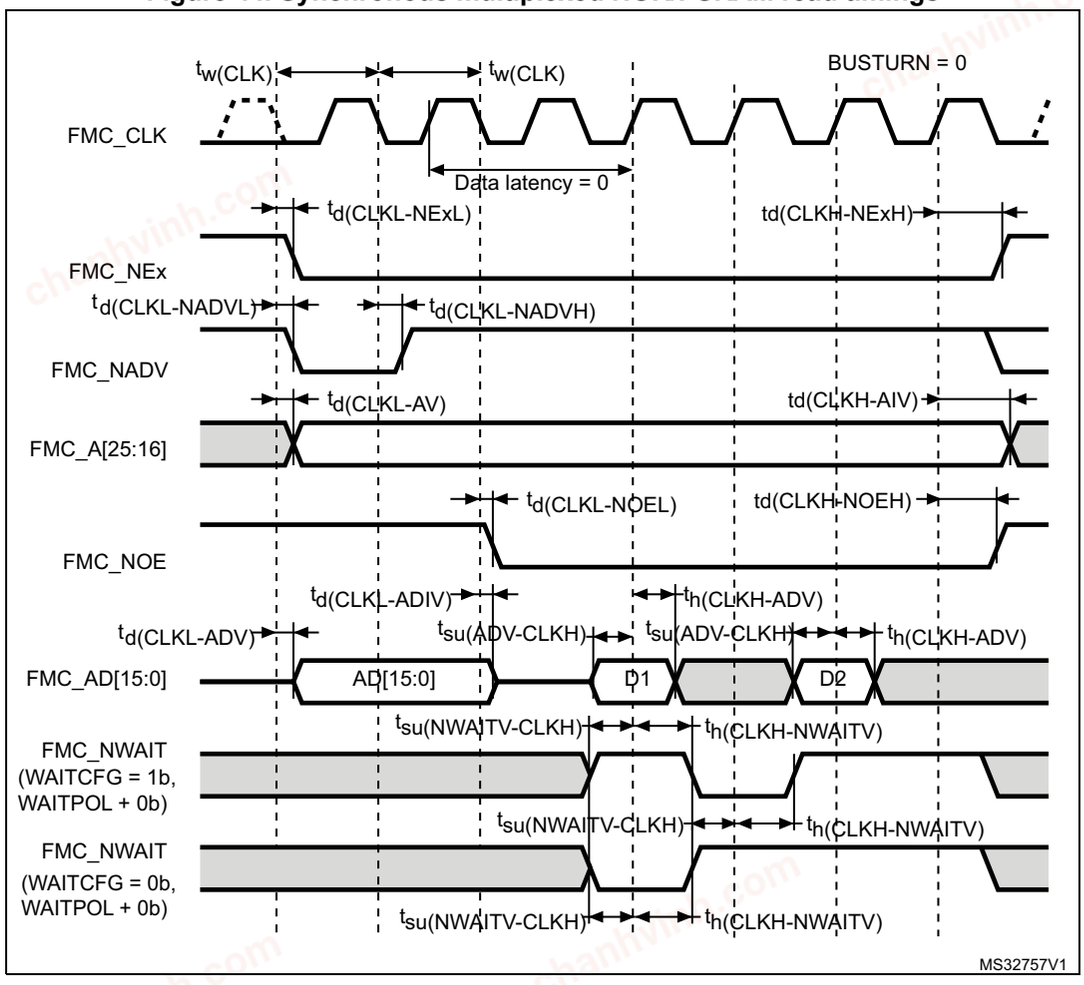
Table 90. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max(2)	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc_ker_ck}+1$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	2.5	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	1.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

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Figure 44. Synchronous multiplexed NOR/PSRAM read timings



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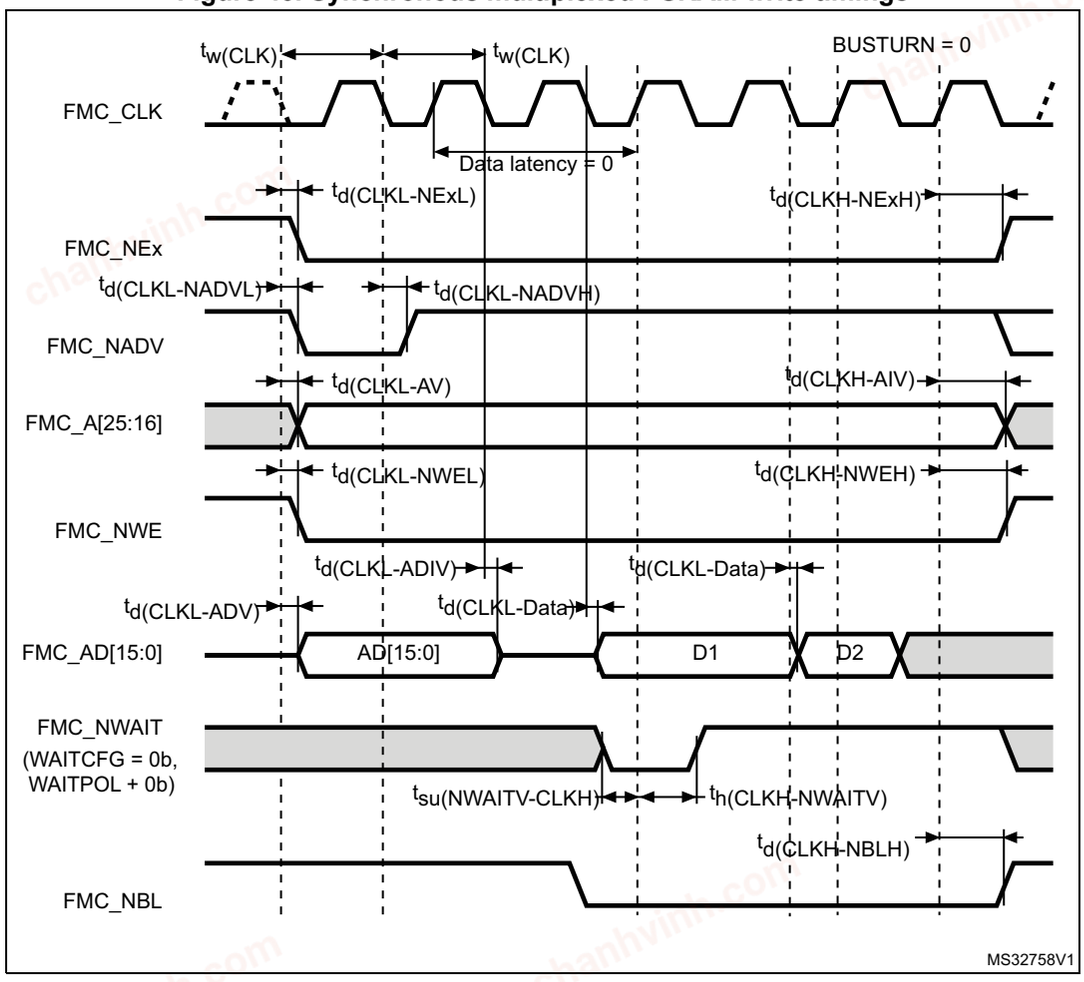
Table 91. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max(2)	Unit
$t_{w(CLK)}$	FMC_CLK period, V_{DD} = 2.7 to 3.6 V	$2T_{fmc_ker_ck}$ –0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x =0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$T_{fmc_ker_ck}$ +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	1	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x =16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x =16…25)	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck}$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to to FMC_AD[15:0] valid	-	2	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	2	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck}$ +0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

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Figure 45. Synchronous multiplexed PSRAM write timings



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NAND controller waveforms and timings

Figure 46 through *Figure 49* represent synchronous waveforms, and *Table 92* and *Table 93* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration and a capacitive load (C_L) of 30 pF:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Table 92. Switching characteristics for NAND flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc_ker_ck} - 0.5$	$4T_{fmc_ker_ck}+0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12.5	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc_ker_ck}$ +0.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc_ker_ck}-1$	-	

1. Guaranteed by characterization results.

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Figure 46. NAND controller waveforms for read access

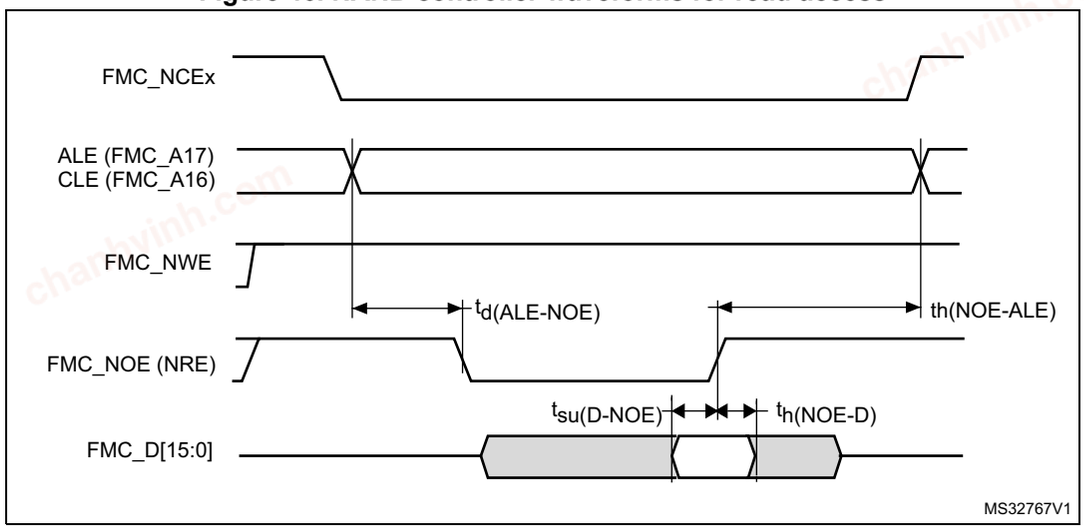


Figure 47. NAND controller waveforms for common memory read access

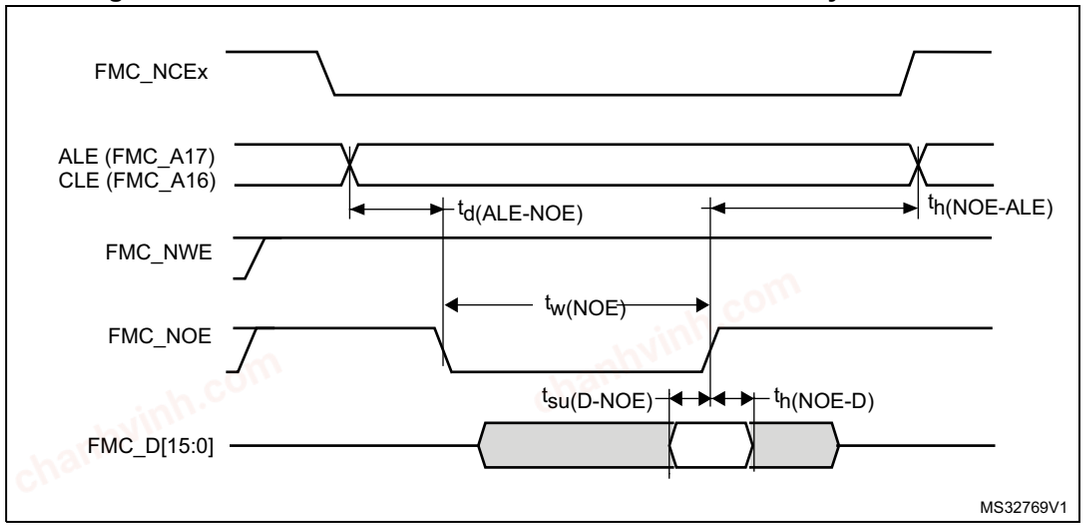


Table 93. Switching characteristics for NAND flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc_ker_ck} - 0.5$	$4T_{fmc_ker_ck} + 0.5$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc_ker_ck} + 1$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc_ker_ck} - 2$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc_ker_ck} - 1$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc_ker_ck} + 1.5$	-	

1. Guaranteed by characterization results.

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Figure 48. NAND controller waveforms for write access

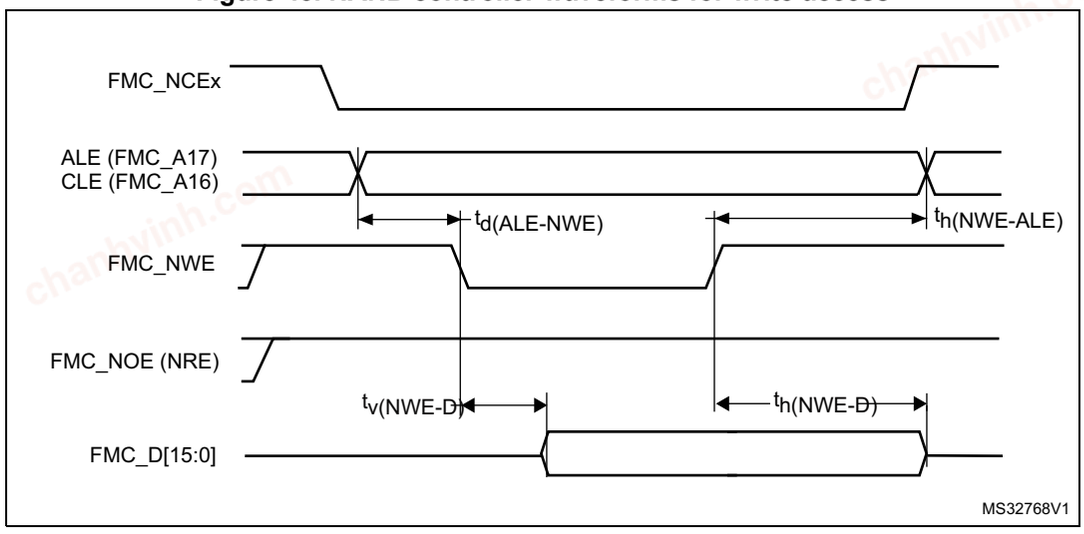
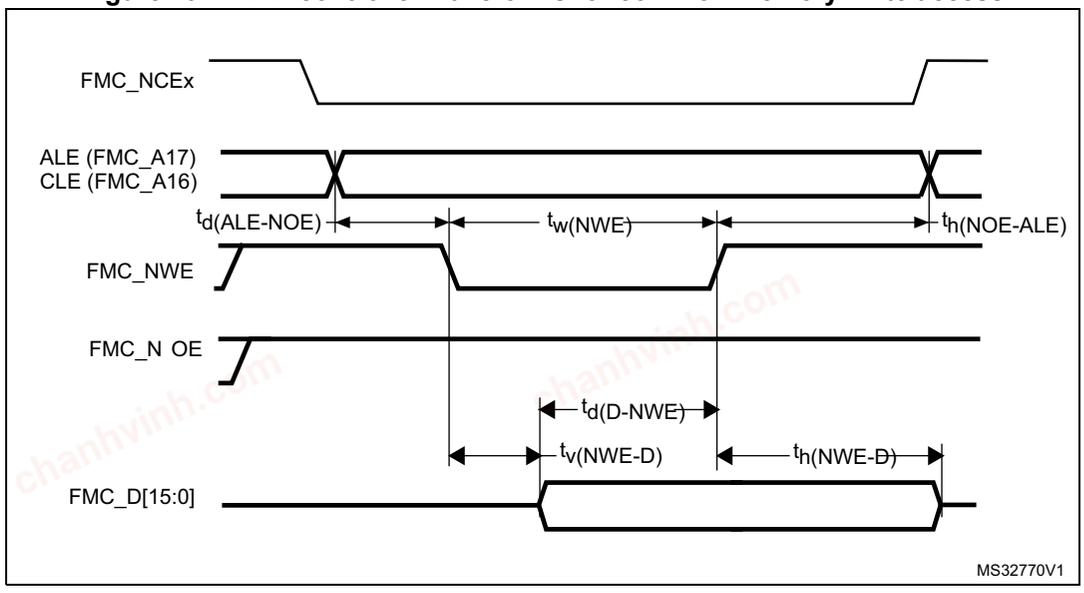


Figure 49. NAND controller waveforms for common memory write access



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SDRAM waveforms and timings

In all timing tables, $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period, with the following FMC_SDCLK maximum values:

- For 2.7 V<V_{DD}<3.6 V: maximum FMC_CLK = 95 MHz at 20 pF
- For 2.7 V<VDD<3.6 V: maximum FMC_CLK = 100 MHz at 15 pF
- For 1.71 V<V_{DD}<1.9 V: maximum FMC_CLK = 90 MHz at 20 pF
- For 1.71 V<$_{DD}$<1.9 V: maximum FMC_CLK = 95 MHz at 15 pF

Note: At VOS low, the performance can be degraded by up to 7 % compared to VOS high.

Table 94. SDRAM read timings(1)

Symbol	Parameter	Min	Max(2)	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck} + 0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	2.5	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	0.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

Table 95. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max(2)	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck} + 0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	1	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

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Figure 50. SDRAM read access waveforms (CL = 1)

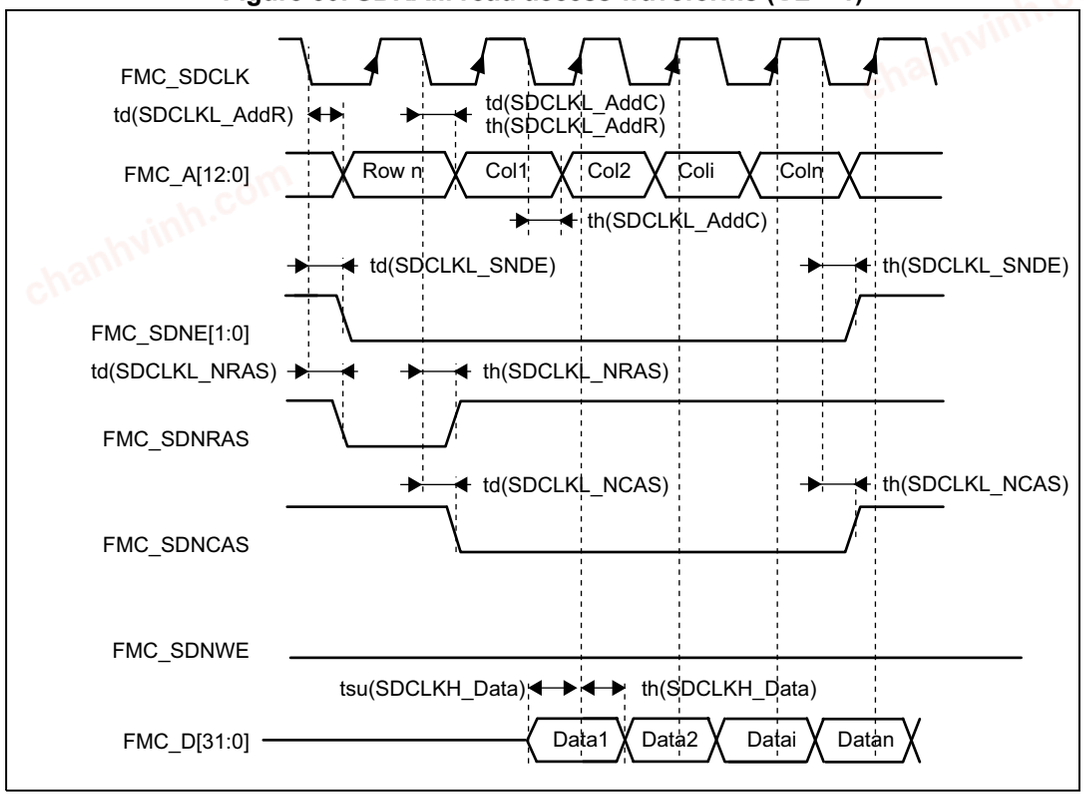


Table 96. SDRAM Write timings(1)

Symbol	Parameter	Min	Max(2)	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck}+0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	1.5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL-_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

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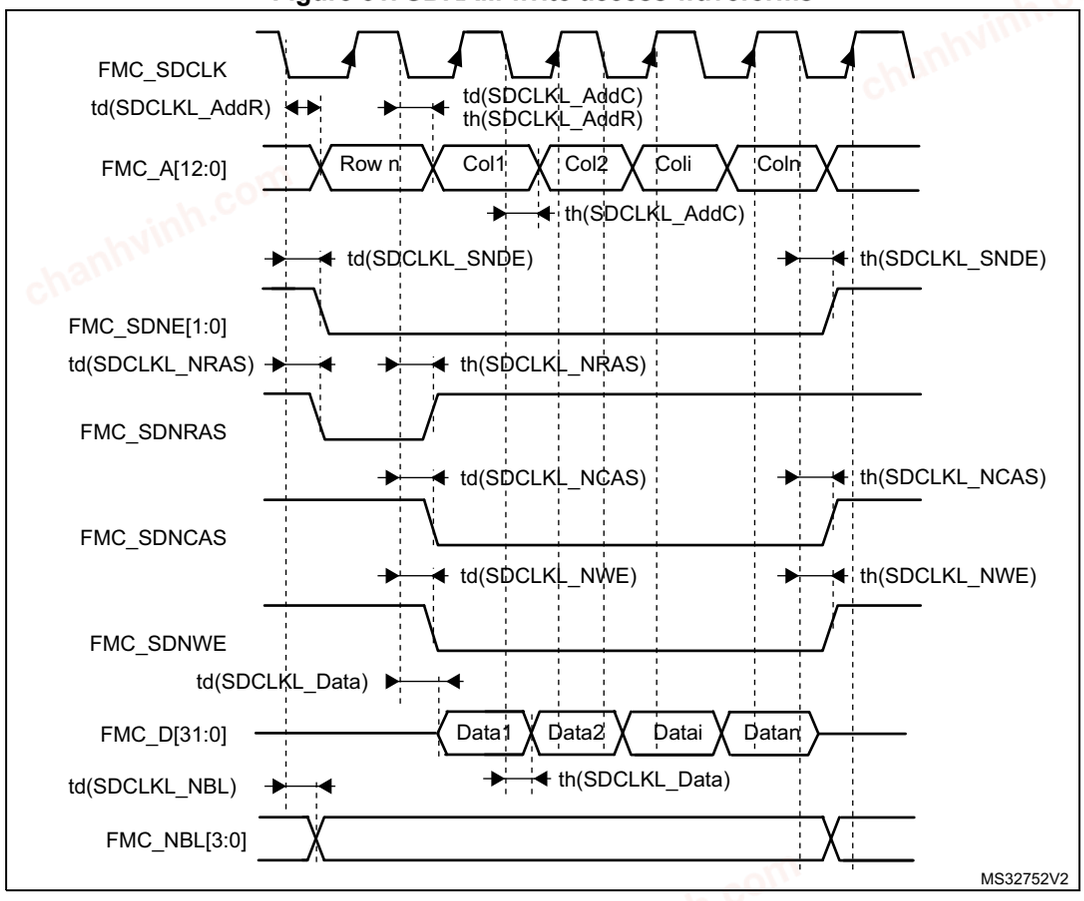
Table 97. LPSDR SDRAM Write timings(1)

Symbol	Parameter	Min	Max(2)	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck}+0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	1.5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL-SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

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Figure 51. SDRAM write access waveforms



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6.3.18 XSPI interface characteristics

Unless otherwise specified, the parameters given in *Table 98* and *Table 100* for XSPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS high

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 98. XSPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
$F_{(CLK)}$	XSPI clock frequency	2.7 V < V_{DD} < 3.6 V, 2.7 V<$V_{DDXSPI1/2}$<3.6 V, C_{LOAD} = 15 pF	-	-	180(3)	MHz
		1.71 V < V_{DD} < 3.6 V, 1.62 V<$V_{DDXSPI1/2}$<3.6 V, C_{LOAD} =15 pF	-	-	145(3)	
$t_{w(CLKH)}$	XSPI clock high and low time, even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}/2$	-	$t_{(CLK)}/2+1$	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2–1$	-	$t_{(CLK)}/2$	
$t_{w(CLKH)}$	XSPI clock high and low time, odd division	PRESCALER[7:0] = n = 2,4,6,8	$(n/2)*t_{(CLK)}/(n+1)$	-	$(n/2)*t_{(CLK)}/(n+1)+1$	
$t_{w(CLKL)}$			$(n/2+1)*t_{(CLK)}/(n+1)–1$	-	$(n/2+1)*t_{(CLK)}/(n+1)$	
$t_{s(IN)}$	Data input setup time	-	2.0	-	-	
$t_{h(IN)}$	Data input hold time	-	2.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0.5	1	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

1. Guaranteed by characterizatin results.
2. At VOS Low, these values are degraded by up to 7%.
3. Tuning COARSE[4:0] and FINE[6:0] of the XSPI_CALMR register is required to achieve this frequency

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Table 99. XSPI characteristics in DTR mode (no DQS)(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
$F_{(CLK)}$	XSPI clock frequency	1.71 V < V_{DD} < 3.6 V, 1.62 V<$V_{DDXSPI1/2}$<3.6 V, C_{LOAD} = 15 pF	-	-	135(3)	MHz
$t_{w(CLKH)}$	XSPI clock high and low time, even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}/2$	-	$t_{(CLK)}/2+1$	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2–1$	-	$t_{(CLK)}/2$	
$t_{w(CLKH)}$	XSPI clock high and low time, odd division	PRESCALER[7:0] = n = 2,4,6,8	$(n/2)*t_{(CLK)}/(n+1)$	-	$(n/2)*t_{(CLK)}/(n+1)+1$	
$t_{w(CLKL)}$			$(n/2+1)*t_{(CLK)}/(n+1) – 1$	-	$(n/2+1)*t_{(CLK)}/(n+1)$	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input setup time	-	2.0	-	-	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	-	2.5	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	-	-	$t_{(CLK)}/4+ 0.5$	$t_{(CLK)}/4+1.5$	
		Prescaler = 0, $F_{(CLK)}$<60 MHz		5	7	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	-	$t_{(CLK)}/4 - 0.5$	-	-	
		Prescaler = 0, $F_{(CLK)}$<60 MHz	3.5			

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.
3. Tuning COARSE[4:0] and FINE[6:0] of the XSPI_CALMR register is required to achieve this frequency.

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Table 100. XSPI characteristics in DTR mode (with DQS)/Hyperbus(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
$F_{(CLK)}$	XSPI clock frequency	1.71 V < V_{DD} < 3.6 V, 1.62 V<$V_{DDXSPI1/2}$<3.6 V, C_{LOAD} = 10 pF	-	-	190	MHz
		1.71 V < V_{DD} < 3.6 V, 1.62 V<$V_{DDXSPI1/2}$<3.6 V, C_{LOAD} = 15 pF	-	-	185	
$t_{w(CLKH)}$	XSPI clock high and low time, even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}/2$	-	$t_{(CLK)}/2+1$	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2–1$	-	$t_{(CLK)}/2$	
$t_{w(CLKH)}$	XSPI clock high and low time, odd division	PRESCALER[7:0] = n = 2,4,6,8	$(n/2)*t_{(CLK)}/(n+1)$	-	$(n/2)*t_{(CLK)}/(n+1)+1$	ns
$t_{w(CLKL)}$			$(n/2+1)*t_{(CLK)}/(n+1)–1$	-	$(n/2+1)*t_{(CLK)}/(n+1)$	
$t_{v(CK)}$	Clock valid time	-	-	-	$t_{(CLK)}+1$	
$t_{h(CK)}$	Clock hold time	-	$t_{(CLK)}/2$	-	-	
$V_{ODr(CK)}$	CK,$\overline{CK}$ crossing level on CK rising edge	V_{DD}=$V_{DDXSPI1}$ =$V_{DDXSPI2}$=1.8 V	1024	-	1353	mV
$V_{ODf(CK)}$	CK,$\overline{CK}$ crossing level on CK falling edge	V_{DD}=$V_{DDXSPI1}$ =$V_{DDXSPI2}$=1.8 V	907	-	1229	
$t_{w(CS)}$	Chip select high time	-	$3*t_{(CLK)}$	-	-	ns
$t_{v(DQ)}$	Data input vallid time	-	0	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	3 x $t_{(CLK)}$	
$t_{sr(DQ)}$, $t_{sf(DQ)}$	Data input setup time	-	1.5 - $t_{(CLK)}/4$	-	-	
		$F_{(CLK)}$ < 60 MHz	-3			
$t_{hr(DQ)}$, $t_{hf(DQ)}$	Data input hold time	-	1.5 + $t_{(CIK)}/4$	-	-	
		$F_{(CLK)}$ < 60 MHz	7.5			
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	-	-	$t_{(CIK)}/4+0.5$	$t_{(CIK)}/4+1.5$	
		Prescaler = 0, $F_{(CLK)}$ < 60 MHz		5	7	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	-	$t_{(CIK)}/4-1$	-		
		Prescaler = 0, $F_{(CLK)}$ < 60 MHz	3.5			

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

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Figure 52. XSPI DTR (with DQS) write timing diagram

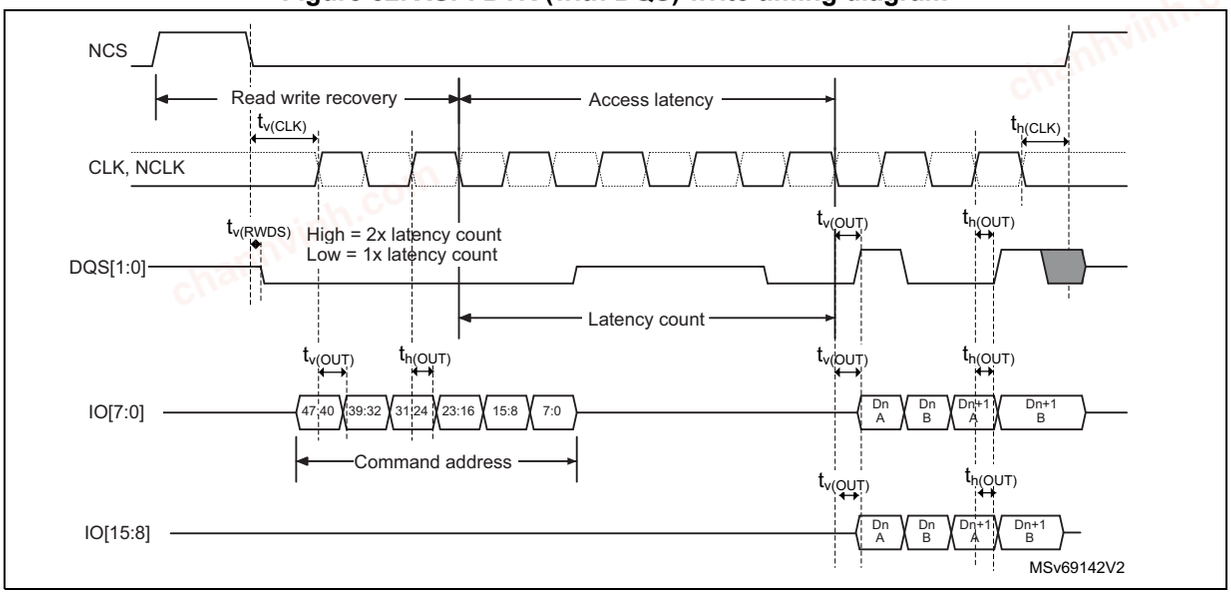


Figure 53. XSPI DTR (with DQS) read timing diagram

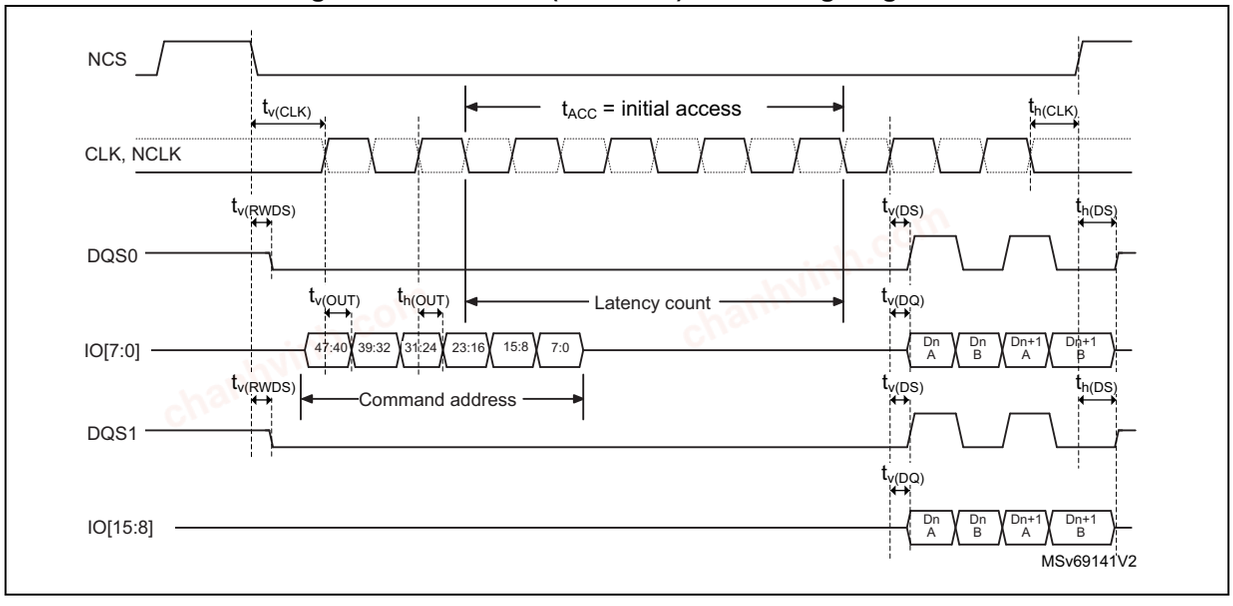
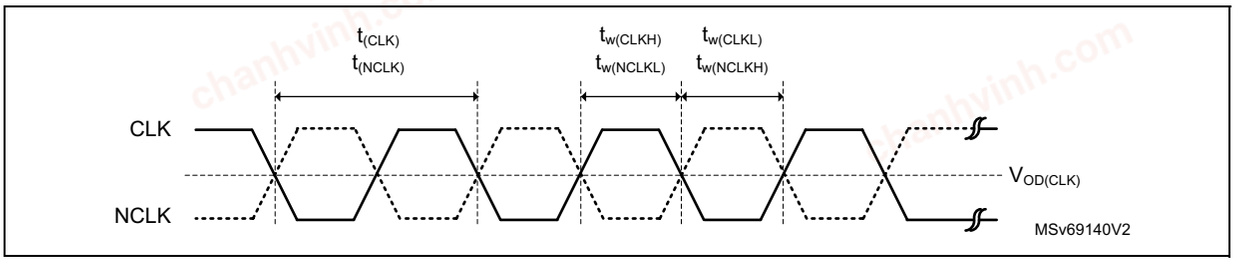


Figure 54. XSPI DTR clock timing diagram



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6.3.19 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 101* for the delay block are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 26: General operating conditions*, with the following configuration:

Table 101. Delay block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	2400	2500	3000	ps
t_{Δ}	Unit Delay	-	41	48	57	

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6.3.20 ADC characteristics

Unless otherwise specified, the parameters given in *Table 102*, *Table 103* and *Table 104* are derived from tests performed under the ambient temperature and V_{DDA} supply voltage conditions summarized in *Table 26: General operating conditions*. In *Table 102*, *Table 103* and *Table 104*, f_{ADC} refers to $f_{adc_ker_ck}$.

Table 102. ADC characteristics(1)(2)

Symbol	Parameter	Conditions						Min	Typ	Max	Unit
V_{DDA}	Analog power supply for ADC ON	-						1.62	-	3.6	V
V_{REF+}	Positive reference voltage	-						1.62	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-						V_{SSA}			V
f_{ADC}	ADC clock frequency	1.62 V ≤ V_{DDA} ≤ 3.6 V						1.5	-	75	MHz
f_S(3) with R_{AIN}=47Ω and C_{PCB}=22 pF	Sampling rate for fast channels (V_{IN}[0:5])	Resolution = 12 bits	Continuous mode	1.8 V≤V_{DDA}≤3.6 V	-40°C ≤ T_J ≤ 130°C	f_{ADC}= 75 MHz	SMP=2.5	-	5.00	-	MSPS
				1.6 V≤V_{DDA}≤3.6 V		f_{ADC}= 70 MHz		-	4.66		
			Single or discontinuous mode	2.4 V≤V_{DDA}≤3.6V		f_{ADC}= 60 MHz		-	4.00	-	
				1.6 V≤V_{DDA}≤3.6 V		f_{ADC}= 50 MHz		-	3.33	-	
		Resolution = 10 bits	Continuous Mode	1.6V≤V_{DDA}≤3.6 V	-40°C ≤ T_J ≤ 130°C	f_{ADC}= 75 MHz	SMP=2.5	-	5.77	-	
			Single or discontinuous mode	2.4 V≤V_{DDA}≤3.6 V		f_{ADC}= 75 MHz			5.77	-	
				1.6 V≤V_{DDA}≤3.6 V		f_{ADC}= 65 MHz			5.00	-	
		Resolution = 8 bits	All modes	1.6 V≤V_{DDA}≤3.6V	-40°C ≤ T_J ≤ 130°C	f_{ADC}= 75 MHz	SMP=2.5	-	6.82	-	
		Resolution = 6 bits	All modes	1.6 V≤V_{DDA}≤3.6V	-40°C ≤ T_J ≤ 130°C	f_{ADC}= 75 MHz		-	8.33	-	
	Sampling rate for slow channels	Resolution = 12 bits	All modes	1.6 V≤V_{DDA}≤3.6 V	-40°C ≤ T_J ≤ 130°C	f_{ADC}= 35MHz	SMP=2.5	-	2.30	-	
		Resolution = 10 bits				f_{ADC}= 35MHz		-	2.70	-	
		Resolution = 8 bits				f_{ADC}= 50MHz		-	4.50	-	
		Resolution = 6 bits				f_{ADC}= 50MHz		-	5.50	-	
t_{TRIG}	External trigger period	Resolution = 12 bits						-	-	15	$1/f_{ADC}$

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Table 102. ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AIN}(2)	Conversion voltage range	-	0	-	VREF+	V
V_{CMIV}	Common mode input voltage	-	V_{REF}/2–10%	V_{REF}/2	V_{REF}/2 + 10%	
R_{AIN}(4)	External input impedance	Resolution = 12 bits, T_J = 140°C (Tolerance 4 LSBs)	-	-	321	Ω
		Resolution = 12 bits, T_J = 125°C	-	-	220	
		Resolution = 10 bits, T_J = 125°C	-	-	2100	
		Resolution = 8 bits, T_J = 125°C	-	-	12000	
		Resolution = 6 bits, T_J = 125°C	-	-	80000	
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
$t_{ADCVREG_STUP}$	ADC LDO startup time	-	-	5	10	µs
t_{STAB}	ADC power-up time	LDO already started	1	-	-	Conversion cycles
t_{OFF_CAL}	Offset calibration time	-	1335			f_{ADC} clock cycles
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	
		CKMODE = 01	-	-	2.5	
		CKMODE = 10			2.5	
		CKMODE = 11			2.25	
$t_{LATRINJ}$	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	2.5	3	3.5	
		CKMODE = 01	-	-	3.5	
		CKMODE = 10	-	-	3.5	
		CKMODE = 11	-	-	3.25	
t_S	Sampling time	-	2.5	-	640.5	
t_{CONV}	Total conversion time (including sampling time)	N-bits resolution	t_S + 0.5 + N			

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Table 102. ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA_D}(ADC)	ADC consumption on VDDA and VREF, Differential mode	fs= 5 MSPS	-	600	-	µA
		fs= 1 MSPS	-	190	-	
		fs= 0.1 MSPS	-	50	-	
$I_{DDA_SE(ADC)}$	ADC consumption on VDDA and VREF Single-ended mode	fs= 5 MSPS	-	500	-	
		fs= 1 MSPS	-	150	-	
		fs= 0.1 MSPS	-	50	-	
$I_{DD(ADC)}$	ADC consumption on VDD	f_{ADC}=75 MHz	-	265	-	
		f_{ADC}=50 MHz		175	-	
		f_{ADC}=25 MHz	-	90	-	
		f_{ADC}=12.5 MHz	-	45	-	
		f_{ADC}=6.25 MHz	-	22	-	
		f_{ADC}=3.125 MHz	-	11	-	

1. Guaranteed by design.
2. The voltage booster on ADC switches must be used for VDDA < 2.4 V (embedded I/O switches).
3. These values are valid on BGA packages
4. The tolerance is 2 LSBs for 12-bit, 10-bit and 8-bit resolutions, unless otherwise specified.

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Table 103. Minimum sampling time vs R_{AIN} (12-bit ADC)[1][2]

Resolution	RAIN (Ω)	Minimum sampling time (s)	
		Fast channels[3]	Slow channels[4]
12 bits	47	3.75E-08	6.12E-08
	68	3.94E-08	6.25E-08
	100	4.36E-08	6.51E-08
	150	5.11E-08	7.00E-08
	220	6.54E-08	7.86E-08
	330	8.80E-08	9.57E-08
	470	1.17E-07	1.23E-07
	680	1.60E-07	1.65E-07
10 bits	47	3.19E-08	5.17E-08
	68	3.35E-08	5.28E-08
	100	3.66E-08	5.45E-08
	150	4.35E-08	5.83E-08
	220	5.43E-08	6.50E-08
	330	7.18E-08	7.89E-08
	470	9.46E-08	1.00E-07
	680	1.28E-07	1.33E-07
	1000	1.81E-07	1.83E-07
	1500	2.63E-07	2.63E-07
	2200	3.79E-07	3.76E-07
	3300	5.57E-07	5.52E-07

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Table 103. Minimum sampling time vs R_{AIN} (12-bit ADC)[1][2] (continued)

Resolution	RAIN (Ω)	Minimum sampling time (s)	
		Fast channels[3]	Slow channels[4]
8 bits	47	2.64E-08	4.17E-08
	68	2.76E-08	4.24E-08
	100	3.02E-08	4.39E-08
	150	3.51E-08	4.66E-08
	220	4.27E-08	5.13E-08
	330	5.52E-08	6.19E-08
	470	7.17E-08	7.72E-08
	680	9.68E-08	1.00E-07
	1000	1.34E-07	1.37E-07
	1500	1.93E-07	1.94E-07
	2200	2.76E-07	2.74E-07
	3300	4.06E-07	4.01E-07
	4700	5.73E-07	5.62E-07
	6800	8.21E-07	7.99E-07
	10000	1.20E-06	1.17E-06
	15000	1.79E-06	1.74E-06
6 bits	47	2.14E-08	3.16E-08
	68	2.23E-08	3.21E-08
	100	2.40E-08	3.31E-08
	150	2.68E-08	3.52E-08
	220	3.13E-08	3.87E-08
	330	3.89E-08	4.51E-08
	470	4.88E-08	5.39E-08
	680	6.38E-08	6.79E-08
	1000	8.70E-08	8.97E-08
	1500	1.23E-07	1.24E-07
	2200	1.73E-07	1.73E-07
	3300	2.53E-07	2.49E-07
	4700	3.53E-07	3.45E-07
	6800	5.04E-07	4.90E-07
	10000	7.34E-07	7.11E-07
	15000	1.09E-06	1.05E-06

1. Guaranteed by design.
2. Data valid up to 130 °C, with a 22 pF PCB capacitor and V_{DDA} = 1.6 V.

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3. Fast channels correspond to ADCx_INP0 to _INP5, and for ADCx_ INN0 to _INN5.
4. Slow channels correspond to all ADC inputs except for the Fast channels.

Table 104. ADC accuracy(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Fast and slow channels	Single ended	-	±3.5	±12	LSB
			Differential	-	±2.5	±7.5	
EO	Offset error	-	Single ended	-	±3	±5.5	
		-	Differential	-	±2	±3.5	
EG	Gain error	-	Single ended	-	±3.5	±11	
		-	Differential	-	±2.5	±7	
ED	Differential linearity error	-	Single ended		±0.75	+2/-1	
		-	Differential	-	±0.75	+2/-1	
EL	Integral linearity error	Fast and slow channels	Single ended	-	±2	±6.5	
			Differential	-	±1	±4	
ENOB	Effective number of bits	Single ended		-	10.8	-	bits
		Differential		-	11.5	-	
SINAD	Signal-to-noise and distortion ratio	Single ended		-	68	-	dB
		Differential		-	71	-	
SNR	Signal-to-noise ratio	Single ended		-	70	-	
		Differential		-	72	-	
THD	Total harmonic distortion	Single ended		-	-70	-	
		Differential		-	-80	-	

1. Data guaranteed by characterization for BGA packages. The values for LQFP packages might differ.
2. ADC DC accuracy values are measured after internal calibration in continuous mode.

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6.3.21 Voltage reference buffer characteristics

Table 105. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode, V_{DDA} = 3.3 V	VRS = 000	2.8	3.3	3.6	V
			VRS = 001	2.4	-	3.6	
			VRS = 010	2.1	-	3.6	
		Degraded mode(2)	VRS = 000	1.62	-	2.80	
			VRS = 001	1.62	-	2.40	
			VRS = 010	1.62	-	2.10	
V_{REFBUF_OUT}	Voltage reference buffer output, at 30 °C, I_{load}= 100 µA	Normal mode at 30 °C, I_{load} = 100 µA	VRS = 000	2.4980(3)	2.5000	2.5035(3)	
			VRS = 001	2.0460	2.0490	2.0520	
			VRS = 010	1.8010	1.8040	1.8060	
		Degraded mode(2)	VRS = 000	V_{DDA}- 150 mV	-	V_{DDA}	
			VRS = 001	V_{DDA}- 150 mV	-	V_{DDA}	
			VRS = 010	V_{DDA}- 150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
C_L	Load capacitor	-	-	0.5	1	1.50	µF
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω
I_{LOAD}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	-40 °C < T_J < +125 °C		-	-	T_{coeff} V_{REFINT} + 100	ppm/ °C
PSRR	Power supply rejection	DC		-	60	-	dB
		100 KHz		-	40	-	
t_{START}	Start-up time	C_L=0.5 µF		-	300	-	µs
		C_L=1 µF		-	500	-	
		C_L=1.5 µF		-	650	-	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(4)	-		-	8	-	mA

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Table 105. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA} (VREFBUF)	VREFBUF consumption from V_{DDA}	I_{LOAD} = 0 µA	-	15	25	µA
		I_{LOAD} = 500 µA	-	16	30	
		I_{LOAD} = 4 mA	-	32	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}- drop voltage).
3. Evaluated in characterization not tested in production.
4. To properly control VREFBUF IINRUSH current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VRS = 010, 001 and 000, respectively.

6.3.22 Analog temperature sensor characteristics

Table 106. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature (from V_{sensor} voltage)	-	-	3	°C
	V_{SENSE} linearity with temperature (from ADC counter)	-	-	3	
Avg_Slope(2)	Average slope (from V_{SENSE} voltage)	-	2	-	mV/°C
	Average slope (from ADC counter)	-	2	-	
V_{30}(3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run}	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

Table 107. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA}=3.3 V	0x08FF F814 - 0x08FF F815
TS_CAL2	Temperature sensor raw data acquired value at 130 °C, V_{DDA}=3.3 V	0x08FF F818 - 0x08FF F819

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6.3.23 Voltage booster for analog switch

Table 108. Voltage booster for analog switch characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.71	2.6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.71 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

1. Evaluated by characterization - Not tested in production.

6.3.24 Digital temperature sensor characteristics

Table 109. Digital temperature sensor characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}(2)	Output clock frequency	VDD_CORE = 1.19 V(3)	500	750	1150	kHz
T_{LC}(2)	Temperature linearity coefficient		1660	2100	2750	Hz/°C
T_{TOTAL_ERROR}(2)	Temperature offset measurement, all VOS	T_J = -40°C to 30°C	-13	-	4	°C
		T_J = 30°C to 130°C	-7	-	2	
T_{VDD_CORE}	Additional error due to supply variation	-	-1	-	1	°C
t_{TRIM}	Calibration time	-	-	-	2	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready bit is set	-	-	67	116.00	µs
I_{DDCORE_DTS}	DTS consumption on VDD_CORE	-	8.5	30	70.0	µA

1. Guaranteed by design, unless otherwise specified.
2. Evaluated by characterization - Not tested in production.
3. The characterization is done at VDD_CORE = 1.19 V for Typ/Min/Max.

6.3.25 V_{CORE} monitoring characteristics

Table 110. V_{CORE} monitoring characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ts_vcore	ADC sampling time when reading the VCORE voltage	-	1	-	-	µs

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6.3.26 Temperature and V_{BAT} monitoring

Table 111. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	4x26	-	kΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	-10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs
$V_{BAThigh}$	High supply monitoring	-	3.575	-	V
V_{BATlow}	Low supply monitoring	-	1.36	-	
$I_{VBATbuf}$(1)	Sensor buffer consuption	-	3.8	6.5	µA

1. Guaranteed by design.

Table 112. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	kΩ
		VBRS in PWR_CR3= 1		1.5	-	

Table 113. Temperature monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	-	126	-	°C
$TEMP_{low}$	Low temperature monitoring	-	-37	-	

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6.3.27 Audio digital filter (ADF)

Unless otherwise specified, the parameters given in for ADF are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Measurement points are done at CMOS levels: 0.5VDD
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- Voltage scale is set to VOS high

Refer to *Table 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics.

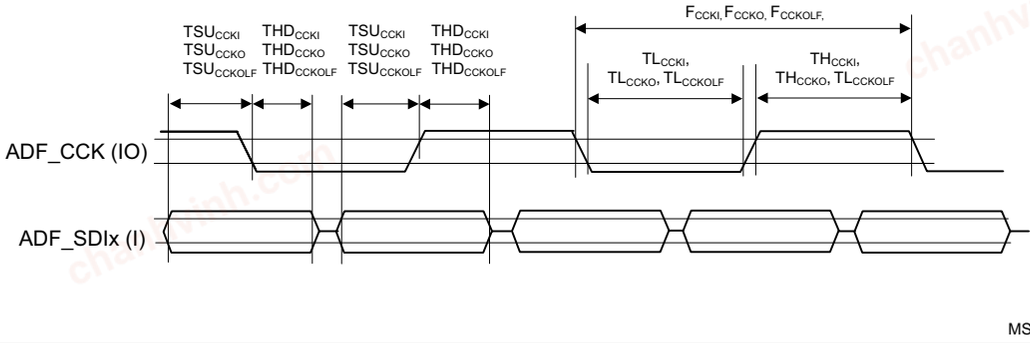
Table 114. ADF characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{CCKI}	Input clock frequency via the ADF_CCK[1:0] pin, in SLAVE_SPI mode	1.71<VDD<3.6 V	-	-	25	MHz
F_{CCKO}	Output clock frequency in MASTER_SPI	1.71<VDD<3.6 V	-	-	25	MHz
F_{CCKOLF}	Output clock frequency in LF_MASTER_SPI	1.71<VDD<3.6 V	-	-	5	MHz
F_{SYMB}	Input symbol rate in MANCHESTER mode	1.71<VDD<3.6 V	-	-	20	MHz
T_{HCCKI}, T_{LCCKI}	ADF_CCK[1:0] input clock high and low time	In SLAVE_SPI mode	2 x $T_{adf_proc_ck}$	-	-	ns
T_{HCCKO}, T_{LCCKO}	ADF_CCK[1:0] output clock high and low time	In MASTER_SPI mode	2 x $T_{adf_proc_ck}$	-	-	ns
$T_{HCCKOLF}$, $T_{LCCKOLF}$	ADF_CCK[1:0] output clock high and low time	In LF_MASTER_SPI mode	$T_{adf_proc_ck}$	-	-	ns
T_{SUCCKI}	Data setup time w.r.t. ADF_CCK[1:0] input	In SLAVE_SPI mode: ADF_CCK[1:0] configured in input, measured on rising and falling edge	2.5	-	-	ns
T_{HDCCKI}	Data hold time w.r.t. ADF_CCK[1:0] input		0.5	-	-	ns
T_{SUCCKO}	Data setup time w.r.t. ADF_CCK[1:0] output	In MASTER_SPI mode: ADF_CCK[1:0] configured in output, measured on rising and falling edge	3	-	-	ns
T_{HDCCKO}	Data hold time w.r.t. ADF_CCK[1:0] output		1	-	-	ns
$T_{SUCCKOLF}$	Data setup time w.r.t. ADF_CCK[1:0] output	In LF_MASTER_SPI mode: ADF_CCK[1:0] configured in output, measured on rising and falling edge	13	-	-	ns
$T_{HDCCKOLF}$	Data hold time w.r.t. ADF_CCK[1:0] output		0	-	-	ns

1. Guaranteed by characterization results.

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Figure 55. ADF timing diagram



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6.3.28 Digital camera interface (DCMIPP) characteristics

Unless otherwise specified, the parameters given in **Table xx** for DCMIPP are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in **Table 24** *General operating conditions*,, with the following configuration:

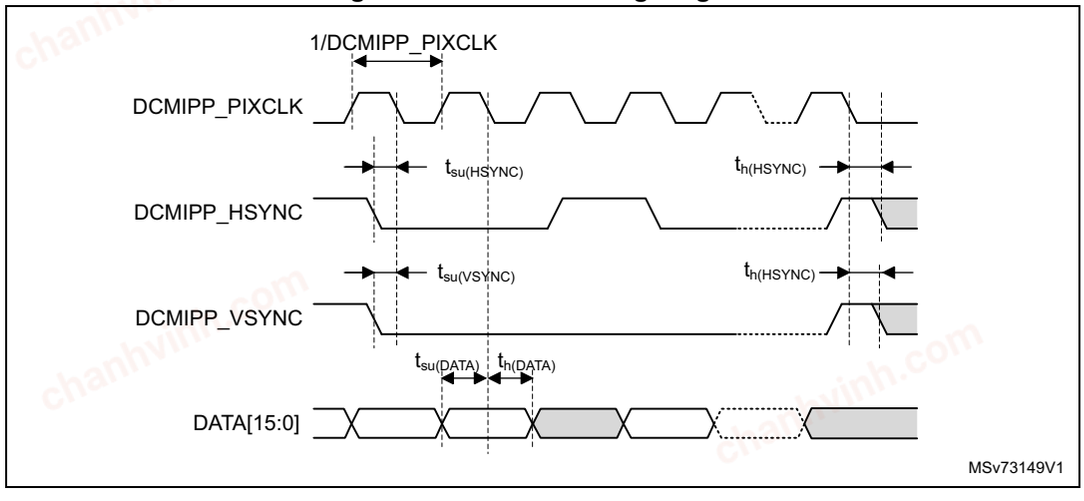
- DCMIPP_PIXCLK polarity: falling
- DCMIPP_VSYNC and DCMIPP_HSYNC polarity: high
- Data formats: 16 bits
- Capacitive load C=30pF
- Measurement points are done at CMOS levels: 0.5VDD
- Voltage scale is set to VOS high

Table 115. DCMIPP characteristics(1)

Symbol	Parameter	Min	Max(2)	Unit
DCMIPP_PIXCLK	Pixel Clock input	-	120	MHz
D_{pixel}	Pixel Clock input duty cycle	30	70	%
$t_{su(}$DATA)	Data input setup time	3	-	ns
t_h(DATA)	Data hold time	1	-	
tsu(HSYNC), tsu(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input setup time	2.5	-	
th(HSYNC), th(VSYNC)	DCMI_HSYNC/ DCMI_VSYNC input hold time	1	-	

1. Evaluated By characterization – Not tested in production.
2. At VOS low, these values are degraded by up to 7%.

Figure 56. DCMIPP timing diagram



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6.3.29 Parallel synchronous slave interface (PSSI) characteristics

Unless otherwise specified, the parameters given in *Table 116* and *Table 117* for PSSI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 26: General operating conditions* with the following configuration:

- PSSI_PDCK polarity: falling
- PSSI_RDY and PSSI_DE polarity: low
- Bus width: 16 lines
- Data width: 32 bits
- Capacitive load CL = 30 pF
- Measurement points done at CMOS levels: 0.5*VDD
- I/O compensation cell activated
- HSLV activated when VDD ≤ 2.7 V
- Voltage scale is set to VOS high

Table 116. PSSI transmit characteristics(1)

Symbol	Parameter	Conditions	Min	Max(2)	Unit
-	Frequency ratio PSSI_PDCK/f_{HCLK}	-	-	0.4	-
PSSI_PDCK	PSSI Clock input	1.71 V<V_{DD}<3.6 V	-	80(3)	MHz
D_{pixel}	PSSI Clock input duty cycle	-	30	70	%
t_{ov}(DATA)	Data output valid time	1.71 V<V_{DD}<3.6 V	-	12.5	ns
t_{oh}(DATA)	Data output hold time		5.5	-	
$t_{ov(}$(DE)	DE output valid time		-	12	
t_{oh}(DE)	DE output hold time		5.5	-	
tsu(RDY)	RDY input setup time		0	-	
th(RDY)	RDY input hold time		5.5	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.
3. This maximum frequency does not consider receiver setup and hold timings.

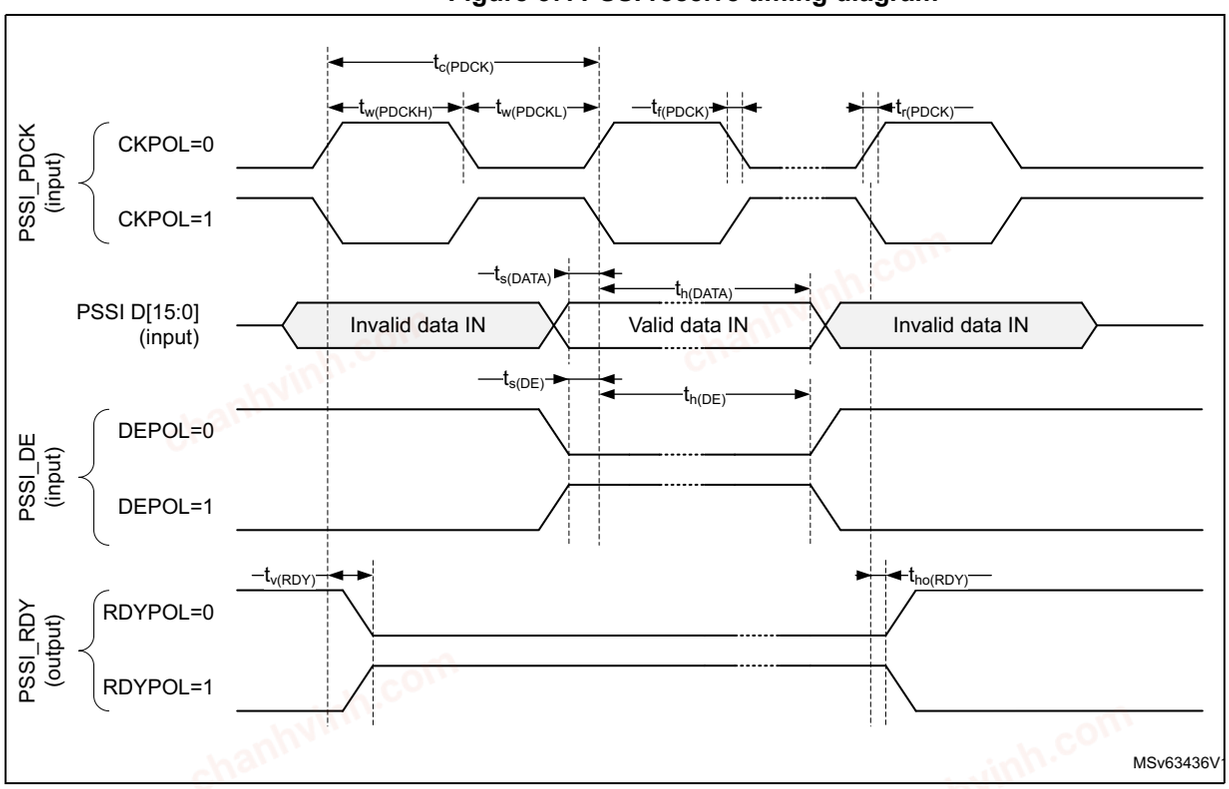
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Table 117. PSSI receive characteristics(1)

Symbol	Parameter	Conditions	Min	Max(2)	Unit
-	Frequency ratio PSSI_PDCK/f_{HCLK}	-	-	0.4	-
PSSI_PDCK	PSSI Clock input	1.71 V<V_{DD}<3.6 V	-	100	MHz
D_{pixel}	PSSI Clock input duty cycle	-	30	70	%
t_{su}(DATA)	Data input setup time	1.71 V<V_{DD}<3.6 V	1	-	ns
t_h(DATA)	Data input hold time		1.5	-	
$t_{su(}$(DE)	DE input setup time		1	-	
t_h(DE)	DE input hold time		1.5	-	
tov(RDY)	RDY output valid time		-	11.5	
toh(RDY)	RDY output hold time		5.5	-	

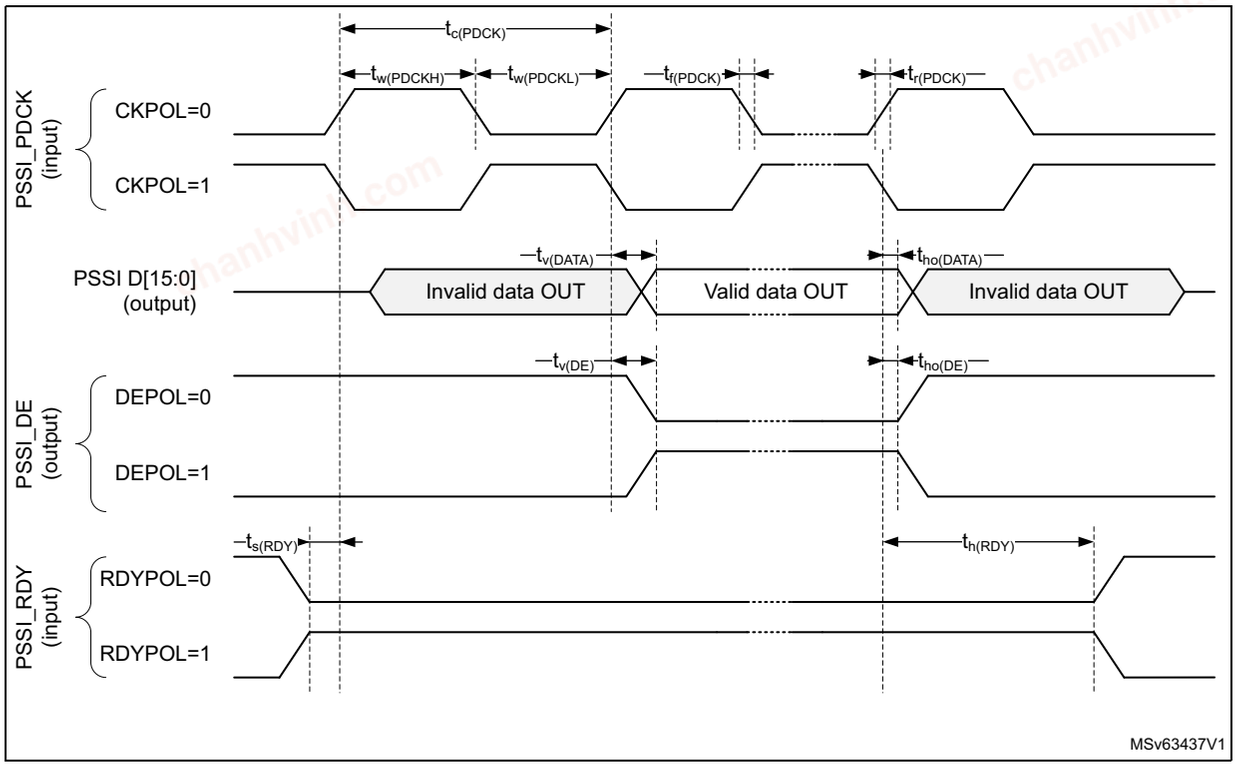
1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

Figure 57. PSSI receive timing diagram



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Figure 58. PSSI transmit timing diagram



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6.3.30 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 118* for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 26: General operating conditions*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: 0.5VDD
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS high

Table 118. LTDC characteristics(1)

Symbol	Parameter		Min	Max(2)	Unit
f_{CLK}	LTDC clock output frequency	1.71<V_{DD}<3.6 V, 30 pF	-	90	MHz
D_{CLK}	LTDC clock output duty cycle		45	55	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time		$t_{w(CLK)}$//2-0.5	$t_{w(CLK)}$/2+0.5	ns
$t_{v(DATA)}$	Data output valid time		-	3.5	
$t_{h(DATA)}$	Data output hold time		0.5	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time		-	3.0	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC/VSYNC/DE output hold time		0.5	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

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Figure 59. LCD-TFT horizontal timing diagram

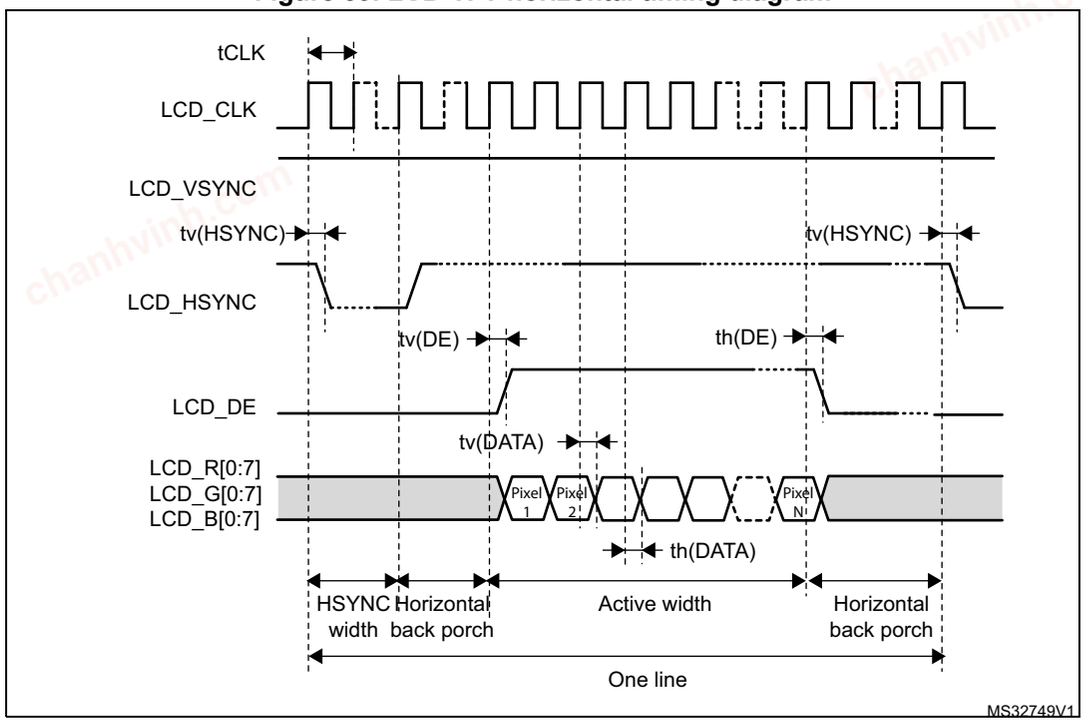
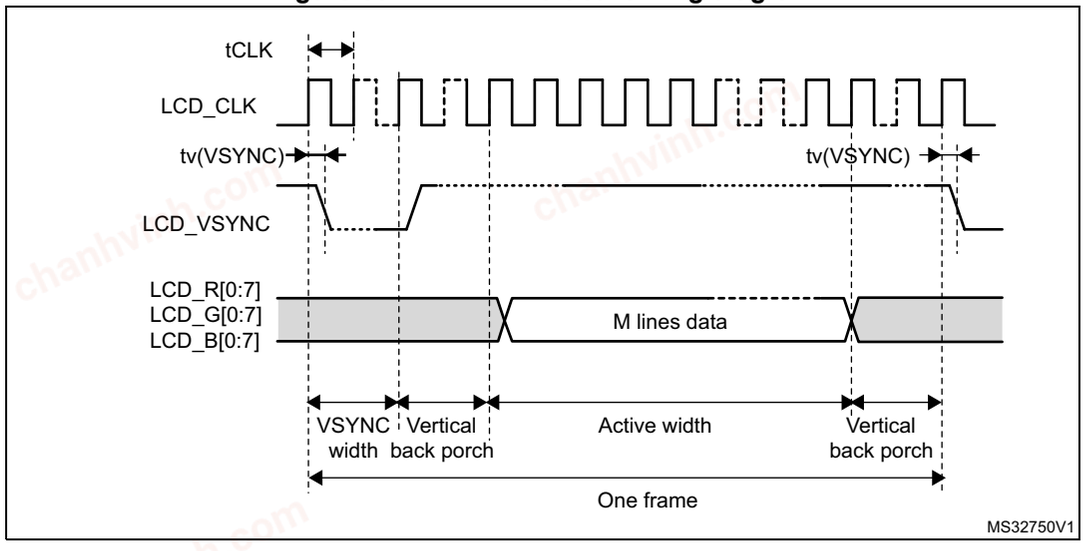


Figure 60. LCD-TFT vertical timing diagram



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6.3.31 Timer characteristics

The parameters given in *Table 119* are guaranteed by design.

Refer to *Section 6.3.15: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 119. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 300 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 150 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 240 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 300 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4x F_{rcc_pclkx1} or TIMxCLK = 4x F_{rcc_pclkx2}.

6.3.32 Low-power timer characteristics

The parameters given in *Table 120* are guaranteed by design.

Refer to *Section 6.3.15: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 120. LPTIMx characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	150	MHz
f_{EXT}	Timer external clock frequency on Input1 and Input2	0	$f_{LPTIMxCLK}/2$	
Res_{TIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{TIMxCLK}$

1. LPTIMx is used as a general term to refer to the LPTIM1 to LPTIM5 timers.
2. Guaranteed by design.

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6.3.33 Communication interfaces

I3C interface characteristics

The I3C interface meets the timings requirements of the MIPI® I3C specification v1.1.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

The parameters given in *Table 121* are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS high

The timings are in line with the MIPI specification, except for those given in *Table 121* and *Table 122*. For t_{SU_OD} and t_{SU_PP} this can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register. For further details refer to AN5879.

Table 121. I3C open-drain measured timing(1)

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SU_OD}	SDA data setup time during open drain mode	Controller 1.71 V < V_{DD} < 3.6 V	3	-	16	ns

1. Guaranteed by characterization results.

Table 122. I3C push-pull measured timing(1)

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SU_PP}	SDA signal data setup in push-pull mode	Controller 1.71 V < V_{DD} < 3.6 V	3	-	14.5	ns

1. Guaranteed by characterization results.

I2C interface characteristics

The I2C interface meets the timings requirements of the I2C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The parameters given in *Table 123* are obtained with the following configuration:

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- Output speed is set to OSPEEDRy[1:0] = 00

The I^2C timing requirements are specified by design, and not tested in production, when the I2C peripheral is properly configured (refer to the product reference manual):

The SDA and SCL I/O requirements are met with the following restrictions: The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.15: I/O port characteristics* for the I2C I/O characteristics:

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 123. I^2C analog filter characteristics(1)(2)

Symbol	Parameter	Min	Max(3)	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by analog filter	50(4)	165(5)	ns

1. Guaranteed by characterization results.
2. Measurement points are done at 50% V_{DD}.
3. At VOS low, the performance can be degraded by up to 7% compared to VOS high.
4. Spikes with widths below $t_{AF(min)}$ are filtered.
5. Spikes with widths above $t_{AF(max)}$ are not filtered.

USART interface characteristics

Unless otherwise specified, the parameters given in *Table 124* for USART are derived from tests performed under the ambient temperature, f_{PCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS high

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

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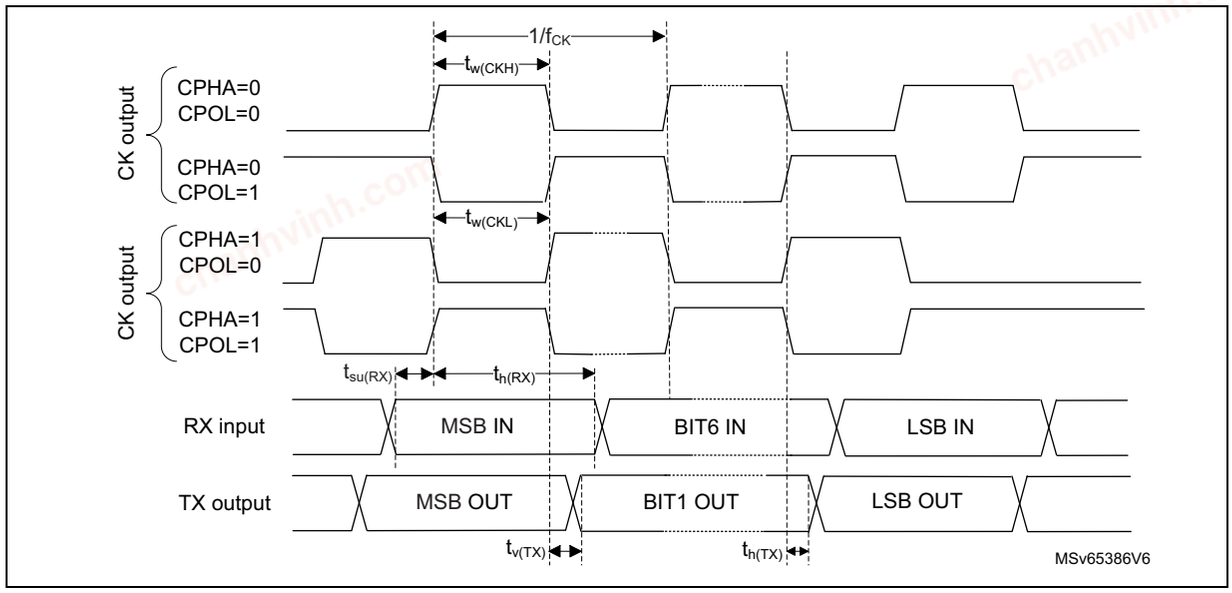
Table 124. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
f_{CK}	USART clock frequency	Master mode, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	15.5	MHz
		Slave receiver mode, 1.71 V ≤ V_{DD} ≤ 3.6 V			41.5	
		Slave transmitter mode, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	40.0	
		Slave transmitter mode, 2.7 V ≤ V_{DD} ≤ 3.6 V			41.5	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker}+2	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	0.5	-	-	
$t_{w(CKH)}$, $t_{w(CKL)}$	CK high and low time	Master mode	$1/f_{CK}/2-1$	$1/f_{CK}/2$	$1/f_{CK}/2+1$	
$t_{su(RX)}$	Data input setup time	Master mode	11.5	-	-	
		Slave mode	1.5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	
		Slave mode	0.5	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode, , 2.7 V ≤ V_{DD} ≤ 3.6 V	-	8.0	10.5	
		Slave mode, , 1.71 V ≤ V_{DD} ≤ 3.6 V	-	8.0	12.5	
		Master mode	-	1	2	
$t_{h(TX)}$	Data output hold time	Slave mode	6	-	-	
		Master mode	0.5	-	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

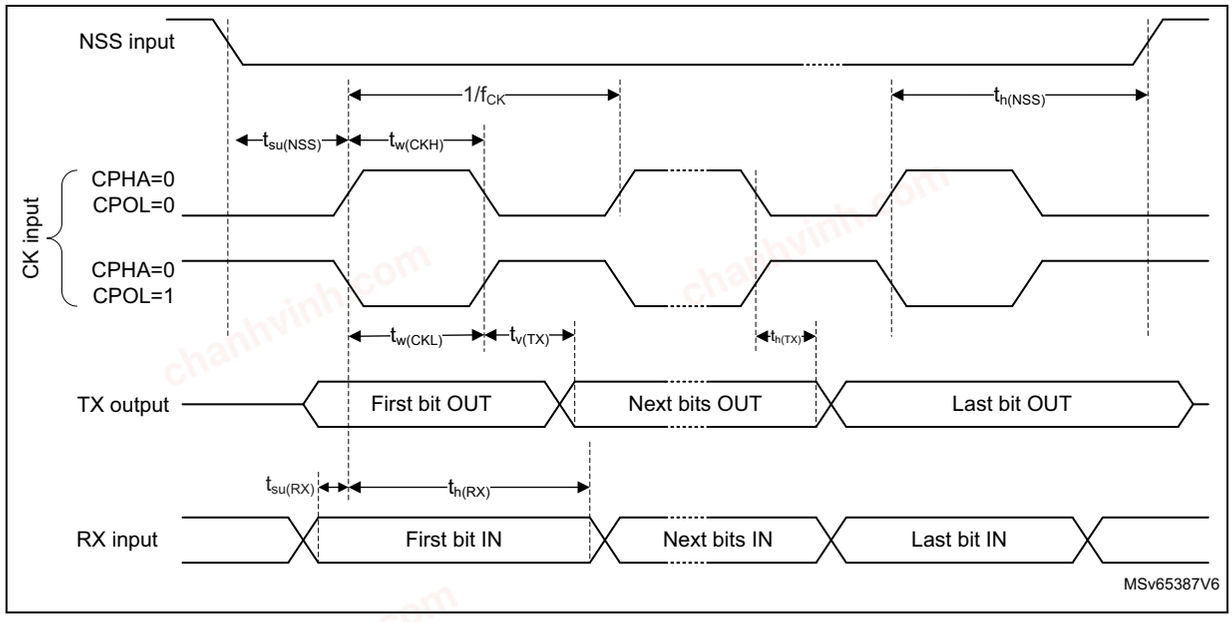
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Figure 61. USART timing diagram in master mode



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 62. USART timing diagram in slave mode



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SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 125* for SPI are derived from tests performed under the ambient temperature, f_{PCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS high

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (SS, SCK, MOSI, MISO for SPI).

Table 125. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
f_{SCK}	SPI clock frequency	Master mode, 1.71 V < V_{DD} < 3.6 V	-	-	90	MHz
		Master mode, 2.7 V < V_{DD} < 3.6 V, SPI2, 3, 4, 5, 6			133	
		Master mode, 2.7 V < V_{DD} < 3.6 V, SPI1			130	
		Slave receiver mode, 2.7 V < V_{DD} < 3.6 V, SPI2, 3, 4, 5, 6			140	
		Slave receiver mode, 1.71 V < V_{DD} < 3.6 V, SPI1			130	
		Slave mode transmitter/full duplex, 2.7 V < V_{DD} < 3.6 V			45	
		Slave mode transmitter/full duplex, 1.71 V < V_{DD} < 3.6 V			38	
$t_{su(NSS)}$	NSS setup time	Slave mode	2.5	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode, prescaler = 2	t_{SCK}-1	t_{SCK}	t_{SCK}+1	

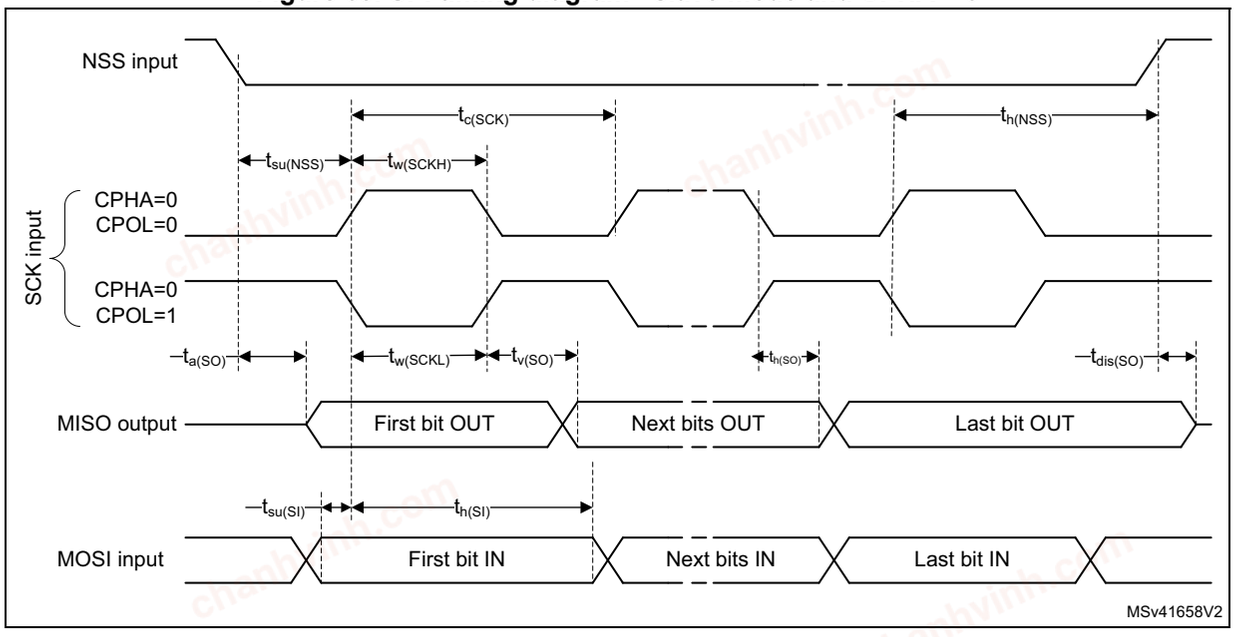
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Table 125. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
$t_{su(MI)}$	Data input setup time	Master mode	1.5	-	-	ns
$t_{su(SI)}$		Slave mode	2	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	1.5	-	-	
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	11.5	15.5	
$t_{dis(SO)}$	Data output disable time	Slave mode	7.5	8	12	
$t_{v(SO)}$	Data output valid time	Slave mode, 2.7 V < V_{DD} < 3.6 V	-	9	11	
		Slave mode, 1.71 V < V_{DD} < 3.6 V	-	9	13	
$t_{v(MO)}$		Master mode, 1.71 V < V_{DD} < 3.6 V	-	0.5	1	
$t_{h(SO)}$	Data output hold time	Slave mode	6.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. At VOS low, these values are degraded by up to 7%.

Figure 63. SPI timing diagram - slave mode and CPHA = 0



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Figure 64. SPI timing diagram - slave mode and CPHA = 1

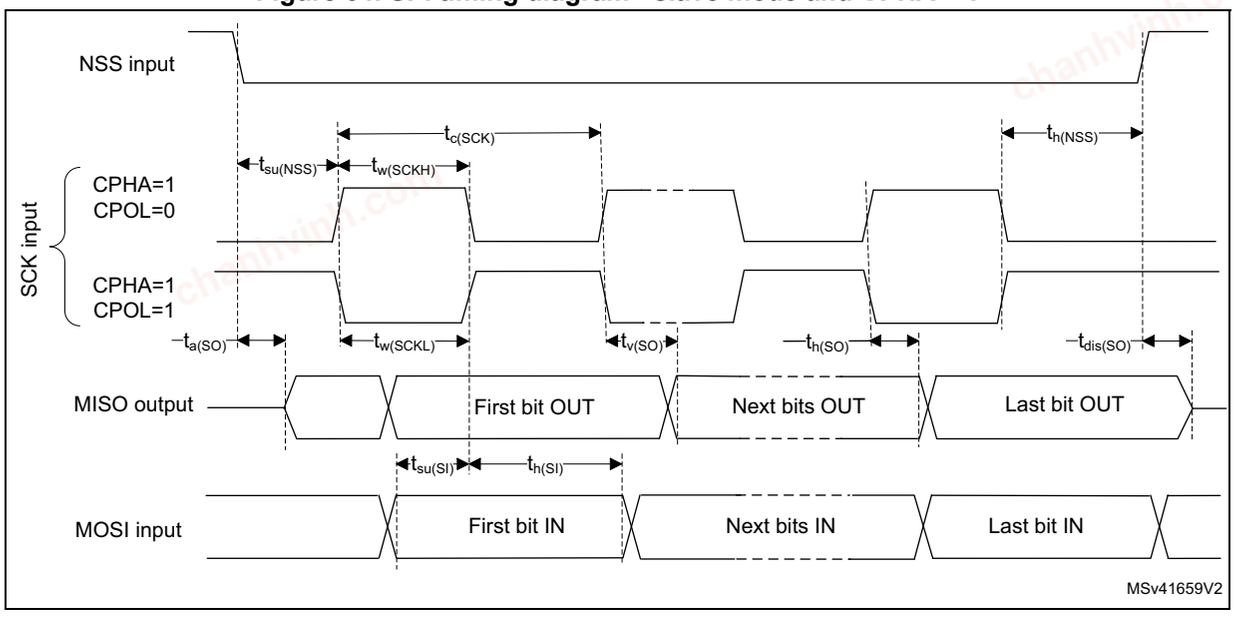
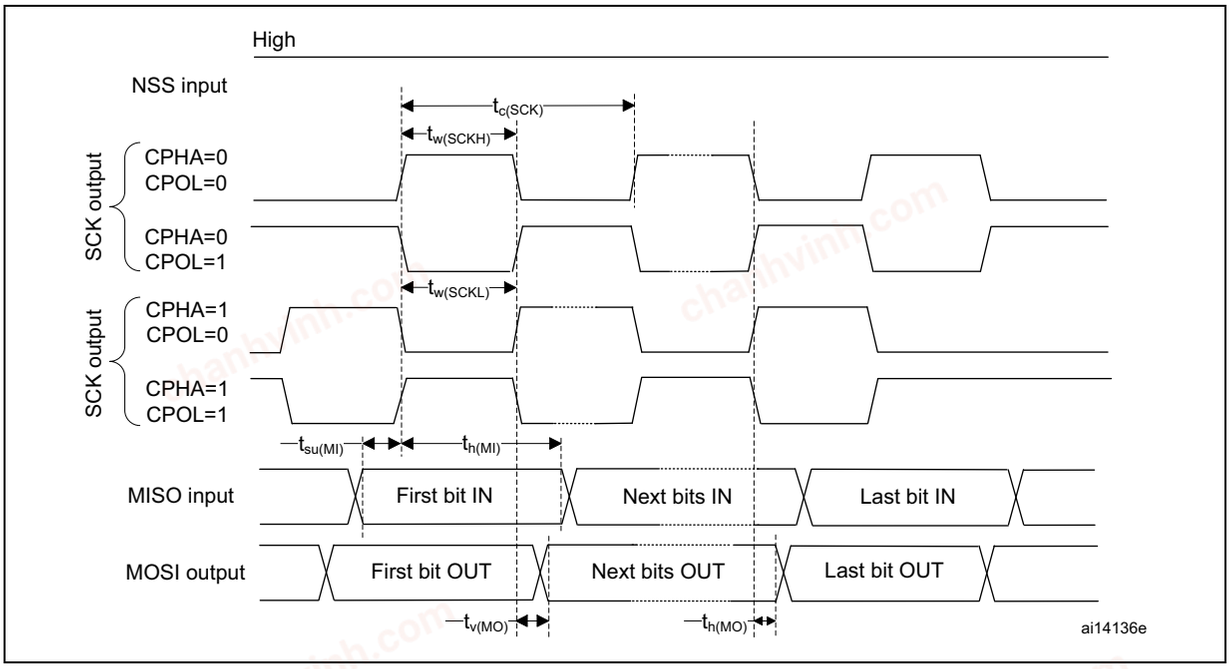


Figure 65. SPI timing diagram - master mode



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I²S Interface characteristics

Unless otherwise specified, the parameters given in *Table 126* for I²S are derived from tests performed under the ambient temperature, f_{PCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS high

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,WS).

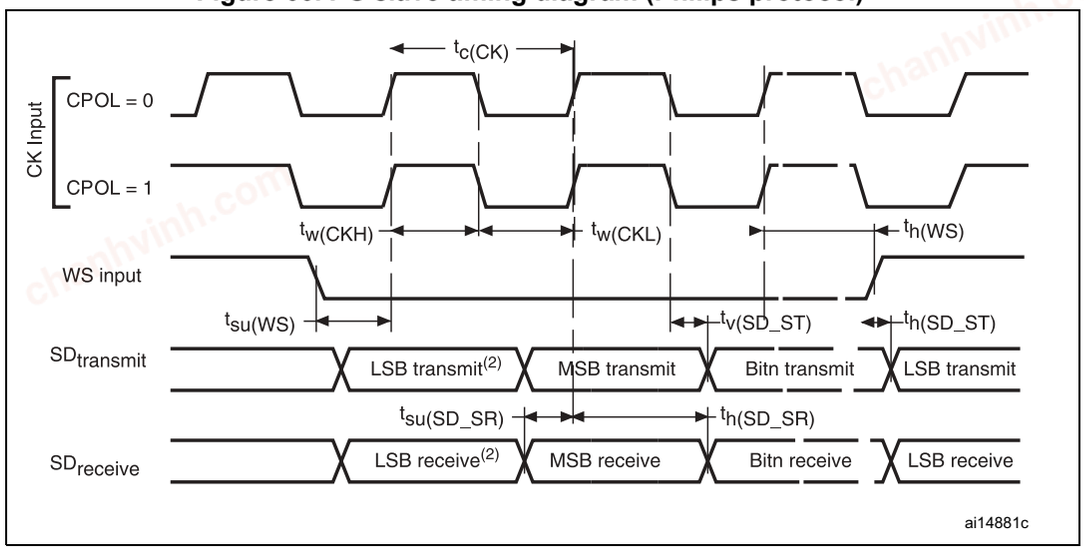
Table 126. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max(2)	Unit
f_{MCK}	I²S main clock output	-	-	50	MHz
		Master transmitter	-	50	
		Master receiver	-	28	
		Slave transmitter	-	23	
		Slave receiver	-	50	
$t_{v(WS)}$	WS valid time	Master mode	-	1.5	ns
$t_{h(WS)}$	WS hold time		0.5	-	
$t_{su(WS)}$	WS setup time	Slave mode	3	-	
$t_{h(WS)}$	WS hold time		1	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	1.5	-	
$t_{su(SD_SR)}$		Slave receiver	1.5	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	2	-	
$t_{h(SD_SR)}$		Slave receiver	1	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	13	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	2	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7.5	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0.5	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

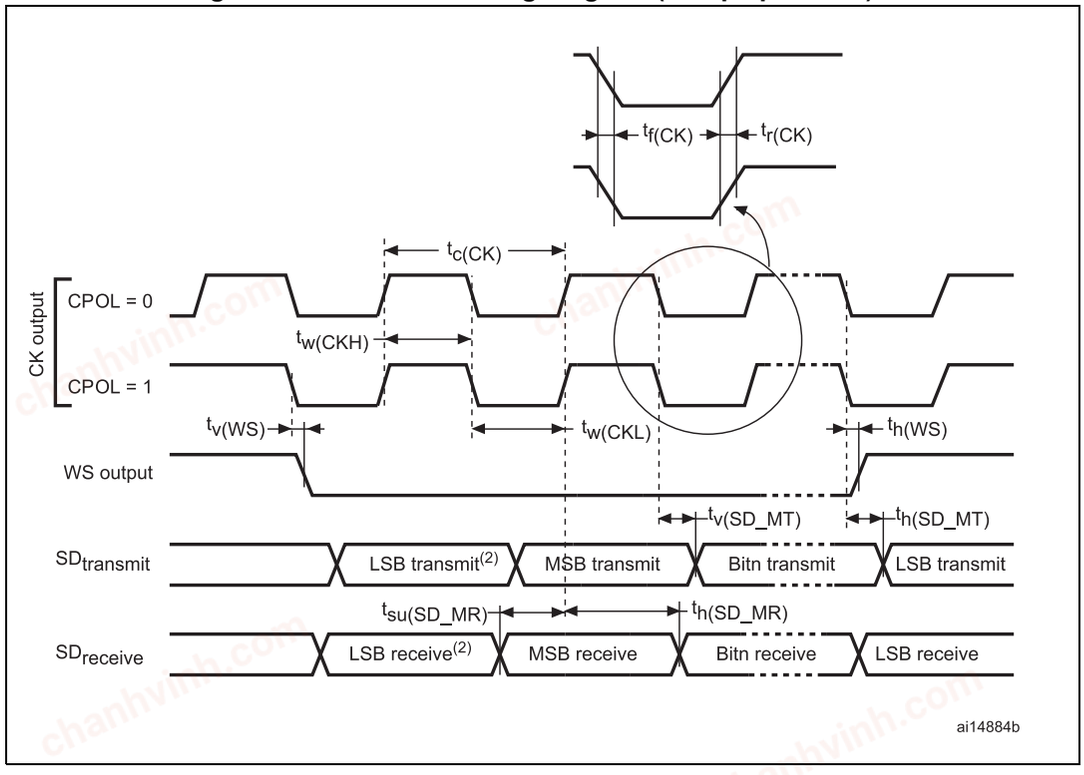
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Figure 66. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 67. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

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SAI characteristics

Unless otherwise specified, the parameters given in *Table 127* for SAI are derived from tests performed under the ambient temperature, f_{PCLK} frequency and VDD supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- IO Compensation cell activated.
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS high

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 127. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max (2)	Unit
f_{MCK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(3)	Master transmitter	-	34	
		Master receiver	-	38	
		Slave transmitter	-	35	
		Slave receiver	-	50	
$t_{v(FS)}$	F_S valid time	Master mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	ns
		Master mode, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	13	
$t_{su(FS)}$	F_S setup time	Slave mode	3	-	
$t_{h(FS)}$	F_S hold time	Master mode	7	-	
		Slave mode	1	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD_B_SR)}$		Slave receiver	1.5	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	2	-	
$t_{h(SD_B_SR)}$		Slave receiver	1	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	14	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7.5	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	14.5	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	7	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.
3. APB clock frequency must be at least twice SAI clock frequency.

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Figure 68. SAI master timing waveforms

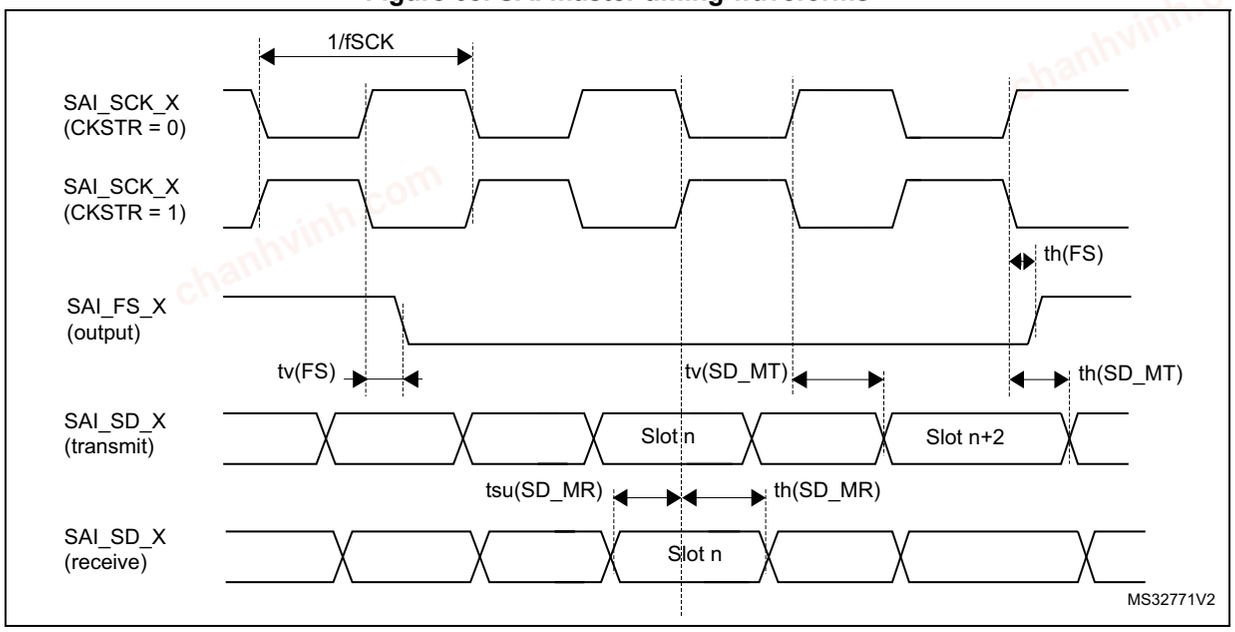
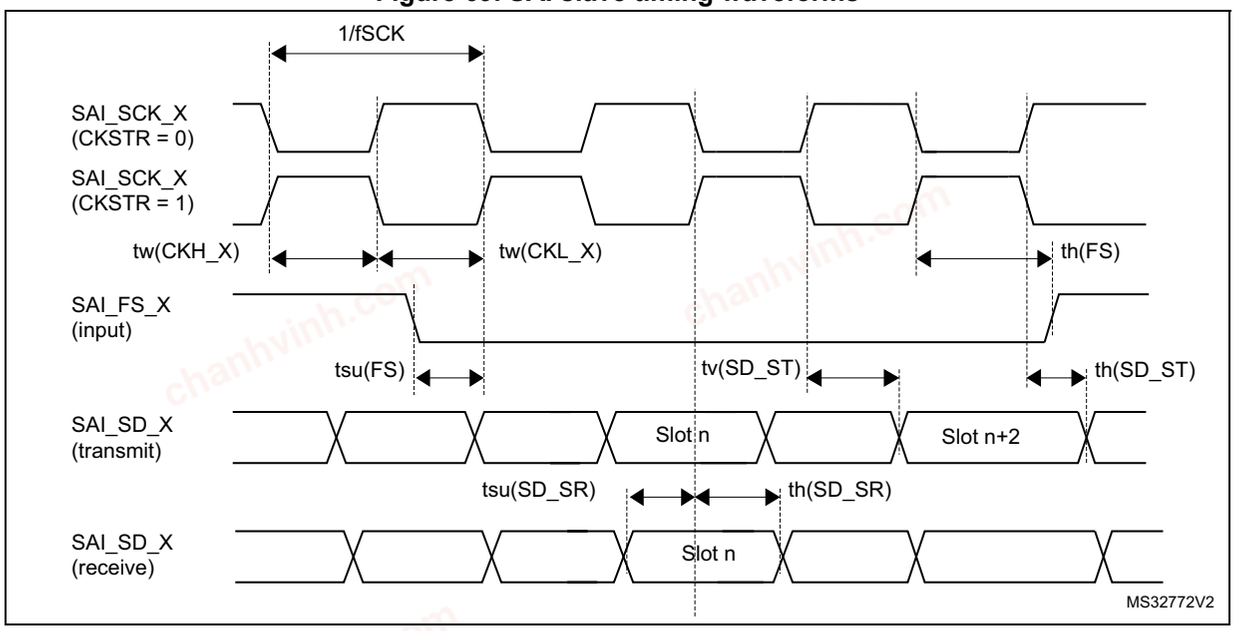


Figure 69. SAI slave timing waveforms



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MDIO characteristics

Unless otherwise specified, the parameters given in *Table 128* for the MDIO are derived from tests performed under the ambient temperature, f_{PCLK} frequency and VDD supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

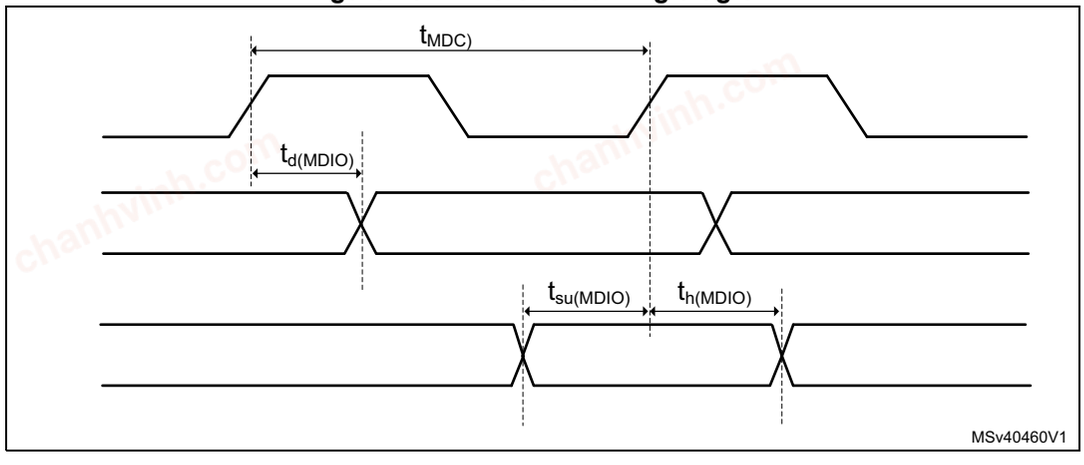
- Output speed is set to OSPEEDRy[1:0] = 10
- I/O Compensation cell activated.
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS high

Table 128. MDIO slave timing parameters(1)

Symbol	Parameter	Min	Typ	Max(2)	Unit
F_{MDC}	Management Data Clock	-	-	30	MHz
$t_{d(MDIO)}$	Management Data Iput/output output valid time	6	8.5	13	ns
$t_{su(MDIO)}$	Management Data Iput/output setup time	2.5	-	-	
$t_{h(MDIO)}$	Management Data Iput/output hold time	0.5	-	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.

Figure 70. MDIO slave timing diagram



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SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 129* and *Table 130* for SDIO are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS high

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 129. Dynamic characteristics: SD / MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	120(3)	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} =52MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(4)/DDR(4) mode						
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IH}	Input hold time HS	-	1.5	-	-	
t_{IDW}(4)	Input valid window (variable window)	-	3.5	-	-	
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(5)/DDR(5) mode						
t_{OV}	Output valid time HS	-	-	6	6.5	ns
t_{OH}	Output hold time HS	-	4	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	2.5		-	ns
t_{IHD}	Input hold time SD	-	1.5		-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	1	1.5	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. Guaranteed by characterization results.
2. At VOS Low, these values are degraded by up to 7%.
3. With capacitive load CL = 20 pF.
4. For SD 1.8 V support, an external voltage converter is needed.
5. Minimum window of time where the data needs to be stable for proper sampling in tuning mode.

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Table 130. Dynamic characteristics: eMMC characteristics VDD = 1.71V to 1.9V(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
f_{PP}	Clock frequency in data transfer mode	-	-	-	130(3)	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} =52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	-	2	-	-	ns
t_{IH}	Input hold time HS	-	1.5	-	-	
t_{IDW}(4)	Input valid window (variable window)	-	3	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OVD}	Output valid time HS	-	-	6	6.5	ns
t_{OHD}	Output hold time HS	-	4	-	-	

1. Guaranteed by characterization results.
2. At VOS low, these values are degraded by up to 7%.
3. C_L = 20 pF.
4. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Figure 71. SD high-speed mode

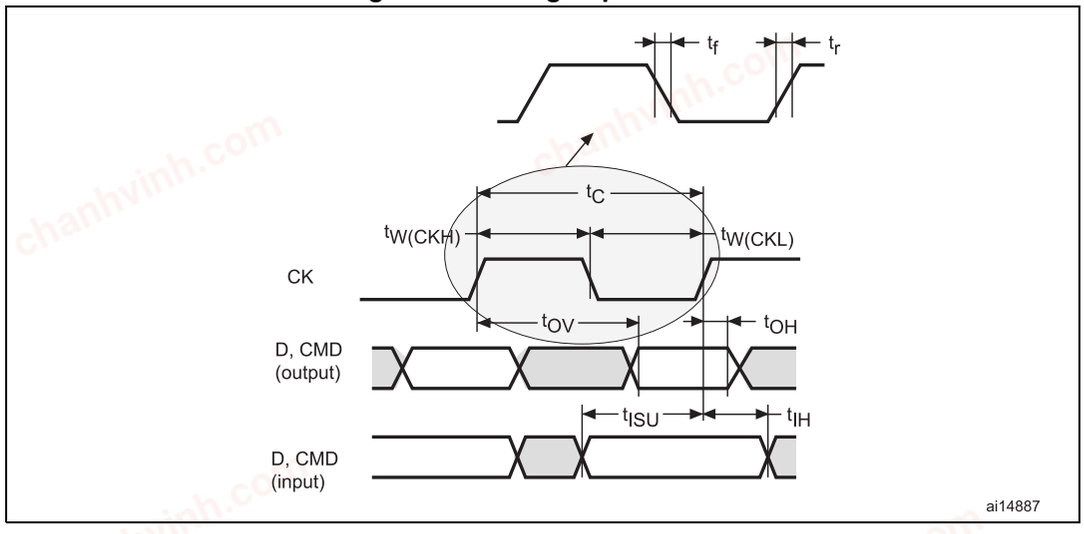
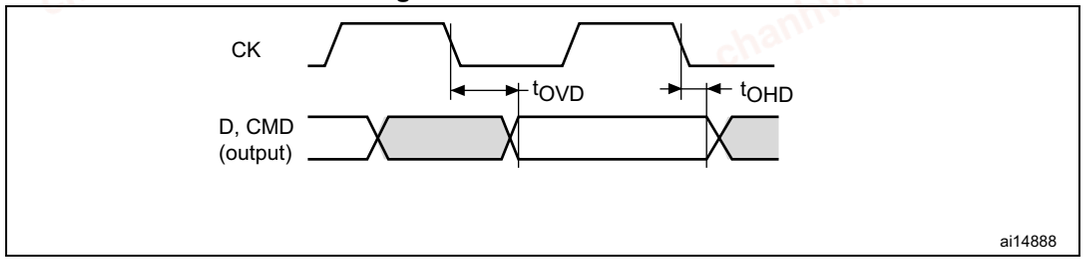
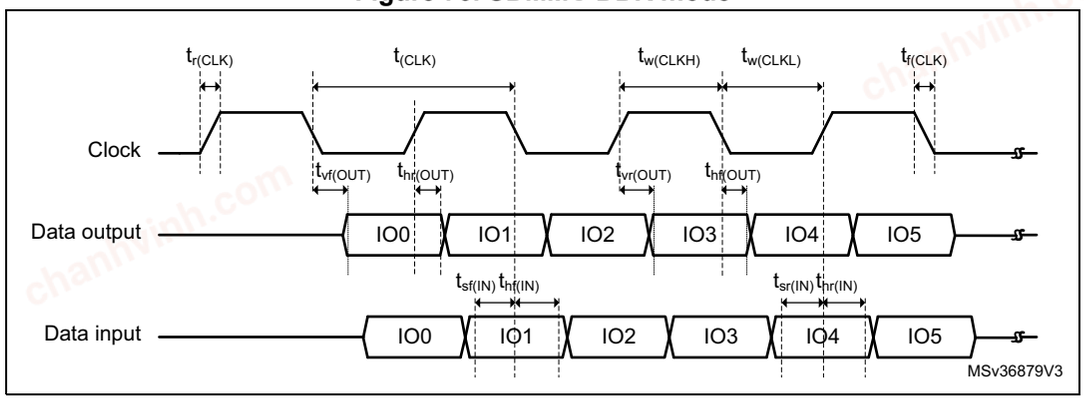


Figure 72. SD default mode



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Figure 73. SDMMC DDR mode



USB OTG_FS characteristics

Table 131. USB OTG_FS electrical characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD33USB}$	USB transceiver operating voltage	-	3.0(1)	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}	Output driver impedance(2)	Driver high and low	28	36	44	

1. The USB functionality is ensured down to 2.7 V. However, not all USB electrical characteristics are degraded in the 2.7 to 3.0 V voltage range.
2. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

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USB OTG_HS characteristics

The OTG_HS controller complies with the following specifications:

- USB On-The-Go supplement, revision 2.0
- Universal Serial Bus revision 2.0 specification
- Battery charging specification, revision 1.2

The parameters given in *Table 132* and *Table 133* are derived from tests performed under temperature and VDD supply voltage conditions summarized in *Table 26: General operating conditions*.

Table 132. USB OTG_HS DC electrical characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage	-	3.12(2)	-	3.6	V
f_{HCLK}	f_{HCLK} value to guarantee proper operation of the OTG_HS interface	-	30(3)	-	-	MHz
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1575	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1425(3)	2250	3090(3)	
R_{PD}	Embedded USB_DP and USB_DM pull-down value	-	14250	-	24800	
Z_{DRV}	Output driver impedance(4)	Driving high or low	40.5(3)	45	49.5(3)	
t_{lr}	Rise time	CL < 5 pF	0.5(3)	-	-	ns
t_{lf}	Fall time	CL < 5 pF	0.5(3)	-	-	
t_{lrfm}	Rise/fall time matching	-	80(3)	-	125(3)	%

1. Evaluated by characterization. Not tested in production, unless otherwise specified.
2. The USB functionality is ensured down to 3 V but not the full USB electrical characteristics which are degraded in 3.0 to 3.12 V voltage range.
3. Specified by design. Not tested in production.
4. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-). The matching impedance is already included in the embedded driver.

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Table 133. OTG_HS current consumption characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{DD(OTG_HS)}$	USB (PLL and PHY) current consumption on V_{DDUSB}	Full Speed Transmit(2)	-	5.65	6.02	mA
		High Speed Idle(2)	-	5.66	6	
		High Speed Transmit(2)	-	14.6	14.92	
$I_{DD11(OTG_HS)}$	USB (PLL and PHY) current consumption on $V_{DD11USB}$	Full Speed Transmit(2)	-	6.00	10.59	mA
		High Speed Idle(2)	-	5.93	10.51	
		High Speed Transmit(2)	-	6.87	11.98	

1. Evaluated by characterization. Not tested in production.
2. Suspend when operating in Device mode with no far-side host termination on DP/DM during measurements.

UCPD characteristics

The UCPD controller complies with USB Type-C Rev 1.2 and USB Power Delivery Rev 3.0 specifications.

Table 134. UCPD electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	UCPD operating supply voltage	-	3.0	3.3	3.6	V

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Ethernet interface characteristics

Unless otherwise specified, the parameters given in *Table 135*, *Table 136* and *Table 137* for SMI, RMII and MII are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS high

Due to timing constraint Pxy_C I/Os cannot be used as ethernet signals.

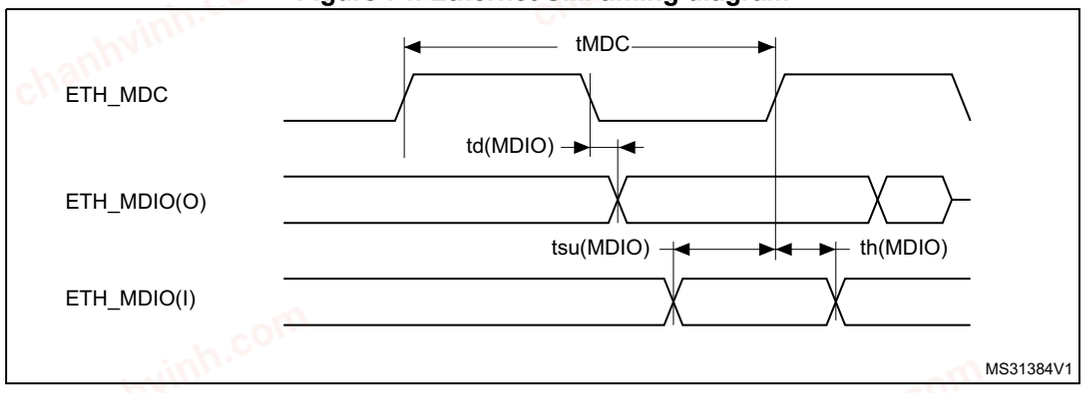
Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics:

Table 135. Dynamic characteristics: Ethernet MAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max(2)	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	400	400	400	ns
$T_{d(MDIO)}$	Write data valid time	0	1	1.5	
$t_{su(MDIO)}$	Read data setup time	12.5	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.
2. At VOS low, these values are degraded by up to 7%.

Figure 74. Ethernet SMI timing diagram



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Table 136. Dynamic characteristics: Ethernet MAC signals for RMII (1)

Symbol	Parameter	Min	Typ	Max(2)	Unit
$t_{su(RXD)}$	Receive data setup time	2.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1	-	-	
$t_{su(CRS)}$	Carrier sense setup time	1.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	7	9.5	14	
$t_{d(TXD)}$	Transmit data valid delay time	7	10.5	14.5	

1. Guaranteed by characterization results.
2. At VOS low, these values are degraded by up to 7%.

Figure 75. Ethernet RMII timing diagram

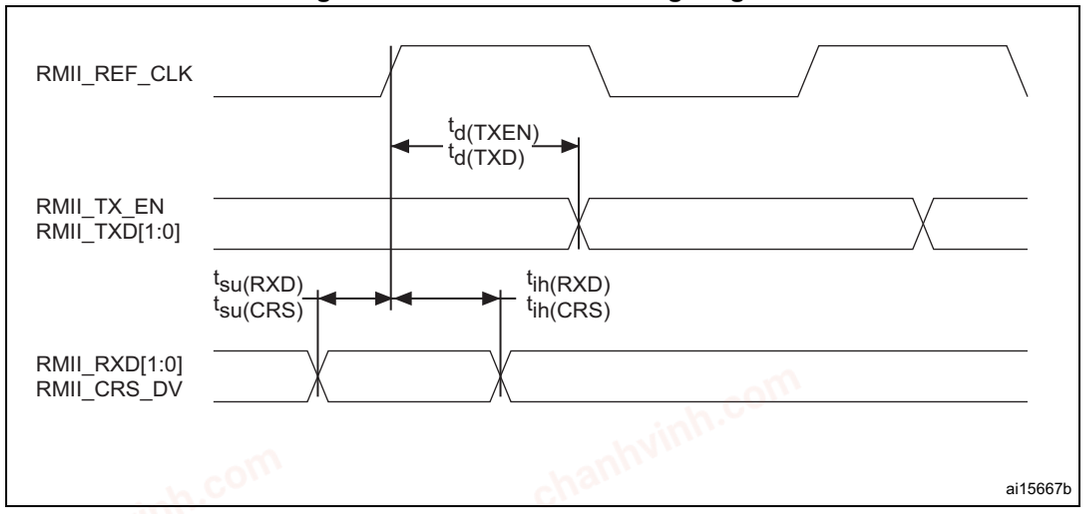


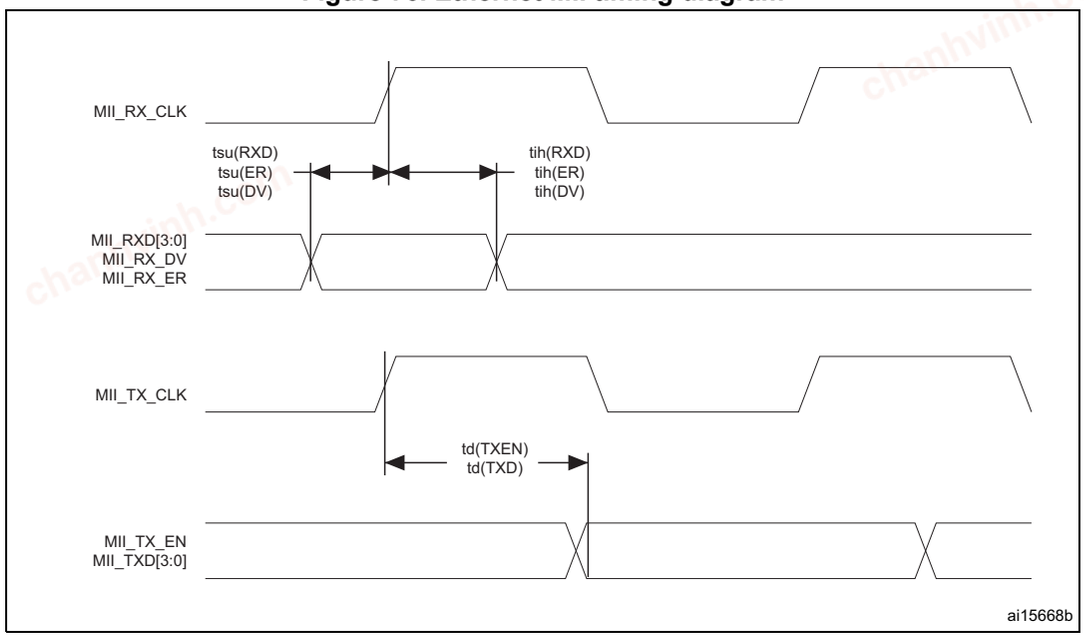
Table 137. Dynamic characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max(2)	Unit
$t_{su(RXD)}$	Receive data setup time	2.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1	-	-	
$t_{su(DV)}$	Data valid setup time	1	-	-	
$t_{ih(DV)}$	Data valid hold time	0.5	-	-	
$t_{su(ER)}$	Error setup time	2	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	6.5	9	13	
$t_{d(TXD)}$	Transmit data valid delay time	6.5	10	14.5	

1. Guaranteed by characterization results.
2. At VOS low, these values are degraded by up to 7%.

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Figure 76. Ethernet MII timing diagram



JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 138* and *Table 139* for JTAG/SWD are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 26: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS high

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics:

Table 138. Dynamic JTAG characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
F_{TCK}	T_{CK} clock frequency	2.7 V ≤ V_{DD}≤ 3.6 V	-	-	50	MHz
		1.71 ≤ V_{DD} ≤ 3.6 V	-	-	40	
$ti_{su(TMS)}$	TMS input setup time	-	3	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	2	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	1	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7 V <V_{DD}< 3.6 V	-	9	10	
		1.71 <V_{DD}< 3.6 V	-	10	12.5	
$t_{oh(TDO)}$	TDO output hold time	-	8	-	-	

1. Guaranteed by characterization results.
2. At VOS low, these values are degraded by up to 7%.

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Table 139. Dynamics SWD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
F_{SWCLK}	SWCLK clock frequency	2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	90	MHz
		1.71 ≤ V_{DD} ≤ 3.6 V	-	-	60	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	1	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time	-	2.5	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	2.7 V ≤ V_{DD} ≤ 3.6 V	-	9	11	
		1.71 ≤ V_{DD} ≤ 3.6 V	-	11	16.5	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8	-	-	

1. Guaranteed by characterization results.
2. At VOS low, these values are degraded by up to 7%.

Figure 77. JTAG timing diagram

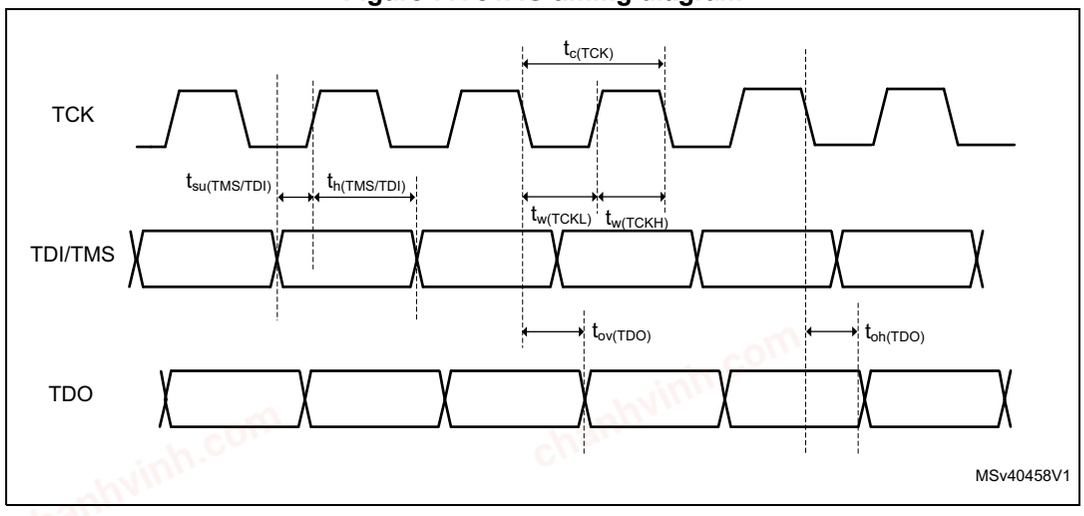
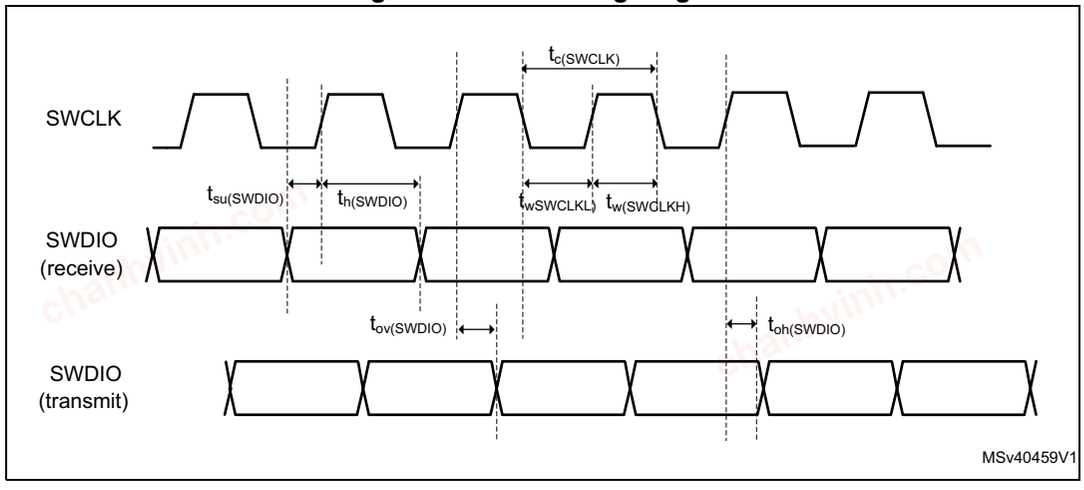


Figure 78. SWD timing diagram



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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at *www.st.com.* ECOPACK is an ST trademark.

7.1 Device marking

Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

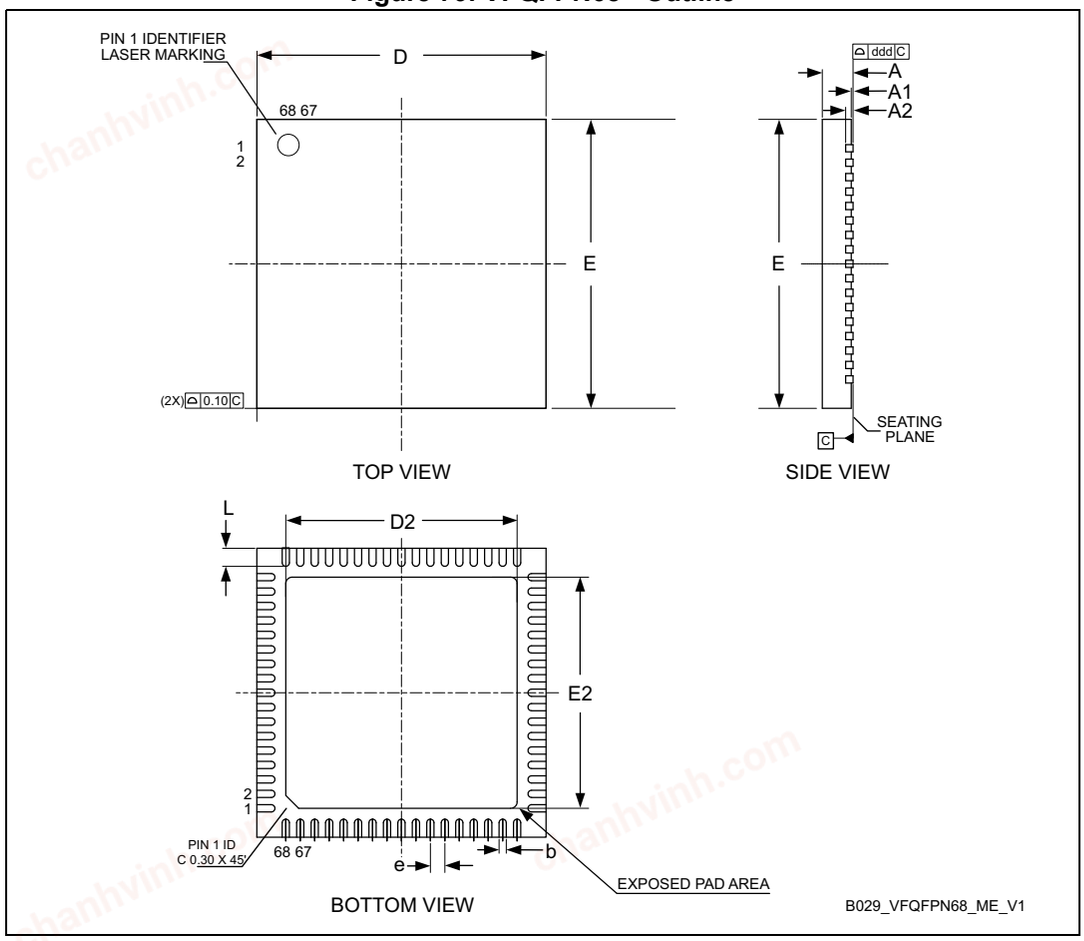
A WLCSP simplified marking example is provided in the corresponding package information subsection.

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7.2 VFQFPN68 package information (B029)

This VFQFPN is a 68 pins, 8 x 8 mm, 0.4 mm pitch, very thin fine pitch quad flat package

Figure 79. VFQFPN68 - Outline



1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Packages No lead. Sawed version. Very thin profile: 0.80 < A ≤ 1.00mm.
2. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

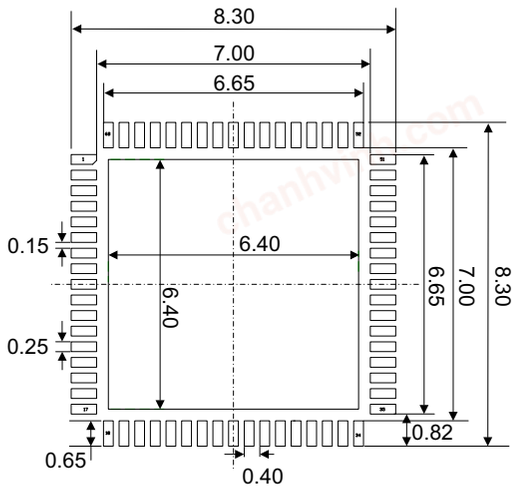
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Table 140. VFQFPN68 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05	0	0.0008	0.0020
A3	-	0.20	-	-	0.0008	-
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
D	7.85	8.00	8.15	0.3091	0.3150	0.3209
D2	6.30	6.40	6.50	0.2480	0.2520	0.2559
E	7.85	8.00	8.15	0.3091	0.3150	0.3209
E2	6.30	6.40	6.50	0.2480	0.2520	0.2559
e	-	0.40	-	-	0.0157	-
L	0.40	0.50	0.60	0.0157	0.0197	0.0236
ddd	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 80. VFQFPN68 - Recommended footprint



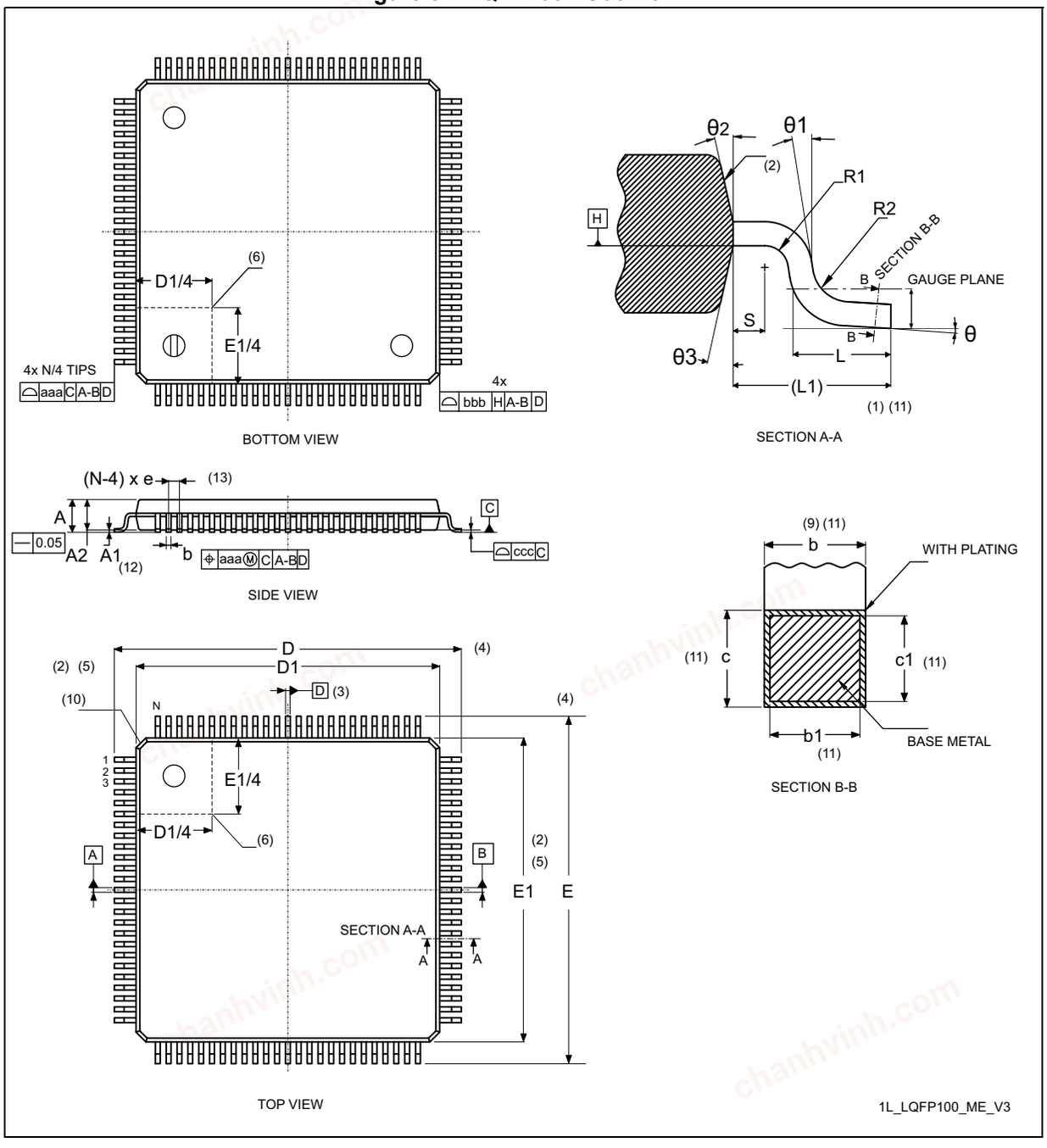
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7.3 LQFP100 package information (1L)

This LQFP is 100 lead, 14 x 14 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 81. LQFP100 - Outline(15)



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Table 141. LQFP100 - Mechanical data

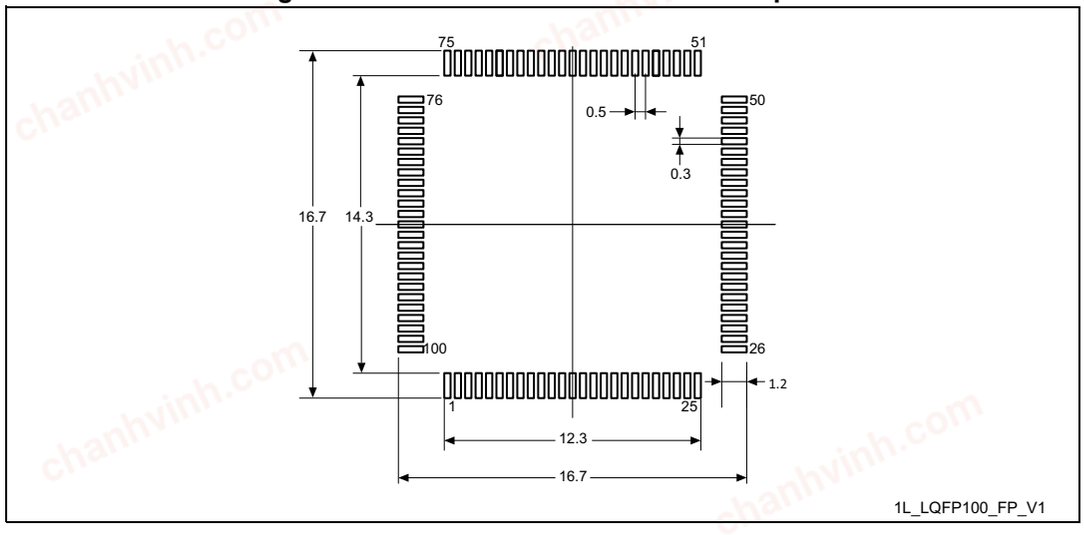
Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1[12]	0.05	-	0.15	0.0019	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	16.00 BSC			0.6299 BSC		
D1[2][5]	14.00 BSC			0.5512 BSC		
E[4]	16.00 BSC			0.6299 BSC		
E1[2][5]	14.00 BSC			0.5512 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.177	0.0236	0.0295
L1[1][11]	1.00			-	0.0394	-
N[13]	100					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 82. LQFP100 - Recommended footprint



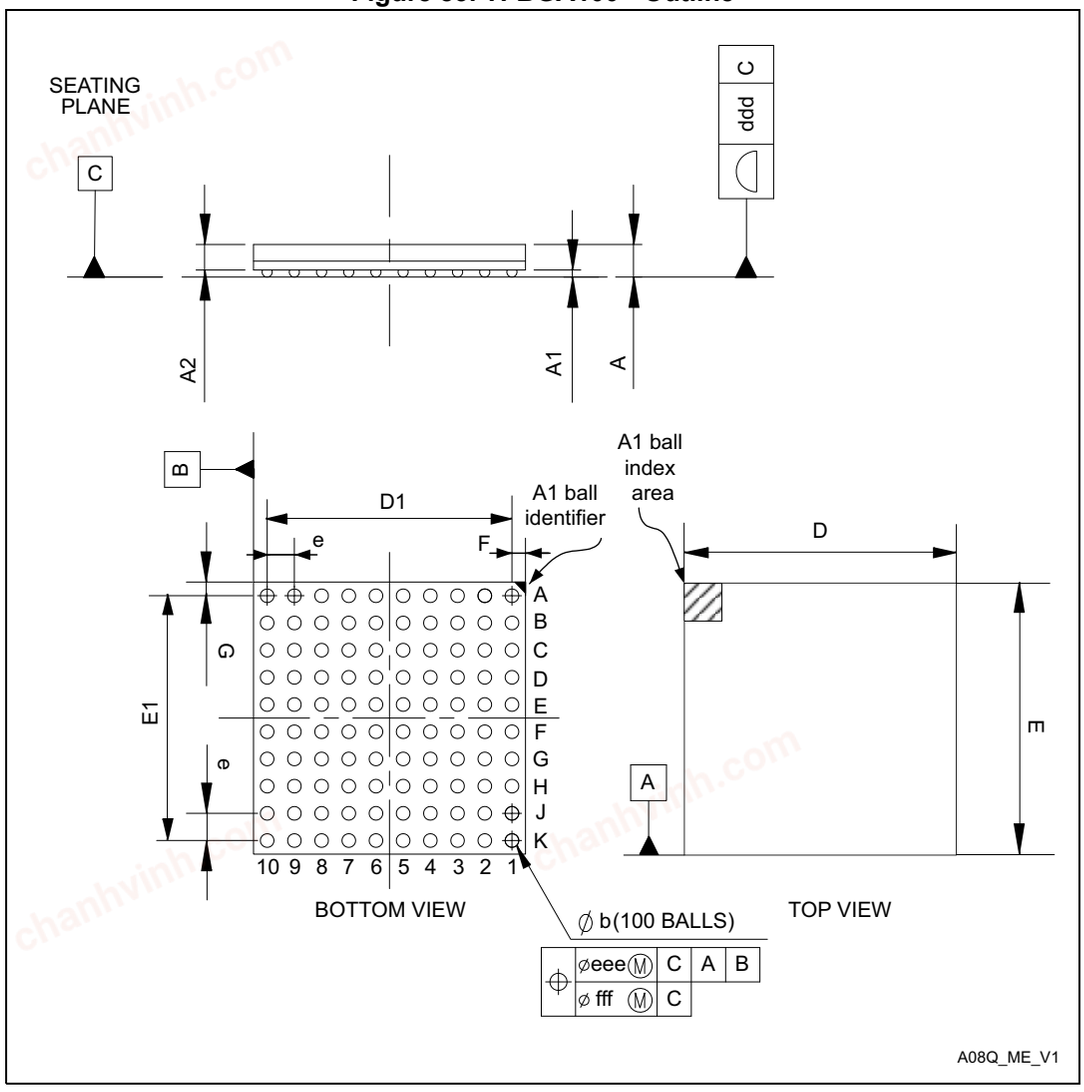
1. Dimensions are expressed in millimeters.

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7.4 TFBGA100 package information (A08Q)

This TFBGA is 100 - ball, 8X8 mm, 0.8 mm pitch fine pitch ball grid array package.

Figure 83. TFBGA100 - Outline



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Table 142. TFBGA100 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.100	-	-	0.0433
A1[3]	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b[4]	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	7.850	8.000	8.150	0.3091	0.3150	0.3209
D1	-	7.200		-	0.2835	-
E	7.850	8.000	8.150	0.3091	0.3150	0.3209
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	0.400	-	-	0.0157	-
G	-	0.400	-	-	0.0157	-
ddd	-	-	0.100	-	-	0.0039
eee[5]	-	-	0.150	-	-	0.0059
fff[6]	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The total profile height (Dim A) is measured from the seating plane to the top of the component
3. • The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
   • A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optiona
4. Initial ball equal 0.350mm.
5. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
6. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

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Figure 84. TFBGA100 - Recommended footprint

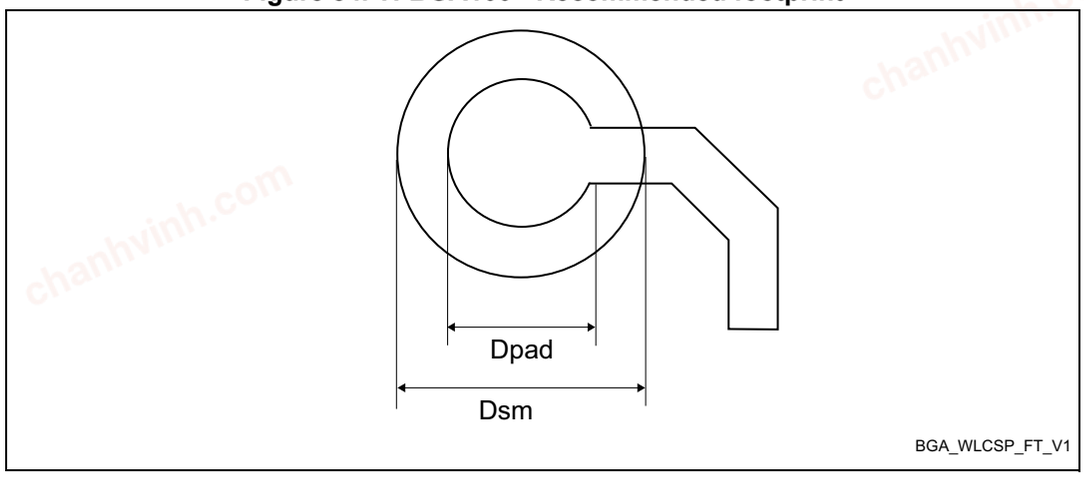


Table 143. TFBGA100 - Recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

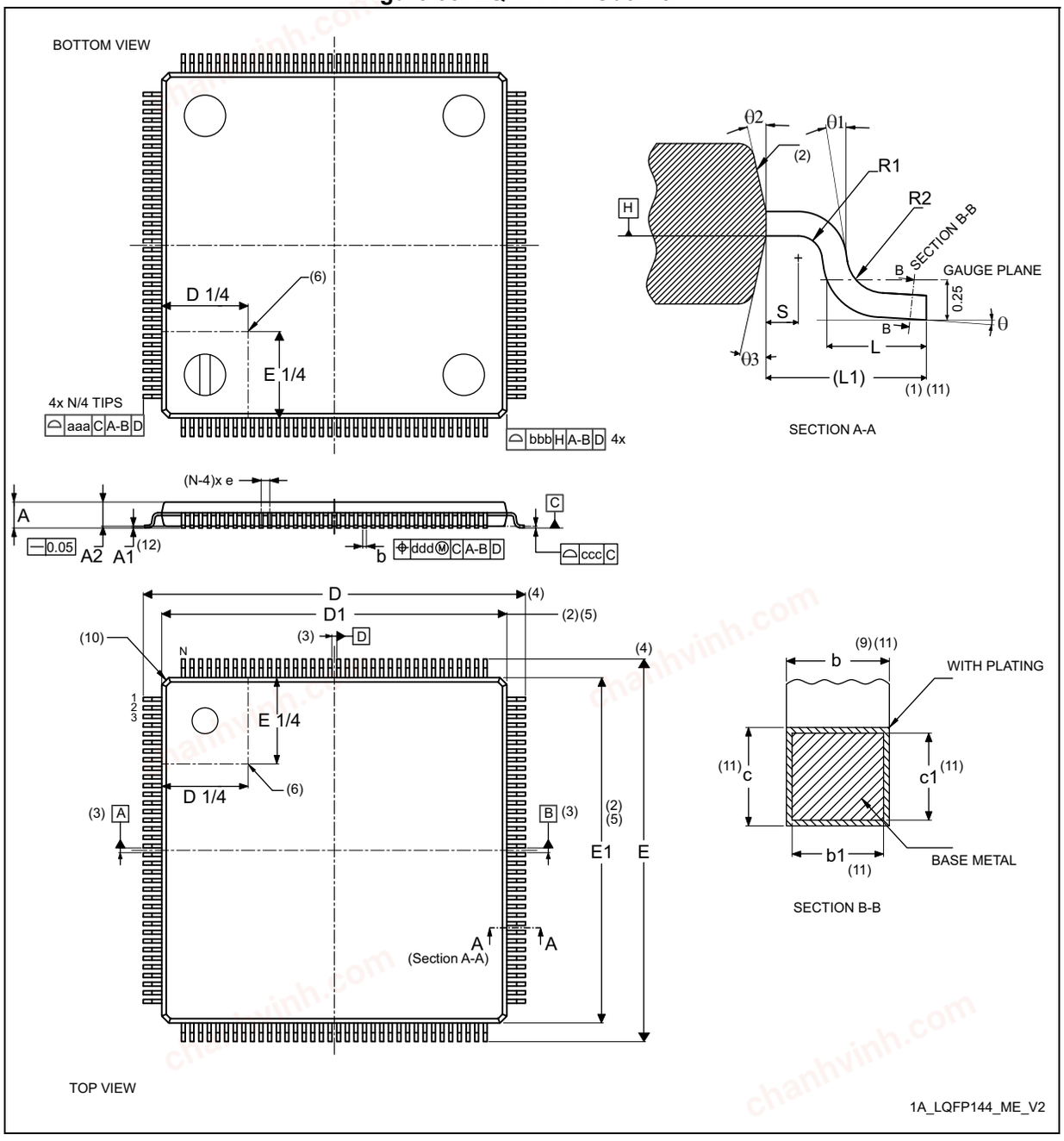
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7.5 LQFP144 package information (1A)

This LQFP is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 85. LQFP144 - Outline(15)



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Table 144. LQFP144 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	22.00 BSC			0.8661 BSC		
D1[2][5]	20.00 BSC			0.7874 BSC		
E[4]	22.00 BSC			0.8661 BSC		
E1[2][5]	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	144					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

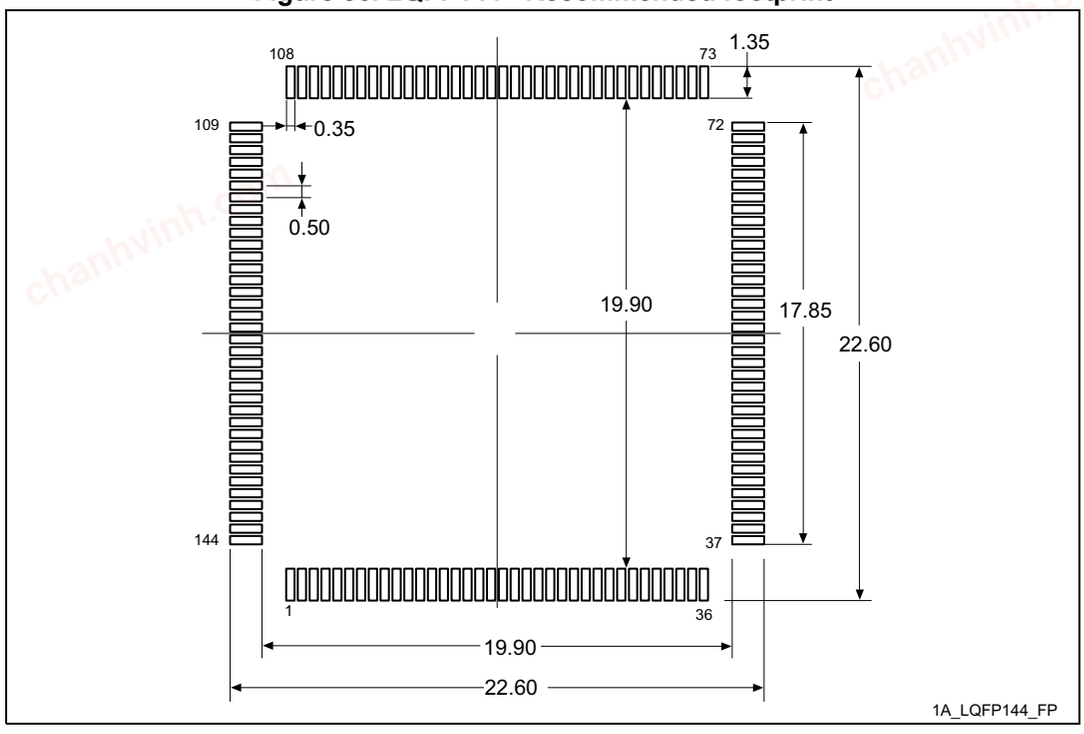
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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

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Figure 86. LQFP144 - Recommended footprint



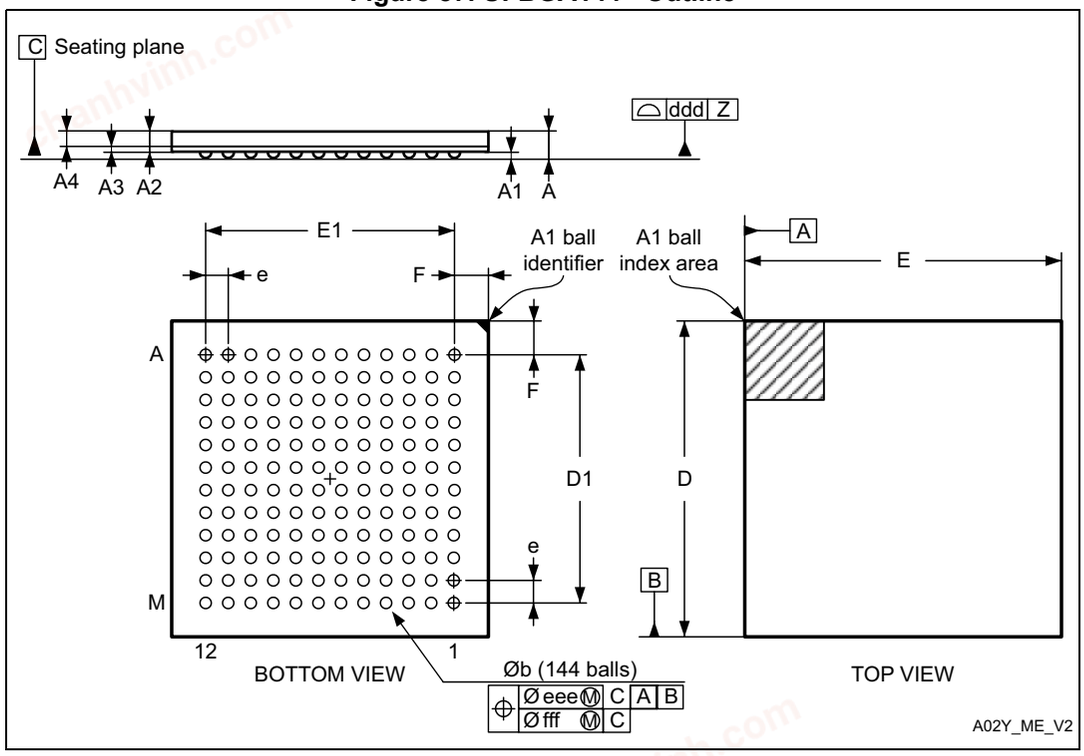
1. Dimensions are expressed in millimeters.

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7.6 UFBGA144 package information (A02Y)

This UFBGA is a 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package.

Figure 87. UFBGA144 - Outline



1. Drawing is not to scale.

Table 145. UFBGA144 - Mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.360	0.400	0.440	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.2736	0.2756	0.2776
D1	8.750	8.800	8.850	0.2343	0.2362	0.2382
E	9.950	10.000	10.050	0.2736	0.2756	0.2776
E1	8.750	8.800	8.850	0.2343	0.2362	0.2382
e	0.750	0.800	0.850	-	0.0197	-

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Table 145. UFBGA144 - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.550	0.600	0.650	0.0177	0.0197	0.0217
ddd	-	-	0.080	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 88. UFBGA144 - Recommended footprint

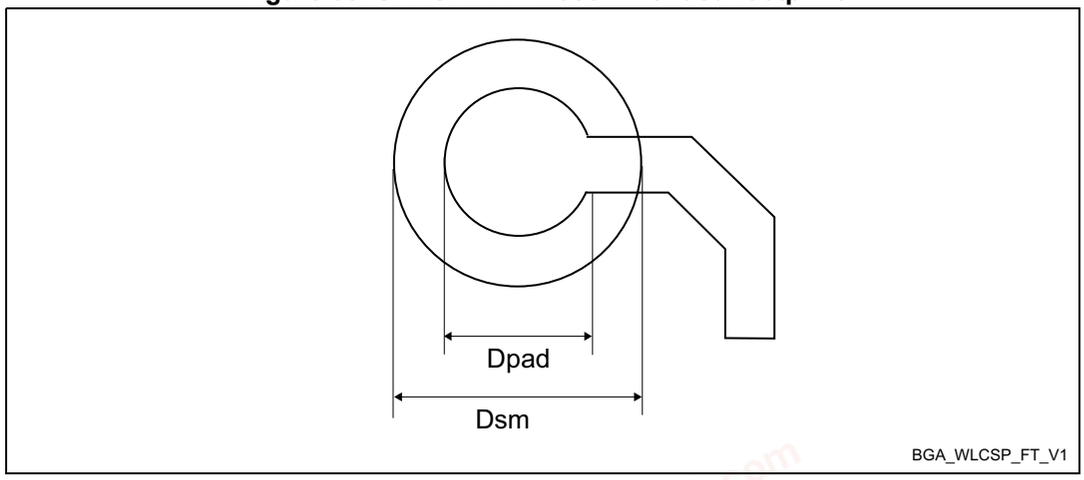


Table 146. UFBGA144 - Recommended PCB design rules (0.80 mm pitch BGA)

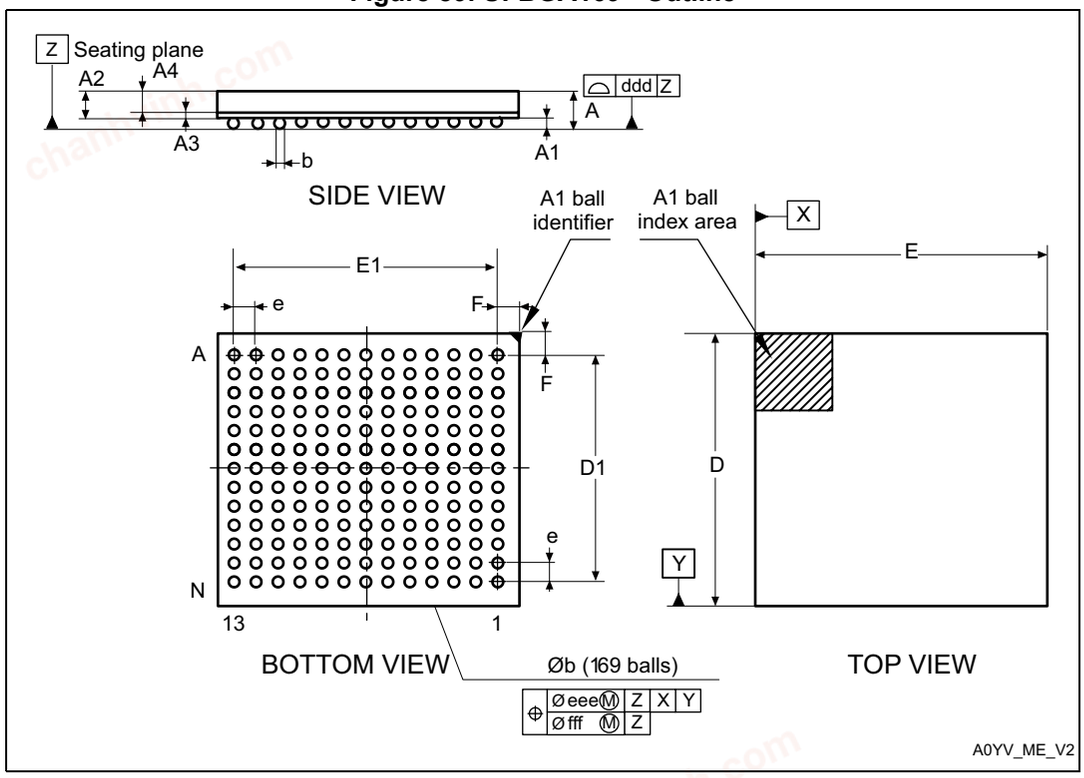
Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

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7.7 UFBGA169 package information (A0YV)

This UFBGA is a 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Figure 89. UFBGA169 - Outline



1. Drawing is not to scale.

Table 147. UFBGA169 - Mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-
F	0.450	0.500	0.550	0.0177	0.0197	0.0217

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Table 147. UFBGA169 - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 90. UFBGA169 - Recommended footprint

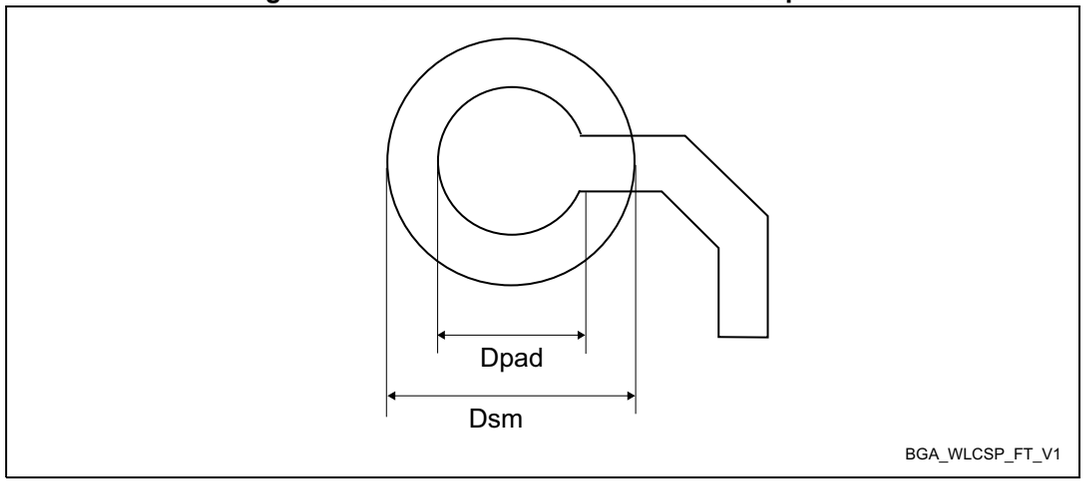


Table 148. UFBGA169 - Recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

Note: 4 to 6 mils solder paste screen printing process.

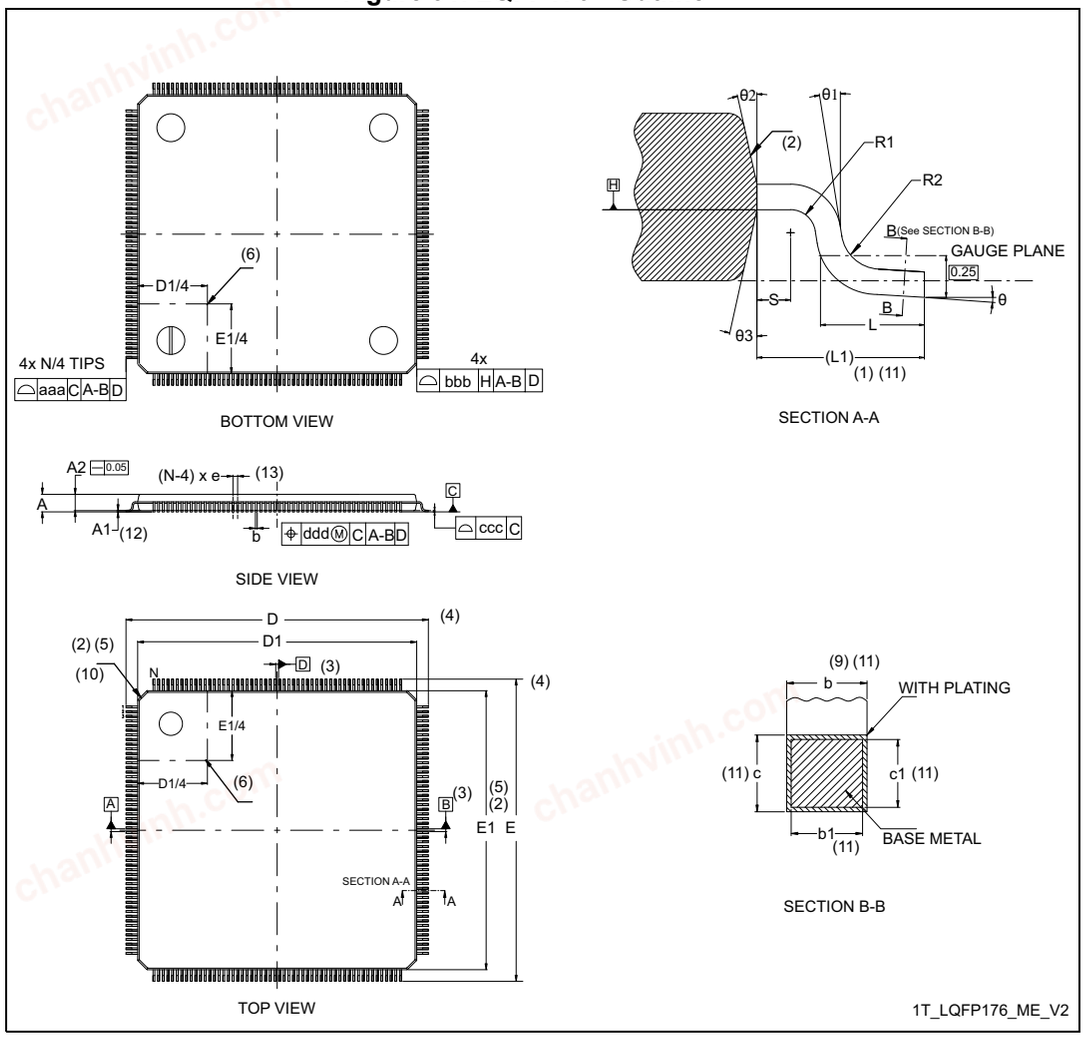
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7.8 LQFP176 package information (1T)

This LQFP is a 176-pin, 24 x 24 mm, 0.5 mm pitch, low profile quad flat package.

Note: See list of notes in the notes section.

Figure 91. LQFP176 - Outline(15)



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Table 149. LQFP176 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1[12]	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b[9][11]	0.170	0.220	0.270	0.0067	0.0087	0.0106
b1[11]	0.170	0.200	0.230	0.0067	0.0079	0.0091
c[11]	0.090	-	0.200	0.0035	-	0.0079
c1[11]	0.090	-	0.160	0.0035	-	0.063
D[4]	26.000			1.0236		
D1[2][5]	24.000			0.9449		
E[4]	26.000			0.0197		
E1[2][5]	24.000			0.9449		
e	0.500			0.1970		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1[1][11]	1			0.0394 REF		
N[13]	176					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.080	-	-	0.0031	-	-
R2	0.080	-	0.200	0.0031	-	0.0079
S	0.200	-	-	0.0079	-	-
aaa[1]	0.200			0.0079		
bbb[1]	0.200			0.0079		
ccc[1]	0.080			0.0031		
ddd[1]	0.080			0.0031		

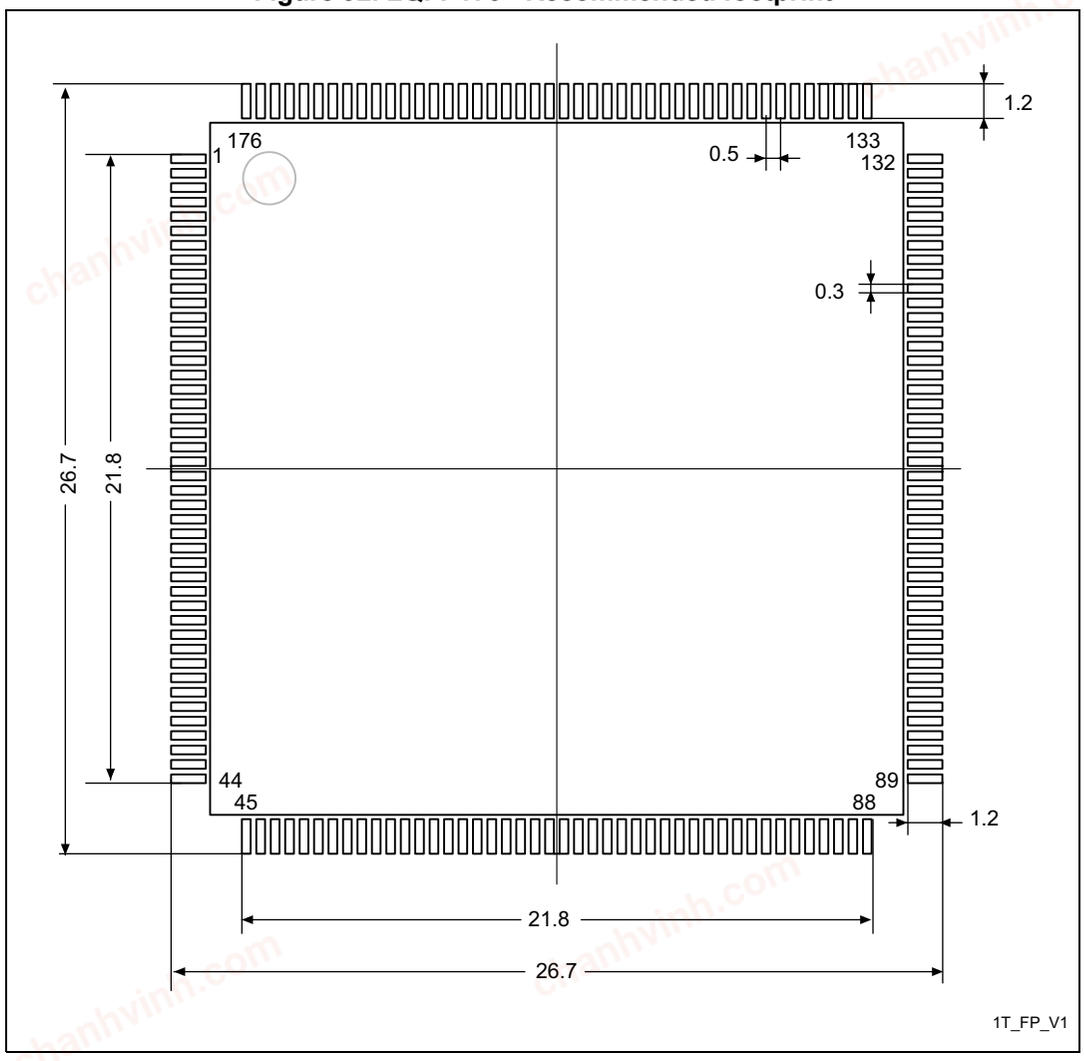
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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

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Figure 92. LQFP176 - Recommended footprint



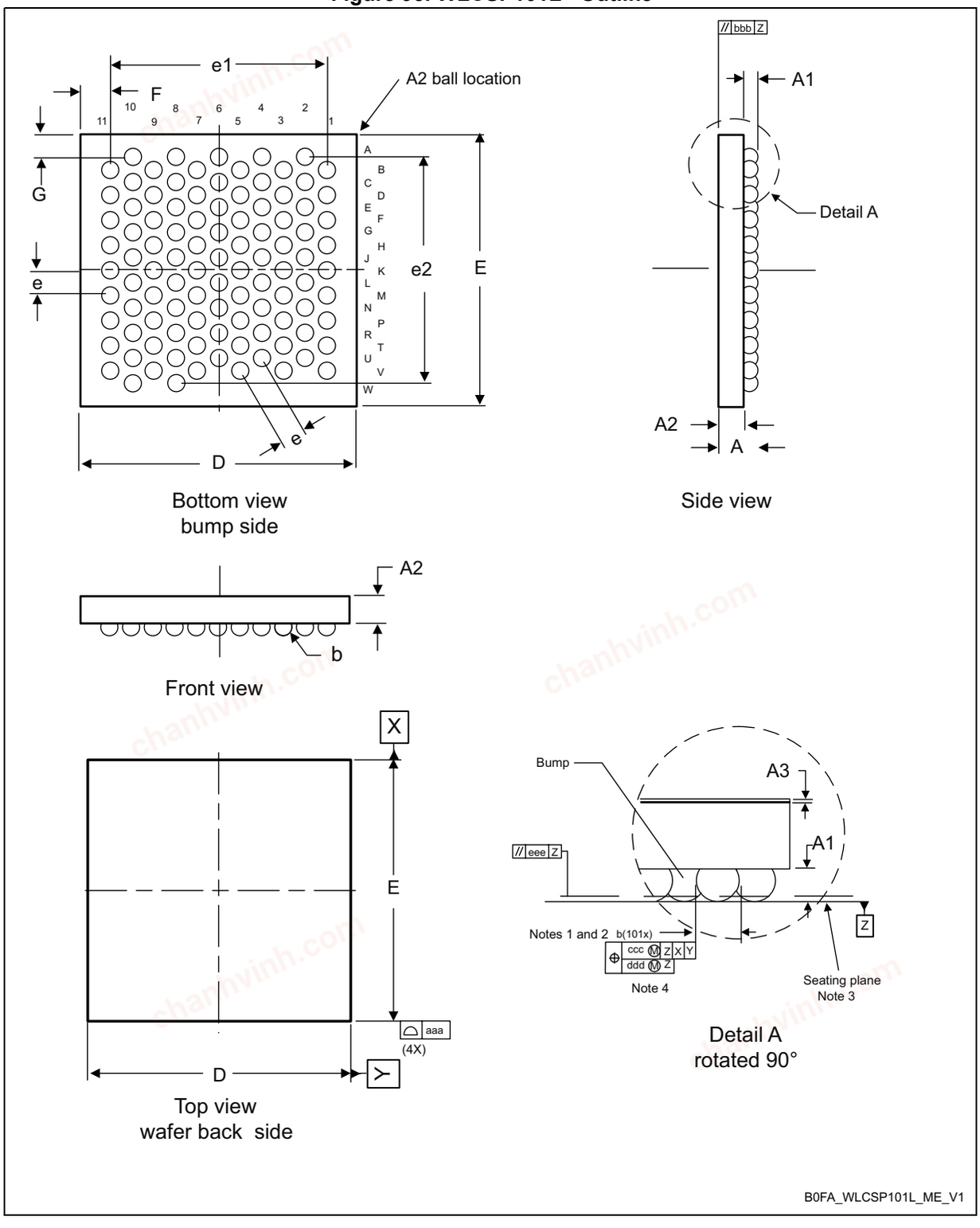
Dimensions are expressed in millimeters.

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7.9 WLCSP101 package information (B0FA)

This WLCSP is a 101 ball, 3.86 x 3.79 mm, 0.35 mm pitch, wafer level chip scale package.

Figure 93. WLCSP101L - Outline



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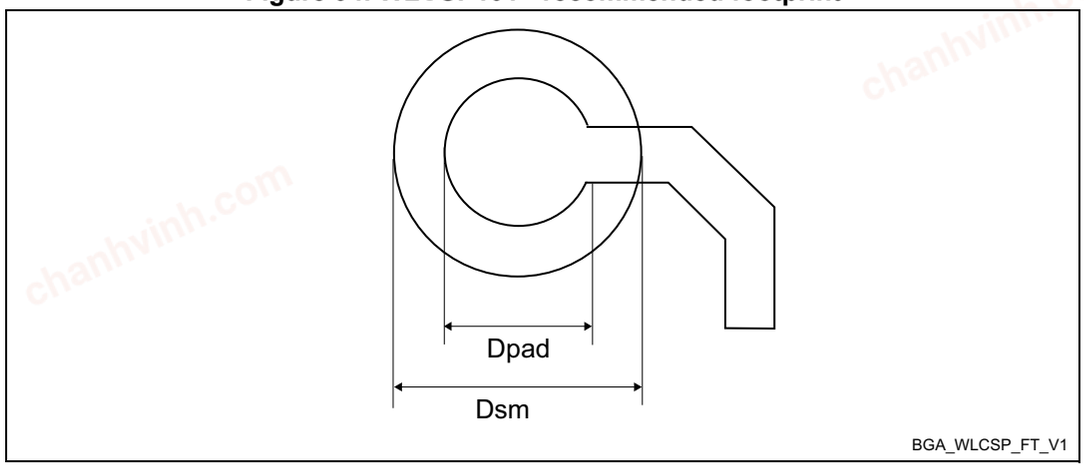
Table 150. WLCSP101 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.58	-	-	0.0228
A1	-	0.17		-	0.0065	-
A2	-	0.38	-	-	0.0150	-
A3[3]	-	0.025	-	-	0.0010	-
Øb[4]	0.21	0.24	0.27	0.0083	0.0094	0.0106
D	3.84	3.86	3.88	0.1512	0.1519	0.1527
E	3.77	3.79	3.81	0.1482	0.1490	0.1498
e	-	0.35	-	-	0.0138	-
e1	-	3.03	-	-	0.1193	-
e2	-	3.15	-	-	0.1240	-
F[5]	-	0.414	-	-	0.0163	-
G[5]	-	0.320	-	-	0.0125	-
N[6]	101					
Tolerance of form and position						
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc[7]	-	-	0.10	-	-	0.004
ddd[8]	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
5. Calculated dimensions are rounded to the third decimal place.
6. N is the total number of terminals.
7. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.
8. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone ddd perpendicular to datum Z and located on true position as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone. Each tolerance zone ddd in the array is contained entirely in the respective zone ccc above. The axis of each ball must lie simultaneously in both tolerance zones.

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Figure 94. WLCSP101 - recommended footprint



1. Dimensions are expressed in millimeters.

Table 151. WLCSP101 - recommended PCB design rules

Dimension	Recommended values
Pitch	0.35 mm
Dpad	0.210 mm
Dsm	0.275 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.235 mm
Stencil thickness	0.100 mm

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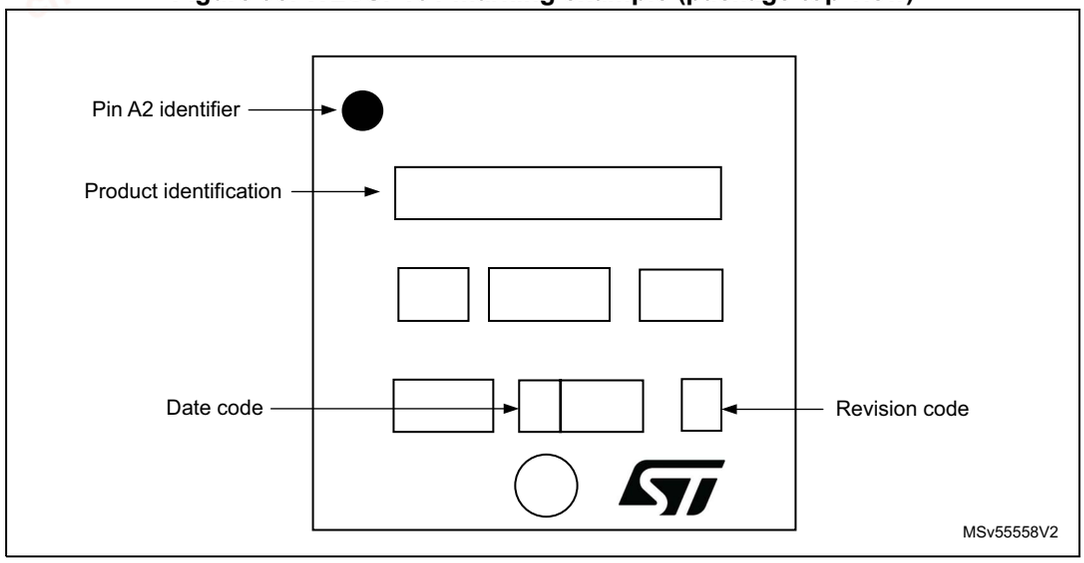
7.9.1 Device marking for WLCSP101

The following figure gives an example of topside marking orientation versus A2 ball identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

Figure 95. WLCSP101 marking example (package top view)

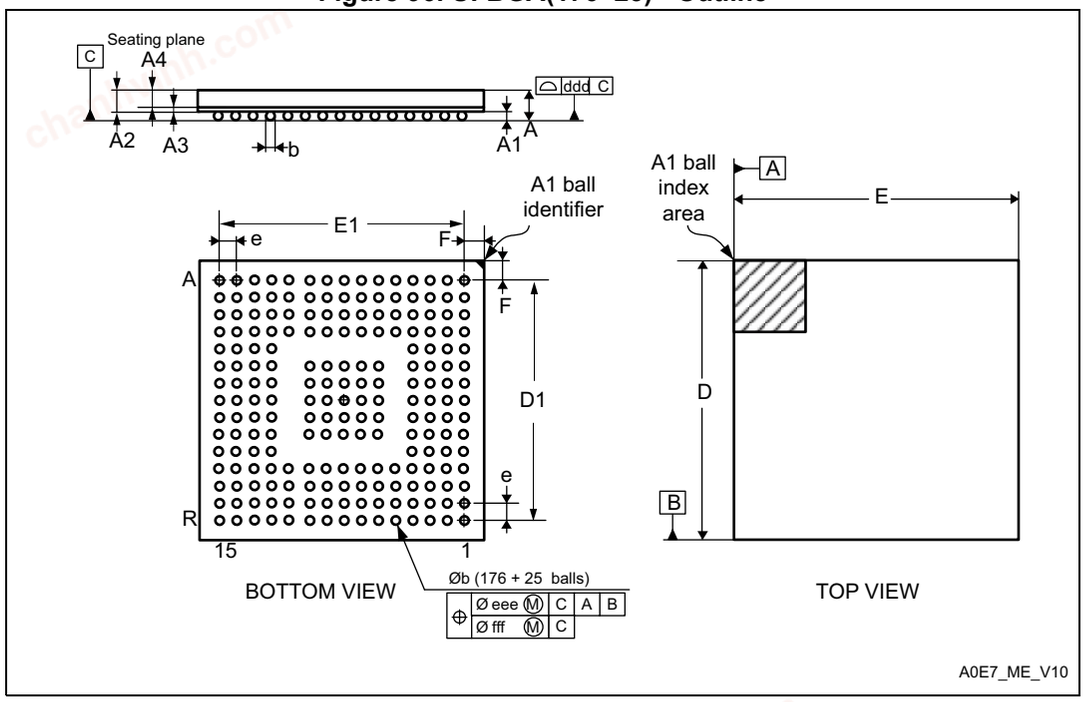


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7.10 UFBGA(176+25) package information (A0E7)

This UFBGA is a 176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package

Figure 96. UFBGA(176+25) - Outline



1. Drawing is not to scale.

Table 152. UFBGA(176+25) - Mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
F	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

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Table 152. UFBGA(176+25) - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 97. UFBGA(176+25) - Recommended footprint

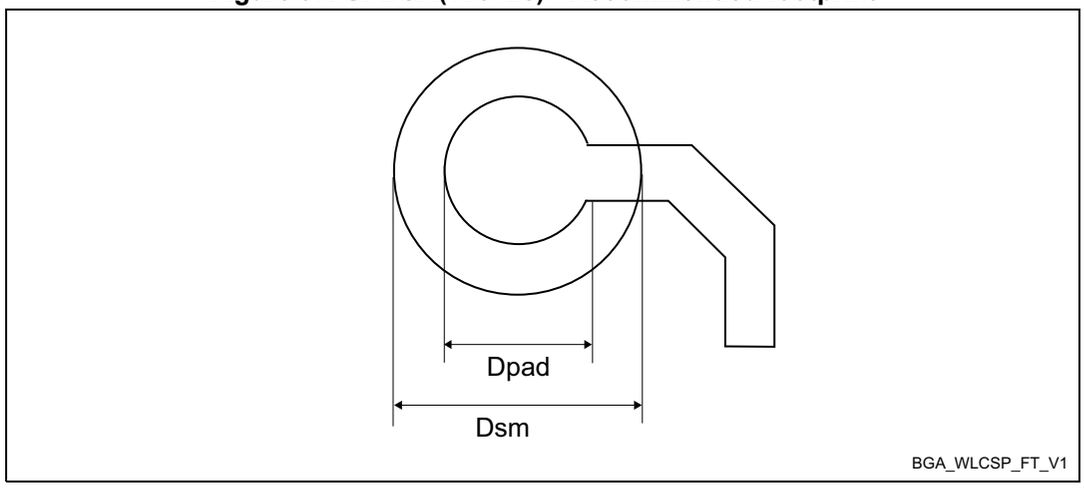


Table 153. UFBGA(176+25) - Recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

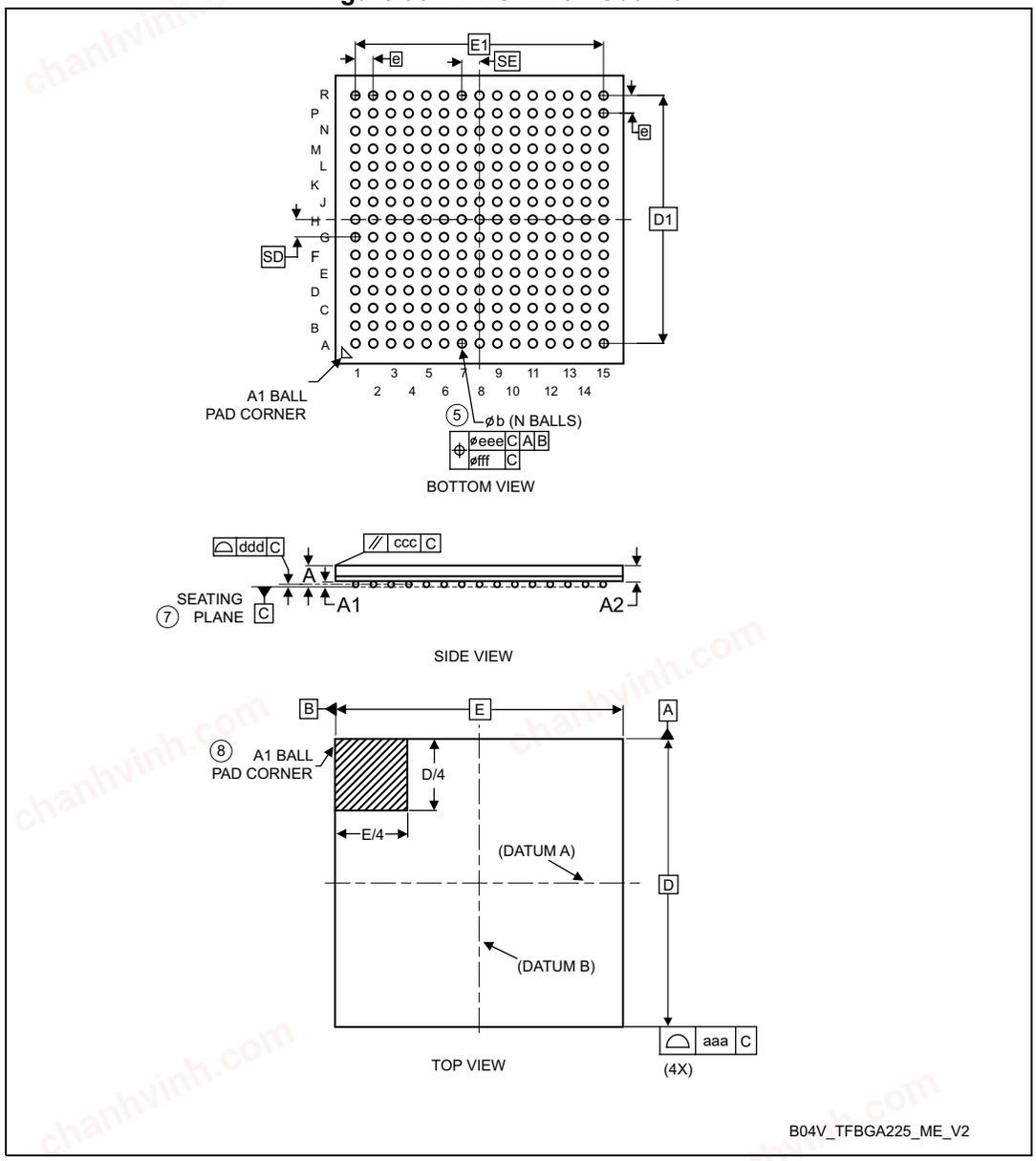
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7.11 TFBGA225 package information (B04V)

This TFBGA is a 225-ball, 13 x 13 mm, 0.8 mm pitch, thin profile fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 98. TFBGA225 - Outline(13)



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Table 154. TFBGA225 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	-	-	1.20	-	-	0.0472
A1[4]	0.15	-	-	0.0059	-	-
A2	-	0.76	-	-	0.0299	-
b[5]	0.35	0.40	0.45	0.0138	0.0157	0.0177
D[6]	13.00 BSC			0.5118 BSC		
D1	11.20 BSC			0.4409 BSC		
E	13.00 BSC			0.5118 BSC		
E1	11.20 BSC			0.4409 BSC		
e[9]	0.80 BSC			0.0315 BSC		
N[11]	225					
SD[12]	0.80 BSC			0.0315 BSC		
SE[12]	0.80 BSC			0.0315 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.0031		

Notes:

1. For dimensions in millimeters, dimensioning and tolerancing schemes conform to ASME Y14.5M-2018.
2. TFBGA stands for Thin profile Fine pitch Ball Grid Array: 1.00mm < A ≤ 1.20mm / Fine pitch e < 1.00mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or

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integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD & SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

Figure 99. TFBGA225 - Recommended footprint

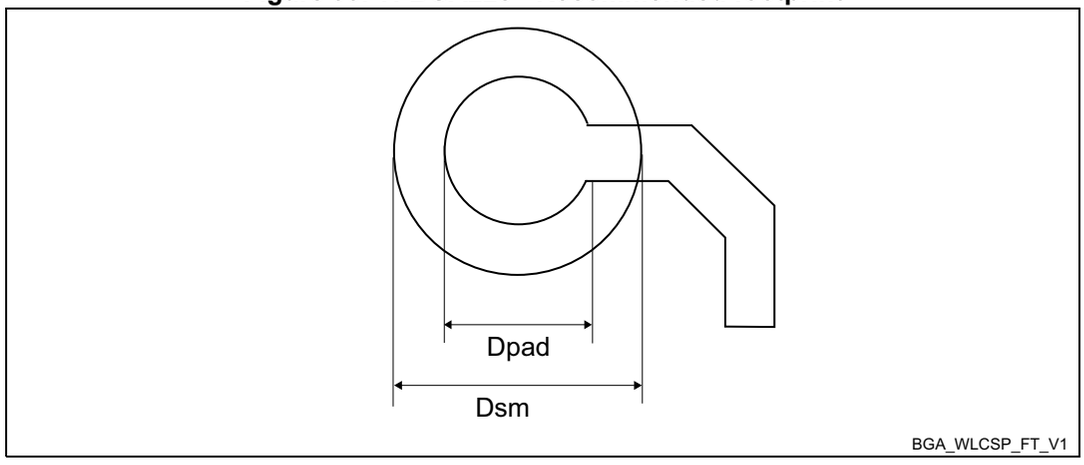


Table 155. TFBGA225 - Recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.400 mm
Dsm	0.550 mm
Stencil opening	0.400 mm
Stencil thickness	0.125 to 0.100 mm

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7.12 Package thermal characteristics

The maximum chip-junction temperature, T_{Jmax} in degrees Celsius, can be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins:

$$P_{I/Omax} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} – V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 156. Package thermal characteristics

Symbol	Definition	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	Thermal resistance junction-ambient VFQFPN68 - 8 x 8 mm / 0.35 mm pitch	23.8	°C/W
		Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	34.9	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm / 0.5 mm pitch	36.4	
		Thermal resistance junction-ambient LQFP176 - 24 x 24 mm / 0.5 mm pitch	35.9	
		Thermal resistance junction-ambient WLCSP101 - 3.86 x 3.79 mm / 0.35 mm pitch	43.2	
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm / 0.8 mm pitch	35.0	
		Thermal resistance junction-ambient UFBGA144 - 10 x 10 mm / 0.8 mm pitch	35.0	
		Thermal resistance junction-ambient UFBGA169 - 7 x 7 mm / 0.5 mm pitch	37.1	
		Thermal resistance junction-ambient UFBGA176 - 10 x 10 mm / 0.65 mm pitch	35.7	
		Thermal resistance junction-ambient TFBGA225 - 13 x 13 mm / 0.8 mm pitch	32.8	

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Table 156. Package thermal characteristics (continued)

Symbol	Definition	Parameter	Value	Unit
Θ_{JB}	Thermal resistance junction-ambient	Thermal resistance junction-ambient VQFN68 - 8 x 8 mm / 0.35 mm pitch	9.0	°C/W
		Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	20.8	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm / 0.5 mm pitch	25.3	
		Thermal resistance junction-ambient LQFP176 - 24 x 24 mm / 0.5 mm pitch	25.9	
		Thermal resistance junction-ambient WLCSP101 - 3.86 mm / 0.35 mm pitch	21.1	
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm / 0.8 mm pitch	22.0	
		Thermal resistance junction-ambient UFBGA144 - 10 x 10 mm / 0.8 mm pitch	22.9	
		Thermal resistance junction-ambient UFBGA169 - 7 x 7 mm / 0.5 mm pitch	22.8	
		Thermal resistance junction-ambient UFBGA176 - 10 x 10 mm / 0.65 mm pitch	23.6	
		Thermal resistance junction-ambient TFBGA225 - 13 x 13 mm / 0.8 mm pitch	22.3	
Θ_{JC}	Thermal resistance junction-ambient	Thermal resistance junction-ambient VQFN68 - 8 x 8 mm / 0.35 mm pitch	10.7	°C/W
		Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	7.7	
		Thermal resistance junction-ambient LQFP144 - 20 x 20 mm / 0.5 mm pitch	7.9	
		Thermal resistance junction-ambient LQFP176 - 24 x 24 mm / 0.5 mm pitch	9.2	
		Thermal resistance junction-ambient WLCSP101 - 3.86 mm / 0.35 mm pitch	1.8	
		Thermal resistance junction-ambient TFBGA100 - 8 x 8 mm / 0.8 mm pitch	12.6	
		Thermal resistance junction-ambient UFBGA144 - 10 x 10 mm / 0.8 mm pitch	9.0	
		Thermal resistance junction-ambient UFBGA169 - 7 x 7 mm / 0.5 mm pitch	9.4	
		Thermal resistance junction-ambient UFBGA176 - 10 x 10 mm / 0.65 mm pitch	9.0	
		Thermal resistance junction-ambient TFBGA225 - 13 x 13 mm / 0.8 mm pitch	12.0	

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8 Ordering information

Example: STM32 H 7S3 Z 8 J 6 H

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

H = High performance

Device subfamily

7S3 = STM32H7S3x8

7S7 = STM32H7S7x8

Pin count

R = 68 pins

V = 100 or 101 pins/balls

Z = 144 pins

A = 169 balls

I = 176 pins/balls

L = 225 balls

Flash memory size

8 = 64 Kbytes

Package

J = UFBGA pitch 0.8 ECOPACK2

Y = WLCSP pitch 0.35 ECOPACK2

V = VFQFPN pitch 0.4 ECOPACK2

T = LQFP ECOPACK2

K = UFBGA pitch 0.65 mm ECOPACK2

I = UFBGA pitch 0.5 mm ECOPACK2

H = TFBGA ECOPACK2

Temperature range

6 = –40 to 85 °C

Hexadeca SPI support

No character = Octo/Quad SPI support

H = Hexadeca SPI support

For a list of available options (speed, package, and so on) or for further information on any aspect of this device, contact your nearest ST sales office.

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10 Revision history

Table 157. Document revision history

Date	Revision	Changes
02-Nov-2023	1	Initial release.
13-Mar-2024	2	Corrected maximum CPU frequency in *Table 3: STM32H7Sxx8 features and peripheral counts*. Added *Section 6: Electrical characteristics*.

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