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STM32H533xx

Arm® Cortex®-M33 32-bit MCU+TrustZone® + FPU, 375 DMIPS 250 MHz, 512-Kbyte flash, 272-Kbyte RAM, cryptography

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

Core

- Arm® Cortex®-M33 CPU with TrustZone®, FPU, frequency up to 250 MHz, MPU, 375 DMIPS (Dhrystone 2.1)

ART Accelerator

- 8-Kbyte instruction cache allowing 0-wait-state execution from flash and external memories
- 4-Kbyte data cache for external memories

Benchmarks

- 1.5 DMIPS/MHz (Drystone 2.1)
- 1023 CoreMark® (4.092 CoreMark®/MHz)

Memories

- Up to 512 Kbytes of embedded flash memory with ECC, two banks read-while-write
- Up to 48-Kbyte per bank with high-cycling capability (100 K cycles) for data flash
- 2-Kbyte OTP (one-time programmable)
- 272 Kbytes of SRAM (80-Kbyte SRAM2 with ECC)
- 2 Kbytes of backup SRAM available in the lowest power modes
- Flexible external memory controller with up to 16-bit data bus: SRAM, PSRAM, FRAM, NOR/NAND memories
- One Octo-SPI memory interface with support for serial PSRAM/NAND/NOR, hyper RAM/flash frame formats
- One SD/SDIO/MMC interface



LQFP48 (7 x 7 mm)
LQFP64 (10 x 10 mm)
LQFP100 14 x 14 mm)
LQFP144 (20 x 20 mm)



UFBGA100 (7 x 7 mm)
UFBGA144 (10 x 10 mm)



UFQFPN48 (7 x 7 mm)



WLCSP39 (2.76 x 2.78 mm, pitch 0.4mm)

Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-50 MHz HSE, 32.768 kHz LSE

General-purpose inputs/outputs

- Up to 112 fast I/Os with interrupt capability (most 5 V tolerant)
- Up to ten I/Os with independent supply down to 1.08 V

Low-power consumption

- Sleep, Stop, and Standby modes
- V_{BAT} supply for RTC, 32 backup registers (32-bit)

Security

- Arm® TrustZone® with Armv8-M mainline security extension
- Up to eight configurable SAU regions
- TrustZone® aware and securable peripherals

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- Flexible life cycle scheme with secure debug authentication
- SESIP3 and PSA Level 3 certified assurance target
- Preconfigured immutable root of trust (ST-iROT)
- SFI (secure firmware installation)
- Root of trust thanks to unique boot entry and secure hide protection area (HDP)
- Secure data storage with hardware unique key (HUK)
- Secure firmware upgrade support with TF-M
- Two AES coprocessors including one with DPA resistance
- Public key accelerator, DPA resistant
- On-the-fly decryption of Octo-SPI external memories
- HASH hardware accelerator
- True random number generator, NIST SP800-90B compliant
- 96-bit unique ID
- Active tampers

Two DMA controllers to offload the CPU

- Two dual-port DMAs with FIFO

Reset and supply management

- 1.71 V to 3.6 V application supply and I/O
- POR, PDR, PVD, and BOR
- Embedded regulator with configurable scalable output to supply the digital circuitry

Up to 16 timers

- 10x 16-bit (including two low-power 16-bit timers available in Stop mode)
- Two 32-bit timers with up to four IC/OC/PWM or pulse counters and quadrature (incremental) encoder input
- Two watchdogs
- Two SysTick timers

Up to 34 communication interfaces

- Up to three I2Cs Fm+ (SMBus/PMBus®)
- Two I3Cs
- Up to six U(S)ARTs (ISO7816 interface, LIN, IrDA, modem control) and one LPUART
- Up to four SPIs including three muxed full-duplex I2S audio class accuracy via internal audio PLL or external clock, and up to four additional SPIs from four USARTs when configured in Synchronous mode (one additional SPI with OctoSPI)
- Two FDCAN controllers
- One 8- to 14-bit camera interface
- One 16-bit parallel slave synchronous-interface
- One HDMI-CEC
- One USB 2.0 full-speed host and device (crystal-less)
- One USB Type-C®/ USB Power Delivery r3.1

Analog

- Two 12-bit ADCs with up to 5 Msps in 12-bit
- One 12-bit DAC with two channels
- Digital temperature sensor
- Voltage reference buffer

Debug

- Authenticated debug and flexible device life cycle
- Serial wire-debug (SWD), JTAG, Embedded Trace Macrocell™ (ETM)

ECOPACK2 compliant packages

Table 1. Device summary

Reference	Part numbers
STM32H533xx	STM32H533CE, STM32H533HE, STM32H533RE, STM32H533VE, STM32H533ZE

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Contents

1 Introduction . . . 13

2 Description . . . 14

3 Functional overview . . . 18

3.1 Arm Cortex-M33 core with TrustZone and FPU . . . 18

3.2 ART Accelerator (ICACHE and DCACHE) . . . 18

3.2.1 Instruction cache (ICACHE) . . . 18

3.2.2 Data cache (DCACHE) . . . 19

3.3 Memory protection unit . . . 20

3.4 Embedded flash memory . . . 20

3.4.1 FLASH security and protections . . . 21

3.4.2 FLASH privilege protection . . . 21

3.5 Embedded SRAMs . . . 21

3.5.1 SRAMs TrustZone security . . . 22

3.5.2 SRAMs privilege protection . . . 22

3.6 Security overview . . . 22

3.7 Boot modes . . . 23

3.7.1 STM32H533xx boot modes . . . 23

3.8 Global TrustZone controller (GTZC) . . . 24

3.9 TrustZone security architecture . . . 25

3.9.1 TrustZone peripheral classification . . . 25

3.9.2 Default TrustZone security state . . . 26

3.10 Power supply management . . . 26

3.10.1 Power supply schemes . . . 27

3.10.2 Power supply supervisor . . . 29

3.10.3 Reset mode . . . 30

3.10.4 VBAT operation . . . 30

3.10.5 PWR TrustZone security . . . 31

3.11 Peripheral interconnect matrix . . . 31

3.12 Reset and clock controller (RCC) . . . 31

3.12.1 RCC TrustZone security . . . 32

3.13 Clock recovery system (CRS) . . . 32

chanhvinh.com

3.14 General-purpose inputs/outputs (GPIOs) . . . 33
3.14.1 GPIOs TrustZone security . . . 33
3.15 Multi-AHB bus matrix . . . 33
3.16 General purpose direct memory access controller (GPDMA) . . . 33
3.17 Interrupts and events . . . 35
3.17.1 Nested vectored interrupt controller (NVIC) . . . 35
3.17.2 Extended interrupt/event controller (EXTI) . . . 35
3.18 Cyclic redundancy check calculation unit (CRC) . . . 36
3.19 Flexible memory controller (FMC) . . . 36
3.19.1 LCD parallel interface . . . 36
3.19.2 FMC TrustZone security . . . 36
3.20 Octo-SPI interface (OCTOSPI) . . . 37
3.20.1 OCTOSPI TrustZone security . . . 37
3.21 Delay block (DLYB) . . . 38
3.22 Analog-to-digital converter (ADC1 and ADC2) . . . 38
3.22.1 Analog temperature sensor . . . 39
3.22.2 Internal voltage reference (VREFINT) . . . 39
3.22.3 VBAT battery voltage monitoring . . . 39
3.23 Digital temperature sensor (DTS) . . . 39
3.24 Digital to analog converter (DAC) . . . 39
3.25 Voltage reference buffer (VREFBUF) . . . 40
3.26 Digital camera interface (DCMI) . . . 40
3.27 Parallel synchronous slave interface (PSSI) . . . 41
3.28 True random number generator (RNG) . . . 41
3.29 Secure advanced encryption standard hardware accelerator (SAES) and encryption standard hardware accelerator (AES) . . . 42
3.30 HASH hardware accelerator (HASH) . . . 43
3.31 On-the-fly decryption engine (OTFDEC) . . . 44
3.32 Public key accelerator (PKA) . . . 45
3.33 Timers and watchdogs . . . 45
3.33.1 Advanced-control timers (TIM1, TIM8) . . . 46
3.33.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM12, TIM15) . . . 46
3.33.3 Basic timers (TIM6 and TIM7) . . . 47
3.33.4 Low-power timers (LPTIM1, LPTIM2) . . . 47

chanhvinh.com

3.33.5 Independent watchdog (IWDG) . . . 47
3.33.6 Window watchdog (WWDG) . . . 48
3.33.7 SysTick timer . . . 48
3.34 Real-time clock (RTC), tamper and backup registers . . . 48
3.34.1 Real-time clock (RTC) . . . 48
3.34.2 Tamper and backup registers (TAMP) . . . 49
3.35 Inter-integrated circuit interface (I^2C) . . . 50
3.36 Improved inter-integrated circuit (I3C) . . . 51
3.37 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART) . . . 52
3.37.1 Universal synchronous/asynchronous receiver transmitter (USART/UART) . . . 53
3.37.2 Low-power universal asynchronous receiver transmitter (LPUART) . . . 54
3.38 Serial peripheral interface (SPI) / inter-integrated sound interfaces (I2S) 56
3.39 Secure digital input/output and MultiMediaCards interface (SDMMC) . . . 57
3.40 Controller area network (FDCAN) . . . 58
3.41 USB full speed (USB) . . . 59
3.42 USB Type-C / USB Power Delivery controller (UCPD) . . . 59
3.43 High-definition multimedia interface (HDMI) - consumer electronics control (CEC) . . . 60
3.44 Development support . . . 60
3.44.1 Serial-wire/JTAG debug port (SWJ-DP) . . . 60
3.44.2 Embedded Trace Macrocell . . . 60

4 Pinout, pin description and alternate function . . . 61
4.1 Pinout/ballout schematics . . . 61
4.2 Pin description . . . 66
4.3 Alternate functions . . . 82

5 Electrical characteristics . . . 96
5.1 Parameter conditions . . . 96
5.1.1 Minimum and maximum values . . . 96
5.1.2 Typical values . . . 96
5.1.3 Typical curves . . . 96
5.1.4 Loading capacitor . . . 96

chanhvinh.com

5.1.5 Pin input voltage . . . 96
5.1.6 Power supply scheme . . . 97
5.2 Absolute maximum ratings . . . 98
5.3 Operating conditions . . . 99
5.3.1 General operating conditions . . . 99
5.3.2 VCAP external capacitor . . . 103
5.3.3 Operating conditions at power-up/down . . . 103
5.3.4 Embedded reset and power control block characteristics . . . 104
5.3.5 Embedded reference voltage . . . 105
5.3.6 Supply current characteristics . . . 106
5.3.7 External clock source characteristics . . . 118
5.3.8 Internal clock source characteristics . . . 122
5.3.9 PLL characteristics . . . 125
5.3.10 Memory characteristics . . . 126
5.3.11 EMC characteristics . . . 127
5.3.12 Absolute maximum ratings (electrical sensitivity) . . . 129
5.3.13 I/O current injection characteristics . . . 130
5.3.14 I/O port characteristics . . . 130
5.3.15 NRST pin characteristics . . . 144
5.3.16 Extended interrupt and event controller input (EXTI) characteristics . . . 145
5.3.17 FMC characteristics . . . 145
5.3.18 Octo-SPI interface characteristics . . . 162
5.3.19 Delay block (DLYB) characteristics . . . 166
5.3.20 DCMI interface characteristics . . . 166
5.3.21 PSSI interface characteristics . . . 167
5.3.22 12-bit ADC characteristics . . . 170
5.3.23 DAC characteristics . . . 178
5.3.24 Analog temperature sensor characteristics . . . 181
5.3.25 Digital temperature sensor characteristics . . . 182
5.3.26 V_{CORE} monitoring characteristics . . . 182
5.3.27 Temperature and V_{BAT} monitoring . . . 183
5.3.28 Voltage booster for analog switch . . . 183
5.3.29 V_{REFBUF} characteristics . . . 184
5.3.30 Timer characteristics . . . 185
5.3.31 Low-power timer characteristics . . . 186
5.3.32 Communication interfaces . . . 186

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6 Package information 201

6.1 Device marking 201

6.2 WLCSP39 package information (B0MM) 202

6.3 LQFP48 package information (5B) 205

6.4 LQFP64 package information (5W) 208

6.5 UFQFPN48 package information (A0B9) 211

6.6 LQFP100 package information (1L) 213

6.7 UFBGA100 package information (A0C2) 216

6.8 LQFP144 package information (1A) 219

6.9 UFBGA144 package information (A0Y2) 223

6.10 Package thermal characteristics 226

6.10.1 Reference documents 227

7 Ordering information 228

8 Important security notice 229

9 Revision history 230

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List of tables

Table 1. Device summary . . . 2
Table 2. STM32H533xx features and peripheral counts . . . 15
Table 3. STM32H533xx boot mode when TrustZone is disabled (TZEN = 0xC3) . . . 24
Table 4. STM32H533xx boot mode when TrustZone is enabled (TZEN = 0xB4) . . . 24
Table 5. ADC features . . . 38
Table 6. AES/SAES features . . . 43
Table 7. Timer features . . . 45
Table 8. I2C implementation . . . 51
Table 9. I3C peripheral controller/target features versus MIPI v1.1 . . . 52
Table 10. USART, UART and LPUART features . . . 52
Table 11. SPI features . . . 57
Table 12. SDMMC features . . . 58
Table 13. Legend/abbreviations used in the pinout table . . . 66
Table 14. STM32H533xx pin/ball definition . . . 67
Table 15. Alternate function AF0 to AF7 . . . 82
Table 16. Alternate function AF8 to AF15 . . . 89
Table 17. Voltage characteristics . . . 98
Table 18. Current characteristics . . . 99
Table 19. Thermal characteristics . . . 99
Table 20. General operating conditions . . . 99
Table 21. Maximum allowed clock frequencies . . . 102
Table 22. Supply voltage and maximum frequency configuration . . . 103
Table 23. Operating conditions at power-up/down (regulator ON) . . . 103
Table 24. Embedded reset and power control block characteristics . . . 104
Table 25. Embedded reference voltage . . . 105
Table 26. Internal reference voltage calibration value . . . 106
Table 27. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 2-way instruction cache ON, PREFETCH ON . . . 107
Table 28. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 1-way instruction cache ON, PREFETCH ON . . . 108
Table 29. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 1-way . . . 108
Table 30. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 2-way . . . 109
Table 31. Typical consumption in Run mode with CoreMark running from flash memory and SRAM . . . 110
Table 32. Typical consumption in Run mode with SecureMark running from flash memory and SRAM . . . 111
Table 33. Typical and maximum current consumption in Sleep mode . . . 111
Table 34. Typical and maximum current consumption in Stop mode . . . 112
Table 35. Typical and maximum current consumption in Standby mode . . . 112
Table 36. Typical and maximum current consumption in VBAT mode . . . 112
Table 37. Peripheral current consumption in Sleep mode . . . 114
Table 38. Low-power mode wake-up timings . . . 117
Table 39. High-speed external user clock characteristics . . . 118
Table 40. Low-speed external user clock characteristics . . . 119
Table 41. 4-50 MHz HSE oscillator characteristics . . . 120
Table 42. Low-speed external user clock characteristics . . . 121

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Table 43. HSI48 oscillator characteristics . . . 122
Table 44. HSI oscillator characteristics . . . 123
Table 45. CSI oscillator characteristics . . . 124
Table 46. LSI oscillator characteristics . . . 124
Table 47. PLL characteristics (wide VCO frequency range) . . . 125
Table 48. PLL characteristics (medium VCO frequency range) . . . 126
Table 49. Flash memory characteristics . . . 126
Table 50. Flash memory programming . . . 127
Table 51. Flash memory endurance and data retention . . . 127
Table 52. EMS characteristics . . . 128
Table 53. EMI characteristics . . . 129
Table 54. ESD absolute maximum ratings . . . 129
Table 55. Electrical sensitivities . . . 130
Table 56. I/O current injection susceptibility . . . 130
Table 57. I/O static characteristics . . . 131
Table 58. Output voltage characteristics for all I/Os except PC13, PC14, and PC15 . . . 133
Table 59. Output voltage characteristics for FT_c I/Os (PB13/PB14) . . . 134
Table 60. Output voltage characteristics for PC13 . . . 134
Table 61. Output voltage characteristics for PC14 and PC15 . . . 135
Table 62. Output timing characteristics (HSLV OFF) . . . 136
Table 63. Output timing characteristics (HSLV ON) . . . 140
Table 64. Output timing characteristics VDDIO2 1.2 V range (HSLV OFF) . . . 141
Table 65. Output timing characteristics VDDIO2 1.2 V (HSLV ON) . . . 143
Table 66. Output timing characteristics for FT_c I/Os (PB13/PB14) . . . 144
Table 67. NRST pin characteristics . . . 145
Table 68. EXTI input characteristics . . . 145
Table 69. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings . . . 148
Table 70. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings . . . 148
Table 71. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . 149
Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings . . . 150
Table 73. Asynchronous multiplexed PSRAM/NOR read timings . . . 151
Table 74. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings . . . 151
Table 75. Asynchronous multiplexed PSRAM/NOR write timings . . . 152
Table 76. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings . . . 152
Table 77. Synchronous multiplexed NOR/PSRAM read timings . . . 154
Table 78. Synchronous multiplexed PSRAM write timings . . . 156
Table 79. Synchronous non-multiplexed NOR/PSRAM read timings . . . 157
Table 80. Synchronous non-multiplexed PSRAM write timings . . . 158
Table 81. Switching characteristics for NAND flash read cycles . . . 161
Table 82. Switching characteristics for NAND flash write cycles . . . 161
Table 83. OCTOSPI characteristics in SDR mode . . . 162
Table 84. OCTOSPI characteristics in DTR mode (no DQS) . . . 163
Table 85. OCTOSPI characteristics in DTR mode (with DQS) / hyperbus . . . 163
Table 86. Delay block characteristics . . . 166
Table 87. DCMI characteristics . . . 166
Table 88. PSSI transmit characteristics . . . 167
Table 89. PSSI receive characteristics . . . 168
Table 90. 12-bit ADC characteristics . . . 170
Table 91. Minimum sampling time versus R_{AIN} . . . 172
Table 92. ADC accuracy . . . 175
Table 93. DAC characteristics . . . 178
Table 94. DAC accuracy . . . 180

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Table 95. Analog temperature sensor characteristics . . . 181
Table 96. Temperature sensor calibration values . . . 182
Table 97. Digital temperature sensor characteristics . . . 182
Table 98. V_{CORE} monitoring characteristics . . . 182
Table 99. V_{BAT} monitoring characteristics . . . 183
Table 100. V_{BAT} charging characteristics . . . 183
Table 101. Temperature monitoring characteristics . . . 183
Table 102. Voltage booster for analog switch characteristics . . . 183
Table 103. V_{REFBUF} characteristics . . . 184
Table 104. TIMx characteristics . . . 185
Table 105. LPTIMx characteristics . . . 186
Table 106. I2C analog filter characteristics . . . 186
Table 107. USART characteristics . . . 187
Table 108. I3C open-drain measured timing . . . 189
Table 109. I3C push-pull measured timing . . . 189
Table 110. SPI characteristics . . . 190
Table 111. I^2S dynamic characteristics . . . 192
Table 112. USB DC electrical characteristics . . . 194
Table 113. USB startup time . . . 195
Table 114. USB electrical characteristics . . . 195
Table 115. USB BCD DC electrical characteristics . . . 195
Table 116. Dynamic characteristics: SD/MMC characteristics, VDD = 2.7 to 3.6 V . . . 196
Table 117. Dynamic characteristics: eMMC characteristics, VDD = 1.71 to 1.9 V . . . 197
Table 118. Dynamic JTAG characteristics . . . 199
Table 119. Dynamic SWD characteristics . . . 199
Table 120. WLCSP39 - Mechanical data . . . 203
Table 121. LQFP48 - Mechanical data . . . 206
Table 122. LQFP64 - Mechanical data . . . 209
Table 123. UFQFPN48 – Mechanical data . . . 212
Table 124. LQFP100 - Mechanical data . . . 214
Table 125. UFBGA100 - Mechanical data . . . 217
Table 126. UFBGA100 - Example of PCB design rules (0.5 mm pitch BGA) . . . 218
Table 127. LQFP144 - Mechanical data . . . 220
Table 128. UFBGA144 - Mechanical data . . . 224
Table 129. UFBGA144 - Example of PCB design rules (0.80 mm pitch BGA) . . . 225
Table 130. Package thermal characteristics . . . 226
Table 131. Document revision history . . . 230

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List of figures

Figure 1. STM32H533xx block diagram . . . 17
Figure 2. STM32H533xx power supply overview . . . 28
Figure 3. Power-up/down sequence . . . 29
Figure 4. WLCSP39 pinout . . . 61
Figure 5. LQFP48 pinout . . . 61
Figure 6. UFQFPN48 pinout . . . 62
Figure 7. LQFP64 pinout . . . 62
Figure 8. LQFP100 pinout . . . 63
Figure 9. UFBGA100 ballout . . . 63
Figure 10. LQFP144 pinout . . . 64
Figure 11. UFBGA144 ballout . . . 65
Figure 12. Pin loading conditions . . . 96
Figure 13. Pin input voltage . . . 96
Figure 14. STM32H523xx/H533xx power supply scheme . . . 97
Figure 15. External capacitor C_{EXT} . . . 103
Figure 16. High-speed external clock source AC timing diagram . . . 119
Figure 17. Low-speed external clock source AC timing diagram . . . 120
Figure 18. Typical application with an 8 MHz crystal . . . 121
Figure 19. Typical application with a 32.768 kHz crystal . . . 122
Figure 20. VIL/VIH for all I/Os except BOOT0 . . . 132
Figure 21. Recommended NRST pin protection . . . 145
Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . 147
Figure 23. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . 149
Figure 24. Asynchronous multiplexed PSRAM/NOR read waveforms . . . 150
Figure 25. Synchronous multiplexed NOR/PSRAM read timings . . . 153
Figure 26. Synchronous multiplexed PSRAM write timings . . . 155
Figure 27. Synchronous non-multiplexed NOR/PSRAM read timings . . . 157
Figure 28. Synchronous non-multiplexed PSRAM write timings . . . 158
Figure 29. NAND controller waveforms for read access . . . 159
Figure 30. NAND controller waveforms for write access . . . 160
Figure 31. NAND controller waveforms for common memory read access . . . 160
Figure 32. NAND controller waveforms for common memory write access . . . 161
Figure 33. OCTOSPI SDR read/write timing diagram . . . 162
Figure 34. OCTOSPI timing diagram - DTR mode . . . 164
Figure 35. OCTOSPI hyperbus clock . . . 165
Figure 36. OCTOSPI hyperbus read . . . 165
Figure 37. OCTOSPI hyperbus write . . . 165
Figure 38. DCMI timing diagrams . . . 167
Figure 39. PSSI transmit timing diagram . . . 169
Figure 40. PSSI receive timing diagram . . . 169
Figure 41. ADC conversion timing diagram . . . 174
Figure 42. ADC accuracy characteristics . . . 176
Figure 43. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function . . . 176
Figure 44. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) . . . 177
Figure 45. Power supply and reference decoupling (V_{REF+} connected to V_{DDA}) . . . 177
Figure 46. 12-bit buffered/non-buffered DAC . . . 181
Figure 47. USART timing diagram in Master mode . . . 188

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Figure 48. USART timing diagram in Slave mode . . . 188
Figure 49. SPI timing diagram - Master mode . . . 191
Figure 50. SPI timing diagram - Slave mode and CPHA = 0 . . . 191
Figure 51. SPI timing diagram - Slave mode and CPHA = 1 . . . 192
Figure 52. I^2S slave timing diagram (Philips protocol)(1) . . . 193
Figure 53. I^2S master timing diagram (Philips protocol)(1) . . . 194
Figure 54. USB timings - definition of data signal rise and fall time . . . 195
Figure 55. SDIO high-speed/eMMC timing . . . 198
Figure 56. SD default speed timings . . . 198
Figure 57. DDR mode timings . . . 198
Figure 58. JTAG timing diagram . . . 200
Figure 59. SWD timing diagram . . . 200
Figure 60. WLCSP39 - Outline . . . 202
Figure 61. WLCSP39 - Footprint example . . . 204
Figure 62. WLCSP39 - Marking example (package top view) . . . 204
Figure 63. LQFP48 - Outline(15) . . . 205
Figure 64. LQFP48 - Footprint example . . . 207
Figure 65. LQFP64 - Outline(15) . . . 208
Figure 66. LQFP64 - Footprint example . . . 210
Figure 67. UFQFPN48 – Outline . . . 211
Figure 68. UFQFPN48 – Footprint example . . . 212
Figure 69. LQFP100 - Outline(15) . . . 213
Figure 70. LQFP100 - Footprint example . . . 215
Figure 71. UFBGA100 - Outline(13) . . . 216
Figure 72. UFBGA100 - Footprint example . . . 218
Figure 73. LQFP144 - Outline(15) . . . 219
Figure 74. LQFP144 - Footprint example . . . 222
Figure 75. UFBGA144 - Outline(13) . . . 223
Figure 76. UFBGA144 - Footprint example . . . 225

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32H533xx microcontrollers.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32H533xx errata sheet.

For information on the Arm®(a) Cortex®-M33 core, refer to the Cortex®-M33 Technical Reference Manual, available from the www.arm.com website.

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2 Description

The STM32H533xx devices are high-performance microcontrollers of the STM32H5 series, based on the high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 250 MHz.

The Cortex®-M33 core features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types.

The Cortex®-M33 core implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (512 Kbytes of dual bank flash memory and 272 Kbytes of SRAM), a flexible external memory controller (FMC) for devices with packages of 100 pins and more, one OCTOSPI memory interface (at least one Quad-SPI available on all packages), and an extensive range of enhanced I/Os and peripherals connected to three APB buses, three AHB buses, and a 32-bit multi-AHB bus matrix.

The devices offer security foundation compliant with the trusted-based security architecture (TBSA) requirements from Arm®. Besides these capabilities, the devices incorporate a secure firmware installation that allows the customer to secure the provisioning of the code during its production. A flexible life cycle is managed thanks to multiple levels of protection and secure debug authentication. Firmware hardware isolation is supported thanks to securable peripherals, memories, and I/Os, and to privilege configuration of peripherals and memories.

The devices feature several protection mechanisms for embedded flash memory and SRAM: readout protection, write protection, secure, and hide protection areas.

Dedicated peripherals reinforce security: an HASH hardware accelerator, and a true random number generator.

The devices offer active tamper detection and protection against transient and environmental perturbation attacks, thanks to several internal monitoring, generating secret data erase in case of attack. This helps to fit the PCI requirements for point of sales applications.

The devices offer two fast 12-bit ADCs, two DAC channels, an internal voltage reference buffer, a low-power RTC, two 32-bit general-purpose timers, two 16-bit PWM timers dedicated to motor control, eight 16-bit general-purpose timers, two 16-bit basic timers, and six 16-bit low-power timers.

The devices also feature standard and advanced communication interfaces, namely: three I^2Cs, two I3Cs, four SPIs with three muxed full-duplex I2S, four USARTs, two UARTs and one low-power UART, one digital camera interface (DCMI), one SDMMC, two FDCANs, one USB full-speed, one USB Type-C®/USB power delivery controller.

The devices operate in the -40 to +85 °C/105 °C (+130 °C junction), and to 125 °C at low dissipation temperature ranges from a 1.71 to 3.6 V power supply.

A comprehensive set of power-saving modes allow the design of low-power applications.

Independent power supplies are supported: an analog independent supply input for ADC, DACs, a 3.3 V dedicated supply input for USB, and a dedicated supply input for some GPIOs and SDMMC. A VBAT input is available to connect a backup battery, to preserve the RTC functionality, and to backup 32x 32-bit registers and a 2-Kbyte SRAM.

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The devices offer eight packages, from 39 to 144 pins.

Table 2. STM32H533xx features and peripheral counts

Peripherals		STM32H533HE	STM32H533CE	STM32H533RE	STM32H533VE	STM32H533ZE
Flash memory (Kbytes)		512				
SRAM	System (Kbytes)	272 (128+80+64)				
	Backup (bytes)	2K				
Flexible memory controller for external memories (FMC)		No			Yes(1)	Yes
OCTOSPI		Yes				
Timers	Advanced control	2(16 bits)				
	General purpose	2 (32 bits) 4 (16 bits)				
	Basic	2 (16 bits)				
	Low power	2 (16 bits)				
	SysTick timer	2 (24 bits)				
	Watchdog timers (independent, window)	2				
Communication interfaces	SPI / I2S	3/2	4/3			
	I2C	2	3			
	I3C	2				
	USART	2	3	4		
	UART	2				
	LPUART	1				
	FDCAN	2				
	USB FS	Yes				
	UCPD	No	Yes			
	SDMMC	No		Yes		
	Digital camera interface (DCMI)/ PSSI(2)	No		Yes		
HDMI-CEC		Yes				
Real time clock (RTC)		Yes				
Tamper pins		4	4	5	8	8

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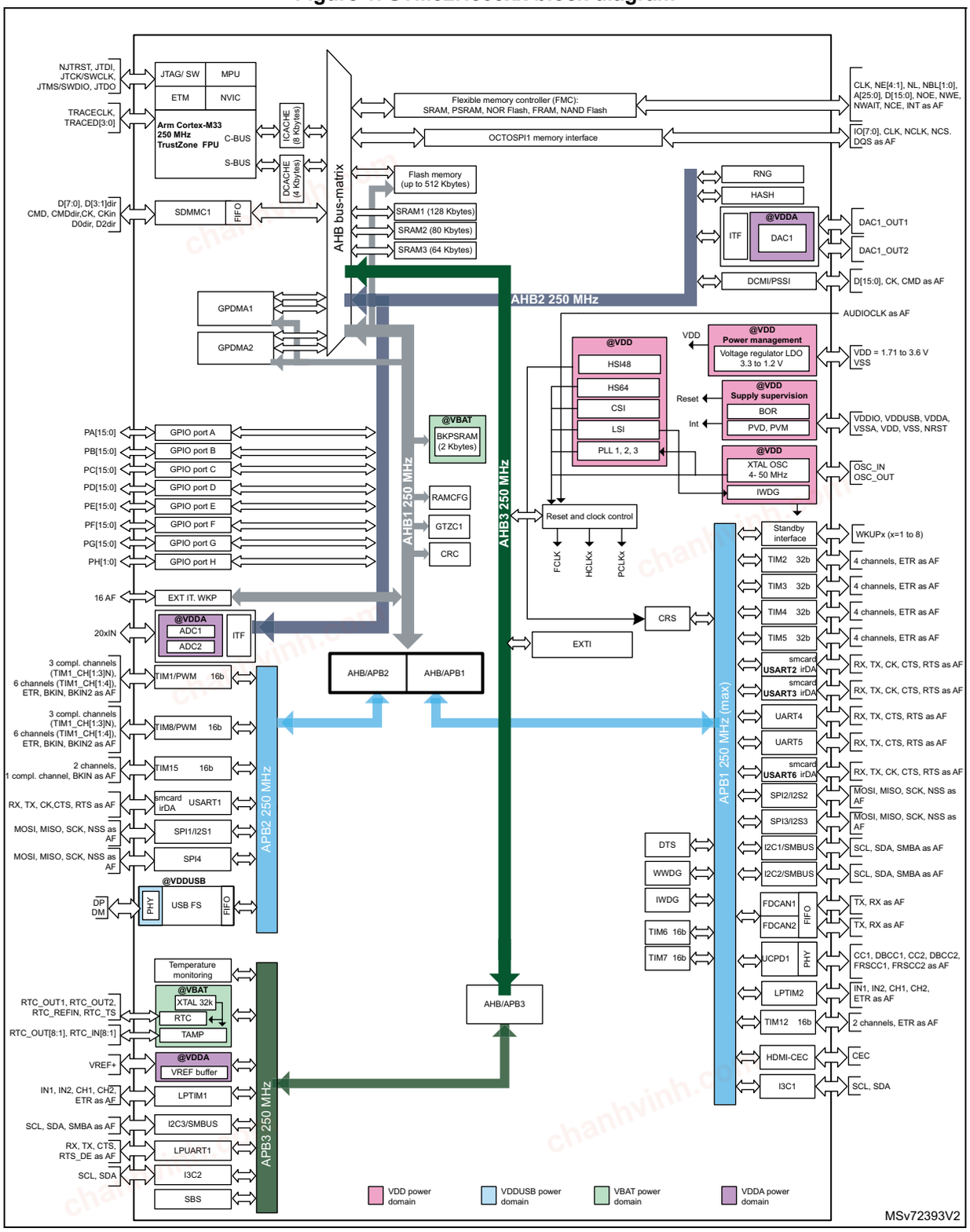
Table 2. STM32H533xx features and peripheral counts (continued)

Peripherals		STM32H533HE	STM32H533CE	STM32H533RE	STM32H533VE	STM32H533ZE
Active tampers(3)		3	3	4	7	7
True random number generator		Yes				
SAES, AES		Yes				
Public key accelerator (PKA)		Yes				
HASH (SHA-512)		Yes				
On-the-fly decryption for OCTOSPI		Yes				
GPIOs		26	35	49	80	112
Wakeup pins		4	4	6	7	7
Number of I/Os down to 1.08 V		N/A			4	10
ADC	12-bit ADC	2				
	Number of channels	10		16		20
DAC	12-bit DAC controller	1				
	Number of channels	2				
Internal voltage reference buffer		No			Yes	
Maximum CPU frequency		250 MHz				
Operating voltage		1.71 to 3.6 V				
Operating temperature		Ambient operating temperature: -40 to 85 °C / -40 to 105 °C Junction temperature: -40 to 130 °C				
Package		WLCSP39	UFQFPN48/ LQFP48	LQFP64	LQFP100/ UFBGA100	LQFP144/ UFBGA144

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. DCMI and PSSI cannot be used at the same time as they share the same circuitry.
3. Active tampers in output sharing mode (one output shared by all inputs).

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Figure 1. STM32H533xx block diagram



Note: PC[15:13] are in the V_{BAT} domain.

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3 Functional overview

3.1 Arm Cortex-M33 core with TrustZone and FPU

The Cortex-M33 with TrustZone and FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex-M33 processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. It features:

- Arm TrustZone technology, using the Armv8-M main extension supporting secure and non-secure states
- Memory protection units (MPUs), supporting up to 16 regions for secure and non-secure applications
- Configurable secure attribute unit (SAU) supporting up to eight memory regions as secure or non-secure
- Floating-point arithmetic functionality with support for single precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex-M33 processor supports the following bus interfaces:

- System AHB bus:

  The system AHB (S-AHB) bus interface is used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, external RAM and external device, or Vendor_SYS regions of the Armv8-M memory map.
- Code AHB bus:

  The code AHB (C-AHB) bus interface is used for any instruction fetch and data access to the code region of the Armv8-M memory map.

Figure 1 shows the general block diagram of the STM32H533xx devices.

3.2 ART Accelerator (ICACHE and DCACHE)

3.2.1 Instruction cache (ICACHE)

The instruction cache (ICACHE) is introduced on C-AHB code bus of Cortex-M33 processor to improve performance when fetching instruction (or data) from both internal and external memories.

ICACHE offers the following features:

- Multi-bus interface:
  - slave port receiving the memory requests from the Cortex-M33 C-AHB code execution port
  - master1 port performing refill requests to internal memories (flash memory and SRAMs)
  - master2 port performing refill requests to external memories (external flash memory and RAMs through Octo-SPI and FMC interfaces)
  - a second slave port dedicated to ICACHE registers access

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- Close to 0 wait-states instructions/data access performance:
  - 0 wait-states on cache hit
  - hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - critical-word-first refill policy, minimizing processor stalls on cache miss
  - hit ratio improved by two-way set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - dual master ports allowing to decouple internal and external memory traffic, respectively, on fast and slow buses, minimizing impact on interrupt latency
  - optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - performance monitoring by means of a hit counter and a miss counter
- Extension of cacheable region beyond the code memory space, by means of address remapping logic that allows four cacheable external regions to be defined
- Power consumption reduced intrinsically (more accesses to cache memory rather to bigger main memories); even improved by configuring ICACHE as direct mapped (rather than the default two-way set-associative mode)
- TrustZone security support
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

3.2.2 Data cache (DCACHE)

The data cache (DCACHE) is introduced on S-AHB system bus of Cortex-M33 processor to improve the performance of data traffic to/from external memories.

DCACHE offers the following features:

- Multi-bus interface:
  - slave port receiving the memory requests from the Cortex-M33 S-AHB system port
  - master port performing refill requests to external memories (external flash memory and RAMs through Octo-SPI and FMC interfaces)
  - a second slave port dedicated to DCACHE registers access
- Close to zero wait-states external data access performance:
  - zero wait-states on cache hit
  - hit-under-miss capability, allowing to serve new processor requests to cached data, while a line refill (due to a previous cache miss) is still ongoing
  - critical-word-first refill policy for read transactions, minimizing processor stalls on cache miss
  - hit ratio improved by two-way set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - performance monitoring by means of two hit counters (for read and write) and two miss counters (for read and write)

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- Supported cache accesses:
  - supports both write-back and write-through policies (selectable with AHB bufferable attribute)
  - read and write-back always allocated
  - write-through always non-allocated (write-around)
  - supports byte, half-word and word writes
- TrustZone security support
- Maintenance operations for software management of cache coherency:
  - full cache invalidation (non interruptible)
  - address range clean and/or invalidate operations (background task, interruptible)
- Error management: detection of error for master port request initiated by DCACHE (line eviction or clean operation), with optional interrupt raising

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by other active tasks. This memory area is organized into up to 20 protected areas (12 secure and 8 non-secure). The MPU regions and registers are banked across secure and non-secure states.

The MPU is especially helpful for applications where critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

If a program accesses a memory location prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

3.4 Embedded flash memory

The devices feature 512 Kbytes of embedded flash memory for storing programs and data. The flash memory supports high-cycle data area of up to 100 K cycles.

The flash memory interface features:

- dual-bank operating modes
- read-while-write (RWW)

This allows a read operation to be performed from one bank while an erase or program operation is performed to the other bank. Each bank contains 32 pages of 8 Kbytes.

The flash memory embeds a 2-Kbyte OTP (one-time programmable) for user data, and up to 96 Kbytes supporting high cycling capability (100 K cycles), to be used for data (EEPROM emulation).

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Option bytes are available to set the flash memory protection mechanisms:

- Different product states for protecting memory content from debug access
- Write protection (WRP) to protect areas against erasing and programming. Two areas per bank can be selected with 8-Kbyte granularity.
- Sector group write-protection (WRPSG), protecting up to 32 groups of four sectors (32 Kbytes) per bank
- Two secure-only areas (one per user flash memory bank). When enabled, this area is accessible only if the STM32 device operates in Secure-access mode
- One HDP area per bank providing temporal isolation for startup code

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single-error detection and correction
- Double-error detection
- ECC fail address report

3.4.1 FLASH security and protections

Sensitive information is stored in the flash memory and it is important to protect the memory against unwanted operations such as reading confidential areas, illegal programming of immutable sectors, or malicious flash memory erasing.

For that purpose FLASH implements the following protection mechanisms:

- TrustZone backed watermark and block security protection
- Temporal isolation protection (HDP)
- Configuration protection
- User flash memory write protection
- Device non-volatile security life cycle and application boot state management
- OTP locking

Refer to the product reference manual for a detailed description of the security mechanisms.

3.4.2 FLASH privilege protection

Each flash memory sector can be programmed on the fly as privileged or unprivileged.

3.5 Embedded SRAMs

Four SRAMs are embedded in the STM32H533xx devices, each with specific features. SRAM1, SRAM2, and SRAM3 are the main SRAMs.

These SRAMs are made of several blocks that can be powered down in Stop mode to reduce consumption:

- SRAM1: 128 Kbytes
- SRAM2: 80 Kbytes with ECC
- SRAM3: 64 Kbytes
- BKPSRAM (backup SRAM): 2 Kbytes with ECC. The BKPSRAM can be retained in all low-power modes and when V_{DD} is off in VBAT mode.

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Note: The ECC is supported by SRAM2, and BKPSRAM when enabled with the SRAM2_ECC, and BKPRAM_ECC user option bits.

3.5.1 SRAMs TrustZone security

When the TrustZone security is enabled, all SRAMs are secure after reset. The SRAM1, SRAM2, SRAM3, can be programmed as secure or non-secure by blocks, using the MPCBB (block-based memory protection controller).

The granularity of SRAM secure block based is a page of 512 bytes. Backup SRAM regions can be programmed as secure or non-secure with watermark, using the TZSC (TrustZone security controller) in the GTZC (global TrustZone controller).

3.5.2 SRAMs privilege protection

The SRAM1, SRAM2, SRAM3, can be programmed as privileged or non-privileged by blocks, using the MPCBB. The granularity of SRAM privilege block based is a page of 512 bytes. Backup SRAM regions can be programmed as privileged or non-privileged with watermark, using the TZSC (TrustZone security controller) in the GTZC (global TrustZone controller).

3.6 Security overview

The STM32H533xx security enables the possibility to reopen the debug mode even if the product is in secure state.

The reopening of the debug mode is controlled with a debug authentication procedure which permits the authentication of the host.

The sensible assets such as keys or secret codes must be protected when opening the debug mode. The protection is made via code protection and hardware keys storage solutions where all *root of trust* can be protected thanks to hardware mechanisms.

In cases where sensitive information cannot be protected, a partial or a full regression can be launched in order to allow a debugging. Regressions are enabled by a debug authentication method.

The STM32H533xx design also permits the developers to introduce their own root of trust solution (OEM-iROT), including their installation in a non-trusted environment thanks to a secure firmware install (SFI) solution.

The STM32H533xx boot stages are isolated via a hardware mechanism called HDPL (temporal isolation level). The HDPL guarantees isolation of the different boot stages: ST assets, iROT (immutable root of trust), uROT (updatable root of trust), secure operating system and non-secure applications.

STM32H533xx devices embed a hardware key storage solution with the following characteristics:

- Feature a dedicated flash memory area per boot stages with access-control based on HDPL and which can be secure or non-secure.
- The keys can be stored encrypted with a derived key related to the current execution context (HDPL, regression counter called EPOCH, secure or non-secure).
- One crypto accelerator hardware DPA resistant (SAES), connected via hardware key bus to a non-DPA protected accelerator.

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STM32H533xx devices are powered by an Arm Cortex-M33 microcontroller, which is associated with all the TrustZone isolation infrastructure. This design permits to benefit from a run time isolation to run secure applications.

3.7 Boot modes

At startup, a BOOT0 pin and NSBOOTADD[31:8]/SECBOOTADD[31:8] option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory
  - Bootloader
  - ST immutable root of trust (ST-iROT)
  - Root security service (RSS)
  - Debug authentication library (RSS-DA)

Embedded bootloader

The embedded bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the flash memory by using USART, I2C, I3C, SPI, FDCAN, or USB in device mode through the DFU (device firmware upgrade).

Refer to AN2606 *STM32 microcontroller system memory boot mode*.

Embedded root security services (RSS)

The embedded RSS are located in the secure information block, programmed by ST during production.

Refer to AN4992 *Overview secure firmware install (SFI)*.

Embedded immutable root of trust (ST-iROT)

The embedded ST-iROT in the system memory, programmed by ST during production. ST-iROT is the immutable root of trust managing the secure boot and secure install of the first updatable level to execute in a boot sequence.

Embedded debug authentication (ST-DA)

The embedded ST-DA in the system memory, programmed by ST during production. ST-DA is the library that manages the debug authentication protocol by allowing to securely reopen the debug or to launch regressions on secured products in the field.

For further information, refer to AN6008 “Getting started with debug authentication (DA) for STM32H5 MCUs”.

3.7.1 STM32H533xx boot modes

Table 3 and *Table 4*, respectively, provide the detail of the boot mode when TrustZone is disabled (TZEN = 0xC3) and enabled (TZEN = 0xB4).

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Table 3. STM32H533xx boot mode when TrustZone is disabled (TZEN = 0xC3)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OP TSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	NA	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	NA	Bootloader	Bootloader
Provisioning	x	NA	NA	RSS	RSS
Provisioned, Closed, Locked	x	NA	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

Table 4. STM32H533xx boot mode when TrustZone is enabled (TZEN = 0xB4)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OP TSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	x	SECBOOTADD [31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
-	1	0xB4	NA	Bootloader	Bootloader
-	1	0xC3	NA	ST-iROT	ST-iROT
Provisioning	x	NA	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	x	0xC3	ST-iROT	ST-iROT	ST-iROT
	x	0xB4	SECBOOTADD [31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

When TrustZone is enabled (TZEN=0xB4), the boot space must be in secure area. The SECBOOTADD0[24:0] option bytes are used to select the boot secure memory address. A unique boot entry option can be selected by setting the SECBOOT_LOCK option bit.

3.8 Global TrustZone controller (GTZC)

GTZC is used to configure TrustZone and privileged attributes within the full system.

The GTZC includes three different sub-blocks:

- TZSC: TrustZone security controller

  This sub-block defines the secure/privilege state of slave/master peripherals. It also controls the non-secure area size for the watermark memory peripheral controller

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(MPCWM). The TZSC block informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.

- TZIC: TrustZone illegal access controller

  This sub-block gathers all security illegal access events in the system and generates a secure interrupt towards NVIC.

- MPCBB: MPCBB: block-based memory protection controller

  This sub-block controls secure states of all memory blocks (512-byte pages) of the associated SRAM. This peripheral aims at configuring the internal RAM in a TrustZone system product having segmented SRAM with programmable-security and privileged attributes.

The GTZC main features are:

- Three independent 32-bit AHB interfaces for TZSC, TZIC and MPCBB
- MPCBB and TZIC accessible only with secure transactions
  - Enable illegal access events that may trigger a secure interrupt
- Secure and non-secure access supported for privileged/non-privileged part of TZSC
- Set of registers to define product security settings:
  - Secure/privilege regions for external memories
  - Secure/privilege access mode for securable peripherals
  - Secure/privilege access mode for securable legacy masters

3.9 TrustZone security architecture

The security architecture is based on Arm TrustZone with the Armv8-M main extension.

The TrustZone security is activated by the TZEN option bit in the FLASH_OPTSR2 register.

When the TrustZone is enabled, the SAU (security attribution unit) and IDAU (implementation defined attribution unit) define the access permissions based on secure and non-secure state.

- SAU: up to eight SAU configurable regions are available for security attribution.
- IDAU: It provides a first memory partition as non-secure or non-secure callable attributes. It is then combined with the results from the SAU security attribution and the higher security state is selected.

Based on IDAU security attribution, the flash memory, system SRAMs and peripherals memory space is aliased twice for secure and non-secure states. However, the external memories space is not aliased.

3.9.1 TrustZone peripheral classification

When the TrustZone security is active, a peripheral can be either securable or TrustZone-aware type as follows:

- securable: peripheral protected by an AHB/APB firewall gate controlled from TZSC to define security properties
- TrustZone-aware: peripheral connected directly to AHB or APB bus and implementing a specific TrustZone behavior such as a subset of registers being secure

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3.9.2 Default TrustZone security state

The default system security state is detailed below:

- CPU:
  - Cortex-M33 is in secure state after reset. The boot address must be in secure address.
- Memory map:
  - SAU is fully secure after reset. Consequently, all memory map is fully secure. Up to eight SAU configurable regions are available for security attribution.
- Flash memory:
  - Flash memory security area is defined by watermark user options.
  - Flash memory block based area is non-secure after reset.
- SRAMs:
  - All SRAMs are secure after reset. MPCBB (memory protection block based controller) is secure.
- External memories:
  - FMC, OCTOSPI banks are secure after reset. MPCWMx (memory protection watermark based controller) is secure.
- Peripherals
  - Securable peripherals are non-secure after reset.
  - TrustZone-aware peripherals are non-secure after reset. Their secure configuration registers are secure.
- All GPIOs are secure after reset.
- Interrupts:
  - NVIC: All interrupts are secure after reset. NVIC is banked for secure and non-secure state.
- TZIC: All illegal access interrupts are disabled after reset.

3.10 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domain (V_{CORE})
  - V_{DD} domain
  - Backup domain (V_{BAT})
  - Analog domain (V_{DDA})
  - VDDIO2 domain
  - VDDUSB for USB transceiver
- System supply voltage regulation
  - Voltage regulator (LDO)
- Power supply supervision
  - POR/PDR monitor
  - BOR monitor
  - PVD monitor

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- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes
- VBAT battery charging
- TrustZone security and privileged protection

3.10.1 Power supply schemes

The devices require a 1.71 to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- V_{DDA} = 1.62 V (ADCs), 1.8 V (DACs), or 2.1 V (VREFBUF) to 3.6 V

  V_{DDA} is the external analog power supply for ADCs, DACs and voltage reference buffer. This voltage level is independent from V_{DD}, and must preferably be connected to V_{DD} when these peripherals are not used.
- V_{DDUSB} = 3.0 V to 3.6 V

  V_{DDUSB} is the external independent power supply for USB transceivers. It is independent from V_{DD}, and must preferably be connected to VDD when the USB is not used.
- V_{DDIO2} = 1.08 V to 3.6 V

  V_{DDIO2} is the external power supply for 10 I/Os (PD6, PD7, PG9:14, PB8, PB9). This voltage level is independent from V_{DD}, voltage and must preferably be connected to VDD when those pins are not used.
- V_{BAT} = 1.2 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  V_{REF+} can be grounded when ADC and DAC are not active.

  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.

  When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled.

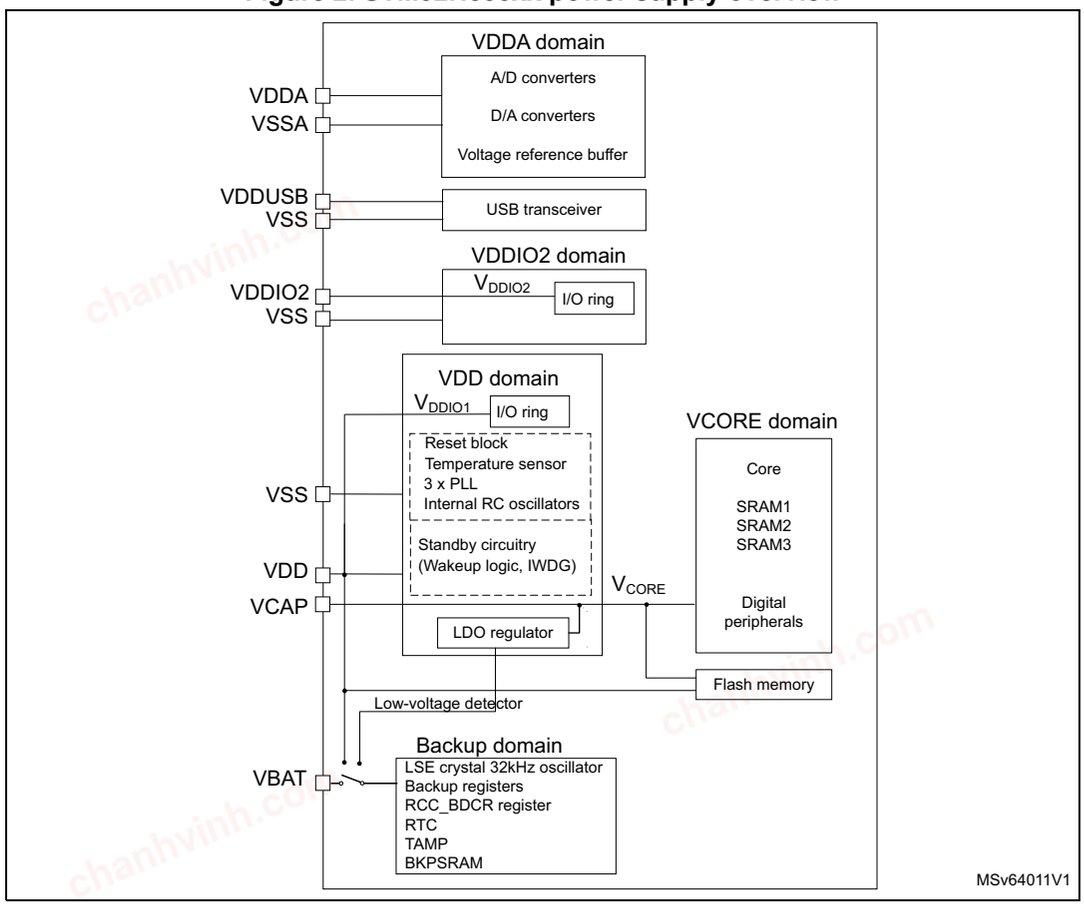
  V_{REF-} must always be equal to V_{SSA}.

The devices embed an LDO regulator to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, SRAM3 and embedded flash memory. The LDO generates this voltage on VCAP pin connected to an external capacitor of 2x 2.2 µF (typical).

This regulator can provide four different voltages (voltage scaling), and can operate in Stop modes.

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Figure 2. STM32H533xx power supply overview

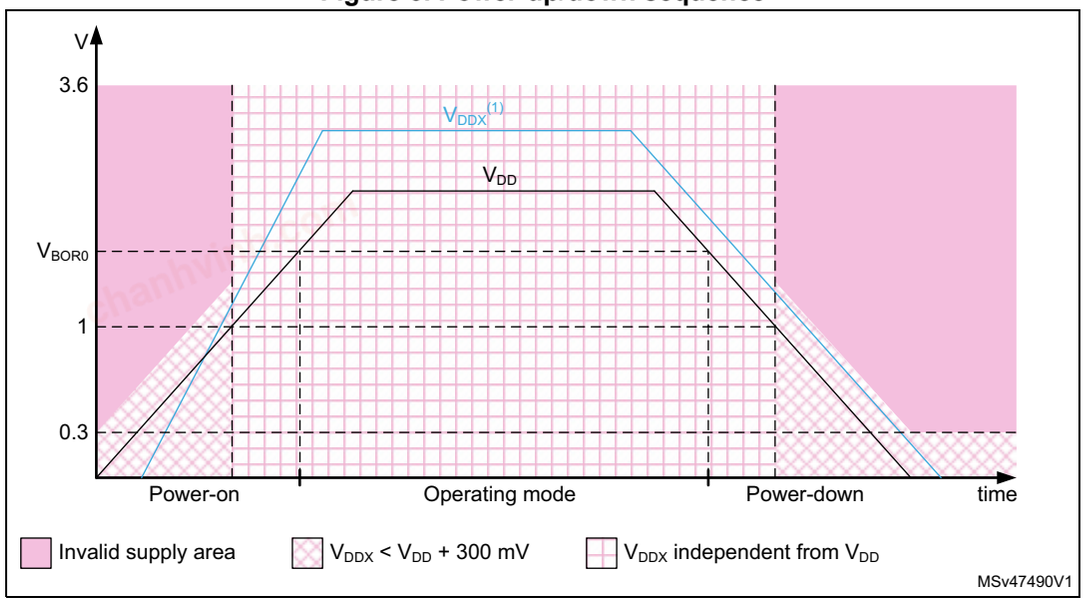


During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

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Figure 3. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDUSB}, and V_{DDIO2}.

3.10.2 Power supply supervisor

The devices have an integrated ultra-low-power brownout reset (BOR) active in all modes; The BOR ensures proper operation of the devices after power on and during power down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold.

An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor that compares the independent supply voltages V_{DDA}, V_{DDUSB} and V_{DDIO2} to ensure that the peripheral is in its functional supply range.

The devices support dynamic voltage scaling to optimize power consumption in Run mode. The voltage from the main regulator that supplies the logic (V_{CORE}) can be adjusted according to the system maximum operating frequency.

The main regulator operates in the following ranges:

- VOS0 (V_{CORE} = 1.35 V) with CPU and peripherals running at up to 250 MHz
- VOS1 (V_{CORE} = 1.2 V) with CPU and peripherals running at up to 200 MHz
- VOS2 (V_{CORE} = 1.1 V) with CPU and peripherals running at up to 150 MHz
- VOS3 (V_{CORE} = 1.0 V) with CPU and peripherals running at up to 100 MHz

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Low-power modes

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the V_{CORE} domain are stopped, the PLL, the CSI, the HSI, the HSI48 and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  The system clock when exiting from Stop mode can be either HSI up to 64 MHz or CSI (4 MHz), depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The PLL, the HSI, the CSI, the HSI48 and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The BOR always remains active in Standby mode.

  The I/Os state during Standby mode can be retained.

  After entering Standby mode, SRAMs and register contents are lost except for registers and backup SRAM in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), an RTC event occurs (alarm, periodic wake-up, timestamp), or a tamper detection. The tamper detection can be raised either due to external pins or due to an internal failure detection.

  The system clock after wake-up is HSI at 32 MHz.

3.10.3 Reset mode

To improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled).

3.10.4 VBAT operation

The VBAT pin allows the device VBAT domain to be powered from an external battery or an external super-capacitor.

The VBAT pin supplies the RTC with LSE, anti-tamper detection (TAMP), backup registers and 2-Kbyte backup SRAM. Eight anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from V_{BAT}, neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.

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3.10.5 PWR TrustZone security

When the TrustZone security is activated by the TZEN option bit, the PWR is switched in TrustZone security mode.

The PWR TrustZone security secures the following configuration:

- Low-power mode
- Wake-up (WKUP) pins
- Voltage detection and monitoring
- VBAT mode

Some of the PWR configuration bits security is defined by the security of other peripherals:

- The voltage scaling (VOS) configuration is secure when the system clock selection is secure in RCC.
- The I/O pull-up/pull-down in Standby mode configuration is secure when the corresponding GPIO is secure.
- The backup domain write protection is secure when the RTC is secure.

3.11 Peripheral interconnect matrix

Several peripherals have direct connections between them, that allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run and Sleep modes.

3.12 Reset and clock controller (RCC)

The clock controller distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- **Clock prescaler:** in order to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Clock security system:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** in order to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 50 MHz high-speed external crystal or ceramic resonator (HSE), can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 64 MHz high-speed internal RC oscillator (HSI), trimmable by software, can supply a PLL.
  - 4 MHz low-power internal oscillator (CSI), trimmable by software, can supply a PLL.
  - System PLL, which can be fed by HSE, HSI or CSI, with a maximum frequency at 250 MHz.

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- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48), can be used to drive the USB.
- **UCPD kernel clock**, derived from HSI clock. The HSI RC oscillator must be enabled prior to the UCPD kernel clock use.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog.
- **Peripheral clock sources:** several peripherals have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, USB, SDMMC, RNG, FDCAN1, OCTOSPI.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 32 MHz clock (HSI/2). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock automatically switches to HSI and a software interrupt is generated if enabled. LSE failure can also be detected and generates an interrupt.
- Clock-out capability:
  - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application.
  - **LSCO (low-speed clock output):** it outputs LSI or LSE in all low-power modes (except VBAT mode).

Several prescalers allow AHB and APB frequencies configuration. The maximum frequency of the AHB and the APB clock domains is 250 MHz.

3.12.1 RCC TrustZone security

When the TrustZone security is activated by the TZEN option bit, the RCC is switched in TrustZone security mode.

The RCC TrustZone security secures some RCC system configuration and peripheral configuration clock from being read or modified by non-secure accesses: when a peripheral is secure, the related peripheral clock, reset, clock source selection and clock enable during low-power modes control bits are secure.

A peripheral is in secure state:

- when its corresponding SEC security bit is set in the TZSC (TrustZone security controller), for securable peripherals.
- when a security feature of this peripheral is enabled through its dedicated bits, for TrustZone-aware peripherals.

3.13 Clock recovery system (CRS)

The devices embed a special block that allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. The trimming is based on the external synchronization signal, derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin, or generated

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by user software. For faster lock-in during startup, automatic and manual trimming actions can be combined.

3.14 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Ten IOs (PD6, PD7, PG9:14, PB8, PB9) can be independently supplied by a dedicated VDDIO supply.

3.14.1 GPIOs TrustZone security

Each I/O pin of GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against a non-secure access. The associated registers bit access is restricted to a secure software only. After reset, all GPIO ports are secure.

3.15 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all the masters (CPU, GPDMA1, GPDMA2, SDMMC1) and the slaves (flash memory, FMC, OCTOSPI, SRAMs, AHB and APB) peripherals. It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

3.16 General purpose direct memory access controller (GPDMA)

The GPDMA controller is a bus master and system peripheral. It used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU. The GPDMA main features are:

- Dual bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Sleep mode
- Transfers arbitration based on a four-grade programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)

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- Per channel event generation, on any of the following events: transfer complete or half transfer complete or data transfer error or user setting error, and/or update linked-list item error or completed suspension
- Per channel interrupt generation, with separately programmed interrupt enable per event
- 8 concurrent DMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intra-channel DMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intra-channel and inter-channel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - 6 channels with linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - Four channels with 2D source and destination addressing: programmable signed address offsets between successive burst transfers (non-contiguous addressing within a block, combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level)
  - Support for scatter-gather (multi-buffer transfers), data interleaving and de-interleaving via 2D addressing
  - Programmable DMA request and trigger selection
  - Programmable DMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting including FIFO level and event flags
- TrustZone support:
  - Support for secure and non-secure DMA transfers, independently at a first channel level, and independently at a source/destination and link sub-levels
  - Secure and non-secure interrupts reporting, resulting from any of the respectively secure and non-secure channels
  - TrustZone-aware AHB slave port, protecting any DMA secure resource (register, register field) from a non-secure access
- Privileged/unprivileged support:
  - Support for privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AHB slave port

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3.17 Interrupts and events

3.17.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels and to handle up to 125 maskable interrupt channels plus the 16 interrupt lines of the Cortex-M33.

The NVIC benefits are the following:

- closely coupled NVIC giving low-latency interrupt processing
- interrupt entry vector table address passed directly to the core
- early processing of interrupts
- processing of late arriving higher priority interrupts
- support for tail chaining
- processor state automatically saved
- interrupt entry restored on interrupt exit with no instruction overhead
- TrustZone support: NVIC registers banked across secure and non-secure states

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.2 Extended interrupt/event controller (EXTI)

The extended interrupts and event controller (EXTI) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run modes. The EXTI also includes the EXTI multiplexer IO port selection.

The EXTI main features are the following:

- All event inputs allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Selectable active trigger edge
  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt and event generation
  - Software trigger possibility
- TrustZone secure events
  - The access to control and configuration bits of secure input events can be made secure
- EXTI IO port selection

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3.18 Cyclic redundancy check calculation unit (CRC)

The CRC is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and that can be stored at a given memory location.

3.19 Flexible memory controller (FMC)

The FMC includes three memory controllers:

- NOR/PSRAM memory controller
- NAND memory controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (four memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
  - Ferroelectric RAM (FRAM)
- 8-,16- bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

3.19.1 LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel® 8080 and Motorola® 6800 modes, and is flexible enough to adapt to specific LCD interfaces.

This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

3.19.2 FMC TrustZone security

When the TrustZone security is enabled, the whole FMC banks are secure after reset. Non-secure area can be configured using the TZSC MPCWMx controller.

- The FMC NOR/PSRAM bank:
  - Up to two non-secure area can be configured thought the TZSC MPCWM2 controller with a 64-Kbyte granularity
- The FMC NAND bank:

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– Can be either configured as fully secure or fully non-secure using the TZSC MPCWM3 controller

The FMC registers can be configured as secure through the TZSC controller.

3.20 Octo-SPI interface (OCTOSPI)

The OCTOSPI supports most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, HyperRAMs™ and HyperFlash™ memories, with the following functional modes:

- Indirect mode: all the operations are performed using the OCTOSPI registers.
- Status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting.
- Memory-mapped mode: the external memory is memory mapped and is seen by the system as if it were an internal memory supporting read and write operation.

The OCTOSPI supports the following protocols with associated frame formats:

- the standard frame format with the command, address, alternate byte, dummy cycles and data phase
- the HyperBus™ frame format

The OCTOSPI offers the following features:

- Three functional modes: Indirect, Status-polling, and Memory-mapped
- Read and write support in Memory-mapped mode
- Supports for single, dual, quad and octal communication
- Dual-quad mode, where eight bits can be sent/received simultaneously by accessing two quad memories in parallel.
- SDR (single-data rate) and DTR (double-transfer rate) support
- Data strobe support
- Fully programmable opcode
- Fully programmable frame format
- HyperBus support
- Integrated FIFO for reception and transmission
- 8-, 16-, and 32-bit data accesses allowed
- DMA channel for Indirect mode operations
- Interrupt generation on FIFO threshold, timeout, operation complete, and access error

3.20.1 OCTOSPI TrustZone security

When the TrustZone security is enabled, the whole OCTOSPI bank is secure after reset.

Up to two non-secure area can be configured thought the TZSC MPCWM1 controller with a granularity of 64 Kbytes.

The OCTOSPI registers can be configured as secure through the TZSC controller.

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3.21 Delay block (DLYB)

The delay block (DLYB) is used to generate an output clock dephased from the input clock. The phase of the output clock must be programmed by the user application. The output clock is then used to clock the data received by another peripheral such as an SDMMC or Octo-SPI interface. The delay is voltage and temperature dependent, that may require the application to re-configure and recenter the output clock phase with the received data.

The delay block main features are:

- Input clock frequency ranging from 25 to 250 MHz
- Up to 12 oversampling phases

3.22 Analog-to-digital converter (ADC1 and ADC2)

The devices embed two successive approximation analog-to-digital converters.

Table 5. ADC features

Mode/feature	ADC1	ADC2
Resolution	12 bit	
Maximum sampling speed	up to 5 Msps (12-bit resolution)	
Dual mode operation	X	
Hardware offset calibration	X	
Hardware linearity calibration	-	
Single-end input	X	
Differential input	X	
Injected channel conversion	X	
Oversampling	Up to x256	
Data register	16 bits	
Data register FIFO depth	3 stages	
DMA support	X	
Parallel data output to ADF	-	
Offset compensation	X	
Gain compensation	-	
Number of analog watchdogs	3	
Option register	X	

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3.22.1 Analog temperature sensor

This sensor generates a voltage (V_{SENSE}) that varies linearly with temperature. It is internally connected to an ADC input channel used to convert the output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect only temperature changes.

To improve the measurement accuracy, each device is individually factory-calibrated by ST. The calibration data are stored in the system memory area, accessible in read-only mode.

3.22.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC. The VREFINT is internally connected to ADC input channel.

The precise voltage of VREFINT is individually measured for each part by STMicroelectronics during production test and stored in the system memory area. It is accessible in read-only mode.

3.22.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using ADC or input channel. As the V_{BAT} voltage may be higher than the V_{DDA}, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by four. As a consequence, the converted digital value is a quarter of the V_{BAT} voltage.

3.23 Digital temperature sensor (DTS)

The devices embeds a sensor that converts the temperature into a square wave, whose frequency is proportional to the temperature. The PCLK or the LSE clock can be used as reference clock for the measurements. Use the formula given in the product reference manual to calculate the temperature according to the measured frequency stored in the DTS_DR register.

3.24 Digital to analog converter (DAC)

The DAC module is a 12-bit, voltage output digital-to-analog converter. The DAC can be configured in 8- or 12-bit mode, and can be used in conjunction with the DMA controller. In 12-bit mode, the data may be left- or right-aligned.

The DAC features two output channels, each with its own converter. In dual DAC channel mode, conversions can be done independently or simultaneously when both channels are grouped together for synchronous update operations. An input reference pin, VREF+ (shared with others analog peripherals) is available for better resolution. An internal reference can also be set on the same input.

The DAC_OUTx pin can be used as general purpose input/output (GPIO) when the DAC output is disconnected from output pad and connected to on chip peripheral. The DAC output buffer can be optionally enabled to allow a high drive output current. An individual

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calibration can be applied on each DAC output channel. The DAC output channels support a low power mode, the Sample and hold mode.

The digital interface supports the following features:

- One DAC interface, maximum two output channels
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave and triangular-wave generation
- Sawtooth wave generation
- Dual DAC channel for independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- Double data DMA capability to reduce the bus activity
- External triggers for conversion
- DAC output channel buffered/unbuffered modes
- Buffer offset calibration
- Each DAC output can be disconnected from the DAC_OUTx output pin
- DAC output connection to on chip peripherals
- Sample and Hold mode for low-power operation in Stop mode. The DAC voltage can be changed autonomously with the DMA while the device is in Stop mode.
- Voltage reference input

3.25 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer that can be used as reference for ADCs and DACs, and also as reference for external components through the VREF+ pin.

The internal voltage reference buffer supports voltages: 1.8 V, 2.048 V and 2.5 V.

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

3.26 Digital camera interface (DCMI)

DCMI is a synchronous parallel interface able to receive a high-speed data flow from an external 8-, 10-, 12- or 14-bit CMOS camera module, supporting YCbCr4:2:2/RGB565 progressive video and compressed data (JPEG) formats. It can be used with black and white cameras, X24 and X5 cameras (it is assumed that all preprocessing such as resizing is performed in the camera module).

Main features:

- 8-, 10-, 12-, or 14-bit parallel interface
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature
- Support of the following data formats:

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- 8/10/12/14-bit progressive video: monochrome or raw Bayer
- YCbCr 4:2:2 progressive video
- RGB 565 progressive video
- Compressed data: JPEG

3.27 Parallel synchronous slave interface (PSSI)

The PSSI peripheral and the DCMI (digital camera interface) use the same circuitry. As a result, these two peripherals cannot be used at the same time: when using the PSSI, the DCMI registers cannot be accessed, and vice versa. In addition, the PSSI and the DCMI share the same alternate functions and the same interrupt vector.

The PSSI is a generic synchronous 8-/16-bit parallel data input/output slave interface. It enables the transmitter to send a data valid signal that indicates when the data is valid, and the receiver to output a flow control signal that indicates when it is ready to sample the data.

The PSSI peripheral main features are the following:

- Slave mode operation
- 8-bit or 16-bit parallel data input or output
- 4-word (16-byte) FIFO
- Data enable (PSSI_DE) alternate function input and ready (PSSI_RDY) alternate function output

When selected, these inputs can either enable the transmitter to indicate when the data is valid, or allow the receiver to indicate when it is ready to sample the data, or both.

3.28 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a non-deterministic random bit generator (NDRBG).

The true random generator:

- delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage
- can be used as entropy source to construct a non-deterministic random bit generator (NDRBG)
- produces four 32-bit random samples every 412 AHB clock cycles if f_{AHB} < 77 MHz (256 RNG clock cycles otherwise)
- embeds start-up and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration)
- has an AMBA AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored)

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3.29 Secure advanced encryption standard hardware accelerator (SAES) and encryption standard hardware accelerator (AES)

The devices embed two AES accelerators: SAES and AES. The SAES with hardware unique key embeds protection against differential power analysis (DPA) and related side channel attacks. The SAES can share its current key register information with the faster AES using a dedicated hardware bus.

The SAES and the AES can be used to both encrypt and decrypt data using the AES algorithm. It is a fully compliant implementation of the advanced encryption standard (AES) as defined by Federal Information Processing Standards Publication (FIPS PUB 197, Nov 2001).

Multiple chaining modes are supported for key sizes of 128 or 256 bits. ECB, CBC, CTR, CCM, GCM and GMAC chaining are supported by the AES and SAES.

SAES and AES support DMA single transfers for incoming and outgoing data (two DMA channels required).

The SAES supports the selection of all the following key sources, while the AES support only the first:

- 256-bit software key, written by the application in the key registers (write only)
- 256-bit derived by hardware secure key management.

The SAES and AES peripherals support:

- Compliant implementation of standard NIST *Special Publication 197, Advanced Encryption Standard (AES)* and *Special Publication 800-38A, Recommendation for Block Cipher Modes of Operation*
- 128-bit data block processing
- Support for cipher keys length of 128-bit and 256-bit
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- 528 or 743 clock cycle latency in ECB encryption mode for SAES processing one 128-bit block of data with, respectively, 128-bit or 256-bit key
- 51 or 75 clock cycle latency in ECB encryption mode for AES processing one 128-bit block of data with, respectively, 128-bit or 256-bit key
- Integrated round key scheduler to compute the last round key for AES ECB/CBC decryption
- 256-bit register for storing the cryptographic key (four 32-bit registers), with key atomicity enforcement
- 128-bit registers for storing initialization vectors (four 32-bit registers)
- One 32-bit INPUT buffer and one 32-bit OUTPUT buffer
- Automatic data flow control with support of single-transfer direct memory access (DMA) using two channels (one for incoming data, one for processed data)

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- Data swapping logic to support 1-, 8-, 16- or 32-bit data
- Possibility for software to suspend a message if the SAES/AES needs to process another message with a higher priority (suspend/resume operation)

Table 6. AES/SAES features

AES/SAES modes/features(1)	AES	SAES
ECB, CBC chaining	X	X
CTR, CCM, GCM chaining	X	X
AES 128-bit ECB encryption in cycles	51	528
DHUK and BHK key selection	-	X
Side-channel attacks resistance	-	X
Shared key between SAES and AES	X	

1. X = supported.

3.30 HASH hardware accelerator (HASH)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-224, SHA-256, SHA-512) and the HMAC (keyed-hash message authentication code) algorithm. HMAC is suitable for applications requiring message authentication.

The HASH computes FIPS (Federal information processing standards) approved digests of length of 160, 224, 256, 512 bits, for messages of up to (2^{64} – 1).

The HASH main features are:

- Suitable for data authentication applications, compliant with:
  - Federal Information Processing Standards Publication FIPS PUB 180-4, *Secure Hash Standard* (SHA-1 and SHA-2 family)
  - Federal Information Processing Standards Publication FIPS PUB 186-4, *Digital* Signature Standard (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, *HMAC: Keyed-Hashing for Message Authentication* and Federal Information Processing Standards Publication FIPS PUB 198-1, *The Keyed-Hash Message* Authentication Code (HMAC)
- Fast computation of SHA-1, SHA-224, SHA-256 and SHA-512
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit string
  - Word swapping supported: bits, bytes, half-words and 32-bit words
- Automatic padding to complete the input bit string to fit digest minimum block size of 512 bits (16 × 32 bits)
- Single 32-bit input register associated to an internal input FIFO of sixteen 32-bit words, corresponding to one block size

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- AHB slave peripheral, accessible through 32-bit word accesses only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H7) for output message digest
- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of 4 supported.
- Interruptible message digest computation, on a per-32-bit word basis
  - Re-loadable digest registers
  - Hashing computation suspend/resume mechanism, including using DMA

3.31 On-the-fly decryption engine (OTFDEC)

The OTFDEC allows the decryption of the on-the-fly AHB traffic based on the read request address information, for example execute-in-place of a code stored encrypted. Four independent and non-overlapping encrypted regions can be defined in OTFDEC.

OTFDEC uses AES-128 in counter mode to achieve the lowest possible latency. As a consequence, each time the content of one encrypted region is changed the entire region must be re-encrypted with a different cryptographic context (key or initialization vector). This constraint makes OTFDEC suitable to decrypt read-only data or code, stored in external NOR flash.

Note: When OTFDEC is used in conjunction with OCTOSPI, it is mandatory to access the flash memory using the Memory-mapped mode of the flash memory controller.

When security is enabled in the product, OTFDEC can be programmed only by a secure host.

The OTFDEC main features are the following:

- On-the-fly 128-bit decryption during OCTOSPI memory-mapped read operations (single or multiple)
  - Use of AES in counter (CTR) mode, with two 128-bit keystream buffers
  - Support for any read size
  - Physical address of the reads is used for the encryption/decryption
- Up to 4 independent encrypted regions
  - Granularity of the region definition: 4096 bytes
  - Region configuration write locking mechanism
  - Each region has its own 128-bit key, two bytes firmware version, and eight bytes application-defined nonce. At least one of those must be changed each time an encryption is performed by the application.
- Encryption keys confidentiality and integrity protection
  - Write-only registers, with software locking mechanism
  - Availability of 8-bit CRC as public key information
- Support for OCTOSPI pre-fetching mechanism
- Possibility to select an enhanced encryption mode to add a proprietary layer of protection on top of AES stream cipher (execute only)
- AMBA® AHB slave peripheral, accessible through 32-bit word single accesses only (otherwise an AHB bus error is generated, and write accesses are ignored)
- Secure only programming if TrustZone security is enabled

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- Encryption mode

3.32 Public key accelerator (PKA)

The PKA is used for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann or ECC (elliptic curve cryptography) over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

The PKA main features are:

- Acceleration of RSA, DH and ECC over GF(p) operations, based on the Montgomery method for fast modular multiplications. More specifically:
  - RSA modular exponentiation, RSA Chinese remainder theorem (CRT) exponentiation
  - ECC scalar multiplication, point on curve check, complete addition, double base ladder, projective to affine
  - ECDSA signature generation and verification
- Capability to handle operands up to 4160 bits for RSA/DH and 640 bits for ECC
- Arithmetic and modular operations such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication
- Built-in Montgomery domain inward and outward transformations
- Protection against differential power analysis (DPA) and related side-channel attacks.

3.33 Timers and watchdogs

The devices include two advanced control timers, up to seven general-purpose timers, two basic timers, six low-power timers, two watchdog timers and two SysTick timers.

Table 7 compares the features of the advanced control, general-purpose and basic timers.

Table 7. Timer features

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16 bits	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM2, TIM5	32 bits				4	No
	TIM3, TIM4	16 bits				4	No
General purpose	TIM12, TIM15	16 bits	Up			2	1
Basic	TIM6, TIM7	16 bits	Up			0	No

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3.33.1 Advanced-control timers (TIM1, TIM8)

These timers can be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 - 100 %)
- One-pulse mode output

In Debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in the next section) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the *Timer Link* feature for synchronization or event chaining.

3.33.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM12, TIM15)

The devices embed up to seven synchronizable general-purpose timers (see *Table 7*), each of them can be used to generate PWM outputs, or act as a simple time base.

- TIM2 and TIM5

  Full-featured general-purpose timers with 32-bit auto-reload up/downcounter and 32-bit prescaler.

  These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.

  The counters can be frozen in Debug mode.

  All have independent DMA request generation and support quadrature encoders.
- TIM3 and TIM4

  Full-featured general-purpose timers with 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output.

  They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.

  The counters can be frozen in Debug mode. All have independent DMA request generation and support quadrature encoders.
- TIM12, and 15

  General-purpose timers with mid-range features.

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM12 and TIM15 have two channels and one complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

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The timers can work together via the *Timer Link* feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in Debug mode.

3.33.3 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebase.

3.33.4 Low-power timers (LPTIM1, LPTIM2)

The devices embed six low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wake up the system from Stop mode.

The low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
  - Internal clock sources: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM input (working with no LP oscillator running, used by *Pulse Counter* application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
  - Update event
  - Input capture

3.33.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and, as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for

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application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in Debug mode.

3.33.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

3.33.7 SysTick timer

The Cortex-M33 with TrustZone embeds two SysTick timers.

When TrustZone is activated, two SysTick timer are available:

- SysTick, secure instance
- SysTick, non-secure instance

When TrustZone is disabled, only one SysTick timer is available. This timer (secure or non-secure) is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.34 Real-time clock (RTC), tamper and backup registers

3.34.1 Real-time clock (RTC)

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in BCD (binary-coded decimal) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period
- TrustZone support:

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  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or non-secure configuration
  - Alarm A, alarm B, wake-up timer and timestamp individual privileged protection

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The RTC clock sources can be one of the following:

- 32.768 kHz external crystal (LSE)
- external resonator or oscillator (LSE)
- internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- high-speed external clock (HSE), divided by a prescaler in the RCC.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes.

3.34.2 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 32-bit backup registers are retained in all low-power modes and in VBAT mode. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with eight tamper pins and nine internal tampers. The external tamper pins can be configured for edge detection, or level detection with or without filtering, or active tamper that increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- A tamper detection can erase the backup registers, backup SRAM, SRAM2, caches and cryptographic peripherals.
- 32 32-bit backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the Backup domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off.
- Up to 8 tamper pins for 8 external tamper detection events:
  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks
  - Flexible active tamper I/O management: from 4 meshes (each input associated to its own exclusive output) to 7 meshes (single output shared for up to 7 tamper inputs)
  - Passive tampers: ultra-low power edge or level detection with internal pull-up hardware management
  - Configurable digital filter

Note: As input, only PC13, PA0, PA1, and PA2 are functional in Standby and VBAT modes. As output, only PC13, and PA1 are functional in Standby and VBAT modes.

- Internal tamper events to protect against transient or environmental perturbation attacks

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- Each tamper can be configured in two modes:
  - Hardware mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Software mode: erase of secrets following a tamper detection launched by software
- Any tamper detection can generate an RTC time stamp event.
- TrustZone support:
  - Tamper secure or non-secure configuration.
  - Backup registers configuration in 3 configurable-size areas:
    - 1 read/write secure area
    - 1 write secure/read non-secure area
    - 1 read/write non-secure area
- Tamper configuration and backup registers privilege protection
- Monotonic counter

3.35 Inter-integrated circuit interface (I2C)

The device embeds three I2C. Refer to *Table 8* for the implemented features.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and Master modes, multimaster capability
  - Standard-mode (Sm), with a bit rate up to 100 Kbit/s
  - Fast-mode (Fm), with a bit rate up to 400 Kbit/s
  - Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7- and 10-bit addressing modes, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C commun.ication speed to be independent from the PCLK reprogramming
- Wake-up from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

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Table 8. I2C implementation

I2C features[1]	I2C1	I2C2	I2C3
Standard-mode (up to 100 Kbit/s)	X	X	X
Fast-mode (up to 400 Kbit/s)	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	X	X	X
Independent clock	X	X	X
Wakeup capability	X	X	X

1. X: supported

3.36 Improved inter-integrated circuit (I3C)

The I3C interface handles communication between the MCU and others, like sensors and host processor(s), all connected on an I3C bus.

The peripheral implements the required features of the MIPI I3C specification v1.1. It can control I3C bus-specific sequencing, protocol, arbitration and timing, and can act as controller (formerly known as master) or as target (formerly known as slave). When acting as controller the peripheral improves the features of the I2C interface, preserving some backward compatibility: it allows an I2C target to operate on an I3C bus in legacy I2C fast-mode (Fm) or legacy I2C fast-mode plus (Fm+), provided that the latter does not perform clock stretching.

The I3C peripheral can be used with DMA to off-load the CPU.

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Table 9. I3C peripheral controller/target features versus MIPI v1.1

Feature	MIPI v1.1	When controller	When target	Comments
I3C SDR message	X	X	X	-
Legacy I^2C message (Fm/Fm+)	X	X	-	Mandatory when controller, and the I3C bus is mixed with (external) legacy I^2C target(s). Optional in MIPI v1.1 when target.
HDR DDR message	X	-	-	Optional in MIPI v1.1
HDR-TSL/TSP, HDR-BT	X	-	-	
Dynamic address assignment	X	X	X	-
Static address	X	X	-	No (intended) support of I3C peripheral as a target on an I^2C bus.
Grouped addressing	X	X	-	Optional in MIPI v1.1
CCCs	X	X	X	Mandatory and some optional CCCs supported.
Error detection and recovery	X	X	X	-
In-band interrupt (with MDB)	X	X	X	-
Secondary controller	X	X	X	-
Hot-join mechanism	X	X	X	-
Target reset	X	X	X	-
Synchronous timing control	X	X	-	Optional in MIPI v1.1
Asynchronous timing control 0	X	X	-	
Asynchronous timing control 1, 2, 3	X	-	-	
Device to device tunneling	X	X	-	
Multi-lane data transfer	X	X	-	
Monitoring device early termination	X	-	-	

3.37 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices have four embedded universal synchronous receiver transmitters (USART1/USART2/USART3/USART6), two universal asynchronous receiver transmitters (UART4/UART5), and one low-power universal asynchronous receiver transmitter (LPUART1).

Table 10. USART, UART and LPUART features

Mode/feature(1)	USART 1/2/3/6	UART 4/5	LPUART 1
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X

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Table 10. USART, UART and LPUART features (continued)

Mode/feature[1]	USART 1/2/3/6	UART 4/5	LPUART 1
Multiprocessor communication	X	X	X
Synchronous mode (master/slave)	X	-	-
Smartcard mode	X	-	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual-clock domain and wake-up from Stop mode	X[2]	X[2]	X[2]
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Auto-baud rate detection	X	X	-
Driver enable	X	X	X
USART data length	7, 8, and 9 bits		
Tx/Rx FIFO	X	X	X
Tx/Rx FIFO size	8 bytes		

1. X = supported.
2. Wake-up supported from Stop mode.

3.37.1 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The USART offers a flexible means to perform full-duplex data exchange with external equipments requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications up to 20 Mbauds are possible by using the DMA (direct memory access) for multibuffer configuration.

The USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or by 8, to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data
  Each FIFO can be enabled/disabled by software and come with a status flag.
- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK

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- Auto baud rate detection
- Programmable data word length (7, 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous Master/Slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from stop capability
- LIN master synchronous break send capability and LIN slave break detection capability
  - 13-bit break generation and 10/11 bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16 bit duration for Normal mode
- Smartcard mode
  - Supports the T=0 and T=1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

3.37.2 Low-power universal asynchronous receiver transmitter (LPUART)

The LPUART supports bidirectional asynchronous serial communication with minimum power consumption. It also supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher-speed clock can be used to reach higher baud-rates.

The LPUART interface can be served by the DMA controller.

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The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data
  Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop capability

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3.38 Serial peripheral interface (SPI) / inter-integrated sound interfaces (I2S)

The devices embed four serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to setup communication with concrete slave and to assure it handles the data flow properly. The Motorola data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4-bit to 32-bit data size selection or fixed to 8-bit and 16-bit only
- Multi master or multi slave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO x MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can secure communication at the end of transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 16x or 8x 8-bit embedded Rx and TxFIFOs with DMA capability
- Programmable number of data in transaction
- Configurable FIFO thresholds (data packing)
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Wake-up from Stop capability
- Optional status pin RDY signalizing the slave device ready to handle the data flow.

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Three standard I2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in Master or Slave mode, in full-duplex communication modes, and can be configured to operate with configurable resolution as input or output channel.

I2S main features:

- Full duplex communication
- Simplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler
- Data length may be 16, 24 or 32 bits
- Channel length can be 16 or 32 in master, any value in slave
- Programmable clock polarity
- Error flags signaling for improved reliability: Underrun, Overrun and Frame Error
- Embedded Rx and TxFIFOs
- Supported I2S protocols:
  - I2S Philips standard
  - MSB-Justified standard (Left-Justified)
  - LSB-Justified standard (Right-Justified)
  - PCM standard (with short and long frame synchronization)
- Data ordering programmable (LSb or MSb first)
- DMA capability for transmission and reception
- Master clock can be output to drive an external audio component. The ratio is fixed at 256 x FWS (where FWS is the audio sampling frequency)

Table 11. SPI features

SPI feature	SPI1, SPI2, SPI3 (full feature set instances)
Data size	Configurable from 4 to 32-bit
CRC computation	CRC polynomial length configurable from 5 to 33-bit
Size of FIFOs	16x 8-bit
Number of transfered data	Unlimited, expandable
I2S feature	Yes

3.39 Secure digital input/output and MultiMediaCards interface (SDMMC)

The SD/SDIO, embedded MultiMediaCard (*e*•MMC™) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and *e*•MMC devices.

The MultiMediaCard system specifications are available through the MultiMediaCard association website at www.mmca.org, published by the MMCA technical committee.

SD memory card and SD I/O card system specifications are available through the SD card Association website at www.sdcard.org.

The SDMMC features include the following:

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- Compliance with Embedded MultiMediaCard System Specification Version 5.1

  Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit

  (HS200 SDMMC_CK speed limited to maximum allowed I/O speed) (HS400 is not supported).
- Full compatibility with previous versions of MultiMediaCards (backward compatibility).
- Full compliance with *SD memory card specifications version 6.0*

  (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Full compliance with *SDIO card specification version 4.0*

  Card support for two different databus modes: 1-bit (default) and 4-bit

  (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Data transfer up to 208 Mbyte/s for the 8-bit mode

  (Depending maximum allowed I/O speed).
- Data and command output enable signals to control external bidirectional drivers
- IDMA linked list support

The MultiMediaCard/SD bus connects cards to the host.

The current version of the SDMMC supports only one SD/SDIO/*e*•MMC card at any one time and a stack of *e*•MMC.

Table 12. SDMMC features

Mode/feature(1)	SDMMC1	SDMMC2
Variable delay (SDR104, HS200)	X	X
SDMMC_CKIN	X	X
SDMMC_CDIR, SDMMC_D0DIR	X	-
SDMMC_D123DIR	X	-

1. X = supported.

3.40 Controller area network (FDCAN)

The controller area network (CAN) subsystem consists of one CAN module, a shared message RAM memory and a configuration block.

The modules (FDCAN) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 0.8-Kbyte message RAM implements filters, receives FIFOs, transmits event FIFOs and transmits FIFOs.

The FDCAN main features are:

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015, -4
- CAN FD with maximum 64 data bytes supported
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering

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- 2 receive FIFOs of three payloads each (up to 64 bytes per payload)
- Separate signaling on reception of high priority messages
- Configurable transmit FIFO / queue of three payload (up to 64 bytes per payload)
- Configurable transmit Event FIFO
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains: APB bus interface and CAN core kernel clock
- Power-down support

3.41 USB full speed (USB)

USB main features

- USB specification version 2.0 full-speed compliant
- Host and device functions
- 2048 bytes of dedicated SRAM data buffer memory with 32-bit access
- USB clock recovery
- Configurable number of endpoints from 1 to 8
- Cyclic redundancy check (CRC) generation/checking, non-return-to-zero inverted (NRZI) encoding/decoding and bit-stuffing
- Isochronous transfers support
- Double-buffered bulk/isochronous endpoint support
- USB suspend/resume operations
- Frame-locked clock pulse generation
- USB 2.0 Link power management support
- Battery charging specification revision 1.2 support in device

3.42 USB Type-C / USB Power Delivery controller (UCPD)

The device embeds one controller (UCPD) compliant with USB Type-C Cable and Connector Specification release 2.0 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB power delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- “Dead battery” support
- USB power delivery message transmission and reception
- FRS (fast role swap) support

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The digital controller handles notably:

- USB Type-C level detection with debounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB power delivery payload, generating interrupts (DMA compatible)
- USB power delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB power delivery messages and FRS signaling.

3.43 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wake up the MCU from Stop mode on data reception.

3.44 Development support

3.44.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.44.2 Embedded Trace Macrocell

The Arm Embedded Trace Macrocell (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

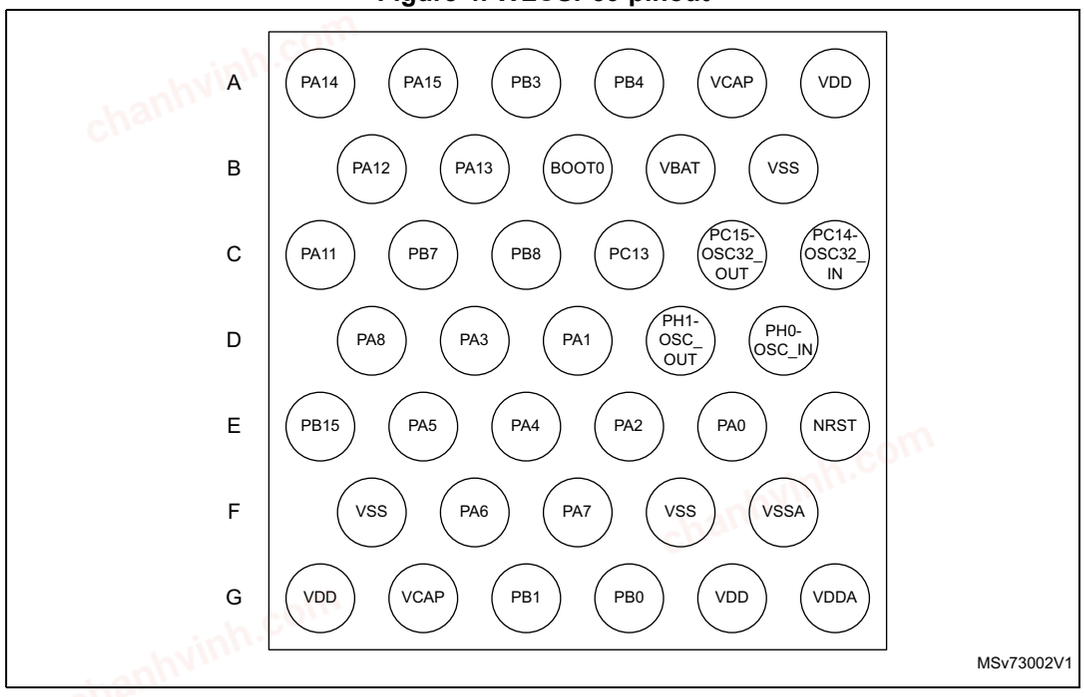
The ETM operates with third party debugger software tools.

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4 Pinout, pin description and alternate function

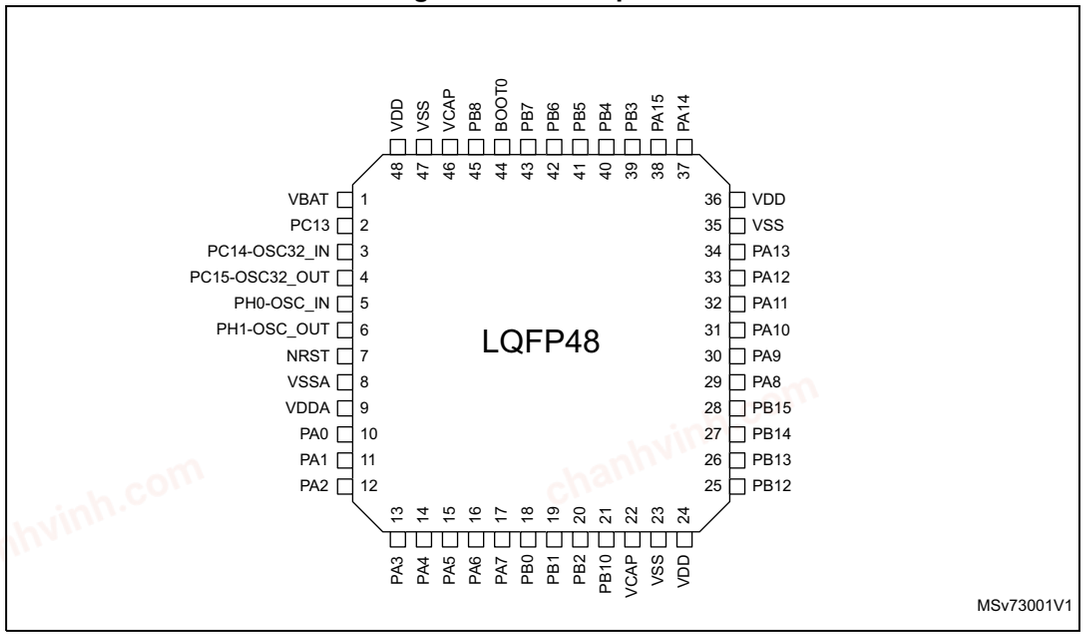
4.1 Pinout/ballout schematics

Figure 4. WLCSP39 pinout



1. The above figure shows the package top view.

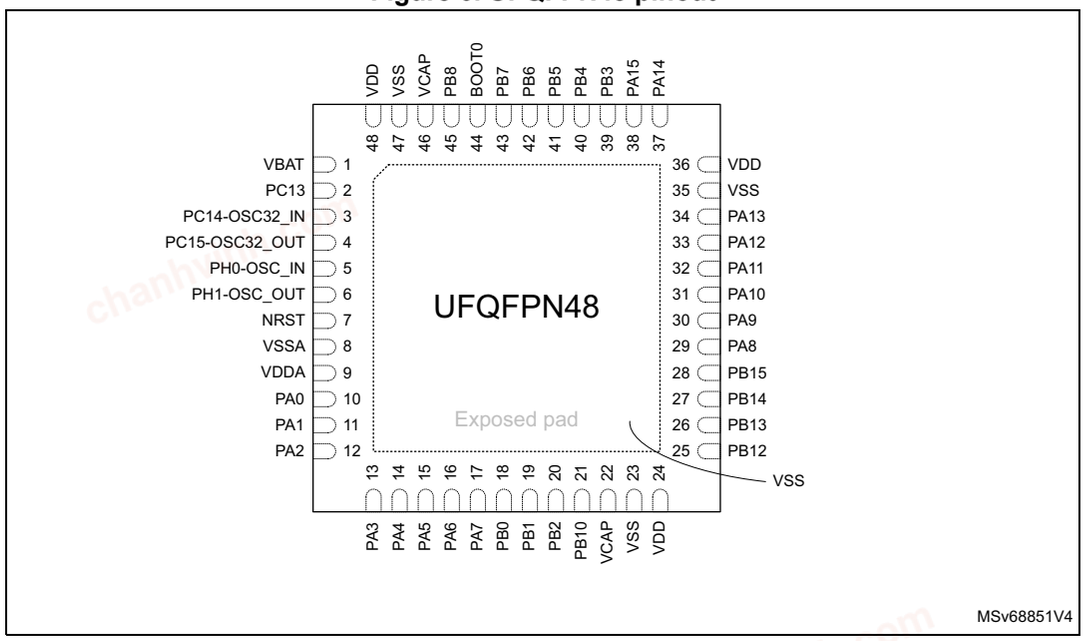
Figure 5. LQFP48 pinout



1. The above figure shows the package top view.

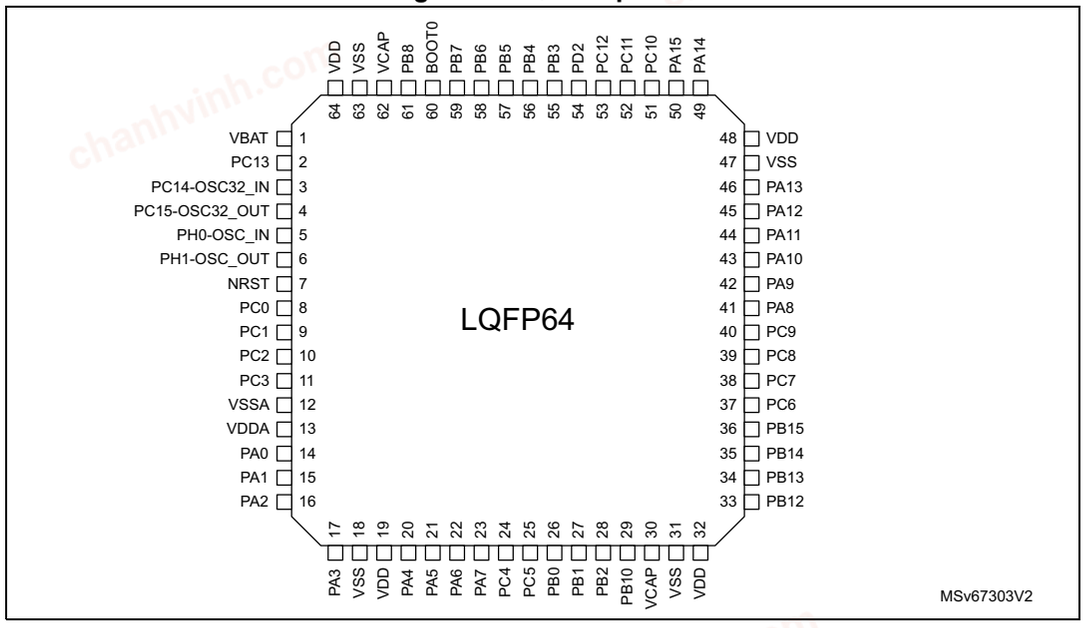
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Figure 6. UFQFPN48 pinout



1. The above figure shows the package top view.

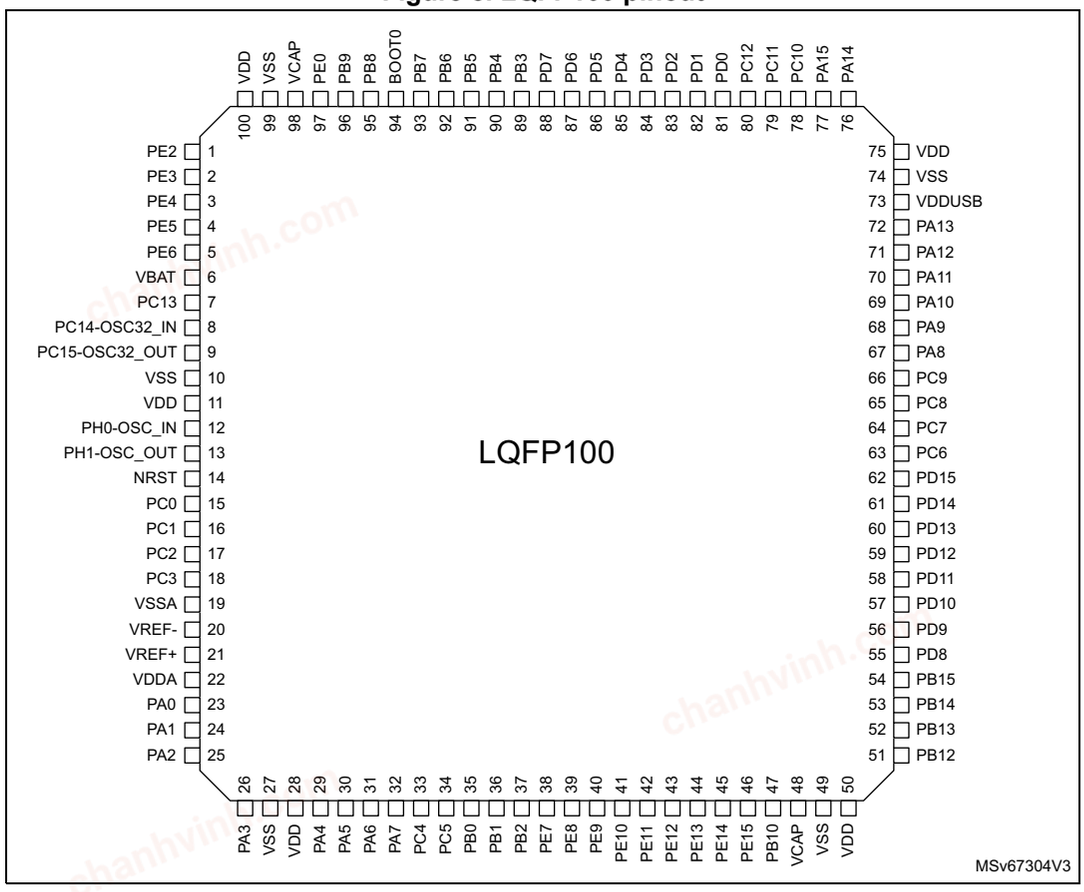
Figure 7. LQFP64 pinout



1. The above figure shows the package top view.

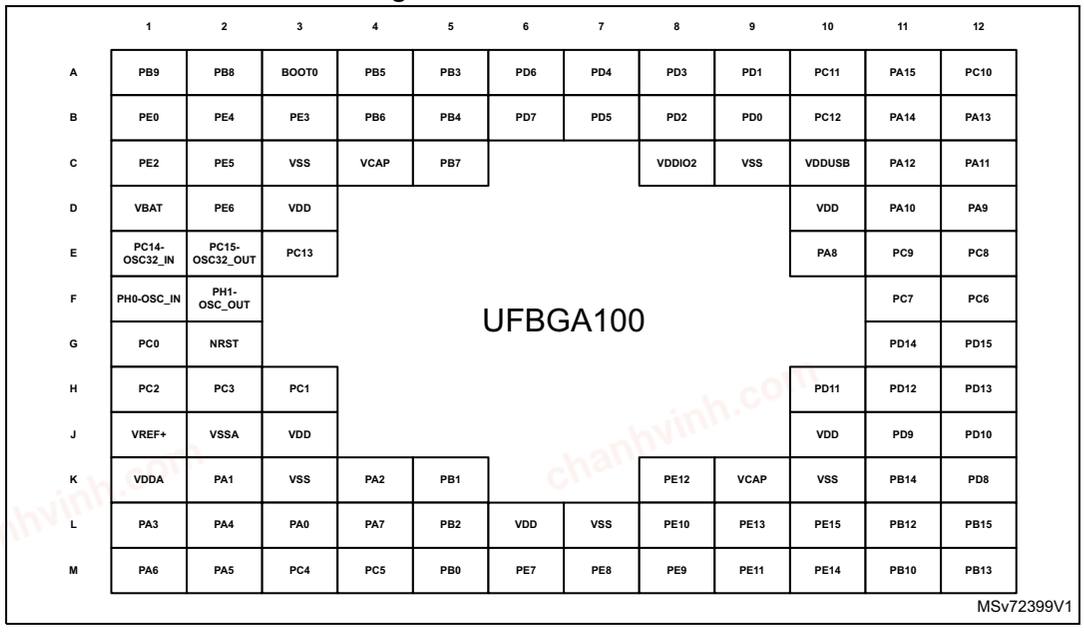
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Figure 8. LQFP100 pinout



1. The above figure shows the package top view.

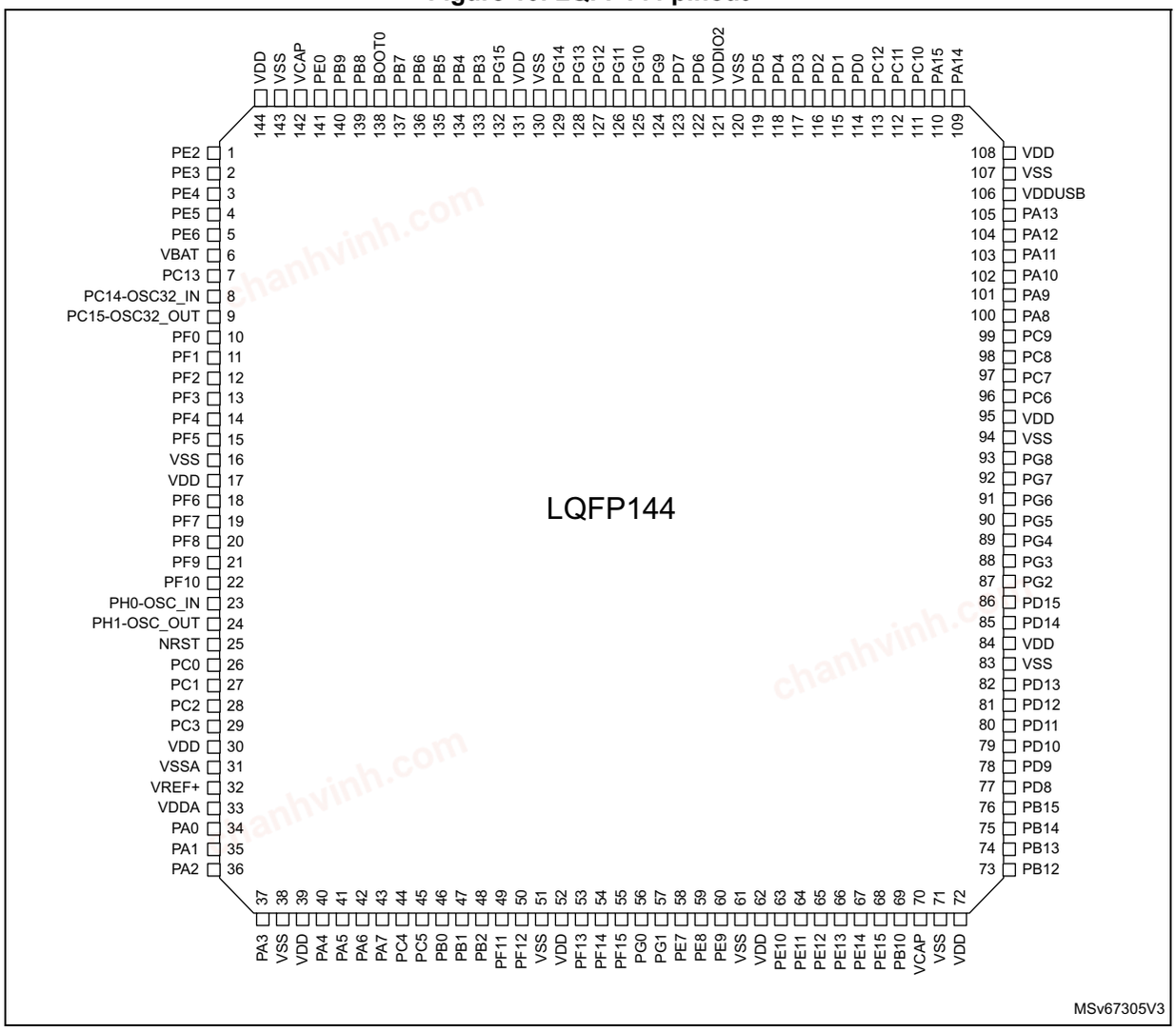
Figure 9. UFBGA100 ballout



1. The above figure shows the package top view.

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Figure 10. LQFP144 pinout



1. The above figure shows the package top view.

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Figure 11. UFBGA144 ballout

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	PB9	PB7	PB4	PG15	PG12	PG11	PD7	PD4	PD2	PC10	VSS
B	PE2	PE0	PB8	PB6	PB3	PG14	PG10	PD6	PD3	PC12	PA14	PA10
C	VBAT	PE4	PE3	BOOT0	VDDIO2	VSS	VDDIO2	PD5	PD1	VDDUSB	PA12	PA11
D	PC15-OSC32_OUT	PC14-OSC32_IN	PE5	VSS	VCAP	PG13	PG9	PD0	PC11	VSS	PA9	PA8
E	PF1	PF0	PC13	PE6	VDD	PB5	VDD	PA15	PA13	PC9	PC8	PC7
F	PF5	PF4	PF3	PF2	VSS	VDD	VSS	VDD	PC6	PG8	PG7	PG6
G	PF6	PF7	PF9	PF8	VDD	VSS	VDD	PD11	PD15	PG3	PG4	PG5
H	PH0-OSC_IN	PH1-OSC_OUT	PF10	VREF-	VSS	VDD	VSS	PB14	PB15	PD12	PD14	PG2
J	NRST	PC0	VREF+	VDDA	PA7	PB1	PG1	VCAP	VSS	PD8	PD9	PD13
K	PC2	PC1	VSSA	PA2	PC4	PB2	PF15	PE9	PE12	PE15	PB13	PD10
L	PC3	PA0	PA1	PA5	PC5	PF11	PF14	PE7	PE10	PE14	PB10	PB12
M	VSS	PA3	PA4	PA6	PB0	PF12	PF13	PG0	PE8	PE11	PE13	M12

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1. The above figure shows the package top view.

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4.2 Pin description

Table 13. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input/output pin
I/O structure		FT	5V-tolerant I/O
		TT	3.6V-tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os(1)	
		_a	I/O, with analog switch function supplied by V_{DDA}
		_c	I/O with USB Type-C power delivery function
		_d	I/O with USB Type-C power delivery dead battery function
		_f	I/O, Fm+ capable
		_h	I/O with high-speed low-voltage mode
		_s	I/O supplied only by V_{DDIO2}
		_t	I/O with tamper function functional in VBAT mode
		_u	I/O, with USB function supplied by V_{DDUSB}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in the table below are a concatenation of various options. Examples: FT_hat, FT_fs, FT_u, TT_a.

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Table 14. STM32H533xx pin/ball definition

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
-	-	-	-	1	C1	1	B1	PE2	I/O	FT_h	-	TRACECLK, LPTIM1_IN2, SPI4_SCK, OCTOSPI1_IO2, FMC_A23, DCMI_D3/PSSI_D3, EVENTOUT	-
-	-	-	-	2	B3	2	C3	PE3	I/O	FT_h	-	TRACED0, TIM15_BKIN, FMC_A19, EVENTOUT	TAMP_IN6/TAMP_OUT3
-	-	-	-	3	B2	3	C2	PE4	I/O	FT_h	-	TRACED1, TIM15_CH1N, SPI4_NSS, FMC_A20, DCMI_D4/PSSI_D4, EVENTOUT	TAMP_IN7/TAMP_OUT8
-	-	-	-	4	C2	4	D3	PE5	I/O	FT_h	-	TRACED2, TIM15_CH1, SPI4_MISO, FMC_A21, DCMI_D6/PSSI_D6, EVENTOUT	TAMP_IN8/TAMP_OUT7
-	-	-	-	5	D2	5	E4	PE6	I/O	FT_h	-	TRACED3, TIM1_BKIN2, TIM15_CH2, SPI4_MOSI, FMC_A22, DCMI_D7/PSSI_D7, EVENTOUT	TAMP_IN3/TAMP_OUT6
-	-	-	-	-	D3	-	E5	VDD	S	-	-	-	-
-	-	-	-	-	C3	-	A1	VSS	S	-	-	-	-
B8	1	1	1	6	D1	6	C1	VBAT	S	-	-	-	-
-	-	-	-	-	C9	-	A12	VSS	S	-	-	-	-
C7	2	2	2	7	E3	7	E3	PC13	I/O	FT_t	(4)	EVENTOUT	TAMP_IN1/TAMP_OUT2/TAMP_OUT3, RTC_OUT1/RTC_TS, WKUP4
-	-	-	-	-	K3	-	C6	VSS	S	-	-	-	-
C11	3	3	3	8	E1	8	D2	PC14-OSC32_IN (OSC32_IN)	I/O	FT	-	EVENTOUT	OSC32_IN

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
C9	4	4	4	9	E2	9	D1	PC15-OSC32_OUT (OSC32_OUT)	I/O	FT	-	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	10	E2	PF0	I/O	FT_f	-	I3C2_SDA, I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	-	-	-	-	11	E1	PF1	I/O	FT_f	-	I3C2_SCL, I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	-	-	-	-	12	F4	PF2	I/O	FT_h	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	-	-	13	F3	PF3	I/O	FT_h	-	FMC_A3, EVENTOUT	-
-	-	-	-	-	-	14	F2	PF4	I/O	FT_h	-	FMC_A4, EVENTOUT	-
-	-	-	-	-	-	15	F1	PF5	I/O	FT_h	-	I3C1_SCL, FMC_A5, EVENTOUT	-
-	-	-	-	10	K10	16	D4	VSS	S	-	-	-	-
-	-	-	-	11	D10	17	E7	VDD	S	-	-	-	-
-	-	-	-	-	-	18	G1	PF6	I/O	FT_h	-	OCTOSPI1_IO3, EVENTOUT	-
-	-	-	-	-	-	19	G2	PF7	I/O	FT_h	-	OCTOSPI1_IO2, EVENTOUT	-
-	-	-	-	-	-	20	G4	PF8	I/O	FT_h	-	OCTOSPI1_IO0, EVENTOUT	-
-	-	-	-	-	-	21	G3	PF9	I/O	FT_h	-	OCTOSPI1_IO1, EVENTOUT	-
-	-	-	-	-	-	22	H3	PF10	I/O	FT_h	-	PSSI_D15, OCTOSPI1_CLK, DCMI_D11/PSSI_D11, EVENTOUT	-
D10	5	5	5	12	F1	23	H1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
D8	6	6	6	13	F2	24	H2	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
E11	7	7	7	14	G2	25	J1	NRST	I/O	RST	-	-	-
-	-	-	8	15	G1	26	J2	PC0	I/O	FT_a	-	SPI4_MISO, SPI2_RDY, FMC_A25, OCTOSPI1_IO7, EVENTOUT	ADC12_INP10
-	-	-	9	16	H3	27	K2	PC1	I/O	FT_ah	-	TRACED0, SPI2_MOSI/I2S2_SDO, SPI4_MOSI, OCTOSPI1_IO4, EVENTOUT	ADC12_INP11, ADC12_INN10, TAMP_IN3/TAMP_OUT5, WKUP6
-	-	-	10	17	H1	28	K1	PC2	I/O	FT_a	-	PWR_CSLEEP, TIM4_CH4, SPI2_MISO/I2S2_SDI, OCTOSPI1_IO5, OCTOSPI1_IO2, EVENTOUT	ADC12_INP12, ADC12_INN11
-	-	-	11	18	H2	29	L1	PC3	I/O	FT_a	-	PWR_CSTOP, LPUART1_TX, SPI2_MOSI/I2S2_SDO, OCTOSPI1_IO6, OCTOSPI1_IO0, EVENTOUT	ADC12_INP13, ADC12_INN12
-	-	-	-	-	J3	30	F6	VDD	S	-	-	-	-
-	-	-	-	-	L7	-	D10	VSS	S	-	-	-	-
F10	8	8	12	19	J2	31	K3	VSSA	S	-	-	-	-
-	-	-	-	20	-	-	H4	VREF-	S	-	-	-	-
-	-	-	-	21	J1	32	J3	VREF+	S	-	-	-	-
G11	9	9	13	22	K1	33	J4	VDDA	S	-	-	-	-
E9	10	10	14	23	L3	34	L2	PA0	I/O	FT_at	(4)	TIM2_CH1, TIM5_CH1, TIM8_ETR, TIM15_BKIN, SPI4_SCK, SPI3_RDY, USART2_CTS/USART2_NSS, UART4_TX, FDCAN2_RX, TIM2_ETR, EVENTOUT	ADC12_INP0, ADC12_INN1, TAMP_IN2/TAMP_OUT1, WKUP1

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
D6	11	11	15	24	K2	35	L3	PA1	I/O	FT_aht	(4)	TIM2_CH2, TIM5_CH2, TIM15_CH1N, LPTIM1_IN1, OCTOSPI1_DQS, USART2_RTS, UART4_RX, OCTOSPI1_IO3, USART6_CK, EVENTOUT	ADC12_INP1, TAMP_IN5/TAMP_OUT4
E7	12	12	16	25	K4	36	K4	PA2	I/O	FT_at	(4)	TIM2_CH3, TIM5_CH3, LPUART1_TX, TIM15_CH1, LPTIM1_IN2, USART2_TX, EVENTOUT	ADC12_INP14, TAMP_IN4/TAMP_OUT3, WKUP2
D4	13	13	17	26	L1	37	M2	PA3	I/O	FT_ah	-	TIM2_CH4, TIM5_CH4, OCTOSPI1_CLK, TIM15_CH2, SPI2_NSS/I2S2_WS, SPI3_MOSI/I2S3_SDO, USART2_RX, EVENTOUT	ADC12_INP15
B10	-	-	18	27	-	38	F5	VSS	S	-	-	-	-
A11	-	-	19	28	J10	39	F8	VDD	S	-	-	-	-
E5	14	14	20	29	L2	40	M3	PA4	I/O	TT_a	-	TIM5_ETR, LPTIM2_CH1, SPI3_MOSI/I2S3_SDO, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, DCMI_HSYNC/PSSI_DE, EVENTOUT	ADC12_INP18, DAC1_OUT1
E3	15	15	21	30	M2	41	L4	PA5	I/O	TT_ah	-	TIM2_CH1, TIM8_CH1N, SPI1_SCK/I2S1_CK, PSSI_D14, TIM2_ETR, EVENTOUT	ADC12_INP19, ADC12_INN18, DAC1_OUT2
F4	16	16	22	31	M1	42	M4	PA6	I/O	FT_ah	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, OCTOSPI1_IO3, DCMI_PIXCLK/PSSI_PDCK, EVENTOUT	ADC12_INP3

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
F6	17	17	23	32	L4	43	J5	PA7	I/O	FT_ah	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SDO, OCTOSPI1_IO2, FMC_NWE, EVENTOUT	ADC12_INP7, ADC12_INN3
-	-	-	24	33	M3	44	K5	PC4	I/O	FT_a	-	TIM2_CH4, LPTIM2_ETR, I2S1_MCK, USART3_RX, EVENTOUT	ADC12_INP4
-	-	-	25	34	M4	45	L5	PC5	I/O	FT_ah	-	TIM1_CH4N, PSSI_D15, SPI4_SCK, OCTOSPI1_DQS, EVENTOUT	ADC12_INP8, ADC12_INN4
-	-	-	-	-	L6	-	G5	VDD	S	-	-	-	-
-	-	-	-	-	-	-	F7	VSS	S	-	-	-	-
G7	18	18	26	35	M5	46	M5	PB0	I/O	FT_ah	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI3_MISO/I2S3_SDI, OCTOSPI1_IO1, USART2_TX, UART4_CTS, EVENTOUT	ADC12_INP9, ADC12_INN5
G5	19	19	27	36	K5	47	J6	PB1	I/O	FT_ah	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, SPI3_SCK, SPI2_NSS/I2S2_WS, OCTOSPI1_IO0, USART3_RX, EVENTOUT	ADC12_INP5
-	20	20	28	37	L5	48	K6	PB2	I/O	FT_ah	-	RTC_OUT2, TIM8_CH4N, SPI1_RDY, LPTIM1_CH1, SPI2_SCK/I2S2_CK, SPI3_MOSI/I2S3_SDO, OCTOSPI1_CLK, OCTOSPI1_DQS, SDMMC1_CMD, EVENTOUT	LSCO
-	-	-	-	-	-	49	L6	PF11	I/O	FT_ah	-	OCTOSPI1_NCLK, DCMI_D12/PSSI_D12, EVENTOUT	ADC1_INP2
-	-	-	-	-	-	50	M6	PF12	I/O	FT_ah	-	FMC_A6, EVENTOUT	ADC1_INP6, ADC1_INN2
-	-	-	-	-	-	51	G6	VSS	S	-	-	-	-
-	-	-	-	-	-	52	G7	VDD	S	-	-	-	-
-	-	-	-	-	-	53	M7	PF13	I/O	FT_ah	-	FMC_A7, EVENTOUT	ADC2_INP2

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
-	-	-	-	-	-	54	L7	PF14	I/O	FT_fah	-	FMC_A8, EVENTOUT	ADC2_INP6, ADC2_INN2
-	-	-	-	-	-	55	K7	PF15	I/O	FT_fh	-	I3C1_SDA, FMC_A9, EVENTOUT	-
-	-	-	-	-	-	56	M8	PG0	I/O	FT_h	-	FMC_A10, EVENTOUT	-
-	-	-	-	-	-	-	H5	VSS	S	-	-	-	-
-	-	-	-	-	-	-	H6	VDD	S	-	-	-	-
-	-	-	-	-	-	57	J7	PG1	I/O	FT_h	-	SPI2_MOSI/I2S2_SDO, FMC_A11, EVENTOUT	-
-	-	-	-	38	M6	58	L8	PE7	I/O	FT_ah	-	TIM1_ETR, OCTOSPI1_IO4, FMC_D4/FMC_AD4, EVENTOUT	-
-	-	-	-	39	M7	59	M9	PE8	I/O	FT_ah	-	TIM1_CH1N, OCTOSPI1_IO5, FMC_D5/FMC_AD5, EVENTOUT	-
-	-	-	-	40	M8	60	K8	PE9	I/O	FT_ah	-	TIM1_CH1, OCTOSPI1_IO6, FMC_D6/FMC_AD6, EVENTOUT	-
-	-	-	-	-	-	61	H7	VSS	S	-	-	-	-
-	-	-	-	-	-	62	-	VDD	S	-	-	-	-
-	-	-	-	41	L8	63	L9	PE10	I/O	FT_ah	-	TIM1_CH2N, OCTOSPI1_IO7, FMC_D7/FMC_AD7, EVENTOUT	-
-	-	-	-	42	M9	64	M10	PE11	I/O	FT_ah	-	TIM1_CH2, SPI1_RDY, SPI4_NSS, OCTOSPI1_NCS, FMC_D8/FMC_AD8, EVENTOUT	-
-	-	-	-	43	K8	65	K9	PE12	I/O	FT_h	-	TIM1_CH3N, SPI4_SCK, FMC_D9/FMC_AD9, EVENTOUT	-
-	-	-	-	44	L9	66	M11	PE13	I/O	FT_h	-	TIM1_CH3, SPI4_MISO, FMC_D10/FMC_AD10, EVENTOUT	-

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
-	-	-	-	45	M10	67	L10	PE14	I/O	FT_h	-	TIM1_CH4, SPI4_MOSI, FMC_D11/FMC_AD11, EVENTOUT	-
-	-	-	-	46	L10	68	K10	PE15	I/O	FT_h	-	TIM1_BKIN, TIM1_CH4N, FMC_D12/FMC_AD12, EVENTOUT	-
-	21	21	29	47	M11	69	L11	PB10	I/O	FT_f	-	TIM2_CH3, TIM8_CH1, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OCTOSPI1_NCS, EVENTOUT	-
G3	22	22	30	48	K9	70	J8	VCAP	S	-	-	-	-
F8	23	23	31	49	-	71	J9	VSS	S	-	-	-	-
G9	24	24	32	50	-	72	-	VDD	S	-	-	-	-
-	25	25	33	51	L11	73	L12	PB12	I/O	FT_h	-	TIM1_BKIN, TIM8_CH3, OCTOSPI1_NCLK, I2C2_SDA, SPI2_NSS/I2S2_WS, UCPD1_FRSTX, USART3_CK, FDCAN2_RX, UART5_RX, EVENTOUT	-
-	26	26	34	52	M12	74	K11	PB13	I/O	FT_c	-	TIM1_CH1N, TIM8_CH2, LPTIM2_CH1, I2C2_SMBA, SPI2_SCK/I2S2_CK, USART3_CTS/USART3_NSS, LPUART1_RX, FDCAN2_TX, SDMMC1_D0, UART5_TX, EVENTOUT	UCPD1_CC1
-	27	27	35	53	K11	75	H8	PB14	I/O	FT_c	-	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, USART3_RTS, UART4_RTS, EVENTOUT	UCPD1_CC2

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
E1	28	28	36	54	L12	76	H9	PB15	I/O	FT_h	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, SPI1_MOSI/I2S1_SDO, UART4_CTS, OCTOSPI1_CLK, DCMI_D2/PSSI_D2, UART5_RX, EVENTOUT	PVD_IN
-	-	-	-	55	K12	77	J10	PD8	I/O	FT_h	-	USART3_TX, FMC_D13/FMC_AD13, EVENTOUT	-
-	-	-	-	56	J11	78	J11	PD9	I/O	FT_h	-	USART3_RX, FDCAN2_RX, FMC_D14/FMC_AD14, EVENTOUT	-
-	-	-	-	57	J12	79	K12	PD10	I/O	FT_h	-	LPTIM2_CH2, USART3_CK, FMC_D15/FMC_AD15, EVENTOUT	-
-	-	-	-	58	H10	80	G8	PD11	I/O	FT_h	-	LPTIM2_IN2, USART3_CTS/USART3_NSS, UART4_RX, OCTOSPI1_IO0, FMC_A16/FMC_CLE, EVENTOUT	-
-	-	-	-	59	H11	81	H10	PD12	I/O	FT_fh	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I3C1_SCL, USART3_RTS, UART4_TX, OCTOSPI1_IO1, FMC_A17/FMC_ALE, DCMI_D12/PSSI_D12, EVENTOUT	-
-	-	-	-	60	H12	82	J12	PD13	I/O	FT_fh	-	LPTIM1_CH1, TIM4_CH2, LPTIM2_CH1, I3C1_SDA, OCTOSPI1_IO3, FMC_A18, DCMI_D13/PSSI_D13, EVENTOUT	-
-	-	-	-	-	-	83	M1	VSS	S	-	-	-	-
-	-	-	-	-	-	84	-	VDD	S	-	-	-	-
-	-	-	-	61	G11	85	H11	PD14	I/O	FT_h	-	TIM4_CH3, FMC_D0/FMC_AD0, EVENTOUT	-

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
-	-	-	-	62	G12	86	G9	PD15	I/O	FT_h	-	TIM4_CH4, FMC_D1/FMC_AD1, EVENTOUT	-
-	-	-	-	-	-	87	H12	PG2	I/O	FT_h	-	TIM8_BKIN, FMC_A12, EVENTOUT	-
-	-	-	-	-	-	88	G10	PG3	I/O	FT_h	-	TIM8_BKIN2, FMC_A13, EVENTOUT	-
-	-	-	-	-	-	89	G11	PG4	I/O	FT_h	-	TIM1_BKIN2, FMC_A14, EVENTOUT	-
-	-	-	-	-	-	90	G12	PG5	I/O	FT_h	-	TIM1_ETR, FMC_A15, EVENTOUT	-
-	-	-	-	-	-	91	F12	PG6	I/O	FT_h	-	I3C1_SDA, SPI1_RDY, OCTOSPI1_NCS, UCPD1_FRSTX, FMC_NE3, DCMI_D12/PSSI_D12, EVENTOUT	-
-	-	-	-	-	-	92	F11	PG7	I/O	FT_h	-	I3C1_SCL, USART6_CK, UCPD1_FRSTX, FMC_INT, DCMI_D13/PSSI_D13, EVENTOUT	-
-	-	-	-	-	-	93	F10	PG8	I/O	FT_h	-	TIM8_ETR, SPI3_MOSI/I2S3_SDO, USART6_RTS, EVENTOUT	-
-	-	-	-	-	-	94	-	VSS	S	-	-	-	-
-	-	-	-	-	-	95	-	VDD	S	-	-	-	-
-	-	-	37	63	F12	96	F9	PC6	I/O	FT_h	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, FMC_NWAIT, I3C2_SCL, OCTOSPI1_IO5, SDMMC1_D6, DCMI_D0/PSSI_D0, EVENTOUT	-
-	-	-	38	64	F11	97	E12	PC7	I/O	FT_h	-	TRGIO, TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, FMC_NE1, I3C2_SDA, OCTOSPI1_IO6, SDMMC1_D7, DCMI_D1/PSSI_D1, EVENTOUT	-

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
-	-	-	39	65	E12	98	E11	PC8	I/O	FT_h	-	TRACED1, TIM3_CH3, TIM8_CH3, USART6_CK, UART5_RTS, FMC_NE2/FMC_NCE, FMC_INT, FMC_ALE, SDMMC1_D0, DCMI_D2/PSSI_D2, EVENTOUT	-
-	-	-	40	66	E11	99	E10	PC9	I/O	FT_fh	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, AUDIOCLK, UART5_CTS, OCTOSPI1_IO0, FMC_CLE, SDMMC1_D1, DCMI_D3/PSSI_D3, EVENTOUT	UCPD1_DB2
D2	29	29	41	67	E10	100	D12	PA8	I/O	FT_fh	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, SPI1_RDY, SPI4_MOSI, USART1_CK, I3C2_SCL, USB_SOF, FMC_NOE, DCMI_D3/PSSI_D3, EVENTOUT	-
-	30	30	42	68	D12	101	D11	PA9	I/O	FT_h	-	TIM1_CH2, LPUART1_TX, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, FMC_NWE, DCMI_D0/PSSI_D0, EVENTOUT	UCPD1_DB1
-	31	31	43	69	D11	102	B12	PA10	I/O	FT_h	-	TIM1_CH3, LPUART1_RX, LPTIM2_IN2, UCPD1_FRSTX, USART1_RX, FDCAN2_TX, SDMMC1_D0, DCMI_D1/PSSI_D1, EVENTOUT	-
C1	32	32	44	70	C12	103	C12	PA11	I/O	FT_u	-	TIM1_CH4, LPUART1_CTS, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS/USART1_NSS, FDCAN1_RX, USB_DM, EVENTOUT	-

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
B2	33	33	45	71	C11	104	C11	PA12	I/O	FT_u	-	TIM1_ETR, LPUART1_RTS, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, FDCAN1_TX, USB_DP, EVENTOUT	-
B4	34	34	46	72	B12	105	E9	PA13(JTMS/SWDIO)	I/O	FT	(5)	JTMS/SWDIO, EVENTOUT	-
-	-	-	-	73	C10	106	C10	VDDUSB	S	-	-	-	-
F2	35	35	47	74	-	107	-	VSS	S	-	-	-	-
G1	36	36	48	75	-	108	-	VDD	S	-	-	-	-
A1	37	37	49	76	B11	109	B11	PA14(JTCK/SWCLK)	I/O	FT	-	JTCK/SWCLK, EVENTOUT	-
A3	38	38	50	77	A11	110	E8	PA15 (JTDI)	I/O	FT	(5)	JTDI, TIM2_CH1, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART1_TX, UART4_RTS, OCTOSPI1_NCS, FMC_NBL1, DCMI_D11/PSSI_D11, TIM2_ETR, EVENTOUT	-
-	-	-	51	78	A12	111	A11	PC10	I/O	FT_h	-	I3C2_SCL, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, OCTOSPI1_IO1, SDMMC1_D2, DCMI_D8/PSSI_D8, EVENTOUT	-
-	-	-	52	79	A10	112	D9	PC11	I/O	FT_h	-	I3C2_SDA, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, OCTOSPI1_NCS, SDMMC1_D3, DCMI_D4/PSSI_D4, EVENTOUT	-
-	-	-	53	80	B10	113	B10	PC12	I/O	FT_h	-	TRACED3, TIM15_CH1, LPTIM2_CH2, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9/PSSI_D9, EVENTOUT	-

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
-	-	-	-	81	B9	114	D8	PD0	I/O	FT_h	-	TIM8_CH4N, UART4_RX, FDCAN1_RX, FMC_D2/FMC_AD2, EVENTOUT	-
-	-	-	-	82	A9	115	C9	PD1	I/O	FT_h	-	UART4_TX, FDCAN1_TX, FMC_D3/FMC_AD3, EVENTOUT	-
-	-	-	54	83	B8	116	A10	PD2	I/O	FT_h	-	TRACED2, TIM3_ETR, TIM15_BKIN, UART5_RX, SDMMC1_CMD, DCMI_D11/PSSI_D11, EVENTOUT	WKUP7
-	-	-	-	84	A8	117	B9	PD3	I/O	FT_h	-	SPI2_SCK/I2S2_CK, USART2_CTS/USART2_NSS, FMC_CLK, DCMI_D5/PSSI_D5, EVENTOUT	WKUP8
-	-	-	-	85	A7	118	A9	PD4	I/O	FT_h	-	USART2_RTS, OCTOSPI1_IO4, FMC_NOE, EVENTOUT	-
-	-	-	-	86	B7	119	C8	PD5	I/O	FT_h	-	TIM1_CH4N, SPI2_RDY, USART2_TX, FDCAN1_TX, OCTOSPI1_IO5, FMC_NWE, EVENTOUT	-
-	-	-	-	-	-	120	-	VSS	S	-	-	-	-
-	-	-	-	-	C8	121	C5	VDDIO2	S	-	-	-	-
-	-	-	-	87	A6	122	B8	PD6	I/O	FT_sh	-	I3C2_SCL, I2C3_SCL, SPI3_MOSI/I2S3_SDO, USART2_RX, OCTOSPI1_IO6, SDMMC1_CK, FMC_NWAIT, DCMI_D10/PSSI_D10, EVENTOUT	-
-	-	-	-	88	B6	123	A8	PD7	I/O	FT_sh	-	I3C2_SDA, I2C3_SDA, SPI1_MOSI/I2S1_SDO, SPI3_MISO/I2S3_SDI, USART2_CK, OCTOSPI1_IO7, SDMMC1_CMD, FMC_NE1/FMC_NCE, EVENTOUT	-

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
-	-	-	-	-	-	124	D7	PG9	I/O	FT_sh	-	SPI1_MISO/I2S1_SDI, USART6_RX, OCTOSPI1_IO6, SDMMC1_D0, FMC_NE2/FMC_NCE, DCMI_VSYNC/PSSI_RDY, EVENTOUT	-
-	-	-	-	-	-	125	B7	PG10	I/O	FT_sh	-	SPI1_NSS/I2S1_WS, SDMMC1_D1, FMC_NE3, DCMI_D2/PSSI_D2, EVENTOUT	-
-	-	-	-	-	-	126	A7	PG11	I/O	FT_sh	-	LPTIM1_IN2, SPI1_SCK/I2S1_CK, SDMMC1_D2, DCMI_D3/PSSI_D3, EVENTOUT	-
-	-	-	-	-	-	127	A6	PG12	I/O	FT_sh	-	LPTIM1_IN1, PSSI_D15, USART6_RTS, SDMMC1_D3, FMC_NE4, DCMI_D11/PSSI_D11, EVENTOUT	-
-	-	-	-	-	-	128	D6	PG13	I/O	FT_sh	-	TRACED0, LPTIM1_CH1, USART6_CTS/USART6_NSS, FMC_A24, EVENTOUT	-
-	-	-	-	-	-	129	B6	PG14	I/O	FT_sh	-	TRACED1, LPTIM1_ETR, LPTIM1_CH2, USART6_TX, OCTOSPI1_IO7, FMC_A25, EVENTOUT	-
-	-	-	-	-	-	130	-	VSS	S	-	-	-	-
-	-	-	-	-	-	131	-	VDD	S	-	-	-	-
-	-	-	-	-	-	132	A5	PG15	I/O	FT_h	-	SPI4_RDY, USART6_CTS/USART6_NSS, DCMI_D13/PSSI_D13, EVENTOUT	-

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
A5	39	39	55	89	A5	133	B5	PB3(JTDO/ TRACESWO)	I/O	FT_h	-	JTDO/TRACESWO, TIM2_CH2, I3C2_SCL, I2C2_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, LPUART1_TX, FDCAN2_TX, CRS_SYNC, UART5_TX, EVENTOUT	-
A7	40	40	56	90	B5	134	A4	PB4 (NJTRST)	I/O	FT_h	(5)	NJTRST, TIM3_CH1, OCTOSPI1_CLK, LPTIM1_CH2, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, I2C3_SDA, I3C2_SDA, DCMI_D7/PSSI_D7, EVENTOUT	-
-	41	41	57	91	A4	135	E6	PB5	I/O	FT_h	-	TIM3_CH2, OCTOSPI1_NCLK, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, USART6_TX, SPI3_MOSI/I2S3_SDO, FDCAN2_RX, I3C2_SCL, DCMI_D10/PSSI_D10, UART5_RX, EVENTOUT	-
-	42	42	58	92	B4	136	B4	PB6	I/O	FT_f	-	TIM4_CH1, I3C1_SCL, I2C1_SCL, HDMI_CEC, USART6_RX, USART1_TX, LPUART1_TX, FDCAN2_TX, OCTOSPI1_NCS, DCMI_D5/PSSI_D5, UART5_TX, EVENTOUT	-
C3	43	43	59	93	C5	137	A3	PB7	I/O	FT_fa	-	TIM4_CH2, I3C1_SDA, I2C1_SDA, SPI4_MISO, USART6_CTS/USART6_NSS, USART1_RX, LPUART1_RX, FDCAN1_TX, FMC_NL, DCMI_VSYNC/PSSI_RDY, EVENTOUT	WKUP5
B6	44	44	60	94	A3	138	C4	BOOT0	I	B	-	-	-

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Table 14. STM32H533xx pin/ball definition (continued)

Pin number[1]								Pin name (function after reset)[2][3]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP39	LQFP48	UFQFPN48	LQFP64	LQFP100	UFBGA100	LQFP144	UFBGA144						
C5	45	45	61	95	A2	139	B3	PB8	I/O	FT_fsh	-	TIM4_CH3, I3C1_SCL, I2C1_SCL, SPI4_RDY, SPI3_NSS/I2S3_WS, SDMMC1_CKIN, UART4_RX, FDCAN1_RX, SDMMC1_D4, DCMI_D6/PSSI_D6, EVENTOUT	-
-	-	-	-	96	A1	140	A2	PB9	I/O	FT_fsh	-	TIM4_CH4, I3C1_SDA, I2C1_SDA, SPI2_NSS/I2S2_WS, SPI3_SCK/I2S3_CK, SDMMC1_CDIR, UART4_TX, FDCAN1_TX, SDMMC1_D5, DCMI_D7/PSSI_D7, EVENTOUT	-
-	-	-	-	97	B1	141	B2	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, LPTIM2_CH2, LPTIM2_ETR, SPI3_RDY, FDCAN1_RX, FMC_NBL0, DCMI_D2/PSSI_D2, EVENTOUT	-
A9	46	46	62	98	C4	142	D5	VCAP	S	-	-	-	-
-	47	47	63	99	-	143	-	VSS	S	-	-	-	-
-	48	48	64	100	-	144	-	VDD	S	-	-	-	-
-	-	-	-	-	-	-	C7	VDDIO2	S	-	-	-	-

1. A non-connected I/O in a given package is configured as an output tied to VSS. When VREF+ pad is not available on a package, the internal voltage reference buffer (VREFBUF) is not available and must be kept disabled.
2. PC13, PC14 and PC15 are supplied through the power switch (by VSW). Since the switch only sinks a limited amount of current, the use of PC13 to PC15 GPIOs in output mode is limited: The speed must not exceed 2 MHz with a maximum load of 30 pF. These GPIOs must not be used as current sources (for example to drive a LED).
3. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function depends then on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the backup domain and RTC register descriptions in the product reference manual.
4. As a tamper input, only PC13, PA0, PA1, and PA2 are functional in Standby and VBAT mode. As a tamper output, only PC13, and PA1 are functional in Standby and VBAT mode
5. After reset, these pins are configured as JTAG/SW debug alternate functions. The internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated too.

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4.3 Alternate functions

Table 15. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
Port		SYS	LPTIM1/ TIM1/2	TIM3/4/5/ 8/12/15	I3C1/2/LPTIM2/LPUART1/OCTOSPI/ TIM1/8	CEC/DCMI/I2C1/2/3/LPTIM1/2/SPI1/I2S1/SPI3/I2S3/TIM15/USART1	CEC/I3C1/LPTIM1/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4	OCTOSPI/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/USART6/USB_PD	SDMMC1/SPI2/I2S2/SPI3/I2S3/USART1/2/3/6
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	TIM15_BKIN	SPI4_SCK	SPI3_RDY	USART2_CTS/USART2_NSS
	PA1	-	TIM2_CH2	TIM5_CH2	-	TIM15_CH1N	LPTIM1_IN1	OCTOSPI1_DQS	USART2_RTS
	PA2	-	TIM2_CH3	TIM5_CH3	LPUART1_TX	TIM15_CH1	LPTIM1_IN2	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	OCTOSPI1_CLK	TIM15_CH2	SPI2_NSS/ I2S2_WS	SPI3_MOSI/I2S3_SDO	USART2_RX
	PA4	-	-	TIM5_ETR	LPTIM2_CH1	SPI3_MOSI/ I2S3_SDO	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK
	PA5	-	TIM2_CH1	-	TIM8_CH1N	-	SPI1_SCK/ I2S1_CK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO/I2S1_SDI	OCTOSPI1_IO3	-
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SDO	-	-
	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	SPI1_RDY	SPI4_MOSI	USART1_CK
	PA9	-	TIM1_CH2	-	LPUART1_TX	I2C3_SMBA	SPI2_SCK /I2S2_CK	-	USART1_TX
	PA10	-	TIM1_CH3	-	LPUART1_RX	LPTIM2_IN2	-	UCPD1_FRSTX	USART1_RX
	PA11	-	TIM1_CH4	-	LPUART1_CTS	-	SPI2_NSS/ I2S2_WS	UART4_RX	USART1_CTS/ USART1_NSS
	PA12	-	TIM1_ETR	-	LPUART1_RTS	-	SPI2_SCK/ I2S2_CK	UART4_TX	USART1_RTS
	PA13	JTMS/SWDIO	-	-	-	-	-	-	-
	PA14	JTCK/SWCLK	-	-	-	-	-	-	-
	PA15	JTDI	TIM2_CH1	-	-	HDMI_CEC	SPI1_NSS/ I2S1_WS	SPI3_NSS/I2S3_WS	USART1_TX

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Table 15. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	LPTIM1/ TIM1/2	TIM3/4/5/ 8/12/15	I3C1/2/LPTIM2/LPUART1/OCTOSPI/ TIM1/8	CEC/DCMI/I2C1/2/3/LPTIM1/2/SPI1/I2S1/SPI3/I2S3/TIM15/USART1	CEC/I3C1/LPTIM1/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4	OCTOSPI/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/USART6/USB_PD	SDMMC1/SPI2/I2S2/SPI3/I2S3/USART1/2/3/6
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI3_MISO/ I2S3_SDI	OCTOSPI1_IO1	USART2_TX
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	SPI3_SCK	SPI2_NSS/I2S2_WS	OCTOSPI1_IO0	USART3_RX
	PB2	RTC_OUT2	-	-	TIM8_CH4N	SPI1_RDY	LPTIM1_CH1	SPI2_SCK/I2S2_CK	SPI3_MOSI/I2S3_SDO
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	I3C2_SCL	I2C2_SDA	SPI1_SCK/ I2S1_CK	SPI3_SCK/I2S3_CK	-
	PB4	NJTRST	-	TIM3_CH1	OCTOSPI1_CLK	LPTIM1_CH2	SPI1_MISO/ I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/ I2S2_WS
	PB5	-	-	TIM3_CH2	OCTOSPI1_NCLK	I2C1_SMBA	SPI1_MOSI/ I2S1_SDO	USART6_TX	SPI3_MOSI/ I2S3_SDO
	PB6	-	-	TIM4_CH1	I3C1_SCL	I2C1_SCL	HDMI_CEC	USART6_RX	USART1_TX
	PB7	-	-	TIM4_CH2	I3C1_SDA	I2C1_SDA	SPI4_MISO	USART6_CTS/USART6_NSS	USART1_RX
	PB8	-	-	TIM4_CH3	I3C1_SCL	I2C1_SCL	SPI4_RDY	SPI3_NSS/I2S3_WS	SDMMC1_CKIN
	PB9	-	-	TIM4_CH4	I3C1_SDA	I2C1_SDA	SPI2_NSS/I2S2_WS	SPI3_SCK/I2S3_CK	SDMMC1_CDIR
	PB10	-	TIM2_CH3	TIM8_CH1	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	-	USART3_TX
	PB12	-	TIM1_BKIN	TIM8_CH3	OCTOSPI1_NCLK	I2C2_SDA	SPI2_NSS/ I2S2_WS	UCPD1_FRSTX	USART3_CK
	PB13	-	TIM1_CH1N	TIM8_CH2	LPTIM2_CH1	I2C2_SMBA	SPI2_SCK/ I2S2_CK	-	USART3_CTS/USART3_NSS
	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/ I2S2_SDI	-	USART3_RTS
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SDO	SPI1_MOSI/I2S1_SDO	-

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Table 15. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	LPTIM1/ TIM1/2	TIM3/4/5/ 8/12/15	I3C1/2/LPTIM2/LPUART1/OCTOSPI/ TIM1/8	CEC/DCMI/I2C1/2/3/LPTIM1/2/SPI1/I2S1/SPI3/I2S3/TIM15/USART1	CEC/I3C1/LPTIM1/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4	OCTOSPI/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/USART6/USB_PD	SDMMC1/SPI2/I2S2/SPI3/I2S3/USART1/2/3/6
Port C	PC0	-	-	-	-	-	-	SPI4_MISO	SPI2_RDY
	PC1	TRACED0	-	-	-	-	SPI2_MOSI/I2S2_SDO	SPI4_MOSI	-
	PC2	PWR_CSLEEP	-	TIM4_CH4	-	-	SPI2_MISO/I2S2_SDI	OCTOSPI1_IO5	-
	PC3	PWR_CSTOP	-	-	LPUART1_TX	-	SPI2_MOSI/I2S2_SDO	OCTOSPI1_IO6	-
	PC4	-	TIM2_CH4	-	LPTIM2_ETR	-	I2S1_MCK	-	USART3_RX
	PC5	-	TIM1_CH4N	-	-	PSSI_D15	-	SPI4_SCK	-
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	I2S2_MCK	-	USART6_TX
	PC7	TRGIO	-	TIM3_CH2	TIM8_CH2	-	-	I2S3_MCK	USART6_RX
	PC8	TRACED1	-	TIM3_CH3	TIM8_CH3	-	-	-	USART6_CK
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	AUDIOCLK	-	-
	PC10	-	-	-	I3C2_SCL	-	-	SPI3_SCK/I2S3_CK	USART3_TX
	PC11	-	-	-	I3C2_SDA	-	-	SPI3_MISO/I2S3_SDI	USART3_RX
	PC12	TRACED3	-	TIM15_CH1	LPTIM2_CH2	-	-	SPI3_MOSI/I2S3_SDO	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

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Table 15. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	LPTIM1/ TIM1/2	TIM3/4/5/ 8/12/15	I3C1/2/LPTIM2/LPUART1/OCTOSPI/ TIM1/8	CEC/DCMI/I2C1/2/3/LPTIM1/2/SPI1/I2S1/SPI3/I2S3/TIM15/USART1	CEC/I3C1/LPTIM1/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4	OCTOSPI/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/USART6/USB_PD	SDMMC1/SPI2/I2S2/SPI3/I2S3/USART1/2/3/6
Port D	PD0	-	-	-	TIM8_CH4N	-	-	-	-
	PD1	-	-	-	-	-	-	-	-
	PD2	TRACED2	-	TIM3_ETR	-	TIM15_BKIN	-	-	-
	PD3	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CTS/USART2_NSS
	PD4	-	-	-	-	-	-	-	USART2_RTS
	PD5	-	TIM1_CH4N	-	-	-	SPI2_RDY	-	USART2_TX
	PD6	-	-	-	I3C2_SCL	I2C3_SCL	SPI3_MOSI/I2S3_SDO	-	USART2_RX
	PD7	-	-	-	I3C2_SDA	I2C3_SDA	SPI1_MOSI/I2S1_SDO	SPI3_MISO/I2S3_SDI	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	LPTIM2_CH2	-	-	-	USART3_CK
	PD11	-	-	-	LPTIM2_IN2	-	-	-	USART3_CTS/USART3_NSS
	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	-	I3C1_SCL	-	USART3_RTS
	PD13	-	LPTIM1_CH1	TIM4_CH2	LPTIM2_CH1	-	I3C1_SDA	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-

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Table 15. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	LPTIM1/ TIM1/2	TIM3/4/5/ 8/12/15	I3C1/2/LPTIM2/LPUART1/OCTOSPI/ TIM1/8	CEC/DCMI/I2C1/2/3/LPTIM1/2/SPI1/I2S1/SPI3/I2S3/TIM15/USART1	CEC/I3C1/LPTIM1/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4	OCTOSPI/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/USART6/USB_PD	SDMMC1/SPI2/I2S2/SPI3/I2S3/USART1/2/3/6
Port E	PE0	-	LPTIM1_ETR	TIM4_ETR	LPTIM2_CH2	LPTIM2_ETR	-	SPI3_RDY	-
	PE2	TRACECLK	LPTIM1_IN2	-	-	-	SPI4_SCK	-	-
	PE3	TRACED0	-	-	-	TIM15_BKIN	-	-	-
	PE4	TRACED1	-	-	-	TIM15_CH1N	SPI4_NSS	-	-
	PE5	TRACED2	-	-	-	TIM15_CH1	SPI4_MISO	-	-
	PE6	TRACED3	TIM1_BKIN2	-	-	TIM15_CH2	SPI4_MOSI	-	-
	PE7	-	TIM1_ETR	-	-	-	-	-	-
	PE8	-	TIM1_CH1N	-	-	-	-	-	-
	PE9	-	TIM1_CH1	-	-	-	-	-	-
	PE10	-	TIM1_CH2N	-	-	-	-	-	-
	PE11	-	TIM1_CH2	-	-	SPI1_RDY	SPI4_NSS	OCTOSPI1_NCS	-
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	-	-
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	-	-
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-
	PE15	-	TIM1_BKIN	-	TIM1_CH4N	-	-	-	-

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Table 15. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	LPTIM1/ TIM1/2	TIM3/4/5/ 8/12/15	I3C1/2/LPTIM2/LPUART1/OCTOSPI/ TIM1/8	CEC/DCMI/I2C1/2/3/LPTIM1/2/SPI1/I2S1/SPI3/I2S3/TIM15/USART1	CEC/I3C1/LPTIM1/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4	OCTOSPI/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/USART6/USB_PD	SDMMC1/SPI2/I2S2/SPI3/I2S3/USART1/2/3/6
Port F	PF0	-	-	-	I3C2_SDA	I2C2_SDA	-	-	-
	PF1	-	-	-	I3C2_SCL	I2C2_SCL	-	-	-
	PF2	-	-	-	-	I2C2_SMBA	-	-	-
	PF3	-	-	-	-	-	-	-	-
	PF4	-	-	-	-	-	-	-	-
	PF5	-	-	-	-	-	I3C1_SCL	-	-
	PF6	-	-	-	-	-	-	-	-
	PF7	-	-	-	-	-	-	-	-
	PF8	-	-	-	-	-	-	-	-
	PF9	-	-	-	-	-	-	-	-
	PF10	-	-	-	-	PSSI_D15	-	-	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	-	-	-
	PF13	-	-	-	-	-	-	-	-
	PF14	-	-	-	-	-	-	-	-
	PF15	-	-	-	-	-	I3C1_SDA	-	-

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Table 15. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	LPTIM1/ TIM1/2	TIM3/4/5/ 8/12/15	I3C1/2/LPTIM2/LPUART1/OCTOSPI/ TIM1/8	CEC/DCMI/I2C1/2/3/LPTIM1/2/SPI1/I2S1/SPI3/I2S3/TIM15/USART1	CEC/I3C1/LPTIM1/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4	OCTOSPI/SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/USART6/USB_PD	SDMMC1/SPI2/I2S2/SPI3/I2S3/USART1/2/3/6
Port G	PG0	-	-	-	-	-	-	-	-
	PG1	-	-	-	-	-	-	-	SPI2_MOSI/I2S2_SDO
	PG2	-	-	-	TIM8_BKIN	-	-	-	-
	PG3	-	-	-	TIM8_BKIN2	-	-	-	-
	PG4	-	TIM1_BKIN2	-	-	-	-	-	-
	PG5	-	TIM1_ETR	-	-	-	-	-	-
	PG6	-	-	-	I3C1_SDA	-	SPI1_RDY	-	-
	PG7	-	-	-	I3C1_SCL	-	-	-	USART6_CK
	PG8	-	-	-	TIM8_ETR	-	SPI3_MOSI/I2S3_SDO	-	USART6_RTS
	PG9	-	-	-	-	-	SPI1_MISO/I2S1_SDI	-	USART6_RX
	PG10	-	-	-	-	-	SPI1_NSS/I2S1_WS	-	-
	PG11	-	LPTIM1_IN2	-	-	-	SPI1_SCK/I2S1_CK	-	-
	PG12	-	LPTIM1_IN1	-	-	PSSI_D15	-	-	USART6_RTS
	PG13	TRACED0	LPTIM1_CH1	-	-	-	-	-	USART6_CTS/USART6_NSS
	PG14	TRACED1	LPTIM1_ETR	-	-	LPTIM1_CH2	-	-	USART6_TX
	PG15	-	-	-	-	-	SPI4_RDY	-	USART6_CTS/USART6_NSS
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

1. Refer to the next table for AF8 to AF15.

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Table 16. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/SDMMC1/UART4/5	FDCAN1/2/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/I2C3/I3C2/OCTOSPI	CRS/FMC[NAND16)/I3C2/OCTOSPI/SDMMC1/USB_	FMC[NAND16)/OCTOSPI/SDMMC1/USB_PD	FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/SDMMC1	DCMI/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)	TIM2/UART5/USART6	SYS
Port A	PA0	UART4_TX	FDCAN2_RX	-	-	-	-	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	OCTOSPI1_IO3	-	-	-	-	USART6_CK	EVENTOUT
	PA2	-	-	-	-	-	-	-	EVENTOUT
	PA3	-	-	-	-	-	-	-	EVENTOUT
	PA4	-	-	-	-	-	DCMI_HSYNC/PSSI_DE	-	EVENTOUT
	PA5	-	-	-	-	-	PSSI_D14	TIM2_ETR	EVENTOUT
	PA6	-	-	-	-	-	DCMI_PIXCLK/PSSI_PDCK	-	EVENTOUT
	PA7	-	-	OCTOSPI1_IO2	-	-	FMC_NWE	-	EVENTOUT
	PA8	-	I3C2_SCL	USB_SOF	-	FMC_NOE	DCMI_D3/PSSI_D3	-	EVENTOUT
	PA9	-	-	-	-	FMC_NWE	DCMI_D0/PSSI_D0	-	EVENTOUT
	PA10	-	FDCAN2_TX	-	-	SDMMC1_D0	DCMI_D1/PSSI_D1	-	EVENTOUT
	PA11	-	FDCAN1_RX	USB_DM	-	-	-	-	EVENTOUT
	PA12	-	FDCAN1_TX	USB_DP	-	-	-	-	EVENTOUT
	PA13	-	-	-	-	-	-	-	EVENTOUT
	PA14	-	-	-	-	-	-	-	EVENTOUT
	PA15	UART4_RTS	OCTOSPI1_NCS	-	-	FMC_NBL1	DCMI_D11/PSSI_D11	TIM2_ETR	EVENTOUT

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Table 16. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/SDMMC1/UART4/5	FDCAN1/2/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/I2C3/I3C2/OCTOSPI	CRS/FMC[NAND16)/I3C2/OCTOSPI/SDMMC1/USB_	FMC[NAND16)/OCTOSPI/SDMMC1/USB_PD	FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/SDMMC1	DCMI/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)	TIM2/UART5/USART6	SYS
Port B	PB0	UART4_CTS	-	-	-	-	-	-	EVENTOUT
	PB1	-	-	-	-	-	-	-	EVENTOUT
	PB2	-	OCTOSPI1_CLK	OCTOSPI1_DQS	-	SDMMC1_CMD	-	-	EVENTOUT
	PB3	LPUART1_TX	FDCAN2_TX	CRS_SYNC	-	-	-	UART5_TX	EVENTOUT
	PB4	-	I2C3_SDA	I3C2_SDA	-	-	DCMI_D7/PSSI_D7	-	EVENTOUT
	PB5	-	FDCAN2_RX	I3C2_SCL	-	-	DCMI_D10/PSSI_D10	UART5_RX	EVENTOUT
	PB6	LPUART1_TX	FDCAN2_TX	OCTOSPI1_NCS	-	-	DCMI_D5/PSSI_D5	UART5_TX	EVENTOUT
	PB7	LPUART1_RX	FDCAN1_TX	-	-	FMC_NL	DCMI_VSYNC/PSSI_RDY	-	EVENTOUT
	PB8	UART4_RX	FDCAN1_RX	-	-	SDMMC1_D4	DCMI_D6/PSSI_D6	-	EVENTOUT
	PB9	UART4_TX	FDCAN1_TX	-	-	SDMMC1_D5	DCMI_D7/PSSI_D7	-	EVENTOUT
	PB10	-	OCTOSPI1_NCS	-	-	-	-	-	EVENTOUT
	PB12	-	FDCAN2_RX	-	-	-	-	UART5_RX	EVENTOUT
	PB13	LPUART1_RX	FDCAN2_TX	-	-	SDMMC1_D0	-	UART5_TX	EVENTOUT
	PB14	UART4_RTS	-	-	-	-	-	-	EVENTOUT
	PB15	UART4_CTS	-	OCTOSPI1_CLK	-	-	DCMI_D2/PSSI_D2	UART5_RX	EVENTOUT

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Table 16. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/SDMMC1/UART4/5	FDCAN1/2/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/I2C3/I3C2/OCTOSPI	CRS/FMC[NAND16)/I3C2/OCTOSPI/SDMMC1/USB_	FMC[NAND16)/OCTOSPI/SDMMC1/USB_PD	FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/SDMMC1	DCMI/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)	TIM2/UART5/USART6	SYS
Port C	PC0	-	FMC_A25	OCTOSPI1_IO7	-	-	-	-	EVENTOUT
	PC1	-	-	OCTOSPI1_IO4	-	-	-	-	EVENTOUT
	PC2	-	OCTOSPI1_IO2	-	-	-	-	-	EVENTOUT
	PC3	-	OCTOSPI1_IO0	-	-	-	-	-	EVENTOUT
	PC4	-	-	-	-	-	-	-	EVENTOUT
	PC5	-	-	OCTOSPI1_DQS	-	-	-	-	EVENTOUT
	PC6	SDMMC1_D0DIR	FMC_NWAIT	I3C2_SCL	OCTOSPI1_IO5	SDMMC1_D6	DCMI_D0/PSSI_D0	-	EVENTOUT
	PC7	SDMMC1_D123DIR	FMC_NE1	I3C2_SDA	OCTOSPI1_IO6	SDMMC1_D7	DCMI_D1/PSSI_D1	-	EVENTOUT
	PC8	UART5_RTS	FMC_NE2/FMC_NCE	FMC_INT	FMC_ALE	SDMMC1_D0	DCMI_D2/PSSI_D2	-	EVENTOUT
	PC9	UART5_CTS	OCTOSPI1_IO0	-	FMC_CLE	SDMMC1_D1	DCMI_D3/PSSI_D3	-	EVENTOUT
	PC10	UART4_TX	OCTOSPI1_IO1	-	-	SDMMC1_D2	DCMI_D8/PSSI_D8	-	EVENTOUT
	PC11	UART4_RX	OCTOSPI1_NCS	-	-	SDMMC1_D3	DCMI_D4/PSSI_D4	-	EVENTOUT
	PC12	UART5_TX	-	-	-	SDMMC1_CK	DCMI_D9/PSSI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

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Table 16. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/SDMMC1/UART4/5	FDCAN1/2/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/I2C3/I3C2/OCTOSPI	CRS/FMC[NAND16)/I3C2/OCTOSPI/SDMMC1/USB_	FMC[NAND16)/OCTOSPI/SDMMC1/USB_PD	FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/SDMMC1	DCMI/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)	TIM2/UART5/USART6	SYS
Port D	PD0	UART4_RX	FDCAN1_RX	-	-	FMC_D2/FMC_AD2	-	-	EVENTOUT
	PD1	UART4_TX	FDCAN1_TX	-	-	FMC_D3/FMC_AD3	-	-	EVENTOUT
	PD2	UART5_RX	-	-	-	SDMMC1_CMD	DCMI_D11/PSSI_D11	-	EVENTOUT
	PD3	-	-	-	-	FMC_CLK	DCMI_D5/PSSI_D5	-	EVENTOUT
	PD4	-	-	OCTOSPI1_IO4	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	FDCAN1_TX	OCTOSPI1_IO5	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	OCTOSPI1_IO6	SDMMC1_CK	FMC_NWAIT	DCMI_D10/PSSI_D10	-	EVENTOUT
	PD7	-	-	OCTOSPI1_IO7	SDMMC1_CMD	FMC_NE1/FMC_NCE	-	-	EVENTOUT
	PD8	-	-	-	-	FMC_D13/FMC_AD13	-	-	EVENTOUT
	PD9	-	FDCAN2_RX	-	-	FMC_D14/FMC_AD14	-	-	EVENTOUT
	PD10	-	-	-	-	FMC_D15/FMC_AD15	-	-	EVENTOUT
	PD11	UART4_RX	OCTOSPI1_IO0	-	-	FMC_A16/FMC_CLE	-	-	EVENTOUT
	PD12	UART4_TX	OCTOSPI1_IO1	-	-	FMC_A17/FMC_ALE	DCMI_D12/PSSI_D12	-	EVENTOUT
	PD13	-	OCTOSPI1_IO3	-	-	FMC_A18	DCMI_D13/PSSI_D13	-	EVENTOUT
	PD14	-	-	-	-	FMC_D0/FMC_AD0	-	-	EVENTOUT
	PD15	-	-	-	-	FMC_D1/FMC_AD1	-	-	EVENTOUT

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Table 16. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/SDMMC1/UART4/5	FDCAN1/2/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/I2C3/I3C2/OCTOSPI	CRS/FMC[NAND16)/I3C2/OCTOSPI/SDMMC1/USB_	FMC[NAND16)/OCTOSPI/SDMMC1/USB_PD	FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/SDMMC1	DCMI/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)	TIM2/UART5/USART6	SYS
Port E	PE0	-	FDCAN1_RX	-	-	FMC_NBL0	DCMI_D2/PSSI_D2	-	EVENTOUT
	PE2	-	OCTOSPI1_IO2	-	-	FMC_A23	DCMI_D3/PSSI_D3	-	EVENTOUT
	PE3	-	-	-	-	FMC_A19	-	-	EVENTOUT
	PE4	-	-	-	-	FMC_A20	DCMI_D4/PSSI_D4	-	EVENTOUT
	PE5	-	-	-	-	FMC_A21	DCMI_D6/PSSI_D6	-	EVENTOUT
	PE6	-	-	-	-	FMC_A22	DCMI_D7/PSSI_D7	-	EVENTOUT
	PE7	-	-	OCTOSPI1_IO4	-	FMC_D4/FMC_AD4	-	-	EVENTOUT
	PE8	-	-	OCTOSPI1_IO5	-	FMC_D5/FMC_AD5	-	-	EVENTOUT
	PE9	-	-	OCTOSPI1_IO6	-	FMC_D6/FMC_AD6	-	-	EVENTOUT
	PE10	-	-	OCTOSPI1_IO7	-	FMC_D7/FMC_AD7	-	-	EVENTOUT
	PE11	-	-	-	-	FMC_D8/FMC_AD8	-	-	EVENTOUT
	PE12	-	-	-	-	FMC_D9/FMC_AD9	-	-	EVENTOUT
	PE13	-	-	-	-	FMC_D10/FMC_AD10	-	-	EVENTOUT
	PE14	-	-	-	-	FMC_D11/FMC_AD11	-	-	EVENTOUT
	PE15	-	-	-	-	FMC_D12/FMC_AD12	-	-	EVENTOUT

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Table 16. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/SDMMC1/UART4/5	FDCAN1/2/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/I2C3/I3C2/OCTOSPI	CRS/FMC[NAND16)/I3C2/OCTOSPI/SDMMC1/USB_	FMC[NAND16)/OCTOSPI/SDMMC1/USB_PD	FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/SDMMC1	DCMI/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)	TIM2/UART5/USART6	SYS
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	OCTOSPI1_IO3	-	-	-	-	EVENTOUT
	PF7	-	-	OCTOSPI1_IO2	-	-	-	-	EVENTOUT
	PF8	-	-	OCTOSPI1_IO0	-	-	-	-	EVENTOUT
	PF9	-	-	OCTOSPI1_IO1	-	-	-	-	EVENTOUT
	PF10	-	OCTOSPI1_CLK	-	-	-	DCMI_D11/PSSI_D11	-	EVENTOUT
	PF11	-	OCTOSPI1_NCLK	-	-	-	DCMI_D12/PSSI_D12	-	EVENTOUT
	PF12	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	FMC_A9	-	-	EVENTOUT

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Table 16. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/SDMMC1/UART4/5	FDCAN1/2/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/I2C3/I3C2/OCTOSPI	CRS/FMC[NAND16)/I3C2/OCTOSPI/SDMMC1/USB_	FMC[NAND16)/OCTOSPI/SDMMC1/USB_PD	FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)/SDMMC1	DCMI/FMC[NAND16)/FMC[NORmux)/FMC[NOR_RAM)	TIM2/UART5/USART6	SYS
Port G	PG0	-	-	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	-	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	FMC_A12	-	-	EVENTOUT
	PG3	-	-	-	-	FMC_A13	-	-	EVENTOUT
	PG4	-	-	-	-	FMC_A14	-	-	EVENTOUT
	PG5	-	-	-	-	FMC_A15	-	-	EVENTOUT
	PG6	-	-	OCTOSPI1_NCS	UCPD1_FRSTX	FMC_NE3	DCMI_D12/PSSI_D12	-	EVENTOUT
	PG7	-	-	-	UCPD1_FRSTX	FMC_INT	DCMI_D13/PSSI_D13	-	EVENTOUT
	PG8	-	-	-	-	-	-	-	EVENTOUT
	PG9	-	OCTOSPI1_IO6	-	SDMMC1_D0	FMC_NE2/FMC_NCE	DCMI_VSYNC/PSSI_RDY	-	EVENTOUT
	PG10	-	-	-	SDMMC1_D1	FMC_NE3	DCMI_D2/PSSI_D2	-	EVENTOUT
	PG11	-	-	SDMMC1_D2	-	-	DCMI_D3/PSSI_D3	-	EVENTOUT
	PG12	-	-	SDMMC1_D3	-	FMC_NE4	DCMI_D11/PSSI_D11	-	EVENTOUT
	PG13	-	-	-	-	FMC_A24	-	-	EVENTOUT
	PG14	-	OCTOSPI1_IO7	-	-	FMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	DCMI_D13/PSSI_D13	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT

1. Refer to the previous table for AF0 to AF7.

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5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes, and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = V_{DDA} = 3.3 V (for the 1.71 ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 12*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 13*.

Figure 12. Pin loading conditions

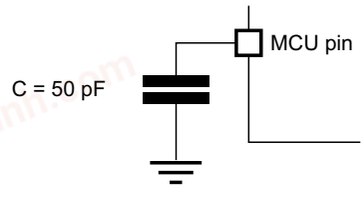
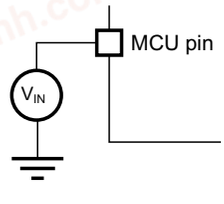


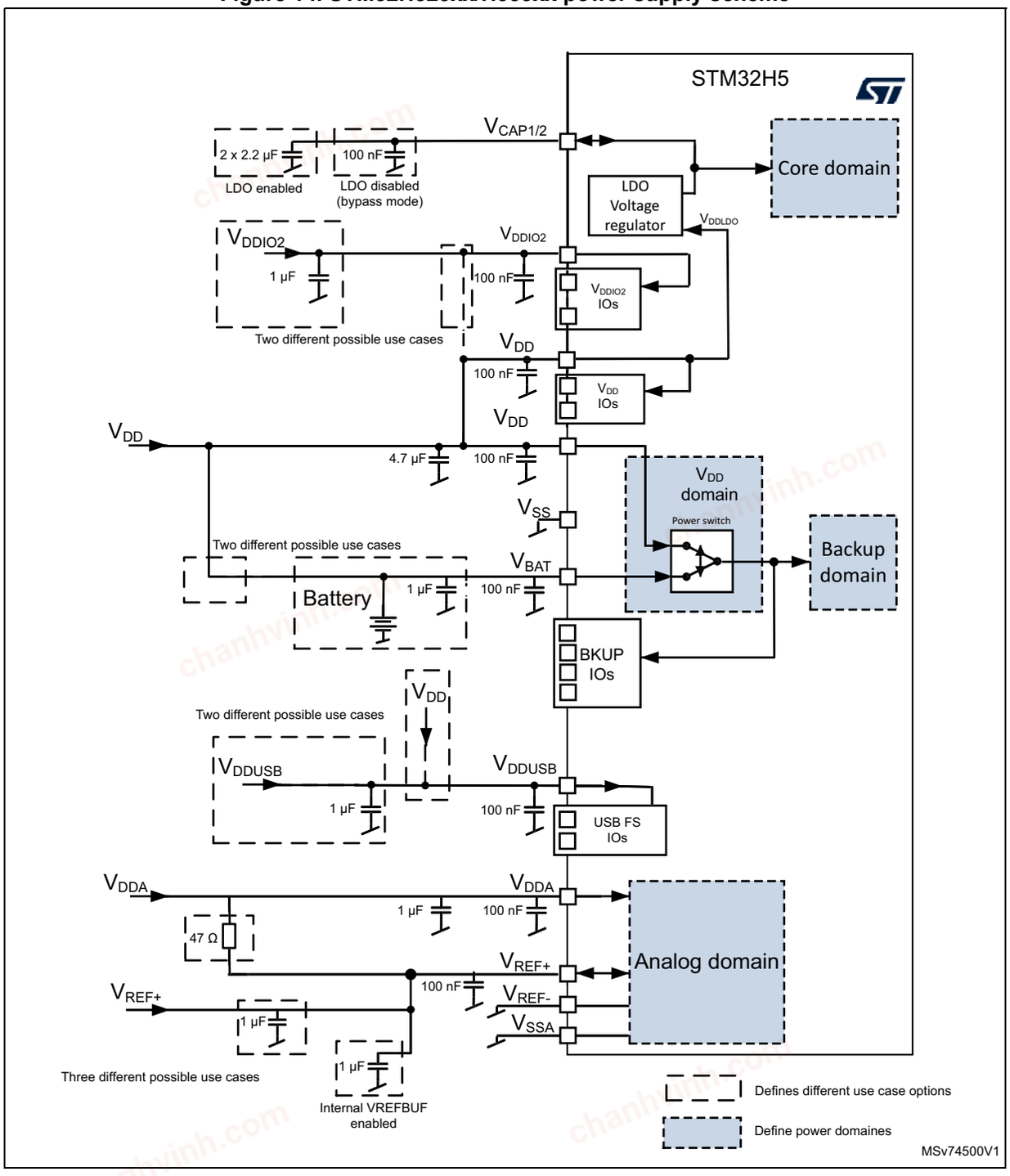
Figure 13. Pin input voltage



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5.1.6 Power supply scheme

Figure 14. STM32H523xx/H533xx power supply scheme



Note: Refer to "Getting started with STM32H5 Series hardware development" (AN5711) for more details.

Caution: Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to or below the appropriate

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pins on the underside of the PCB to ensure the good functionality of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 17*, *Table 18*, and *Table 19* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 17. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	External main supply voltage (including V_{DDA}, V_{DDUSB}, V_{DDIO2}(2)(3)(4), V_{BAT}, and V_{REF+})	-0.3	4.0	V
V_{DDIOx}(4) - V_{SS}	I/O supply when HSLV(2) = 0	-0.3	4.0	V
	I/O supply when HSLV(2) = 1	-0.3	2.75	
V_{IN}(5)	Input voltage on FT_xxx pins except FT_c pins	V_{SS} - 0.3	min (min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0, 6.0 V)(6)(7)	V
	Input voltage on FT_t in V_{BAT} mode	V_{SS} - 0.3	min (min(V_{BAT}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0V, 6.0 V)	V
	Input voltage on TT_xx pins	V_{SS} - 0.3	4.0	
	Input voltage on BOOT0 pin	V_{SS}	min (min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 4.0, 6.0 V)(6)	
	Input voltage on FT_c pins	V_{SS} - 0.3	5.5	
	Input voltage on any other pins	V_{SS} - 0.3	4.0	
V_{REF+}-V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50.0	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50.0	

1. All main power (V_{DD}, $V_{DDA}V_{DDUSB}$, V_{DDIO2}, V_{REF+}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. HSLV = High-speed low-voltage mode. Refer to General-purpose I/Os (GPIO) section of RM0481.
3. If HSLV = 0.
4. V_{DDIO1} or V_{DDIO2}. V_{DDIO1} = V_{DD}.
5. V_{IN} maximum must always be respected. Refer to the maximum allowed injected current values.
6. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
7. This formula must be applied on power supplies related to the I/O structure described by the pin definition table.

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Table 18. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	350	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	350	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk/sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, NRST pins	-5 / 0	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, and V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os, and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 17* for the minimum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum\lvert I_{INJ(PIN)}\rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 19. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	130(1)	°C

1. The junction temperature is limited to 105 °C in the VOS0 voltage range.

5.3 Operating conditions

5.3.1 General operating conditions

Table 20. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	HSLV(1) = 0	1.71(2)	-	3.6	V
		HSLV(1) = 1	1.71(2)	-	2.7	
V_{DDIO2}	PB8, PB9, PD6, PD7, PG[9:14] I/Os supply voltage	At least one I/O in PB8, PB9, PD6, PD7, PG[9:14] is used, HSLV(1) = 0	1.08	-	3.6	V
		At least one I/O in PB8, PB9, PD6, PD7, PG[9:14] is used, HSLV(1) = 1	1.08	-	2.7	
		PB8,PB9, PD6,PD7, PG[9:14] not use	0		3.6	

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Table 20. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB supply voltage	USB is used	3.0	-	3.6	V
		USB is not used	0	-	3.6	
V_{DDA}	Analog supply voltage	ADC is used	1.62	-	3.6	V
		DAC is used	1.8	-		
		VREFBUF is used	2.1	-		
		ADC, DAC, and VREFBUF are not used	0	-		
V_{BAT}	Backup domain supply voltage	-	1.2	-	3.6	V
V_{IN}	I/O input voltage	All I/Os except FT_c and TT_xx	-0.3	-	min (min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 3.6V, 5.5 V) (3)(4)	V
		Input voltage on FT_t in VBAT mode	-0.3	-	min (min (V_{BAT}, V_{DDA}, V_{DDUSB}, V_{DDIO2}) + 3.6 V, 5.5 V) (3)(4)	
		FT_c I/O	-0.3	-	5.0	
		TT_xx I/O	-0.3	-	V_{DDIOx} + 0.3	
V_{CORE}	Internal regulator ON	VOS0(5) (max frequency for AHB and APB: 250 MHz)	1.30	1.35	1.40	V
		VOS1 (max frequency for AHB and APB: 200 MHz)	1.15	1.20	1.26	
		VOS2 (max frequency for AHB and APB: 150 MHz)	1.05	1.10	1.15	
		VOS3 (max frequency for AHB and APB: 100 MHz)	0.95	1.00	1.05	
	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on VCAP pins	VOS0(5)	1.32	1.35	1.40	V
		VOS1	1.17	1.20	1.26	
		VOS2	1.07	1.10	1.15	
		VOS3	0.97	1.00	1.05	
	Stop mode	SVOS3	-	1.0	-	V
		SVOS4	-	0.9	-	
		SVOS5	-	0.74	-	

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Table 20. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
f_{HCLK}	AHB clock frequency	VOS0(5)	-	-	250	MHz
		VOS1	-	-	200	
		VOS2	-	-	150	
		VOS3	-	-	100	
f_{PCLKx} (x=1,2,3)	APB1, APB2, APB3 clock frequency	VOS0(5)	-	-	250	MHz
		VOS1	-	-	200	
		VOS2	-	-	150	
		VOS3	-	-	100	
P_D	Power dissipation at T_A = 85 °C for suffix 6(6)	WLCSP39	See *Table 137* for appropriate thermal resistance and package. Power dissipation is calculated according to ambient temperature (T_A), maximum junction temperature (T_J), and selected thermal resistance.			mW
		LQFP48				
		UFQFPN48				
		LQFP64				
		LQFP100				
		LQFP144				
		UFBGA100				
		UFBGA144				
P_D	Power dissipation at T_A = 105 °C for suffix 7(6)	WLCSP39	See *Table 137* for appropriate thermal resistance and package. Power dissipation is calculated according to ambient temperature (T_A), maximum junction temperature (T_J), and selected thermal resistance.			mW
		LQFP48				
		UFQFPN48				
		LQFP64				
		LQFP100				
		LQFP144				
		UFBGA100				
		UFBGA144				
T_A	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	-	105	°C
		Low dissipation or LDO bypass mode	-40	-	125	
	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	-	85	
T_J	Junction temperature range	VOS0	-40	-	105	°C
		VOS1, VOS2, and VOS3	-40	-	130	

1. HSLV = High-speed low-voltage mode. Refer to General-purpose I/Os (GPIO) section of RM0481.
2. When RESET is released functionality is guaranteed down to BOR level 0 minimum voltage.
3. This formula must be applied on power supplies related to the I/O structure described by the pin definition table. Maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}, V_{DDIO2}) + 3.6 V and 5.5 V.
4. For operation with voltages higher than min (V_{DD}, V_{DDA}, V_{DDIO2}) + 0.3V, the internal pull-up and pull-down resistors must be disabled.
5. In VOS0 mode the max T_J is 105 °C.

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6. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Table 19*).

Table 21. Maximum allowed clock frequencies

Symbol(1)(2)	Parameter	VOS0	VOS1	VOS2	VOS3	Unit
f_{CPU}	CPU	250	200	150	100	MHz
f_{HCLK}	AHB	250	200	150	100	
f_{PCLK}	APB	250	200	150	100	
-	FMC	250	200	150	100	
$f_{octospi_ker_ck}$	OCTOSPI[1:2]	250	200	150	100	
$f_{sdmmc_ker_ck}$	SDMMC[1:2]	250	200	150	100	
-	HDMI_CEC	4	4	4	4	
$f_{fdcan_ker_ck}$	FDCAN	250	200	150	100	
$f_{I2C_ker_ck}$	I2C[1:4]	250	200	150	100	
$f_{I3C_ker_ck}$	I3C	250	200	150	100	
$f_{lptim_ker_ck}$	LPTIM[1:2]	250	200	150	100	
$f_{tim_ker_ck}$	TIM[1:8], TIM12, TIM15	250	200	150	100	
f_{rng_clk}	RNG	50	50	50	50	
$f_{spi_ker_ck}$	SPI(I2S)1,2,3	125	100	75	50	
	SPI4	125	100	75	50	
$f_{lpuart_ker_ck}$	LPUART1	250	200	150	100	
$f_{usart_ker_ck}$	USART/UART	250	200	150	100	
$f_{usb_ker_ck}$	USB FS	50	50	50	50	
$f_{adc_ker_ck}$	ADC/DAC	125	100	75	50	
f_{dac_pclk}	DAC	250	200	150	100	
$f_{usb_ker_ck}$	USBPD	64	64	64	64	
$f_{rtc_ker_ck}$	RTC	1	1	1	1	
-	DCMI	250	200	150	100	

1. Specified by design - Not tested in production.
2. The maximum kernel clock frequencies can be limited by the maximum peripheral clock frequency (refer to each peripheral electrical characteristics).

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5.3.2 VCAP external capacitor

Stabilization for the embedded LDO regulator is achieved by connecting an external capacitor C_{EXT} to the VCAPx (one or two pins, depending upon the package). CEXT is specified in *Table 22*. VCAP operating conditions. Two external capacitors must be connected to VCAP pins (refer to AN5711 "*STM32H5 Series hardware development*").

Figure 15. External capacitor C_{EXT}

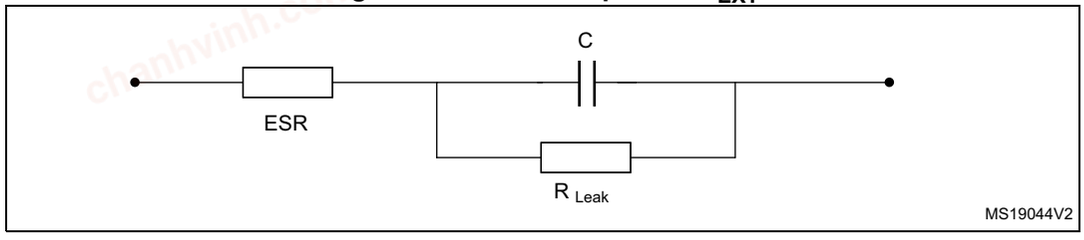


Table 22. Supply voltage and maximum frequency configuration

Symbol	Parameter	Conditions
C_{EXT}	External capacitor for LDO enabled	2.2 µF(1)
ESR	Equivalent series resistance of the external capacitor	< 100 mΩ

1. This value corresponds to CEXT typical value. A variation of ±20% is tolerated

5.3.3 Operating conditions at power-up/down

Subject to general operating conditions for T_A.

Table 23. Operating conditions at power-up/down (regulator ON)

Symbol	Parameter	Min	Max	Unit
T_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
T_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
T_{VDDUSB}	T_{VDDUSB} rise time rate	0	∞	
	T_{VDDUSB} fall time rate	10	∞	
T_{VDDIO2}	T_{VDDIO2} rise time rate	0	∞	
	T_{VDDIO2} fall time rate	10	∞	
T_{VBAT}	T_{VBAT} rise time rate	0	∞	
	T_{VBAT} fall time rate	10	∞	

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5.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 24. Embedded reset and power control block characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 detection	V_{DD} rising	-	377	550	µs
$V_{POR/PDR}$	Power-on/down reset threshold (BORH_EN =0)	Rising edge	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brownout reset threshold 1 (BORH_EN =1)	Rising edge	2.04	2.10	2.15	V
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brownout reset threshold 2 (BORH_EN =1)	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brownout reset threshold 3 (BORH_EN =1)	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	PVD threshold 0	Rising edge	1.90	1.96	2.01	V
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	PVD threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	PVD threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	PVD threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	PVD threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	PVD threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	PVD threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge	2.69	2.76	2.83	
$V_{POR/PDR}$	Hysteresis for power-on/down reset	Hysteresis in Run mode	-	43	-	mV
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BOR (unless BORH_EN = 0) and PVD	-	-	100	-	
$I_{DD_BOR_PVD}$(2)	BOR and PVD consumption from V_{DD}	-	-	-	0.630	µA
$I_{DD_POR_PDR}$	POR and PDR consumption from V_{DD}	-	0.8	-	1.2	

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Table 24. Embedded reset and power control block characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVD0}	V_{DDA} voltage monitor 0 threshold	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVD1}	V_{DDA} voltage monitor 1threshold	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVD2}	V_{DDA} voltage monitor 2 threshold	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVD3}	V_{DDA} voltage monitor 3 threshold	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{IO2VM}	V_{DDIO2} voltage monitor threshold	-	-	0.9	-	V
V_{hyst_AVD}	Hysteresis of V_{DDA} voltage monitor	-	-	100	-	mV
$I_{DD_AVD_IO2VM}$(2)	Power voltage detector consumption from V_{DD} (AVD, IO2VM)	-	-	-	0.25	µA
$I_{DD_AVD_A}$(2)	V_{DDA} analog voltage detector consumption from VDDA (resistor bridge)	-	-	-	0.25	

1. Evaluated by characterization and not tested in production, unless otherwise specified.
2. Specified by design - Not tested in production

5.3.5 Embedded reference voltage

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20*.

Table 25. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltage	-40 °C < T_J < +130 °C	1.180	1.216	1.255	V
$t_{S_vrefint}$(2)(3)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}	V_{BAT} sampling time when reading the internal V_{BAT} voltage		9	-	-	
$t_{start_vrefint}$(3)	Start time of reference voltage buffer when the ADC is enabled	-	-	-	4.4	
I_{refbuf}(3)	Reference buffer consumption for ADC	V_{DD} = 3.3 V	9	13.5	23	µA
ΔV_{REFINT}(3)	Internal reference voltage spread over the temperature range	-40 °C < T_J < +130 °C	-	5	15	mV
T_{Coeff}	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	10	1370	ppm/V

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Table 25. Embedded reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT_DIV1}(3)	1/4 reference voltage	-	-	25	-	%V_{REFINT}
V_{REFINT_DIV2}(3)	1/2 reference voltage		-	50	-	
V_{REFINT_DIV3}(3)	3/4 reference voltage		-	75	-	

1. V_{REFINT} does not take into account package and soldering effects.
2. The shortest sampling time for the application can be determined by multiple iterations.
3. Specified by design - Not tested in production.

Table 26. Internal reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFINT_CAL}	Raw data acquired at 30 °C, V_{DDA} = 3.3 V	0x08FF F810 - 0x08FF F811

5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait-state number, depending on the f_{HCLK} frequency (refer to the tables “FLASH recommended number of wait states and programming delay” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency and the APB clock frequency is AHB frequency.

The parameters given in the following tables are derived from tests performed under supply voltage conditions summarized in *Table 20*, and, unless otherwise specified, at ambient temperature.

The maximum current consumption is given for LDO regulator ON and V_{DD} = 3.6 V. The typical current consumption is given for V_{DD} = 3V at ambient temperature.

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Table 27. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 2-way instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	250	30.8	33	57	70	-	mA
				215	26.7	29	50	63	-	
				200	24.5	26	47	59	-	
			VOS1	200	21.3	23	40	49	65	
				180	19.5	21	37	46	62	
				168	18.1	19	34	44	60	
				150	16.2	18	31	40	57	
			VOS2	150	14.8	16	28	36	49	
				100	10.3	11	21	28	42	
			VOS3	100	9.5	10	19	25	36	
				60	6.1	7	14	19	31	
				25	3.1	4	9	14	25	
		All peripherals enabled	VOS0	250	66.5	69	87	101	-	
				215	57.4	60	76	90	-	
				200	53.3	56	71	84	-	
			VOS1	200	46.5	49	61	72	86	
				180	42.3	44	56	66	81	
				150	35.1	37	47	57	72	
			VOS2	150	32.2	34	43	51	63	
				100	22.0	23	30	37	49	
			VOS3	100	20.1	21	27	33	47	
				60	12.7	14	18	23	36	
				25	6.0	7	11	15	27	

1. Evaluated by characterization - Not tested in production.

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Table 28. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 1-way instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	250	27.6	30	51	64	-	mA
				200	22.1	24	43	55	-	
			VOS1	200	19.1	21	36	46	64	
				180	17.7	19	34	43	58	
				150	14.6	16	29	38	54	
			VOS2	150	13.4	15	26	33	47	
				100	9.3	10	20	27	40	
			VOS3	100	8.5	9	17	23	35	
				25	2.8	4	9	14	25	

1. Evaluated by characterization - Not tested in production.

Table 29. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 1-way

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
I_{DD} (Run)	Supply current in Run mode	All peripherals disabled	VOS0	250	26.8	29	50	63	-	mA
				215	23.6	25	45	57	-	
				200	21.4	23	42	54	-	
			VOS1	200	18.6	20	35	45	60	
				180	17.1	19	33	52	58	
				150	14.1	15	28	37	53	
			VOS2	150	13.0	14	25	33	46	
				100	9.1	10	19	26	40	
			VOS3	100	8.3	9	17	23	34	
				60	5.4	6	13	18	29	
				25	2.8	3	9	14	25	

1. Evaluated by characterization - Not tested in production.

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Table 30. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 2-way

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	250	30.1	32	55	69	-	mA
				200	26.1	28	49	62	-	
				168	24.1	26	46	59	-	
			VOS1	150	20.8	22	39	48	64	
				100	19.1	21	36	46	62	
				250	17.6	19	34	43	59	
				200	15.8	17	31	40	56	
			VOS2	150	14.5	16	28	35	49	
				100	10.1	11	21	28	41	
			VOS3	250	9.2	10	19	25	36	
				200	6.0	7	14	19	30	
				168	3.0	4	9	14	25	

1. Evaluated by characterization - Not tested in production.

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Table 31. Typical consumption in Run mode with CoreMark running from flash memory and SRAM(1)

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Unit	Typ LDO	Unit
		Peripheral	Code					
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, instruction cache 2-way, prefetch ON	FLASH	250	30.8	mA	123.1	µA/MHz
				200	24.5		122.5	
				168	18.1		107.7	
				150	14.8		98.9	
				100	9.5		94.8	
		All peripherals disabled, instruction cache 1-way, prefetch ON	FLASH	250	27.6		110.4	
				200	19.1		95.4	
				150	13.4		89.4	
				100	8.5		85.3	
		All peripherals disabled, instruction cache 2-way	SRAM	250	30.1		120.5	
				200	20.8		103.9	
				168	17.6		104.8	
				150	14.5		97.0	
				100	9.2		92.4	
		All peripherals disabled, instruction cache 1-way	SRAM	250	26.8		107.3	
				200	18.6		92.8	
				150	13.0		86.8	
				100	8.3		82.6	

1. Evaluated by characterization - Not tested in production.

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Table 32. Typical consumption in Run mode with SecureMark running from flash memory and SRAM(1)

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Unit	Typ LDO	Unit
		Peripheral	Code					
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, instruction cache 2-way, prefetch ON	FLASH	250	32.8	mA	131.2	µA/MHz
				180	20.9		116.2	
				168	19.4		115.6	
				150	16.1		107.2	
				100	10.3		102.5	
		All peripherals disabled, instruction cache 1-way, prefetch ON	FLASH	250	30.0		120.0	
				180	19.1		106.4	
				168	17.9		106.3	
				150	14.7		98.3	
				100	9.5		94.6	

1. Evaluated by characterization - Not tested in production.

Table 33. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°	
$I_{DD(sleep)}$	Supply current in sleep mode	All peripherals disabled	VOS0	250	6.3	7	18	27	-	mA
				200	4.9	6	15	25	-	
			VOS1	200	4.2	5	12	20	35	
				180	4.1	5	12	20	35	
				168	3.6	4	12	19	35	
				150	3.3	4	11	18	34	
			VOS2	150	3.0	4	10	16	29	
				100	2.4	3	9	15	28	
			VOS3	100	2.2	3	8	13	24	
				60	1.7	2	7	12	23	

1. Evaluated by characterization - Not tested in production.

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Table 34. Typical and maximum current consumption in Stop mode

Symbol	Parameter	Conditions		Typ LDO	Max(1)				Unit
					T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
I_{DD} (stop)	Supply current in Stop	Flash memory in low power mode, SRAMs ON	SVOS3	0.26	0.79	6.34	11.45	22.31	mA
			SVOS4	0.19	0.59	5.05	9.21	18.13	
			SVOS5	0.15	0.43	3.97	7.42	14.99	
		Flash memory in normal mode, SRAMs ON	SVOS3	0.27	0.81	6.36	11.47	22.35	
			SVOS4	0.21	0.61	5.07	9.24	18.17	
		Flash memory in low power mode, SRAMs OFF except SRAM2 16 Kbytes ON	SVOS3	0.20	0.65	5.08	9.21	18.05	
			SVOS4	0.15	0.48	4.05	7.41	14.68	
			SVOS5	0.10	0.32	2.84	5.32	10.81	
		Flash memory in low power mode, SRAMs OFF except SRAM2 ON	SVOS3	0.21	0.70	5.49	9.93	19.42	
			SVOS4	0.16	0.52	4.37	7.99	15.79	
			SVOS5	0.16	0.36	3.20	5.98	12.12	

1. Evaluated by characterization - Not tested in production.

Table 35. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions		Typ(1)				Max(1)				Unit
		Backup RAM	RTC and LSE(2)	1.8 V	2.4 V	3 V	3.3 V	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 130 °C	
$I_{DD(standby)}$	Supply current in standby mode, IWDG OFF	OFF	OFF	2.6	2.8	3.0	3.2	4.3	8.8	16.5	42.6	µA
		ON	OFF	3.8	4.1	4.4	4.6	6.4	16.9	31.5	75.7	
		OFF	ON	2.9	3.2	3.5	3.7	5.3	10.0	17.8	44.6	
		ON	ON	4.2	4.5	4.9	5.1	7.4	18.1	32.8	77.7	

1. Evaluated by characterization - Not tested in production.
2. LSE is in medium-low drive mode.

Table 36. Typical and maximum current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ(1)				Max(1)				Unit
		Backup RAM	RTC and LSE(2)	1.62 V	2.4 V	3 V	3.3 V	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 130 °C	
$I_{DD(VBAT)}$	Supply current in V_{BAT} mode	OFF	OFF	0.01	0.01	0.02	0.02	0.2	2.0	4.9	14.9	µA
		ON	OFF	1.1	1.1	1.2	1.30	2.7	12.7	23.8	52.2	
		OFF	ON	0.5	0.5	0.5	0.6	1.2	3.2	6.2	16.9	
		ON	ON	1.6	1.6	1.6	1.8	3.7	13.9	25.1	54.2	

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1. Evaluated by characterization - Not tested in production.
2. LSE is in medium-low drive mode.

I/O system current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 57*.

To estimate the current consumption for the output pins, consider also external pull-downs or loads.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this current consumption can be avoided by configuring the I/Os in analog mode. This is notably the case of ADC input pins, to be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done by using pull-up/down resistors, or by configuring the pins in output mode.

In addition to the internal peripheral current consumption, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration
- All peripherals are disabled unless otherwise mentioned
- The I/O compensation cell is enabled
- f_{HCLK} is the CPU clock, $f_{PCLK} = f_{rcc_cpu_ck}$, and $f_{HCLK} = f_{rcc_cpu_ck}$.

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The given value is calculated by measuring the difference of current consumption:

- with all peripherals clocked off
- with only one peripheral clocked on
- $f_{rcc_cpu_ck}$ = 250 MHz (Scale 0), $f_{rcc_cpu_ck}$ = 200 MHz (Scale 1), $f_{rcc_cpu_ck}$ = 150 MHz (Scale 2), $f_{rcc_cpu_ck}$= 100 MHz (Scale 3)
- the ambient operating temperature is 25 °C and V_{DD} = 3.0 V

Table 37. Peripheral current consumption in Sleep mode

Bus	Peripheral	I_{DD} (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB1	SRAM1	0.82	0.71	0.67	0.59	µA/MHz
	BKPRAM	0.84	0.74	0.67	0.61	
	CRC	0.28	0.23	0.19	0.20	
	DCACHE	0.72	0.63	0.58	0.51	
	FLASH	9.62	8.41	7.66	6.99	
	GPDMA1	0.48	0.43	0.38	0.35	
	GPDMA2	0.75	0.67	0.6	0.55	
	GTZC1	0.98	0.85	0.79	0.71	
	ICACHE	0.78	0.67	0.62	0.56	
	RAMCFG	0.57	0.5	0.44	0.41	
	AHB1	0.43	0.4	0.36	0.34	

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Table 37. Peripheral current consumption in Sleep mode (continued)

Bus	Peripheral	I_{DD} (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB2	ADC12	2.16	1.89	1.73	1.56	µA/MHz
	DAC1	1.28	1.12	1.02	0.92	
	DCMI	3.41	3	2.75	2.51	
	GPIOA	0.06	0.05	0.05	0.05	
	GPIOB	0.05	0.05	0.06	0.05	
	GPIOC	0.04	0.04	0.04	0.03	
	GPIOD	0.07	0.07	0.06	0.04	
	GPIOE	0.1	0.06	0.08	0.05	
	GPIOF	0.11	0.07	0.08	0.06	
	GPIOG	0.06	0.03	0.04	0.02	
	GPIOH	0.05	0.05	0.04	0.02	
	HASH1	1.1	0.96	0.88	0.8	
	PKA	5.03	4.41	4.04	3.66	
	RNG1	0.87	0.76	0.71	0.64	
	SAES	6.2	5.81	5.57	5.5	
	SRAM2	1.29	1.12	1.05	0.95	
	SRAM3	0.68	0.6	0.54	0.48	
	AHB2	1.45	1.28	1.18	1.08	
AHB4	FMC	3.96	3.47	3.2	2.92	uA/MHz
	OSPI1	1.76	1.56	1.44	1.32	
	OTFDEC1	1.3	1.13	1.06	0.97	
	SDMMC1	9.07	7.97	7.31	6.66	
	AHB4	0.47	0.42	0.37	0.35	

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Table 37. Peripheral current consumption in Sleep mode (continued)

Bus	Peripheral	I_{DD} (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
APB1	CEC	0.15	0.12	0.12	0.12	µA/MHz
	CRS	0.26	0.22	0.21	0.21	
	FDCAN1	6.36	5.58	5.12	4.66	
	I2C1	0.54	0.47	0.45	0.42	
	I2C2	0.57	0.51	0.47	0.47	
	I3C1	0.29	0.27	0.25	0.24	
	LPTIM2	1.03	0.9	0.83	0.79	
	SPI2/I2S2	1.11	0.98	0.9	0.84	
	SPI3/I2S3	1.07	0.94	0.86	0.82	
	TIM12	1.35	1.19	1.09	1.03	
	TIM7	0.53	0.47	0.43	0.4	
	TIM6	0.53	0.47	0.42	0.4	
	TIM5	2.82	2.49	2.27	2.09	
	TIM4	2.41	2.13	1.94	1.79	
	TIM3	2.37	2.08	1.91	1.76	
	TIM2	2.79	2.45	2.24	2.05	
	DTS	1.54	1.33	1.23	1.15	
	UART4	1.16	1.03	0.93	0.88	
	UART5	1.15	1.02	0.92	0.88	
	UCPD1	1.14	0.98	0.9	0.85	
	USART2	1.28	1.13	1.04	0.96	
	USART3	1.29	1.14	1.06	0.98	
	USART6	1.27	1.13	1.02	0.97	
	WWDG1	1.41	0.29	0.27	0.25	
	APB1	0.32	1.26	1.14	1.03	
APB2	SPI1/I2S1	1.01	0.89	0.81	0.74	µA/MHz
	SPI4	1.06	0.94	0.86	0.77	
	TIM1	4.64	4.09	3.75	3.42	
	TIM15	2.41	2.14	1.96	1.78	
	TIM8	4.55	4	3.69	3.34	
	USART1	1.30	1.15	1.05	0.94	
	USBFS	2.48	2.17	1.99	1.78	
	APB2	0.68	0.59	0.53	0.51	

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Table 37. Peripheral current consumption in Sleep mode (continued)

Bus	Peripheral	I_{DD} (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
APB3	LPTIM1	0.93	0.82	0.73	0.65	uA/MHz
	LPUART1	0.86	0.77	0.68	0.61	
	RTCAPB	2.11	1.85	1.69	1.51	
	SBS	0.45	0.38	0.35	0.32	
	VREFBUF	0.09	0.09	0.05	0.04	
	I3C2	2.55	2.25	2.03	1.84	
	APB3	0.52	0.46	0.42	0.39	

Wake-up time from low-power modes

The times given in *Table 38* are measured starting from the wake-up event trigger up to the first instruction executed by the CPU:

- for Stop or Sleep modes: the wake-up event is WFE.
- WKUP (PA1) pin is used to wake-up from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.0 V.

Table 38. Low-power mode wake-up timings(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up time from Sleep mode	Instruction cache enabled	15	16	CPU clock cycles
		Instruction cache disabled	15	16	
t_{WUSTOP}	Wake-up time from Stop mode	SVOS3, HSI 64 MHz, flash memory in normal mode	4.0	4.8	µs
		SVOS3, HSI 64 MHz, flash memory in low-power mode	7.9	11.5	
		SVOS4, HSI 64 MHz, flash memory in normal mode	13.8	16.0	
		SVOS4, HSI 64 MHz, flash memory in low-power mode	17.7	21.9	
		SVOS5, HSI 64 MHz, flash memory in low-power mode	31.4	36.8	
		SVOS3, CSI 4 MHz, flash memory in normal mode	25.5	31.0	
		SVOS3, CSI 4 MHz, flash memory in low power mode	27.7	34.2	
		SVOS4, CSI 4 MHz, flash memory in normal mode	35.3	40.8	
		SVOS4, CSI 4 MHz, flash memory in low-power mode	37.5	44.0	
		SVOS5, CSI 4 MHz, flash memory in low-power mode	51.2	58.9	
t_{WUSTBY}	Wake-up time from Standby mode	VCAP capacitors discharged	506.0	653.6	

1. Evaluated by characterization - Not tested in production.

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5.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the *Table 39* in addition to *Table 57*. The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0481).

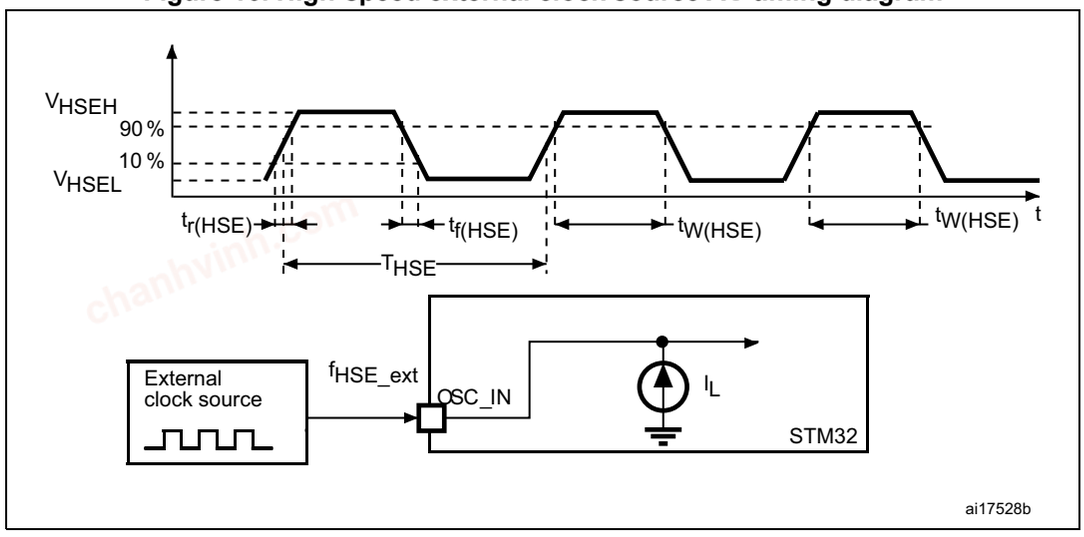
Table 39. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	External digital/analog clock	4	25	50	MHz
V_{HSEH}	Digital OSC_IN input high-level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input low-level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}/t_{w(HSEL)}$ (2)	Digital OSC_IN input high or low time	External digital clock	7	-	-	ns
$V_{isw(HSEH)}$ (V_{HSEH} -V_{HSEH})(3)	Analog low-swing OSC_IN peak-to-peak amplitude	External analog low swing clock	0.2	-	2/3 V_{DD}	V
$DuCy_{HSE}$	Analog low-swing OSC_IN duty cycle		45	50	55	%
$t_{r(HSE)}/t_{f(HSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low swing clock, 10% to 90%	0.05 / f_{HSE_ext}	-	0.3 / f_{HSE_ext}	ns

1. Specified by design - Not tested in production..
2. The rise and fall times for a digital input signal are not specified, but the V_{HSEH} and V_{HSEL} conditions must be fulfilled anyway.
3. The DC component of the signal must ensure that the signal peaks are located between V_{DD} and V_{SS}.

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Figure 16. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the *Table 40* in addition to *Table 57*. The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0481).

Table 40. Low-speed external user clock characteristics(1)

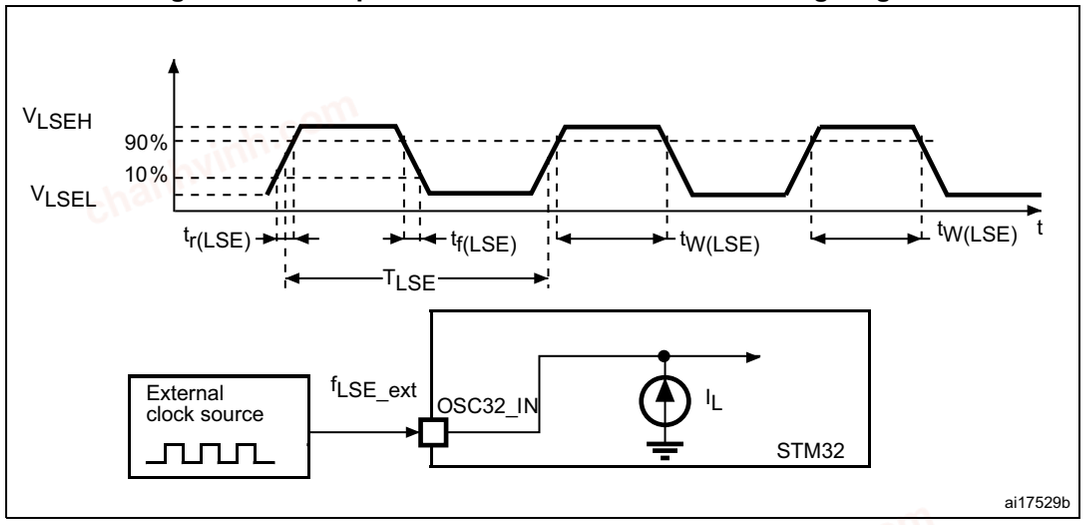
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	External digital/analog clock	-	32.768	1000	kHz
V_{LSEH}	Digital OSC32_IN input high-level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	Digital OSC32_IN input low-level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(LSEH)}/t_{w(LSEL)}$	Digital OSC_IN input high or low time	External digital clock	250	-	-	ns
V_{isw_H}	Analog low-swing OSC_IN high-level voltage	External analog low swing clock	0.6	-	1.225	V
V_{isw_L}	Analog low-swing OSC_IN low-level voltage		0.35	-	0.8	
V_{iswLSE} (V_{LSEH} -V_{LSEL})	Analog low-swing OSC_IN peak-to-peak amplitude		0.5	-	0.875	
$DuCy_{LSE}$	Analog low-swing OSC_IN duty cycle		45	50	55	%
$t_{r(LSE)}/t_{f(LSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low swing clock, 10% to 90%	-	100	200	ns

1. Specified by design - Not tested in production.

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Note: For information on selecting the crystal, refer to AN2867 “Oscillator design guide for ST microcontrollers” available from www.st.com.

Figure 17. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator.

All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. 4-50 MHz HSE oscillator characteristics(1)

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	50	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	10	mA
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 4 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 20 Ω, CL = 10 pF at 16 MHz	-	0.55	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 32 MHz	-	0.67	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 48 MHz	-	1.17	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

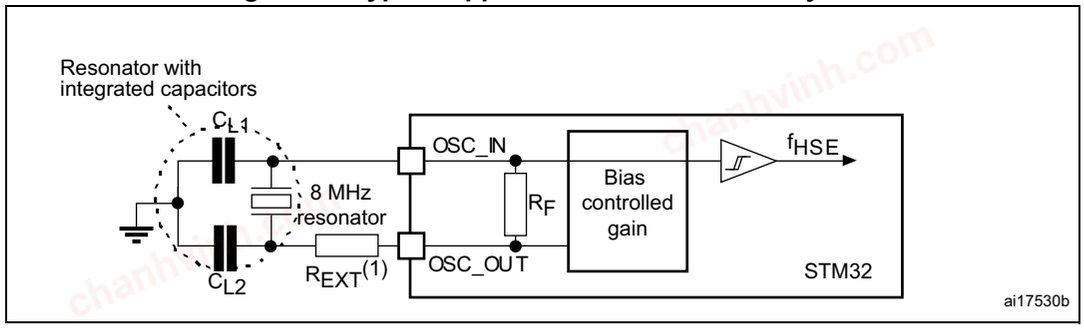
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1. Evaluated by design - Not tested in production.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 to 20 pF range (typical), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 18*). C_{L1} and C_{L2} usually have the same size. The crystal manufacturer typically specifies a load capacitance, which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate for the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to AN2867 “Oscillator design guide for ST microcontrollers”, available from www.st.com.

Figure 18. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph is based on design simulation results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 42. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 01 Medium low drive capability	-	333	-	nA
		LSEDRV[1:0] = 10 Medium high drive capability	-	462	-	
		LSEDRV[1:0] = 11 High drive capability	-	747	-	

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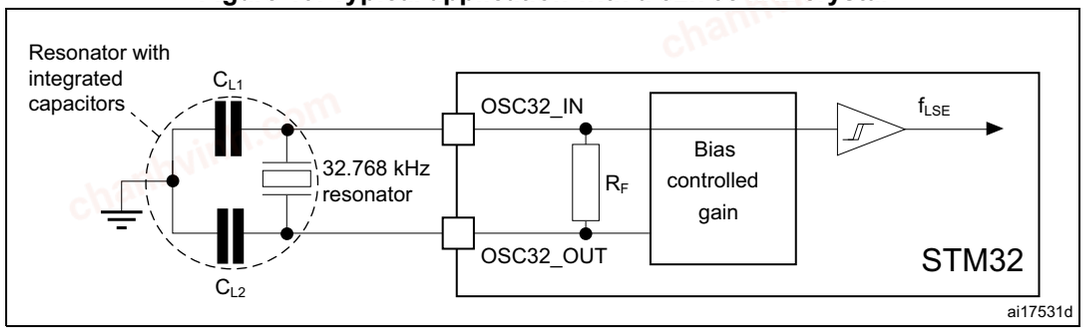
Table 42. Low-speed external user clock characteristics(1) (continued)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	µA/V
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Specified by design - Not tested in production.
2. Refer to the note and caution paragraphs below the table, and to AN2867 "*Oscillator design guide for ST microcontrollers*".
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to when a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to AN2867 "Oscillator design guide for ST microcontrollers", available from www.st.com.

Figure 19. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

5.3.8 Internal clock source characteristics

The parameters given in *Table 43* to *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

48 MHz high-speed internal RC oscillator (HSI48)

Table 43. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD} = 3.3 V, T_J= 30 °C	47.5(1)	48	48.5(1)	MHz
TRIM(3)	User trimming step	-	-	0.175	0.250	%
USER TRIM COVERAGE(2)	User trimming coverage	±32 steps	±4.70	±5.6	-	
DuCy(HSI48)(3)	Duty cycle	-	45	-	55	%

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Table 43. HSI48 oscillator characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ACCHSI48_REL(3)	Accuracy of the HSI48 oscillator over temperature (reference is 30 °C)	T_J = -40 to 130 °C	-4.5	-	4	%
Δ_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD} (reference is 3.3 V)	V_{DD} = 3.0 to 3.6 V	-	0.025	0.05	%
		V_{DD} = 1.71 to 3.6 V	-	0.05	0.1	
t_{su}(HSI48)(3)	HSI48 oscillator start-up time	-	-	2.1	4.0	µs
I_{DD}(HSI48)(3)	HSI48 oscillator power consumption	-	-	350	400	µA
N_T jitter(3)	Next transition jitter accumulated jitter on 28 cycles	-	-	±0.15	-	ns
P_T jitter(3)	Paired transition jitter accumulated jitter on 56 cycles(4)	-	-	±0.25	-	

1. Calibrated during manufacturing tests.
2. Evaluated by characterization - Not tested in production.
3. Specified by design - Not tested in production.
4. Jitter measurements are performed without clock sources activated in parallel.

64 MHz high-speed internal RC oscillator (HSI)

Table 44. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.3 V, T_J = 30 °C	63.7(2)	64.0(2)	64.3(2)	MHz
TRIM	User trimming step	Trimming is not a multiple of 32(3)	-	0.24	0.32	%
		Trimming is 128, 256, and 384(3)	-5.2	-1.8	-	
		Trimming is 64, 192, 320, and 488(3)	-1.4	-0.8	-	
		Other trimmings are multiples of 32 (not including multiples of 64 and 128)(3)	-0.6	-0.25	-	
DuCy(HSI)	Duty cycle	-	45	-	55	%
Δ_{VDD}(HSI)	Frequency drift with V_{DD} (reference is 3.3 V)	V_{DD}= 1.71 to 3.6 V	-0.12	-	0.03	%
Δ_{TEMP}(HSI)	Frequency drift over temperature (reference is 64 MHz)	T_J= -20 to 105 °C	-1(4)	-	1(4)	
		T_J= -40 to 130 °C	-2(4)	-	1(4)	
t_{su}(HSI)	Start-up time	-	-	1.4	2.0	µs
t_{stab}(HSI)	Stabilization time	At 1% of target frequency	-	4	8	µs
		At 1% of target frequency	-	-	4	
I_{DD}(HSI)	Power consumption	-	-	300	450	µA

1. Specified by design - Not tested in production, unless otherwise specified.
2. Calibrated during manufacturing tests.
3. Trimming value of HSICAL[8:0.]
4. Guaranteed by characterization - Not tested n production.

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4 MHz low-power internal RC oscillator (CSI)

Table 45. CSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}	Frequency	V_{DD} = 3.3 V, T_J = 30 °C	3.96(2)	4	4.04(2)	MHz
TRIM	User trimming step	Trimming is not a multiple of 16	-	0.40	0.75	%
		Trimming is not a multiple of 32	-4.75	-2.75	0.75	
		Other trimmings are a multiple of 32 (not including multiples of 64 and 128)	-0.43	0.00	0.75	
DuCy(CSI)	Duty cycle	-	45	-	55	%
Δ_{TEMP}(CSI)	Frequency drift over temperature	T_J= 0 to 85 °C	-3.7(3)	-	4.5(3)	%
		T_J= -40 to T_J = 130 °C	-11(3)	-	7.5(3)	%
Δ_{VDD}(CSI)	Frequency drift over V_{DD}	V_{DD}= 1.71 to 3.6 V	-0.06	-	0.06	%
t_{su}(CSI)	Start-up time	-	-	1	2	µs
t_{stab}(CSI)	Stabilization time (to reach ± 3% of f_{CSI})	-	-	-	4	cycle
I_{DD}(CSI)	Power consumption	-	-	23	30	µA

1. Specified by design - Not tested in production, unless otherwise specified.
2. Calibrated during manufacturing tests.
3. Evaluated by characterization - Not tested in production.

Low-speed internal (LSI) RC oscillator

Table 46. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	V_{DD} = 3.3 V, T_J = 25 °C	31.4(1)	32	32.6(1)	kHz
		T_J = -40 to 110 °C, V_{DD} =1.71 to 3.6 V	29.76(2)	-	33.6(2)	
		T_J = -40 to 130 °C, V_{DD} =1.71 to 3.6 V	29.4(2)	-	33.6(2)	
t_{su}(LSI)(3)	Start-up time	-	-	80	130	µs
t_{stab}(LSI)(3)	Stabilization time (5% of final value)	-	-	120	170	
I_{DD}(LSI)(3)	Power consumption	-	-	130	280	nA

1. Calibrated during manufacturing tests.
2. Evaluated by characterization - Not tested in production.
3. Specified by design - Not tested in production.

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5.3.9 PLL characteristics

The parameters given in *Table 47* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 47. PLL characteristics (wide VCO frequency range)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P, Q, R	VOS0		1	-	250(2)	MHz
		VOS1		1	-	200(2)	
		VOS2		1	-	150(2)	
		VOS3		1	-	100(2)	
f_{VCO_OUT}	PLL VCO output	-		128	-	560(2)	
t_{LOCK}	PLL lock time	Normal mode		-	45	100(3)	µs
		Sigma-delta mode (f_{PLL_IN} ≥ 8 MHz)		-	60	120(3)	
Jitter	Cycle-to-cycle jitter	f_{VCO_OUT} = 128 MHz		-	60	-	±ps
		f_{VCO_OUT} = 200 MHz		-	50	-	
		f_{VCO_OUT} = 400 MHz		-	20	-	
		f_{VCO_OUT} = 560 MHz		-	15	-	
	Long term jitter	Normal mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz		-	±0.2	-	%
		Normal mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz		-	±0.8	-	
		Sigma-delta mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz		-	±0.2	-	
		Sigma-delta mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz		-	±0.8	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}	f_{VCO_OUT} = 560 MHz	V_{DD}	-	330	420	µA
			V_{CORE}	-	630	-	
		f_{VCO_OUT} = 128 MHz	V_{DD}	-	155	230	
			V_{CORE}	-	170	-	

1. Specified by design - Not tested in production, unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Evaluated by characterization - Not tested in production.

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Table 48. PLL characteristics (medium VCO frequency range)

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS0		1.17	-	210	MHz
		VOS1		1.17	-	210	
		VOS2		1.17	-	160(2)	
		VOS3		1.17	-	88(2)	
f_{VCO_OUT}	PLL VCO output	-		150	-	420	
t_{LOCK}	PLL lock time	Normal mode		-	45	80(3)	µs
		Sigma-delta mode		Forbidden			
Jitter	Cycle-to-cycle jitter	f_{VCO_OUT} = 150 MHz	-	-	60	-	±ps
		f_{VCO_OUT} = 200 MHz	-	-	40	-	
		f_{VCO_OUT} = 400 MHz	-	-	18	-	
		f_{VCO_OUT} = 420 MHz	-	-	15	-	
	Period jitter	f_{VCO_OUT} = 150 MHz	f_{PLL_OUT} = 50 MHz	-	75	-	
		f_{VCO_OUT} = 400 MHz		-	25	-	
	Long term jitter	Normal mode f_{VCO_OUT} = 400 MHz		-	±0.2	-	%
I_{DD}(PLL)	PLL power consumption on V_{DD}	f_{VCO_OUT} = 420 MHz	V_{DD}	-	275	360	µA
			V_{CORE}	-	450	-	
		f_{VCO_OUT} = 150 MHz	V_{DD}	-	160	240	
			V_{CORE}	-	165	-	

1. Specified by design - Not tested in production, unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Evaluated by characterization - Not tested in production.

5.3.10 Memory characteristics

Flash memory

The characteristics are given at T_J = -40 to 130 °C unless otherwise specified.

The devices are shipped to customers with the flash memory erased.

Table 49. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
I_{DD}	Supply current	Word program(2)	-	2.5	3.6	mA
		Sector erase	-	1.8	4	
		Mass erase	-	2.0	4	

1. Specified by design - Not tested in production

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2. Data is evaluated with a write of 50% of the programmed bits equal to 0.

Table 50. Flash memory programming(1)

Symbol	Parameter	Conditions	Min(2)	Typ	Max(2)	Unit
t_{prog}	Word program time	128 bits (user area)	-	32	100	µs
		16 bits (OTP area)	-	32	100	
t_{ERASE}	Sector erase time (8 Kbytes)	-	-	2	10	ms
t_{ME}	Mass erase time		-	0.52	2.6	s
V_{prog}	Programming voltage		1.71	-	3.6	V

1. Data are valid for program memory and high-cycling data memory.
2. Specified by design - Not tested in production.

Table 51. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{PEND}	Endurance program memory	T_J = -40 to +130 °C	10	kcycles
N_{DEND}	Endurance data memory	T_J = -40 to +130 °C	100	
t_{PRET}	Program memory, data retention	1 kcycle at T_A = 125 °C	10	Years
		1 kcycles at T_A = 85 °C	30	
		10 kcycles at T_A = 55 °C	30	
t_{DRET}	Data retention for data memory	100 kcycle at T_A = 125 °C	1	
		100 kcycles at T_A = 85 °C	10	
		100 kcycles at T_A = 55 °C	10	

1. Evaluated by characterization - Not tested in production, unless otherwise specified.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD),** positive and negative, is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows to resume normal operation.

The test results are given in *Table 52*. They are based on the EMS levels and classes defined in AN1709 "*EMC design guide for STM8, STM32 and legacy MCUs*".

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Table 52. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to apply on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, LQFP144, $f_{rcc_cpu_ck}$ = 250 MHz, conform to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst limits to apply through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, LQFP144, $f_{rcc_cpu_ck}$ = 250 MHz, conform to IEC 61000-4-4	5A

As a consequence, it is recommended to add a serial resistor (1 kΩ), located as close as possible to the MCU, to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (such as control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or on the oscillator pins for 1 s.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015 *“Software techniques for improving microcontrollers EMC performance”).*

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard, which specifies the test board and the pin loading.

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Table 53. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/250 MHz	
S_{EMI}	Peak level(1)	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package, conforming to IEC61967-2	0.1 to 30 MHz	8	dBµV
			30 to 130 MHz	0	
			130 MHz to 1 GHz	24	
			1 GHz to 2 GHz	18	
			EMI level	4	-

1. Refer to the EMI radiated test chapter of application note AN1709 “EMC design guide for STM8, STM32 and Legacy MCUs” available from the ST website www.st.com.

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive pulse followed by a negative one) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 54. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C conforming to ANSI/ESDA/JEDEC JS-001	All packages	1C	1000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All packages	C2a	500	

1. Evaluated by characterization - Not tested in production.
2. The electrostatic discharge is 2000 V for all pins, except for NRST, PB13 and PB14 for which the test fails at 2000 V and passes at 1400 V.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

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Table 55. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_J = 130 °C, conforming to JESD78	II level A

5.3.13 I/O current injection characteristics

As a general rule, avoid current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) during the normal product operation. To give an indication of the device robustness when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the characterization.

Functional susceptibility to I/O current injection

While a simple application is executed, the device is stressed by injecting current into the I/O pins (one at the time) programmed in floating input mode, and checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits (-5 / +0 µA range) of induced leakage current on adjacent pins, or other functional failures (such as reset, oscillator frequency deviation).

Table 56 shows I/Os current injection susceptibility data. Negative/positive induced leakage currents are caused, respectively, by negative/positive injection.

Table 56. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on pins PC14, PC15, PB6, PB8, PE8	0	0	mA
	Injected current on PB5, PB8, PC5, PD10, PE4, PF6, PH1	5	0	
	Injected current on PA4, PA5, PB2, PD8	0	N/A	
	Injected current on all other pins	5	N/A	

1. Evaluated by characterization - Not tested in production.

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the conditions summarized in *Table 20*. All I/Os are CMOS and TTL compliant (except for BOOT0).

Note: For information on GPIO configuration, refer to AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption”, available on www.st.com.

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Table 57. I/O static characteristics(1)

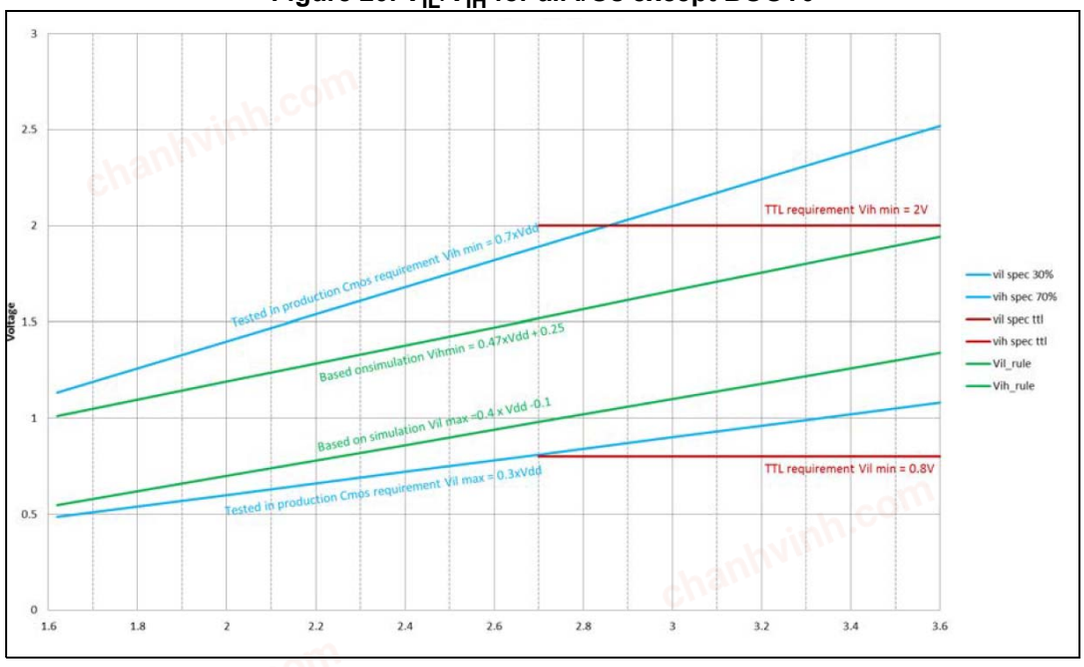
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage except BOOT0	1.08 V < V_{DD} < 3.6 V	-	-	0.3 V_{DDIOx}(2)	V
	I/O input low level voltage except BOOT0		-	-	0.4 V_{DDIOx} - 0.1(3)	
	BOOT0 I/O input low level voltage		-	-	0.19 V_{DDIOx} + 0.1(3)	
V_{IH}	I/O input high level voltage except BOOT0	1.08 V < V_{DD} < 3.6 V	0.7 V_{DDIOx}(2)	-	-	V
	I/O input high level voltage except BOOT0		0.52 V_{DDIOx} + 0.18(3)	-	-	
	BOOT0 I/O input high level voltage		0.17 V_{DDIOx} + 0.6(3)	-	-	
V_{HYS}(3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.08 V < V_{DD} < 3.6 V	-	250	-	mV
	BOOT0 I/O input hysteresis	1.71 V < V_{DD} < 3.6 V	-	200	-	
I_{leak}(4)	FT_xx Input leakage current(3)	0 < V_{IN} ≤ Max(V_{DDXXX})(7)	-	-	±200	nA
		Max(V_{DDXXX}) < V_{IN} ≤ Max(V_{DDXXX})+ 1 V) (5)(7)	-	-	2500	
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(7)	-	-	750	
	TT_xx Input leakage current	0< V_{IN} ≤ Max(V_{DDXXX}) (7)	-	-	±200	
	BOOT0	0< V_{IN} ≤ V_{DDOX}	-	-	15	
R_{PU}	Weak pull-up equivalent resistor(6)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	V_{IN} = V_{DD}(7)	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DDIOx} represents V_{DD} or V_{DDIO2}.
2. Compliant with CMOS requirements.
3. Specified by design - Not tested in production.
4. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_leak_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x $I_{lkg(Max)}$.
5. V_{IN} must be lower than Max(V_{DDXXX}) + 3.6 V.
6. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10%).
7. Max(V_{DDXXX}) is the maximum value of all the I/O supplies.

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All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 20*.

Figure 20. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 18*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 18*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 58* and *Table 60* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*. All I/Os are CMOS and TTL compliant.

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Table 58. Output voltage characteristics for all I/Os except PC13, PC14, and PC15

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port[2], I_{IO} = 8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[2], I_{IO} = -8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}– 0.4	-	
V_{OL}[3]	Output low level voltage	TTL port[2], I_{IO} = 8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[3]	Output high level voltage	TTL port[2], I_{IO} = -8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}[3]	Output low level voltage	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}[3]	Output high level voltage	I_{IO} = -20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 1.3	-	
V_{OL}[3]	Output low level voltage	I_{IO} = 4 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH} [3]	Output high level voltage	I_{IO} = -4 mA 1.71 V ≤ V_{DD} <3.6 V	V_{DD} - 0.4	-	
V_{OL}[3]	Output low level voltage	I_{IO} = 2 mA 1.08 V ≤ V_{DD} ≤ 1.32 V	-	0.3 V_{DDIO2}	
V_{OH} [3]	Output high level voltage	I_{IO} = -2 mA 1.71 V ≤ V_{DD} < 1.32 V	0.7 V_{DDIO2}	-	
V_{OLFM+}[3]	Output low level voltage for an FTf I/O pin in (FT I/O with “f” option)	I_{IO} = 20 mA 2.3 V≤ V_{DD} ≤3.6 V	-	0.4	
		I_{IO} = 10 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 4.5 mA 1.08 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 17*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

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Table 59. Output voltage characteristics for FT_c I/Os (PB13/PB14)

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port[2], I_{IO} = 2 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[2], I_{IO} = -2 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}– 0.4	-	
V_{OL}[3]	Output low level voltage	TTL port[2], I_{IO} = 2 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[3]	Output high level voltage	TTL port[2], I_{IO} = -2 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}[3]	Output low level voltage	I_{IO} = 1 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[3]	Output high level voltage	I_{IO} = -1 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	
V_{OL}[3]	Output low level voltage	I_{IO} = 0.1 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH} [3]	Output high level voltage	I_{IO} = -0.1 mA 1.71 V ≤ V_{DD} < 3.6 V	V_{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 17*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 60. Output voltage characteristics for PC13[1]

Symbol	Parameter	Conditions[3]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port[2], I_{IO} = 3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[2], I_{IO} = -3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	
V_{OL}[3]	Output low level voltage	TTL port[2], I_{IO} = 3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[3]	Output high level voltage	TTL port[2], I_{IO} = -3 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}[3]	Output low level voltage	I_{IO} = 1.5 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[3]	Output high level voltage	I_{IO} = −1.5 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 17*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

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Table 61. Output voltage characteristics for PC14 and PC15(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2), I_{IO} = 0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2), I_{IO} = -0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2), I_{IO} = 0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2), I_{IO} = -0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 0.25 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	I_{IO} = -0.25 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 17*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of GPIOx_HSLVR register can be used to optimize the I/O speed when the voltage is below 2.7 V.

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Table 62. Output timing characteristics (HSLV OFF)(1)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F_{max}(2)(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	8	MHz
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	14	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	16	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5	
	t_r/t_f(4)(5)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	18.0	ns
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	36.0	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17.0	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	34.0	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	15.5	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	32.0	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	14.2	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	30.0	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.2	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	27	

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Table 62. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	F_{max}(2)(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V		40	MHz
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	12	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	45	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	14	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	16	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	18	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	60	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	20	
	t_r/t_f(4)(5)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	6.2	ns
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	11.4	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.7	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	10.5	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.1	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	9.5	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.5	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V		8.4	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V		3.7	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V		7.0	

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Table 62. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	F_{max}(2)(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	80	MHz
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	30	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	90	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	35	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	40	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	110	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	45	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	133	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	50	
	t_r/t_f(4)(5)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.8	ns
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	7.5	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.4	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	6.6	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.9	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5.7	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.5	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	4.7	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.9	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3.7	

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Table 62. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
11	F_{max}(2)(3)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	MHz
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	40	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	120	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	50	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	140	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	60	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	166	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	70	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	200	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	80	
	t_r/t_f(4)(5)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	6.3	
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.8	
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5.5	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.3	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	4.6	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.9	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3.7	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.4	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the conditions (t_r + t_f) ≤ 2/3 T, Skew ≤ 1/20 T, and 45% < Duty cycle < 55%.
3. When 2 V < V_{DD} < 2.7 V the maximum frequency is between values given for V_{DD} = 1.98 V and V_{DD} = 2.7 V.
4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
5. When 2 V < V_{DD} < 2.7 V the maximum t_{rise}/t_{fall} is between values given for V_{DD} = 1.98 V and V_{DD} = 2.7 V.

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Output buffer timing characteristics (HSLV option enabled)

Table 63. Output timing characteristics (HSLV ON)(1)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	8	MHz
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	10	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	12	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	14	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	16	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	17.8	ns
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	15.8	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	14.4	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	13.1	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	11.4	
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	40	MHz
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	45	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	50	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	55	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	60	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	7.2	ns
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	6.5	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5.6	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	4.8	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3.8	
10	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	60	MHz
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	70	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	90	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	110	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	140	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5.3	ns
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	4.6	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3.8	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3.0	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	2.2	

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Table 63. Output timing characteristics (HSLV ON)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
11	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	67	MHz
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	100	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	120	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	155	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	200	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	5.0	ns
			C = 40 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	4.1	
			C = 30 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	3.3	
			C = 20 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	2.5	
			C = 10 pF, 1.71 V ≤ V_{DD} ≤ 2 V	-	1.8	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the conditions: (t_r+t_f) ≤ 2/3 T, Skew ≤ 1/20 T, 45% < Duty cycle < 55%.
3. The fall and rise times are defined, respectively, between 90 and 10% and between 10 and 90% of the output waveform.
4. Compensation system enabled.

Table 64. Output timing characteristics V_{DDIO2} 1.2 V range (HSLV OFF)(1)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	1	MHz
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	1	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	1	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	1	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	1	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	83.0	ns
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	79.0	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	46.0	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	72.0	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	68.0	

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Table 64. Output timing characteristics V_{DDIO2} 1.2 V range (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	MHz
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	24.5	ns
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	22.2	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	20.0	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	17.8	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	15.0	
10	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	10	MHz
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	10	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	10	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	10	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	10	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	16.2	ns
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	14.3	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	12.2	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	10.0	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	7.9	
11	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	20	MHz
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	23	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	25	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	28	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	30	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	14.0	ns
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	12.0	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	10.0	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	8.0	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	6.0	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the conditions: (t_r+t_f) ≤ 2/3 T, Skew ≤ 1/20 T, 45% < Duty cycle < 55%.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

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Table 65. Output timing characteristics V_{DDIO2} 1.2 V (HSLV ON)(1)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	MHz
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	32.5	ns
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	30.0	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	27.5	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	25.0	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	22.5	
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	15.0	MHz
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	17.5	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	20.0	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	22.5	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	25.0	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	14.6	ns
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	12.9	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	11.2	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	9.3	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	7.3	
10	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	25	MHz
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	30	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	33	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	44	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	55	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	11.6	ns
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	9.7	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	7.8	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	6.1	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	4.3	

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Table 65. Output timing characteristics V_{DDIO2} 1.2 V (HSLV ON)(1) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
11	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	30	MHz
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	35	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	44	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	55	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	77	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	11.1	ns
			C = 40 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	9.2	
			C = 30 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	7.2	
			C = 20 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	5.4	
			C = 10 pF, 1.08 V ≤ V_{DDIO2} ≤ 1.32 V	-	3.6	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the conditions: (t_r+t_f) ≤ 2/3 T, Skew ≤ 1/20 T, 45%<Duty cycle<55%.
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Table 66. Output timing characteristics for FT_c I/Os (PB13/PB14)(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F_{max}	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DDIO} ≤ 3.6 V	-	2	MHz
			C = 50 pF, 1.71 V ≤ V_{DDIO} < 2.7 V	-	1	
	t_r/t_f	Output rise and fall time	C = 50 pF, 2.7 V ≤ V_{DDIO} < 3.6 V	-	166	ns
			C = 50 pF, 1.71 V ≤ V_{DDIO} < 2.7 V	-	330	
01	F_{rmax}	Maximum frequency	C = 30 pF, 2.7 V ≤ V_{DDIO} < 3.6 V	-	10	MHz
			C = 30 pF, 1.71 V ≤ V_{DDIO} < 2.7 V	-	4	
	t_r/t_f	Output rise and fall time	C = 30 pF, 2.7 V ≤ V_{DDIO} < 3.6 V	-	33	ns
			C = 30 pF, 1.71 V ≤ V_{DDIO} < 2.7 V	-	65	

1. Specified by design - Not tested in production.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the product reference manual for a description of GPIO port configuration register.

5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 57*).

Unless otherwise specified, the parameters in *Table 67* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

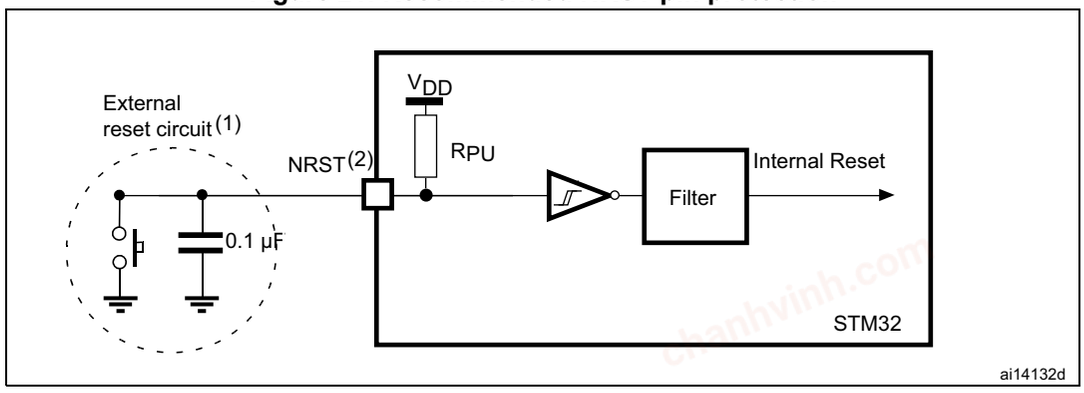
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Table 67. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST input not filtered pulse	1.71 V < V_{DD} < 3.6 V	350	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. The PMOS contribution to the series resistance is minimum (~10 % order).
2. Specified by design - Not tested in production.

Figure 21. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 57*, otherwise the reset is not taken into account by the device.

5.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length to ensure its detection by the event controller.

Table 68. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Specified by design - Not tested in production.

5.3.17 FMC characteristics

Unless otherwise specified, the parameters given in tables *69* to *82* are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 20*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V
- VOS level set to VOS0

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Refer to *Section 5.3.14* for more details on the input/output alternate function characteristics.

Asynchronous waveforms and timings

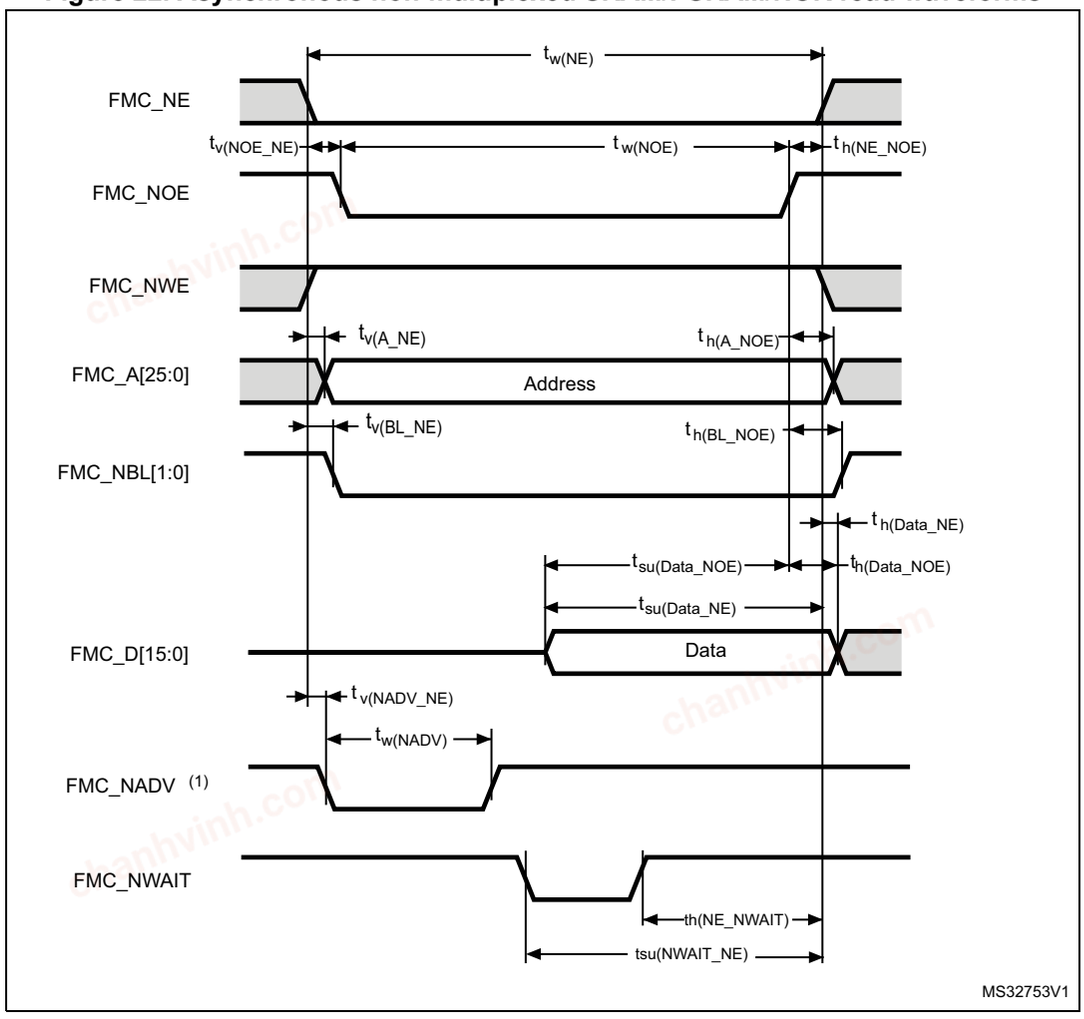
Figures *22* through *24* represent asynchronous waveforms, tables *69* through *76* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- DataHoldTime(DATAHLD) = 0x1 (1 Tfmc_ker_ck for read operations and 2 Tfmc_ker_ck for write operations)
- ByteLaneSetup(NBLSET)=0x1
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all timing tables, the $T_{fmc_ker_ck}$ is the f_{HCLK} clock period.

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Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

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Table 69. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3\ T_{fmc_ker_ck} - 1$	$3\ T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2\ T_{fmc_ker_ck} - 1$	$2\ T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$2\ T_{fmc_ker_ck} - 1.5$	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} + 11.5$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	11.5	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 1$	

1. Evaluated by characterization - Not tested in production.

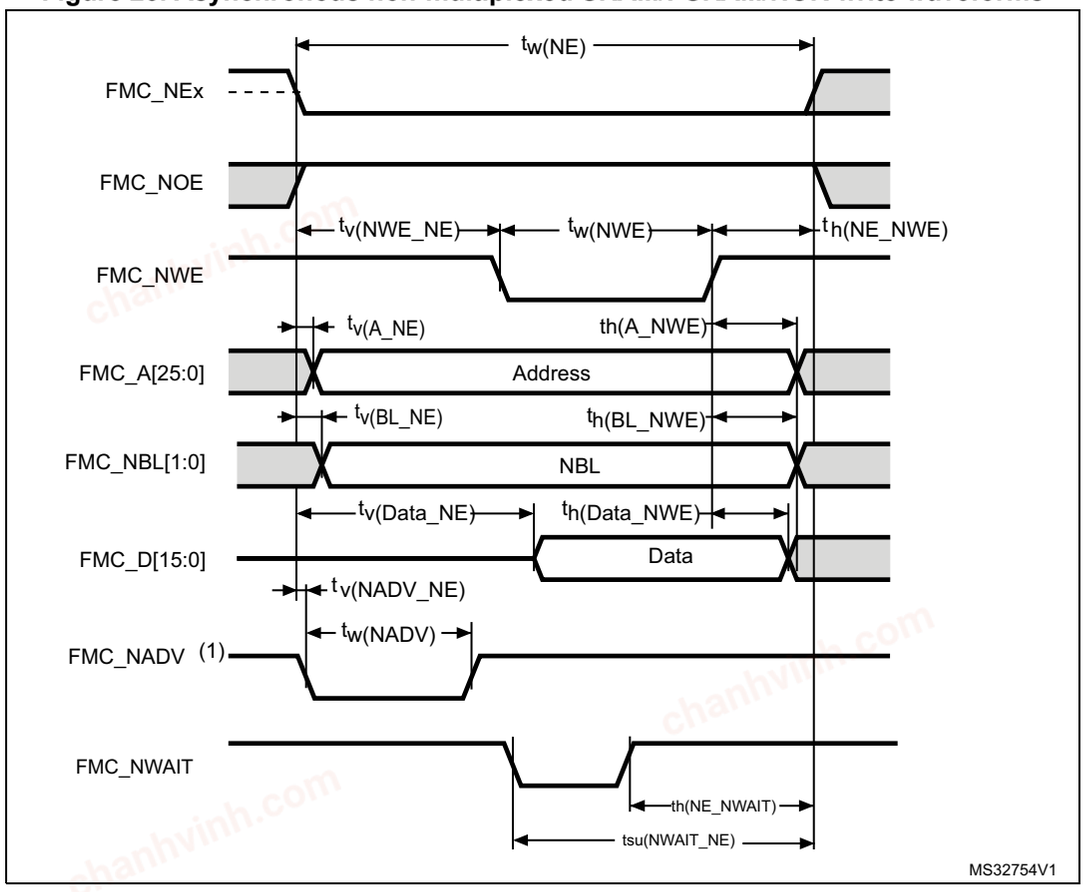
Table 70. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8\ T_{fmc_ker_ck} - 1$	$8\ T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$7\ T_{fmc_ker_ck} - 1$	$7\ T_{fmc_ker_ck} + 1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck}$	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5\ T_{fmc_ker_ck} + 10$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4\ T_{fmc_ker_ck} + 10$	-	

1. Evaluated by characterization - Not tested in production.
2. N_{WAIT} pulse width is equal to one fmc_ker_ck cycle.

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Figure 23. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 71. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3 $T_{fmc_ker_ck}$ - 1	3 $T_{fmc_ker_ck}$ + 1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck}$ - 1	$T_{fmc_ker_ck}$+ 0.5	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck}$ - 1	$T_{fmc_ker_ck}$ +1	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck}$ - 1	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck}$ -1	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck}$ -1	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{fmc_ker_ck}$ + 1	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck}$	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck}$ + 1	

1. Evaluated by characterization - Not tested in production.

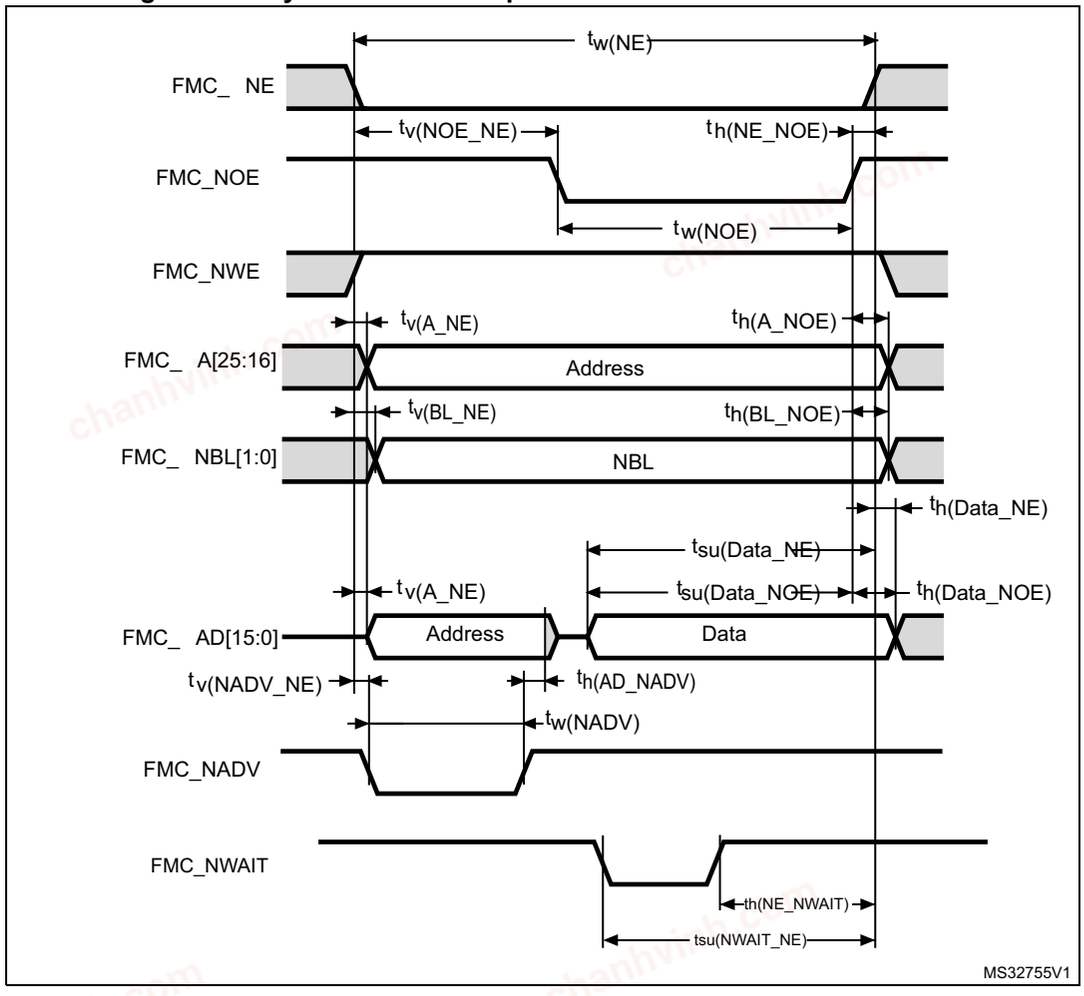
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Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8 $T_{fmc_ker_ck}$ - 1	8 $T_{fmc_ker_ck}$ + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	6 $T_{fmc_ker_ck}$ - 1	6 $T_{fmc_ker_ck}$ + 1	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	5 $T_{fmc_ker_ck}$ + 10	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4 $T_{fmc_ker_ck}$ + 10	-	

1. Evaluated by characterization - Not tested in production.
2. N_{WAIT} pulse width is equal to one fmc_ker_ck cycle.

Figure 24. Asynchronous multiplexed PSRAM/NOR read waveforms



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Table 73. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4\ T_{fmc_ker_ck} - 1$	$4\ T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2\ T_{fmc_ker_ck} - 1$	$2\ T_{fmc_ker_ck} + 0.5$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 0.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$2\ T_{fmc_ker_ck} - 0.5$	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} + 11.5$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	11.5	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Evaluated by characterization - Not tested in production.

Table 74. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9\ T_{fmc_ker_ck} - 1$	$9\ T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NOE low time	$6\ T_{fmc_ker_ck} - 1$	$6\ T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5\ T_{fmc_ker_ck} + 10$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4\ T_{fmc_ker_ck} + 10$	-	

1. Evaluated by characterization - Not tested in production.
2. NWAIT pulse width is equal to one fmc_ker_ck cycle.

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Table 75. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4\ T_{fmc_ker_ck}$ -1	$4\ T_{fmc_ker_ck}$ +1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck}$ - 1	$T_{fmc_ker_ck}$ +0.5	
$t_{w(NWE)}$	FMC_NWE low time	$2\ T_{fmc_ker_ck}$ - 1	$2\ T_{fmc_ker_ck}$ + 1	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck}$ - 0.5	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck}$ - 1	$T_{fmc_ker_ck}$ + 1	
$t_{h(AD_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high	$T_{fmc_ker_ck}$ - 1	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck}$ - 1	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck}$ - 1	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data_NADV)}$	Data hold time after FMC_NEx high	-	$T_{fmc_ker_ck}$ + 0.5	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck}$ - 0.5	-	

1. Evaluated by characterization - Not tested in production.

Table 76. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9\ T_{fmc_ker_ck}$ - 1	$9\ T_{fmc_ker_ck}$ + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	$7\ T_{fmc_ker_ck}$ -1	$7\ T_{fmc_ker_ck}$ + 1	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5\ T_{fmc_ker_ck}$ + 10	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4\ T_{fmc_ker_ck}$ + 10	-	

1. Evaluated by characterization - Not tested in production.
2. N_{WAIT} pulse width is equal to one fmc_ker_ck cycle.

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Synchronous waveforms and timings

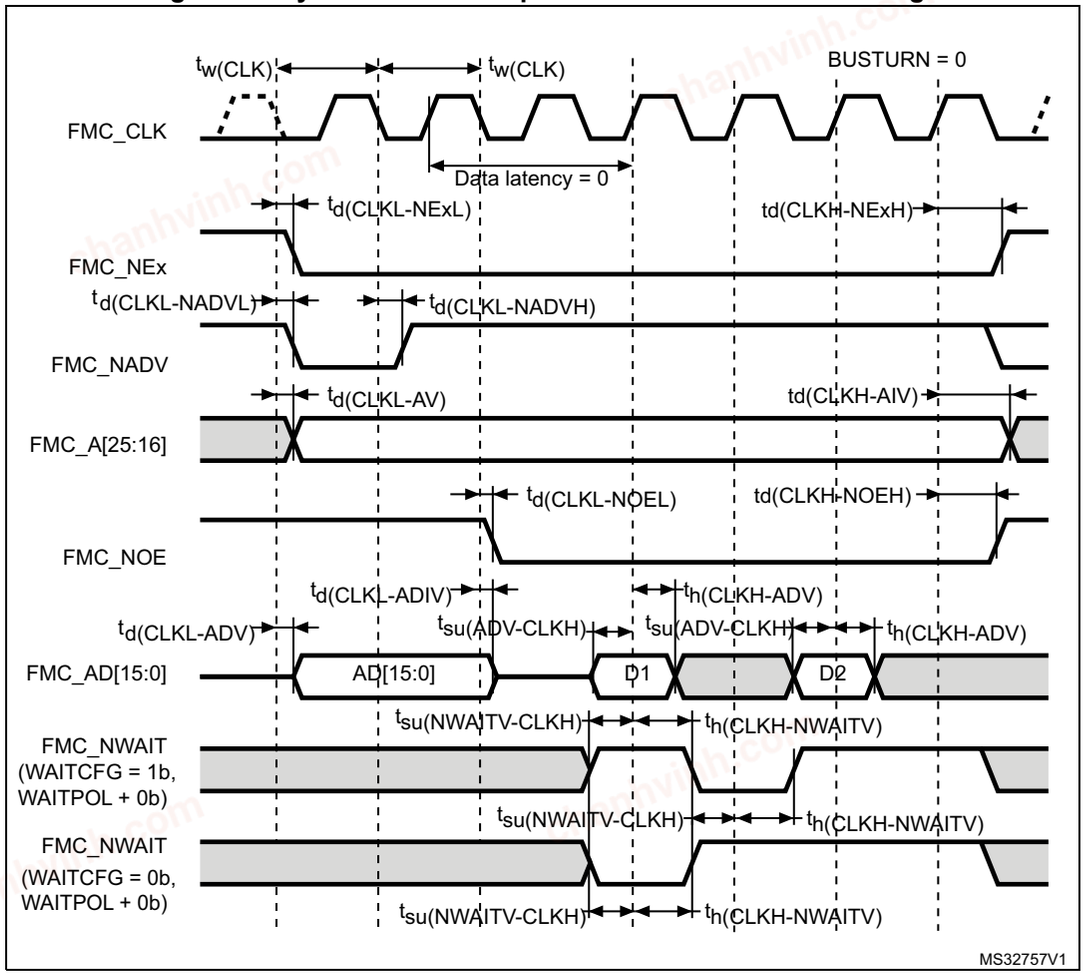
Figures *25* through *28* represent synchronous waveforms, tables *77* through *80* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash, DataLatency = 0 for PSRAM.
- With capacity load C_L = 30 pF

In all the timing tables, the $T_{fmc_ker_ck}$ is the $f_{mc_ker_ck}$ clock period, with the following FMC_CLK maximum values:

- For 2.7 V < V_{DD} < 3.6 V: maximum FMC_CLK = 100 MHz at C_L = 20 pF
- For 1.71 V < V_{DD} < 1.8 V: maximum FMC_CLK = 95 MHz at C_L = 20 pF
- For 1.71 V < V_{DD} < 1.8 V: maximum FMC_CLK = 100 MHz at C_L = 15 pF

Figure 25. Synchronous multiplexed NOR/PSRAM read timings



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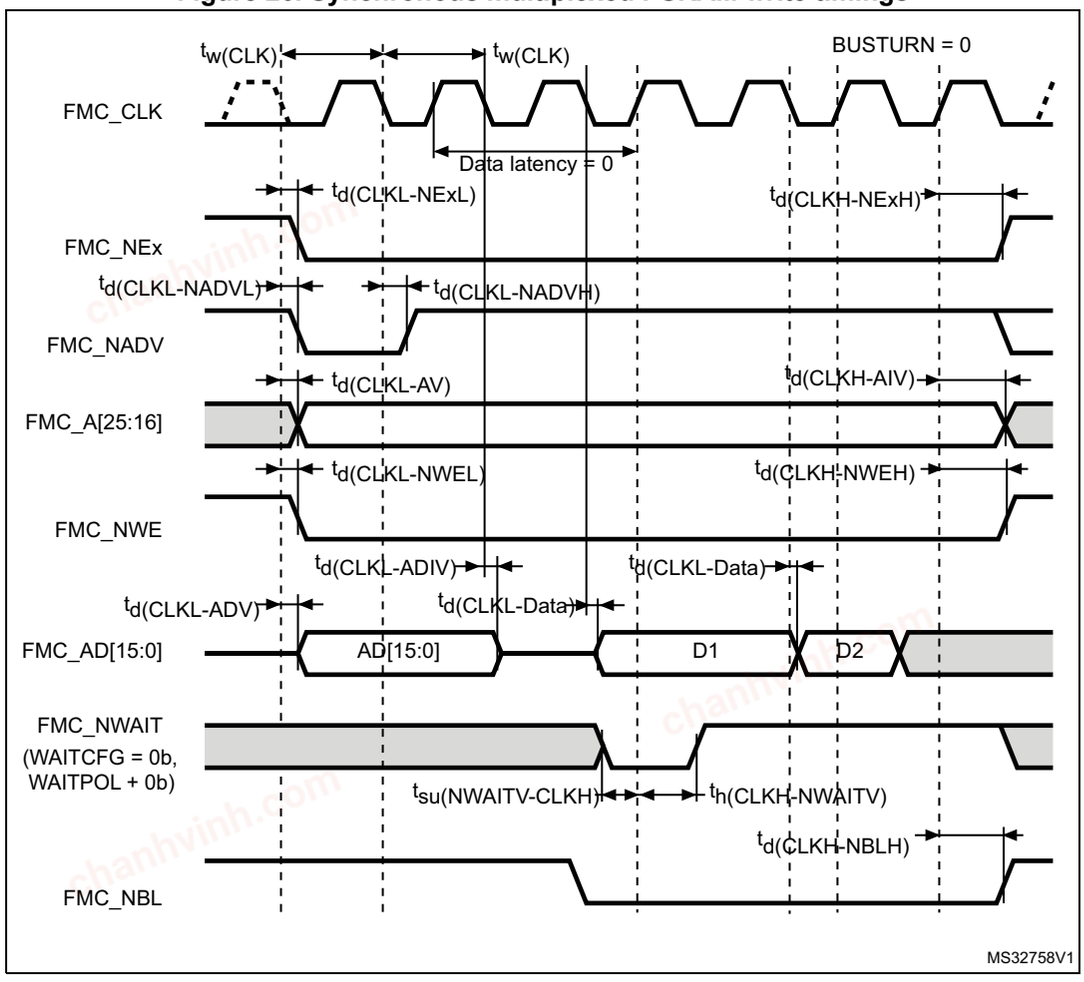
Table 77. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	1	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$T_{fmc_ker_ck}$ - 0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16…25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16…25)	$T_{fmc_ker_ck}$- 0.5	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc_ker_ck}$ + 0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	1	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	3.5	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	1.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Evaluated by characterization - Not tested in production.

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Figure 26. Synchronous multiplexed PSRAM write timings



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Table 78. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$T_{fmc_ker_ck}$ - 0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16…25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16…25)	$T_{fmc_ker_ck}$ - 0.5	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck}$ + 0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	1	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	1	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck}$-0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Evaluated by characterization - Not tested in production.

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Figure 27. Synchronous non-multiplexed NOR/PSRAM read timings

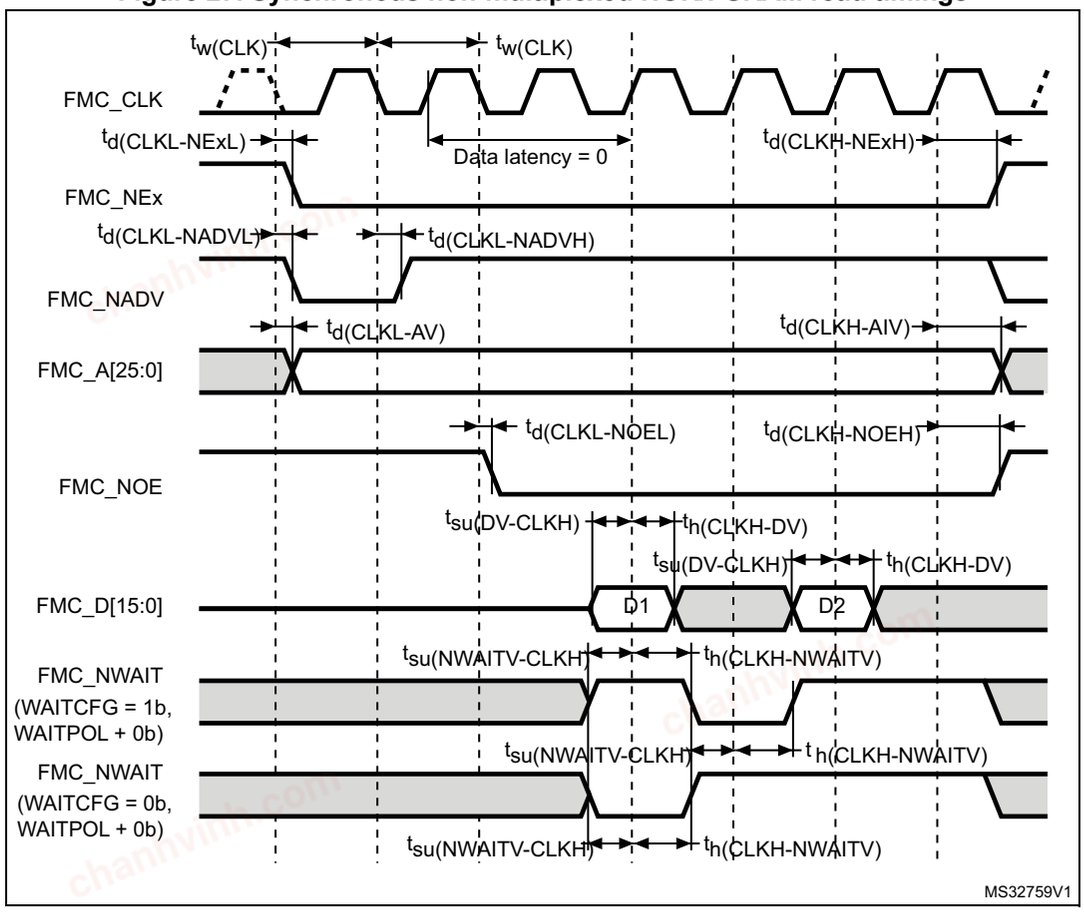


Table 79. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck}$ –0.5	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$T_{fmc_ker_ck}$- 0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16…25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16…25)	$T_{fmc_ker_ck}$- 0.5	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK ow to FMC_NOE low	-	1	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc_ker_ck}$ + 0.5	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	1.5	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

1. Evaluated by characterization - Not tested in production.

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Figure 28. Synchronous non-multiplexed PSRAM write timings

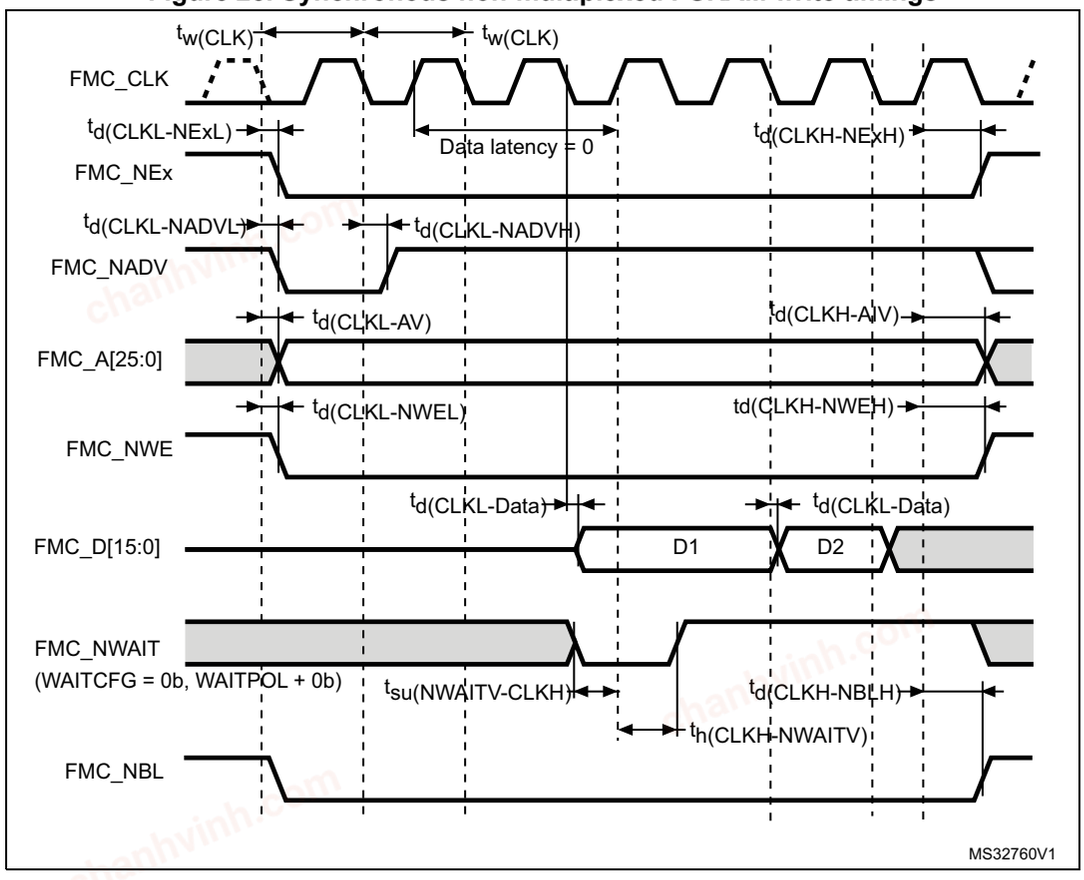


Table 80. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{fmc_ker_ck}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	1	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0…2)	$T_{fmc_ker_ck}$ - 0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16…25)	-	1	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16…25)	$T_{fmc_ker_ck}$ - 0.5	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc_ker_ck}$+ 0.5	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	1.5	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc_ker_ck}$ - 0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1.5	-	

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1. Evaluated by characterization - Not tested in production.

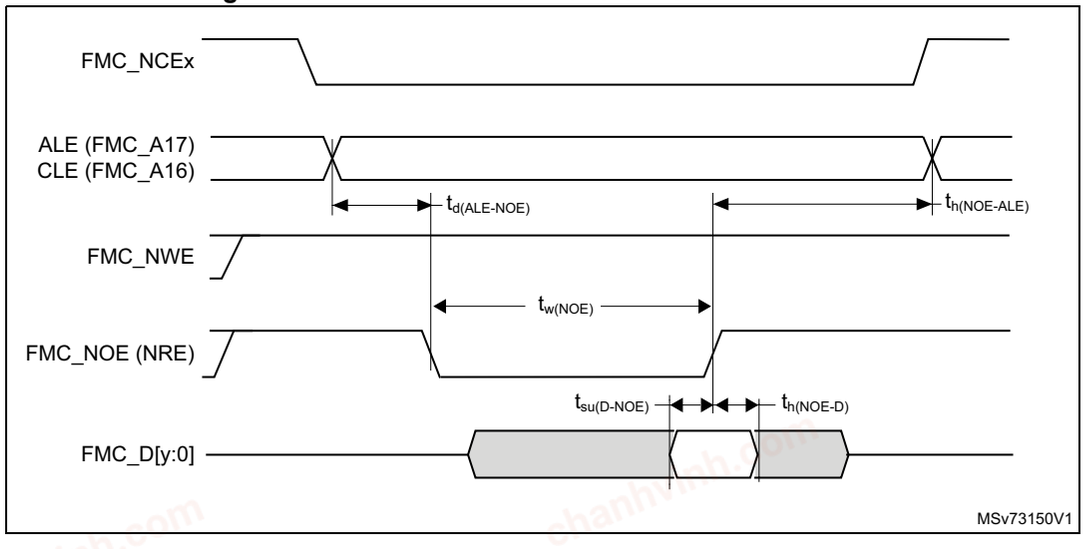
NAND controller waveforms and timings

Figures *29* through *32* represent synchronous waveforms, tables *81* and *82* provide the corresponding timings. The results are obtained with the following FMC configuration and a capacitive load (C_L) of 30 pF:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- Capacitive load C_L = 30 pF

In all timing tables, $T_{fmc_ker_ck}$ is the HCLK clock period.

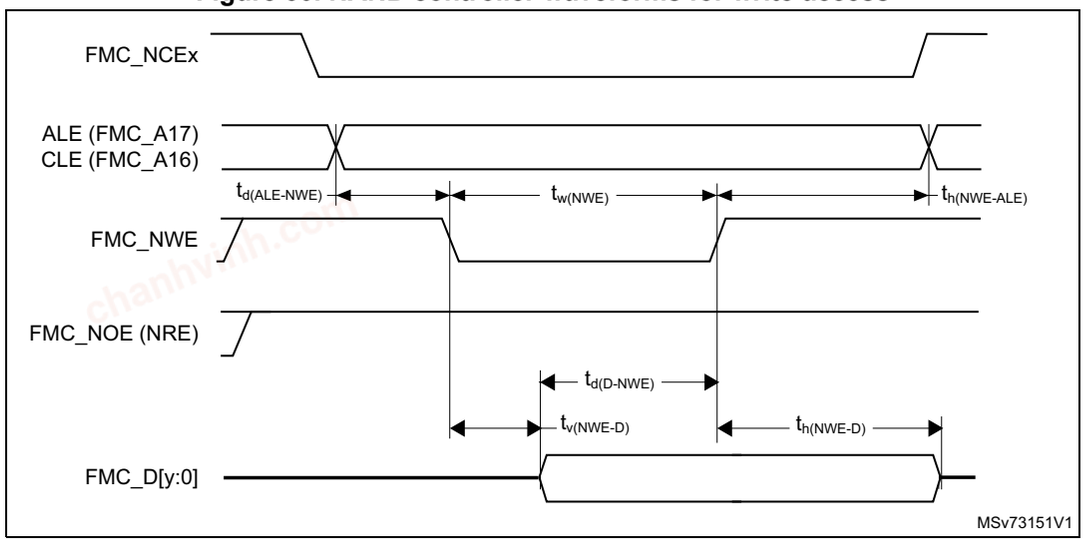
Figure 29. NAND controller waveforms for read access



1. y = 7 or 15, depending upon the NAND flash memory interface.

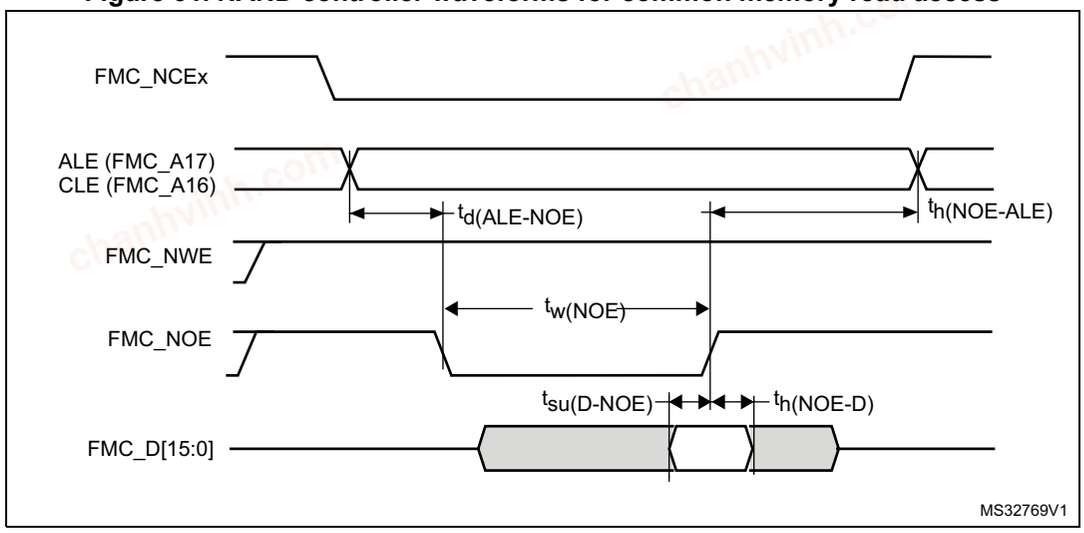
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Figure 30. NAND controller waveforms for write access



1. y = 7 or 15, depending upon the NAND flash memory interface.

Figure 31. NAND controller waveforms for common memory read access



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Figure 32. NAND controller waveforms for common memory write access

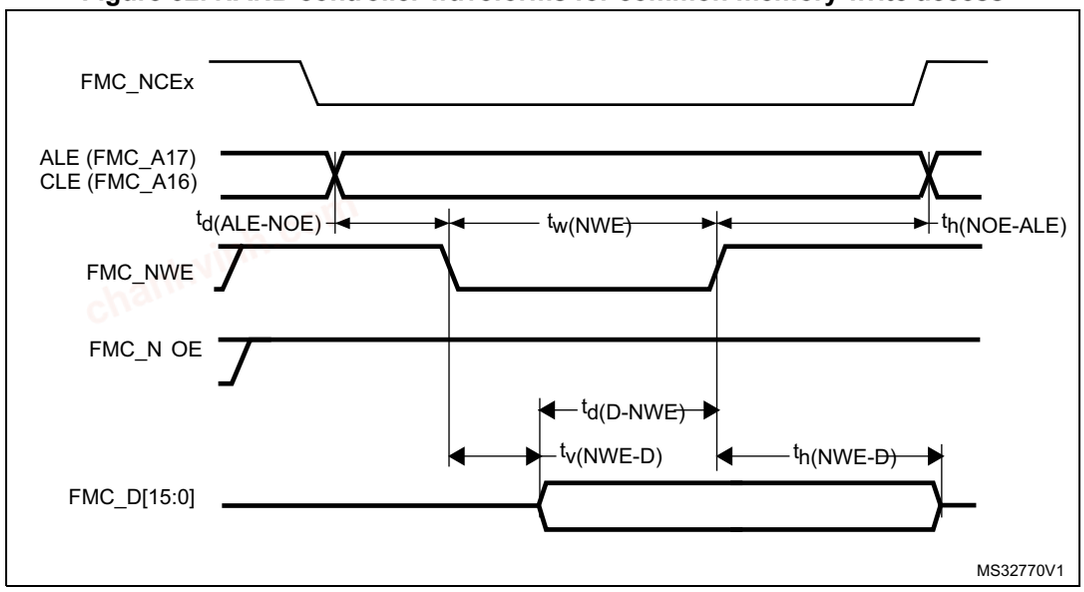


Table 81. Switching characteristics for NAND flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc_ker_ck}$ - 0.5	$4T_{fmc_ker_ck}$+ 0.5	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc_ker_ck}$ + 0.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc_ker_ck}$ - 1	-	

1. Evaluated by characterization - Not tested in production.

Table 82. Switching characteristics for NAND flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc_ker_ck}$ – 0.5	$4T_{fmc_ker_ck}$ + 0.5	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc_ker_ck}$ + 0.5	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc_ker_ck}$ - 2.5	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc_ker_ck}$ + 0.5	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc_ker_ck}$ - 1	-	

1. Evaluated by characterization - Not tested in production.

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5.3.18 Octo-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 83* and *Table 84* are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 20*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS0

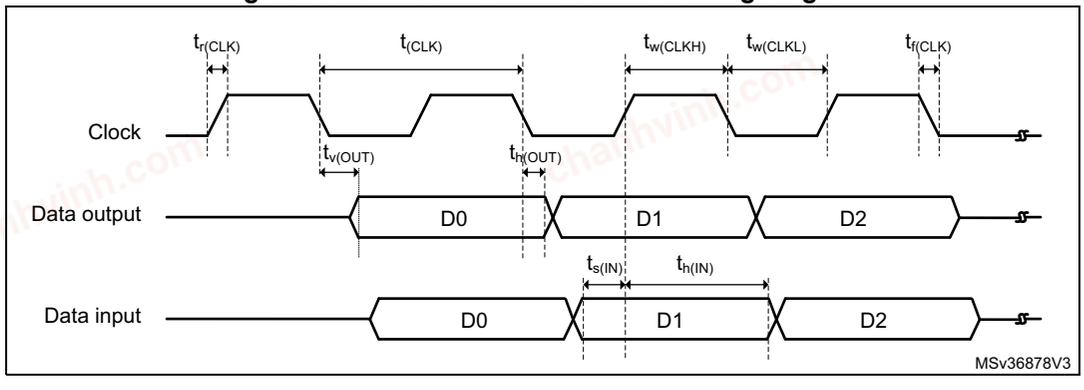
Refer to *Section 5.3.14* for more details on the input/output alternate function characteristics.

Table 83. OCTOSPI characteristics in SDR mode(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	OCTOSPI clock frequency	1.71 V < V_{DD} < 3.6 V, C_L = 15 pF	-	-	110	MHz
		2.7 V < V_{DD} < 3.6 V, C_L =15 pF	-	-	150	
$t_{w(CLKH)}$	OCTOSPI clock high and low time, even division	PRESCALER[7:0] = n (= 0, 1, 3, 5,...,255)	$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2$ - 0.5	-	$t_{(CK)}/2$ + 0.5	
$t_{w(CLKH)}$	OCTOSPI clock high and low time, odd division	PRESCALER[7:0] = n (= 2, 4, 6, ...,254)	(n/2) * $t_{(CLK)}$ / (n + 1) - 0.5	-	(n/2) * $t_{(CLK)}$/ (n + 1) + 0.5	
$t_{w(CLKL)}$			(n/2 + 1) * $t_{(CLK)}$/ (n + 1) - 0.5	-	(n/2 + 1) * $t_{(CLK)}$/ (n + 1) + 0.5	
$t_{s(IN)}$	Data input setup time	-	4	-	-	
$t_{h(IN)}$	Data input hold time	-	1	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0.5	1	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

1. All values apply to Octal and Quad-SPI mode.
2. Evaluated by characterization - Not tested in production.
3. Delay block bypassed.

Figure 33. OCTOSPI SDR read/write timing diagram



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Table 84. OCTOSPI characteristics in DTR mode (no DQS)(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CLK}	OCTOSPI clock frequency	1.71 V < V_{DD} < 3.6 V, C_L = 15 pF	-	-	100(4)	MHz
		2.7 V < V_{DD} < 3.6 V, C_L = 15 pF	-	-	125(4)	
$t_{w(CLKH)}$	OCTOSPI clock high and low time	PRESCALER[7:0] = n (= 0, 1, 3, 5, ..255)	$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	
$t_{w(CLKH)}$	OCTOSPI clock high and low time	PRESCALER[7:0] = n (= 2, 4, 6, 8, ...254)	(n/2) * $t_{(CLK)}$/ (n + 1) - 0.5	-	(n/2) * $t_{(CLK)}$/ (n + 1) + 0.5	ns
$t_{w(CLKL)}$			(n/2 + 1) * $t_{(CLK)}$/ (n + 1) - 0.5	-	(n/2 + 1) * $t_{(CLK)}$/ (n + 1) + 0.5	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	-	4	-	-	ns
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	-	1.5	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	DHQC = 0	-	2.5	3.5	
		DHQC = 1, Prescaler [7:0] = 1, 2...	-	$t_{(CLK)}/4$ + 0.5	$t_{(CLK)}/4$ + 1	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	DHQC = 0	1.5	-	-	
		DHQC = 1, Prescaler [7:0] = 1, 2...	$t_{(CLK)}/4$ - 1	-	-	

1. All values apply to Octal and Quad-SPI mode.
2. Evaluated by characterization - Not tested in production.
3. Delay block bypassed.
4. DHQC must be set to reach the mentioned frequency.

Table 85. OCTOSPI characteristics in DTR mode (with DQS) / hyperbus(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CLK}	OCTOSPI clock frequency	1.71 V < V_{DD} < 3.6 V, C_L = 15 pF	-	-	125(3)(4)	MHz
		2.7 V < V_{DD} < 3.6 V, C_L = 15 pF	-	-	125(3)(5)	
$t_{w(CLKH)}$	OCTOSPI clock high and low time	PRESCALER[7:0] = n = (0, 1, 3, 5, ..255)	$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	
$t_{w(CLKH)}$	OCTOSPI clock high and low time	PRESCALER[7:0] = n = (2, 4, 6, 8, ...254)	(n/2)*$t_{(CLK)}$/ (n+1) - 0.5	-	(n/2)*$t_{(CLK)}$/ (n+1) + 0.5	
$t_{w(CLKL)}$			(n/2+1)*$t_{(CLK)}$/ (n+1) - 0.5	-	(n/2+1)*$t_{(CLK)}$/ (n+1) + 0.5	
$t_{v(CLK)}$	Clock valid time	-	-	-	$t_{(CLK)}$ + 2	
$t_{h(CLK)}$	Clock hold time	-	$t_{(CLK)}/2$ - 1	-	-	

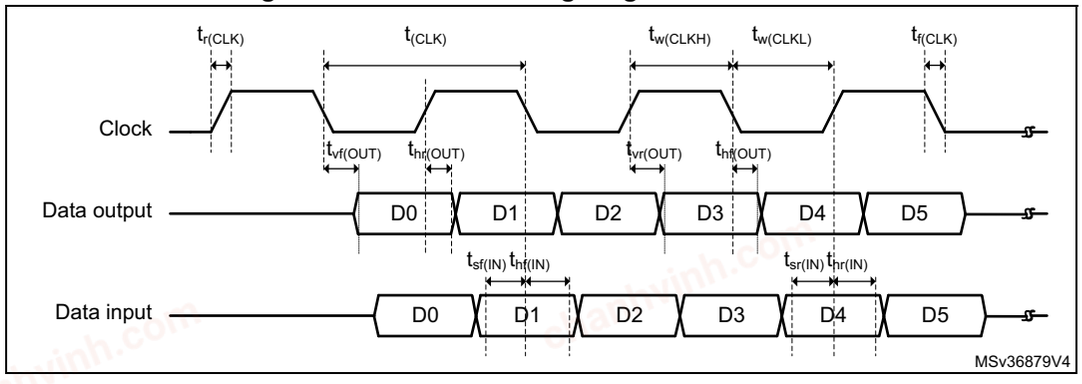
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Table 85. OCTOSPI characteristics in DTR mode (with DQS) / hyperbus(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ODr(CLK)}$(5)	CLK, NCLK crossing level on CLK rising edge	V_{DD} = 1.8 V	1000	-	1080	mV
$V_{ODf(CLK)}$(5)	CLK, NCLK crossing level on CLK falling edge	V_{DD} = 1.8 V	930	-	1040	
$t_{w(CS)}$	Chip select high time	-	3 * $t_{(CLK)}$	-	-	ns
$t_{v(DQ)}$	Data input valid time	-	3	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	1	-	-	
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	3 * $t_{(CLK)}$	
$t_{sr(DQ)}$, $t_{sf(DQ)}$	Data input setup time	-	-0.5	-	-	ns
$t_{hr(DQ)}$, $t_{hf(DQ)}$	Data input hold time	-	2	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	DHQC = 0	-	2.5	3.5	
		DHQC = 1, all prescaler values (except 0)	-	$t_{(CLK)}/4$ + 0.5	$t_{(CLK)}/4$ + 1	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	DHQC = 0	1.5	-	-	
		DHQC = 1, all prescaler values (except 0)	$t_{(CLK)}/4$ - 1	-	-	

1. Evaluated by characterization - Not tested in production.
2. Delay block activated.
3. Maximum frequency value are given for a maximum RWDS to DQ skew of ± 1.0 ns.
4. DHQC must be set to reach the mentioned frequency.
5. PF10/PB5, PB4/PB5 and PA3/PB5 are recommended to be in line with crossing specification.

Figure 34. OCTOSPI timing diagram - DTR mode



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Figure 35. OCTOSPI hyperbus clock

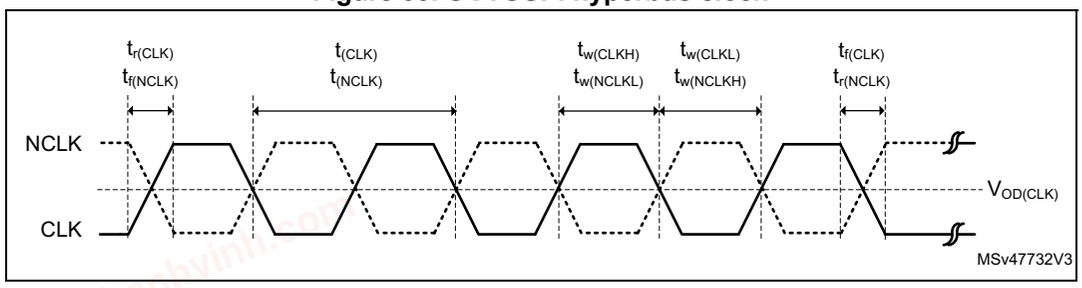


Figure 36. OCTOSPI hyperbus read

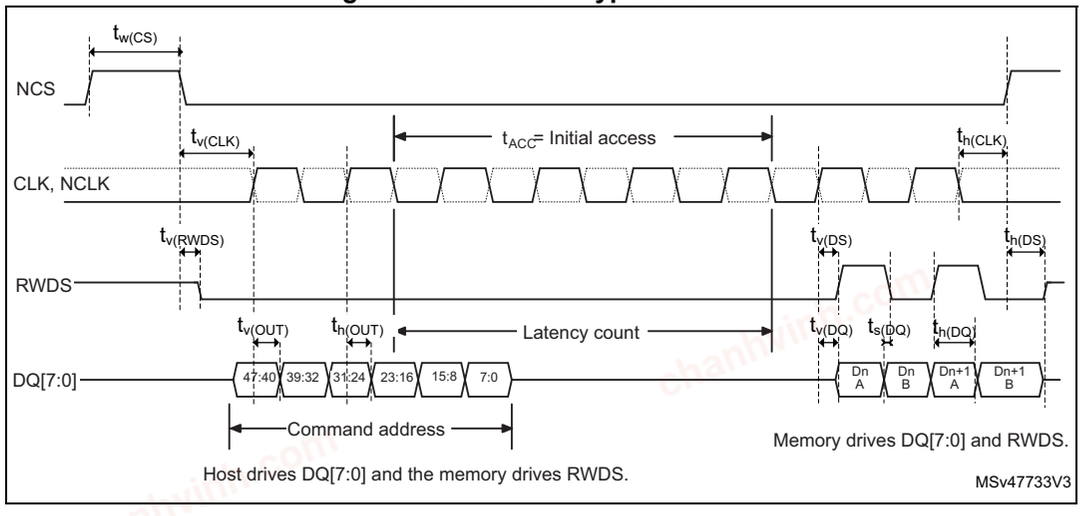
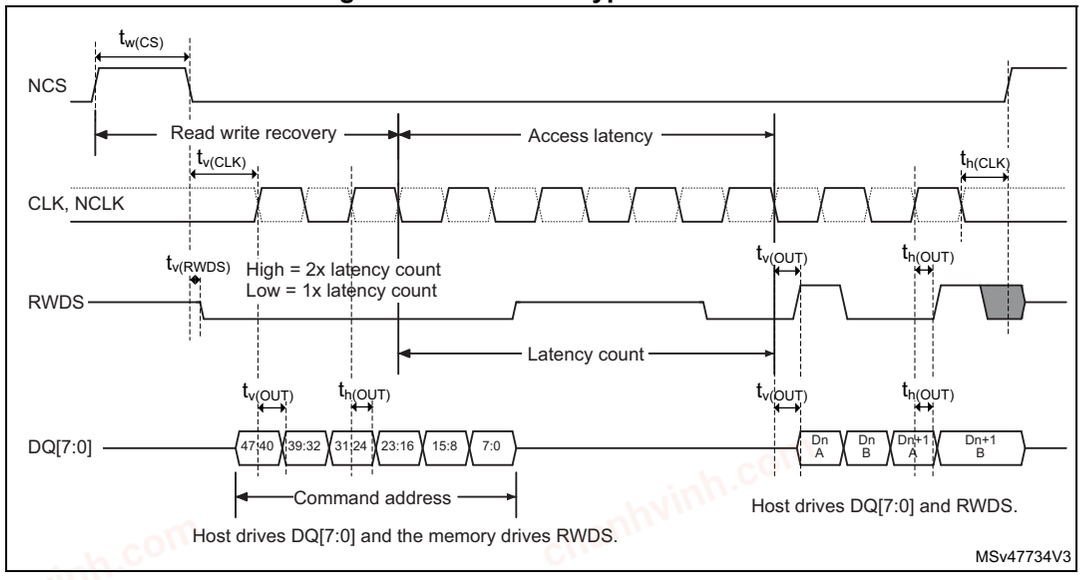


Figure 37. OCTOSPI hyperbus write



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5.3.19 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 86* are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 20*, with the following configuration:

Table 86. Delay block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	640	1040	1760	ps
t_{Δ}	Unit delay	-	38	44	54	ps

5.3.20 DCMI interface characteristics

Unless otherwise specified, the parameters given in *Table 87* are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 20*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scaling VOS0 selected

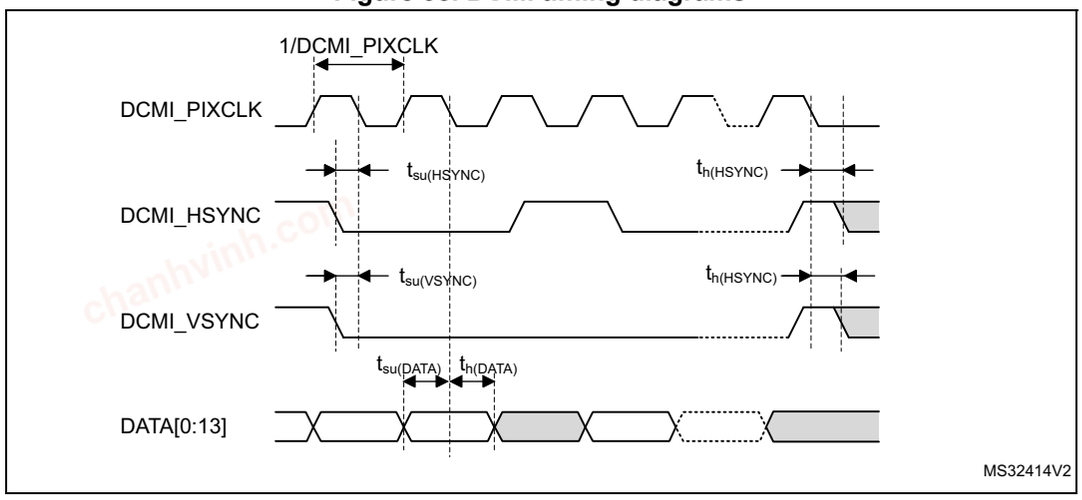
Table 87. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/fHCLK	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	100	MHz
D_{PIXEL}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2.5	-	ns
$t_{h(DATA)}$	Data hold time	2	-	
$t_{su(HSYNC)}$, $t_{su(VSYNC)}$	DCMI_HSYNC and DCMI_VSYNC input setup times	2.5	-	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$	DCMI_HSYNC and DCMI_VSYNC input hold times	1.5	-	

1. Evaluated by characterization - Not tested in production.

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Figure 38. DCMI timing diagrams



5.3.21 PSSI interface characteristics

Unless otherwise specified, the parameters given in *Table 87* and *Table 88* are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 20* and *Section 5.3.1*, with the following configuration:

- PSSI_PDCK polarity: falling
- PSSI_RDY and PSSI_DE polarity: low
- Bus width: 16 lines
- DATA width: 32 bits
- Capacitive load C_L= 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V
- Voltage scaling VOS0 selected

Table 88. PSSI transmit characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
-	Frequency ratio PSSI_PDCK/f_{HCLK}	-	-	0.4	-
PSSI_PDCK	PSSI clock input	2.7 V ≤ V_{DD} ≤ 3.6 V	-	90(2)	MHz
		1.71 V ≤ V_{DD} ≤ 3.6 V	-	86	
D_{pixel}	PSSI clock input duty cycle		30	70	%

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Table 88. PSSI transmit characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{ov}(DATA)	Data output valid time	2.7 V ≤ V_{DD} ≤ 3.6 V	-	11	ns
		1.71 V ≤ V_{DD} ≤ 3.6 V	-	11.5	
t_{oh}(DATA)	Data output hold time	1.71 V ≤ V_{DD} ≤ 3.6 V	5.5	-	
$t_{ov(}$(DE)	DE output valid time		-	11.5	
t_{oh}(DE)	DE output hold time		5.5	-	
tsu(RDY)	RDY input setup time		0.5	-	
th(RDY)	RDY input hold time		0.5	-	

1. Evaluated by characterization - Not tested in production.
2. This maximal frequency does not consider receiver setup and hold timings.

Table 89. PSSI receive characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
-	Frequency ratio PSSI_PDCK/f_{HCLK}		-	0.4	-
PSSI_PDCK	PSSI clock input	1.71 V ≤ V_{DD} ≤ 3.6 V	-	100	MHz
D_{pixel}	PSSI clock input duty cycle	-	30	70	%
t_{su}(DATA)	Data input setup time	1.71 V ≤ V_{DD} ≤ 3.6 V	2.5	-	ns
t_h(DATA)	Data input hold time		2.5	-	
$t_{su(}$(DE)	DE input setup time		1.5	-	
t_h(DE)	DE input hold time		2	-	
t_{ov}(RDY)	RDY output valid time		-	16.5	
t_{oh}(RDY)	RDY output hold time		5.5	-	

1. Evaluated by characterization - Not tested in production.

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Figure 39. PSSI transmit timing diagram

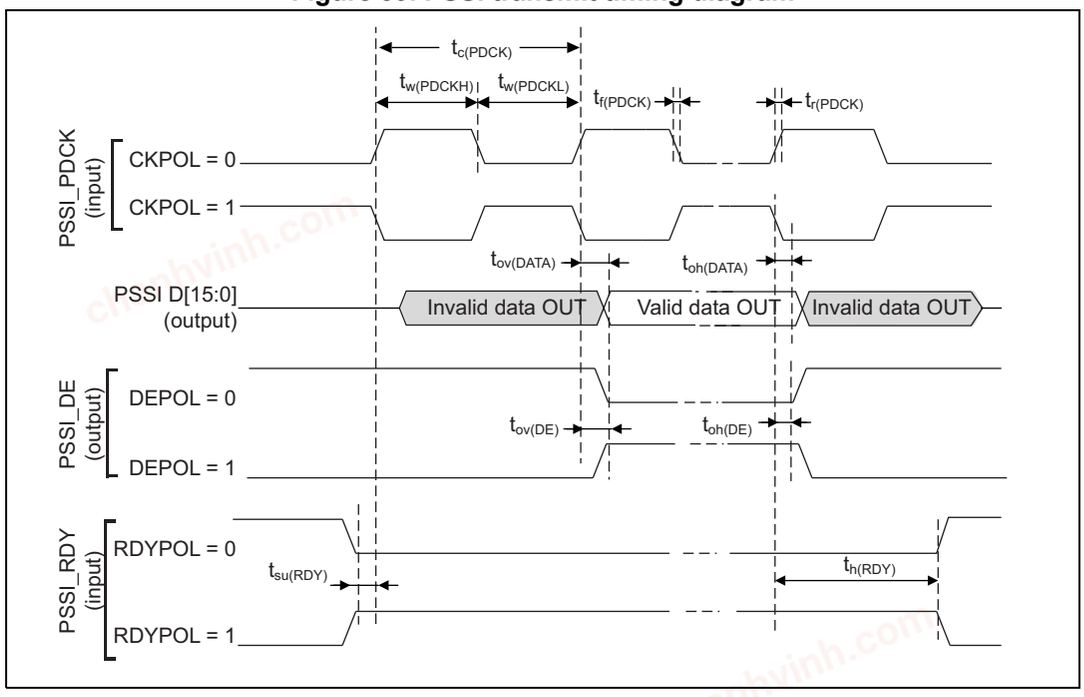
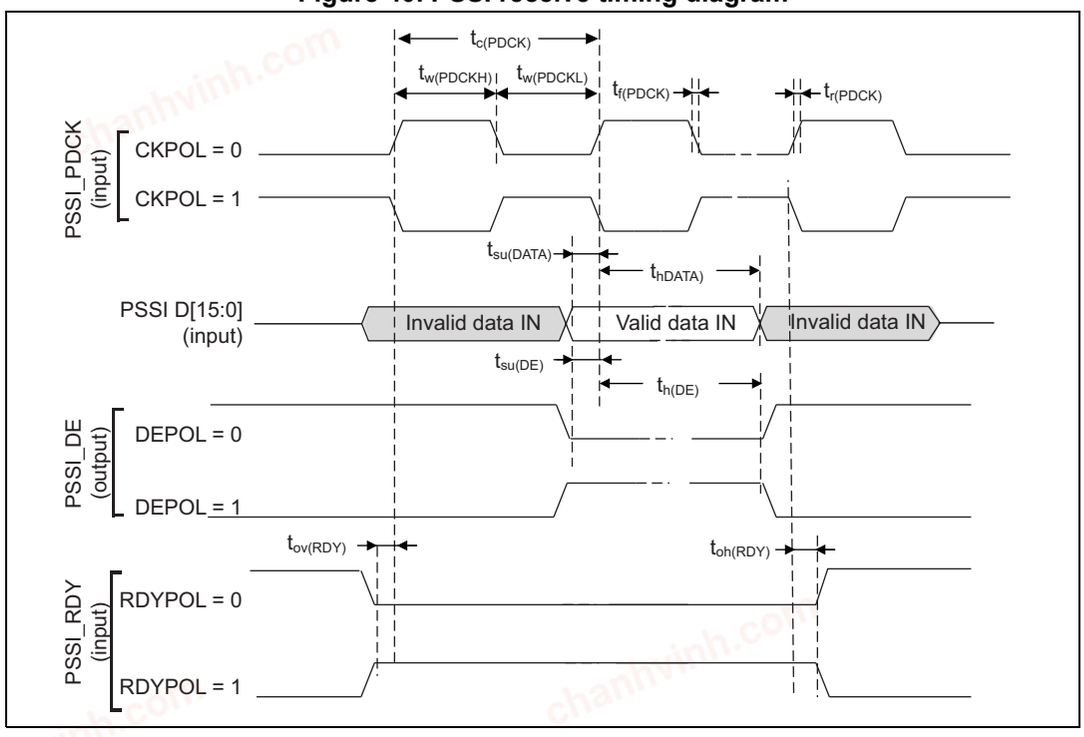


Figure 40. PSSI receive timing diagram



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5.3.22 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 90* are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 20*.

Table 90. 12-bit ADC characteristics(1)(2)

Symbol	Parameter	Conditions						Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-						1.62	-	3.6	V
V_{REF+}	Positive reference voltage	-						1.62	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-						V_{SSA}			
f_{ADC}	ADC clock frequency	1.62V ≤ V_{DDA} ≤ 3.6 V						1.5	-	75	MHz
f_S(3) with R_{AIN} = 47 Ω and C_{PCB} = 22 pF	Sampling rate for fast channels (VIN[0:5])	Resolution = 12 bits	Continuous mode	1.8V ≤ V_{DDA}≤3.6V	-40°C ≤ T_J ≤ 130°C	f_{ADC}= 75 MHz	SMP =2.5	-	5.00	-	MSPS
				1.6V ≤ V_{DDA}≤3.6V		f_{ADC}= 70 MHz			4.66		
			Single or Discontinuous mode	2.4V ≤ V_{DDA}≤3.6V		f_{ADC}= 60 MHz			4.00	-	
				1.6V ≤ V_{DDA}≤3.6V		f_{ADC}= 50MHz			3.33	-	
		Resolution = 10 bits	Continuous mode	1.6V ≤ V_{DDA}≤3.6V		f_{ADC}= 75 MHz		-	5.77	-	
			Single or Discontinuous mode	2.4V ≤ V_{DDA}≤3.6V		f_{ADC}= 75 MHz			5.77	-	
				1.6V ≤ V_{DDA}≤3.6V		f_{ADC}= 65 MHz			5.00	-	
		Resolution = 8 bits	All modes	1.6V ≤ V_{DDA}≤3.6V		f_{ADC}= 75 MHz		-	6.82	-	
		Resolution = 6 bits	All modes	1.6V ≤ V_{DDA}≤3.6V		f_{ADC}= 75 MHz		-	8.33	-	
	Sampling rate for slow channels	Resolution = 12 bits	All modes(4)	1.6V ≤ V_{DDA}≤3.6V		f_{ADC}= 35 MHz		-	2.30	-	
		Resolution = 10 bits				f_{ADC}= 35 MHz		-	2.70	-	
		Resolution = 8 bits				f_{ADC}= 50 MHz		-	4.50	-	
		Resolution = 6 bits				f_{ADC}= 50 MHz		-	5.50	-	
t_{TRIG}	External trigger period	Resolution = 12 bits						-	-	15	$1/f_{ADC}$

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Table 90. 12-bit ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AIN}(2)	Conversion voltage range	-	0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-	V_{REF}/2−10%	V_{REF}/2	V_{REF}/2+10%	V
R_{AIN}(5)	External input impedance	Resolution = 12 bits, T_J = 130°C (Tolerance 4 LSBs)	-	-	321	Ω
		Resolution = 12 bits, T_J = 125°C	-	-	220	
		Resolution = 10 bits, T_J = 130°C	-	-	1039	
		Resolution = 10 bits, T_J = 125°C	-	-	2100	
		Resolution = 8 bits, T_J = 130°C	-	-	6327	
		Resolution = 8 bits, T_J = 125°C	-	-	12000	
		Resolution = 6 bits, T_J = 130°C	-	-	47620	
		Resolution = 6 bits, T_J = 125°C	-	-	80000	
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
$t_{ADCVREG_STUP}$	ADC LDO startup time	-	-	5	10	µs
t_{STAB}	ADC power-up time	LDO already started	1	-	-	conversion cycle
t_{OFF_CAL}	Offset calibration time	-	1335			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	
		CKMODE = 01	-	-	2.5	
		CKMODE = 10			2.5	
		CKMODE = 11			2.25	
$t_{LATRINJ}$	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	2.5	3	3.5	
		CKMODE = 01	-	-	3.5	
		CKMODE = 10	-	-	3.5	
		CKMODE = 11	-	-	3.25	
t_S	Sampling time	-	2.5	-	640.5	
t_{CONV}	Total conversion time (including sampling time)	N-bits resolution	t_S + 0.5 + N			

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Table 90. 12-bit ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA_D(ADC)}$	ADC consumption on V_{DDA} and V_{REF}, Differential mode	fs = 5 MSPS	-	600	-	µA
		fs = 1 MSPS	-	190	-	
		fs = 0.1 MSPS	-	50	-	
$I_{DDA_SE(ADC)}$	ADC consumption on V_{DDA} and V_{REF} Single-ended mode	fs = 5 MSPS	-	500	-	
		fs = 1 MSPS	-	150	-	
		fs = 0.1 MSPS	-	50	-	
$I_{DD(ADC)}$	ADC consumption on V_{DD}	f_{ADC}= 75 MHz	-	265	-	
		f_{ADC}= 50 MHz		175	-	
		f_{ADC}= 25 MHz	-	90	-	
		f_{ADC}= 12.5 MHz	-	45	-	
		f_{ADC}= 6.25 MHz	-	22	-	
		f_{ADC}= 3.125 MHz	-	11	-	

1. Specified by design - Not tested in production.
2. The voltage booster on ADC switches must be used for V_{DDA} < 2.7 V (embedded I/O switches).
3. These values are valid on UFBGA144 package.
4. Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} to V_{SSA}.
5. The tolerance is two LSBs for 12-bit, 10-bit and 8-bit resolutions, otherwise specified.

Table 91. Minimum sampling time versus R_{AIN}(1)(2)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel(3)
12 bits	47	3.75E-08	6.12E-08
	68	3.94E-08	6.25E-08
	100	4.36E-08	6.51E-08
	150	5.11E-08	7.00E-08
	220	6.54E-08	7.86E-08
	330	8.80E-08	9.57E-08
	470	1.17E-07	1.23E-07
	680	1.60E-07	1.65E-07

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Table 91. Minimum sampling time versus R_{AIN}(1)(2) (continued)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel(3)
10 bits	47	3.19E-08	5.17E-08
	68	3.35E-08	5.28E-08
	100	3.66E-08	5.45E-08
	150	4.35E-08	5.83E-08
	220	5.43E-08	6.50E-08
	330	7.18E-08	7.89E-08
	470	9.46E-08	1.00E-07
	680	1.28E-07	1.33E-07
	1000	1.81E-07	1.83E-07
	1500	2.63E-07	2.63E-07
	2200	3.79E-07	3.76E-07
	3300	5.57E-07	5.52E-07
8 bits	47	2.64E-08	4.17E-08
	68	2.76E-08	4.24E-08
	100	3.02E-08	4.39E-08
	150	3.51E-08	4.66E-08
	220	4.27E-08	5.13E-08
	330	5.52E-08	6.19E-08
	470	7.17E-08	7.72E-08
	680	9.68E-08	1.00E-07
	1000	1.34E-07	1.37E-07
	1500	1.93E-07	1.94E-07
	2200	2.76E-07	2.74E-07
	3300	4.06E-07	4.01E-07
	4700	5.73E-07	5.62E-07
	6800	8.21E-07	7.99E-07
	10000	1.20E-06	1.17E-06
	15000	1.79E-06	1.74E-06

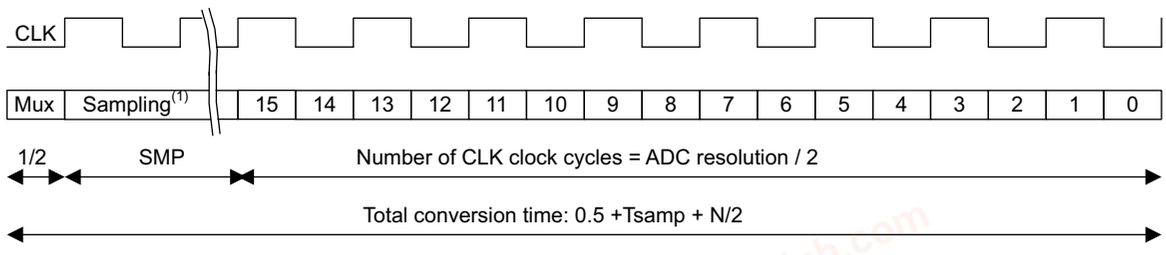
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Table 91. Minimum sampling time versus R_{AIN}(1)(2) (continued)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel(3)
6 bits	47	2.14E-08	3.16E-08
	68	2.23E-08	3.21E-08
	100	2.40E-08	3.31E-08
	150	2.68E-08	3.52E-08
	220	3.13E-08	3.87E-08
	330	3.89E-08	4.51E-08
	470	4.88E-08	5.39E-08
	680	6.38E-08	6.79E-08
	1000	8.70E-08	8.97E-08
	1500	1.23E-07	1.24E-07
	2200	1.73E-07	1.73E-07
	3300	2.53E-07	2.49E-07
	4700	3.53E-07	3.45E-07
	6800	5.04E-07	4.90E-07
	10000	7.34E-07	7.11E-07
	15000	1.09E-06	1.05E-06

1. Specified by design - Not tested in production.
2. Data valid up to 130 °C, with a 22 pF PCB capacitor, and V_{DDA} = 1.6 V.
3. Slow channels correspond to all ADC inputs except for the fast channels.

Figure 41. ADC conversion timing diagram



1. The sampling time defines the minimum sampling clock cycles (SMP) to be programmed in the ADC (refer to the product reference manual for details).

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Table 92. ADC accuracy(1)(2)

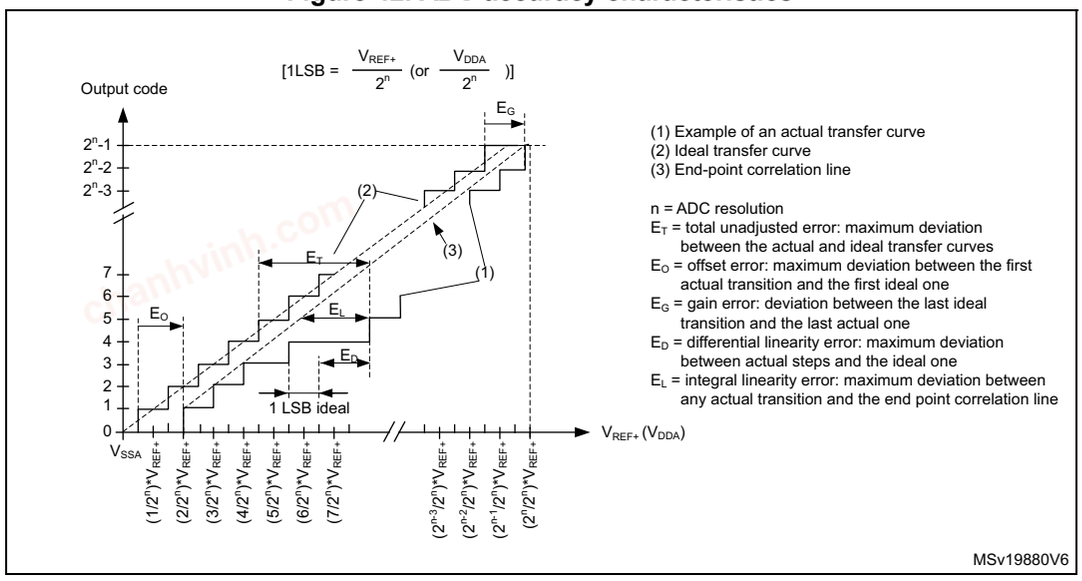
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Fast and slow channels	Single ended	-	±3.5	±12	LSB
			Differential	-	±2.5	±7.5	
EO	Offset error	-	Single ended	-	±3	±5.5	
		-	Differential	-	±2	±3.5	
EG	Gain error	-	Single ended	-	±3.5	±11	
		-	Differential		±2.5	±7	
ED	Differential linearity error	-	Single ended	-	±0.75	+2/-1	
		-	Differential	-	±0.75	+2/-1	
EL	Integral linearity error	Fast and slow channels	Single ended	-	±2	±6.5	
			Differential	-	±1	±4	
ENOB	Effective number of bits	Single ended		-	10.8	-	Bits
		Differential		-	11.5	-	
SINAD	Signal-to-noise and distortion ratio	Single ended		-	68	-	dB
		Differential		-	71	-	
SNR	Signal-to-noise ratio	Single ended		-	70	-	
		Differential		-	72	-	
THD	Total harmonic distortion	Single ended		-	-70	-	
		Differential		-	-80	-	

1. Evaluated by characterization for BGA packages. The values for LQFP package can differ. Not tested in production.
2. ADC DC accuracy values are measured after internal calibration in continuous mode.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins, which may potentially inject negative currents.

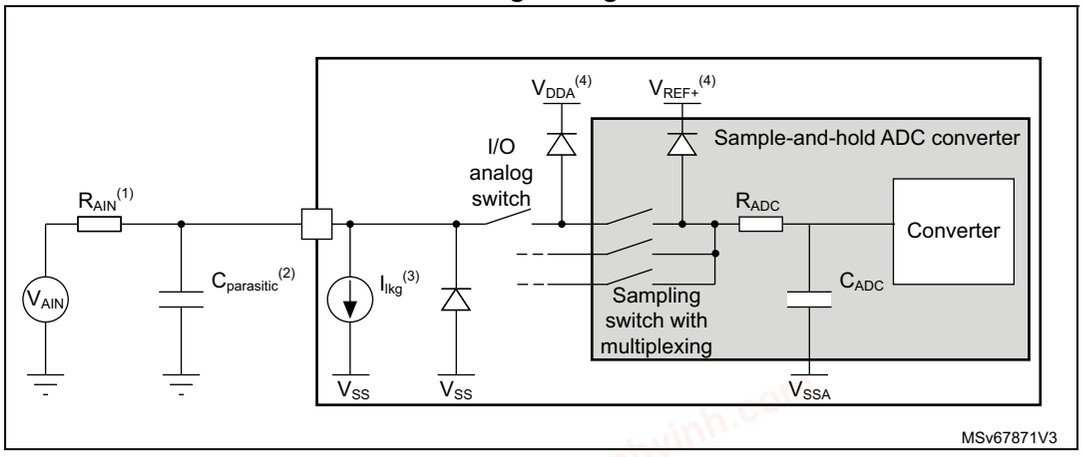
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Figure 42. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
5. EO = Offset error: deviation between the first actual transition and the first ideal one.
6. EG = Gain error: deviation between the last ideal transition and the last actual one.
7. ED = Differential linearity error: maximum deviation between actual steps and the ideal one.
8. EL = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 43. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



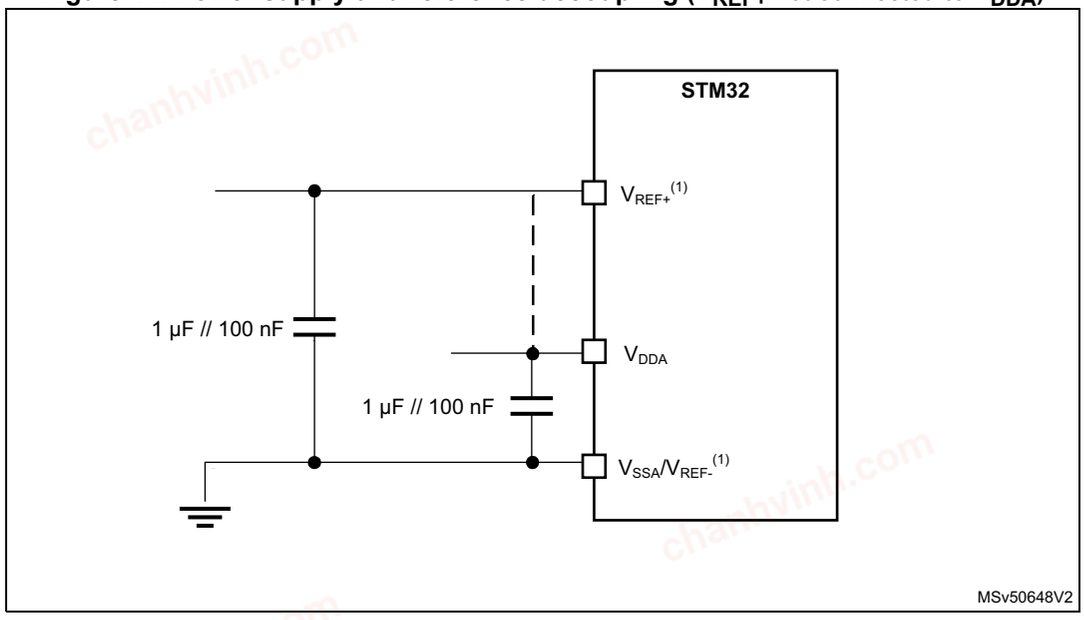
1. Refer to *Table 90* for the values of R_{AIN}, and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 57*). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 57* for the value of I_{lkg}.

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General PCB design guidelines

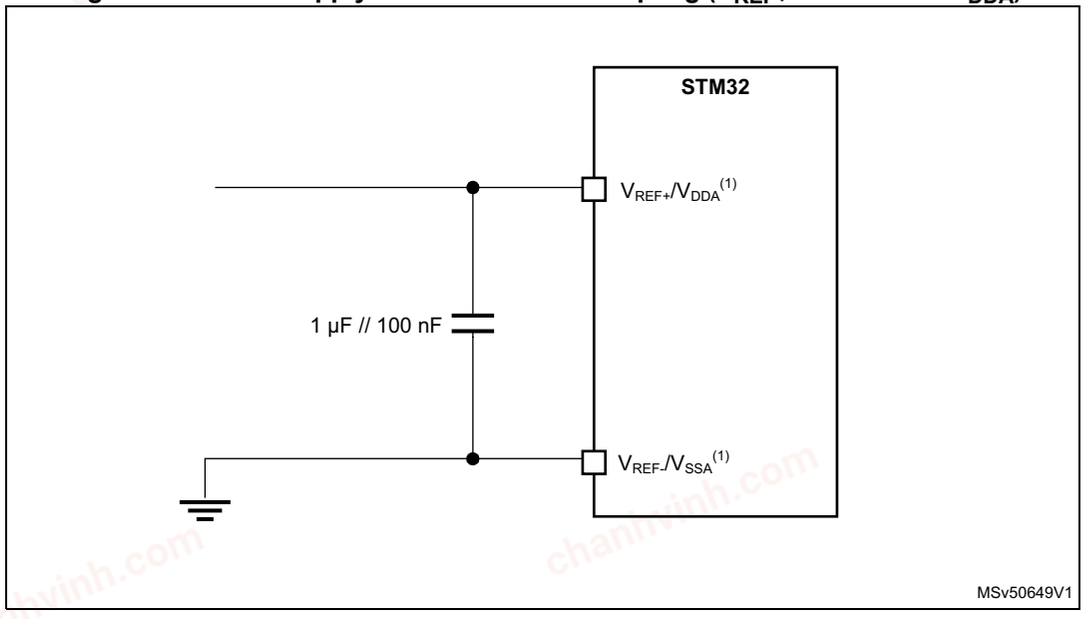
It is recommended to perform power supply decoupling as shown in *Figure 44* or *Figure 45*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors must be ceramic (good quality), and placed as close as possible to the chip.

Figure 44. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is not available on all packages (refer to *Table 15*), V_{REF-} is available only on LQFP100 and UFBGA144 packages. When V_{REF+} is not available, it is internally connected to V_{SSA}.

Figure 45. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is not available on all packages (refer to *Table 15*), V_{REF-} is available only on LQFP100 and UFBGA144 packages. When V_{REF-} is not available, it is internally connected to V_{SSA}. If V_{REF-} is not available, it is connected internally to V_{DDA}.

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5.3.23 DAC characteristics

Table 93. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	
R_L	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
R_O	Output impedance	DAC output buffer OFF		10.3	13	16	
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	
C_L	Capacitive load	DAC output buffer OFF		-	-	50	pF
C_{SH}		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} −0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	±0.5 LSB	-	2.05	3	µs
			±1 LSB	-	1.97	2.87	
			±2 LSB	-	1.67	2.84	
			±4 LSB	-	1.66	2.78	
			±8 LSB	-	1.65	2.7	
		Normal mode, DAC output buffer OFF, ±1LSB C_L= 10 pF		-	1.7	2	
t_{WAKEUP}(2)	Wake-up time from off state (setting the ENx bit in the DAC control register) until the final value of ±1LSB is reached	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, R_L = 5 kΩ		-	5	7.5	µs
		Normal mode, DAC output buffer OFF, $C_L \leq 10$ pF		-	2	5	
PSRR	DC V_{DDA} supply rejection ratio	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, R_L = 5 kΩ		-	-80	-28	dB

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Table 93. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{SAMP}	Sampling time in Sample and Hold mode C_L= 100 nF (code transition between the lowest and the highest input code when DAC_OUT reaches the ±1LSB final value)	MODE<2:0>_V12 = 100/101 (BUFFER ON)		-	0.7	2.6	ms
		MODE<2:0>_V12 = 110 (BUFFER OFF)		-	11.5	18.7	
		MODE<2:0>_V12=111(3) (INTERNAL BUFFER OFF)		-	0.3	0.6	µs
I_{leak}	Output leakage current	-		-	-	(4)	nA
C_{lint}	Internal sample and hold capacitor	-		1.8	2.2	2.6	pF
t_{TRIM}	Middle code offset trim time	Minimum time to verify each code		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	850	-	µV
		V_{REF+} = 1.8 V		-	425	-	
$I_{DDA(DAC)}$	DAC quiescent consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	360	-	µA
			No load, worst code (0xF1C)	-	490	-	
		DAC output buffer OFF	No load, middle/ worst code (0x800)	-	20	-	
		Sample and Hold mode, C_{SH}= 100 nF		-	$360*T_{ON}/(T_{ON}+T_{OFF})$(5)	-	
$I_{DDV(DAC)}$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	170	-	µA
			No load, worst code (0xF1C)	-	170	-	
		DAC output buffer OFF	No load, middle/ worst code (0x800)	-	160	-	
		Sample and Hold mode, buffer ON, C_{SH}= 100 nF (worst code)		-	$170*T_{ON}/(T_{ON}+T_{OFF})$(5)	-	
		Sample and Hold mode, buffer OFF, C_{SH}= 100 nF (worst code)		-	$160*T_{ON}/(T_{ON}+T_{OFF})$(5)	-	

1. Specified by design - Not tested in production, unless otherwise specified.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).
3. DACx_OUT pin is not connected externally (internal connection only).
4. Refer to *Table 57*.

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5. T_{ON} is the refresh phase duration, T_{OFF} is the hold phase duration. Refer to the reference manual for more details.

Table 94. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity(2)	DAC output buffer ON		−2	-	2	LSB
		DAC output buffer OFF		−2	-	2	
-	Monotonicity	10 bits		-	-	-	-
INL	Integral non linearity(3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		−4	-	4	LSB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		−4	-	4	
Offset	Offset error at code 0x800 (3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	$V_{REF+} = 3.6$ V	-	-	±12	
			$V_{REF+} = 1.8$ V	-	-	±25	
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±5	
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	$V_{REF+} = 3.6$ V	-	-	±5	
			$V_{REF+} = 1.8$ V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	-	±1	%
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±1	
TUE	Total unadjusted error	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	-	±30	LSB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L				±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	-	±23	
SNR	Signal-to-noise ratio(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ, 1 kHz, BW = 500 kHz		-	67.8	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L,1 kHz, BW = 500 kHz		-	67.8	-	
THD	Total harmonic distortion(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ, 1 kHz		-	−78.6	-	
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 kHz		-	−78.6	-	
SINAD	Signal-to-noise and distortion ratio(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ, 1 kHz		-	67.5	-	
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 kHz		-	67.5	-	

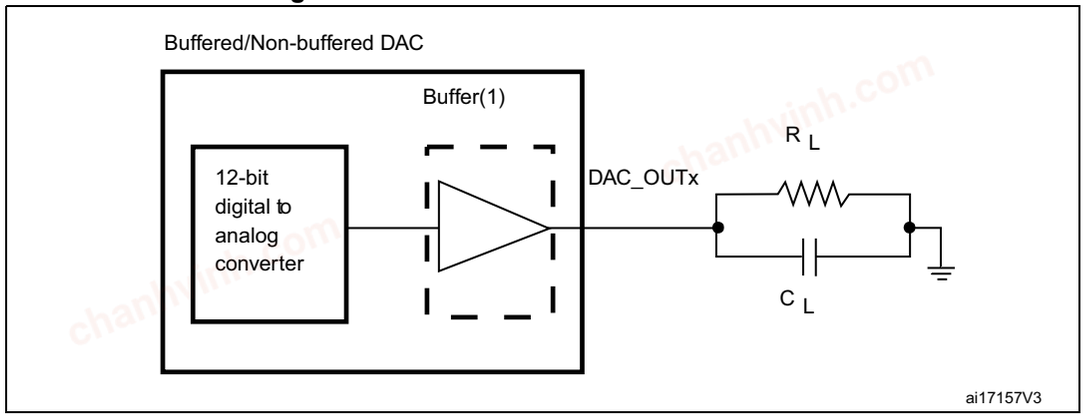
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Table 94. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	DAC output buffer ON, C_L≤50 pF, R_L ≥ 5 kΩ, 1 kHz	-	10.9	-	bits
		DAC output buffer OFF, C_L ≤ 50 pF, no R_L, 1 kHz	-	10.9	-	

1. Evaluated by characterization - Not tested in production.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2 V) when the buffer is ON.
6. Signal is −0.5 dBFS with $F_{sampling}$ = 1 MHz.

Figure 46. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly, without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.24 Analog temperature sensor characteristics

Table 95. Analog temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature (from V_{SENSOR} voltage)	-	-	3	°C
	V_{SENSE} linearity with temperature (from ADC counter)	-	-	3	
Avg_Slope(2)	Average slope (from V_{SENSOR} voltage)	-	2	-	mV/°C
	Average slope (from ADC counter)	-	2	-	
V_{30}(3)	Voltage at 30 °C ± 5 °C	-	0.62	-	V
t_{start_run}	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

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1. Specified by design - Not tested in production.
2. Evaluated by characterization - Not tested in production.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 bytes.

Table 96. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA} = 3.3 V	0x08FF F814 -0x08FF F815
TS_CAL2	Temperature sensor raw data acquired value at 130 °C, V_{DDA} = 3.3 V	0x08FF F818 - 0x08FF F819

5.3.25 Digital temperature sensor characteristics

Table 97. Digital temperature sensor characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}(2)	Output clock frequency	-	500	750	1150	kHz
T_{LC}(2)	Temperature linearity coefficient	VOS2	1660	2100	2750	Hz/°C
T_{TOTAL_ERROR}(2)	Temperature offset measurement, all VOS	T_J = −40 to 30 °C	-13	-	4	°C
		T_J = 30 °C to T_{Jmax}	-7	-	2	
T_{VDD_CORE}	Additional error due to supply variation	VOS2	0	-	0	°C
		VOS0, VOS1, VOS3	-1	-	1	
t_{TRIM}	Calibration time	-	-	-	2	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready bit is set	-	-	67	116	µs
I_{DDCORE_DTS}	DTS consumption on V_{DD_CORE}	-	8.5	30	70	µA

1. Specified by design - Not tested in production, unless otherwise specified.
2. Evaluated by characterization - Not tested in production.

5.3.26 V_{CORE} monitoring characteristics

Table 98. V_{CORE} monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_{S_VCORE}	ADC sampling time when reading the V_{CORE} voltage	1	-	-	µs

1. Specified by design - Not tested in production.

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5.3.27 Temperature and V_{BAT} monitoring

Table 99. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	4 x 26	-	kΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	-10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs
$V_{BAThigh}$	High supply monitoring	3.50	3.575	3.63	V
V_{BATlow}	Low supply monitoring	-	1.36	-	
$I_{VBATbuf}$	Sensor buffer consumption	-	3.8	6.5	µA

1. Specified by design - Not tested in production.

Table 100. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3 = 0	-	5	-	kΩ
		VBRS in PWR_CR3 = 1	-	1.5	-	

Table 101. Temperature monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	-	126	-	°C
$TEMP_{low}$	Low temperature monitoring	-	-37	-	

5.3.28 Voltage booster for analog switch

Table 102. Voltage booster for analog switch characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.71	2.6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.71 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

1. Evaluated by characterization - Not tested in production.

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5.3.29 V_{REFBUF} characteristics

Table 103. V_{REFBUF} characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode at V_{DDA} = 3.3 V	VRS = 000	2.8	3.3	3.6	V
			VRS = 001	2.4	-	3.6	
			VRS = 010	2.1	-	3.6	
		Degraded mode(2)	VRS = 000	1.62	-	2.80	
			VRS = 001	1.62	-	2.40	
			VRS = 010	1.62	-	2.10	
V_{REFBUF_OUT}	Voltage reference buffer output	Normal mode at 30 °C, I_{LOAD} = 100 µA	VRS = 000	2.498(3)	2.5000	2.5035(3)	V
			VRS = 001	2.0460	2.0490	2.0520	
			VRS = 010	1.8010	1.8040	1.8060	
		Degraded mode(2)	VRS = 000	V_{DDA} – 150 mV	-	2.5035	
			VRS = 001	V_{DDA} – 150 mV	-	2.0520	
			VRS = 010	V_{DDA} – 150 mV	-	1.8060	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF
esr	Equivalent serial resistor of C_L	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤ 4 mA	Normal mode	-	50	-	ppm/mA
T_{coeff}	Temperature coefficient	-40 °C < T_J < +130 °C	-	-	-	100	ppm/°C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100 kHz	-	-	40	-	
t_{START}	Start-up time	C_L= 0.5 µF	-	-	300	-	µs
		C_L= 1 µF	-	-	500	-	
		C_L= 1.5 µF	-	-	650	-	

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Table 103. V_{REFBUF} characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(4)(4)	-		-	8	-	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from VDDA	I_{LOAD} = 0 µA	-	-	15	25	µA
		I_{LOAD} = 500 µA	-	-	16	30	
		I_{LOAD} = 4 mA	-	-	32	50	

1. Specified by design - Not tested in production, unless otherwise specified.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}−drop voltage).
3. Evaluated by characterization - Not tested in production.
4. To properly control V_{REFBUF} I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 2.1 V - 3.6 V, 2.4 V -3.6 V and 2.8 V - 3.6 V for VRS = 010, 001, and 000, respectively.

5.3.30 Timer characteristics

The parameters given in *Table 104* are guaranteed by design.

Refer to *Section 5.3.14* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 104. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler = 1, 2, or 4, $f_{TIMxCLK}$ = 250 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler > 4, $f_{TIMxCLK}$ = 125 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 250 MHz	0	$f_{TIMxCLK}$ / 2	MHz
Res_{TIM}	Timer resolution		-	16 / 32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Specified by design - Not tested in production.
3. The maximum timer frequency on APB1 or APB2 is up to 250 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4 x F_{rcc_pclkx1} or TIMxCLK = 4 x F_{rcc_pclkx2}.

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5.3.31 Low-power timer characteristics

Table 105. LPTIMx characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	250	MHz
f_{EXT}	Timer external clock frequency on Input1 and Input2	0	$f_{LPTIMxCLK}/2$	
Res_{TIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{TIMxCLK}$

1. LPTIMx is used as a general term to refer to the LPTIM1 to LPTIM6 timers.
2. Specified by design - Not tested in production.

5.3.32 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are specified by design, not tested in production, when the I²C peripheral is properly configured (refer to the product reference manual - RM0481)

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 5.3.14* for the I2C I/Os characteristics

All I²C SDA and SCL I/Os embed an analog filter, refer to *Table 106* for its characteristics.

Table 106. I²C analog filter characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes suppressed by analog filter	50(3)	160(4)	ns

1. Evaluated by characterization - Not tested in production.
2. Measurement points are done at 50% V_{DD}.
3. Spikes with widths below $t_{AF(min)}$ are filtered.
4. Spikes with widths above $t_{AF(max)}$ are not filtered.

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USART interface characteristics

Unless otherwise specified, the parameters given in *Table 107* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 20*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- VOS level set to VOS0

Refer to *Section 5.3.14* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 107. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master receiver 1.71 V < V_{DD} < 3.6 V	-	-	31	MHz
		Master transmitter 2.7 V < V_{DD} < 3.6 V			31/6(2)	
		Master transmitter 1.71 V < V_{DD} < 3.6 V			31/6(2)	
		Slave receiver 1.71 V < V_{DD} < 3.6 V			83	
		Slave transmitter 2.7 V < V_{DD} < 3.6 V			34/6(2)	
		Slave transmitter 1.71 V < V_{DD} < 3.6 V			32/6(2)	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker}(3) + 6.5	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2.5	-	-	
$t_{w(CKH)}$ $t_{w(CKL)}$	CK high and low time	Master mode	$1/f_{ck}/2$ -1	$1/f_{ck}/2$	$1/f_{ck}/2$ +1	
$t_{su(RX)}$	Data input setup time	Master mode	13	-	-	
		Slave mode	3.5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0.5	-	-	
		Slave mode	1.5	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode, 2.7 V < V_{DD} < 3.6 V	-	11.5	14.5/38.5(2)	
		Slave mode, 1.71 V < V_{DD} < 3.6 V	-		15.5/71.5(2)	
		Master mode, 2.7 V < V_{DD} < 3.6 V	-	2.5	3/24.5(2)	
		Master mode, 1.71 V < V_{DD} < 3.6 V	-		3/54(2)	

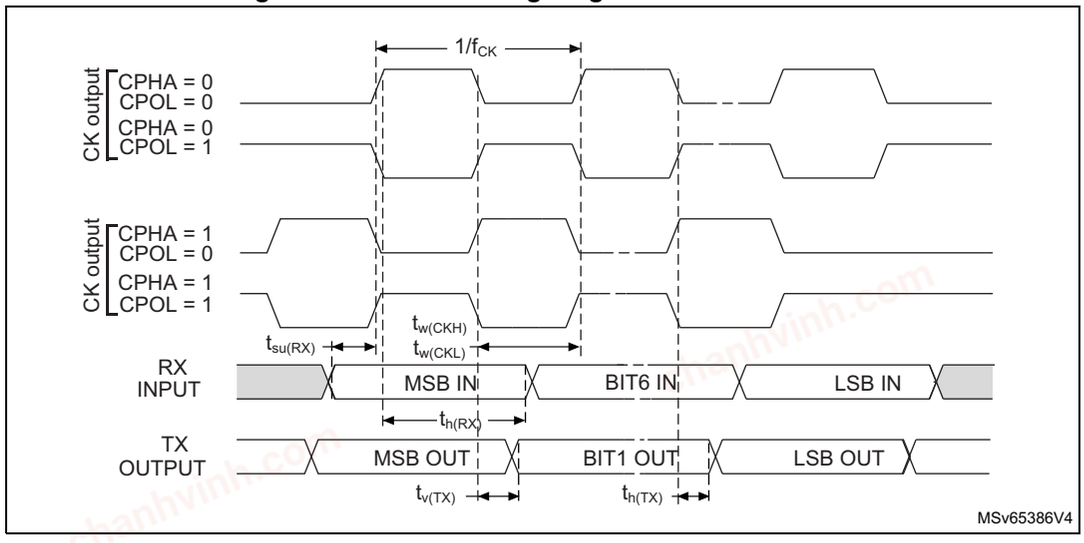
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Table 107. USART characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(TX)}$	Data output hold time	Slave mode	7.5	-	-	ns
		Master mode	0	-	-	

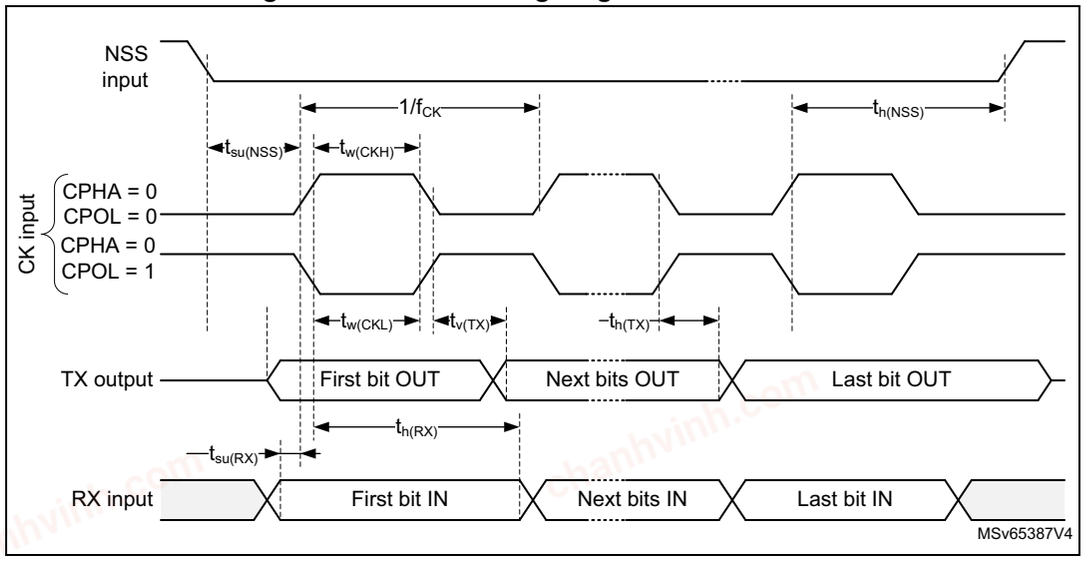
1. Evaluated by characterization - Not tested in production.
2. For PB14 with OSPEEDRy[1:0] = 01.
3. T_{ker} is the usart_ker_ck_pres clock period.

Figure 47. USART timing diagram in Master mode



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 48. USART timing diagram in Slave mode



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I3C interface characteristics

The I3C interface meets the timings requirements of the MIPI® I3C specification v1.1.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

The parameters given in *Table 108* are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V
- VOS level set to VOS 0

The timings are in line with MIPI specification, except for the ones given in *Table 108* and *Table 109*. For t_{SU_OD} and t_{SU_PP} this can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register. For t_{SCO} this can be mitigated by enabling and adjusting the clock stall time both on the address ACK phase and on the data read Tbit phase in the I3C_TIMINGR2 register. This can also be mitigated by increasing the SCL low duration in the I3C_TIMINGR0 register. For further details refer to AN5879.

Table 108. I3C open-drain measured timing

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SU_OD}	SDA data setup time during open drain mode	Controller 1.71 V < V_{DD} < 3.6 V	3	-	16.5	ns

Table 109. I3C push-pull measured timing

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SU_PP}	SDA signal data setup in push-pull mode	Controller 1.71 V < V_{DD} < 3.6 V	3	-	12	ns

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 110* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 20*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V

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- VOS level set to VOS0

Refer to *Section 5.3.14* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 110. SPI characteristics(1)

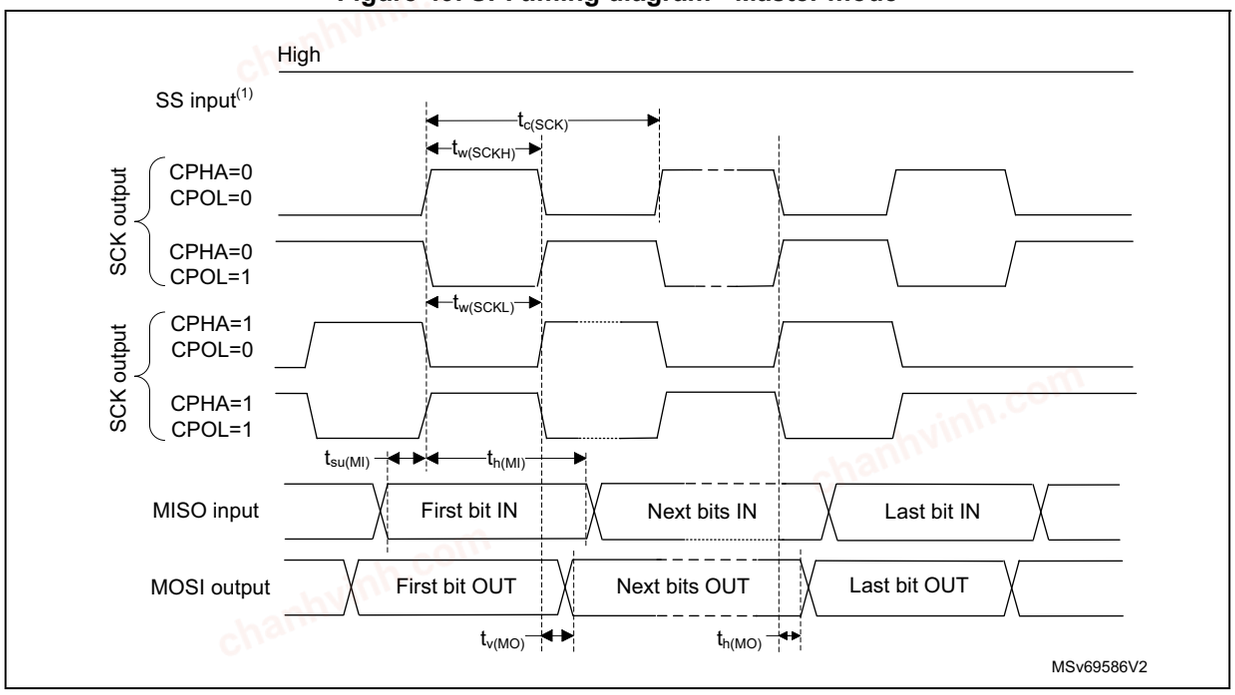
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{SCK}$	SPI clock frequency	Master receiver mode 2.7 V < V_{DD} < 3.6 V	-	-	135/3(2)	MHz
		Master receiver mode 1.71 V < V_{DD} < 2.7 V	-	-	120/3(2)	
		Master transmitter mode 2.7 V < V_{DD} < 3.6 V			135/3(2)	
		Master transmitter mode 1.71 V < V_{DD} < 2.7 V	-	-	120/3(2)	
		Slave receiver mode 1.71 V < V_{DD} < 3.6 V	-	-	120	
		Slave transmitter mode 2.7 V < V_{DD} < 3.6 V	-	-	43(3)/6(4)	
		Slave transmitter mode 1.71 V < V_{DD} < 2.7 V	-	-	41.5(3)/6(4)	
$t_{su(NSS)}$	NSS setup time	Slave mode	3.5	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	4.5	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	t_{SCK}(5) - 1	t_{SCK}(5)	t_{SCK}(5) + 1	ns
$t_{su(MI)}$	Data input setup time	Master mode	3.5	-	-	ns
$t_{su(SI)}$		Slave mode	2	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	1	-	-	ns
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	6.5	13	15	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	7.5	13	18	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	10/26.5(4)	11.5/35.5(4)	ns
		Slave mode (after enable edge), 1.71 V < V_{DD} < 2.7 V	-	11/61.5(4)	12/76(4)	
$t_{v(MO)}$		Master mode (after enable edge)	-	1.5	2	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	6.5/20.5(4)	-	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	0	-	-	

1. Evaluated by characterization - Not tested in production.

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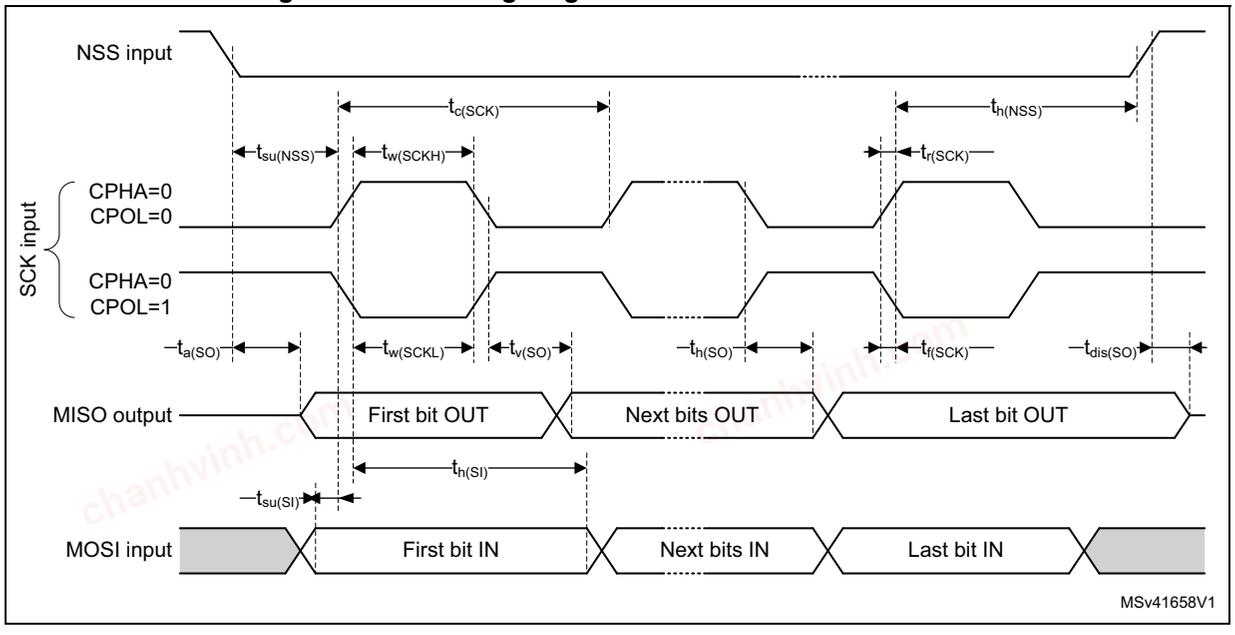
2. When using PB13.
3. Maximum frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which must fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%.
4. When using PB14.
5. $t_{SCK} = t_{ker_ck}$ * Baud rate prescaler.

Figure 49. SPI timing diagram - Master mode



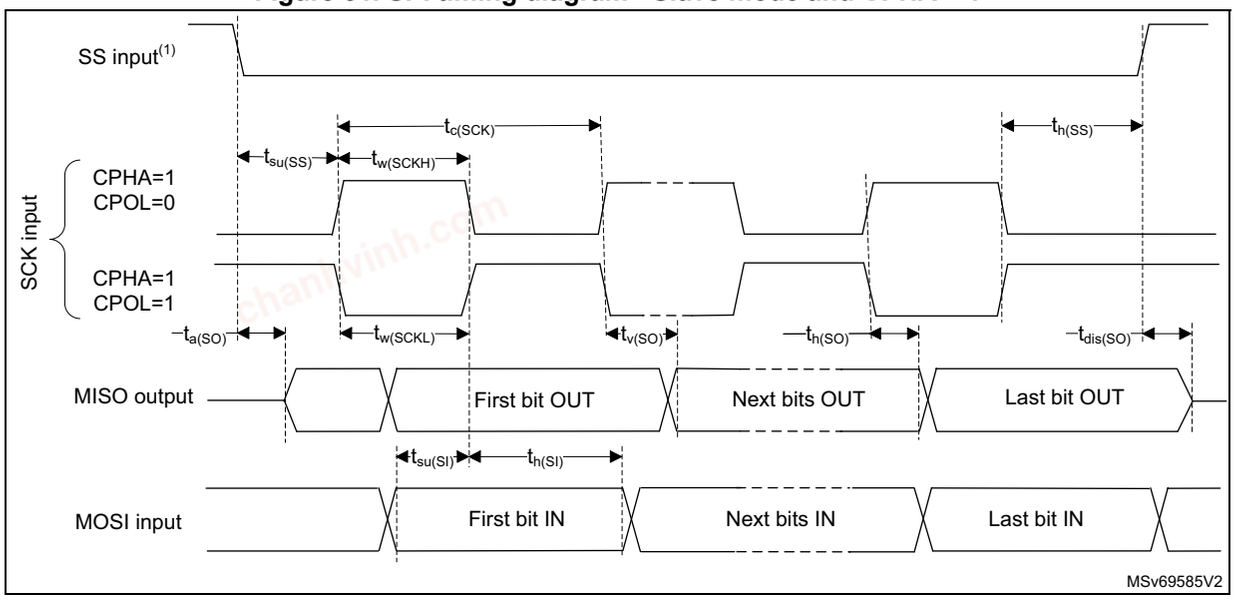
1. The SS input can be configured to active low or active high.

Figure 50. SPI timing diagram - Slave mode and CPHA = 0



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Figure 51. SPI timing diagram - Slave mode and CPHA = 1



1. The SS input can be configured to active low or active high.

I²S Interface characteristics

Unless otherwise specified, the parameters given in *Table 111* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 20*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 5.3.14* for more details on the input/output alternate function characteristics (CK,SD,WS).

Table 111. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I²S main clock output	-	-	50	MHz
f_{CK}	I²S clock output	Master transmitter	-	50	
		Slave transmitter (TX)	-	21	
		Slave receiver (RX)	-	50	

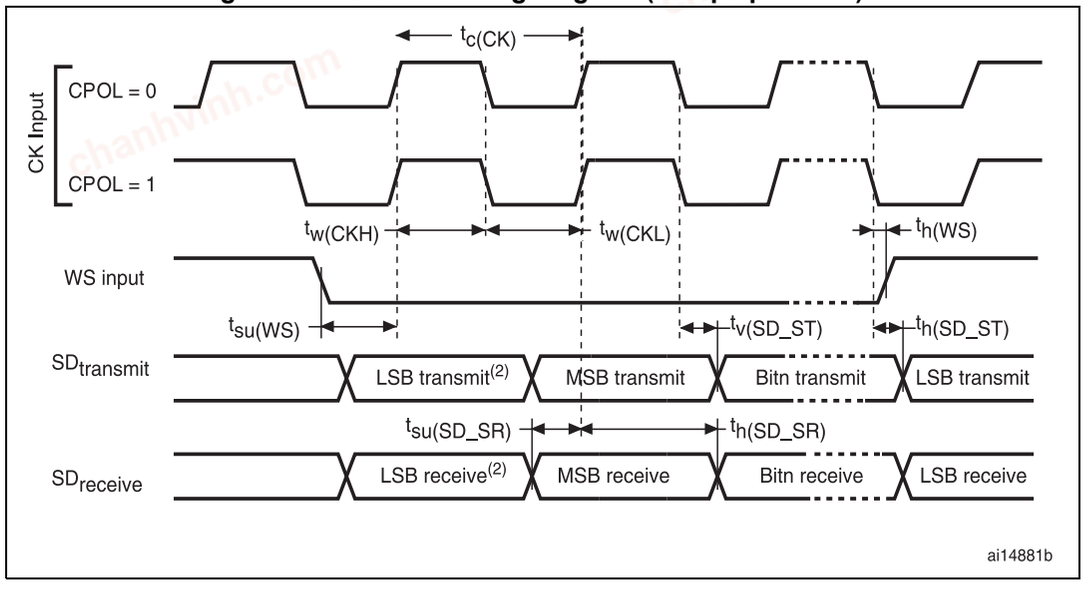
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Table 111. I²S dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(WS)}$	WS valid time	Master mode	-	2	ns
$t_{h(WS)}$	WS hold time		1	-	
$t_{su(WS)}$	WS setup time	Slave mode	3	-	
$t_{h(WS)}$	WS hold time		1.5	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	4	-	
$t_{su(SD_SR)}$		Slave receiver	2	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	1	-	
$t_{h(SD_SR)}$		Slave receiver	1.5	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	14	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	1	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5.5	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	

1. Evaluated by characterization - Not tested in production.

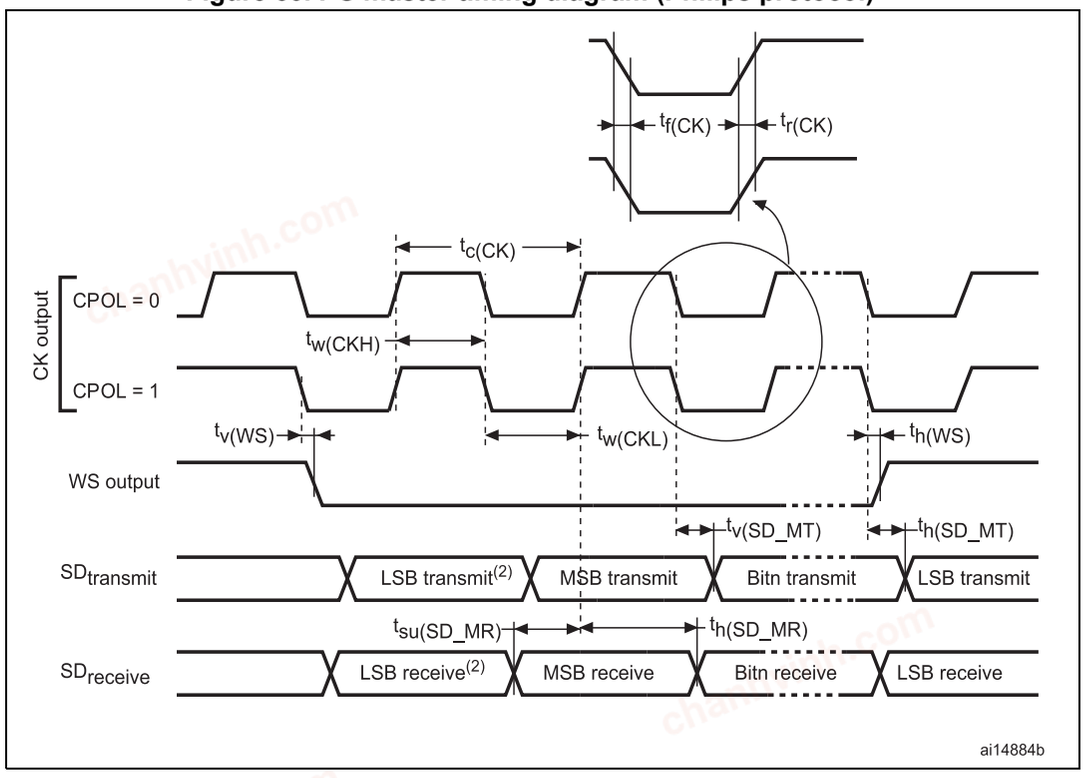
Figure 52. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

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Figure 53. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB full speed (FS) characteristics

The USB interface is fully compliant with the USB specification version 2.0.

Table 112. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	USB full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
V_{DI}(3)	Differential input sensitivity	Over VCM range	0.2	-	-	V
V_{CM}(3)	Differential input common mode range	Includes V_{DI} range	0.8	-	2.5	
V_{SE}(3)	Single ended receiver input threshold	-	0.8	-	2.0	
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}(3)	Pull down resistor on PA11, PA12 (USB_DP/DM)	V_{IN} = V_{DD}	14.25	-	24.8	kΩ
R_{PU}(3)	Pull-up resistor on PA12 (USB_DP)	V_{IN} = V_{SS}, during idle	0.9	1.25	1.575	
	Pull-up resistor on PA12 (USB_DP)	V_{IN} = V_{SS} during reception	1.425	2.25	3.09	

1. All the voltages are measured from the local ground potential.
2. The USB full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics, which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Specified by design - Not tested in production.

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4. R_L is the load connected on the USB full speed drivers.

Figure 54. USB timings - definition of data signal rise and fall time

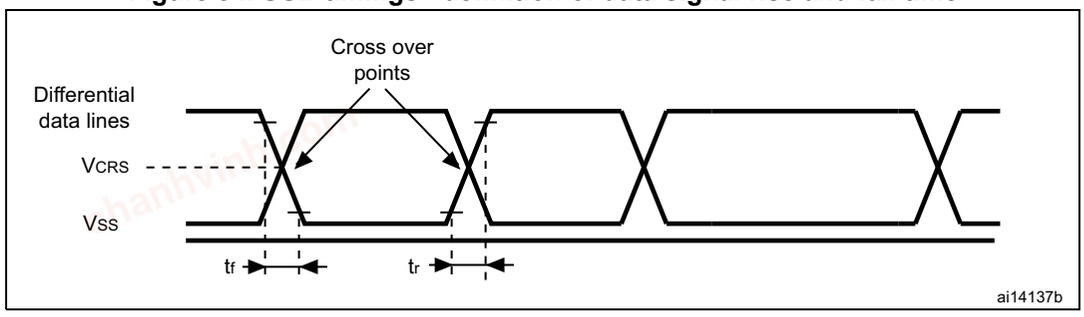


Table 113. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Specified by design - Not tested in production.

Table 114. USB electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rLS}	Rise time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{fLS}	Fall time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{rfmLS}	Rise/fall time matching in LS	t_r/t_f	80	125	%
t_{rFS}	Rise time in FS(2)	C_L = 50 pF	4	20	ns
t_{fFS}	Fall time in FS(2)	C_L = 50 pF	4	20	ns
t_{rfmFS}	Rise/fall time matching in FS	t_r/t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Specified by design - Not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed information, refer to USB specification - chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 115. USB BCD DC electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-	300	
RDAT_LKG	Data line leakage resistance	-	300	-	-	kΩ
VDAT_LKG	Data line leakage voltage	-	0.0	-	3.6	V

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Table 115. USB BCD DC electrical characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
VLGC_HI	Logic high	-	2.0	-	3.6	V
VLGC_LOW	Logic low	-	-	-	0.8	
VLGC	Logic threshold	-	0.8	-	2.0	
VDAT_REF	Data detect voltage	-	0.25	-	0.4	
VDP_SRC	D+ source voltage	-	0.5	-	0.7	
VDM_SRC	D- source voltage	-	0.5	-	0.7	
IDP_SINK	D+ sink current	-	25	-	175	µA
IDM_SINK	D- sink current	-	25	-	175	

1. Specified by design - Not tested in production.

SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 116* and *Table 117* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in *Table 20*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- HSLV activated when V_{DD} ≤ 2.7 V

Refer to *Section 5.3.14* for more details on the input/output characteristics.

Table 116. Dynamic characteristics: SD/MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}(2)	Clock frequency in data transfer mode	-	-	-	130/6 (3)	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} =52MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(4)/DDR(4) mode						
t_{ISU}	Input setup time HS	-	3	-	-	ns
t_{IH}	Input hold time HS	-	1	-	-	
t_{IDW}(5)	Input valid window (variable window)	-	4.5	-	-	
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(4)/DDR(4) mode						
t_{OV}	Output valid time HS	-	-	6.5	7/38(3)	ns
t_{OH}	Output hold time HS	-	3.5	-	-	

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Table 116. Dynamic characteristics: SD/MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	3		-	ns
t_{IHD}	Input hold time SD	-	1.5		-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	1.5	2/33(3)	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. Evaluated by characterization - Not tested in production.
2. C_L applied is 20 pF.
3. When using PB13 & PB14.
4. For SD 1.8 V support, an external voltage converter is needed.
5. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

Table 117. Dynamic characteristics: eMMC characteristics, V_{DD} = 1.71 to 1.9 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}(2)	Clock frequency in data transfer mode	-	-	-	110/6 (3)	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} =52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IH}	Input hold time HS	-	2	-	-	
t_{IDW}(4)	Input valid window (variable window)	-	4	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	-	-	6.5	7/5(3)	ns
t_{OH}	Output hold time HS	-	3.5	-	-	

1. Evaluated by characterization - Not tested in production.
2. C_L = 20 pF.
3. When using PB13 and PB14.
4. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

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Figure 55. SDIO high-speed/eMMC timing

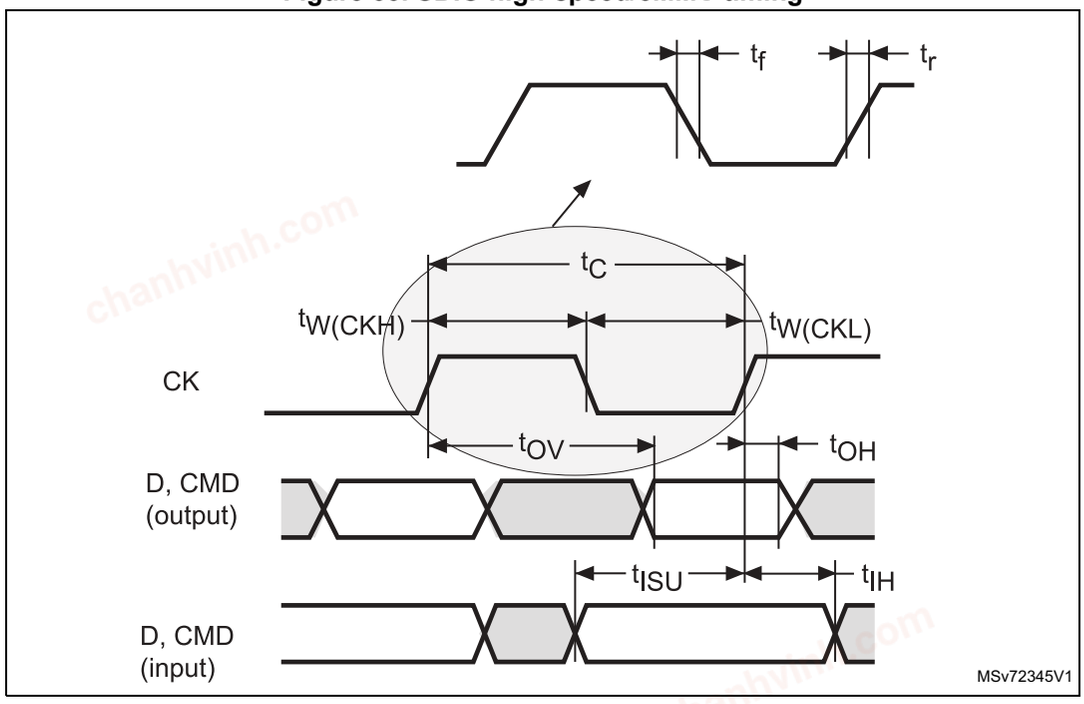


Figure 56. SD default speed timings

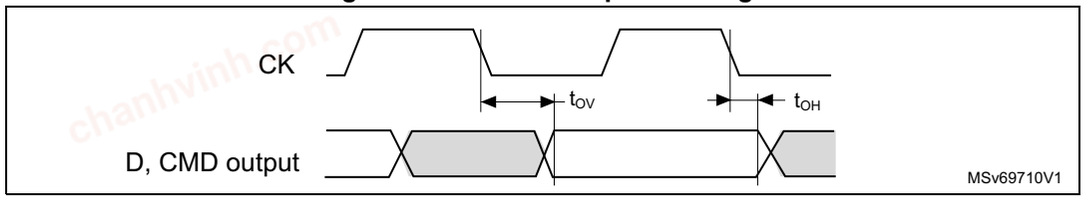
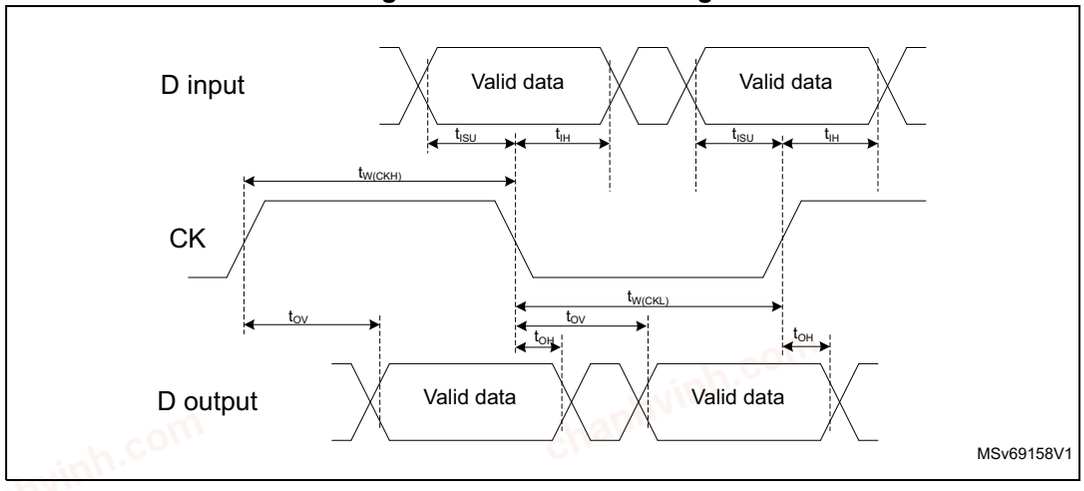


Figure 57. DDR mode timings



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JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 118* and *Table 119* for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in *Table 20*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L= 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.14* for more details on the input/output characteristics:

Table 118. Dynamic JTAG characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{TCK}	T_{CK} clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	47.5	MHz
$1/t_{c(TCK)}$		1.71 V < V_{DD} < 3.6 V	-	-	45	
$ti_{su(TMS)}$	TMS input setup time	-	3.5	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	-	1.5	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	2.5	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	1.5	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7V < V_{DD} < 3.6 V	-	8	10.5	
		1.71 < V_{DD} < 3.6 V	-	8	11	
$t_{oh(TDO)}$	TDO output hold time	-	6.5	-	-	

1. Evaluated by characterization - Not tested in production.

Table 119. Dynamic SWD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{SWCLK}	SWCLK clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	80	MHz
$1/t_{c(SWCLK)}$		1.71 V < V_{DD} < 3.6 V	-	-	71	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	1.5	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time	-	1.5	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	2.7 V < V_{DD} < 3.6 V	-	10.5	12.5	
		1.71 V < V_{DD} < 3.6 V	-	10.5	14.0	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8.5	-	-	

1. Evaluated by characterization - Not tested in production.

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Figure 58. JTAG timing diagram

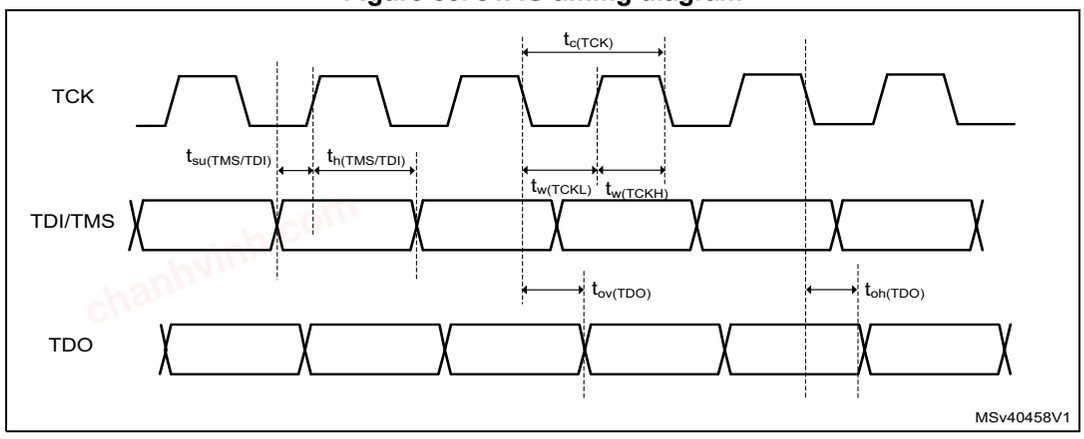
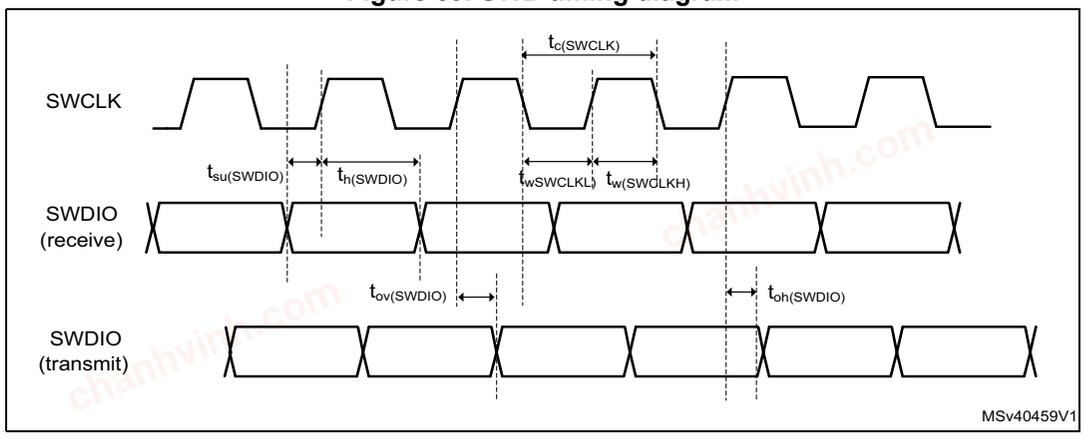


Figure 59. SWD timing diagram



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6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 Device marking

Refer to “*Reference device marking schematics for STM32 microcontrollers and microprocessors*” (TN1433), available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

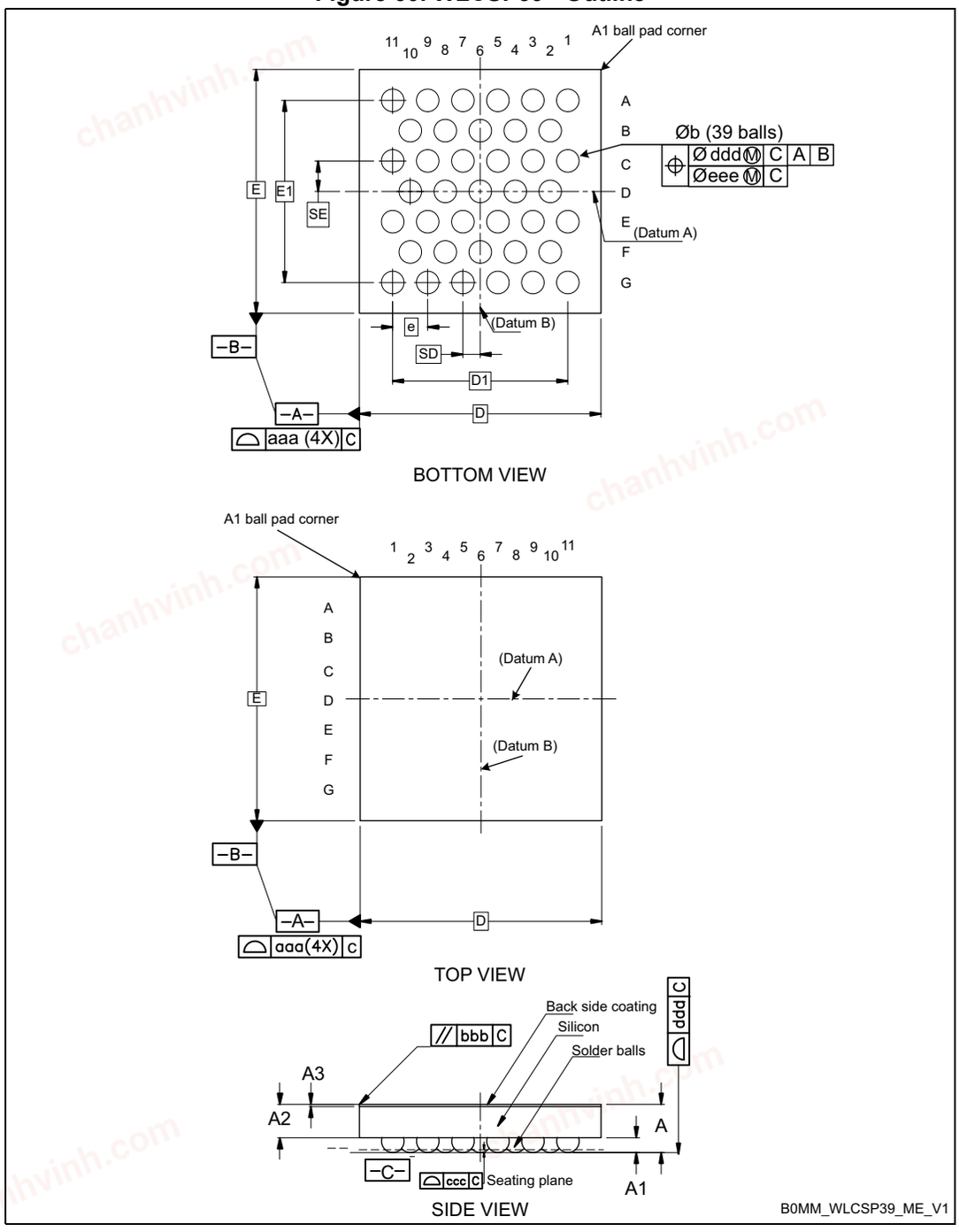
A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

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6.2 WLCSP39 package information (B0MM)

This WLCSP is a 39-ball, 2.76 x 2.78 mm, 0.4 mm pitch, wafer level chip scale array package.

Figure 60. WLCSP39 - Outline



1. Drawing is not to scale.
2. The A1 corner must be identified on the top surface of the package by using a marking or a physical feature. A distinguish feature is allowable on the bottom surface of the package to identify the A1 corner. Exact shape of each corner is optional.

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Table 120. WLCSP39 - Mechanical data

Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.58	-	-	0.0228
A1[3]	-	0.17	-	-	0.0067	-
A2	-	0.38	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b[4]	0.23	0.26	0.28	0.0091	0.0102	0.0110
D	2.76 BSC[5]			0.1087 BSC		
D1	2.000 BSC			0.0787 BSC		
E	2.78 BSC			0.1094 BSC		
E1	2.078 BSC			0.0818 BSC		
e[6]	0.40 BSC			0.0157 BSC		
SD[7]	0.200 BSC			0.0079 BSC		
SE[7]	0.346 BSC			0.0136 BSC		
N	39[8]					
aaa[9]	0.02 BSC			0.0008 BSC		
bbb[9]	0.06 BSC			0.0024 BSC		
ccc[9]	0.03 BSC			0.0012 BSC		
ddd[9]	0.015 BSC			0.0006 BSC		
eee[9]	0.05 BSC			0.0020 BSC		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to datum C.
5. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance.
6. e represents the solder balls grid pitch(es).
7. Basic dimensions SD and SE are defining the ball matrix position with respect to datums A and B.
8. N represents the total number of balls.
9. The tolerance of position that controls the location of the balls within the matrix with respect to each other.

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Figure 61. WLCSP39 - Footprint example

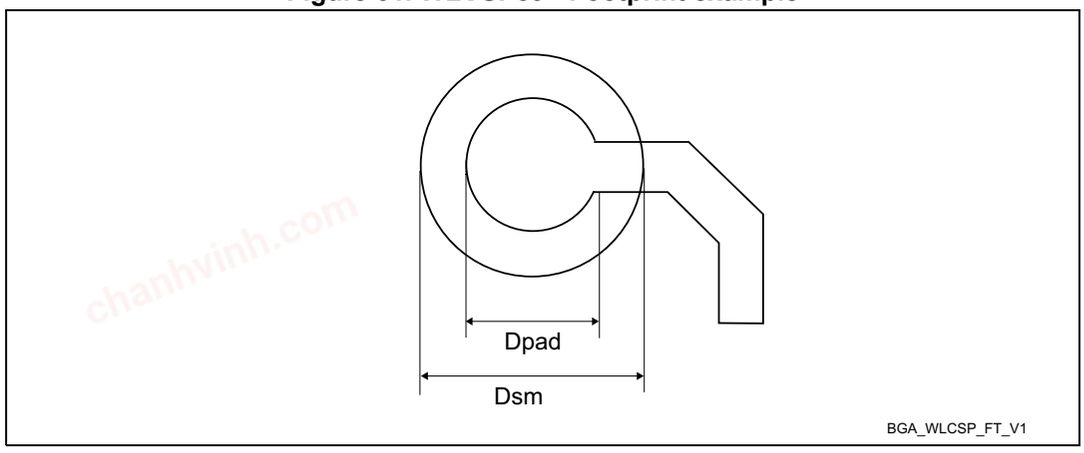
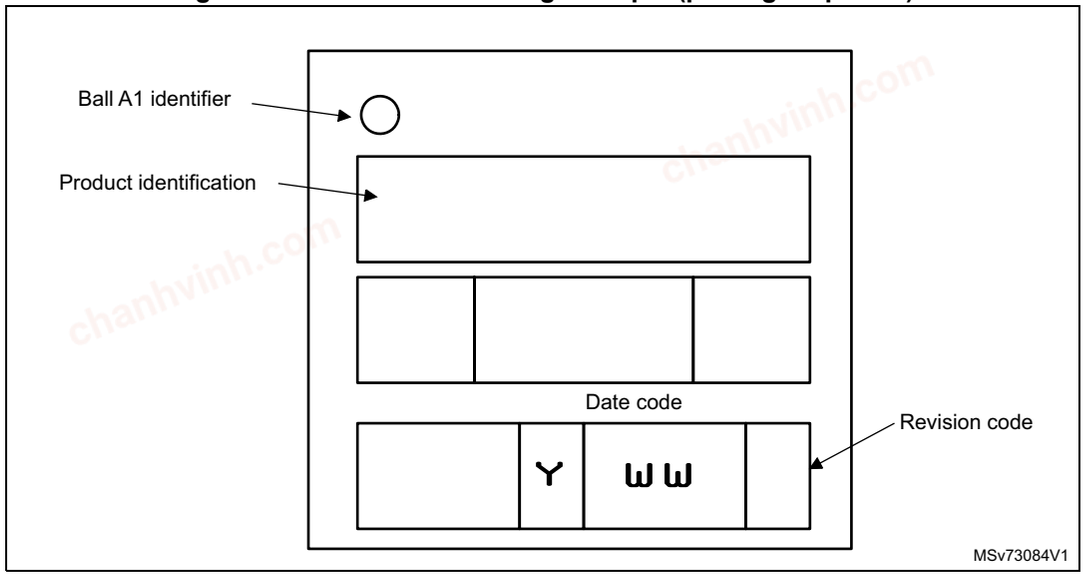


Figure 62. WLCSP39 - Marking example (package top view)



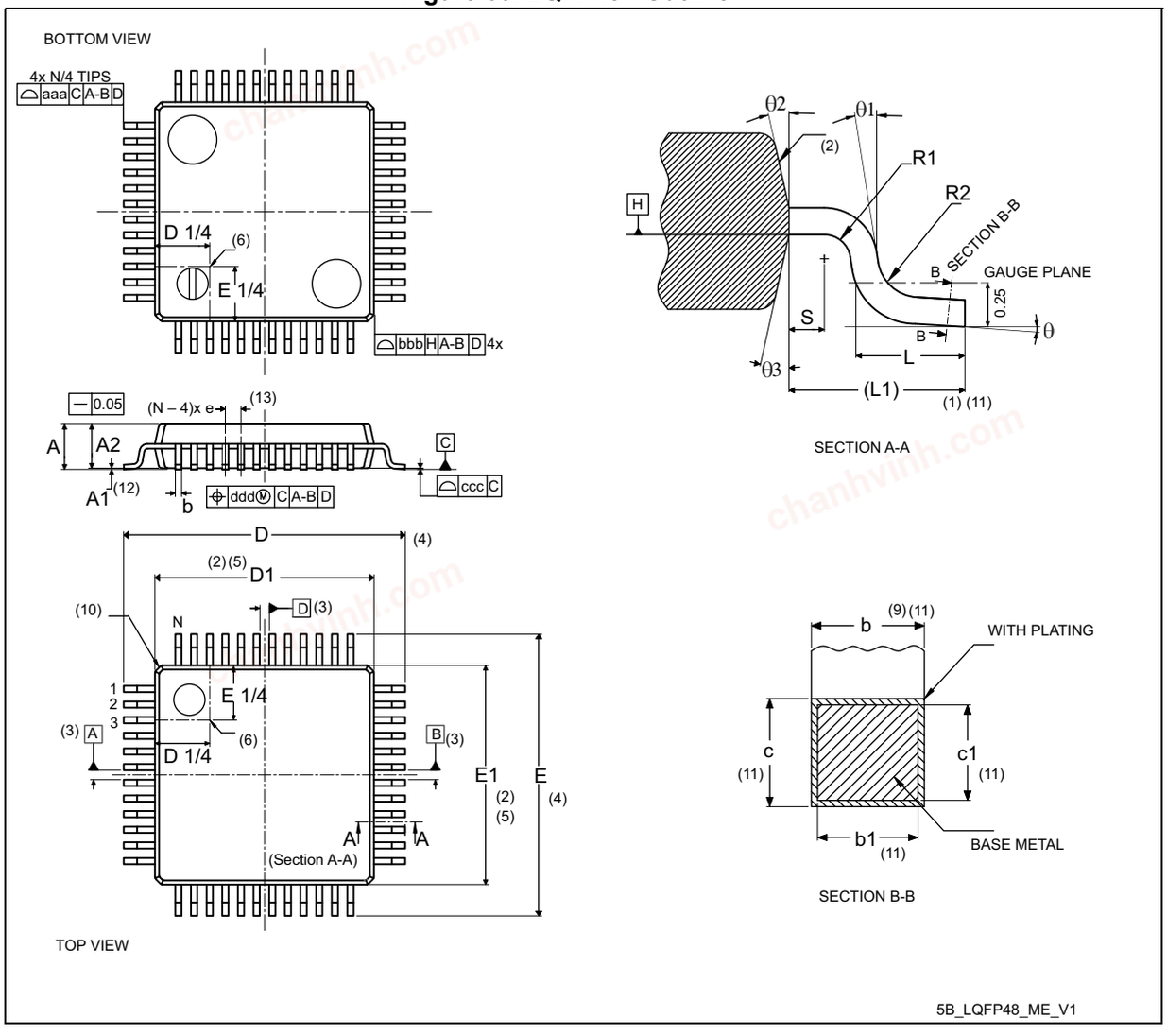
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6.3 LQFP48 package information (5B)

This LQFP is a 48-pin, 7 x 7 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 63. LQFP48 - Outline(15)



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Table 121. LQFP48 - Mechanical data

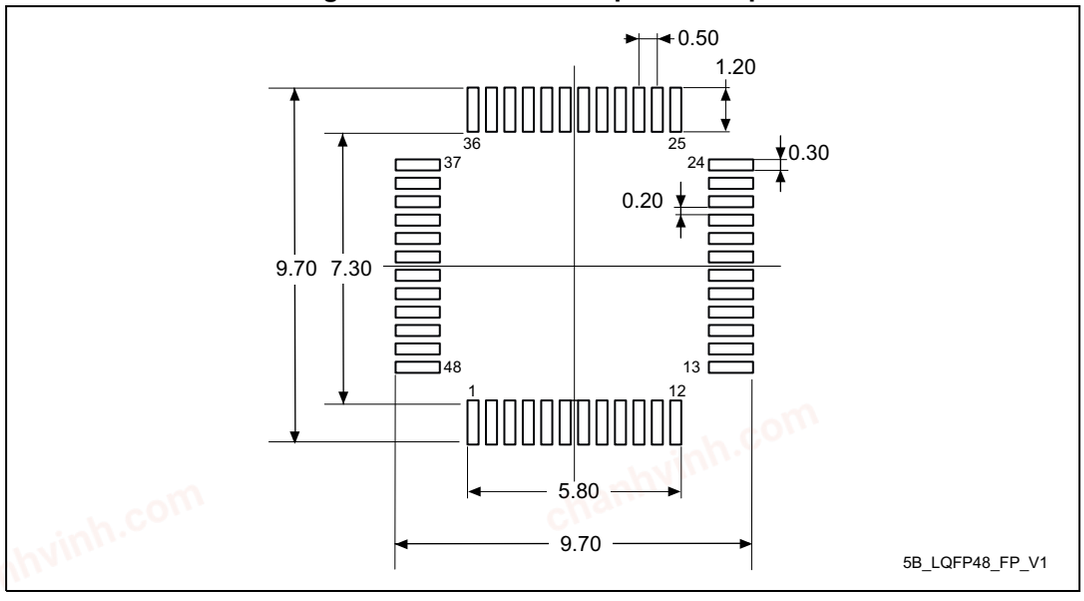
Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	9.00 BSC			0.3543 BSC		
D1[2][5]	7.00 BSC			0.2756 BSC		
E[4]	9.00 BSC			0.3543 BSC		
E1[2][5]	7.00 BSC			0.2756 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	48					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1][7]	0.20			0.0079		
bbb[1][7]	0.20			0.0079		
ccc[1][7]	0.08			0.0031		
ddd[1][7]	0.08			0.0031		

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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 64. LQFP48 - Footprint example



1. Dimensions are expressed in millimeters.

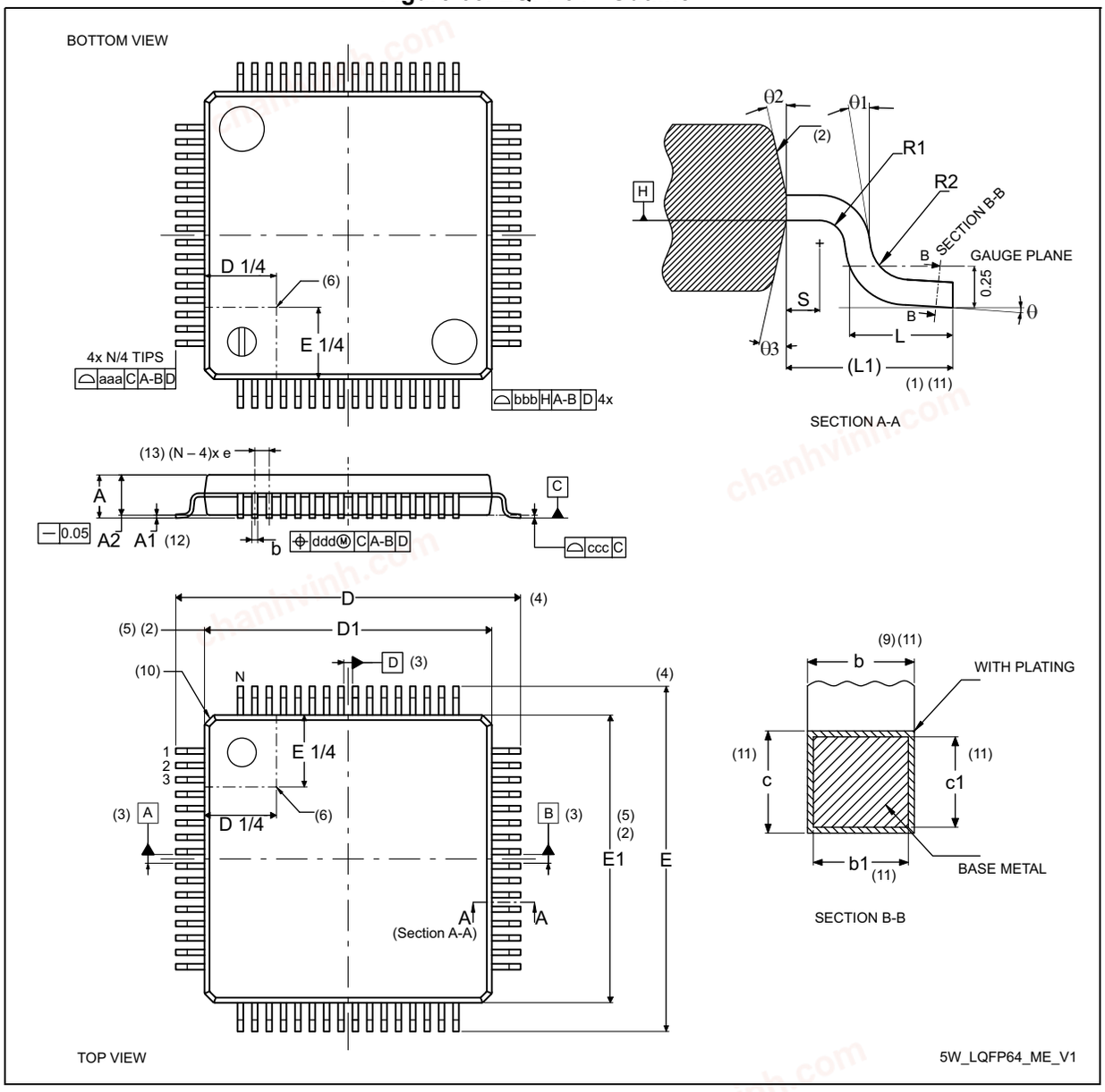
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6.4 LQFP64 package information (5W)

This LQFP is 64-pin, 10 x 10 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 65. LQFP64 - Outline(15)



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Table 122. LQFP64 - Mechanical data

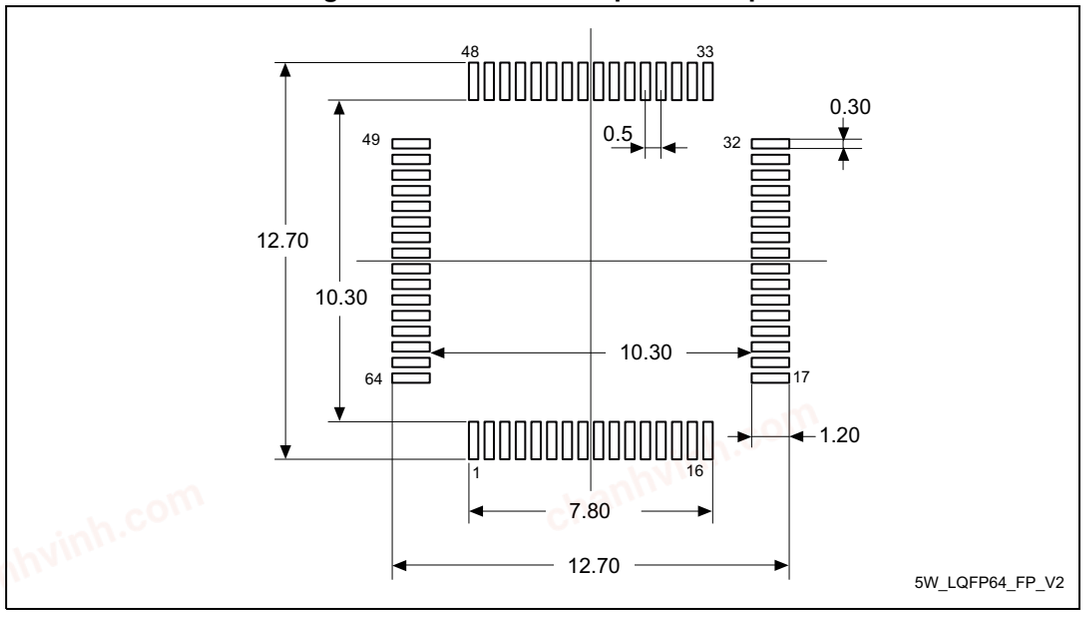
Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	12.00 BSC			0.4724 BSC		
D1[2][5]	10.00 BSC			0.3937 BSC		
E[4]	12.00 BSC			0.4724 BSC		
E1[2][5]	10.00 BSC			0.3937 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	64					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 66. LQFP64 - Footprint example



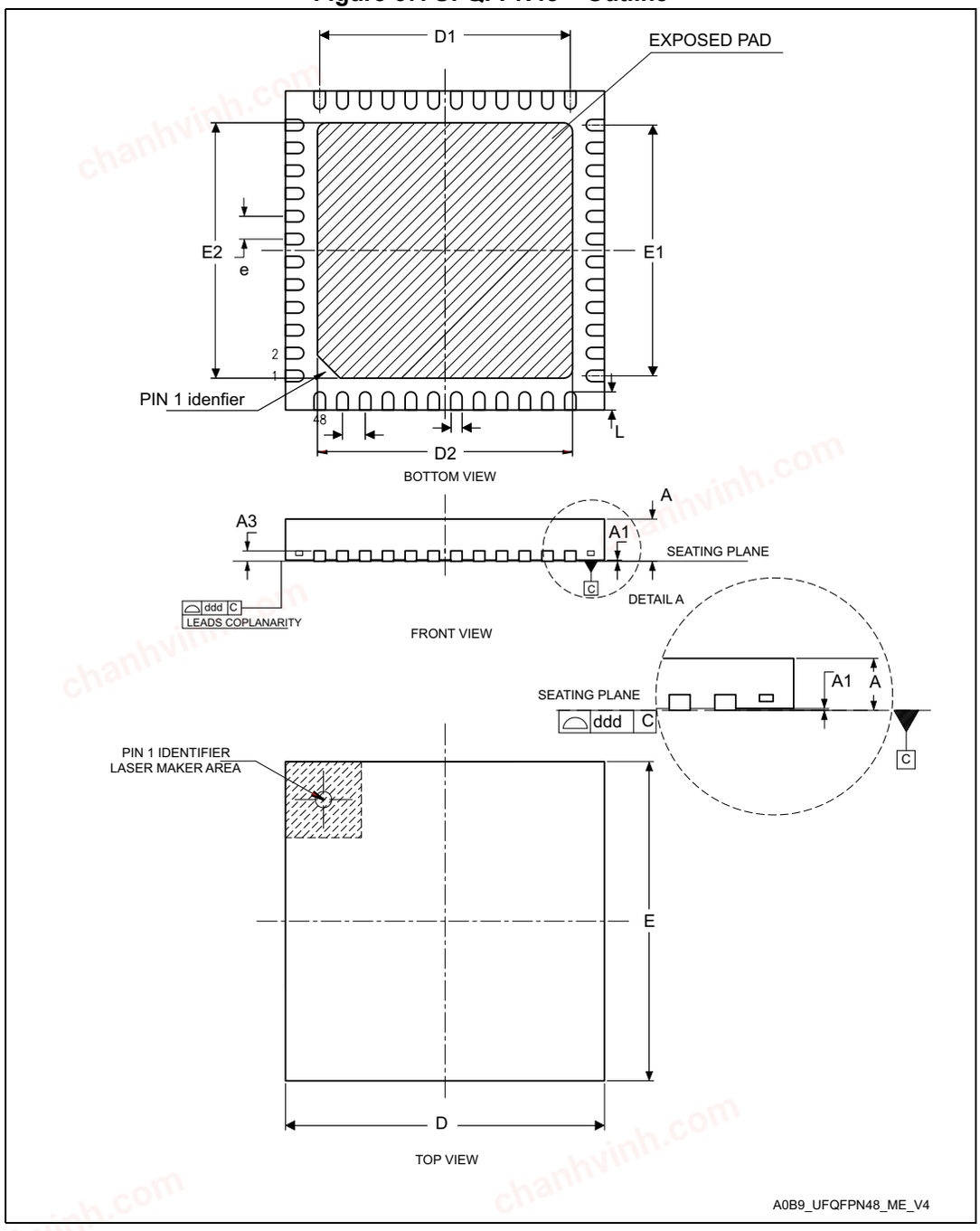
1. Dimensions are expressed in millimeters.

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6.5 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 67. UFQFPN48 – Outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.

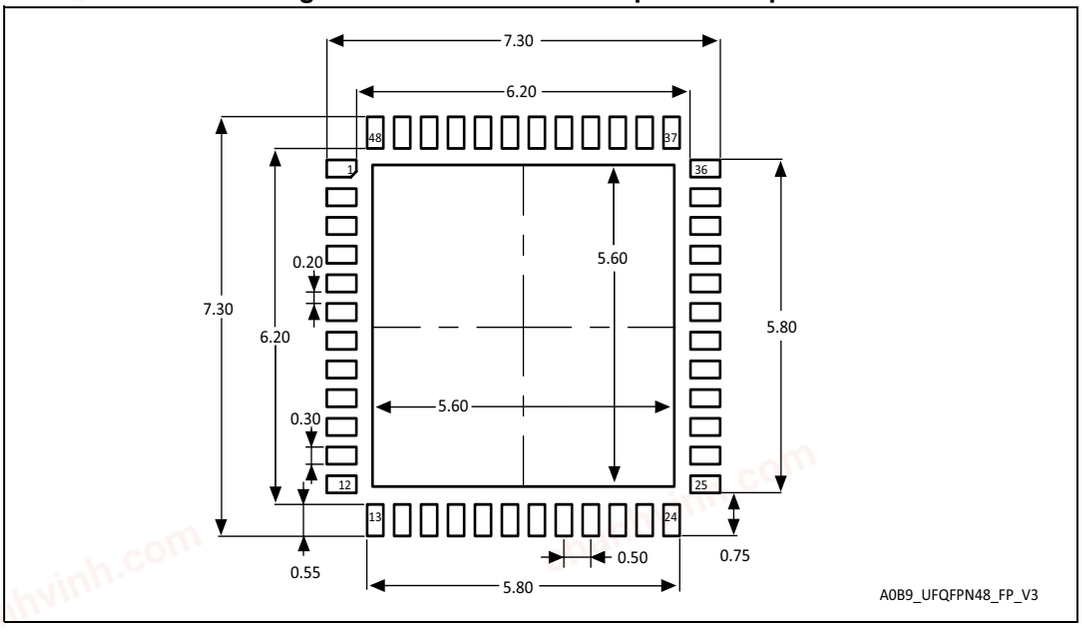
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Table 123. UFQFPN48 – Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
D1	5.400	5.500	5.600	0.2126	0.2165	0.2205
D2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
E[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
E1	5.400	5.500	5.600	0.2126	0.2165	0.2205
E2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.
3. Dimensions D2 and E2 are not in accordance with JEDEC.

Figure 68. UFQFPN48 – Footprint example



1. Dimensions are expressed in millimeters.

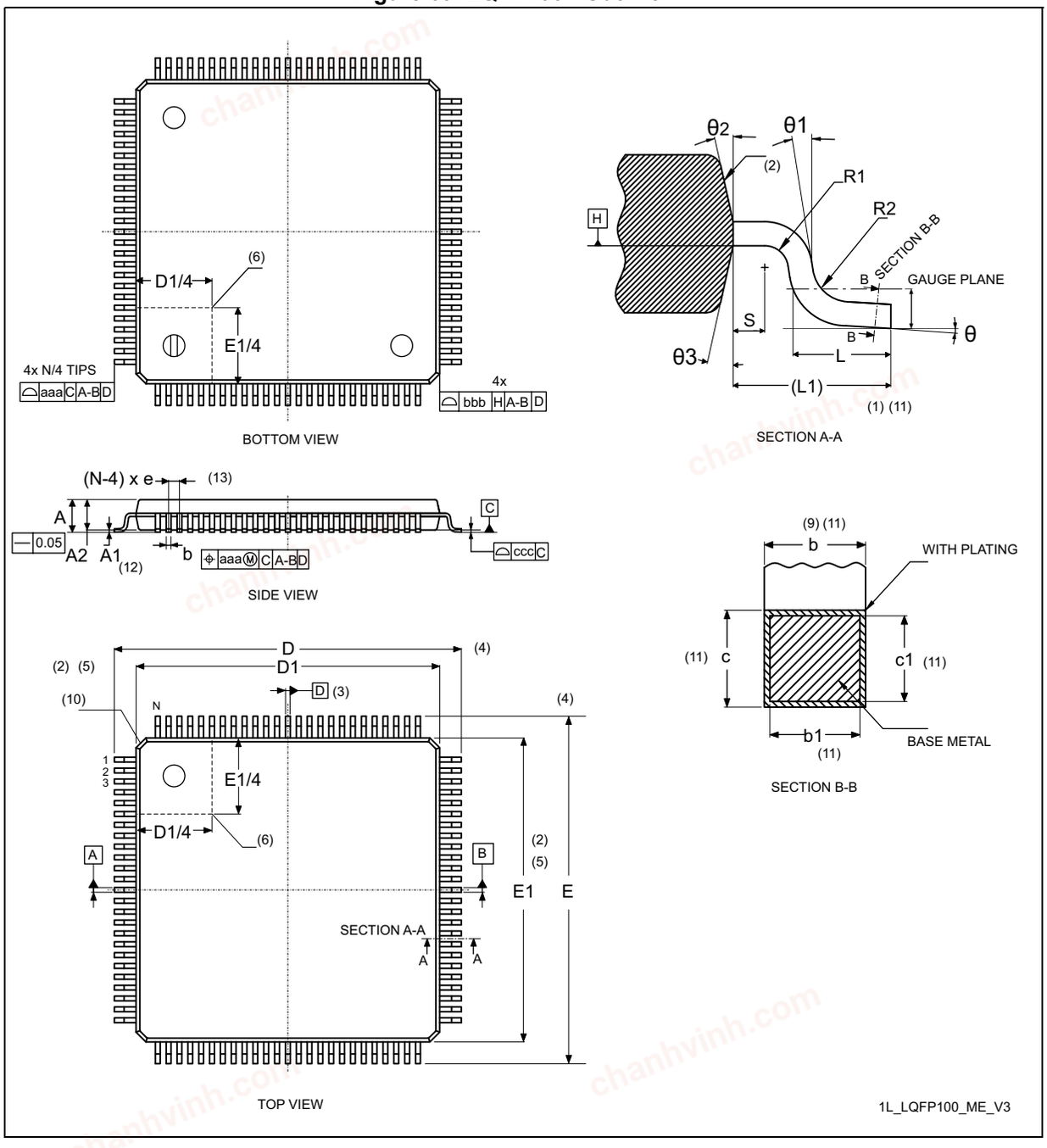
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6.6 LQFP100 package information (1L)

This LQFP is 100 lead, 14 x 14 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 69. LQFP100 - Outline(15)



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Table 124. LQFP100 - Mechanical data

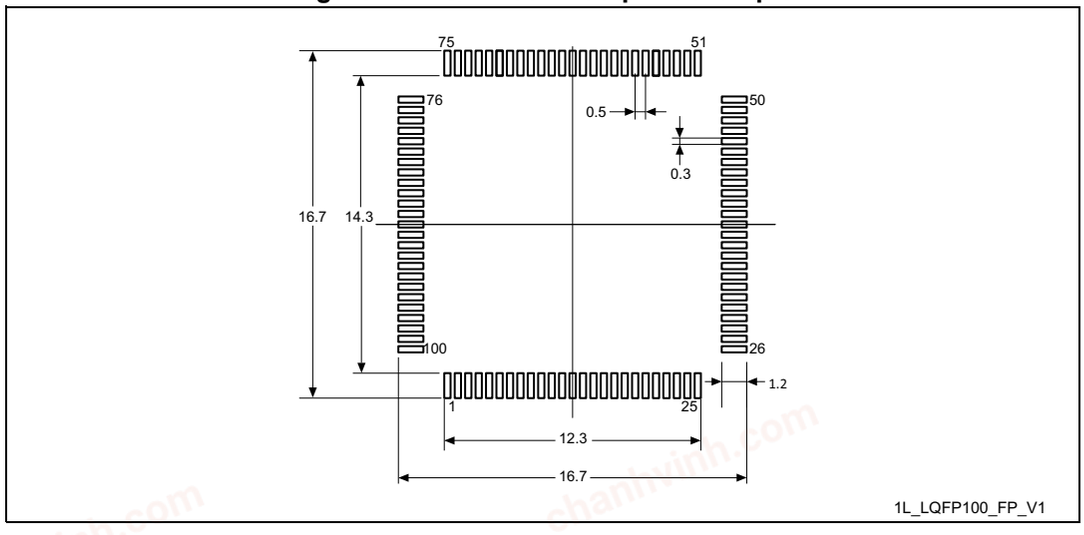
Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1[12]	0.05	-	0.15	0.0019	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	16.00 BSC			0.6299 BSC		
D1[2][5]	14.00 BSC			0.5512 BSC		
E[4]	16.00 BSC			0.6299 BSC		
E1[2][5]	14.00 BSC			0.5512 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.177	0.0236	0.0295
L1[1][11]	1.00			-	0.0394	-
N[13]	100					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 70. LQFP100 - Footprint example



1. Dimensions are expressed in millimeters.

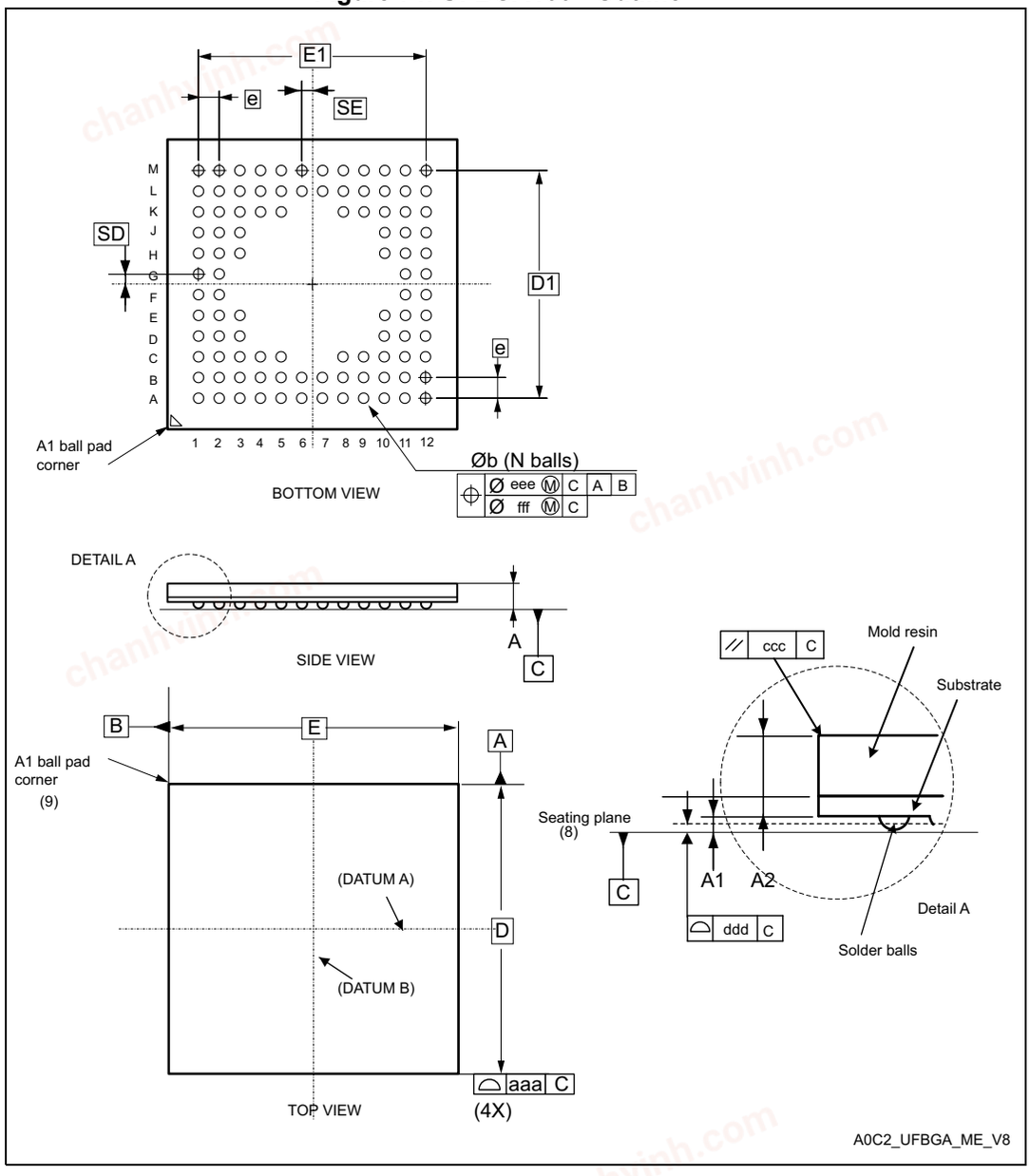
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6.7 UFBGA100 package information (A0C2)

This UFBGA is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 71. UFBGA100 - Outline(13)



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Table 125. UFBGA100 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2][3]	-	-	0.60	-	-	0.0236
A1[4]	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-
b[5]	0.23	0.28	0.33	0.0090	0.0110	0.0130
D[6]	7.00 BSC			0.2756 BSC		
D1	5.50 BSC			0.2165 BSC		
E	7.00 BSC			0.2756 BSC		
E1	5.50 BSC			0.2165 BSC		
e[9]	0.50 BSC			0.0197 BSC		
N[11]	100					
SD[12]	0.25 BSC			0.0098 BSC		
SE[12]	0.25 BSC			0.0098 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.05			0.0020		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ulta profile fine pitch ball grid array: 0.50 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metalized markings, or other feature of package body or

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integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

Figure 72. UFBGA100 - Footprint example

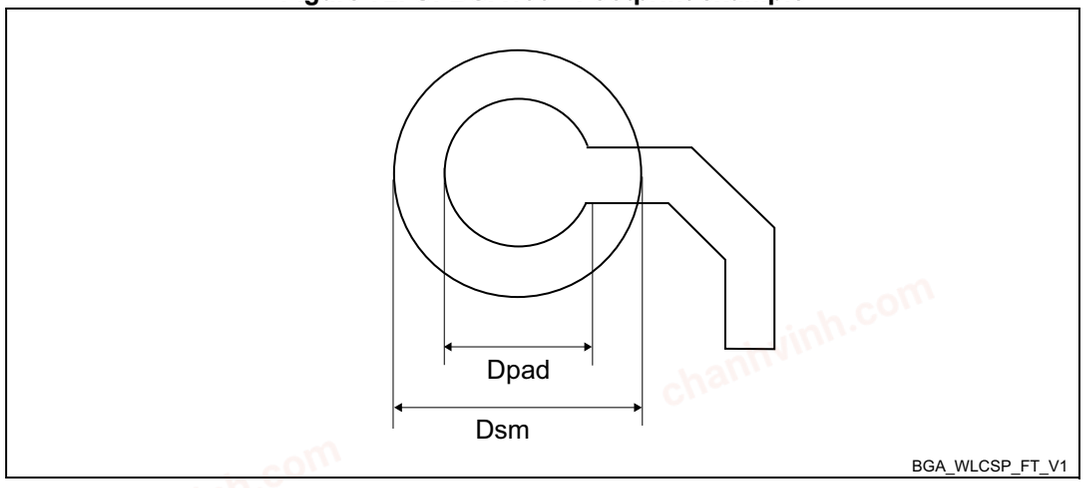


Table 126. UFBGA100 - Example of PCB design rules (0.5 mm pitch BGA)

Dimension	Values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the solder mask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

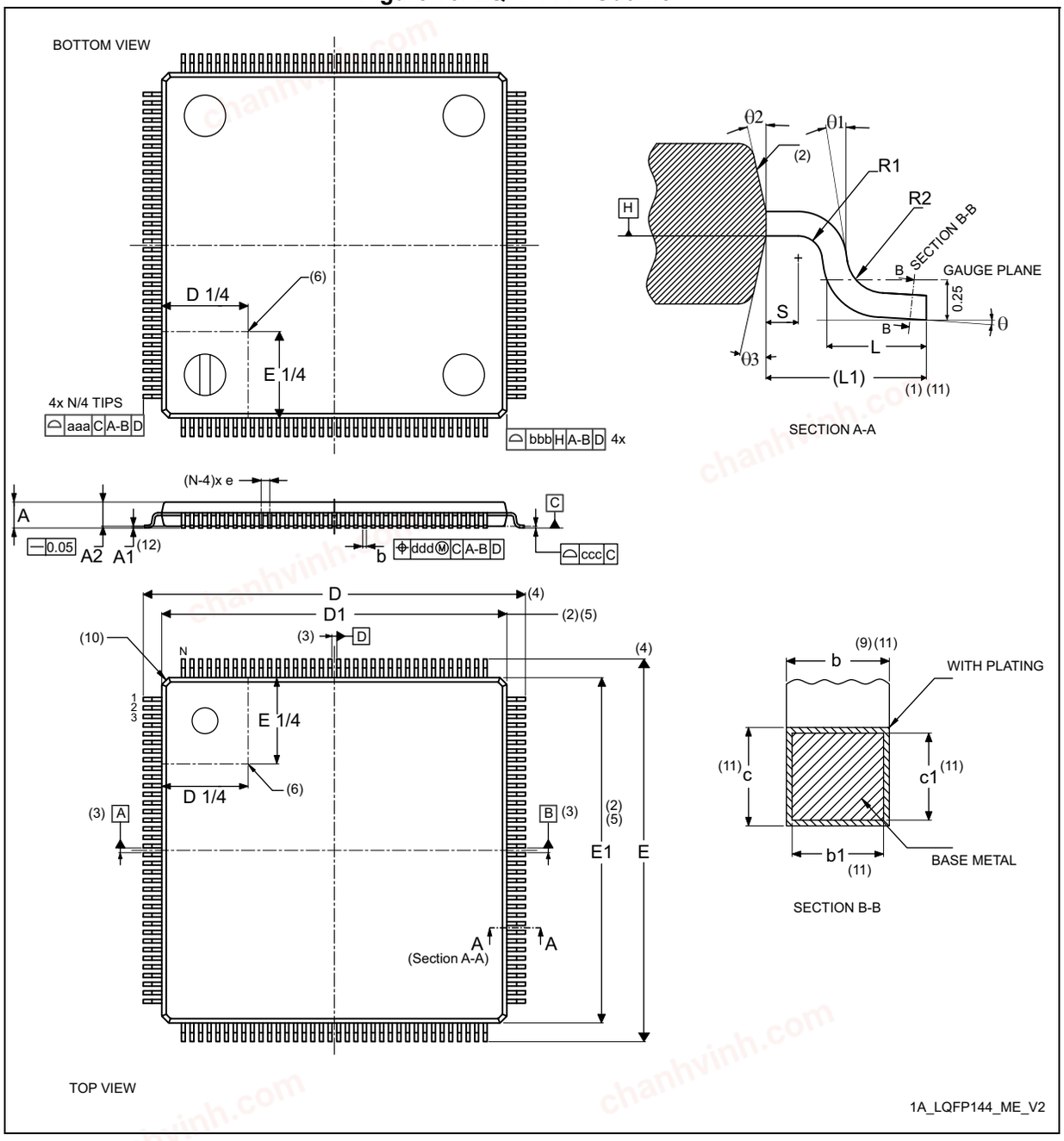
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6.8 LQFP144 package information (1A)

This LQFP is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 73. LQFP144 - Outline(15)



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Table 127. LQFP144 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	22.00 BSC			0.8661 BSC		
D1[2][5]	20.00 BSC			0.7874 BSC		
E[4]	22.00 BSC			0.8661 BSC		
E1[2][5]	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	144					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

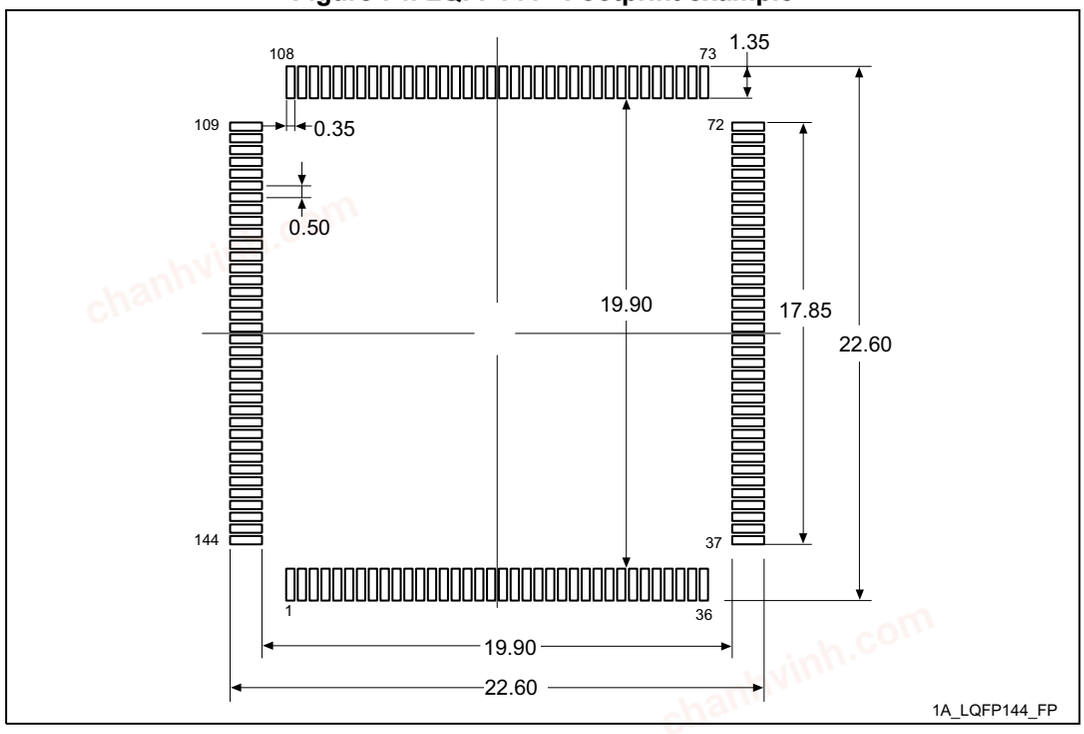
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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

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Figure 74. LQFP144 - Footprint example



1. Dimensions are expressed in millimeters.

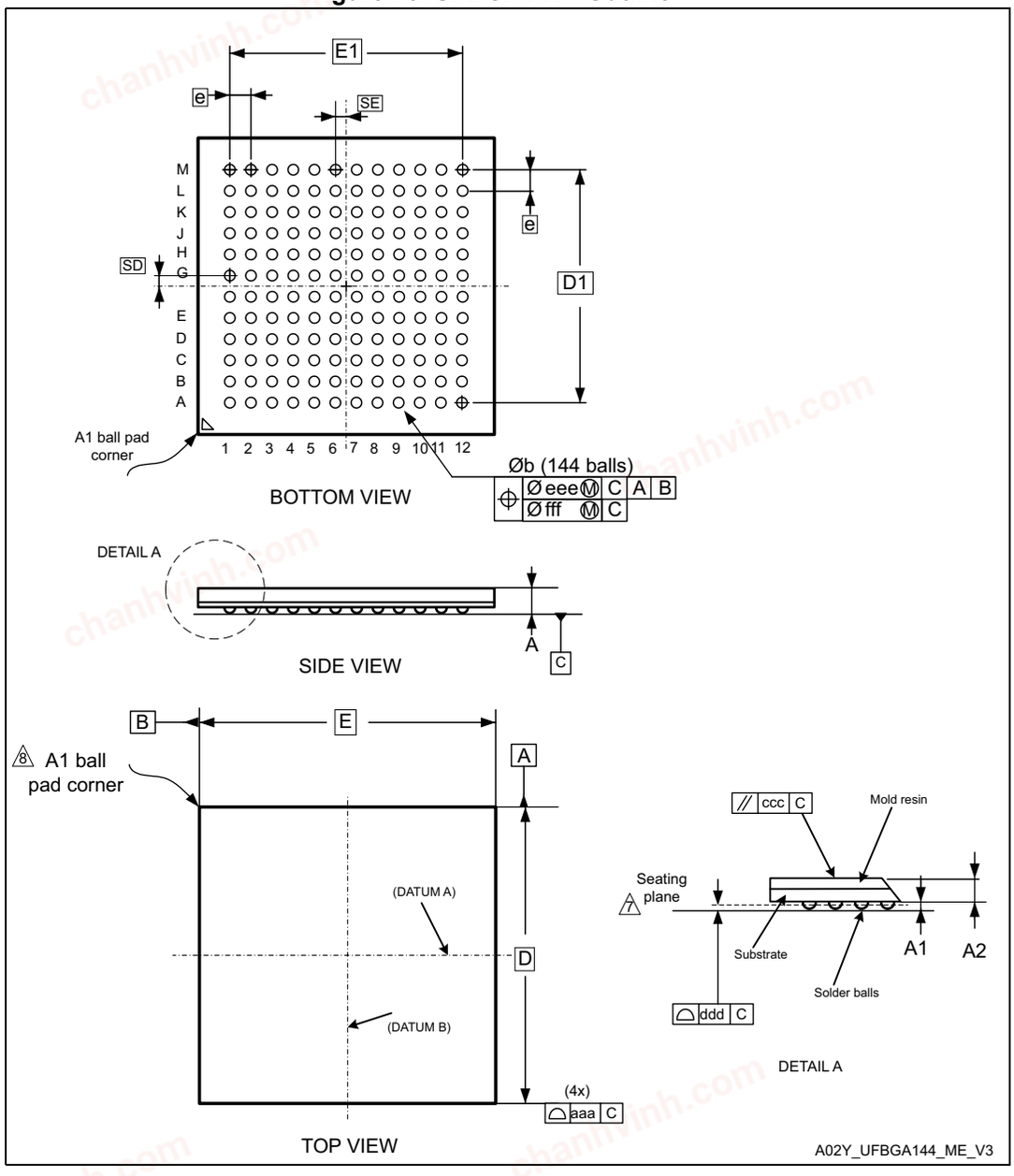
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6.9 UFBGA144 package information (A0Y2)

This UFBGA is a 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 75. UFBGA144 - Outline(13)



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Table 128. UFBGA144 - Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2][3]	-	-	0.60	-	-	0.0236
A1[4]	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-
b[5]	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	10.00 BSC[6]			0.3937 BSC		
D1	8.80 BSC			0.3465 BSC		
E	10.00 BSC			0.3937 BSC		
E1	8.80 BSC			0.3465 BSC		
e[9]	0.80 BSC			0.0315 BSC		
N[11]	144					
SD[12]	0.40 BSC			0.0157 BSC		
SE[12]	0.40 BSC			0.0157 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ulta profile fine pitch ball grid array: 0.50 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metalized markings, or other feature of package body or

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integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

Figure 76. UFBGA144 - Footprint example

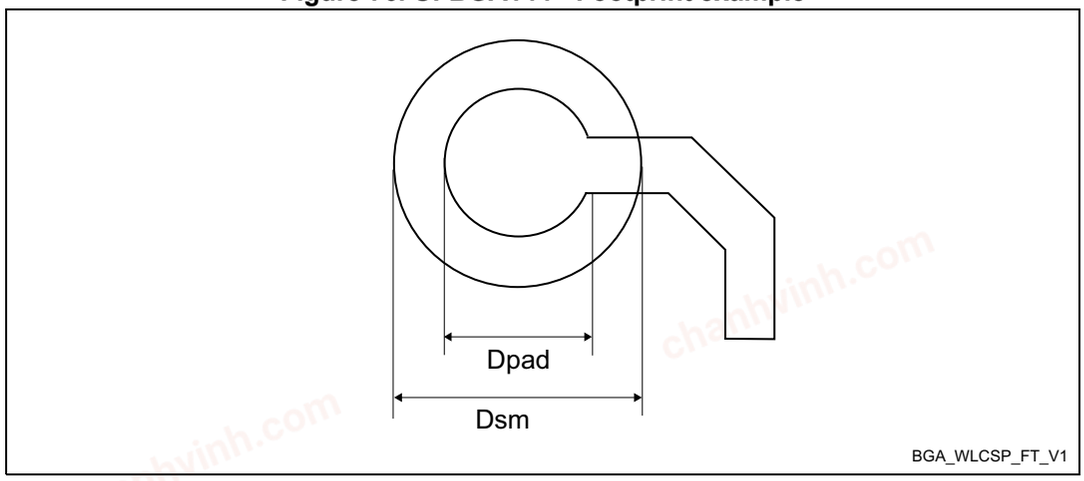


Table 129. UFBGA144 - Example of PCB design rules (0.80 mm pitch BGA)

Dimension	Values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

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6.10 Package thermal characteristics

The maximum chip-junction temperature, T_{Jmax} in degrees Celsius, can be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$),
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins:

$$P_{I/Omax} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} – V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 130. Package thermal characteristics

Symbol	Definition	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	WLCSP39 (2.76 x 2.78 mm)	65.3	°C/W
		UFQFPN48 (7 x 7 mm)	28.5	
		LQFP48 (7 x 7 mm)	51.2	
		LQFP64 (10 x 10 mm)	44.2	
		LQFP100 (14 x 14 mm)	36.4	
		UFBGA100 (7 x 7 mm)	50	
		LQFP144 (20 x 20 mm)	37.9	
		UFBGA144 (10 x 10 mm)	45.5	
Θ_{JB}	Thermal resistance junction-board	WLCSP39 (2.76 x 2.78 mm)	38	°C/W
		UFQFPN48 (7 x 7 mm)	12.9	
		LQFP48 (7 x 7 mm)	28.6	
		LQFP64 (10 x 10 mm)	26.6	
		LQFP100 (14 x 14 mm)	22.3	
		UFBGA100 (7 x 7 mm)	35.8	
		LQFP144 (20 x 20 mm)	26.7	
		UFBGA144 (10 x 10 mm)	33.4	

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Table 130. Package thermal characteristics (continued)

Symbol	Definition	Parameter	Value	Unit
Θ_{JC}	Thermal resistance junction-case	WLCSP39 (2.76 x 2.78 mm)	3.4	°C/W
		UFQFPN48 (7 x 7 mm)	10.2	
		LQFP48 (7 x 7 mm)	14.2	
		LQFP64 (10 x 10 mm)	12	
		LQFP100 (14 x 14 mm)	9.3	
		UFBGA100 (7 x 7 mm)	15	
		LQFP144 (20 x 20 mm)	9.4	
		UFBGA144 (10 x 10 mm)	14.6	

6.10.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.
- For information on thermal management, refer to “*Thermal management guidelines for STM32 32-bit Arm Cortex MCUs applications*” (AN5036) available from *www.st.com*.

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7 Ordering information

Example: STM32 H 533 V E T 6 TR

Device family

STM32 = Arm based 32-bit microcontroller

Product type

H = high performance

Device subfamily

533 = STM32H533xx devices

Pin count

C = 48 pins
R = 64 pins
H = 39 balls
V = 100 pins/balls
Z = 144 pins/balls

Flash memory size

E = 512 Kbytes

Package

U = UFQFPN
T = LQFP
I = UFBGA (7 x 7 mm)
K= UFBGA (10 x 10)
Y = WLCSP

Temperature range

6 = Temperature range, -40 to 85 °C

7 = Temperature range, -40 to 105 °C, and up to 125 °C at low dissipation (130 °C juntion)

Packing

TR = tape and reel

xxx = programmed parts

For a list of available options (such as speed or package) or for further information on any aspect of this device, contact the nearest ST sales office.

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9 Revision history

Table 131. Document revision history

Date	Revision	Changes
02-Apr-2024	1	Initial release.

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