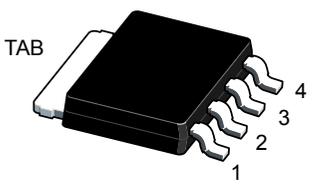
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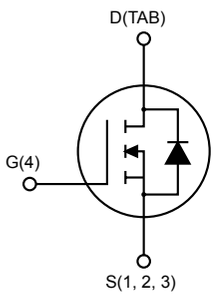
STK184N4F7AG

Datasheet

Automotive-grade N-channel 40 V, 1.6 mΩ typ., 100 A, STripFET™ F7 Power MOSFET in an LFPAK 5x6 package



LFPAK 5x6



G4S123DTAB_LFPAK

STPOWER

Product status link
STK184N4F7AG

Product summary	
Order code	STK184N4F7AG
Marking	184N4F7AG
Package	LFPAK 5x6
Packing	Tape and reel

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STK184N4F7AG	40 V	2.0 mΩ	100 A

- AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	100	A
	Drain current (continuous) at T_C = 100 °C	100	A
I_{DM} (2)	Drain current (pulsed)	400	A
P_{TOT}	Total power dissipation at T_C = 25 °C	136	W
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	42	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AV}, V_{DD} = 25 V)	280	mJ
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. *Drain current is limited by package, the current capability of the silicon is 184 A at 25 °C.*
2. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.1	°C/W

1. *When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s.*

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2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 50 A		1.6	2.0	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS}= 0 V	-	2750	-	pF
C_{oss}	Output capacitance		-	625	-	pF
C_{rss}	Reverse transfer capacitance		-	200	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 100 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	35	-	nC
Q_{gs}	Gate-source charge		-	16	-	nC
Q_{gd}	Gate-drain charge		-	8.9	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 50 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	12	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	33.4	-	ns
t_f	Fall time		-	20.7	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 100 A, V_{GS} = 0 V	-		1.1	V
t_{rr}	Reverse recovery time	I_D = 100 A, di/dt = 100 A/µs V_{DD} = 20 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	25		ns
Q_{rr}	Reverse recovery charge		-	9.5		nC
I_{RRM}	Reverse recovery current		-	0.8		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

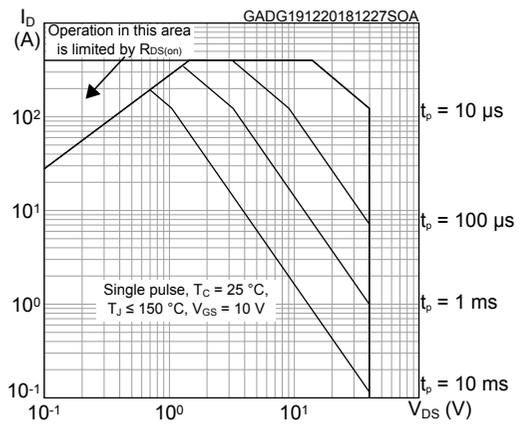


Figure 2. Thermal impedance

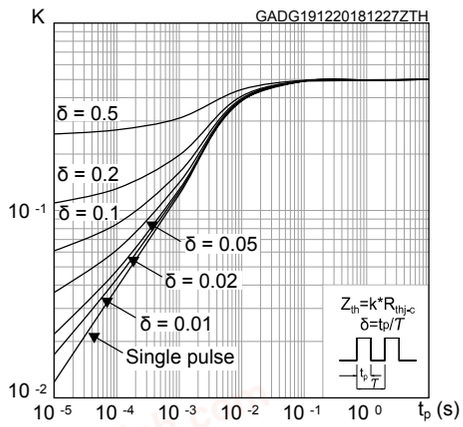


Figure 3. Output characteristics

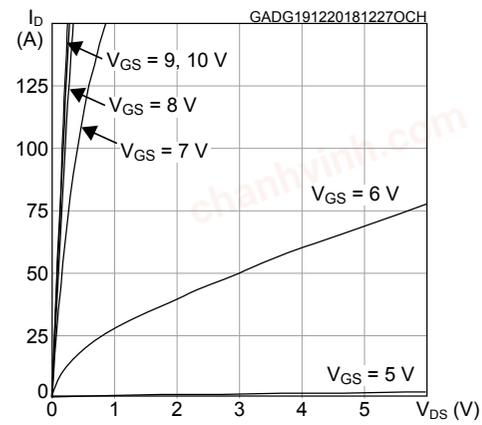


Figure 4. Transfer characteristics

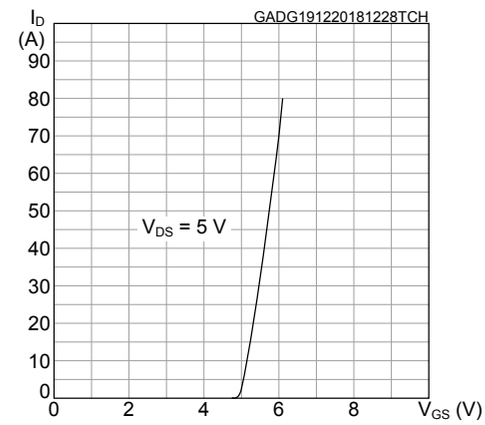


Figure 5. Gate charge vs gate-source voltage

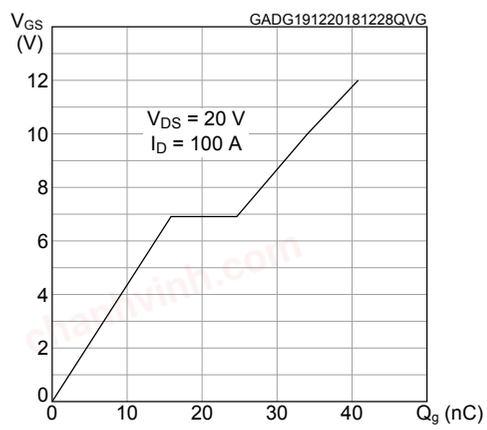
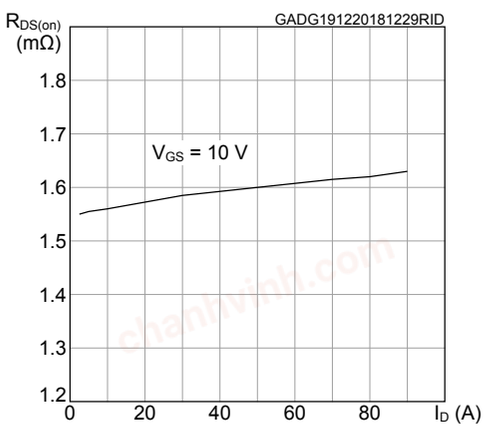


Figure 6. Static drain-source on-resistance



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Figure 7. Capacitance variations

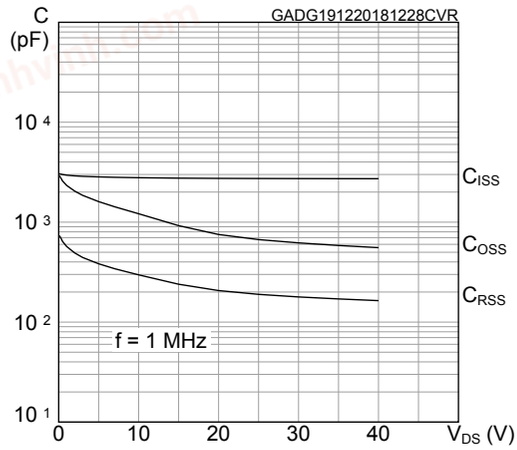


Figure 8. Normalized $V_{(BR)DSS}$ vs temperature

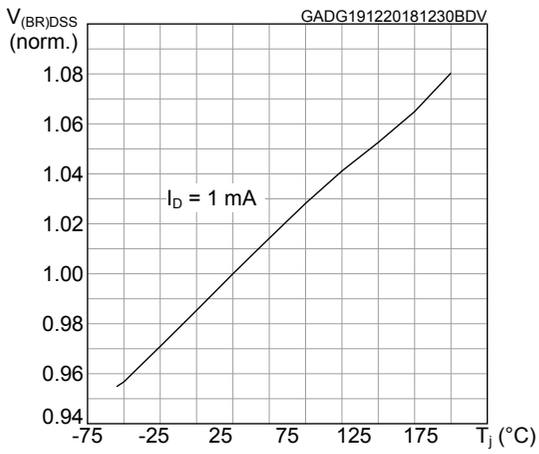


Figure 9. Normalized gate threshold voltage vs temperature

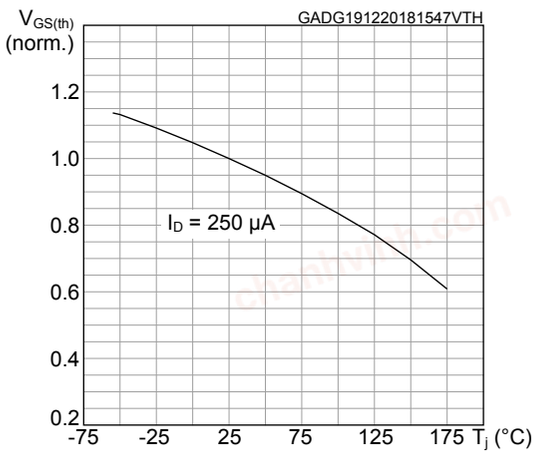


Figure 10. Normalized on-resistance vs temperature

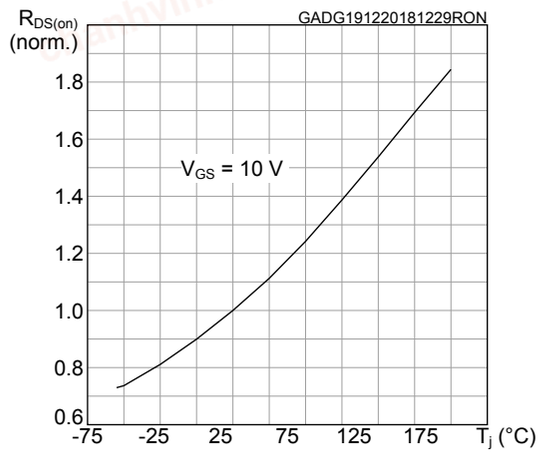
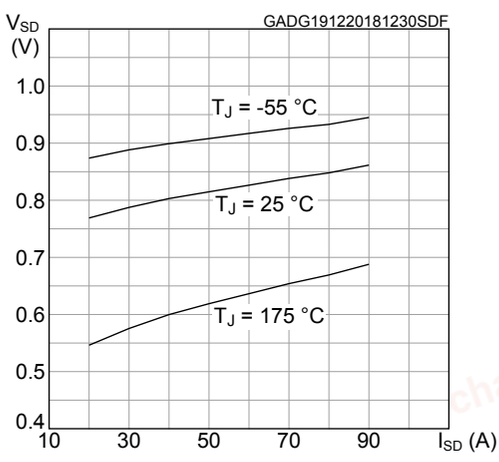


Figure 11. Source-drain diode forward characteristics



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3 Test circuits

Figure 12. Test circuit for resistive load switching times

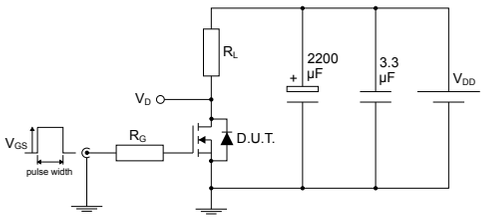


Figure 13. Test circuit for gate charge behavior

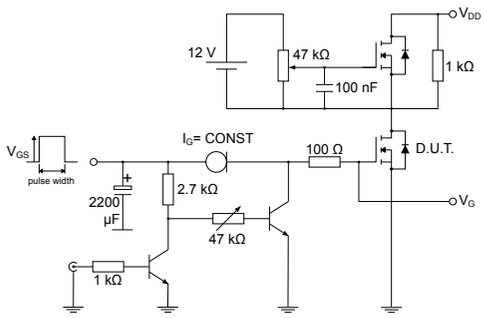


Figure 14. Test circuit for inductive load switching and diode recovery times

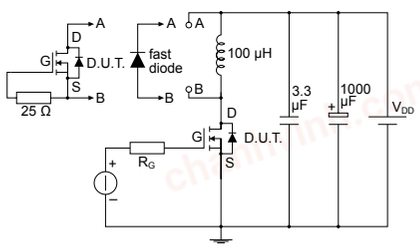


Figure 15. Unclamped inductive load test circuit

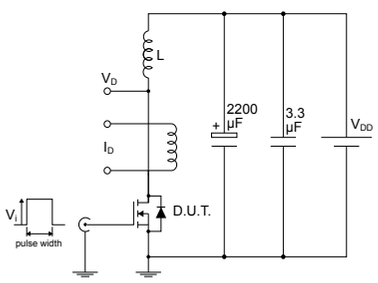


Figure 16. Unclamped inductive waveform

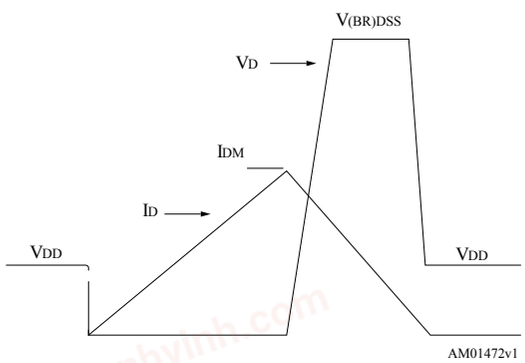
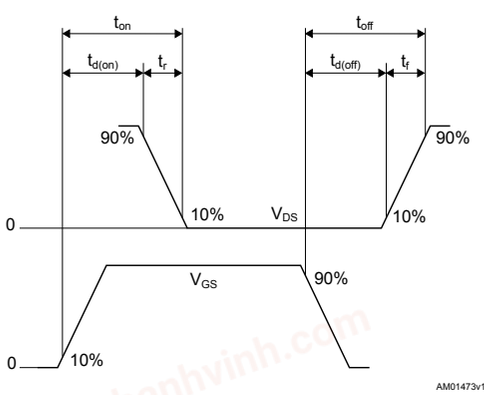


Figure 17. Switching time waveform



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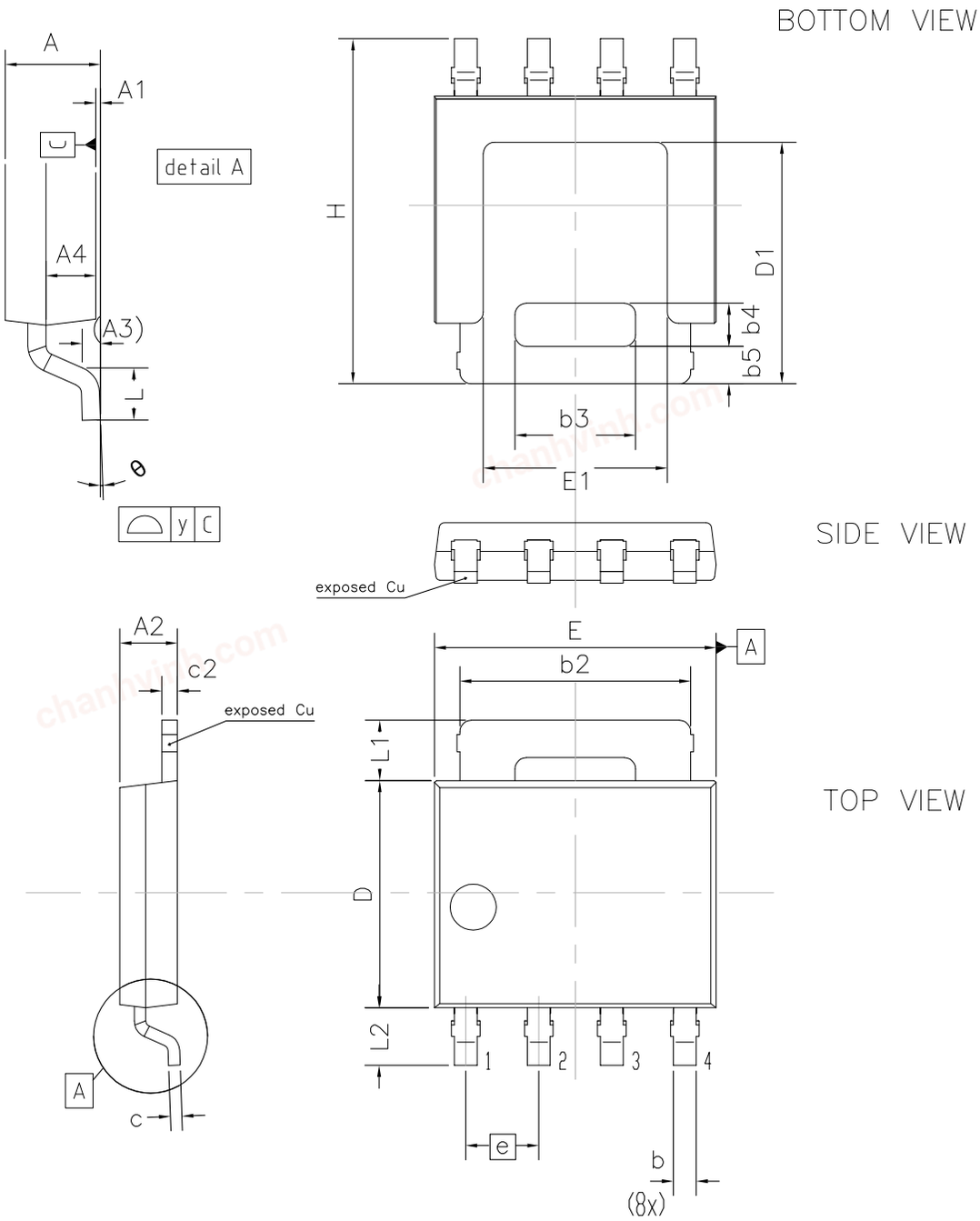
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

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4.1 LFPAK 5x6 package information

Figure 18. **LFPAK 5x6 package outline**



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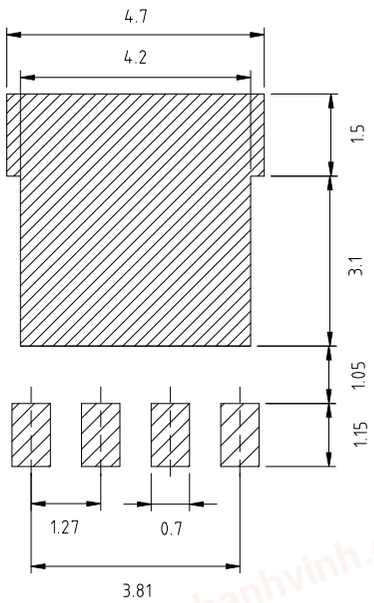
Table 7. **LFPAK 5x6 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	1.01		1.20
A1	0.00		0.15
A2	0.95		1.10
A3		0.25	
A4	0.50	0.55	0.65
b	0.35		0.50
b2	3.62		4.41
b3	2.0		2.20
b4	0.70		0.90
b5			0.7
c	0.19	0.20(1)	0.25
c2	0.24		0.30
D	3.80		4.10
D1	3.80	4.00	4.20
E	4.8		5.0
E1	3.1		3.3
e		1.27	
H	5.8		6.2
L	0.40		0.85
L1	0.80		1.30
L2	0.80		1.3
w		0.25	
y		0.10	
Θ	0°		8°

1. *Dimension without plating*

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Figure 19. **LFPAK 5x6 recommended footprint**



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Revision history

Table 8. **Document revision history**

Date	Revision	Changes
05-Jul-2018	1	First release.
10-Jan-2019	2	Updated title and features on cover page. Updated Section 1 Electrical ratings and Section 2 Electrical characteristics. Added Section 2.1 Electrical characteristics (curves). Minor text changes

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