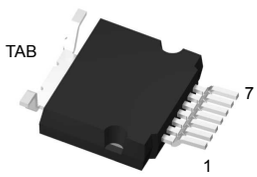
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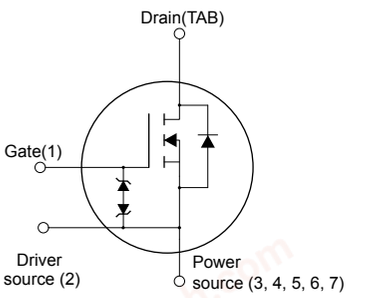
STHU47N60DM6AG

Datasheet

Automotive-grade N-channel 600 V, 70 mΩ typ., 36 A MDmesh DM6 Power MOSFET in an HU3PAK package



HU3PAK



N-chG1DS2PS34567DTABZ

STPOWER

Product status link
STHU47N60DM6AG

Product summary	
Order code	STHU47N60DM6AG
Marking	47N60DM6
Package	HU3PAK
Packing	Tape and reel

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STHU47N60DM6AG	600 V	80 mΩ	36 A

- AEC-Q101 qualified
- Fast-recovery body diode
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q_{rr}), recovery time (t_{rr}) and excellent improvement in $R_{DS(on)}$ per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	36	A
I_D	Drain current (continuous) at T_C = 100 °C	22	A
I_D (1)	Drain current (pulsed)	137	A
P_{TOT}	Total power dissipation at T_C = 25 °C	250	W
dv/dt (2)	Peak diode recovery voltage slope	50	V/ns
di/dt (3)	Peak diode recovery current slope	1000	A/µs
dv/dt (3)	MOSFET dv/dt ruggedness	100	V/ns
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		°C

1. *Pulse width limited by safe operating area*
2. *I_{SD} ≤ 36 A, $V_{DS}(peak) < V_{(BR)DSS}$, V_{DD} = 400 V*
3. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.5	°C/W
R_{thJB} (1)	Thermal resistance, junction-to-board	30	

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	7	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 100 V)	700	mJ

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2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			200	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4.00	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 18 A		70	80	mΩ

1. *Specified By Design – Not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	2350	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	416	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 36 A, V_{GS}= 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	55	-	nC
Q_{gs}	Gate-source charge		-	12	-	nC
Q_{gd}	Gate-drain charge		-	31	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 300 V, I_D = 18 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Switching times test circuit for resistive load and Figure 19. Switching time waveform)	-	23	-	ns
t_r	Rise time		-	5.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	57	-	ns
t_f	Fall time		-	9	-	ns

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Table 7. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		36	A
I_{SDM} (1)	Source-drain current (pulsed)		-		137	A
V_{SD} (2)	Forward on voltage	I_{SD} = 36 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 36 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	115		ns
Q_{rr}	Reverse recovery charge		-	0.54		µC
I_{RRM}	Reverse recovery current		-	9.5		A
t_{rr}	Reverse recovery time	I_{SD} = 36 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	210		ns
Q_{rr}	Reverse recovery charge		-	2.1		µC
I_{RRM}	Reverse recovery current		-	20.4		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

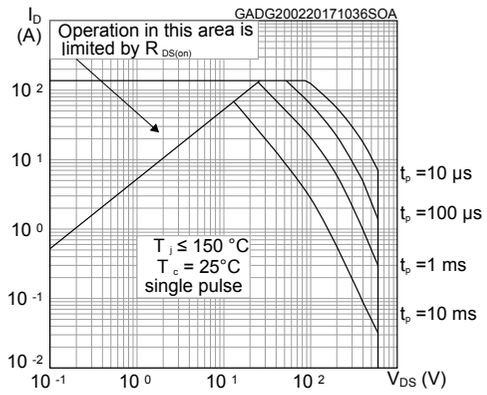


Figure 2. Thermal impedance

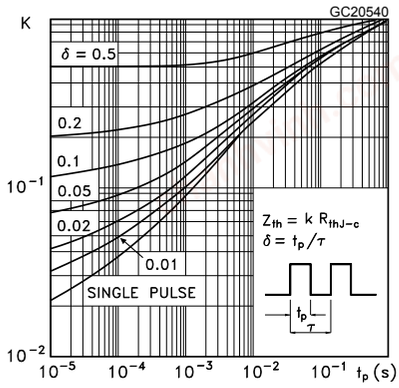


Figure 3. Output characteristics

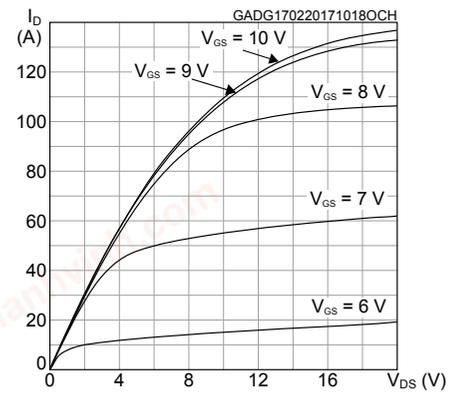


Figure 4. Transfer characteristics

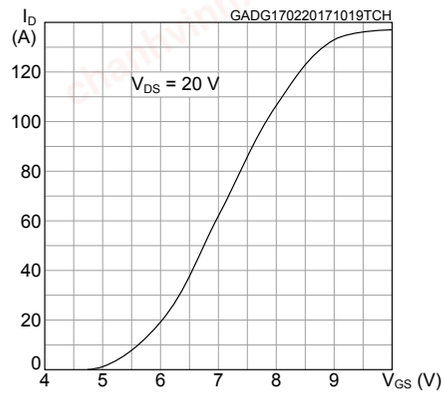


Figure 5. Gate charge vs gate-source voltage

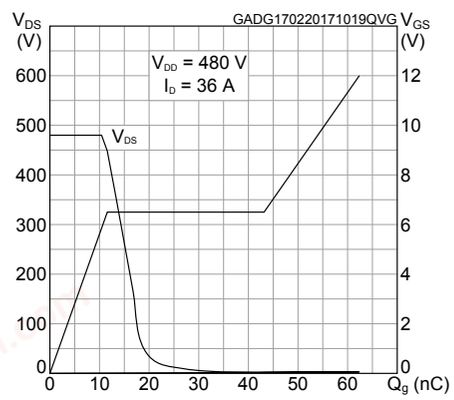
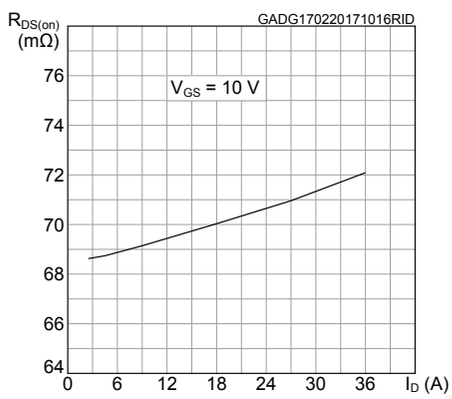


Figure 6. Static drain-source on-resistance



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Figure 7. Capacitance variations

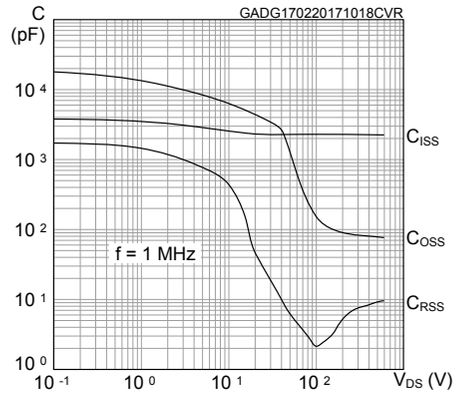


Figure 8. Normalized gate threshold voltage vs temperature

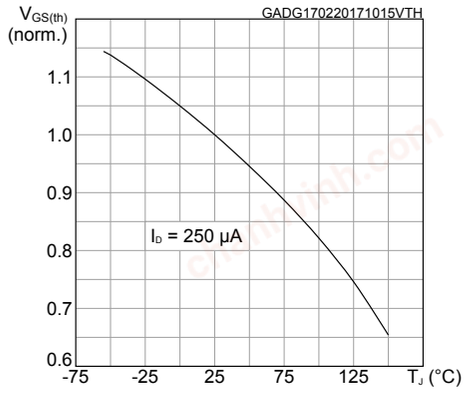


Figure 9. Normalized on-resistance vs temperature

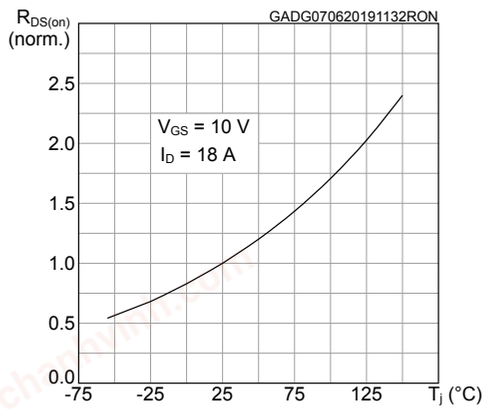


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

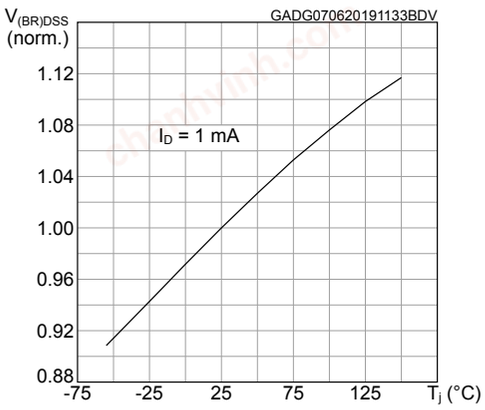


Figure 11. Source-drain diode forward characteristics

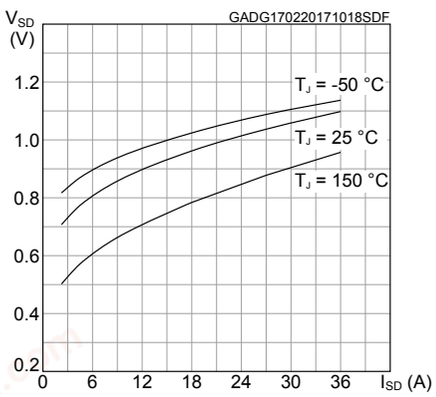
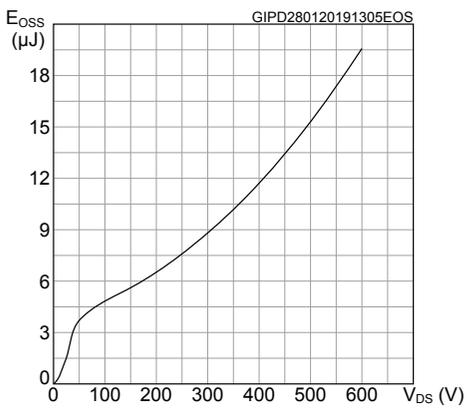


Figure 12. Output capacitance stored energy



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3 Test circuits

Figure 13. Switching times test circuit for resistive load

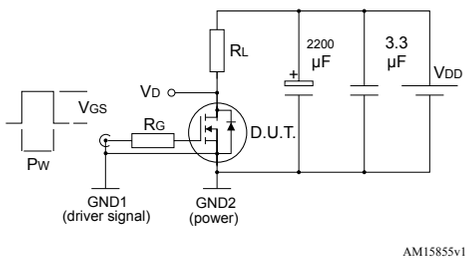


Figure 14. Test circuit for gate charge behavior

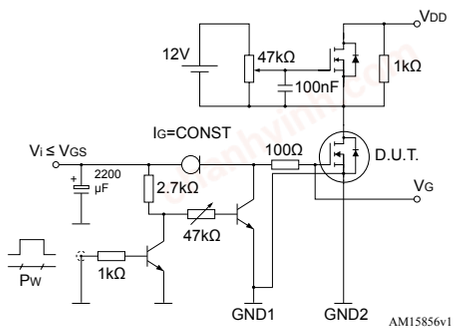


Figure 15. Test circuit for inductive load switching and diode recovery times

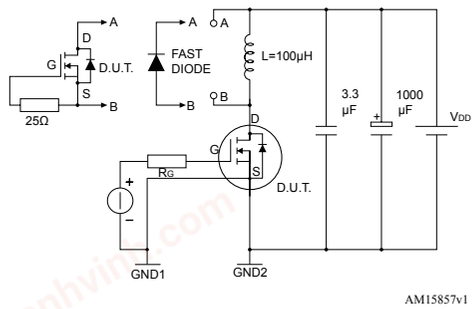


Figure 16. Unclamped inductive load test circuit

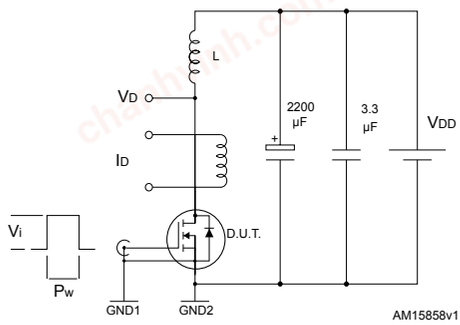


Figure 17. Unclamped inductive waveform

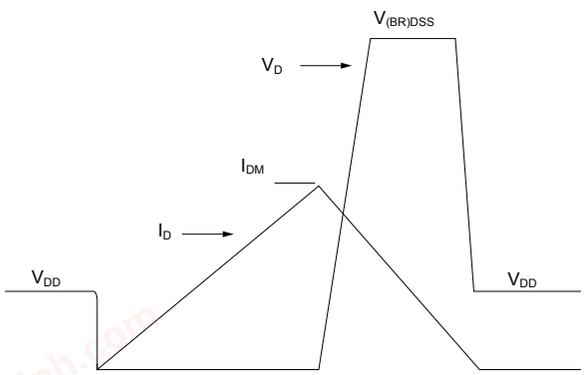
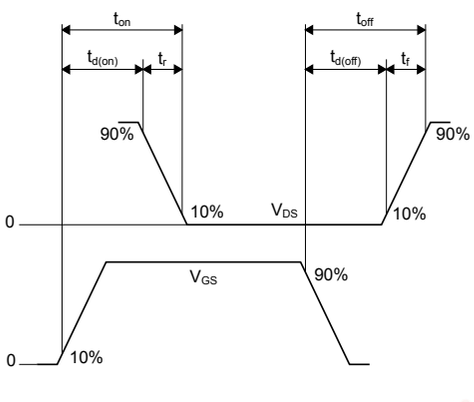


Figure 18. Switching time waveform



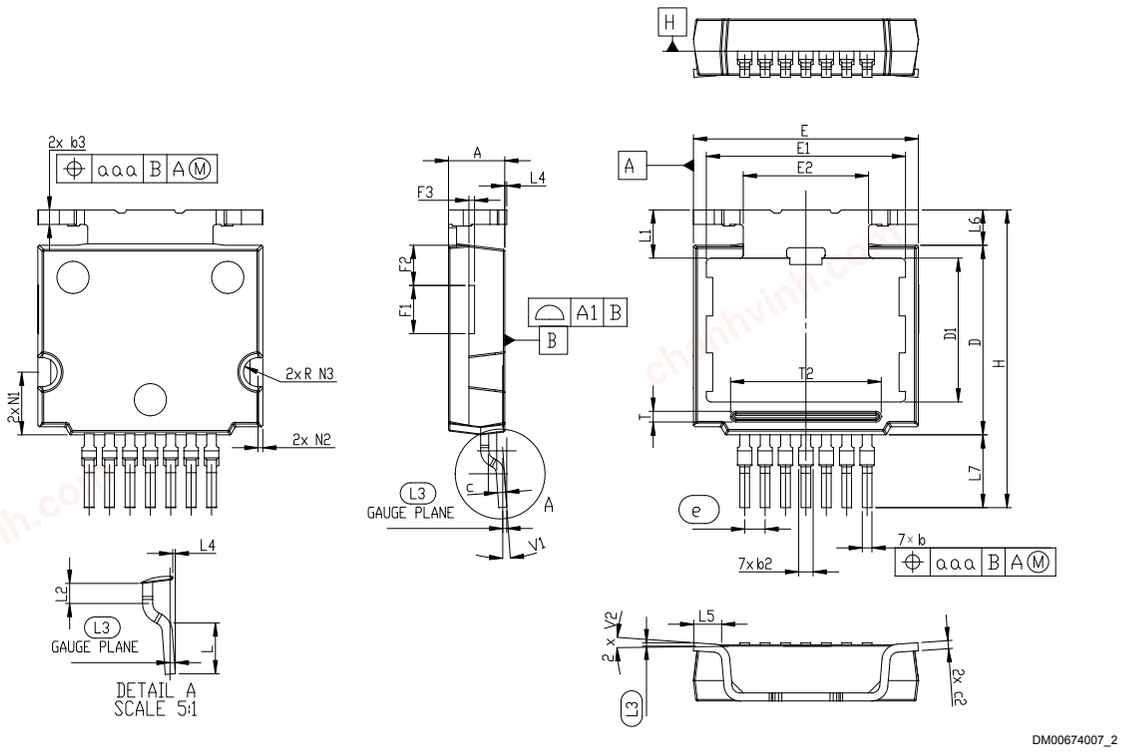
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 HU3PAK package information

Figure 19. HU3PAK package outline



DM00674007_2

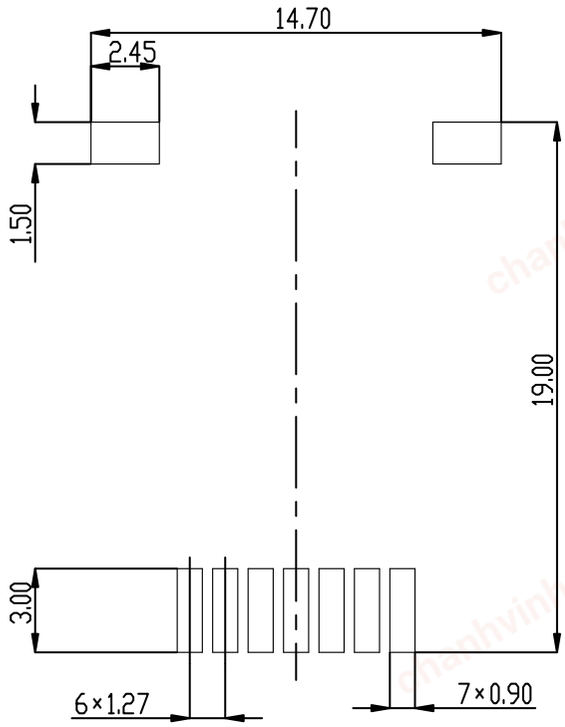
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Table 8. **HU3PAK package mechanical data**

Ref.	Dimensions		
	mm		
	Min.	Typ.	Max.
A	3.40	3.50	3.60
A1		0.05	
b	0.50	0.60	0.70
b2	0.50	0.70	1.00
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.70	11.80	11.90
D1	8.80	8.955	9.10
E	13.90	14.00	14.10
E1	12.30	12.40	12.50
E2	7.75	7.80	7.85
e		1.27	
H	18.00	18.58	19.00
aaa		0.10	
L	2.40	2.52	2.60
L1		3.05	
L2	0.90	1.00	1.10
L3		0.26	
L4	0.075	0.125	0.175
L5	1.83	1.93	2.03
L6	2.14	2.24	2.34
L7	4.44	4.54	4.64
F1	2.90	3.00	3.10
F2	2.40	2.50	2.60
F3	0.25	0.35	0.45
N1	3.80	3.90	4.00
N2	0.25	0.30	0.45
N3	0.80	0.90	1.00
T	0.50	0.67	0.70
T2	9.18	9.38	9.43

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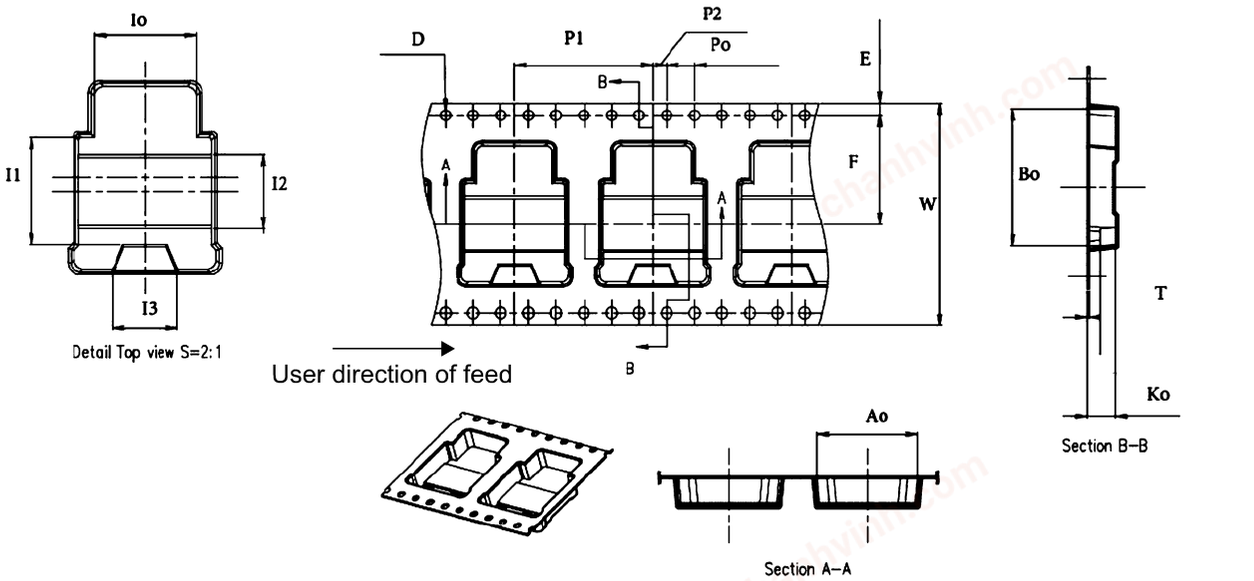
Figure 20. **HU3PAK recommended footprint (dimensions are in mm)**



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4.2 HU3PAK packing information

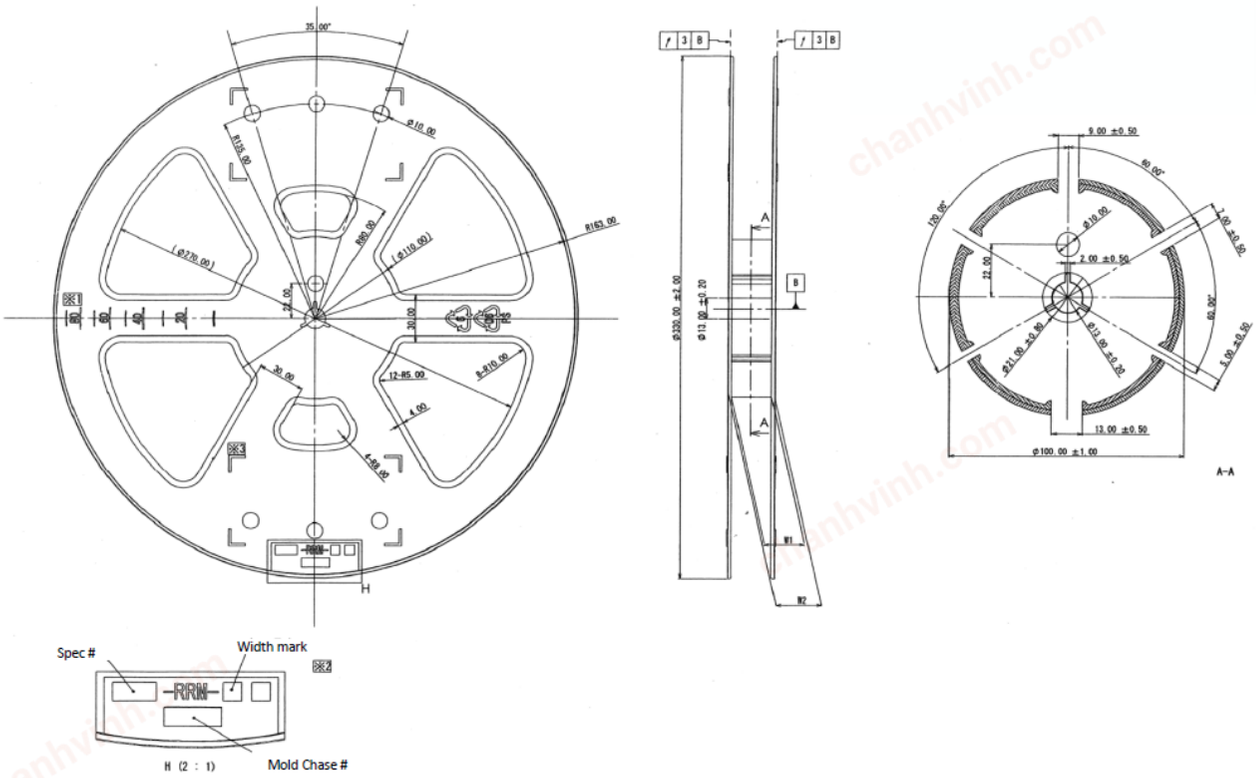
Figure 21. **HU3PAK carrier tape outline**



DM00345054_3

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Figure 22. **HU3PAK reel outline**



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Table 9. **HU3PAK tape mechanical data**

Dimension	Value
	mm
A0	14.40 ±0.10
B0	19.70
D	1.50 ±0.10
E	1.75 ±0.10
F	15.65 ±0.10
I0	11.00
I1	11.60 ±0.10
I2	8.00
I3	7.00
K0	4.20
P0	4.00 ±0.10
P1	20.00 ±0.10
P2	2.00 ±0.10
T	0.40 ±0.50
W	32.00 ±0.30

Table 10. **HU3PAK reel mechanical data**

Dimension	Value
	mm
Reel width	32.0
Reel inner width	33.4 ±1.0
Reel outer width	37.4 ±1.0

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Revision history

Table 11. **Document revision history**

Date	Revision	Changes
07-Jun-2019	1	Initial release.
06-Oct-2021	2	Modified Features on cover page. Modified Table 1. Absolute maximum ratings and Table 4. On/off-state. Modified Section 4 Package information. Minor text changes.

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