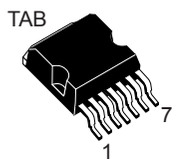
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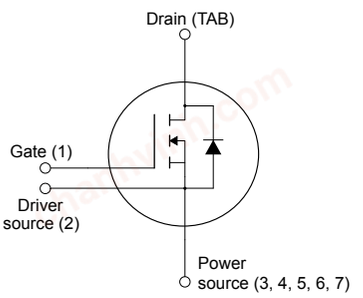
STH65N050DM9-7AG

Datasheet

Automotive-grade N-channel 650 V, 38 mΩ typ., 51 A MDmesh DM9 Power MOSFET in an H²PAK-7 package



H²PAK-7



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH65N050DM9-7AG	650 V	50 mΩ	51 A

- AEC-Q101 qualified
- Fast-recovery body diode
- Very low FOM ($R_{DS(on)} \cdot Q_g$)
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggednes
- Excellent switching performance thanks to the extra driving source pin

Applications

- DC/DC converter for EV/HEV
- On board charger (OBC)

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh DM9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area coupled with a fast-recovery diode. The silicon-based DM9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The fast-recovery diode featuring very low recovery charge (Q_{rr}), time (t_{rr}) and $R_{DS(on)}$ makes this fast-switching super-junction Power MOSFET tailored for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Product status link
STH65N050DM9-7AG

Product summary	
Order code	STH65N050DM9-7AG
Marking	65A050DM9
Package	H²PAK-7
Packing	Tape and reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D[1]	Drain current (continuous) at T_C = 25 °C	51	A
	Drain current (continuous) at T_C = 100 °C	32	
I_{DM}[2]	Drain current (pulsed)	220	A
P_{TOT}	Total power dissipation at T_C = 25 °C	266	W
dv/dt[3]	Peak diode recovery voltage slope	120	V/ns
di/dt[3]	Peak diode recovery current slope	1000	A/µs
dv/dt[4]	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Referred to TO-247 long leads package.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 25.5 A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} (peak) < $V_{(BR)\ DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.47	°C/W
R_{thJA}[1]	Thermal resistance, junction-to-ambient	30	°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	760	mJ

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2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			5	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.5	4.0	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 25.5 A		38	50	mΩ

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 250 kHz, V_{GS} = 0 V	-	4680	-	pF
C_{oss}	Output capacitance		-	76	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	1070	-	pF
R_g	Intrinsic gate resistance	f = 250 kHz, open drain	-	1	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 25.5 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	100	-	nC
Q_{gs}	Gate-source charge		-	26	-	nC
Q_{gd}	Gate-drain charge		-	36	-	nC

1. *$C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 25.5 A, R_G = 4.7 Ω , V_{GS} = 10 V (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	29	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time		-	80	-	ns
t_f	Fall time		-	5	-	ns

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Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		51	A
I_{SDM} (2)	Source-drain current (pulsed)		-		220	A
V_{SD} (3)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 51 A	-	1.1	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 51 A, di/dt = 100 A/µs,	-	170		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 150 V	-	1.2		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12		A
t_{rr}	Reverse recovery time	I_{SD} = 51 A, di/dt = 100 A/µs,	-	225		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 150 V, T_J = 150 °C	-	2.2		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	18		A

1. *Referred to TO-247 long leads package.*
2. *Pulse width is limited by safe operating area.*
3. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

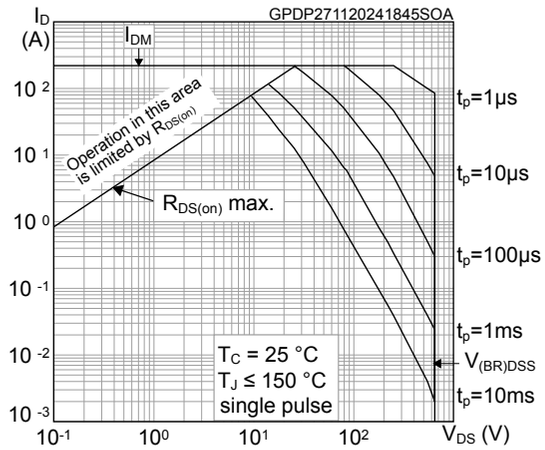


Figure 2. Maximum transient thermal impedance

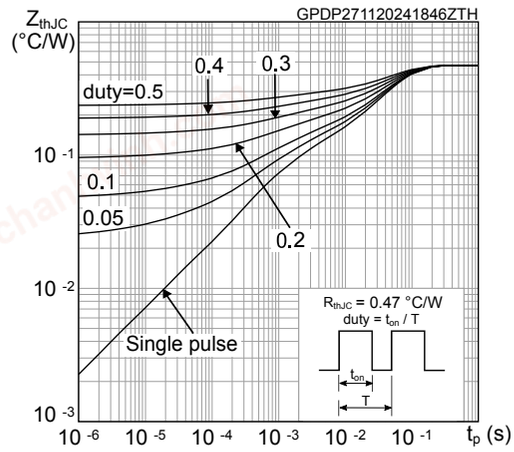


Figure 3. Typical output characteristics

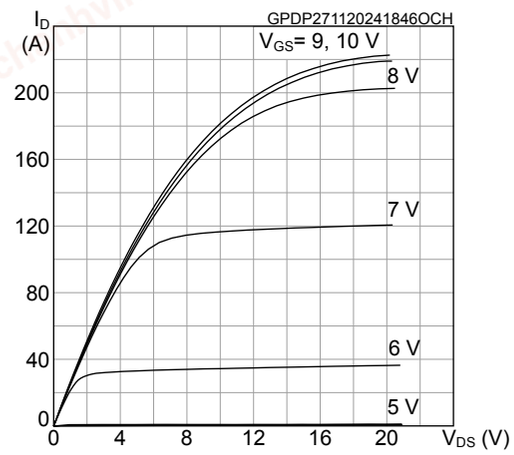


Figure 4. Typical transfer characteristics

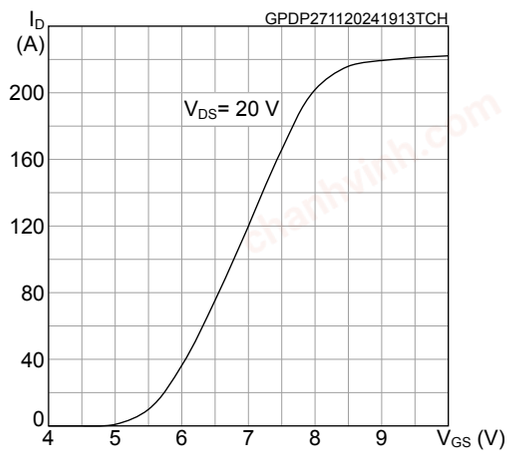


Figure 5. Typical gate charge characteristics

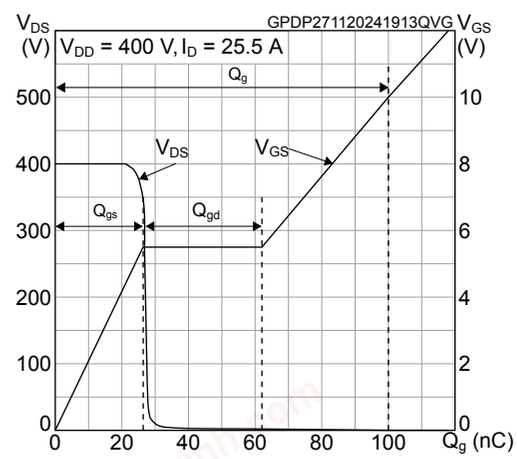
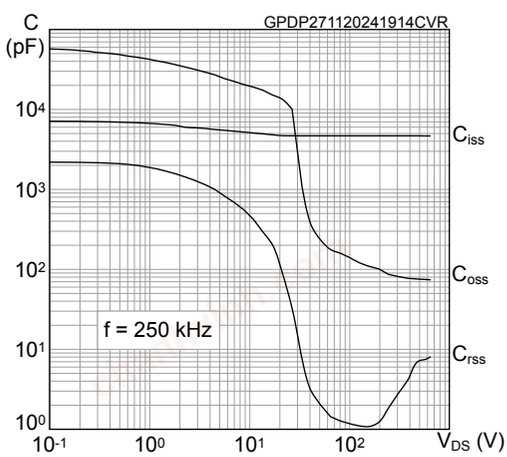


Figure 6. Typical capacitance characteristics



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Figure 7. Typical drain-source on-resistance

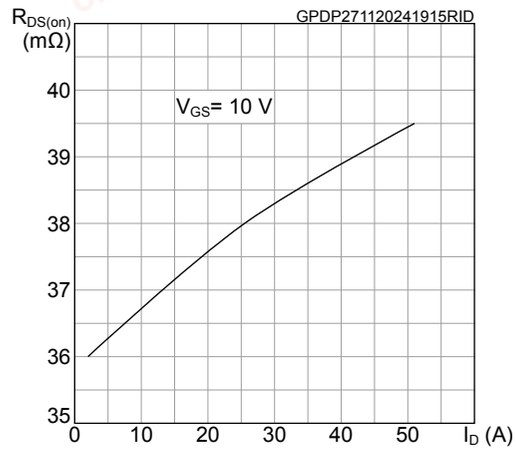


Figure 8. Normalized on-resistance vs temperature

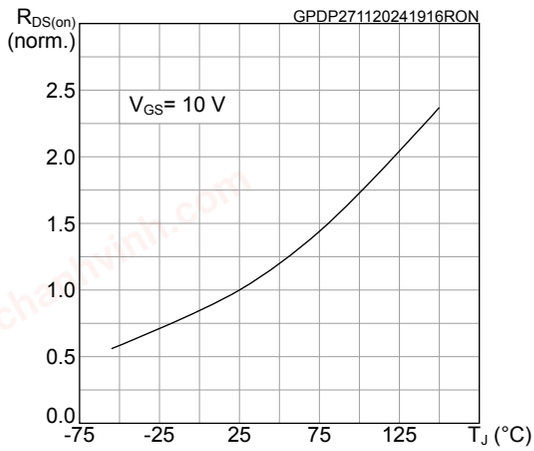


Figure 9. Normalized gate threshold vs temperature

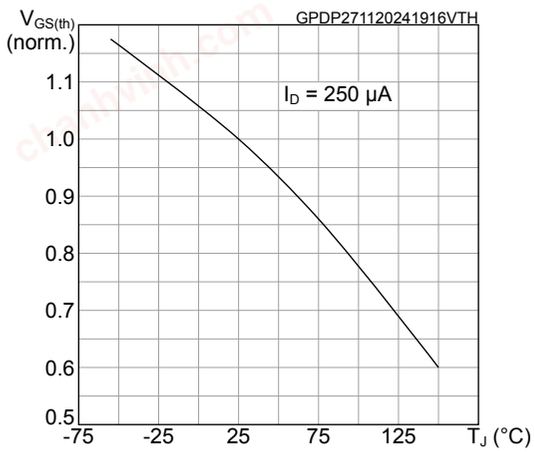


Figure 10. Normalized breakdown voltage vs temperature

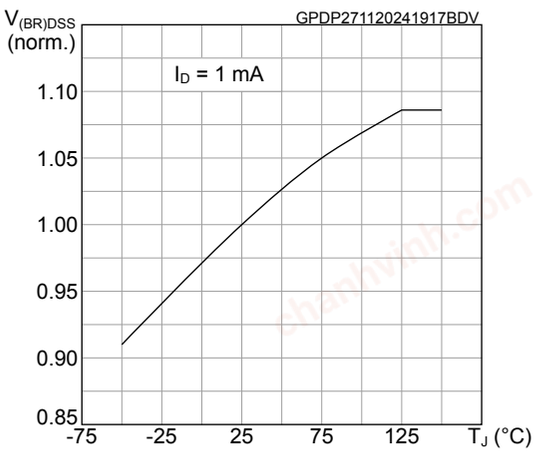


Figure 11. Typical reverse diode forward characteristics

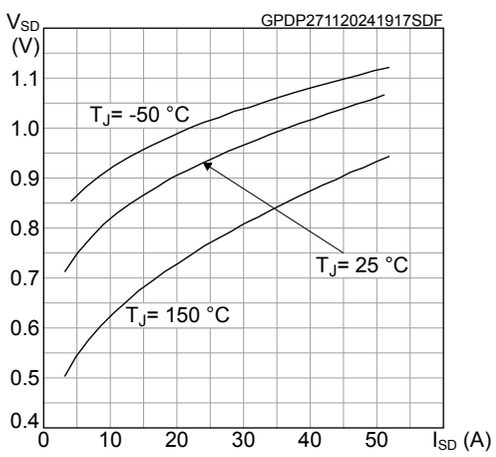
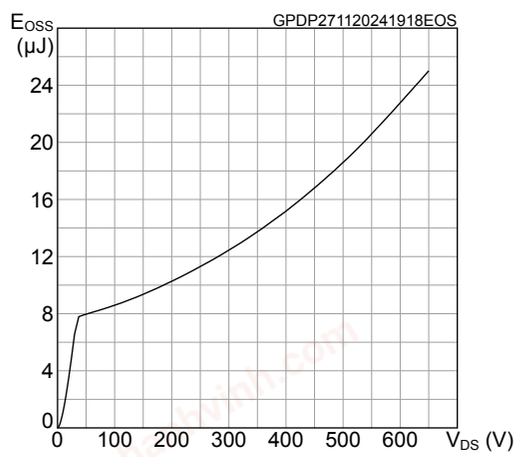


Figure 12. Typical output capacitance stored energy



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3 Test circuits

Figure 13. Switching times test circuit for resistive load

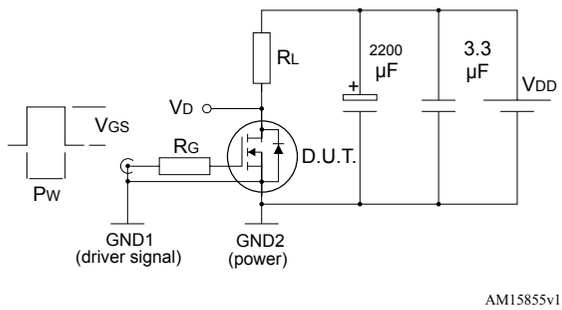


Figure 14. Test circuit for gate charge behavior

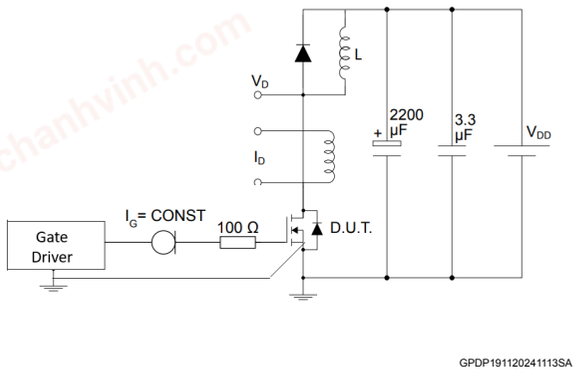


Figure 15. Test circuit for inductive load switching and diode recovery times

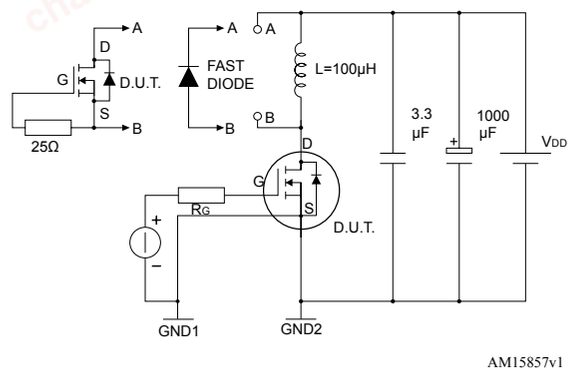


Figure 16. Unclamped inductive load test circuit

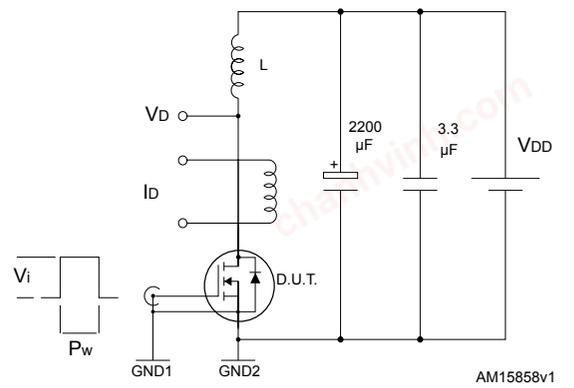


Figure 17. Unclamped inductive waveform

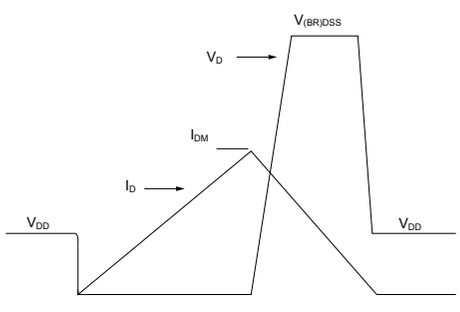
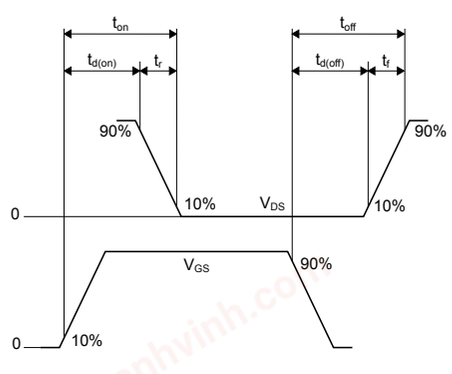


Figure 18. Switching time waveform



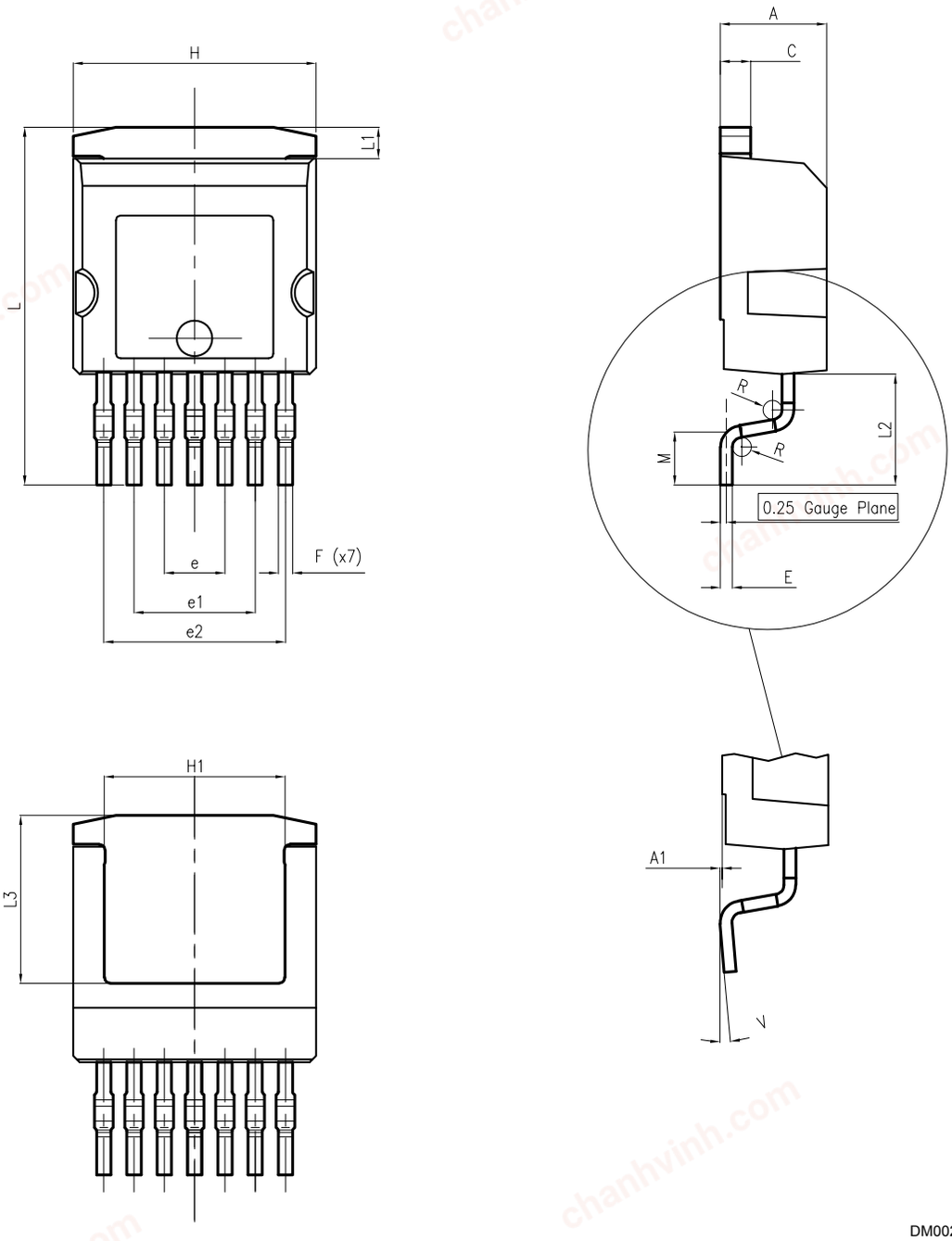
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-7 package information

Figure 19. **H²PAK-7 package outline**



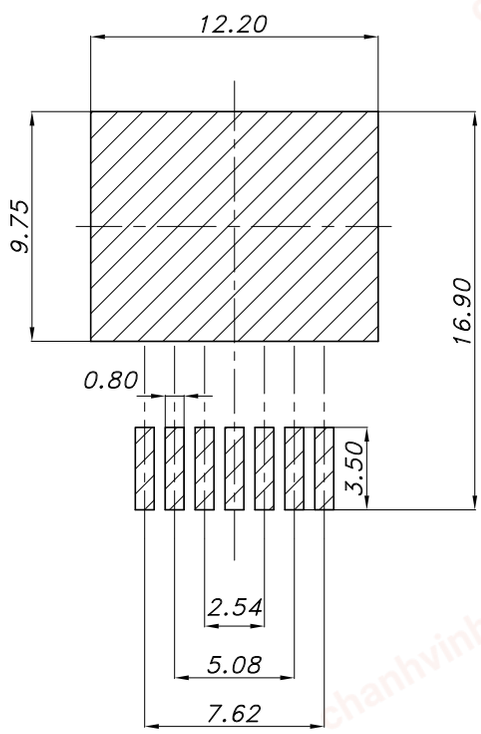
DM00249216_6

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Table 8. **H²PAK-7 package mechanical data**

Dim.	mm	
	Min.	Max.
A	4.30	4.80
A1	0.03	0.20
C	1.17	1.37
e	2.34	2.74
e1	4.88	5.28
e2	7.42	7.82
E	0.45	0.60
F	0.50	0.70
H	10.00	10.40
H1	7.40	8.00
L	14.75	15.25
L1	1.27	1.40
L2	4.35	4.95
L3	6.85	7.25
M	1.90	2.50
R	0.20	0.60
V	0°	8°

Figure 20. **H²PAK-7 recommended footprint**



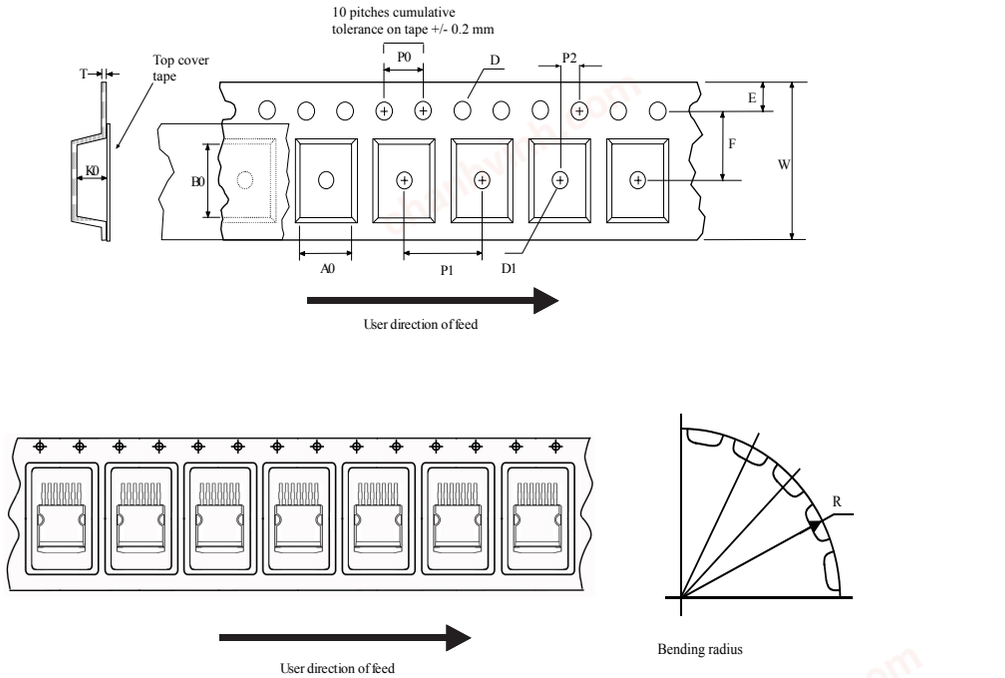
footprint_DM00249216_6

Note: Dimensions are in mm.

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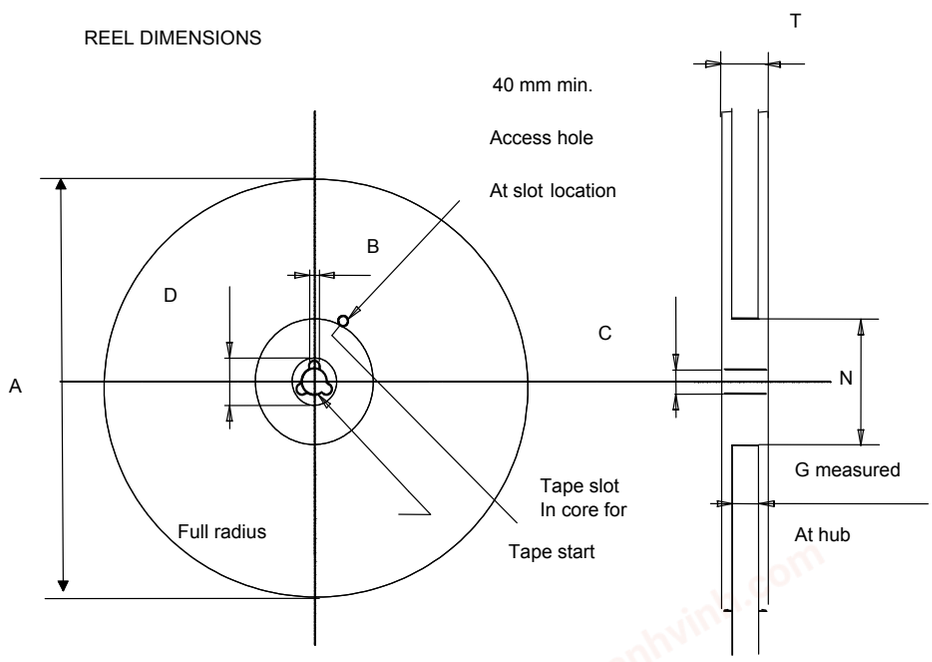
4.2 Packing information

Figure 21. **Tape outline**



GADG160620211017SA

Figure 22. **Reel outline**



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Table 9. **Tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

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Revision history

Table 10. **Document revision history**

Date	Revision	Changes
05-Jun-2024	1	First release.
01-Oct-2024	2	Modified $R_{DS(on)}$ value in *Table 3. On/off-states*.
28-Nov-2024	3	Updated *Features* on cover page. Added *Table 3. Avalanche characteristics*. Updated *Table 5. Dynamic characteristics*, *Table 6. Switching times* and *Table 7. Source-drain diode*. Updated *Section 2.1: Electrical characteristics (curves)*. Updated *Section 3: Test circuits*. Minor text changes.
28-Jan-2025	4	Updated Applications. Updated Figure 10. Normalized breakdown voltage vs temperature.

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Contents

1 **Electrical ratings** 2
2 **Electrical characteristics** 3
2.1 Electrical characteristics (curves) 5
3 **Test circuits** 7
4 **Package information** 8
4.1 H²PAK-7 package information 8
4.2 Packing information 10
Revision history 12

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