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STGAP4S

Datasheet

Automotive advanced isolated gate driver for IGBTs and SiC MOSFETs



SO-36W

Product status link
STGAP4S

Product label
SUSTAINABLE TECHNOLOGY

Features

- AEC-Q100 qualified
- High voltage rail up to 1200 V
- Two output pins for direct driving of external MOSFET buffer
- Driver current capability:
  - OUT1: 0.6/2.5 A sink/source
  - OUT2: 2.4/0.6 A sink/source
- Negative gate drive ability
- dV/dt transient immunity ±100 V/ns in full temperature range
- Integrated controller for isolated flyback power supply
- Active Miller clamp driver for external N-channel MOSFET
- Programmable Desaturation detection
- Programmable Overcurrent detection
- Soft turn-off
- V_{CE} active clamp
- Two diagnostic status outputs
- Programmable UVLO and OVLO on each supply
- Programmable input deglitch filter
- Asynchronous stop command
- Isolated 8-bit A/D converter
- Integrated temperature sensor
- Programmable deadtime, with violation error
- SPI interface for parameters programming and extended diagnostic
- Temperature warning and shutdown protection
- Self-diagnostic routines for protection features

Applications

- Inverters for EV/HEV
- 600/1200 V industrial inverters
- EV charging stations
- UPS equipment
- AC/AC converters
- DC/DC converters
- Solar inverters

Description

The STGAP4S is a galvanically isolated single gate driver for IGBTs and SiC MOSFETs with advanced protection, configuration and diagnostic features. The architecture of the STGAP4S isolates the channel gate driving from the control and the low voltage interface circuitry through true galvanic isolation.

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The unique output architecture is designed to allow the use of an external MOSFET push-pull stage giving flexibility in terms of current capability dimensioning and easing the use of several power switches in parallel. The 2 pre-driver outputs are characterized by current capability and output voltage swing optimized for that topology and allow the use of a negative gate driving supply.

The integrated controller for isolated flyback power supply allows to generate positive and negative gate driver supply voltages with few external components, enabling PCB space saving.

Protection functions such as the Miller clamp driver, desaturation and overcurrent detection, UVLO and OVLO are included to easily design high reliability systems.

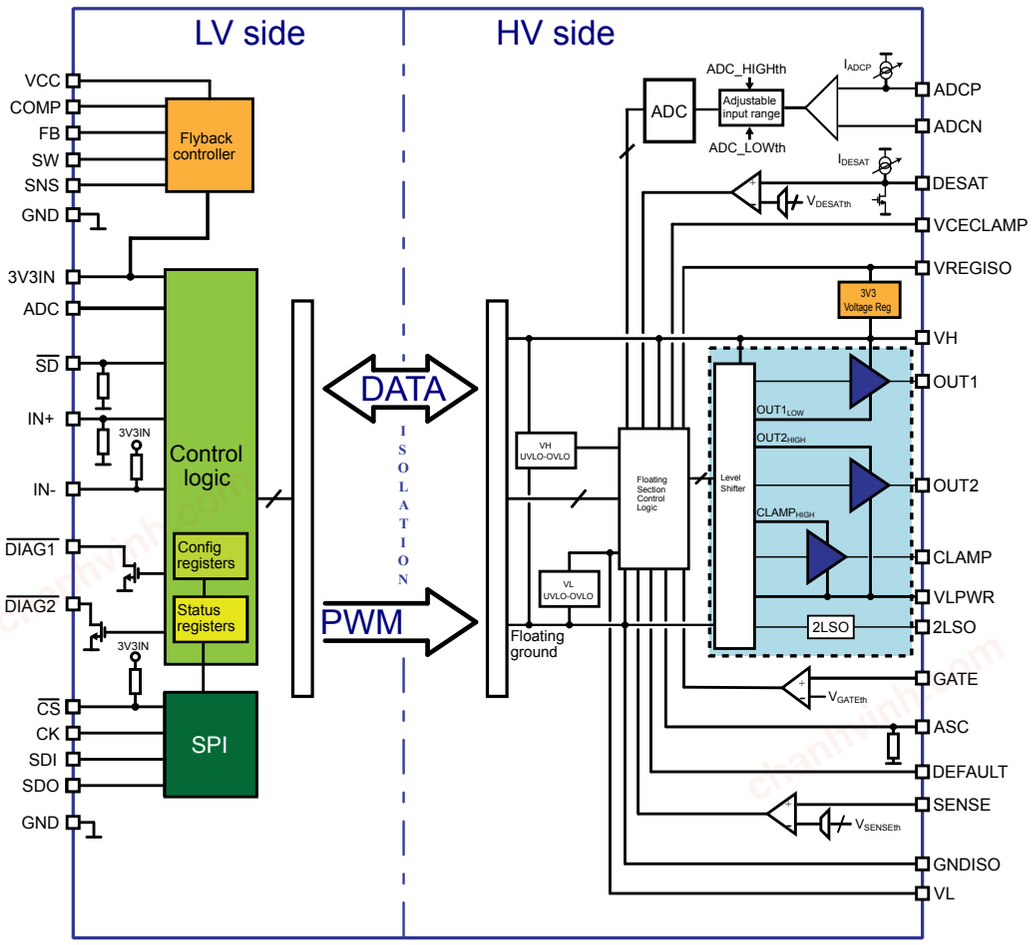
A temperature sensor is integrated in the driver.

Open drain diagnostic outputs are present and detailed device conditions can be monitored through the SPI. Each function’s parameter can be programmed via the SPI, making the device very flexible and allowing it to fit in a wide range of applications.

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1 Block diagram

Figure 1. **Block Diagram**



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2 Pin description and connection diagram

Figure 2. **Pin connection (top view)**

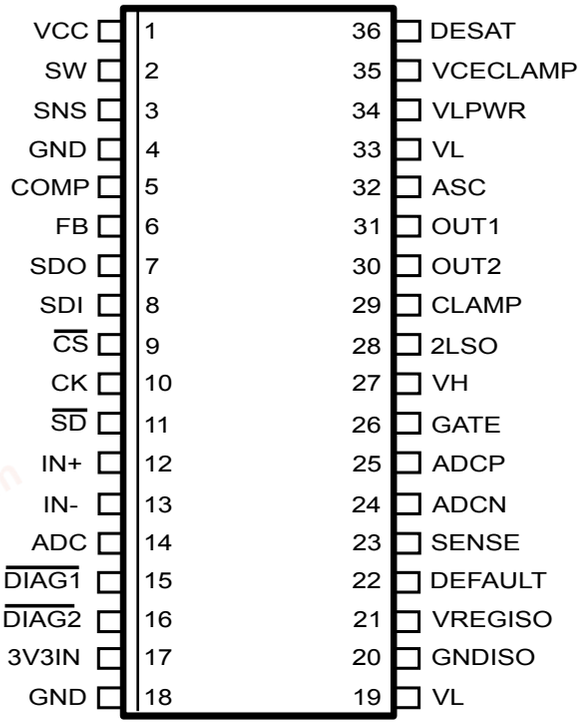


Table 1. **Pin description**

Pin #	Pin Name	Type	Function
1	VCC	Power supply	Flyback controller, power supply for external MOSFET driving
2	SW	Analog output	Flyback controller, switching pin for MOSFET gate driving
3	SNS	Analog input	Flyback controller, external shunt resistor sensing
4, 18	GND	Ground	Low voltage side ground
5	COMP	Analog input	Flyback controller, compensation
6	FB	Analog input	Flyback controller, feedback
7	SDO	Logic output	SPI serial data output
8	SDI	Logic input	SPI serial data input
9	$\overline{CS}$	Logic input	SPI chip select (active low)
10	CK	Logic input	SPI clock
11	$\overline{SD}$	Logic input	Shutdown input (active low)
12	IN+	Logic input	Gate command input
13	IN-	Logic input	Gate command input
14	ADC	Logic output	Pulse width modulated output for ADC conversion result
15	$\overline{DIAG1}$	Open drain output	Open drain diagnostic output 1 (active low)
16	$\overline{DIAG2}$	Open drain output	Open drain diagnostic output 2 (active low)
17	3V3IN	Power supply	Low voltage side power supply
19, 33	VL	Power supply	High voltage side negative supply or ground

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Pin #	Pin Name	Type	Function
20	GNDISO	Ground	High voltage side ground
21	VREGISO	Power supply	High voltage side internal regulator output pin for decoupling capacitor
22	DEFAULT	Logic input	Configuration pin for the operation flow chart
23	SENSE	Analog input	Sense input for overcurrent protection
24	ADCN	Analog input	Analog measurement reference, must be connected to GNDISO
25	ADCP	Analog input	Analog measurement input
26	GATE	Analog input	Gate voltage feedback
27	VH	Power supply	High voltage side positive power supply
28	2LSO	Analog output	Soft turn-off output
29	CLAMP	Analog output	Miller clamp controller output
30	OUT2	Analog output	Pre-driver output 2, for external push-pull N-channel MOSFET
31	OUT1	Analog output	Pre-driver output 1, for external push-pull P-channel MOSFET
32	ASC	Digital input	Asynchronous stop command
34	VLPWR	Power supply	High voltage side negative power supply or ground for external push-pull driving, must be shorted to VL
35	VCECLAMP	Analog input	VCE active clamping protection input
36	DESAT	Analog input	Desaturation protection input

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3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
VCC	Low voltage side power supply voltage vs. GND	-	-0.30	28	V
FB	Feedback pin voltage	I_{FB} within AMR limits	Self limited	Self limited	V
I_{FB}	Feedback pin source/ sink current	-	-2	2	mA
COMP	OTA output voltage	-	-0.30	3.60	V
SNS	Current sensing pin voltage	-	-0.30	1	V
SW	Gate driver output of flyback controller	-	-0.30	(VCC + 0.3, 12) min.	V
3V3IN	Low voltage side power supply voltage vs. GND	-	-0.30	3.60	V
VREGISO	High voltage side internal regulator voltage vs. GNDISO	-	-0.30	3.60	V
V_{LOGIC_INPUT}	Input logic pins voltage vs. GND	-	-0.30	6	V
V_{LOGIC_OUTPUT}	Output logic pins voltage vs. GND	-	-0.30	3.60	V
V_{HL}	Differential supply voltage (VH vs. VL)	-	-0.30	36	V
VH	Positive power supply voltage (VH vs. GNDISO)	-	-0.30	36	V
VL	Negative supply voltage (VL vs. GNDISO)	-	-15	0.30	V
VLPWR	Negative power supply voltage (VLPWR vs. GNDISO)	-	-15	0.30	V
V_{PS} (1)	Differential voltage between VLPWR and VL pin	-	-0.30	+0.30	V
V_{OUT1}	Voltage on OUT1 pre-driver output (OUT1 vs. VH)	-	(-20, VLPWR - 0.3) max.	+0.30	V
$I_{OUT1sink}$	OUT1 pre-driver output sink current	-	-	Self limited (2)	mA
$I_{OUT1source}$	OUT1 pre-driver output source current	OUT1 = LOW	-	10	mA
V_{OUT2}	Voltage on OUT2 pre-driver output (OUT2 vs. VLPWR)	-	-0.30	(+ 20, VH + 0.3) min	V

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Symbol	Parameter	Test condition	Min.	Max.	Unit
$I_{OUT2sink}$	OUT2 pre-driver output sink current	OUT2 = HIGH	-	10	mA
$I_{OUT2source}$	OUT2 pre-driver output source current	-	-	Self limited(2)	mA
V_{GATE}	Voltage on GATE pin vs. GNDISO	-	VL-0.30	VH + 0.30	V
V_{CLAMP}	Voltage on CLAMP pre-driver output (CLAMP vs. VLPWR)	-	-0.30	(+ 20, VH + 0.3) min.	V
$I_{CLAMPsink}$	CLAMP pre-driver output sink current	CLAMP = HIGH	-	10	mA
$I_{CLAMPsource}$	CLAMP pre-driver output source current	-	-	Self limited(2)	mA
V_{DESAT}	Voltage on DESAT pin vs. GNDISO	-	-0.30	VH + 0.30	V
V_{ADCP}	Voltage on ADCP pin vs. GNDISO	-	-0.30	3.6	V
V_{ADCN}	Voltage on ADCN pin vs. GNDISO	-	-0.30	+0.30	V
V_{SENSE}	Voltage on SENSE pin vs. GNDISO	-	-2	(VH +0.30, 20) min.	V
$V_{CECLAMP}$	Voltage on VCECLAMP pin vs. GNDISO	-	VL -0.30	VH +0.30	V
$V_{2LTO_SOFTOFF}$	Voltage on 2LSO pin vs. GNDISO	-	VL -0.30	VH +0.30	V
V_{ASC}	Voltage on ASC pin vs. GNDISO	-	-0.30	VH +0.30	V
$V_{DEFAULT}$	Voltage on DEFAULT pin vs. GNDISO	-	-0.30	VH +0.30	V
V_{DIAGx}	Open drain output voltage	-	-0.30	6	V
T_J	Junction temperature	-	-40	150	°C
T_{STG}	Storage temperature	-	-50	150	°C
T_A	Ambient temperature	-	-40	125	°C
P_{Din}	Power dissipation input chip	T_A = 80 °C	-	600	mW
P_{Dout}	Power dissipation output chip	T_A = 80 °C	-	800	mW
ESD	Human body model	-	2		kV

1. V_{PS} = VLPWR – VL
2. *Actual limit depends on power dissipation constraints*

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	51	°C/W

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3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Max.	Unit
VH	High voltage side positive power supply voltage (VH vs. GNDISO)	-	5(1)	32	V
VL	High voltage side negative supply voltage (VL vs. GNDISO)	-	-10	0(2)	V
VREGISO	High voltage side logic supply voltage (VREGISO vs. GNDISO)	-	3.3 ± 5%		V
V_{HL}	Differential supply voltage (VH vs. VL)	-	5	32	V
V_{PS}(3)	Differential voltage between VLPWR and VL pin	-	-100	100	mV
VCC	Low voltage side power supply voltage vs. GND	-	7.2	24	V
3V3IN	Low voltage side power supply voltage vs. GND	-	3.3 ± 5%		V
V_{LOGIC_INPUT}	Logic pins voltage vs. GND	-	0	5.5	V
V_{DIAGx}	Open drain output voltage	-	0	5.5	V
V_{ADCP}	ADCP voltage vs. GNDISO	-	0	3.0	V
V_{ADCN}	ADCN voltage vs. GNDISO	-	0	100	mV
GATE	GATE pin voltage vs. GNDISO	-	VL	VH	V
ASC	ASC pin voltage vs. GNDISO	-	0	$(VH, 15)_{min}$	V
DEFAULT	DEFAULT pin voltage vs. GNDISO	-	0	$(VH, 15)_{min}$	V
$V_{DESATth}$	Desaturation protection threshold	DESAT enabled	-	VH – 2 V	V
f_{SW}	Maximum switching frequency	-	-	80 (4)(5)	kHz

1. *When UVLO is enabled this value is VH_{on},max*
2. *When UVLO is enabled this value is VL_{on},min*
3. *V_{PS} = VLPWR – VL*
4. *Actual limit depends on power dissipation constraints*
5. *A lower switching frequency is suggested if continuous readings of HV side registers and ADC sampling are implemented*

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4 Electrical characteristics

4.1 AC operation

Table 5. AC operation electrical characteristics

(T_J = -40 to 125 °C, VH = 15 V, VL = GNDISO, VCC = 15 V, 3V3IN = 3.3 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{deglitch}$	Input deglitch time	INfilter = ‘01’	50	70	90	ns
		INfilter = ‘10’	100	160	220	ns
		INfilter = ‘11’	420	500	580	ns
t_{INmin}	Minimum propagated input pulse	INfilter = ‘00’	-	-	20	ns
t_{Don}	Input to output propagation delay ON	INfilter = ‘00’, DTset = ‘000’ to OUT2, No load See Figure 11	45	60	100	ns
t_{Doff}	Input to output propagation delay OFF	INfilter = ‘00’, DTset = ‘000’ to OUT1, No load Figure 11	45	60	100	ns
t_{r1}	OUT1 rise time	C_L = 1 nF, 10% ÷ 90%	-	-	15	ns
t_{f1}	OUT1 fall time	C_L = 1 nF, 90% ÷ 10%	-	-	45	ns
$t_{r2,CLAMP}$	OUT2, CLAMP rise time	C_L = 1 nF, 10% ÷ 90%	-	-	45	ns
$t_{f2,CLAMP}$	OUT2, CLAMP fall time	C_L = 1 nF, 90% ÷ 10%	-	-	15	ns
PWD	Pulse width distortion $\lvert t_{Don} - t_{Doff} \rvert$	t_{IN} > 100 ns INfilter = ‘00’	-	0	30	ns
OUT_{DT}	"OUT1 to OUT2" and "OUT2 to OUT1" deadtime	OUT_DTth = ‘0’	46	55	64	ns
		OUT_DTth = ‘1’	77	88	97	ns
DT	Deadtime	DTset = ‘000’	Disabled			ns
		DTset = ‘001’	205	250	310	
		DTset = ‘010’	410	500	610	
		DTset = ‘011’	615	750	905	
		DTset = ‘100’	820	1000	1200	
		DTset = ‘101’	1025	1250	1495	
		DTset = ‘110’	1230	1500	1790	
		DTset = ‘111’	1640	2000	2380	
$t_{release}$	Minimum flag release time	$\overline{SD}$= ‘0’, SD_FLAG = ‘1’	-	-	100	µs
CMTI (1)	Common-mode transient immunity, $\lvert dV_{ISO}/dt \rvert$	V_{CM} = 1200 V see Figure 49	100	-	-	V/ns

1. *Characterization data, not tested in production.*

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4.2 DC operation

Table 6. DC operation electrical characteristics

(TJ = -40 to 125 °C, VH = 15 V, VL = GNDISO, VCC = 15 V, 3V3IN = 3.3 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic inputs/output						
V_{ol}	SDO, ADC logic “0” output voltage	I = 4 mA	-	-	0.15	V
V_{oh}	SDO, ADC logic “1” output voltage	I = 4 mA	3V3IN - 0.15	-	-	V
I_{IN+h}	IN+ logic “1” input bias current	Vin = 3.3 V	41	66	88	µA
I_{IN+l}	IN+ logic “0” input bias current	Vin = GND	-	-	0.10	µA
I_{IN-h}	IN- logic “1” input bias current	Vin = 3.3 V	-	-	0.10	µA
I_{IN-l}	IN- logic “0” input bias current	Vin = GND	12	18	26	µA
I_{SD+h}	$\overline{SD}$ logic “1” input bias current	Vin = 3.3 V	41	66	88	µA
I_{SD+l}	$\overline{SD}$ logic “0” input bias current	Vin = GND	-	-	0.10	µA
I_{CSh}	$\overline{CS}$ logic “1” input bias current	Vin = GND	35	60	95	µA
I_{CSl}	$\overline{CS}$ logic “0” input bias current	Vin = 3.3 V	-	-	0.10	µA
R_{in_pd}	IN+ and $\overline{SD}$ input pull-down resistors	Vin = 3.3 V	37	50	81	kΩ
R_{in_IN-}	IN- input pull-up resistor	-	126	180	275	kΩ
R_{in_CS}	$\overline{CS}$ input pull-up resistor	Vin = GND	34	55	95	kΩ
V_{IL}	Low logic level voltage	-	0.29 · 3V3IN	0.33 · 3V3IN	0.37 · 3V3IN	V
V_{IH}	High logic level voltage	-	0.62 · 3V3IN	0.66 · 3V3IN	0.72 · 3V3IN	V
V_{hyst}	Logic input threshold hysteresis	-	1.05	1.15	1.25	V
Driver buffer section and CLAMP function						
$I_{OUT1source}$	Source peak current	t_{pulse} < 5 µs DC = 1 %	1650	2500	3400	mA
$I_{OUT1sink}$	Sink peak current	t_{pulse} < 5 µs DC = 1 %	400	600	800	mA
$I_{OUT2source}$, $I_{CLAMPsource}$	Source peak current	t_{pulse} < 5 µs DC = 1 %	350	600	900	mA
$I_{OUT2sink}$, $I_{CLAMPsink}$	Sink peak current	t_{pulse} < 5 µs DC = 1 %	1700	2400	3100	mA
$I_{SOFTOFFsink}$	Sink peak current	t_{pulse} < 5 µs DC = 1 %	440	800	1400	mA
$R_{DSonOUT1source}$	Source MOSFET R_{DS_on}	I_D = 100 mA	0.8	1.5	2.8	Ω
$R_{DSonOUT2sink}$, $R_{DSonCLAMPsink}$	Sink MOSFET R_{DS_on}	I_D = 100 mA	0.5	0.8	1.8	Ω
$R_{DSonSOFTOFFsink}$	Sink MOSFET R_{DS_on}	I_D = 20 mA	2.5	4.5	10	Ω
$OUT1_{LOW}$	OUT1 low output voltage	No load, VH – VL = 15 V	VH-13	VH-11.7	VH-10.5	V

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Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$OUT1_{LOW}$	OUT1 low output voltage	No load, VH – VL = 5 V	VL+0.4	VL+0.7	VL+1.1	V
$OUT2_{HIGH}$, $CLAMP_{HIGH}$	OUT2, CLAMP high output voltage	No load, VH – VL = 15 V	VL+10.5	VL+11.7	VL+13	V
		No load, VH – VL = 5 V	VH-1.1	VH-0.7	VH-0.4	
V_{GATEth_OFF}	CLAMP function voltage threshold	GATE vs. VL	1.7	2	2.3	V
V_{GATEth_ON}	GATE voltage ON threshold	GATE vs. VH	-1.7	-2	-2.3	V
t_{CLAMP}	V_{GATEth_OFF} to CLAMP propagation delay	OUT1 = HIGH OUT2 = HIGH	30	50	80	ns
Supply voltage						
$UVLO3V3IN_{ON}$	3V3IN UVLO turn-on threshold	-	2.7	2.9	3.04	V
$UVLO3V3IN_{OFF}$	3V3IN UVLO turn-off threshold	-	2.67	2.85	2.98	V
$UVLO3V3IN_{hys}$	3V3IN UVLO hysteresis	-	45	55	65	mV
I_{Q3V3}	3V3IN quiescent supply current	INx = GND	-	7	11.2	mA
		IN- = GND IN+ = $\overline{SD}$ = 3V3IN	-	12	19.2	
		IN- = GND SD = 3V3IN IN+: f = $f_{SW,MAX}$ D = 50%	-	9.5	15.	
VCC_{on}	VCC UVLO turn-on threshold	-	6.6	7	7.4	V
VCC_{off}	VCC UVLO turn-off threshold	-	6.4	6.8	7.2	V
VCC_{hys}	VCC UVLO hysteresis	-	0.185	0.235	0.285	V
I_{QCC}	VCC quiescent supply current	SW no load F_{swDCDC} = 400 kHz	-	2	4	mA
VH_{on}	VH UVLO turn-on threshold	VHONth = '000'	Disabled			V
		VHONth = '001'	10.35	11	11.55	
		VHONth = '010'	11.30	12	12.60	
		VHONth = '011'	12.25	13	13.65	
		VHONth = '100'	13.15	14	14.70	
		VHONth = '101'	14.10	15	15.95	
		VHONth = '110'	15.00	16	17.00	
		VHONth = '111'	15.95	17	18.05	
VH_{off}	VH UVLO turn-off threshold	VHONth = '000'	Disabled			V
		VHONth = '001'	9.40	10	10.60	
		VHONth = '010'	10.35	11	11.55	
		VHONth = '011'	11.30	12	12.60	
		VHONth = '100'	12.25	13	13.65	
		VHONth = '101'	13.15	14	14.70	
		VHONth = '110'	14.10	15	15.95	
		VHONth = '111'	15.00	16	17.00	
VH_{hyst}	VH UVLO hysteresis	-	0.7	1	1.3	V
VL_{off}	VL UVLO	VLONth = '00'	Disabled			V

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Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VL_{off}	turn-off threshold	VLONth = '01'	-2.10	-2	-1.80	V
		VLONth = '10'	-4.25	-4	-3.80	
		VLONth = '11'	-6.35	-6	-5.70	
VL_{on}	VL UVLO turn-on threshold	VLONth = '00'	Disabled			V
		VLONth = '01'	-3.15	-3	-2.80	
		VLONth = '10'	-5.25	-5	-4.70	
		VLONth = '11'	-7.35	-7	-6.55	
VL_{hys}	VL UVLO hysteresis	-	0.7	1	1.3	V
$OVVH_{on}$	VH OVLO turn-on threshold	OVLOVHth = '00'	16.90	18	19.10	V
		OVLOV Hth= '01'	18.80	20	21.20	
		OVLOVHth = '10'	20.70	22	23.35	
		OVLOVHth = '11'	31.1	33	34.9	
$OVVH_{off}$	VH OVLO turn-off threshold	OVLOVHth = '00'	17.85	19	20.15	V
		OVLOVHth = '01'	19.75	21	22.25	
		OVLOVHth = '10'	21.60	23	24.40	
		OVLOVHth = '11'	32.1	34	35.9	
$OVVH_{hys}$	VH OVLO hysteresis	-	0.7	1	1.3	V
$OVVL_{off}$	VL OVLO turn-off threshold	-	-12.8	-12	-11.2	V
$OVVL_{on}$	VL OVLO turn-on threshold	-	-11.8	-11	-10.2	V
$OVVL_{hyst}$	VL OVLO hysteresis	-	0.7	1	1.3	V
I_{QH}	VH quiescent supply current	$\overline{SD}$ = 3V3IN IN+ = IN- = GND	-	10	13	mA
		$\overline{SD}$ = 3V3IN IN- = GND IN+: f = $f_{SW,MAX}$ D=50%	-	12	18	
I_{QL}	VL quiescent supply current	$\overline{SD}$ = 3V3IN IN+ = IN- = GND	-	2.5	3.5	mA
		$\overline{SD}$ = 3V3IN IN- = GND IN+: f = $f_{SW,MAX}$ D=50%	-	3.2	5	
Isolated Flyback Controller section – Oscillator						
F_{swDCDC}	Main oscillator frequency	CONTROLLER_FREQ = '00'	370	400	430	kHz
		CONTROLLER_FREQ = '01'	180	200	220	
		CONTROLLER_FREQ = '10'	270	300	330	
		CONTROLLER_FREQ = '11'	540	600	660	
ΔF_{swDCDC}	Frequency jittering peak amplitude	-	1.4	1.75	2	% of F_{swDCDC}
F_{jit}	Jittering frequency	-	400	500	600	Hz
Isolated Flyback Controller section – Demagnetization Detector						
I_{FB}	Static Input Bias Current	V_{FB} = 2.5 V	-	0.5	1	µA
V_{FBH}	Upper Clamp Voltage	I_{FB} = 1 mA	3	3.3	3.6	V

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Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{FBL}	Lower Clamp Voltage	I_{FB} = - 1 mA	-90	-60	-30	mV
dV_{FB}/dt	Minimum detectable slope	Voltage falling	0.05	0.08	0.15	V/µs
V_{FBA}	Arming Voltage	Positive-going edge, % of sampled voltage	69	75	81	%
V_{FBT}	Triggering Voltage	Negative-going edge, % of sampled voltage	61	67	73	%
t_{BLANK}	Demag detection blanking time	After V_{SW} going low	140	203	240	ns
Isolated Flyback Controller section – Transconductance Error Amplifier of PSR loop						
V_{REF}	Voltage Reference	T_J = 25 °C	2.45	2.5	2.55	V
		T_J = -40 ÷ +125 °C	2.425	-	2.575	
g_m	Transconductance	V_{FB} = 2.5 V	1.6	2.3	3.1	mS
I_{COMP}	Source Current	V_{COMP} = 2.8 V	0.65	1	1.3	mA
	Sink Current	V_{COMP} = 0.9 V	1.3	2	2.5	mA
$V_{COMPsat.hi}$	Upper saturation voltage	I_{COMP} = 100 µA (source)	3V3IN -100mV	-	3V3IN	V
Isolated Flyback Controller section – burst mode						
V_{COMP_BM}	Burst-mode entry level	-	1.05	1.1	1.15	V
V_{COMP_PRK}	Parking level during idle mode	-	1.1	1.15	1.2	V
V_{COMP_0}	COMP offset	-	0.9	1.02	1.1	V
G_{FF}	Feedforward gain	-	0.125	0.150	0.175	-
t_{WAKE}	Burst repetition time	-	400	500	600	µs
Isolated Flyback Controller section – Current sensing						
Isns	Bias current	V_{sns} = 0.2 V, V_{sw} = V_{sw_H}	-	-	1	µA
$t_{d(H-L)}$	Delay to Output	dV_{CS}/dt = 0.5 V/µs	20	45	70	ns
t_{LEB}	Leading Edge Blanking time	-	50	70	110	ns
V_{sns_OCP1}	Cycle-by-cycle OCP level	-	110	125	150	mV
V_{sns_OCP2}	2nd OCP level	-	170	200	230	mV
Isolated Flyback Controller section – Internal soft-start						
t_{SS}	Soft-start time	-	5	8	11	ms
Isolated Flyback Controller section – Output undervoltage protection						
V_{UVP}	UVP threshold	-	1.045	1.1	1.155	V
t_{UVP}	UVP blanking time	After soft-start end	17	25	33	ms
N_{UVP}	Consecutive cycles for UVP triggering	Continuos switching	-	4	-	-
		Burt Mode wake up	-	3	-	
Isolated Flyback Controller section – Fault protection timer						
$t_{RESTART}$	Restart delay after fault	-	0.53	0.8	1.06	s
Isolated Flyback Controller section – Aux winding disconnection detection						
I_{FBON}	Min. source current	SW = HIGH	20	40	55	µA
Isolated Flyback Controller section – Gate driver						

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Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SW_L}	Output Low Voltage	I_{sink} = 100 mA	0.145	0.3	0.55	V
V_{SW_H}	Output High voltage	I_{source} = 5 mA	8	9.5	11	V
		VCC > 7.6 V I_{source} = 5 mA	6	7.5	9	
		VCC = VCC_{off} + 100 mV I_{source} = 5 mA	6.2	6.7	7.2	
I_{src_pk}	Peak source current	-	0.220	0.550	0.800	A
I_{sk_pk}	Peak sink current	-	0.517	1.1	1.62	
t_f	Fall time	C_L = 1 nF, 80% ÷ 20%	7	13	20	ns
t_r	Rise time	C_L = 1 nF, 20% ÷ 80%	5	20	40	ns
R_{UVLO}	R UVLO saturation	-	14	25	34	kΩ
V_{SW_OFF}	SW LOW without 3V3IN	3 < VCC < 24 V, 3V3IN = GND, I_{sk} = 1 mA	0.21	0.37	0.735	V
Desaturation protection						
$V_{DESATth}$	Desaturation threshold	DESATth = '000'	2.80	3	3.20	V
		DESATth = '001'	3.60	4	4.20	
		DESATth = '010'	4.60	5	5.30	
		DESATth = '011'	5.50	6	6.30	
		DESATth = '100'	6.50	7	7.40	
		DESATth = '101'	7.40	8	8.40	
		DESATth = '110'	8.30	9	9.40	
		DESATth = '111'	9.30	10	10.50	
$t_{DESfilter}$	DESAT pin deglitch filter	DESATth = '100' (1)	-	20	-	ns
I_{DESAT}	DESAT blanking charge current	DESATcur = '00'; VDESAT = 0 V	230	250	270	µA
		DESATcur = '01'; V_{DESAT} = 0 V	460	500	540	
		DESATcur = '10'; V_{DESAT} = 0 V	680	750	810	
		DESATcur = '11'; V_{DESAT} = 0 V	910	1000	1080	
I_{DESoff}	DESAT blanking discharge current	V_{DESAT} = 8 V IN+= GND;	35	70	90	mA
t_{FBLK}	DESAT fixed blanking time	-	160	250	340	ns
t_{DESAT}	DESAT intervention time	DESATth = '000' 0→5 V step on V_{DESAT} Step to OUT1 10%	80	150	220	ns
Soft turn-Off function						
$t_{2LTO_SOFTtime}$	SOFTOFF MOSFET activation time when the Soft turn-off function is triggered (SAFE_OF =1; SOFT_2LTO=0)	2LTO_SOFTtime = '1111'	0.22	0.25	0.3	µs
		2LTO_SOFTtime = '0000'	0.43	0.50	0.59	
		2LTO_SOFTtime = '0001'	0.64	0.75	0.89	
		2LTO_SOFTtime = '0010'	0.89	1.00	1.15	
		2LTO_SOFTtime = '0011'	1.36	1.50	1.65	
		2LTO_SOFTtime = '0100'	1.83	2.00	2.18	
		2LTO_SOFTtime = '0101'	2.30	2.50	2.70	

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Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{2LTO_SOFTtime}$	SOFTOFF MOSFET activation time when the Soft turn-off function is triggered (SAFE_OF =1; SOFT_2LTO=0)	2LTO_SOFTtime = ‘0110’	2.77	3.00	3.23	µs
		2LTO_SOFTtime = ‘0111’	3.25	3.50	3.75	
		2LTO_SOFTtime = ‘1000’	3.47	3.75	4.03	
		2LTO_SOFTtime = ‘1001’	3.71	4.00	4.29	
		2LTO_SOFTtime = ‘1010’	3.94	4.25	4.56	
		2LTO_SOFTtime = ‘1011’	4.18	4.50	4.82	
		2LTO_SOFTtime = ‘1100’	4.42	4.75	5.08	
		2LTO_SOFTtime = ‘1101’	4.66	5.00	5.34	
		2LTO_SOFTtime = ‘1110’	4.90	5.25	5.63	
SENSE overcurrent function						
$V_{SENSEth}$	SENSE protection threshold	SENSEth = ‘000’	88	100	112	mV
		SENSEth = ‘001’	110	125	140	
		SENSEth = ‘010’	135	150	165	
		SENSEth = ‘011’	158	175	192	
		SENSEth = ‘100’	185	200	215	
		SENSEth = ‘101’	235	250	268	
		SENSEth = ‘110’	285	300	315	
		SENSEth = ‘111’	380	400	420	
t_{SENSE}	SENSE protection intervention time	SENSEth = ‘111’ 0→1 V step on V_{SENSE} Step to OUT1 10%	50	95	120	ns
VCE active clamping protection						
V_{CECLth}	VCE clamping threshold	-	VL + 1.20	VL + 1.60	VL + 2	V
$V_{CECLhyst}$	VCE clamping hysteresis	-	0.30	0.50	0.60	V
t_{VCECL}	VCE clamping intervetion time	-	10	22	35	ns
t_{COUNT_ACTIVE}	VCE clamping observation window after turn-off command	-	2.77	3	3.23	µs
$t_{VCECLoff}$	VCE clamping time-out	-	2	2.30	2.7	µs
Diagnostics output						
$t_{DIAG1,2}$	Fault event to DIAGx Low delay	Fault event to DIAGx 90%	-	4	-	µs
$I_{DIAG1,2}$	DIAGx low level sink current	V_{DIAGx} = 0.4 V	8	18	30	mA
$R_{DIAG1,2}$	DIAGx pull-down resistor	-	330	550	800	kΩ
Analog measurement function						
I_{ADCP}	Current source connected to ADCP pin	ADC_CScur = ‘00’	Disabled			uA
		ADC_CScur = ‘10’	260	300	330	
		ADC_CScur = ‘01’	500	600	660	
		ADC_CScur = ‘11’	850	1000	1100	
RES	ADC resolution	ADC_LOWth = ‘000’ and ADC_HIGHth = ‘111’	-	8	-	bit
t_{PER_CONV}	ADC periodic conversion rate	-	80	100	120	µs

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Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{ADC}	PWM ADC output frequency	ADC_PWM_EN = '1' and ADC_EN = '1'	8	10	12	kHz
$DC1_{ADC}$	ADC signal maximum duty cycle	ADC_PWM_EN = '1' STATUS5 = 0x00	-	90	-	%
$DC2_{ADC}$	ADC signal medium duty cycle	ADC_PWM_EN = '1' STATUS5 = 0x80	-	50	-	%
$DC3_{ADC}$	ADC signal minimum duty cycle	ADC_PWM_EN = '1' STATUS5 = 0xFF See Section 7.10for details.	-	10	-	%
ADC_HIGHth	ADC higher input threshold level	ADC_HIGHth = '000'	1.470	1.500	1.530	V
		ADC_HIGHth = '001	1.685	1.715	1.745	
		ADC_HIGHth = '010'	1.890	1.930	1.970	
		ADC_HIGHth = '011'	2.110	2.145	2.180	
		ADC_HIGHth = '100'	2.310	2.360	2.400	
		ADC_HIGHth = '101'	2.520	2.570	2.610	
		ADC_HIGHth = '110'	2.730	2.785	2.830	
		ADC_HIGHth = '111'	2.940	3.000	3.040	
ADC_LOWth	ADC lower input threshold level	ADC_LOWth = '000'	-	0	0.015	V
		ADC_LOWth = '001	0.200	0.215	0.230	
		ADC_LOWth = '010'	0.405	0.430	0.455	
		ADC_LOWth = '011'	0.615	0.645	0.670	
		ADC_LOWth = '100'	0.830	0.855	0.890	
		ADC_LOWth = '101'	1.035	1.070	1.105	
		ADC_LOWth = '110'	1.250	1.285	1.320	
		ADC_LOWth = '111'	1.465	1.500	1.530	
ADC_OFFSerr	ADC offset error	ADC_LOWth = '000' and ADC_HIGHth = '111'	-3	-	3	LSB
ADC_GAINerr	ADC gain error		-7	-	3.5	LSB
INL	ADC INL		-3	-	3	LSB
DNL	ADC DNL		-1	-	1	LSB
ADC_IN_LEAK	ADC Input leakage current	ADC_LOWth = '000' and ADC_HIGHth= '111' ADCP-ADCN=3.3 V	-	-	0.50	uA
ASC function						
ASC_{IL}	Low logic level voltage	-	0.80	1.10	1.40	V
ASC_{IH}	High logic level voltage	-	1.80	2.20	2.40	V
ASC_{hyst}	Hysteresis	-	0.95	1.1	1.25	V
I_{ASCh}	ASC logic "1" input bias current	V_{ASC} = 5 V	25	50	75	µA
I_{ASCl}	ASC logic "0" input bias current	V_{ASC} = 0 V	-	-	0.10	µA
R_{ASC}	ASC pull-down resistor	V_{ASC} = 1.5 V	35	50	70	kΩ
t_{ASC}	ASC intervention time	V_{ASC} = 5 V SeeFigure 38	30	55	100	ns
DEFAULT function						
$DEFAULT_{IL}$	Low logic level voltage	-	0.80	1.10	1.40	V

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Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$DEFAULT_{IH}$	High logic level voltage	-	1.80	2.20	2.40	V
$DEFAULT_{hyst}$	hysteresis	-	0.95	1.1	1.25	V
$t_{DEL_HW3PS_ON}$	Delay entering into HW3PS state	$V_{DEFAULT}$ = VREGISO	80	100	120	µs
Functionality checks						
t_{Rchk}	SENSE resistor check time	-	-	-	15	µs
$I_{SENSERchk}$	SENSE resistor check current	V_{SENSE} < 1 V	8	10	12	µA
Overtemperature protection						
T_{WARN}	Warning temperature(1)	-	125	-	-	°C
T_{SDN}	Shutdown temperature(1)	-	155	-	-	°C
T_{hys}	Temperature hysteresis(1)	-	-	20	-	°C
SPI (1)						
t_{CKmax}	Maximuym SPI clock frequency	-	5	-	-	MHz
t_{rCK} t_{fCK}	SPI clock rise and fall time	C_L = 30 pF	-	-	25	ns
t_{hCK} t_{lCK}	SPI clock high and low time	-	75	-	-	ns
t_{setCS}	$\overline{CS}$ set-up time	-	350	-	-	ns
t_{holdCS}	$\overline{CS}$ hold time	-	10	-	-	ns
t_{desCS_LRD}	$\overline{CS}$ deselect time (2)	Local register read	800	-	-	ns
t_{desCS_RRD}		Remote register read	30	-	-	µs
t_{desCS_STC}		Start configuration	1	-	-	µs
t_{desCS_SPC}		Stop configuration	8	-	-	µs
t_{desCS_RST}		ResetStatus, SoftReset	8	-	-	µs
t_{desCS_LWR}		Local register write	700	-	-	ns
t_{desCS_RWR}		Remote register write	12	-	-	µs
t_{desCS_NOP}		NOP command	700	-	-	ns
t_{setSDI}	SDI set-up time	-	25	-	-	ns
$t_{holdSDI}$	SDI hold time	-	20	-	-	ns
t_{enSDO}	SDO enable time	-	-	-	38	ns
t_{disSDO}	SDO disable time	-	-	-	47	ns
t_{vSDO}	SDO valid time	-	-	-	57	ns
$t_{holdSDO}$	SDO hold time	-	37	-	-	ns
t_{SDLCSL}	$\overline{SD}$ falling to $\overline{CS}$ falling	-	350	-	-	ns
t_{CSHSDH}	$\overline{CS}$ rising to $\overline{SD}$ rising	-	350	-	-	ns
t_{CFG}	Configuration timer	-	2.0	2.5	3.0	ms

1. *Characterization data, not tested in production.*
2. *See Section 9*

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5 Isolation

Table 7. Isolation and safety-related specifications

Parameter	Symbol	Value	Unit	Conditions
Clearance (Minimum External Air Gap)	CLR	8	mm	Measured from input terminals to output terminals, shortest distance through air
Creepage (*) (Minimum External Tracking)	CPG	8	mm	Measured from input terminals to output terminals, shortest distance path along body
Comparative Tracking Index (Tracking Resistance)	CTI	≥ 400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 8. Isolation characteristics

Parameter	Symbol	Test conditions	Characteristic	Unit
Maximum Working Isolation Voltage	V_{IORM}		1200	V_{PEAK}
Apparent Charge (Partial Discharge) In accordance to VDE 0884-17	V_{PR}	Method a, Type test	1920	V_{PEAK}
		$V_{PR} = V_{IORM} \times 1.6$, t_m = 10 s		
		Partial discharge < 5 pC		
		Method b1, 100% Production test	2250	V_{PEAK}
		$V_{PR} = V_{IORM} \times 1.875$, t_m = 1 s		
		Partial discharge < 5 pC		
Transient Overvoltage (Highest Allowable Overvoltage)	V_{IOTM}	t_{ini} = 60 s Type test	6400	V_{PEAK}
Maximum Surge Test Voltage	V_{IOSM}	Type test	6400	V_{PEAK}
Isolation Resistance	R_{IO}	V_{IO} = 500 V, Type test	$>10^9$	Ω

Table 9. Isolation voltage as per UL 1577

Parameter	Symbol	Test conditions	Characteristic	Unit
Isolation Withstand Voltage	V_{ISO}	1 min. (type test)	3770/5330	$V_{rms/PEAK}$
Isolation Test voltage	$V_{ISO,test}$	1 sec. (100% production)	4525/6400	$V_{rms/PEAK}$

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6 Power supply management

6.1 Low voltage side

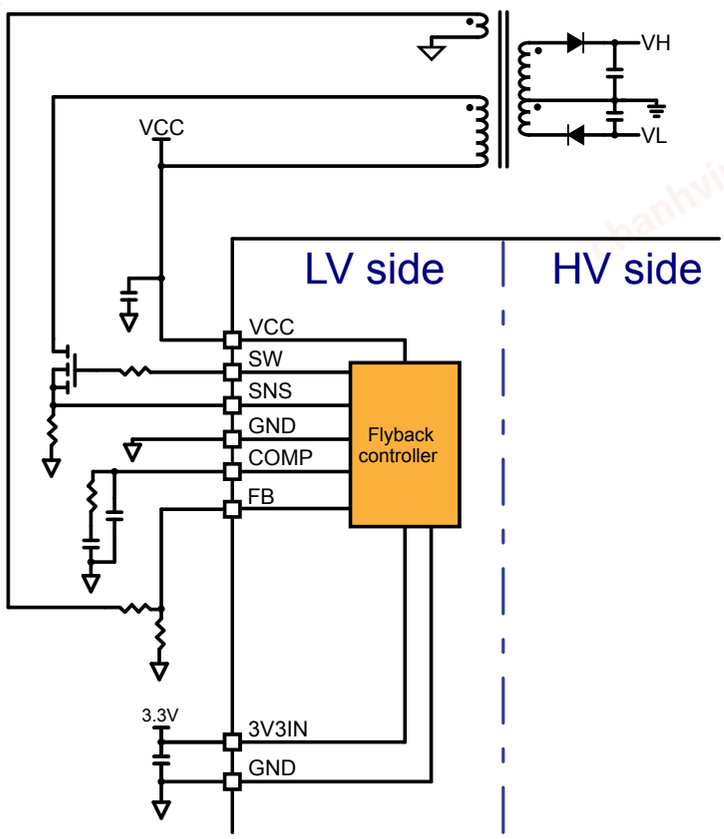
The power supply of the low voltage side has to be provided to the 3V3IN pin. The supply voltage must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors and are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to the 3V3IN supply pin and a second bypass capacitor with greater value must be placed close to it. A capacitor with a minimum 4.7 uF value is recommended.

After the LV side power-on the LVReset bit in STATUS4 register is set HIGH (see Section 9.2.11).

6.2 Integrated flyback controller for isolated power supply

The device integrates in the low voltage section a controller for an isolated flyback DC-DC converter that can be used to generate the VH and VL supply voltages for the gate driving section. The input voltage of the flyback transformer is also fed to the VCC pin and it is used to generate the voltage on the SW pin that drives the external MOSFET.

Figure 3. Isolated flyback power supply



The PWM controller included in the STGAP4S is a voltage-mode controller designed for flyback converters operated from a low DC bus voltage in Discontinuous Conduction Mode (DCM) at a fixed frequency. The input voltage feedforward feature provides the converter with the same dynamic characteristics as with peak current mode control.

The operating frequency is set by an oscillator whose frequency can be chosen in a set of four possible values by means of two programming bits. Its frequency is jittered to mitigate EMI emissions. At very light load the controller enters a controlled burst-mode operation that helps minimize the consumption from the input line.

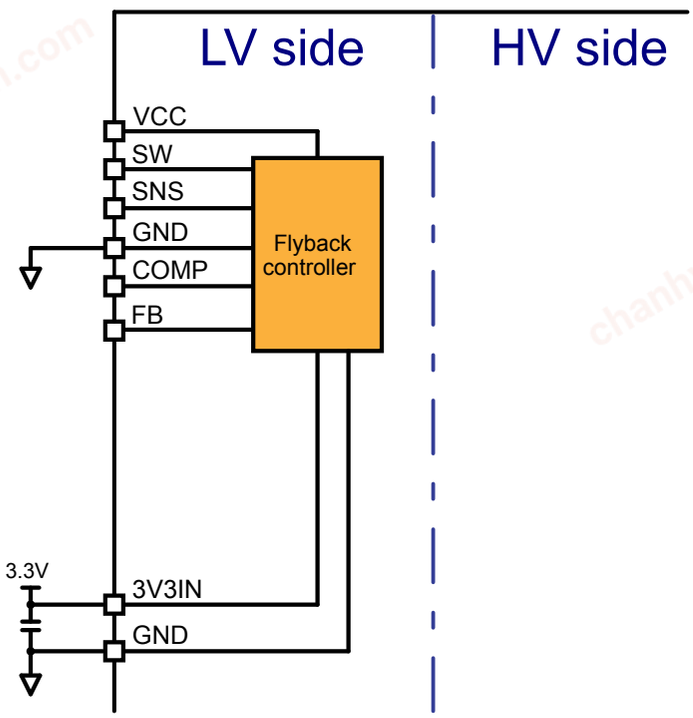
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The device can provide constant output voltage (CV) regulation using the primary-sensing regulation (CV-PSR) technique. This eliminates the need for the optocoupler and the secondary voltage reference, still maintaining quite accurate regulation. Additionally, reducing the components across the isolation barrier leads to greater safety and reliability.

The controller embeds a full set of protection functions: input undervoltage, output overvoltage (OVP), output undervoltage (UVP), anti-CCM operation, a first-level overcurrent protection (OCP1) with cycle-by-cycle current limitation and a second-level overcurrent protection (OCP2) that is invoked when the transformer saturates or the secondary diode fails short. The internal soft-start and the leading-edge blanking of the current sense input for greater noise immunity complete the equipment of this device.

In case the flyback controller is not used, the pins VCC, SW, SNS, FB, COMP must be left unconnected and the pin 4 (GND) must be connected to the low side ground together with the pin 18 (GND), as shown in Figure 4. With this configuration of the pins the flyback controller is disabled without affecting the other functions of the device. The VH and VL supply pins of the HV side must be fed by another power supply. As the VCC voltage is below the UVLO turn-off threshold VCC_{off}, the UVLO_VCC flag in the status register STATUS3 is set HIGH and if this flag is associated to one of the diagnostic outputs, $\overline{DIAG1}$ or $\overline{DIAG2}$, the corresponding open drain output MOSFET is turned-on.

Figure 4. Pin configuration for flyback controller disabling

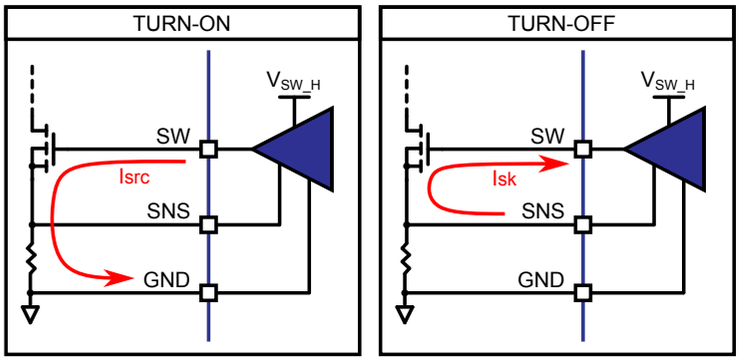


6.2.1 Flyback output stage

The output stage of the flyback controller is designed with different paths for the turn-on and the turn-off phases. At the turn-on the gate driving current is sourced through the SW pin and the gate loop is closed through the GND pin. At the turn-off the gate driving current is sinked by the SW pin and the gate loop is closed through the SNS pin. Thus the SNS pin is part of the gate turn-off loop besides being the pin for the current sensing implemented with the external shunt resistor.

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Figure 5. **Flyback output stage**

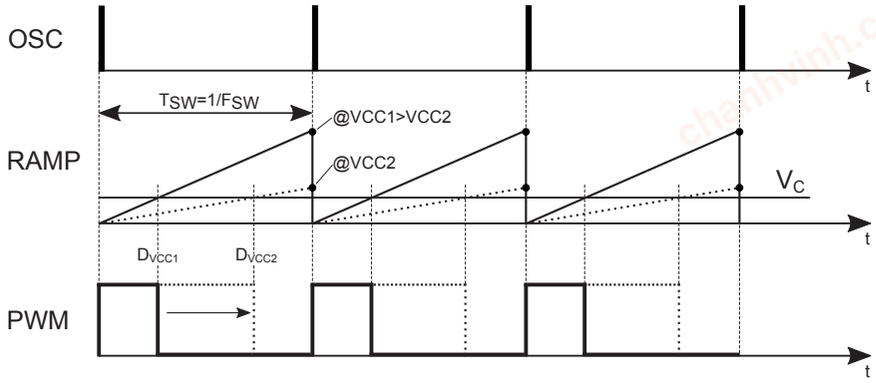


6.2.2 PWM: Voltage-mode control with input voltage feedforward methodology

In voltage-mode control, the PWM is generated by comparing a sawtooth ramp (synchronous to the oscillator) with a fixed control voltage V_C generated by the feedback loop (refer to Figure 7).

Unlike the traditional voltage-mode control, where the sawtooth ramp has a constant amplitude, in this topology the amplitude of the sawtooth ramp varies in direct proportion to the input voltage. Because of that, if the control voltage V_C is constant, the duty cycle varies inversely with the input voltage, thus the volt-second product VCC·D is constant without any control change (see Figure 6).

Figure 6. **Voltage-mode control with input voltage feedforward: operating principle**



A flyback converter operated in the Discontinuous Conduction Mode (DCM) results in excellent open-loop line regulation and very low audio susceptibility, like with peak current mode control. Low closed-loop gain is required to achieve the specification of the output voltage regulation and it may be designed mostly to achieve good dynamic performance.

In this context the choice of using voltage mode with input voltage feedforward control methodology is dictated by the low input voltage: peak current mode control, which is most common in flyback controllers for mains-operated applications, would require a dynamic range of the sensed signal large enough to ensure an acceptable signal-to-noise ratio under all loading conditions. This would eat up a not negligible portion of the input voltage (e.g. ≈ 10% worst case, against < 1% in applications operated from the mains) and would lead to unacceptable losses in the sense resistor.

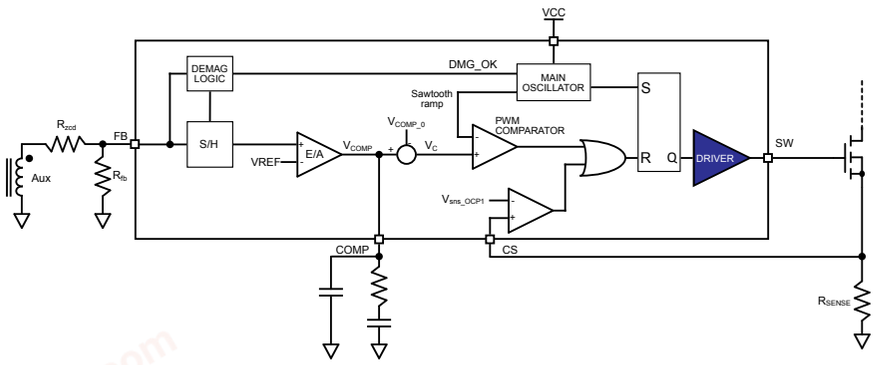
Using voltage-mode control the current sense signal is used for overcurrent protection (OCP) only and the dynamic range can be significantly reduced, being the signal-to-noise ratio significant for the maximum peak current only. This is done with no compromise on the dynamic performance of the converter adding the input voltage feedforward feature.

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6.2.3 Constant voltage primary-sensing regulation (CV-PSR) technique

The controller is specifically designed to work with CV-PSR, whereby the output voltage is sensed indirectly by exploiting the magnetic flux that links the windings in the flyback transformer. More specifically, the output voltage is indirectly observed through a resistor divider sensing the voltage developed across the auxiliary winding during the off-time of the power switch. A high-level block diagram of the internal circuit and the external connections is shown in Figure 7.

Figure 7. CV-PSR: external configuration and principle internal schematic



Due to transformer's parasitics, the auxiliary voltage provides an accurate image of the output voltage V_{out} only in the instant when the secondary current zeroes. A demagnetization detection circuit identifies this instant and the signal on the FB pin is sampled-and-held in that instant. This voltage is compared to the error amplifier internal reference V_{REF} to generate the control voltage Vc provided to the PWM generation block.

The error amplifier is a transconductance type and delivers an output current proportional to the voltage unbalance of the two inputs. The frequency compensation network is connected between its output, available on pin COMP, and GND.

The output voltage can be defined according to the formula:

$$R_{fb}=\frac{V_{REF}}{\frac{N_{aux}}{N_{sec}}Vout-V_{REF}}R_{zcd} \quad (1)$$

where N_{sec} and N_{aux} are respectively the transformer secondary and auxiliary turns number. The R_{zcd} value must be chosen considering that the minimum value of the current sourced by the FB pin during the on-time of the power switch must be larger than the auxiliary winding disconnection detection threshold (I_{FBON}) and its maximum value lower than the I_{FB} AMR:

$$\frac{N_{aux}}{N_{pri}}\frac{Vin_{\min}}{R_{zcd}} > I_{FBON} \qquad \frac{N_{aux}}{N_{pri}}\frac{Vin_{\max}}{R_{zcd}} < I_{FB\,AMR} \quad (2)$$

where N_{pri} is the primary turns number.

6.2.4 Main oscillator with frequency jitter

The main oscillator, which sets the operating frequency of the flyback converter, has an operating frequency F_{swDCDC} with a default typical value of 400 kHz. By programming the appropriate registers its frequency can be changed in a set including three other values: 200, 300 and 600 kHz (typical values).

As shown in Figure 7, the main oscillator generates the pulses that set the PWM latch, determining the turn-on of the power switch, and the sawtooth ramp that, compared to the control voltage V_C by the PWM comparator, resets the PWM latch and determines the turn-off of the power switch. The amplitude of the ramp is adjusted proportionally to the VCC voltage, which is the input voltage of the flyback converter as well. The time relationship between the two signals is illustrated in Figure 6.

It is advantageous to modulate the switching frequency to mitigate converter's EMI emissions. In fact, the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of side-band harmonics. Their overall energy is unchanged, but the individual amplitudes are smaller. The switching frequency is jittered by a percentage ΔF_{DCDC} of the controller switching frequency at a jitter rate F_{jit} with a triangular profile.

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6.2.5 Burst-mode operation

When the load is extremely light or zero at all, the converter enters a controlled on/off operation with essentially constant peak current. A load decrease is then translated into a frequency reduction, which can go down even to few hundred Hertz, thus minimizing the frequency related losses and maintaining the regulation ability without incurring any issues related to the minimum manageable duty cycle.

When V_{COMP} falls below an internally fixed threshold, V_{COMP_BM}, a comparator makes the controller enter an idle state where the SW output is kept in the off-state and most of the internal circuits are disabled to reduce the consumption and minimize the loading on the VCC line. Only the circuitry that determines the end of the idle state stays alive. During the idle state, a “parking circuit” keeps V_{COMP} at a fixed value slightly higher than V_{COMP_BM} plus the hysteresis of the comparator so that the controller is ready to restart.

The end of the idle state is internally clocked: indeed, with PSR the information of the output voltage is acquired by the feedback loop only when the converter is switching because the transformer does not transmit DC information. Therefore, once the converter is stopped at the end of a burst, the loop is opened and no output voltage information is available until switching starts again: the power switch must be then turned on periodically (wake-up) to sense any change in the output voltage.

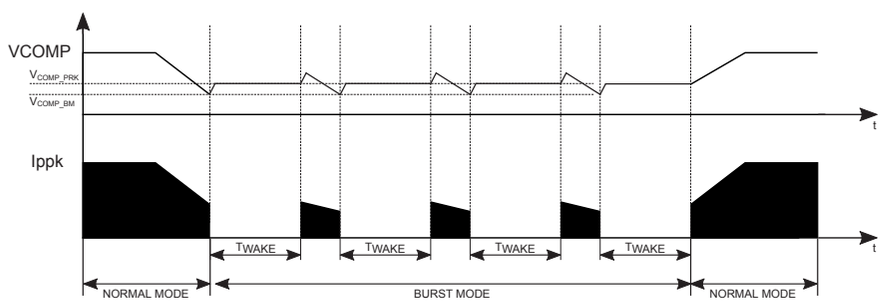
As a result of the energy delivery stop, the output voltage decreases: after t_{WAKE} the controller restarts the switching activity, the parking circuit is disabled after the end of the first cycle and the sampled voltage on the FB pin is compared with the internal reference. If the voltage on the error amplifier output, as a result of the comparison, remains over V_{COMP_BM}, the device continues switching, otherwise it stays off for another t_{WAKE} period. In this way the converter works in burst-mode with an almost constant peak current defined by V_{COMP_BM}. This kind of operation, shown in the timing diagrams of Figure 8, along with the other (continuous switching) previously described, is noise-free since the peak current is low.

The power level P_{outBM} at which the converter enters burst-mode operation can be estimated with the following formula:

$$Pout_{BM} = \frac{\eta}{2Lf_{sw}}\left(\frac{V_{COMP_BM} - V_{COMP_0}}{G_{FF}}\right)^2 \quad (3)$$

Notice, however, that the nonidealities in the control circuit (essentially, propagation delays) cause P_{outBM} to depend on VCC, although ideally not expected.

Figure 8. Load-dependent operating modes: continuous switching and burst-mode operation.



6.2.6 Soft-start

During converter start-up phase, the soft-start function progressively increases the control voltage V_C in 8 steps, each one having 1 ms duration (typical value), starting from an initial low value until the control loop takes over. This helps to reduce the stress on all the power components. For this function no external programming component is required as it is activated at every attempt of converter start-up or restart after a fault.

6.2.7 Anti CCM protection

Ensuring that the flyback converter always works in DCM has a twofold objective: on the one hand it makes the CV-PSR topology correctly monitor the output voltage (CV-PSR principle is based on DCM operation) while on the other hand, at start-up or in case of overload, the transformer is demagnetized in every switching cycle and any risk of current staircasing due to deep CCM (Continuous Current Mode) operation is prevented.

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The same “Demag Logic” function block that in the CV_PSR loop identifies the instant when the secondary current zeroes (demagnetization), provides a DMG_OK signal that is asserted high in each switching cycle only when demagnetization is detected. In case the converter is taken into CCM operation (i.e. the turn-on of the power switch is commanded before the secondary current is zero) the set pulse coming from the oscillator (that generates the turn-on of the power switch and the start of a new switching cycle) is delayed until the DMG_OK signal is asserted high. In this way, the switching frequency becomes lower than the set frequency F_{swDCDC} and the converter works in DCM close to the DCM-CCM boundary. As a side-effect, the power capability of the converter is reduced and the output voltage tends to collapse.

In case of short circuit event the Anti CCM protection is not triggered, nevertheless the maximum primary current is limited by the overcurrent protection (OCP) and the controller is stopped by the output undervoltage protection (UVP).

6.2.8 Current sensing and overcurrent protection (OCP)

The device is equipped with a current sensing input SNS that is used to prevent the peak primary current exceeding a preset value with a cycle-by-cycle current limitation. The current flowing in the power switch is sensed through a shunt resistor R_S connected between its source and the ground. The resistor resulting voltage is sensed through the SNS pin and internally it is compared with a reference V_{sns_OCP1} to determine if the power switch must be turned off. The maximum current level is programmed by means of R_S value:

$$I_{ppk_max}=\frac{V_{SNS_OCP1}}{R_S} \quad (4)$$

R_S is such that the I_{ppk_max} is larger than the expected peak primary current at the maximum load.

For improved noise immunity the sensing is equipped with a blanking time t_{LEB} after the SW turn-on.

In case the first level of overcurrent V_{sns_OCP1} is not able to keep the peak current under control (e.g. in case of transformer saturation or secondary diode short-circuit), a second greater comparison level is located at V_{sns_OCP2}. If this second level is exceeded the controller stops switching and after an idle time $t_{RESTART}$ it goes through a new soft-start sequence.

6.2.9 Output undervoltage protection (UVP)

The output undervoltage function protects the converter in case of severe overload or short-circuit conditions forcing the system to work intermittently (hiccup mode operation).

The voltage sampled on the FB pin at the end of the transformer’s demagnetization is compared with an internal threshold V_{UVP} and if it is lower than this threshold for four consecutive switching cycles (to provide better noise immunity against false protection triggering) an output undervoltage condition is assumed and switching is stopped. The switching resumes after an idle time $t_{RESTART}$ and the converter goes through a new soft-start sequence. Under continuous short-circuit conditions, the converter works intermittently with a low duty cycle (hiccup mode). The average output current and power throughput is then significantly attenuated compared to the levels that would occur in case of continuous operation.

At the end of the soft-start sequence a t_{UVP} blanking time is provided to avoid erroneous UVP triggering during the output voltage rise time.

Note that the UVP level is proportional to the output voltage regulation setpoint. Their ratio is the same as the ratio of V_{REF}/V_{UVP}.

6.2.10 Auxiliary winding disconnection and output overvoltage protection (OVP)

Sensing the voltage across the auxiliary winding through the FB pin plays a fundamental role in the operation of the PWM controller. For this reason, it is extremely important to check the integrity of the connection of the FB pin to the auxiliary winding.

A winding disconnection is sensed by checking the current I_{FB} that the FB pin sources during the on-time of the power switch. This current must exceed a minimum value I_{FBON} to detect that the pin is correctly connected to the winding. If this condition is not met for four consecutive switching cycles, the controller stops switching for an idle time $t_{RESTART}$ and goes through a new soft-start sequence.

As already stated, this function provides a limit to the maximum value of the resistor R_{zcd} that connects the FB pin to the aux winding, constraint here reported for the reader’s convenience:

$$\frac{N_{aux}}{N_{pri}}\frac{Vin_{\min}}{R_{zcd}} > I_{FBON} \quad (5)$$

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With CV-PSR the only hardware failure that may cause the output voltage to rise out of control is just a disconnection of the FB pin from the auxiliary winding. Therefore, this protection serves also as OVP function.

6.2.11 Flyback fault diagnostic

The fault flag FLYBACK _FLT reported in the status register STATUS3 is set HIGH whenever the flyback controller detects one of the following fault conditions:

- Second level overcurrent protection (OCP2)
- Output undervoltage protection (UVP)
- Auxiliary winding disconnection and output overvoltage protection (OVP)

When one of these fault conditions is detected, in addition to stopping the switching, the controller also sets HIGH the FLYBACK _FLT flag immediately and keeps this flag HIGH for all the time $t_{RESTART}$. When the $t_{RESTART}$ expires, the controller sets LOW the flag and goes through a new soft-start sequence. If a fault condition is newly detected, the controller proceeds again as described and thus in case of persistent fault condition the system works intermittently.

6.3 High voltage side

All the power supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors and are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin and a second bypass capacitor with greater value should be placed close to it.

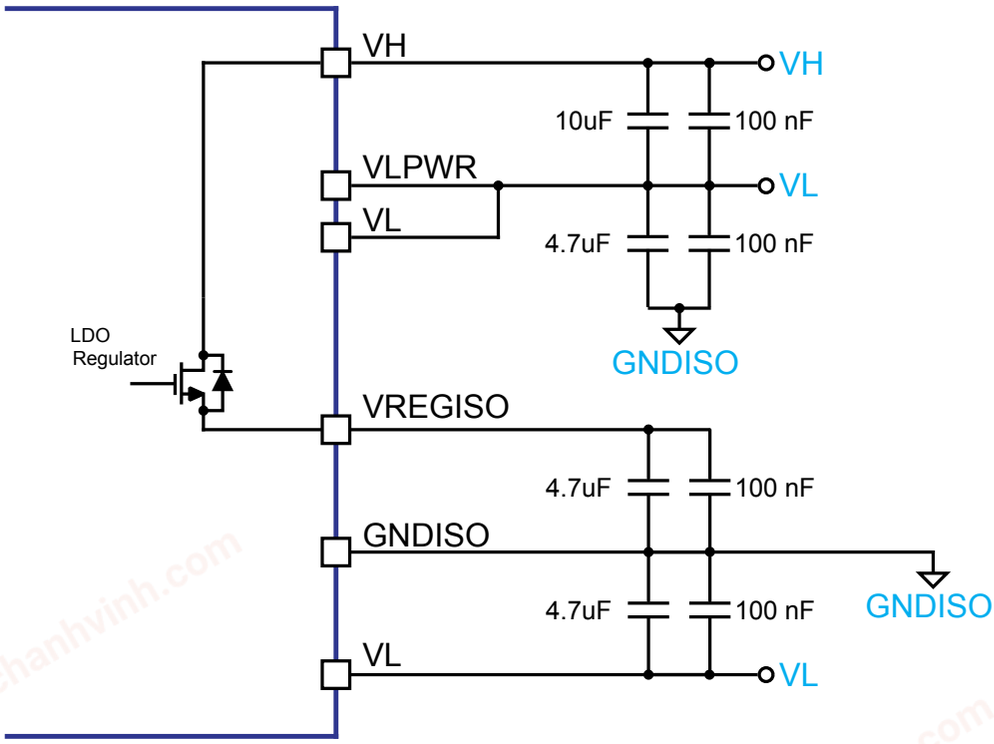
In parallel to the 100 nF one, a capacitor with minimum 10 uF value for the VH supply and 4.7 uF for the negative supply VL (if present) is recommended.

A linear voltage regulator, supplied by the voltage on the VH pin, is integrated in the high voltage side and generates the 3.3 V supply voltage dedicated to the internal logic. Although it is available on the VREGISO pin for filtering purposes it is not intended to supply external components. For the stability of the regulator a capacitor with minimum 4.7 uF value must be connected to the VREGISO pin. Also in this case a 100 nF bypass ceramic capacitor must be placed as close as possible to the VREGISO pin for noise filtering.

After the HV side power-on the HVReset bit in STATUS2 register is set HIGH (see Section 9.2.9).

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Figure 9. **High voltage side 3.3 V internal voltage regulator**



6.4 Operation flowchart

The device can be in one of the following states:

- **Normal operation**
  The outputs OUT1 and OUT2 follow the input commands IN-, IN+, $\overline{SD}$ as described in Section 7.1and can be switched also using the ASC command as described in Section 7.15
- **SafeState**
  The outputs OUT1 and OUT2 are kept HIGH (external power switch in OFF state) whatever the state of the input commands IN-, IN+, $\overline{SD}$. The outputs can be switched using the command ASC as described in Section 7.15
- **HW3PS (Hardware 3 phase short)**
  The outputs OUT1 and OUT2 are kept LOW (external power switch in ON state) whatever the state of the input command IN-, IN+, $\overline{SD}$ and the command ASC.

After the power-on of the HV side the latched flag HVReset='1' forces the driver in SafeState (see Table 62). Other fault flags can be found set to '1' depending on the actual device external conditions, for instance the COMERRR and COMERRL state depends by the power-on timings of the two sides. At the HV side power-on the DEFAULT pin has no influence and the device always goes to SafeState.

When the device is in SafeState it remains in this condition until the flags forcing this state are cleared (see Section 7.14) moving the device to Normal operation.

When the device is Normal operation it goes to SafeState every time an event forcing this state occurs, see Section 9.2.

If the device is NORMAL OPERATION, it goes to HW3PS if the following conditions are verified:

- DEFAULT = HIGH
- COMERRR bit status is set HIGH (HV side is not receiving any response from LV side, see Figure 10 and Table 62).

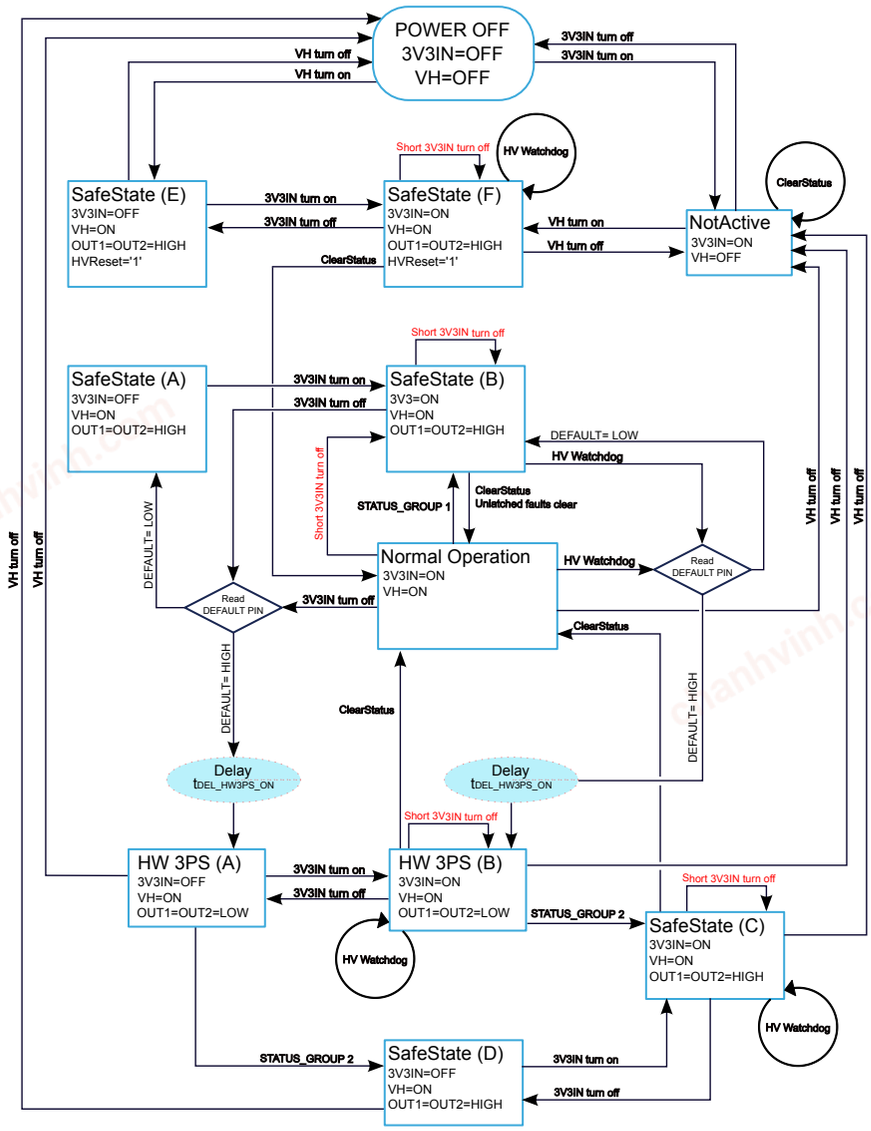
The device monitors the voltage on the pin DEFAULT and when the COMMERR is detected the device goes to HW3PS if DEFAULT is HIGH, otherwise the device goes to SafeState. Thus, the voltage of the DEFAULT pin must be stable when the event is detected. The outputs OUT1 and OUT2 are set LOW after a delay $t_{DEL_HW3PS_ON}$.

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When the device is in “HW3PS” state, including the delay time $t_{DEL_HW3PS_ON}$, if any protection mechanism of the group named STATUS_GROUP2 is activated the device moves immediately to SafeState.

A detailed description of the power-on/power-off sequence and the operation flowchart is reported in Figure 10.

Figure 10. Operation flowchart



Notes:

- The “3V3IN turn off” is recognized by the HV side through the expiration of the communication watchdog that occurs whenever the HV side is not able to communicate with the LV side for any reason. The “3V3IN turn off” and the “HV watchdog” are shown as different events in the flowchart only to highlight the behavior in case of intermittent operation of the 3V3IN supply.
- The “Short 3V3IN turn off” indicates a 3V3IN turn-off condition lasting less than the HV side watchdog timer
- The STATUS_GROUP1 includes the following fault conditions: UVLOH, UVLOL, OVLOH, OVLOL, DESAT, TSD, SENSE, REGERRL, REGERRR
- The STATUS_GROUP2 includes the following fault conditions: UVLOH, OVLOH, DESAT, TSD, SENSE, REGERRR
- If any protection mechanism contained inside STATUS_GROUP2 is activated during the $t_{DEL_HW3PS_ON}$ delay counting, it is interrupted and the device moves immediately to SafeState.

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- The ASC pin overrides the SafeState (see Section 7.15 for a detailed description and conditions)
- The HW3PS state overrides the ASC command
- The integrated flyback controller is operative if 3V3IN is supplied. If 3V3IN is not supplied, VH must be fed by an external auxiliary supply.

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7 Functional description

The STGAP4AS is provided with several advanced protection and diagnostic features to ease the design of reliable and rugged systems. Some of them are allocated to the High Voltage side and assume an interaction with the Low Voltage side. In order to perform these features the device is equipped with isolated communication channels between LV and HV sides.

One channel is fully committed to the transmission of the PWM command from the LV side to the HV side and in Normal Operation allows the execution of the commutation of the outputs OUT1 and OUT2 according to the truth table reported in Section 7.1.

Another interface is used to exchange DATA between the two sides, in particular:

- SPI data (HV registers write and read)
- Diagnostic information (GATE and ASC bits, Diag1 and Diag2 transition due to events on HV)
- ADC data

The device is designed to perform these tasks as long as it stably remains within the recommended operating conditions reported in Table 4.

7.1 Inputs and outputs

The device is controlled through the following logic inputs:

- $\overline{SD}$: active low shutdown
- IN+: driver input
- IN-: driver input
- $\overline{CS}$: active low chip select (SPI)
- SDI: serial data input (SPI)
- CK: serial clock (SPI)

And the following logic outputs:

- SDO: serial logic output (SPI)
- $\overline{DIAG1}$: active low diagnostic signal 1 (open drain)
- $\overline{DIAG2}$: active low diagnostic signal 2 (open drain)

Table 10. Inputs truth table, ASC ='0' , OFFMODE = '0' (device NOT in "SafeState")

$\overline{SD}$	IN+	IN-	OUT1	OUT2	2LSO	External buffer (1)	External power switch state
0	X	X	HIGH	HIGH	LOW	N-ch ON	**OFF**
1	0	0	HIGH	HIGH	LOW	N-ch ON	**OFF**
1	0	1	HIGH	HIGH	LOW	N-ch ON	**OFF**
1	1	0	LOW	LOW	HiZ	P-ch ON	**ON**
1	1	1	HIGH	HIGH	LOW	N-ch ON	**OFF**

1. *P-channel connected to OUT1 and N-channel connected to OUT2.*

Table 11. Inputs truth table, ASC = '0', OFFMODE = '1' (device NOT in "SafeState")

$\overline{SD}$	IN+	IN-	OUT1	OUT2	2LSO	External buffer (1)	External power switch state
0	X	X	HIGH	HIGH	HiZ	N-ch ON	**OFF**
1	0	0	HIGH	HIGH	HiZ	N-ch ON	**OFF**
1	0	1	HIGH	HIGH	HiZ	N-ch ON	**OFF**
1	1	0	LOW	LOW	HiZ	P-ch ON	**ON**

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$\overline{SD}$	IN+	IN-	OUT1	OUT2	2LSO	External buffer (1)	External power switch state
1	1	1	HIGH	HIGH	HiZ	N-ch ON	**OFF**

1. *P-channel connected to OUT1 and N-channel connected to OUT2.*

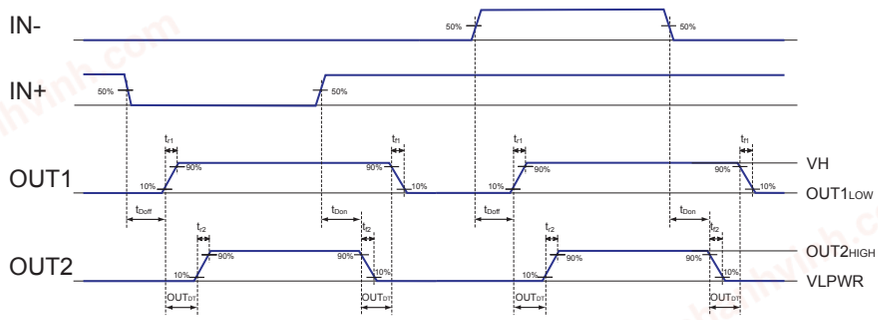
If ASC is used see Section 7.15 for details about the interaction with the logic inputs.

A programmable deglitch filter can be applied to the device inputs ($\overline{SD}$, IN+, IN-). Each input pulse, positive and negative, shorter than the programmed $t_{deglitch}$ value is neglected by the internal logic. The deglitch time can be programmed as listed in Table 5.

When the deglitch filter is disabled (INfilter = '00'), a minimum input pulse t_{INmin} is required to change the device output status. The minimum input pulse timing filters out both positive and negative pulses at the IN+, IN- and $\overline{SD}$ pins.

A deadtime (OUT_{DT}) is applied between OUT1 and OUT2 driver outputs signals to prevent possible cross-conduction in the external push-pull stage (see Figure 11).

Figure 11. Input to output timing diagram

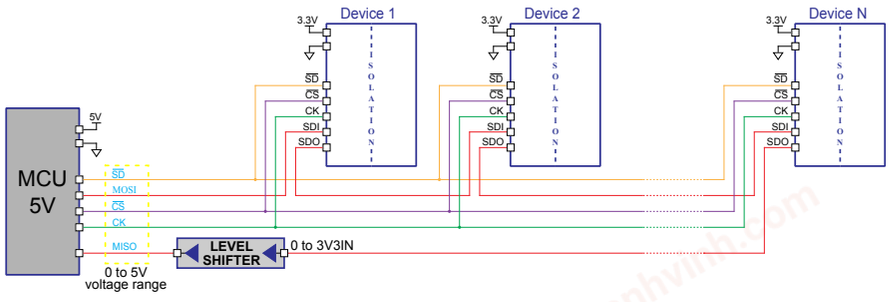


7.2 Logic I/O interface to 5V logic signals

The logic inputs of LV side ($\overline{SD}$, IN+, IN-, $\overline{CS}$, SDI, CK) are 5V tolerant that means that these pins can accept a recommended voltage up to 5.5V (see Table 4) and allow to interface the STGAP4S with devices that have nominal 5V output logic voltage, such as microcontroller units supplied with 5V. The STGAP4S logic inputs thresholds are referred to the 3V3IN supply voltage (see Section 4.2).

The SPI logic output SDO has a voltage range 0 to 3V3IN but it can be adapted to a 5V logic simply adding a level shifter between the driver and the MCU. Thus if a SPI daisy chain configuration is used only one level shifter is needed to make the STGAP4S SPI loop fully compatible with a 5V logic. A connection example is shown in Figure 12:

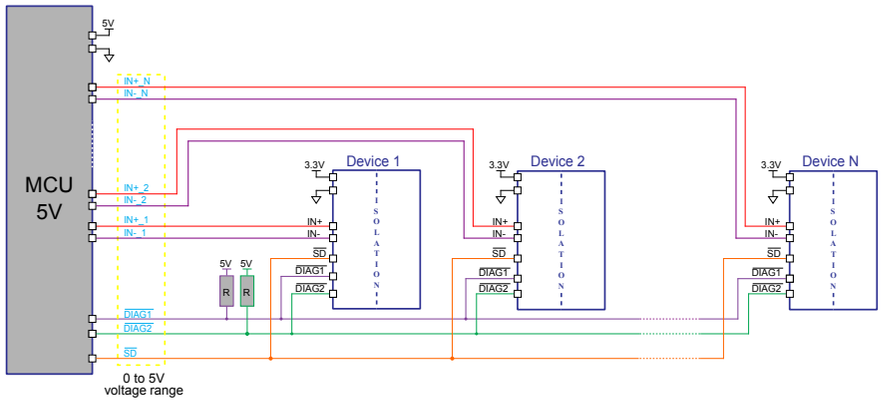
Figure 12. SPI daisy chain connection example with 5V logic



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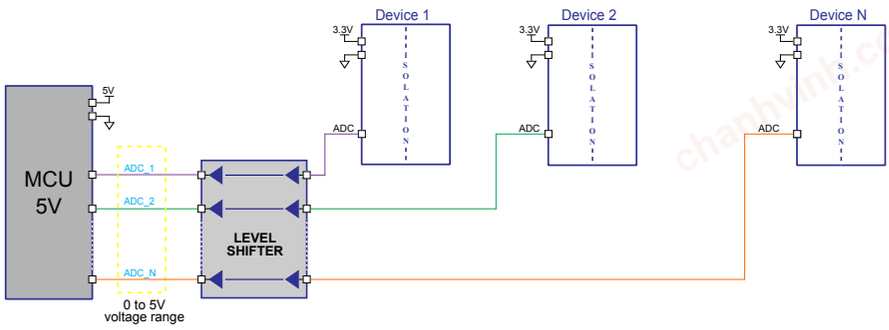
Also the open drain diagnostic outputs $\overline{DIAG1}$ and $\overline{DIAG2}$ are 5V tolerant, that means that these pins can be easily interfaced to a 5V logic using a pull-up resistor tied to the 5V supply as shown for example in Figure 13:

Figure 13. Diagnostic outputs connection example with 5V logic



Also the ADC output has a voltage range 0 to 3V3IN and, as reported for the SDO signal, it can be easily adapted to a 5V logic adding a level shifter between the device pin and the MCU as shown in Figure 14.

Figure 14. ADC outputs connection example with 5V logic

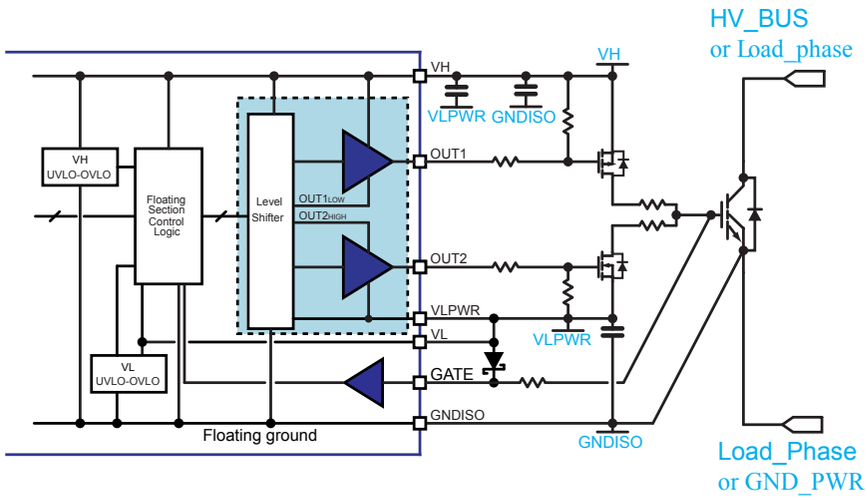


7.3 Outputs driving architecture

The output driving architecture is designed to allow the use of an external MOSFET push-pull stage giving high flexibility in terms of current capability dimensioning to drive the power IGBT/MOSFET stage. The 2 pre-driver outputs are characterized by current capability and output voltage swing specifically optimized for that topology. The OUT1 output is designed to drive the gate of the p-channel of the external MOSFET push-pull while OUT2 is designed to drive the gate of the complementary n-channel. The driver is provided with a dedicated VLPWR pin to connect the source of the N-channel MOSFET. The VL and the VLPWR pins must be connected together close to the device. The simplified schematic is shown in Figure 15.

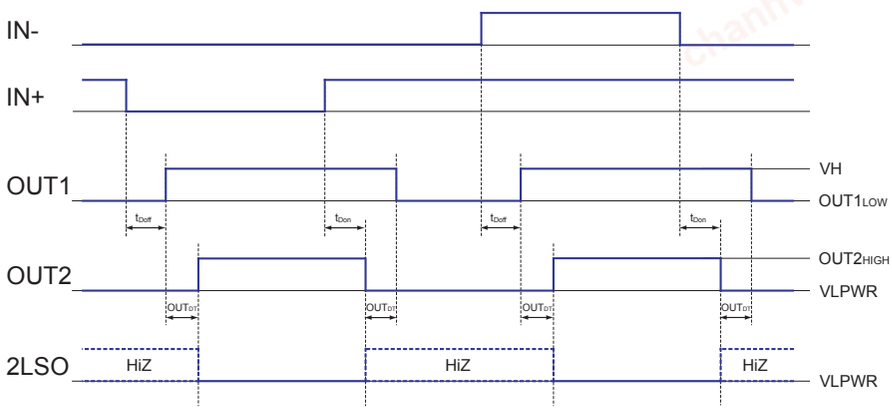
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Figure 15. **Output driving architecture**



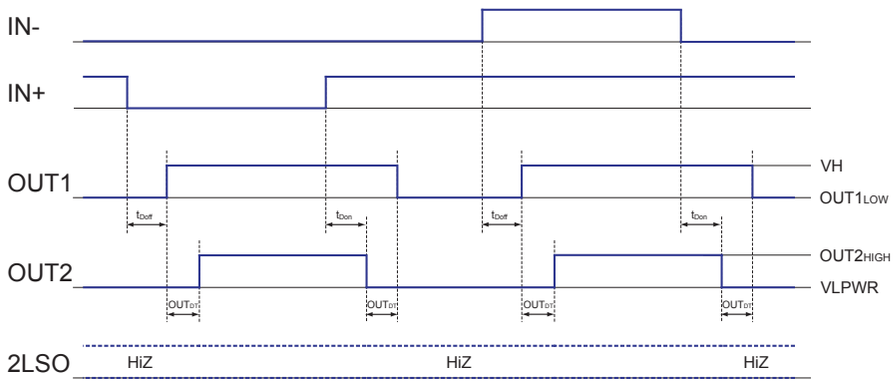
The device offers the possibility to drive the internal SOFTOFF MOSFET, connected to the 2LSO pin, at the same time of OUT2, as shown in Figure 16, allowing the turn-on of the internal SOFTOFF MOSFET at every switching cycle together with the n-channel of the external push-pull. This feature is disabled by default at the HV side power-on, as shown in Figure 17, but can be enabled by configuring OFFMODE=0 in CFG7, see Table 54. This operation mode is inhibited during and after the intervention of the “Soft turn-off” protection function, see Section 7.12 for details.

Figure 16. **OUT1 and OUT2 timing diagram (OFFMODE = ‘0’)**



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Figure 17. **OUT1 and OUT2 timing diagram (OFFMODE = '1')**



7.4 Gate voltage monitor (GATE PIN)

The device is equipped with a comparator dedicated to the monitoring of the gate voltage of the external power IGBT/MOSFET.

The comparator monitors the voltage of the GATE pin and reports the status in the GATE_LEVEL_LV bit contained in the STATUS4 register. Specifically, the comparator has a hysteresis (V_{GATEth_ON} - V_{GATEth_OFF}) and the GATE_LEVEL_LV bit is set HIGH when the voltage on the GATE pin is rising and exceeds the V_{GATEth_ON} threshold, while the GATE_LEVEL_LV bit is set LOW when the voltage on the GATE pin is falling and goes below the V_{GATEth_OFF} threshold. To use this function the GATE pin must be connected to the gate of the external power IGBT/MOSFET through a resistor (see Figure 15).

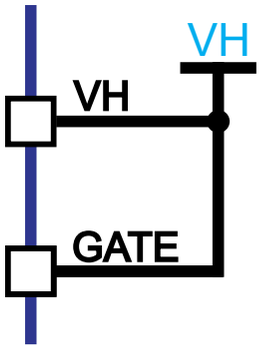
The GATE_LEVEL_LV bit status can be reported to the diagnostic pins $\overline{DIAG1}$ and $\overline{DIAG2}$ by properly configuring the dedicated registers (DIAG1CFGA, DIAG1CFGB, DIAG2CFGA and DIAG2CFGB) (see Section 9.2.14).

The monitoring of the gate of the external power IGBT/MOSFET, connecting the GATE pin to the gate of the external power through a resistor, is mandatory if the Miller clamp function is used (see Section 7.13).

If neither the Miller clamp function nor the reporting of the GATE voltage to DIAGx pins are used, to allow the correct switching operation, the GATE pin must be connected according to one of the following ways:

- through a resistor to the gate of the external power IGBT/MOSFET, as already mentioned (see Figure 15)
- shorted to VH power supply pin (see Figure 18)

Figure 18. **GATE PIN connection to VH**



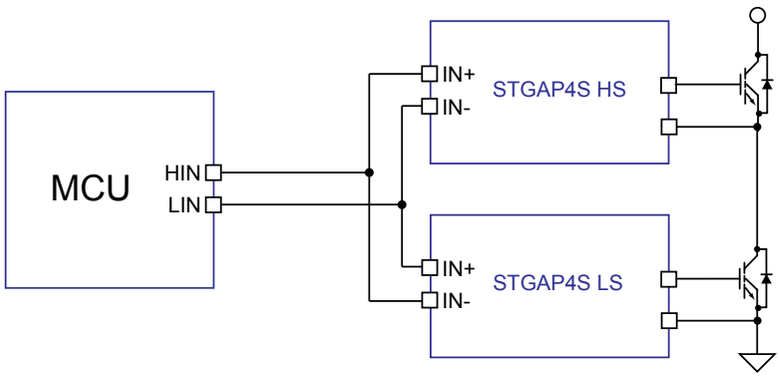
7.5 Deadtime and interlocking

When single gate drivers are used in half-bridge configuration, they usually do not allow preventing cross conduction in case of wrong input signals coming from the controller device. Indeed, each driver does not have the possibility to know the status of the input signal of the other companion driver in the same leg. Thanks to the availability of two input pins with opposite polarity the STGAP4S allows implementing a hardware interlocking that prevents cross conduction even in case of wrong input signals generated by the control unit.

This functionality can be achieved by implementing the connection shown in Figure 19.

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Figure 19. **HW cross conduction prevention in half-bridge configuration with two single gate drivers**



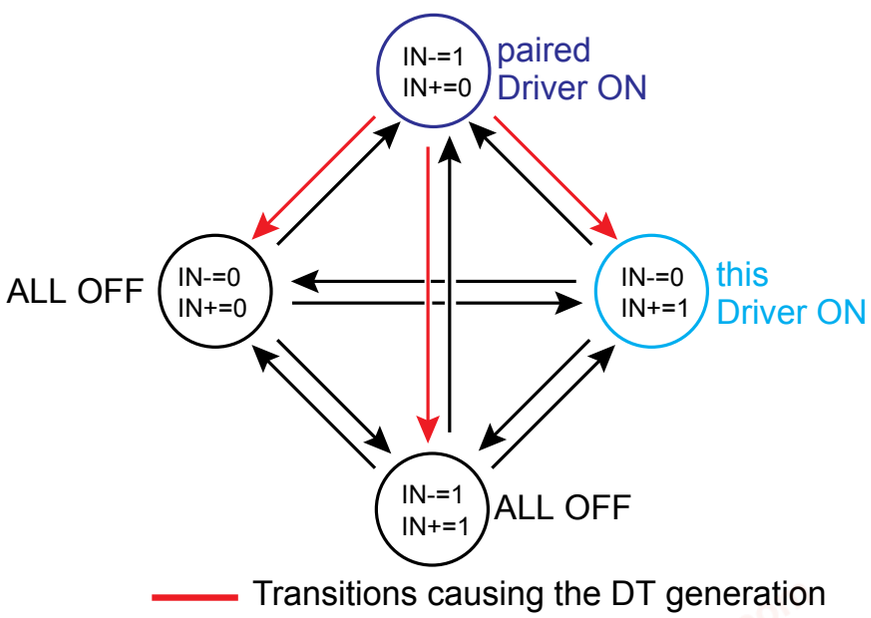
When such configuration is used, it is also possible to enable the STGAP4S programmable deadtime, which guarantees that at least DT time passes between the turn-off of one driver's output and the turn-on of the other driver. The deadtime value DT can be programmed through the SPI interface as shown in Table 5.

If the deadtime feature is enabled, a counter is started when the input status changes from < IN- = '1' and IN+ = '0' > to a different combination, which means that the other driver in the same leg is at the beginning of a turn-off (refer to Figure 20).

Once the counter is started it keeps counting regardless of any input variation until a DT time has passed, and during this time the driver prevents the turn-on of its output even if the controller tries to force the turn-on (inputs set to < IN- = '0' and IN+ = '1' >).

Once the programmed DT counter is expired, the driver immediately turns the output on as soon as a turn-on command is present at the input pins, and no extra delay is added.

Figure 20. **Transitions causing DT generation**



Some examples of the device behavior when the deadtime feature is enabled are shown from Figure 21 to Figure 24.

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Figure 21. **Synchronous control signal edges**

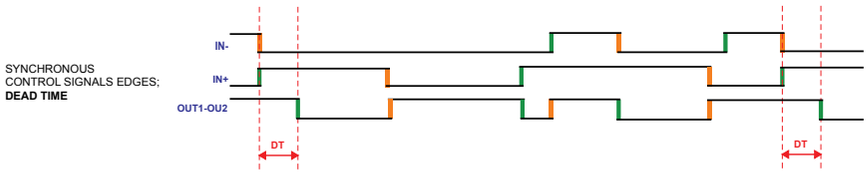


Figure 22. **Control edges signal overlapped, example 1**

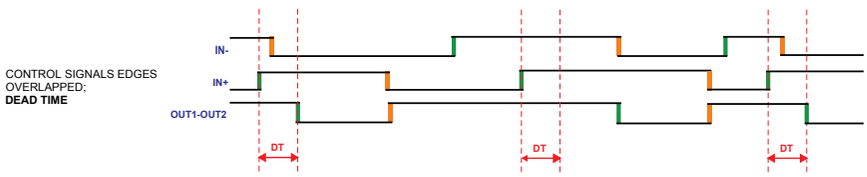


Figure 23. **Control edges signal overlapped, example 2**

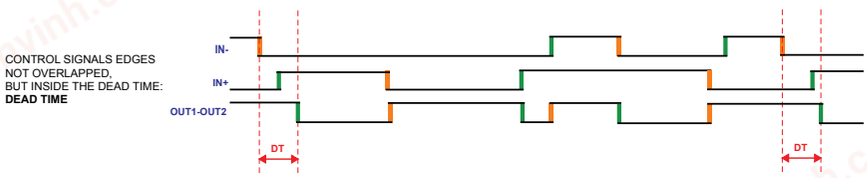


Figure 24. **Control edges signal not overlapped and outside DT (direct control)**

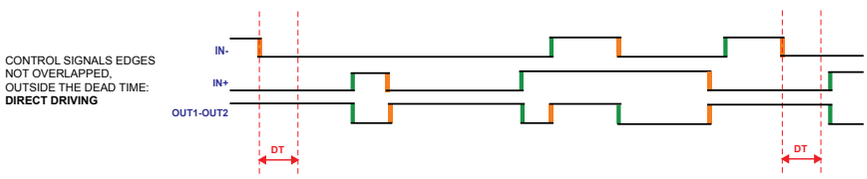
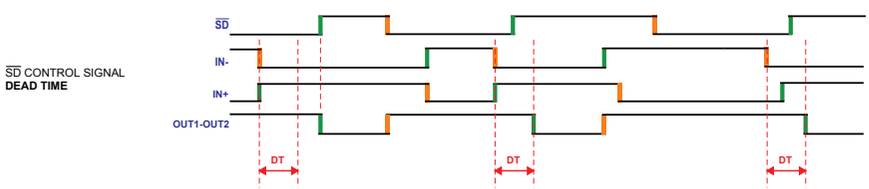


Figure 25. **SD signal interaction**



When the deadtime function is enabled the STGAP4S reports a “deadtime violation” fault in case the control unit tries to turn on any of the drivers in one leg during the counting of the programmed DT time. If such event occurs, the DT_ERR flag is set high and latched.

7.6 Power supply UVLO and OVLO

A programmable undervoltage protection is available on both VH and VL supply pins.

The turn-on thresholds VH_{on} and VL_{on} can be programmed through the SPI writing the CFG3 register and a fixed hysteresis sets the turn-off threshold, respectively VH_{hyst} for the VH supply and VL_{hyst} for the VL supply.

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Both the UVLO protections can be independently disabled by setting the proper value of VHONth and VLONth in the CFG3 register.

When the VH voltage goes below the VH_{off} threshold the device goes in “SafeState” and the UVLOH flag in the STATUS1 register is set high. If the UVLOlatch bit in the CFG3 register is set low (default configuration) the UVLOH status flag is set low when the VH voltage returns above the VH_{on} threshold and the device returns to normal operation. Otherwise, if the UVLOlatch bit in the CFG3 register is set high, the UVLOH flag is latched and the device remains in “SafeState” until VH voltage is higher than the VH_{on} and the UVLOH status flag is reset by the control unit.

When the VL voltage goes over the VL_{off} threshold the device goes in “SafeState” and the UVLOL flag in STATUS1 register is set high. If the UVLOlatch bit in the CFG3 register is set low (default configuration) the UVLOL status flag is set low when VL voltage returns below the VL_{on} threshold and the device returns to normal operation. Otherwise, if the UVLOlatch bit in the CFG3 register is set high, the UVLOL flag is latched and the device remains in “SafeState” until the VL voltage is lower than the VL_{on} threshold and the flag is reset by the control unit.

An overvoltage protection is available on both VH and VL supply pins.

For the VH supply the turn-off threshold $OVVH_{off}$ can be programmed through the SPI writing the CFG3 register and the fixed hysteresis $OVVH_{hyst}$ sets the respective turn-on threshold.

When the VH voltage goes over the $OVVH_{off}$ threshold, the device goes in “SafeState” and the OVLOH flag in the STATUS1 register is set high. The OVLOH flag is latched and the device remains in “SafeState” until VH voltage returns below the $OVVH_{on}$ threshold and the flag is reset by the control unit.

For the VL supply voltage the turn-off threshold $OVVL_{off}$ is fixed and the hysteresis $OVVL_{hyst}$ sets the respective turn-on threshold.

When the VL voltage goes below the $OVVL_{off}$ threshold the device goes in “SafeState” and the OVLOL flag in the STATUS1 register is set high. The OVLOL flag is latched and the device remains in “SafeState” until VL voltage returns above the $OVVL_{off}$ threshold and the flag is reset by the control unit.

The undervoltage protection is available also on the VCC supply and on the 3V3IN supply.

For the VCC voltage the UVLO turn-on threshold VCC_{on} is fixed and the hysteresis VCC_{hys} sets the respective VCC_{off} turn-off threshold.

When the VCC voltage goes below the VCC_{off} threshold the UVLO_VCC flag in the STATUS3 register is set high. The UVLO_VCC status flag is set low when the VCC voltage returns above the VCC_{on} threshold. When the UVLO VCC protection is triggered the internal flyback controller stops switching. The controller restarts the normal operation when the UVLO VCC condition is no longer present, without the need of any external intervention.

For the 3V3IN voltage the UVLO turn-on threshold $UVLO3V3IN_{ON}$ is fixed and the hysteresis $UVLO3V3IN_{hys}$ sets the respective $UVLO3V3IN_{OFF}$ turn-off threshold. The protection is enabled by default at the device power-on but it can be disabled setting high the bit UVLO3V3IN_EN in the configuration register CFG1. The disabling of the UVLO3V3IN has no effect on the flyback controller section that is always stopped in case of UVLO condition on 3V3IN.

See Section 7.14 for indication on how the fault flags can be released.

7.7 Thermal warning and shutdown protection

The device provides a thermal warning and a thermal shutdown protection.

When the junction temperature reaches the T_{WARN} temperature threshold the TWN flag in the STATUS2 register is set high. The TWN flag is set low as soon as the junction temperature is lower than ‘T_{WARN}-T_{hys}’.

When the junction temperature reaches the T_{SDN} temperature threshold, the device goes in “SafeState” and the TSD flag in the STATUS1 register is set high. The device operation is restored and the TSD flag is set low as soon as the junction temperature is lower than ‘T_{SDN} - T_{hys}’.

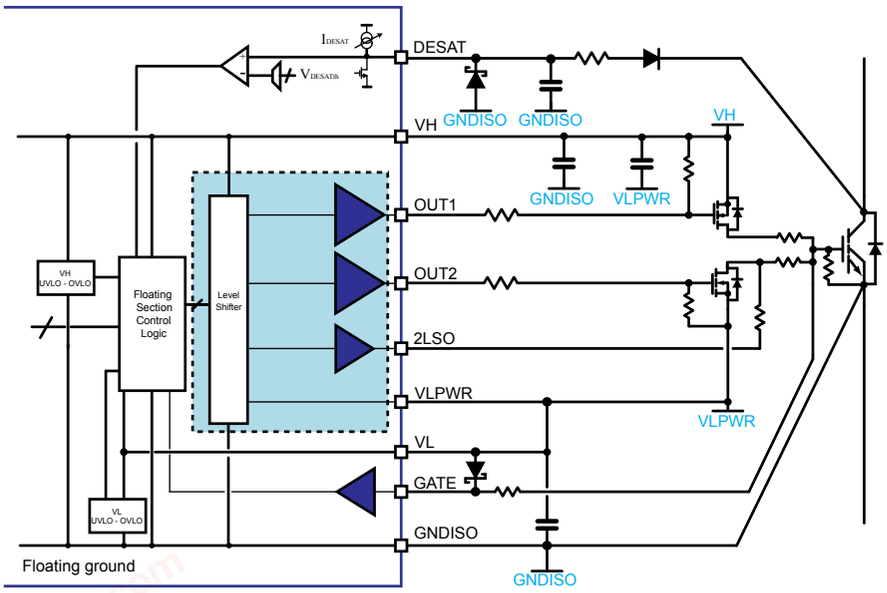
The junction temperature can also be measured using the ADC and setting its input to “Internal IC temperature measurement” (ADC_INPUT=1). Further details are reported in Section 7.16.7.

7.8 Desaturation protection

This feature allows to implement an overload protection for the external power IGBT/MOSFET. The DESAT pin monitors the V_{CE}/V_{DS} voltage of the IGBT/MOSFET when it is in on-state and if the protection threshold is reached the IGBT/MOSFET is turned off.

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Figure 26. **Example of desaturation protection connection**



When the IGBT/MOSFET is off (OUT1 = OUT2 = HIGH) the DESAT pin is kept low internally and the external blanking capacitor connected to the DESAT pin is discharged. The internal current generator is fully switched off and the switch between DESAT and GNDISO pins is turned on.

When the IGBT/MOSFET is turned on (OUT1 = OUT2 = LOW) after a fixed blanking time t_{FBLK} the switch between DESAT and GNDISO pins is turned off and the internal programmable current generator (I_{DESAT}) starts charging the external blanking capacitor.

When a desaturation event occurs the V_{CE}/V_{DS} voltage increases and if the voltage sensed at the DESAT pin reaches the desaturation threshold $V_{DESATth}$, the internal DESAT comparator is triggered. After the time t_{DESAT} the output is turned off (OUT1 = OUT2 = HIGH). The device goes to “SafeState” and the DESAT_OC flag in STATUS1 register is set high approximately 200 ns later.

The DESAT comparator is not active when the external IGBT/MOSFET is off or after a desaturation detection (see Figure 27 and Figure 28).

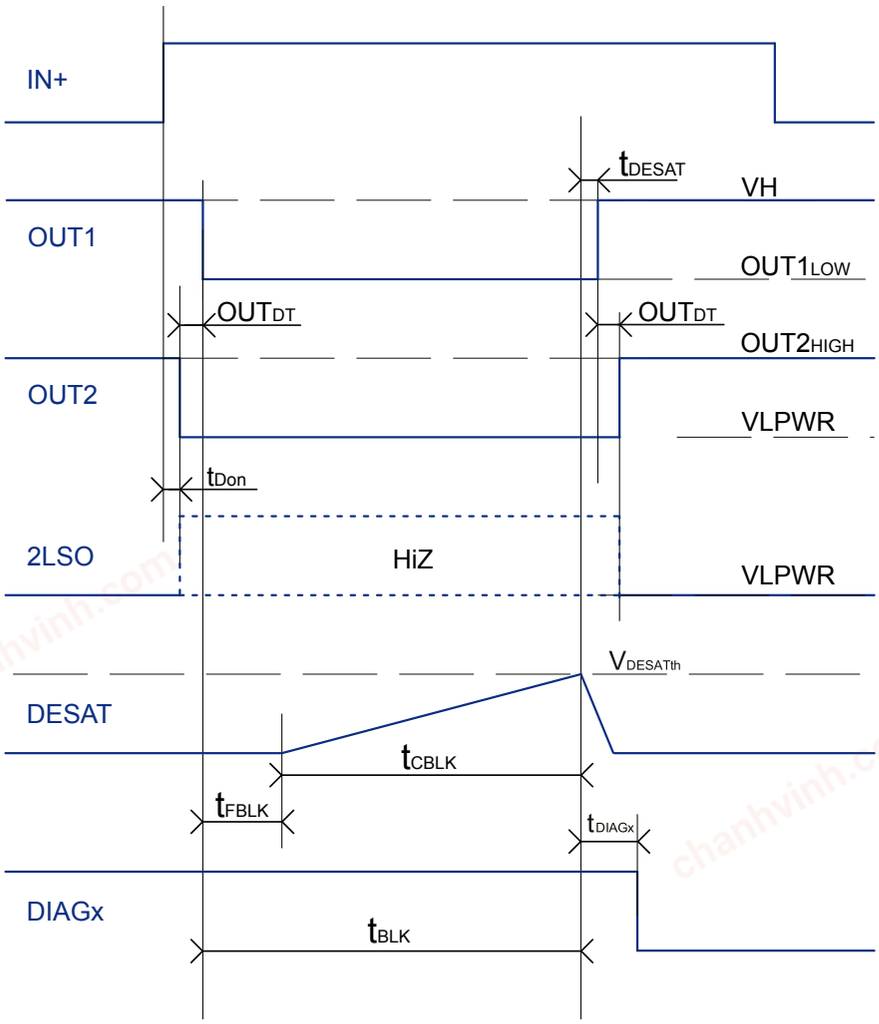
A deglitch filter is applied to the DESAT pin; indeed each pulse exceeding the $V_{DESATth}$ threshold for a time shorter than $t_{DESfilter}$ does not trigger the protection.

The DESAT protection can be enabled/disabled by properly setting the DESAT_EN bit in the CFG2 register. The $V_{DESATth}$ threshold and the I_{DESAT} blanking current are programmable through the SPI interface (refer to Section 9.2).

The external power IGBT/MOSFET turning-off sequence is performed according to SAFE_OFF and SOFT_2LTO bit values (see Section 7.12).

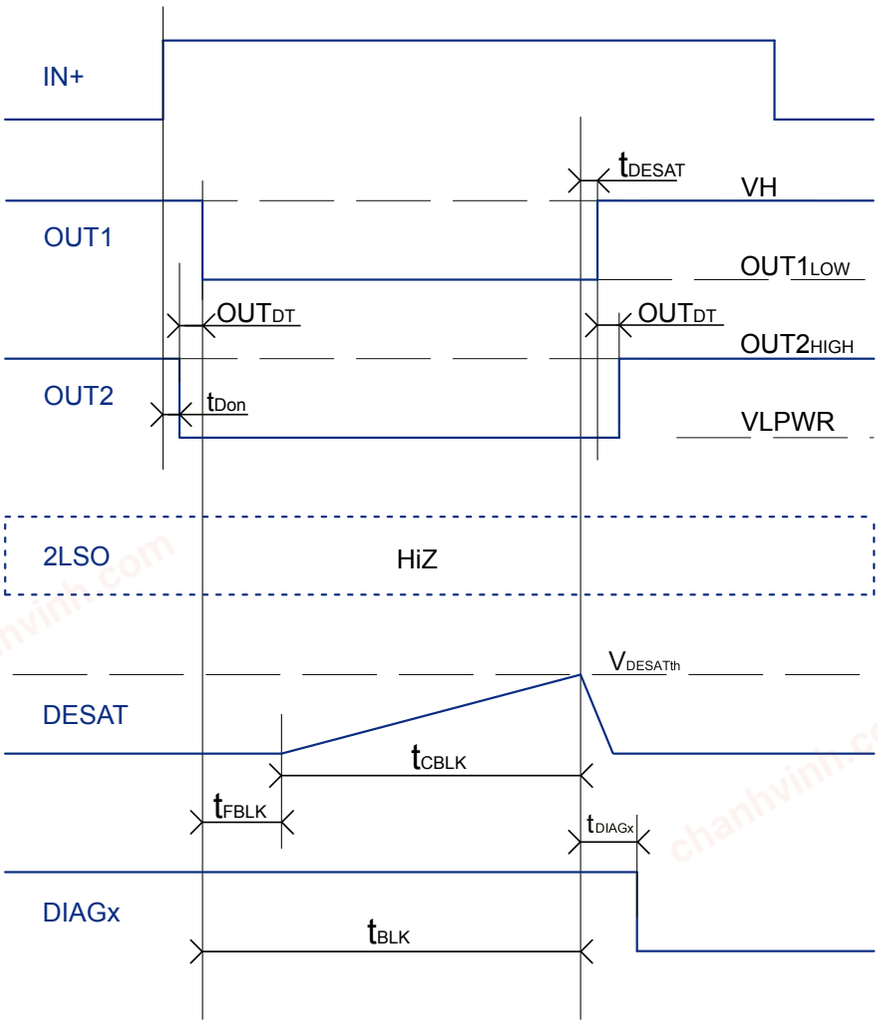
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Figure 27. **DESAT protection timing diagram (SAFE_OFF = '0', OFFMODE = '0')**



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Figure 28. **DESAT protection timing diagram (SAFE_OFF = '0', OFFMODE = '1')**



7.9 SENSE overcurrent protection

This function is suitable in applications in which it is possible to measure the load current through the use of a shunt resistor, or when IGBTs or MOSFETs with current sense pin are used. The load current (or a fraction of it in case senseFETs are used) is converted to voltage by an external shunt resistor and is fed to the SENSE input pin.

If an overcurrent event occurs the voltage at the SENSE pin increases and when the threshold $V_{SENSEth}$ is reached, the SENSE comparator output is set. The output is turned off (OUT1 = OUT2 = HIGH) after a time t_{SENSE}. The device goes to "SafeState" and the SENSE_OC flag is set high approximately 200 ns later.

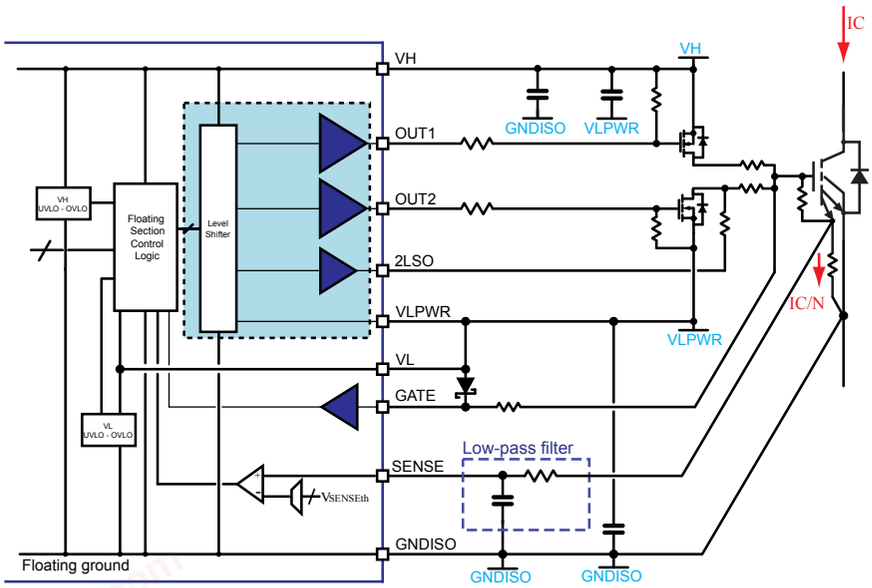
The SENSE protection can be enabled/disabled by properly setting the SENSE_EN bit in the CFG2 register.

The $V_{SENSEth}$ threshold is programmable through the SPI interface (refer to Section 9.2).

The external power IGBT/MOSFET turning-off sequence is performed according to SAFE_OFF and SOFT_2LTO bit values (see Section 7.12).

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Figure 29. **Example of SENSE overcurrent protection connection**



7.10 Analog measurement function

The analog measurement function allows to acquire and convert into a digital representation an analog signal coming from the HV side, for instance:

- Forward voltage of diode integrated into power modules, for temperature monitoring
- Voltage drop across NTC inside power modules, for temperature monitoring
- High voltage DC bus or phase voltage sensing
- Internal IC temperature measurement

This function is realized through an acquisition system which includes, on the HV side, a pre-conditioning block followed by an ADC. The main characteristics are:

- ADC 8 bit resolution
- Fast conversion time
- Fixed conversion period t_{PER_CONV}
- Programmable input range

The analog measurement function is enabled by setting high the ADC_EN bit in the CFG7 register.

The ADC input range can be programmed through ADC_LOWth and ADC_HIGHth parameters in the CFG7 register. This allows to adapt the ADC scale to the dynamic range of the input signal. The selected input range is divided in 256 uniform voltage levels.

The ADC_INPUT bit in CFG4 defines the ADC input source, specifically:

- ADC_INPUT = ‘0’: Differential voltage between ADCP and ADCN
- ADC_INPUT = ‘1’: Internal IC temperature measurement

The ADCN pin must be connected to GNDISO (with a short path close to the device) and it is the ground reference for the external voltage to be measured. The ADCP pin is the input pin for the positive voltage to be measured.

The characteristic of the internal temperature sensor is approximately:

$$V_{TEMP} = -0.00366 * T_{INTERNAL} + 1.5V \quad (6)$$

where:

- V_{TEMP} is the internal sensor voltage applied to the input of the ADC (when ADC_INPUT = ‘1’)
- $T_{INTERNAL}$ is the absolute temperature of the internal sensor expressed in °C

The ADC input range must be programmed according to the voltage range to be converted also when the internal temperature sensor is selected.

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A programmable current source is available on the ADCP pin allowing the feeding of external sensors without adding external components, for instance when a NTC or a diode is used to measure the temperature of a power module. The ADC current source can be programmed trough the ADC_CScur parameters in CFG4 register. The disable option is available.

The block diagram of the analog measurement architecture is shown in Figure 30 and some connection examples are reported in Figure 31.

Figure 30. ADC block diagram

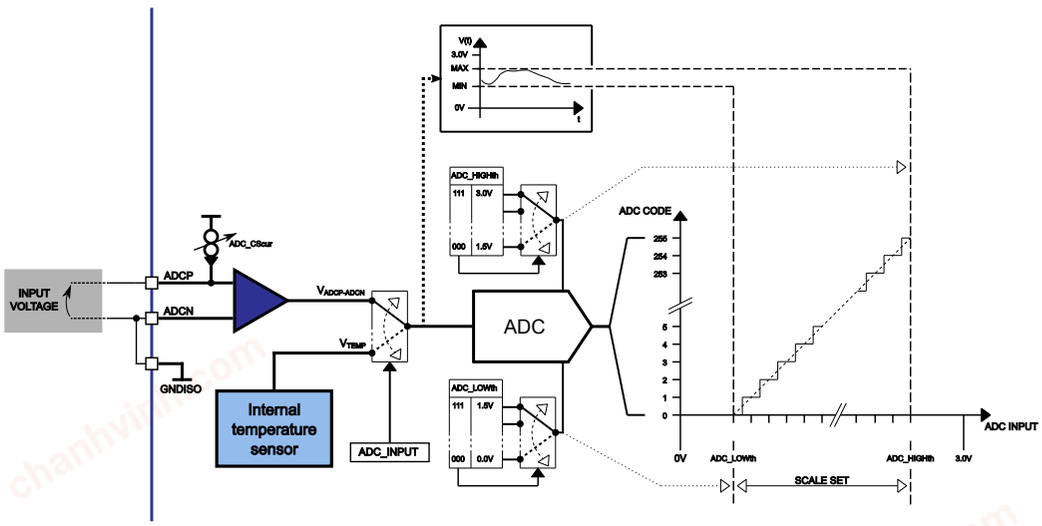
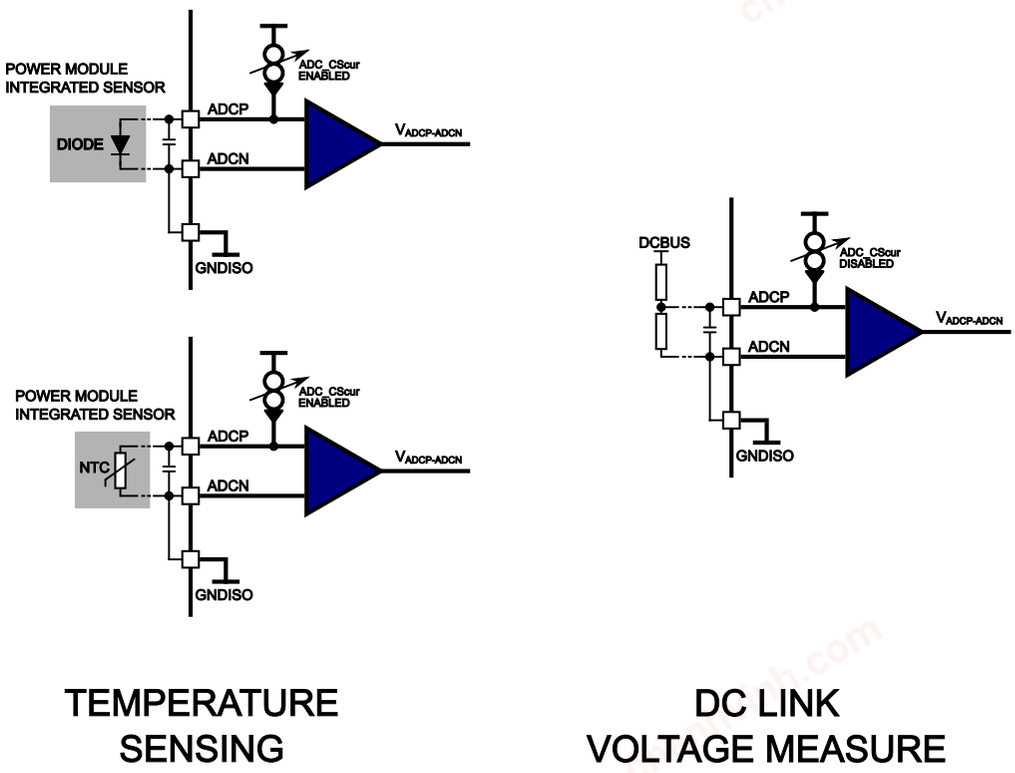


Figure 31. ADC connection example



The ADC output is available in two different ways:

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1. The ADC output information is stored in a dedicated status register (STATUS5), whose content can be read through the SPI interface
2. A PWM signal on the ADC pin, whose duty cycle is modulated by the ADC output code. This signal duty cycle is proportional to the ADC sampled value and varies between $DC3_{ADC}$ and $DC1_{ADC}$. The PWM on ADC output is disabled if ADC_PWM_EN is set low (default configuration).

DATA STORED IN STATUS5

If the ADC_EN bit in CFG7 is set low, that is ADC disabled, the value in the STATUS5 register is 0xFFh.

If the ADC_EN bit in CFG7 is set high, the value in the STATUS5 register is the data converted by the ADC.

If for any reason the value in STATUS5 is not updated for more than approximately 500 µs the value in STATUS5 is set to 0xFFh until a new updated value is stored.

PWM SIGNAL ON PIN ADC:

If the bit ADC_PWM_EN in CFG1 is set low the signal on pin ADC is kept low.

If the bit ADC_PWM_EN in CFG1 is high (PWM on ADC pin enabled) and the ADC_EN bit in CFG7 is high (ADC enabled) the device generates a PWM signal on the pin ADC with nominal frequency 10 kHz and duty cycle proportional to the data value stored in the STATUS5 register by the following equation:

$$Duty\ cycle = DC3_{ADC} + \left(DC1_{ADC} - DC3_{ADC}\right) * \frac{(value\ in\ STATUS5)}{(full\ scale\ value: 0xFFh)} \quad (7)$$

That means that:

- the minimum duty cycle is $DC3_{ADC}$ and matched to STATUS5=0x00h
- the maximum duty cycle is $DC1_{ADC}$ and matched to STATUS5=0xFFh

The duty cycle is updated every time a new conversion is stored in the STATUS5 register.

If for any reason the value in STATUS5 is not updated for more than approximately 500 us, the signal on pin ADC is kept high (duty cycle=100%) until a new updated value is stored. When a new updated value is stored in STATUS5, the duty cycle of the PWM signal on pin ADC is restored at the related consistent value.

Consistently, if the bit ADC_PWM_EN in CFG1 is set high (PWM on ADC pin enabled) but the ADC_EN bit in CFG7 is set low (ADC disabled) the signal on pin ADC is kept high.

7.11 V_{CE} active clamping protection

This protection is used to actively clamp the overvoltage spikes on the drain/collector of the external MOSFET/IGBT during the turn-off.

The feedback of the drain/collector voltage to the VCECLAMP pin can be done via an element with avalanche characteristic such as a TVS. If the drain/collector voltage exceeds the breakdown voltage of the TVS, the $VCECLAMP_{th}$ threshold voltage is reached and the device actively slows down the turn-off of the power switch to keep a safe condition.

At the turn-off of the external MOSFET/IGBT (OUT1/OUT2 rising) a timer lasting t_{COUNT_ACTIVE} is activated and during this observation time the VCECLAMP function is enabled and the protection can be triggered. If at the end of this timer no VCECLAMP events are detected, the VCECLAMP function is disabled up to the next turn-off event. This feature avoids spurious triggering of VCECLAMP far from the turn-off event.

If during the observation time t_{COUNT_ACTIVE} the protection is triggered, because the voltage on VCECLAMP pin exceeds the $VCECLAMP_{th}$ threshold, a new timer $t_{VCECLoff}$ is started. As soon as this timer is activated, the timer t_{COUNT_ACTIVE} no longer has any effect and the protection is kept enabled for a time $t_{VCECLoff}$ starting from the first triggered event of VCECLAMP. During the time $t_{VCECLoff}$ the protection can be triggered multiple times but when this timer expires the VCECLAMP function is disabled up to the next turn-off event.

During the time $t_{VCECLoff}$ everytime the voltage on the VCECLAMP pin exceeds the $VCECLAMP_{th}$ threshold OUT2 is set LOW and the turn-off of the external power MOSFET/IGBT is performed through the internal SOFTOFF N-channel MOSFET connected to the 2LSO pin. When the voltage on VCECLAMP is below the $VCECLAMP_{th}$ threshold OUT2 is set HIGH and the SOFTOFF N-channel MOSFET connected to the 2LSO pin is turned off. To use this protection the 2LSO pin must be connected to the external power MOSFET/IGBT gate through a resistor.

By setting the OFFMODE bit the internal SOFTOFF MOSFET can either be activated in combination with OUT2 or only when the protection is triggered. If OFFMODE=0 the SOFTOFF MOSFET is turned-on when OUT2 is HIGH and thus it is already on when a VCECLAMP event is triggered. If OFFMODE=1 the SOFTOFF MOSFET is turned on only when the VCECLAMP event is triggered.

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Figure 32. **VCECLAMP activation (OFFMODE = '0')**

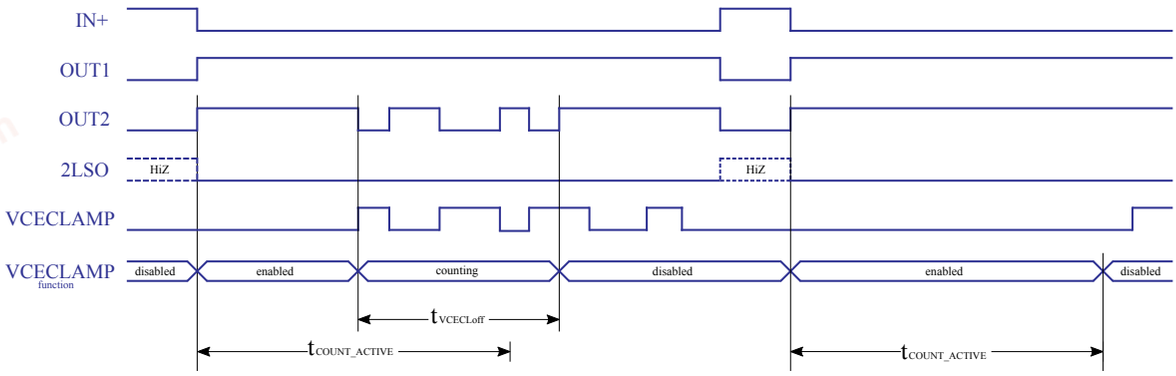
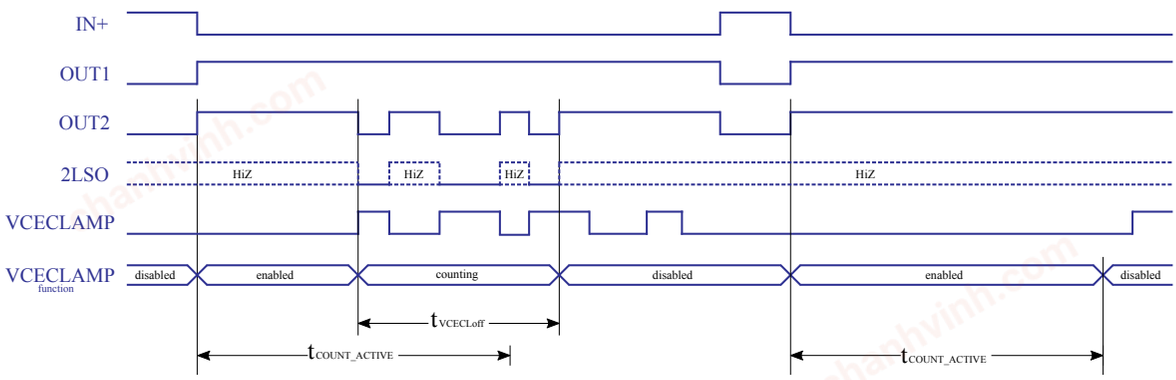


Figure 33. **VCECLAMP activation (OFFMODE = '1')**



When the external power MOSFET/IGBT is on the VCECLAMP pin is masked and has no effect on the driver's outputs status .

If the SOFTOFF function is enabled (SAFE_OFF = 1) for the use in combination with DESAT or SENSE functions (SAFE_OFF = 1), the VCECLAMP is internally disabled when a desaturation or overcurrent event occurs. Thus, if SAFE_OFF = 1 and a desaturation or overcurrent event occurs the VCECLAMP is not performed. The function is again enabled at the next turn-off event of the external MOSFET/IGBT.

Table 12. **VCECLAMP in case of DESAT/SENSE event**

SAFE_OFF	VCECLAMP
0	Enabled
1	Disabled in case of DESAT/SENSE event

To correctly perform the VCE active clamping protection the GATE pin must be connected according to one of the following ways:

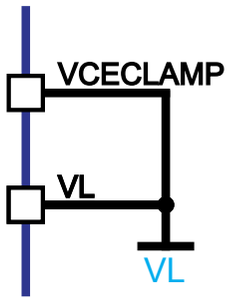
- through a resistor to the gate of the external power IGBT/MOSFET, if the monitoring of the gate or the Miller Clamp functions are used
- shorted to VH power supply pin, if neither the monitoring of the gate nor the Miller Clamp functions are used

See Section 7.4 for details.

If the V_{CE} active clamping protection is not used the VCECLAMP pin must be connected to VL as reported in Figure 34.

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Figure 34. **VCECLAMP disabling**



7.12 Soft turn-off

The Soft turn-off (SOFTOFF) function can be used to slow down the turn-off of the external MOSFET/IGBT in case of turn-off due to an overcurrent condition, thus reducing the overvoltage spike on the drain/collector.

The type of turn-off performed when a DESAT or SENSE event occurs is set configuring the SAFE_OFF and SOFT_2LTO bits. As reported in Table 13, two possible turn-off modes can be selected, the standard described in Section 7.8 and Section 7.9 or the SOFTOFF described below:

Table 13. **Turn-off functions at DESAT or SENSE triggering**

SAFE_OFF	SOFT_2LTO	Turn-off function
0	**0**	Standard
1	**0**	SOFTOFF

The Soft turn-off function (SOFTOFF) switches off the external power MOSFET/IGBT using the internal N-channel MOSFET connected to the 2LSO pin. To use this protection the 2LSO pin must be connected to the external power MOSFET/IGBT gate through a resistor. If SAFE_OFF='1' and SOFT_2LTO='0', when a DESAT or SENSE overcurrent is triggered, OUT1 is immediately set HIGH and after a time OUT_{DT} the SOFTOFF internal MOSFET is turned on, while OUT2 is kept LOW. In this way, selecting the proper resistor value of the Soft turn-off path, the turn-off of the external power MOSFET/IGBT can be slower compared to a standard turn-off sequence performed turning on the n-channel of the push-pull by setting HIGH OUT2. Afterwards, to complete the external power MOSFET/IGBT turn-off, the SOFTOFF internal MOSFET is turned off and OUT2 is set HIGH, activating the n-channel of the external push-pull, at the occurrence of one of the following events:

- the expiration of the time $t_{2LTO_SOFTtime}$
- the voltage on the GATE pin has reached the V_{GATEth_OFF} voltage threshold (before the expiration of the time $t_{2LTO_SOFTtime}$)

To correctly perform the Soft turn-off function the GATE pin must be connected according to one of the following ways:

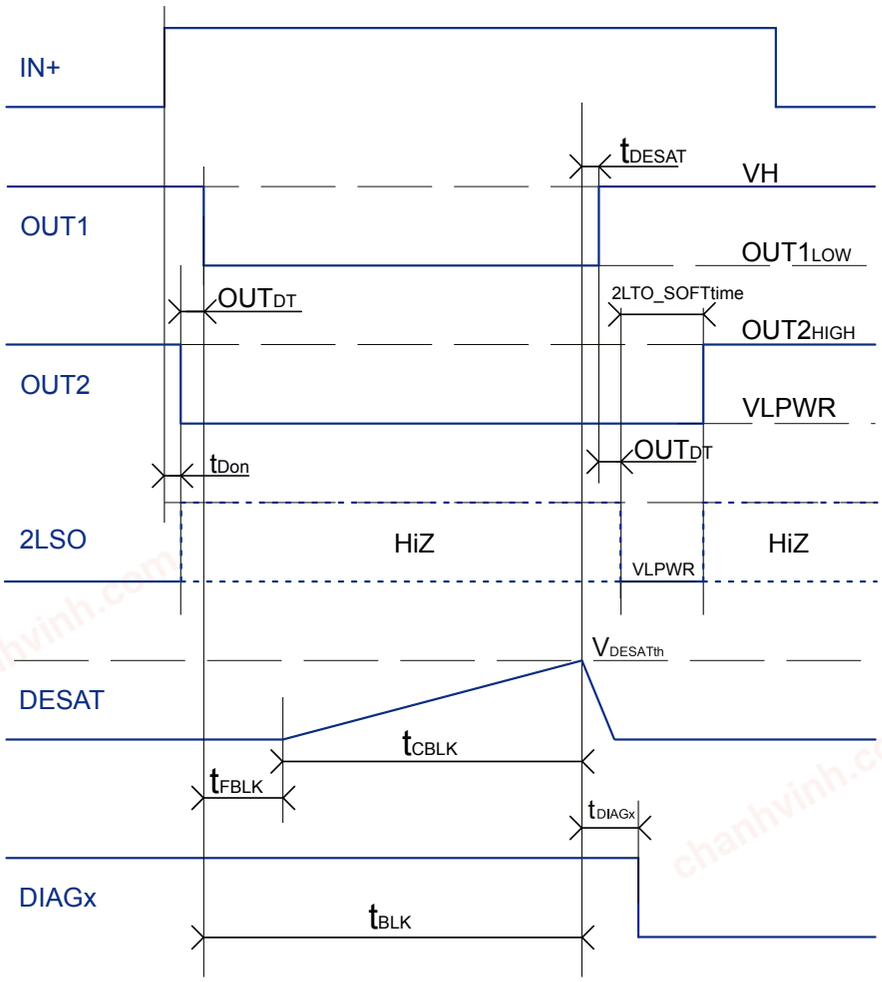
- through a resistor to the gate of the external power IGBT/MOSFET, if the monitoring of the gate or the Miller Clamp functions are used
- shorted to VH power supply pin, if neither the monitoring of the gate nor the Miller Clamp functions are used

See Section 7.4 for details.

The protection timing diagram is shown in Figure 35 and Figure 36 for the DESAT protection but, in principle, for the SENSE protection is analogous.

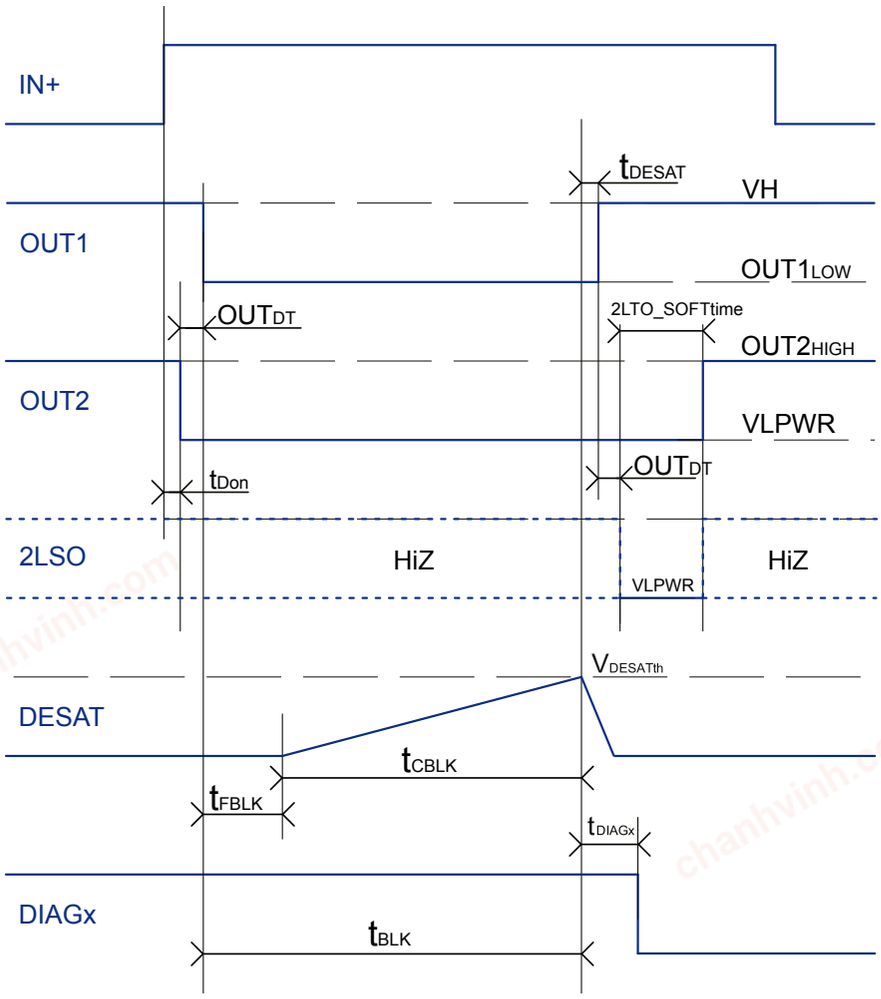
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Figure 35. **DESAT protection timing diagram (SAFE_OFF = '1' - SOFT_2LTO = '0' - OFFMODE = '0')**



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Figure 36. **DESAT protection timing diagram (SAFE_OFF = '1' - SOFT_2LTO = '0' - OFFMODE = '1')**



7.13 Miller clamp function

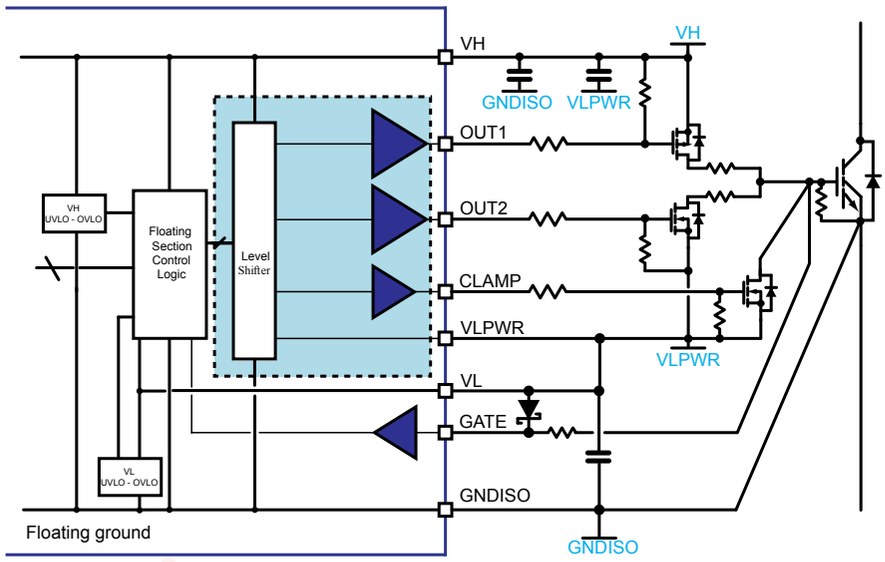
The Miller clamp function allows the control of the Miller current during the power stage switching in half-bridge configurations, preventing the cross-conduction that might be caused by gate spikes. When the external power transistor is in the off-state, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch in the same leg is being turned on, due to the Miller capacitance.

The gate of the external switch is monitored through the GATE pin and during a turn-off commutation the gate of the external CLAMP switch is activated when the voltage on the GATE pin goes below the voltage threshold V_{GATEth_OFF}. The CLAMP pin can drive an external low-voltage N-channel MOSFET, thus creating a low impedance path between the switch gate and the VLPWR pin.

To correctly perform the Miller clamp function the GATE pin must be connected through a resistor to the gate of the external IGBT/MOSFET power (see Section 7.4).

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Figure 37. **Example of Miller clamp protection connection**



7.14 Fault management

The device provides advanced diagnostics through open drain outputs ($\overline{DIAG1}$ and $\overline{DIAG2}$) and internal status registers.

Status registers (STATUS1, STATUS2, STATUS3, STATUS4, STATUS5) provide fault and status information as listed in the related sections.

$\overline{DIAG1}$ and $\overline{DIAG2}$ pins can be independently programmed through the dedicated registers (DIAG1CFGA, DIAG1CFGB, DIAG2CFGA and DIAG2CFGB) to signal one or more fault conditions. The state of each diagnostic output pin is the result of the NOR of the associated status bits, thus if one of the selected status bits is high the related $\overline{DIAGx}$ output is set low.

Some of the fault conditions reported by the status registers are latched, that means that the flag remains set high even if the triggering condition is no longer present.

The fault flags contained in the status registers can be cleared by a ***ClearStatus*** operation that can be executed by two methods:

- **the SPI command *ResetStatus***
  The $\overline{SD}$ pin must be set low before this command and must remain low until the end of the command's execution time. This is the recommended method, because it guarantees that the status registers are cleared only by direct intervention of the MCU. All the flags in the status registers are cleared after a t_{desCS_RST} time following the rising edge of the SPI $\overline{CS}$ (see Section 9.1.4).
- **the *SDReset* driving the $\overline{SD}$ pin**
  All the flags are cleared after the rising edge of the $\overline{SD}$ pin setting low the $\overline{SD}$ pin for at least a $t_{release}$ time. This mode is enabled by default at the device power-on but it can be disabled configuring SD_FLAG='0' in CFG1, avoiding the possibility to clear the flags without the direct intervention of the MCU. Even with SD_FLAG='1', the SDReset is not executed if before the rising edge of the $\overline{SD}$ pin a rising edge of the CK occurs while $\overline{CS}$ is low. This prevents the unintentional clearing of errors that may have been generated during the SPI communication, for instance a configuration sequence. In this case, to be able to execute a SDReset, a rising edge of the $\overline{CS}$ must happen before setting low again the $\overline{SD}$ pin.

The possibility to clear the status registers by SDReset allows to operate the device also without using the SPI interface. In case the SPI is used, it is recommended to disable this functionality by configuring SD_FLAG='0' to avoid the unintentional clearance of fault conditions.

Selected faults force the device in "SafeState"; the device remains in this state until the related status flags are released. Refer to Table 60, Table 62, Table 64, Table 66 for details.

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7.15 Asynchronous stop command

The ASC pin allows to turn on the external power switch acting directly on the HV side driver logic, regardless of the status of the primary side. Indeed, the ASC function works also if the primary-side 3V3IN supply voltage is not present or in UVLO condition. The faults on the LV side haven't any effect on the ASC function. The power supply of the HV side, both VH and VREGISO, must be present and have completed the start-up transient. If the primary side is supplied and no faults are present the ASC pin works according to Table 14:

Table 14. ASC truth table

ASC	External power switch state
0	See Table 10 and Table 11
1	ON

If the HV side is in HW3PS state the ASC command is overridden, thus OUT1 and OUT2 are LOW (External power switch in ON state) even if ASC=0 (see Section 6.4).

In relation to the HV side protection functions the behavior of the ASC pin is as described in Table 15 :

Table 15. ASC interaction with protection functions

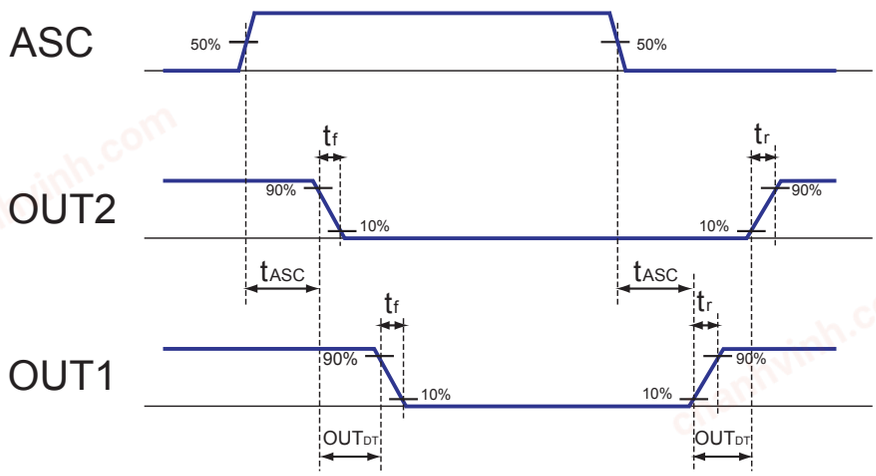
Protection	Protection configuration	ASC functionality
VH UVLO	Enabled	ASC active if VH supply is not in UVLO condition
	Disabled	ASC active if VH supply is within recommended operating values
VH OVLO	-	ASC is not active
VL UVLO	-	ASC is active
VL OVLO	-	ASC is active
REGERRR	-	ASC is active
COMERRR	-	ASC is active
Thermal Warning	-	ASC is active
Thermal Shutdown	-	ASC is not active while in thermal shutdown protection
DESAT	Enabled	The rising edge of ASC turns on the external power switch regardless of DESAT_OC flag status in the STATUS1 register. If a DESAT event occurs, detected when the DESAT pin exceeds the threshold selected, the external power switch is turned off and the DESAT_OC is set or confirmed high. ASC can turn on again the external power switch with a new ASC rising edge. If a ClearStatus command clears the DESAT_OC flag while ASC is high the external power switch maintains the present status. After a ClearStatus one of the following input combinations must be set to enable the output turn-on: IN+ / IN- / $\overline{SD}$ / ASC X / X / 0 / 0 X / 1 / X / 0 0 / X / X / 0
SENSE	Enabled	The rising edge of ASC turns on the external power switch regardless of SENSE_OC flag status in the STATUS1 register. If a SENSE event occurs, detected when the SENSE pin exceeds the selected threshold, the external power switch is turned off and the SENSE_OC is set or confirmed high. ASC can turn on again the external power switch with a new ASC rising edge. If a ClearStatus command clears the SENSE_OC flag while ASC is high the external power switch maintains the present status.

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Protection	Protection configuration	ASC functionality
		After a ClearStatus one of the following input combinations must be set to enable the output turn-on: IN+ | IN- | $\overline{SD}$ | ASC X | X | 0 | 0 X | 1 | X | 0 0 | X | X | 0

The ASC function is active also when the device is in Configuration Mode.
The status of this pin is reported in the ASC_LEVEL_LV bit present in the STATUS4 register.

Figure 38. ASC to OUT1 and OUT2 timing diagram



7.16 Security check functions

The device allows to verify the integrity of many important features through the following security checks:

- OUT1/OUT2 to gate path
- DESAT
- DEFAULT functionality
- SENSE resistor connection
- SENSE comparator
- CLAMP driver
- ADC

These check modes are enabled through a dedicated configuration register TEST1 (refer to Section 9.2.13) and thus require entering into configuration mode to be performed.

To execute the checks correctly the following points must be considered:

- only one check at a time must be enabled
- it is mandatory to execute a ClearStatus before executing each check
- before operating the driver in normal mode the TEST1 register must be set to 0x00
- it is recommended to execute a ClearStatus after having disabled each check
- to prevent the $\overline{SD}$ from clearing the STATUS flags it is recommended to set the SD_FLAG='0'
- ASC must be kept low during all the tests
- a "gate turn-on" is obtained setting: $\overline{SD}$=HIGH, IN-=LOW, IN+=HIGH
- a "gate turn-off" is obtained setting: $\overline{SD}$=HIGH, IN-=LOW, IN+=LOW

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7.16.1 OUT1/OUT2 to gate path

The purpose of this security check is to verify the correct operation of the internal gate comparators and the gate path integrity including the driver's OUT1 and OUT2 outputs, the external push-pull MOSFETs, the gate resistor and the power switch gate.

To perform the check the following steps must be executed:

- Set $\overline{SD}$="LOW"
- Send ResetStatus command
- Send StartConfig command
- Set OUT1OUT2CHK='1'
- Set SD_FLAG='0'
- Set ADC_EN='1'
- Set properly the ADC parameters (ADC_HIGHth, ADC_LOWth)
- Send StopConfig command
- Set $\overline{SD}$="HIGH"
- Apply to the input a "gate turn-on" (ON PHASE)
- Wait 20 us
- Read TWN, PROGHV, REGERRR (STATUS2)
- Read GATE_LEVEL_LV (STATUS4)
- Read the ADC output code (STATUS5)
- Apply to the input a "gate turn-off" (OFF PHASE)
- Wait 20 us
- Read TWN, PROGHV, REGERRR (STATUS2)
- Read GATE_LEVEL_LV (STATUS4)
- Read the ADC output code (STATUS5)

During the test the outputs are driven according to the inputs and during the reading the input state must be kept stable.

The test can be considered passed if the following conditions are verified:

- during the ON PHASE: TWN='1', PROGHV='1' and REGERRR='1'
- during the OFF PHASE: TWN='0', PROGHV='0' and REGERRR='0'

Otherwise the test has failed.

When the check is enabled by setting OUT1OUT2CHK='1' the comparator outputs are reported to the registers in the following way:

Table 16. OUT1/OUT2 to gate path check – Bits mapping

	"1" if…	"0" if…
TWN	$COMP_ON_{OUT}$ is HIGH	$COMP_ON_{OUT}$ is LOW
PROGHV	$COMP_OFF_{OUT}$ is LOW	$COMP_OFF_{OUT}$ is HIGH
REGERR	GATE level is HIGH	GATE level is LOW
	Expected combination during the ON PHASE with test OK	Expected combination during the OFF PHASE with test OK

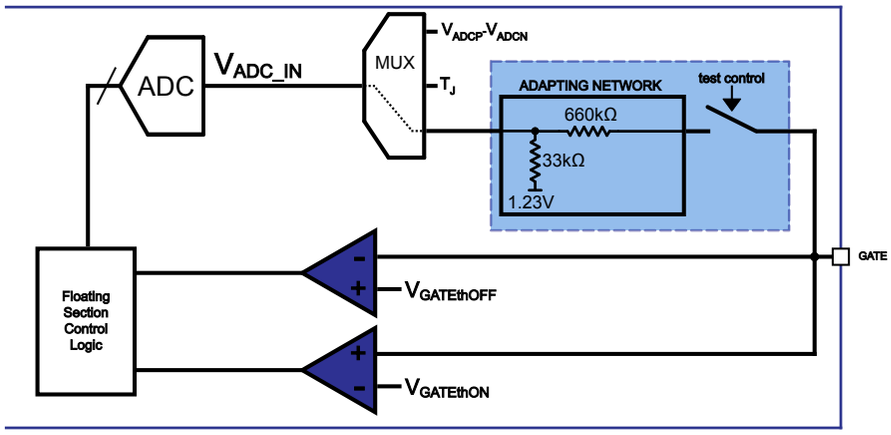
Additionally, during each phase the GATE level is reported to GATE_LEVEL_LV bit in STATUS4 register and the actual voltage of the GATE pin is available in STATUS5 register as ADC output code.

The voltage of the GATE pin must be stable within approximately 2us from the "gate turn-on"/"gate turn-off" commands.

When the security check is activated a test control switch is closed and the input of the ADC is internally diverted to the GATE pin through a dedicated adapting network as reported in Figure 39:

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Figure 39. **OUT1/OUT2 to gate path check**



This test allows to measure and check the VH and VL supply voltages, indeed during the ON PHASE the voltage of the gate of the external power IGBT/SiC is the VH voltage while during the OFF PHASE is the VL voltage.

The input voltage of the ADC can be calculated with the following equation:

$$V_{ADC_IN} = (V_{GATE} - 1.23V) * \left(\frac{33k\Omega}{660k\Omega + 33k\Omega}\right) + 1.23V \quad (8)$$

where:

- V_{ADC_IN} is the input voltage of the ADC referred to GNDISO
- V_{GATE} is the voltage of the GATE pin referred to GNDISO

To allow the correct execution of this measure, the ADC must be enabled setting ADC_EN = '1 in CFG7 configuration register and the ADC input range must be properly programmed according to the voltage range to be converted configuring the ADC_LOWth and the ADC_HIGHth bits. These operations can be done in the configuration sequence that activates the test.

At the end of the test, to return to the correct operation of the driver, the check function must be disabled configuring OUT1OUT2CHK='0' in the configuration register TEST1 and afterwards a ClearStatus must be executed to clear any latched fault. Also the ADC parameters (ADC_EN, ADC_HIGHth, ADC_LOWth, ADC_INPUT) must be configured back to the values used in application.

7.16.2 DESAT

This check allows to verify the correct operation of the DESAT functionality and to detect a short on the DESAT pin.

To perform the check the following steps must be executed:

- Set $\overline{SD}$ =“LOW”
- Send ResetStatus command
- Send StartConfig command
- Set DESAT_EN='1'
- Configure DESAT parameters (DESATcur and DESATth)
- Set DESCHK='1'
- Set SD_FLAG='0'
- Send StopConfig command
- Set $\overline{SD}$=“HIGH”
- Apply to the input a “gate turn-on” for at least t_{DES_chk} (see below definition)
- Read DESAT_OC flag

The test can be considered passed if DESAT_OC='1', otherwise the test has failed.

When DESAT check is activated, the turn-on command received by HV side is not transmitted to OUT1 and OUT2 outputs and the external power MOSFET/IGBT remains OFF.

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During the test ASC must be kept LOW and the external MOSFET/IGBT's drain/collector must be in high impedance state.

When gate turn-on is applied, after the fixed blanking time, I_{DESAT} starts charging the external blanking capacitor. In correct operation the voltage of the input pin DESAT rises and after a time t_{DES_chk} it surpasses $V_{DESATth}$.

The test result is determined by the flag DESAT_OC as follows:

- DESAT_OC='1' if ($V_{DESATcomp}$ > $V_{DESATth}$) which means test PASSED
- DESAT_OC='0' if ($V_{DESATcomp}$ < $V_{DESATth}$) which means test FAILED

Basically, the time t_{DES_chk} can be approximately calculated with the following equation:

$$t_{DES_chk} \approx t_{Don(MAX)} + t_{FBLK(MAX)} + \frac{V_{DESATth(MAX)} \cdot C_{DESAT}}{I_{DESAT(MIN)}} \quad (9)$$

To obtain the actual value the specific case in the application must be considered, indeed the equivalent capacitance seen through the resistor and the diode causes a longer time.

At the end of the test, to return to the correct operation of the driver, the check function must be disabled configuring DESCHK='0' in the configuration register TEST1 and afterwards a ClearStatus must be executed to clear any latched fault.

7.16.3 DEFAULT functionality

This check allows to verify:

- the watchdog mechanism
- the correct setting of the outputs OUT1/OUT2 in case of HV watchdog expiration
- the correct connection of the DEFAULT pin in application

The test is differentiated for the two possible cases, DEFAULT expected low and DEFAULT expected high.

CASE 1 – DEFAULT expected low

- Set $\overline{SD}$="LOW"
- Send ResetStatus command
- Send StartConfig command
- Set DEFAULTCHK='1'
- Set GATECHK='1'
- Set SD_FLAG='0'
- Send StopConfig command
- Set $\overline{SD}$="HIGH"
- Wait 10 us + $t_{DEL_HW3PS_ON}$
- Read GATE_LEVEL_LV
- Read COMMERRR, COMMERRL

The test can be considered passed if:

- GATE_LEVEL_LV='0'
- COMMERRR='1'
- COMMERRL='1'

Otherwise the test has failed.

Internally the device executes the following actions:

- S1 is closed and S2 is opened (see Figure 40)
- Periodical refresh from HV to LV is stopped

CASE 2 – DEFAULT expected high

- Set $\overline{SD}$="LOW"
- Send ResetStatus command
- Send StartConfig command
- Set DEFAULTCHK='1'
- Set GATECHK='0'
- Set SD_FLAG='0'

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- Send StopConfig command
- Set $\overline{SD}$="HIGH"
- Wait 10 us + $t_{DEL_HW3PS_ON}$
- Read GATE_LEVEL_LV
- Read COMMERRR, COMMERRL

The test can be considered passed if:

- GATE_LEVEL_LV='1'
- COMMERRR='1'
- COMMERRL='1'

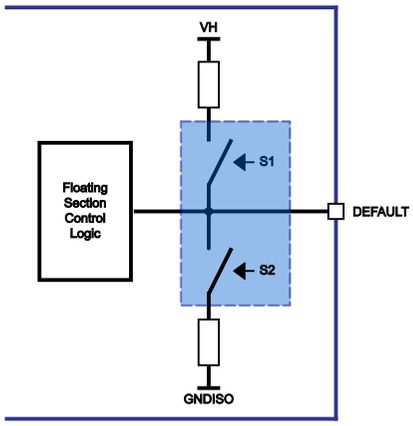
Otherwise the test has failed.

Internally the device executes the following actions:

- S2 is closed and S1 is opened (see Figure 40)
- Periodical refresh from HV to LV is stopped

The device follows the flow described in the "Operation flow chart", thus if the DEAFULT pin is high the output is set as for the HW3PS state.

Figure 40. DEFAULT functionality check



At the end of the test, to return to the correct operation of the driver, the check function must be disabled configuring DEFAULTCHK='0' in the configuration register TEST1 and afterwards a ClearStatus must be executed to clear any latched fault.

7.16.4 SENSE resistor

This check allows to verify the connection to the external sense resistor on the SENSE pin.

To perform the check the following steps must be executed:

- Set $\overline{SD}$="LOW"
- Send ResetStatus command
- Send StartConfig command
- Set SENS_EN='1'
- Set RSNSCHK='1'
- Set SD_FLAG='0'
- Send StopConfig command
- Set $\overline{SD}$="HIGH"
- Wait at least t_{Rchk}
- Read SENSE_OC flag

The test is passed if SENSE_OC='0', otherwise the test has failed.

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The test is performed sourcing a small current $I_{SENSERchk}$ to the SENSE pin. If, for some reason, the pin is floating the voltage rises until exceeding $V_{SENSEth}$ and SENSE_OC='1' is reported in the STATUS1 register. Otherwise, if the pin is correctly shunted, the voltage on the pin remains below $V_{SENSEth}$. The minimum time to have a reliable value in SENSE_OC is t_{Rchk} (SENSE resistor check time).

If an external filter network is present this must be taken into account. To perform the check correctly the voltage drop on the filter, when the $I_{SENSERchk}$ current is sourced, must be lower than the $V_{SENSEth}$, otherwise the test is not passed although the shunt is correctly connected. Also the minimum time to have a reliable result is impacted by the filter and the correct time value to wait must be checked for each specific case.

At the end of the test, to return to the correct operation of the driver, the check function must be disabled configuring RSNSCHK='0' in the configuration register TEST1 and afterwards a ClearStatus must be executed to clear any latched fault.

7.16.5 SENSE comparator

This check allows to verify the functionality of the internal sense comparator.

To perform the check, the following steps must be executed:

- Set $\overline{SD}$="LOW"
- Send ResetStatus command
- Send StartConfig command
- Set SENS_EN='1'
- Set SNSCHK='1'
- Set SD_FLAG='0'
- Send StopConfig command
- Set $\overline{SD}$="HIGH"
- Wait at least t_{Rchk}
- Read SENSE_OC flag

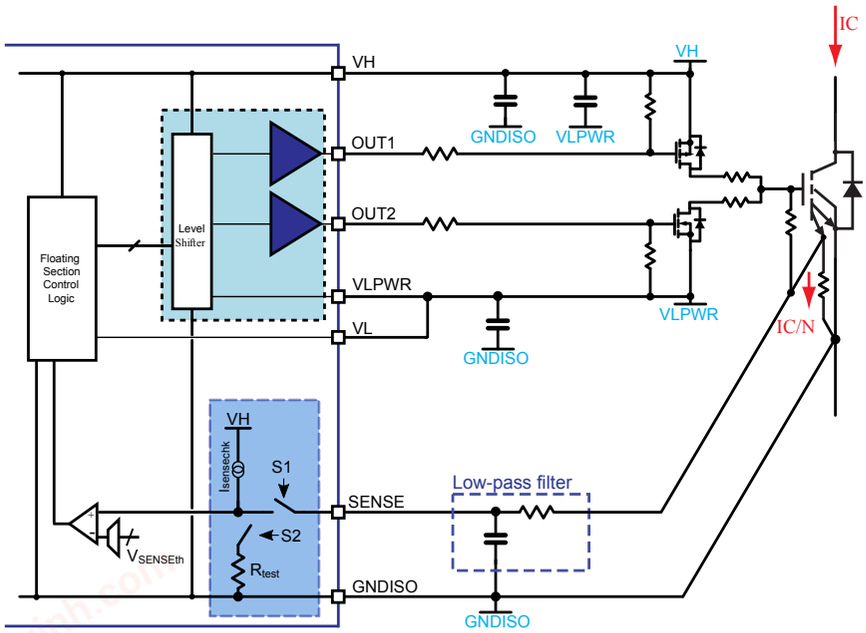
The test is passed if SENSE_OC='1', otherwise the test has failed.

Internally, when the check is enabled, S1 is open and S2 is closed (see Figure 41). The test current $I_{sensechk}$ generates a voltage on test resistor $R_{test.}$ If the voltage is greater than $V_{SENSEth}$ an overcurrent is triggered and the device sets SENSE_OC='1'. If SENSE_OC='0' something is not correctly working.

At the end of the test, to return to the correct operation of the driver, the check function must be disabled configuring SNSCHK='0' in the configuration register TEST1 and afterwards a ClearStatus must be executed to clear any latched fault.

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Figure 41. **SENSE comparator check**



7.16.6 CLAMP driver

This check allows to verify the functionality of the Miller clamp output stage.

To perform the check, the following steps must be executed:

- Set $\overline{SD}$="LOW"
- Send ResetStatus command
- Send StartConfig command
- Set MCPCHK='1'
- Set SD_FLAG='0'
- Send StopConfig command
- Set $\overline{SD}$="HIGH"
- Apply at the input a "gate turn-on" command (ON PHASE)
- Wait at least 10 us
- Read GATE_LEVEL_LV flag
- Apply at the input a "gate turn-off" command (OFF PHASE)
- Wait at least 10 us
- Read GATE_LEVEL_LV flag

During the test, the outputs are driven according to the inputs and during the reading the input state must be kept stable.

The test can be considered passed if the following conditions are verified:

- during the ON PHASE: GATE_LEVEL_LV='1'
- during the OFF PHASE: GATE_LEVEL_LV='0'

Otherwise the test has failed.

Internally the device keeps OUT2=LOW also during the OFF PHASE performing the "gate turn-off" through the external N-channel MOSFET driven by the CLAMP pin.

The voltage of the GATE pin must be stable within approximately 2us from the "gate turn-on"/"gate turn-off" commands. If more time is needed this must be added to the "wait time" after the command.

At the end of the test, to return to the correct operation of the driver, the check function must be disabled configuring MCPCHK='0' in the configuration register TEST1 and afterwards a ClearStatus must be executed to clear any latched fault.

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7.16.7 ADC functionality check

This check allows to verify the functionality of the internal ADC.

To perform the check, the following steps must be executed:

- Set $\overline{SD}$="LOW"
- Send ResetStatus command
- Send StartConfig command
- Set ADC_EN='1'
- Set ADC_INPUT='0'
- Set ADCCHK='1'
- Set SD_FLAG='0'
- Send StopConfig command
- Wait at least 20 us
- Read TWN (STATUS2)

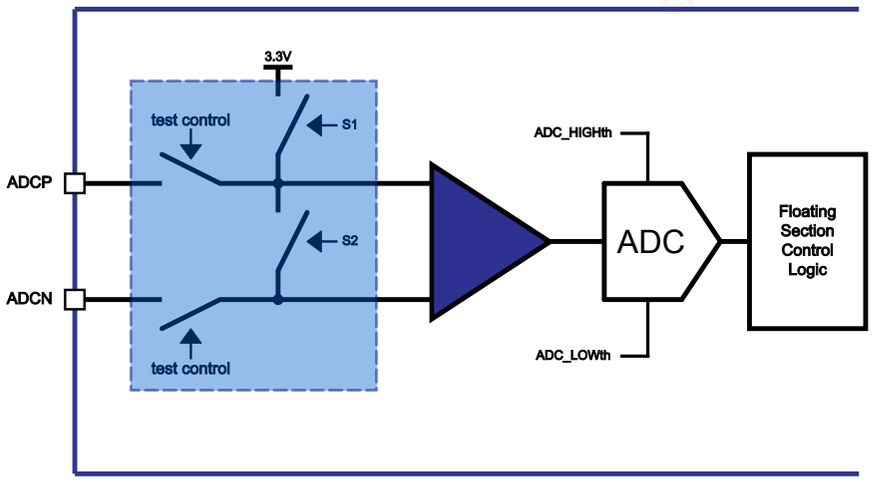
The test is passed if TWN='1', otherwise the test has failed.

Internally the device executes the following steps:

- the switches in series to ADCP and ADCN are opened.
- the ADC output code register is internally forced to "00001111"
- the differential input of the ADC is internally forced to VREGISO (S1 closed, S2 open, see Figure 42)
- if the ADC output code is "11111111" this internal test phase is OK, otherwise FAIL
- the differential input of the ADC is internally forced to 0V (S1 open, S2 closed, see Figure 42)
- if the ADC output code is "00000000" this internal test phase is OK, otherwise FAIL

If both the internal test phases are OK the device sets TWN='1', otherwise the device sets TWN='0'.

Figure 42. ADC functionality check



At the end of the test, to return to the correct operation of the driver, the check function must be disabled configuring ADCCHK='0' in the configuration register TEST1 and afterwards a ClearStatus must be executed to clear any latched fault. The ADC parameters (ADC_EN, ADC_HIGHth, ADCLOWth, ADC_INPUT) must be configured back to the values used in application.

7.17 Registers corruption protection

All the configuration registers are protected against content corruption.

If the value of a local configuration register changes without the execution of a proper command (the configuration sequence or the SoftReset) the REGERRL flag is set HIGH and the device is forced in "SafeState" or remains in "HW3PS" if this is the current state. See details in Section 6.4.

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If the value of a remote configuration register changes without the execution of a proper command (the configuration sequence or the SoftReset) the REGERRR flag is set HIGH and the device is forced in “SafeState”.

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8 SPI interface

The STGAP4S communicates with an external MCU through a 16-bit SPI. This interface is used to set the device parameters and for advanced diagnostics.

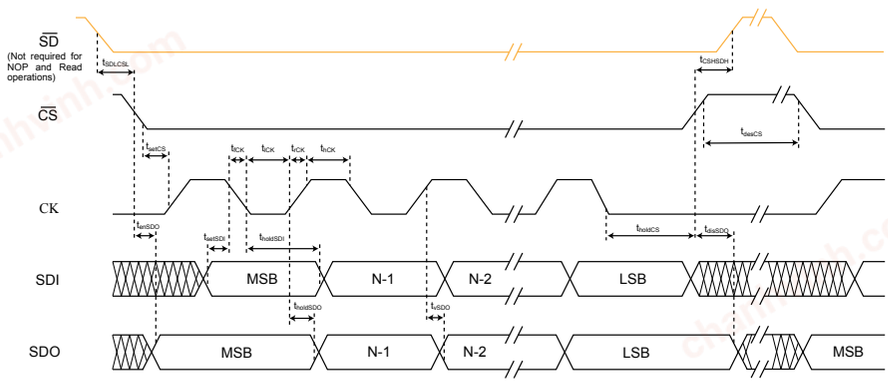
The SPI commands are executed after the rising edge of $\overline{CS}$ and adequate wait time must be respected before a new command is started by setting $\overline{CS}$ low again. Refer to the $\overline{CS}$ deselect time parameters in Section 4.2 for required wait time after each command.

The SPI I/O pins are:

- $\overline{CS}$: chip select (active low)
- CK: serial clock
- SDI: serial data input (MOSI)
- SDO: serial data output (MISO).

The interface uses the SPI configuration CPHA = 1 and CPOL = 0 (serial data is sampled on CK falling edge and it is updated on CK rising edge, at the $\overline{CS}$ falling edge the CK signal must be low) as shown in Figure 43.

Figure 43. SPI timings



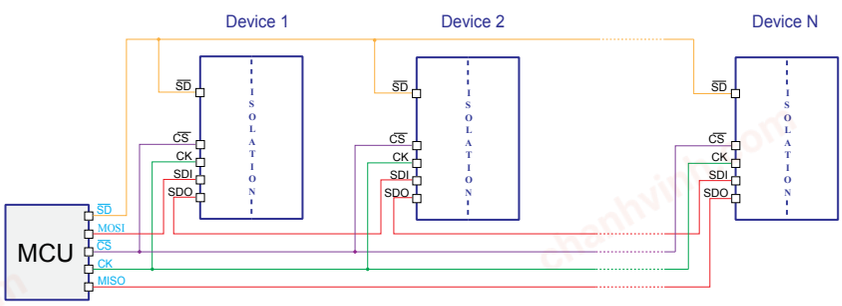
The SPI interface can work with a clock CK up to 5 Mbps and allows the connection of multiple STGAP4S devices in a daisy chain. The SDO output must be connected only to logic inputs of other devices.

In order to guarantee a safe operation and robustness to electrical noise, the number of rising edges within a $\overline{CS}$ negative pulse must be multiples of 16, otherwise the communication cycle is ignored and an error is reported setting high the SPI_ERR flag.

In the daisy chain topology any number of the STGAP4S can be connected and only four SPI lines and one for the $\overline{SD}$ are required in order to access the status and configuration registers of each device. An example of daisy chain configuration is shown in Figure 44.

Each device in the chain can be configured independently allowing, for instance, the differentiation of the configuration for the high-side and low-side drivers.

Figure 44. SPI daisy chain connection example



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8.1 CRC protection

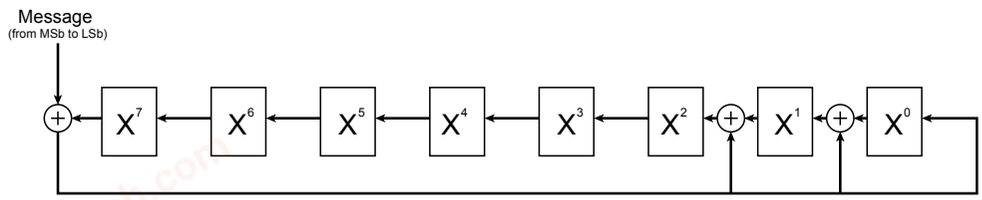
All the commands and data bytes must be followed by a CRC code.

At the power-on or after a SoftReset the SPI CRC is disabled by default (CRC_SPI='0') and the STGAP4S does not consider the content of the CRC byte. In this case the host must transmit the CRC byte anyway although the STGAP4S does not use it for integrity checks. The STGAP4S generates the correct CRC byte in response to the SPI access also with the CRC disabled.

If the SPI CRC is enabled by setting CRC_SPI='1', the CRC byte transmitted by the host is used by the device to check the integrity of the data byte and an error in the CRC check causes the related data byte to be ignored and the SPI_ERR flag is set high.

The polynomial generator of the CRC code is X^8+X^2+X+1 corresponding to the block diagram in Figure 45.

Figure 45. Block diagram of the CRC generator



The host must transmit to the device the inverted CRC code computed using the following procedure:

- Initialize CRC to all 1
- Start the calculation from the most significant bit of the message
- Invert the CRC result

In case of a WriteReg command, the CRC of the data byte (i.e. the new register value) must be calculated initializing the computation system to the CRC of the command byte previously calculated (i.e.: the CRC is calculated on a 16-bit message composed by the command + data byte). In this way a data byte cannot be accepted as a command byte and vice versa.

The device always transmits a response byte followed by a CRC computed using the same polynomial generator ($X^8 + X^2 + X + 1$). The CRC byte transmitted by the device is not inverted.

If no response is required, the word returned by the device has no meaning and it should be discarded.

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9 Programming manual

9.1 SPI commands

The SPI interface is provided with a set of commands that allow the configuration of the device as well as the access to the advanced diagnostic.

The NOP and the ReadReg command, dedicated to the registers content read as described in Section 9.1.3, can be executed without stopping the PWM, as long as the SPI signals are not distorted by noise affecting the integrity of the communication.

The ResetStatus command, dedicated to the clearing of the fault flags as described in Section 9.1.4, is executed only when the $\overline{SD}$ pin is LOW, thus when the PWM is not running.

The device has a one position FIFO buffer (First In First Out) that, in case the LV side recognizes that the HV side is powered-off, stores the last ReadReg or ResetStatus command received. Afterwards the LV side sends the stored command to the HV side as soon as it recognizes that the HV side is powered-on.

Some commands are dedicated to the configuration of the device and also in this case the execution is performed only when the $\overline{SD}$ pin is LOW, corresponding to the condition with PWM not running, and furthermore the modification of the configuration registers content is allowed only when the device is Configuration Mode. The suggested flow is reported in Figure 46.

The commands summary is given in Table 17

Table 17. SPI commands

Command mnemonic	Command value								Action	Notes
StartConfig	0	0	1	0	1	0	1	0	Device configuration start	Enter CFG mode $\overline{SD}$ low only
StopConfig	0	0	1	1	1	0	1	0	Device configuration/check completed	Leave CFG mode $\overline{SD}$ low only
NOP	0	0	0	0	0	0	0	0	No operation	
WriteReg	1	0	0	A	A	A	A	A	Write AAAAA register	CFG mode only
ReadReg	1	0	1	A	A	A	A	A	Read AAAAA register	
ResetStatus	1	1	0	1	0	0	0	0	Reset all the status registers	$\overline{SD}$ low only
SoftReset	1	1	1	0	1	0	1	0	Soft reset	CFG mode only

9.1.1 StartConfig and StopConfig commands

Table 18. StartConfig command synopsis

Byte	1	2
To device	COMMAND	CRC(1)
	0010 1010	1101 1010

1. *If CRC check is disabled this byte is ignored.*

Table 19. StopConfig command synopsis

Byte	1	2
To device	COMMAND	CRC(1)
	0011 1010	1010 1010

1. *If CRC check is disabled this byte is ignored.*

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The device can be configured properly writing the values of the configuration registers (CFGx and DIAGxCFGx), operation that is allowed only entering in configuration mode.

To switch the device to the configuration mode the *StartConfig* command must be sent. The execution needs a $\overline{CS}$ deselect time t_{desCS_STC} and it is valid only if the $\overline{SD}$ input is low, otherwise the command is not executed and the SPI_ERR flag is set HIGH. If the command has been correctly received and interpreted, the configuration registers writing is enabled. When the *StartConfig* command is correctly received, the flag PROGLV (STATUS3) and PROGHV (STATUS2) are set high, indicating that the device has entered the configuration mode.

The $\overline{SD}$ pin must be kept low during the whole configuration procedure. If the $\overline{SD}$ pin is raised during the configuration procedure the device immediately quits the configuration mode causing an error indicated by the SPI_ERROR bit. In this case all the changes operated on the device configuration are ignored and the previous configuration is maintained.

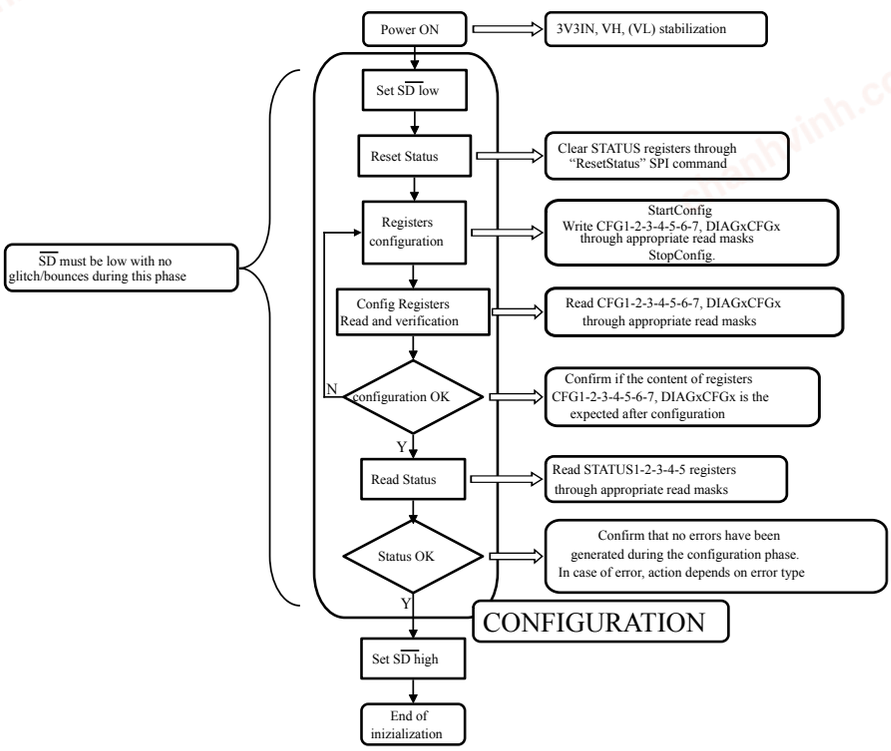
At the end of the device configuration the *StopConfig* command must be sent to quit the configuration mode and to make all changes effective. The execution needs a $\overline{CS}$ deselect time t_{desCS_SPC}.

The PROGLV and PROGHV bits are set low only when the device is configuration mode and a StopConfig command is received.

The configuration sequence must be repeated every time the power supply of one of the two sides (3V3IN or VH) is removed and then restored.

When all supply voltages are stable, the configuration process can be executed. The flow chart shown in Figure 46 is recommended for the configuration. At the end of the configuration sequence it is possible to check that the desired configuration has been correctly executed.

Figure 46. STGAP4S recommended configuration flow



The configuration procedure must be completed within the configuration timer t_{CFG}. The timer is started after receiving a StartConfig command and it is stopped after receiving a StopConfig command. If the configuration is not completed within the timer, that is, the StopConfig is not received before the timer is expired, the device immediately quits the configuration mode causing an error indicated by the SPI_ERROR bit. In this case all the changes operated on the device configuration are ignored and the previous configuration is maintained. In this case the PROGLV and PROGHV bits remain set high.

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9.1.2 WriteReg command

Table 20. WriteReg command synopsis

Byte	1	2	3	4
To device	COMMAND+ADDRESS	CRC(1)	DATA(2)	CRC(3)
	100A AAAA(4)	CCCC CCCC	DDDD DDDD	KKKK KKKK

1. *CRC byte of the command, if CRC check is disabled this byte is ignored.*
2. *Data to be written into the target register.*
3. *CRC byte of the command and data, if CRC check is disabled this byte is ignored.*
4. *Command byte where AAAAA is the address of the target register.*

The device registers can be written through the WriteReg command when the device is set in configuration mode only (refer to Section 9.1.1), otherwise the write command is ignored and the SPI_ERR flag is set HIGH.

A complete WriteReg is composed by 4 bytes thus it requires two SPI accesses to be executed. In the first access the SPI host must send the Byte 1 and Byte 2 (containing the command, the address of the register to be written and the related CRC) followed by the proper $\overline{CS}$ deselect time. Then, in the second access, the host must send the Byte 3 and Byte 4 (containing the data to be written into the target register and the CRC) followed by the same $\overline{CS}$ deselect time.

The $\overline{CS}$ deselect time required depends on the side where the register is located. The writing of a local register (LV side) needs a $\overline{CS}$ deselect time t_{desCS_LWR}. The writing of a remote register (HV side) needs a $\overline{CS}$ deselect time t_{desCS_RWR}. See Section 4.2 for details.

The CRC of the data byte (Byte 4) must be calculated initializing the computation system to the CRC of the command byte previously calculated (Byte 2). In this way, in case of communication error, a data byte cannot be decoded as a command and vice versa (refer to Section 8.1).

9.1.3 ReadReg command

Table 21. ReadReg command synopsis

Byte	1	2	3(1)	4
To device	COMMAND+ADDRESS	CRC(2)	NOP	CRC(3)
	101A AAAA(4)	CCCC CCCC	0000 0000	0000 1100
From device	SPI BUFFER(5)	CRC(6) of the SPI output buffer	REQUESTED DATA(7)	CRC(8)
	XXXX XXXX	YYYY YYYY	DDDD DDDD	KKKK KKKK

1. *Appropriate time has to pass in order to allow the device to prepare the data.*
2. *The CRC byte of the command, if the CRC check is disabled this byte is ignored.*
3. *The CRC byte of the NOP command,if the CRC check is disabled this byte is ignored*
4. *The command byte where AAAAA is the address of the target register.*
5. *Content of the SPI output buffer when the ReadReg is sent*
6. *CRC*
7. *Data read from the target register.*
8. *The CRC byte of the data.*

All the registers of the device can be read anytime and this requires two SPI accesses.

In the first access the SPI host must send the ReadReg containing the command and the address of the register to be read (Byte 1) and the related CRC code (Byte 2). After waiting the proper $\overline{CS}$ deselect time the read result is stored in the SPI output buffer and the host can receive it doing a new SPI access that shifts the output buffer content. Any command can be used for this purpose, including a NOP or the ReadReg command for the next register to be read. In Table 21 an example is reported using the NOP (Byte 3) and the related CRC (Byte 4).

The deselect time required depends on the side where the register is located. The reading of a local register (LV side) needs a $\overline{CS}$ deselect time t_{desCS_LRD}. The reading of a remote register (HV side) needs a $\overline{CS}$ deselect time t_{desCS_RRD}. See Section 4.2 for details.

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The CRC polynomial used by the device during the transmission is the same used by the host, the CRC code is not inverted before transmission (refer to Section 8.1).

Some status and configuration registers contain reserved bits whose content is not predictable. In order to clearly identify the content of relevant information, the value read from each register should be masked with the appropriate masking code (see Table 26).

9.1.4 ResetStatus command

Table 22. ResetStatus command synopsis

Byte	1	2
To device	COMMAND	CRC(1)
	1101 0000	0011 0010

1. *if the CRC check is disabled this byte is ignored.*

The *ResetStatus* command acts on all status registers clearing all the flags. The execution needs a $\overline{CS}$ deselect time t_{desCS_RST} and it is valid only if the $\overline{SD}$ input is low, otherwise the command is not executed and the SPI_ERR flag is set HIGH.

If during the execution of the command a fault is present the related bit is not cleared.

9.1.5 SoftReset command

Table 23. SoftReset command synopsis

Byte	1	2
To device	COMMAND	CRC(1)
	1110 1010	1001 0100

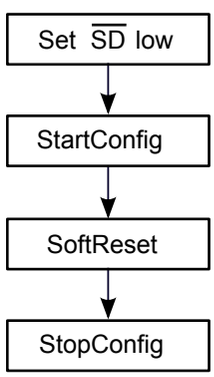
1. *If the CRC check is disabled this byte is ignored.*

The *SoftReset* command restores all the registers (both the Status and the Configuration) to the default value and clears all the fault flags. The command execution needs a $\overline{CS}$ deselect time t_{desCS_RST} and it is valid only when the device is in configuration mode, otherwise the command is not executed and the SPI_ERR flag is set HIGH. The reset of the registers is applied only after the execution of the “StopConfig” command.

If during the execution of the command a fault is present the related bit is not cleared.

When the SoftReset command is executed no other commands must be present in the same configuration slot, as in the sequence reported in Figure 47:

Figure 47. SoftReset Flow



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9.1.6 NOP command

Table 24. **NOP command synopsis**

Byte	1	2
To device	COMMAND	CRC(1)
	0000 0000	0000 1100

1. *If the CRC check is disabled this byte is ignored.*

The command does not modify the device status and does not generate any answer. The execution needs a $\overline{CS}$ deselect time t_{desCS_NOP}.

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9.2 Registers and flags description

All device features can be configured through a set of 8-bit long registers.

There are two different types of registers:

- Local registers are located on the low voltage side
- Remote registers are located on the high voltage side

A map of the user registers is shown in Table 25

Table 25. Registers map

Name	Side(1)	Structure							
-	-	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CFG1	L	UVLO3V3IN_EN	SD_FLAG	DTset			INfilter		ADC_PWM_EN
CFG2	R	SENSE_EN	SAFE_OFF	DESAT_EN	DESATcur		DESATth		
CFG3	R	OVLOVHth		UVLOlatch	VLONth		VHONth		
CFG4	R	SENSEth			ADC_CScur		ADC_INPUT	SOFT_2LTO	OUT_DTth
CFG5	R	-	-	-	-	2LTO_SOFTtime			
CFG6	L	CONTROLLER_FREQ		CRC_SPI	-	-	-	-	-
CFG7	R	ADC_HIGHth			ADC_LOWth			ADC_EN	OFFMODE
STATUS1	R	OVLOH	OVLOL	DESAT_OC	SENSE_OC	UVLOH	UVLOL	TSD	STATUS1_BUSY
STATUS2	R	SAFESTATE	HVReset	-	TWN	PROGHV	REGERRR	COMERRR	STATUS2_BUSY
STATUS3	L	UVLO_3V3IN	UVLO_VCC	-	DT_ERR	SPI_ERR	-	PROGLV	FLYBACK_FLT
STATUS4	L	-	PWM_LV	ASC_LEVEL_LV	GATE_LEVEL_LV	LVReset	REGERRL	COMERRL	SPI_HVbusy
STATUS5	L	ADC							
TEST1	R	ADC_CHK	RSNSCHK	SNSCHK	MCPCHK	DESCHK	DEFAULTCHK	OUT1OUT2CHK	GATECHK
DIAG1CFGA	R	DIAG1CFGA_7	DIAG1CFGA_6	DIAG1CFGA_5	DIAG1CFGA_4	DIAG1CFGA_3	DIAG1CFGA_2	DIAG1CFGA_1	DIAG1CFGA_0
DIAG1CFGB	L	DIAG1CFGB_7	DIAG1CFGB_6	DIAG1CFGB_5	DIAG1CFGB_4	DIAG1CFGB_3	DIAG1CFGB_2	DIAG1CFGB_1	DIAG1CFGB_0
DIAG2CFGA	R	DIAG2CFGA_7	DIAG2CFGA_6	DIAG2CFGA_5	DIAG2CFGA_4	DIAG2CFGA_3	DIAG2CFGA_2	DIAG2CFGA_1	DIAG2CFGA_0
DIAG2CFGB	L	DIAG2CFGB_7	DIAG2CFGB_6	DIAG2CFGB_5	DIAG2CFGB_4	DIAG2CFGB_3	DIAG2CFGB_2	DIAG2CFGB_1	DIAG2CFGB_0

1. *R: remote (high voltage side), L: local (low voltage side).*

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Table 26. **Registers access**

Name	Address	Mask code
CFG1	0x00	0xFF
CFG2	0x11	0xFF
CFG3	0x12	0xFF
CFG4	0x13	0xFF
CFG5	0x14	0x0F
CFG6	0x01	0xE0
CFG7	0x15	0xFF
STATUS1	0x1B	0xFF
STATUS2	0x1C	0xDF
STATUS3	0x0D	0xDB
STATUS4	0x0E	0x7F
STATUS5	0x1D	0xFF
TEST1	0x1F	0xFF
DIAG1CFGA	0x17	0xFF
DIAG1CFGB	0x18	0xFF
DIAG2CFGA	0x19	0xFF
DIAG2CFGB	0x1A	0xFF

9.2.1 CFG1 register (LV side)

The CFG1 register has the structure and default values in Table 27.

Table 27. **CFG1 register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	UVLO3V3IN_EN	SD_FLAG	DTset			INfilter		ADC_PWM_EN
SoftReset/Reset	0	1	000			00		0

The UVLO3V3IN_EN bit enables/disables the UVLO protection of 3V3IN supply voltage. This setting has no effect on the flyback section that is always stopped in case of UVLO condition on 3V3IN.

Table 28. **3V3IN supply voltage UVLO**

UVLO3V3IN_EN	3V3IN UVLO enable
1	Disabled
0	Enabled

The SD_FLAG bit sets the $\overline{SD}$ pin functionality according to Table 29. When the reset of the fault flags through the $\overline{SD}$ pin is enabled, keeping low the $\overline{SD}$ pin for at least $t_{release}$ causes all the flags of the status registers to be released at next $\overline{SD}$ rising edge.

Table 29. **Reset by $\overline{SD}$ pin**

SD_FLAG	$\overline{SD}$ pin functionality
0	$\overline{SD}$ pin do not reset the STATUS registers
1	$\overline{SD}$ pin resets the STATUS registers

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The DTset bits set the deadtime value of DT function.

Table 30. Deadtime

DTset[2..0]			DT Deadtime value [ns]
0	0	0	Disabled
0	0	1	250
0	1	0	500
0	1	1	750
1	0	0	1000
1	0	1	1250
1	1	0	1500
1	1	1	2000

The INfilter bits set the duration $t_{deglitch}$ of input deglitch filter for $\overline{SD}$, IN- and IN+ pins.

Table 31. Input deglitch time

INfilter [1..0]		Input deglitch time [ns]
0	0	Disabled
0	1	70
1	0	160
1	1	500

The ADC_PWM_EN bit enables the PWM output signal on the ADC pin.

Table 32. ADC_PWM_EN

ADC_PWM_EN	ADC PWM output signal enable
0	Disabled
1	Enabled

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9.2.2 CFG2 register (HV side)

The CFG2 register has the structure and default values in Table 33.

Table 33. CFG2 register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SENSE_EN	SAFE_OFF	DESAT_EN	DESATcur		DESATth		
SoftReset/Reset	0	0	1	00		010		

“SoftReset” is obtained by SPI SoftReset command.

“Reset” is obtained by power-on of the HV side.

The SENSE_EN bit enables the sense overcurrent protection function (refer to Section 7.9 for details).

Table 34. SENSE comparator enabling

SENSE_EN	SENSE protection
0	disabled
1	enabled

The SAFE_OFF bit determines the turn-off mode in case of overcurrent or desaturation event (activation of SENSE or DESAT protection).

Table 35. SAFE_OFF

SAFE_OFF	Desaturation/overcurrent turning off mechanism
0	Turn-off is performed as in normal operation
1	Turn-off is performed through SOFTOFF feature (the SOFT_2LTO bit must be set to 0)

The DESAT_EN bit enables the desaturation protection function:

Table 36. DESAT comparator enabling

DESAT_EN	DESAT protection
0	disabled
1	enabled

The DESATcur parameter sets the I_{DESAT} current sourced by DESAT pin according to Table 37 and the DESATth parameter sets the $V_{DESATth}$ threshold of DESAT comparator according to Table 38. Refer to Section 7.8 for details.

Table 37. DESAT current

DESATcur [1..0]		DESAT current [µA]
0	0	250
0	1	500
1	0	750
1	1	1000

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Table 38. **DESAT threshold**

DESATth [2..0]			DESAT threshold [V]
0	0	0	3
0	0	1	4
0	1	0	5
0	1	1	6
1	0	0	7
1	0	1	8
1	1	0	9
1	1	1	10

9.2.3 CFG3 register (HV side)

The CFG3 register has the structure and the default values in Table 39 .

Table 39. **CFG3 register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	OVLOVHth		UVLOlatch	VLONth		VHONth		
SoftReset/Reset	11		0	00		001		

“SoftReset” is obtained by SPI SoftReset command.

“Reset” is obtained by power-on of the HV side.

The OVLOHth bits set the $OVVH_{off}$ and $OVVH_{on}$ OVLO thresholds on VH positive power supply according to Table 40.

Table 40. **VH supply voltage OVLO threshold**

OVLOVHth [1..0]		$OVVH_{off}$ [V]	$OVVH_{on}$[V]
0	0	19	18
0	1	21	20
1	0	23	22
1	1	34	33

The UVLOlatch bit sets if the UVLOH and UVLOL are latched or not (refer to Section 7.6 for details).

Table 41. **VH and VL UVLO protection latch**

UVLOlatch	UVLOH and UVLOL latch
0	disabled
1	enabled

The VLONth bits set the VL_{off} and VL_{on} UVLO thresholds on VL negative power supply according to Table 42. By default at HV side power-on the function is disabled as VLONth=00.

When the function is enabled by configuring the device with one of the available thresholds, after the StopConfig command (see Section 9.1.1) the UVLOL fault could be temporarily asserted (for approximately 10 us) even if the voltage on the VL pin is not in UVLO condition. In this case if the protection is latched (UVLOlatch=1) at the end of the configuration the fault flag UVLOL in STATUS1 is found HIGH. If a diagnostic pin is configured to report the UVLOL fault (see Section 9.2.14) the pin behaves consequently to the UVLOL asserting.

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Table 42. **VL supply voltage UVLO threshold**

VLONth [1..0]		VL_{off} [V]	VL_{on} [V]
0	0	Disabled	
0	1	-2	-3
1	0	-4	-5
1	1	-6	-7

The VHONth bits set the VH_{off} and VH_{on} UVLO threshold on VH positive power supply according to Table 43. Setting VHONth='00' disables the UVLO protection of the VH supply.

Table 43. **VH supply voltage UVLO threshold**

VHONth [2..0]			VH_{off} [V]	VH_{on} [V]
0	0	0	Disabled	
0	0	1	10	11
0	1	0	11	12
0	1	1	12	13
1	0	0	13	14
1	0	1	14	15
1	1	0	15	16
1	1	1	16	17

9.2.4 CFG4 register (HV side)

The CFG4 register has the structure and default values in Table 44.

Table 44. **CFG4 register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SENSEth			ADC_CScur		ADC_INPUT	SOFT_2LTO	OUT_DTth
SoftReset/Reset	000			00		0	0	0

"SoftReset" is obtained by SPI SoftReset command
"Reset" is obtained by power-on of the HV side.
The SENSEth bits set the SENSE comparator threshold according to Table 45. Refer to Section 7.9 for details.

Table 45. **SENSE threshold**

SENSEth [2..0]			SENSE threshold [mV]
0	0	0	100
0	0	1	125
0	1	0	150
0	1	1	175
1	0	0	200
1	0	1	250
1	1	0	300
1	1	1	400

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The ADC_CScur bits define the current source connected to the ADCP pin of internal ADC (refer to Section 7.10 for details).

Table 46. ADC current source

ADC_CScur [1..0]		ADC current source [µA]
0	0	0
0	1	300
1	0	600
1	1	1000

The ADC_INPUT bit defines the input source provided to internal ADC, according to the following table:

Table 47. ADC_INPUT

ADC_INPUT	ADC input signal source
1	Internal IC temperature measurement
0	Differential voltage between V_{ADCP} and V_{ADCN}

The SOFT_2LTO bit is set to ‘0’ by default at HV side power-on and this value must be kept also when the device is configured. No other setting is allowed for this bit. In case SAFE_OFF bit in CFG2 is set at ‘1’ the Soft turn-off function is used when SENSE or DESAT are triggered.

The OUT_DTth bit defines the OUT_{DT} parameter, which sets the deadtime duration between OUT1 and OUT2 (see Figure 11 and Figure 16):

Table 48. OUT_DTth

OUT_DTth	Dead time between OUT1 and OUT2 [ns]
0	55
1	88

9.2.5 CFG5 register (HV side)

The CFG5 register has the structure and default values in Table 49.

Table 49. CFG5 register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	-	-	-	-	2LTO_SOFTtime			
SoftReset/Reset	-	-	-	-	0101			

“SoftReset” is obtained by SPI SoftReset command.

“Reset” is obtained by power-on of the HV side.

If SOFTOFF feature is activated (SAFE_OFF=‘1’; SOFT_2LTO=‘0’) 2LTO_SOFTtime parameter sets the duration of the Soft turn-off after a DESAT/SENSE event (see Figure 35 and Figure 36), according to Table 50.

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Table 50. $t_{2LTO_SOFTtime}$ value

2LTO_SOFTtime [3..0]				Soft turn-off timeout [µs]
1	1	1	1	0.25
0	0	0	0	0.50
0	0	0	1	0.75
0	0	1	0	1.00
0	0	1	1	1.50
0	1	0	0	2.00
0	1	0	1	2.50
0	1	1	0	3.00
0	1	1	1	3.50
1	0	0	0	3.75
1	0	0	1	4.00
1	0	1	0	4.25
1	0	1	1	4.50
1	1	0	0	4.75
1	1	0	1	5.00
1	1	1	0	5.25

9.2.6 CFG6 register (LV side)

The CFG6 register has the structure and default values in Table 51.

Table 51. CFG6 register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CONTROLLER_FREQ		CRC_SPI	-	-	-	-	-
SoftReset/Reset	00		0					

“SoftReset” is obtained by SPI SoftReset command.

“Reset” is obtained by power-on of the LV side.

The CONTROLLER_FREQ parameter sets the main oscillator frequency of the internal PWM controller for the isolated flyback converter, according to Table 52.

Table 52. CONTROLLER_FREQ

CONTROLLER_FREQ [1..0]		Frequency [kHz]
0	0	400
0	1	200
1	0	300
1	1	600

The CRC_SPI bit enables the CRC check on the SPI communication protocol.

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Table 53. **CRC enable**

CRC_SPI	SPI communication protocol CRC enable
0	Disabled
1	Enabled

9.2.7 CFG7 register (HV side)

The CFG7 register has the structure and default values in Table 54.

Table 54. **CFG7 register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ADC_HIGHth			ADC_LOWth			ADC_EN	OFFMODE
SoftReset/Reset	000			000			0	1

“SoftReset” is obtained by SPI SoftReset command.
“Reset” is obtained by power-on of the HV side.
The ADC_HIGHth bits set the higher voltage level of the input signal dynamic range:

Table 55. **ADC_HIGHth**

ADC_HIGHth [2..0]			Higher voltage threshold for ADC input [V]
0	0	0	1.50
0	0	1	1.715
0	1	0	1.930
0	1	1	2.145
1	0	0	2.360
1	0	1	2.570
1	1	0	2.785
1	1	1	3.00

The ADC_LOWth bits set the lower voltage level of the input signal dynamic range:

Table 56. **ADC_LOWth**

ADC_LOWth [2..0]			Lower voltage threshold for ADC input [V]
0	0	0	0
0	0	1	0.215
0	1	0	0.430
0	1	1	0.645
1	0	0	0.855
1	0	1	1.070
1	1	0	1.285
1	1	1	1.500

The ADC_EN bit enables the analog measurement function, and so the periodic update of ADC register with internal ADC output code.

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Table 57. **Analog measurement function enable**

ADC_EN	Analog measurement function
0	Disabled
1	Enabled

The OFFMODE bit sets if the SOFTOFF MOSFET is activated in combination with OUT2 at every switching cycle or if remains off. This setting doesn't affect the behaviour of the pin 2LSO when the "Soft turn-off" is performed upon a DESAT or SENSE event.

Table 58. **SOFTOFF MOSFET activation**

OFFMODE	SOFTOFF MOSFET activation
0	Same time as OUT2
1	Remains OFF

9.2.8 STATUS1 register (HV side)

The STATUS1 is a read-only register. All flags are active high (high value indicates a fault/warning condition). The STATUS1 register has the structure in Table 59.

Table 59. **STATUS1 register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	OVLOH	OVLOL	DESAT_OC	SENSE_OC	UVLOH	UVLOL	TSD	STATUS1_BUSY
ClearStatus	0	0	0	0	0	0	0	X
SoftReset/Reset	0	0	0	0	0	0	0	X

"ClearStatus" is obtained by SPI ResetStatus command or by SDReset.

"SoftReset" is obtained by SPI SoftReset command.

"Reset" is obtained by power-on of the HV side.

When the ClearStatus, SoftReset or Reset are executed the state reported in the table is valid if no fault conditions are present, otherwise the related bit is overwritten according to the fault

When the Reset is executed the actual state can differ from the reported in the table depending on the slope of the supply voltage at the power-on.

A description of STATUS1 register bits is provided in Table 60.

Table 60. **STATUS1 register description**

Name	Bit	Fault	Latched	Force "SafeState"	Note
OVLOH	7	VH overvoltage flag. It is set high when VH is over $OVVH_{off}$ threshold.	Yes	Yes	
OVLOL	6	VL overvoltage flag. It is set high when VL is over $OVVL_{off}$ threshold.	Yes	Yes(1)	
DESAT_OC	5	Desaturation flag. It is set high when DESAT pin voltage reaches DESATth threshold.	Yes	Yes	

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Name	Bit	Fault	Latched	Force “SafeState”	Note
SENSE_OC	4	Sense flag. It is set high when SENSE pin voltage reaches $V_{SENSEth}$ threshold.	Yes	Yes	
UVLOH	3	VH undervoltage flag. It is set high when VH is below VHoff threshold.	Only when UVLOlatch is high	Yes	If not latched (UVLOlatch=0) returns low when VH is over VHon threshold
UVLOL	2	VL undervoltage flag. It is set high when VL is over VLoff threshold.	Only when UVLOlatch is high	Yes(1)	If not latched (UVLOlatch=0) returns low when VL is below VLon threshold
TSD	1	Thermal shutdown protection flag. It is set high when overtemperature shutdown threshold is reached.	No (fixed hysteresis)	Yes	
STATUS1_BUSY	0	This flag is set high if data obtained through SPI access to STATUS1 (bits 7-1) register are not valid.	No	No	The value of the flag is updated at every SPI Read of STATUS1

1. *If current device’s state is HW3PS and this fault is detected, device remains in HW3PS state.*

9.2.9 STATUS2 register (HV side)

The STATUS2 is a read-only register. All flags are active high (high value indicates a fault/warning condition). The STATUS2 register has the structure in Table 61.

Table 61. STATUS2 register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SAFESTATE	HVReset	-	TWN	PROGHV	REGERRR	COMERRR	STATUS2_BUSY
ClearStatus	0	0		0	X(1)	0(2)	0	X
SoftReset/Reset	1	1		0	1(3)	0	0(4)	X

1. *When a “Clearstatus” is executed PROGHV maintains the previous value.*
2. *If a REGGERRR fault has occurred the device configuration must be repeated.*
3. *If a HV side "Reset" occurs while the device is in Configuration Mode the PROGHV bit is set to 0 after the StopConfig command.*
4. *The value actually found depends also on the power-on timing of the LV side.*

“ClearStatus” is obtained by SPI ResetStatus command or by SDReset.

“SoftReset” is obtained by SPI SoftReset command.

“Reset” is obtained by power-on of the HV side.

When the ClearStatus, SoftReset or Reset are executed the state reported in the table is valid if no fault conditions are present otherwise the related bit is overwritten according to the fault.

When the Reset is executed the actual state can differ from that reported in the table depending on the slope of the supply voltage at the power-on.

A description of STATUS2 register bits is provided in Table 62.

Table 62. STATUS2 register description

Name	Bit	Fault/signal	Latched	Force “SafeState”	Note
SAFESTATE	7	The flag is set when HV is in SafeState. It is reset when HV exits from SafeState.	No	-	

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Name	Bit	Fault/signal	Latched	Force “SafeState”	Note
HVReset	6	Set high after a SoftReset/Reset of the HV side.	Yes	Yes	
-	5				
TWN	4	Thermal warning flag. It is set high when overtemperature warning threshold is reached.	No (fixed hysteresis)	No	
PROGHV	3	PROGHV Flag is set high after a SoftReset/Reset or when a StartConfig is correctly received. It is set low when the device is in Configuration mode and the HV side receives a StopConfig command. When this flag is high, it is not set low by the ClearStatus commands.	No	No	
REGERRR	2	It is set high when one or more misalignments have been found in the HV configuration registers.	Yes	Yes	The device configuration must be repeated.
COMERRR	1	Communication error on HV side. It is set high when HV side does not receive any response from LV side (e.g. 3V3IN supply is not provided) within HV WATCHDOG time frame.	Yes	SafeState or HW3PS state is forced, depending on DEFAULT pin’s state.(1)	
STATUS2_BUSY	0	This flag is set high if data obtained through SPI access to STATUS2 register (bits 7-1) are not valid.	No	No	The value of the flag is updated at every SPI Read of STATUS2.

1. *If current device’s state is HW3PS and this fault is detected, device remains in HW3PS state.*

9.2.10 STATUS3 register (LV side)

The STATUS3 is a read-only register. All flags are active high (high value indicates a fault condition). The STATUS3 register has the structure in Table 63.

Table 63. STATUS3 register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	UVLO_3V3IN	UVLO_VCC		DT_ERR	SPI_ERR	-	PROGLV	FLYBACK_FAULT
ClearStatus	0	0	-	0	0	X	X(1)	0
SoftReset/Reset	0	0	-	0	0	X	1	0

1. *When a “Clearstatus” is executed PROGLV maintains the previous value.*

“ClearStatus” is obtained by SPI ResetStatus command or by SDReset.

“SoftReset” is obtained by SPI SoftReset command.

“Reset” is obtained by power-on of the LV side.

When the ClearStatus, SoftReset or Reset are executed the state reported in the table is valid if no fault conditions are present, otherwise the related bit is overwritten according to the fault.

When the Reset is executed the actual state can differ from that reported in the table depending on the slope of the supply voltage at the power-on.

A description of STATUS3 register bits is provided in Table 64.

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Table 64. **STATUS3 register description**

Name	Bit	Fault/signal	Latched	Force “SafeState”	Note
UVLO_3V3IN	7	3V3IN undervoltage flag. It is set high when 3V3IN supply is in UVLO condition.	Yes	Yes	
UVLO_VCC	6	VCC undervoltage flag. It is set high when VCC supply is in UVLO condition. Flyback controller is stopped.	No	No	This fault is not reported when the LV side is in UVLO_3V3IN condition.
-	5				
DT_ERR	4	Deadtime error flag. This bit is set high when a violation of internal DT is detected.	Yes	No	
SPI_ERR	3	SPI communication error flag. It is set high when the SPI communication fails cause: • Wrong CRC check • Wrong number of CK rising edges • Attempt to execute a not-allowed command • Attempt to execute a command not listed in Table 17 • Programming procedure is not correctly performed • Attempt to read or write at a not-available address	Yes	No	
-	2				
PROGLV	1	PROGLV Flag is set high after a SoftReset/ Reset or when a StartConfig is correctly received. It is set low when the LV side correctly receives a StopConfig command if the configuration procedure ends correctly. When this flag is set high, it is not set low by the ClearStatus commands. It can be set low only by completing a configuration.	No	No	
FLYBACK _FLT	0	Flyback controller fault. It is set high when the flyback controller is in fault condition.	No	No	See details in Section 6.2.11

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9.2.11 STATUS4 register (LV side)

The STATUS4 is a read-only register. All flags are active high (high value indicates a fault condition). The STATUS4 register has the structure in Table 65.

Table 65. STATUS4 register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	-	PWM_LV	ASC_LEVEL_LV	GATE_LEVEL_LV	LVReset	REGERRL	COMERRL	SPI_HVbusy
ClearStatus		x(1)	x(1)	x(1)	0	0(2)	0	0
SoftReset/Reset		0	0	0	1	0	0(3)	0

1. *When a "Clearstatus" is executed GATE_LEVEL_LV, PWM_LV, ASC_LV maintain their current values.*
2. *If a REGGERRL fault has occurred the device configuration must be repeated.*
3. *The value actually found depends also on the power-on timing of the HV side.*

"ClearStatus" is obtained by SPI ResetStatus command or by SDReset.

"SoftReset" is obtained by SPI SoftReset command.

"Reset" is obtained by power-on of the LV side.

When the ClearStatus, SoftReset or Reset are executed the state reported in the table is valid if no fault conditions are present, otherwise the related bit is overwritten according to the fault.

When the Reset is executed the actual state can differ from that reported in the table depending on the slope of the supply voltage at the power-on.

A description of STATUS4 register bits is provided in Table 66.

Table 66. STATUS4 register description

Name	Bit	Fault/signal	Latched	Force "SafeState"	Note
-	7		-	-	
PWM_LV	6	PWM command flag. The flag is set according to the last PWM command correctly received by HV side. Flag is '1' for ON command Flag is '0' for OFF command	No	No	
ASC_LEVEL_LV	5	ASC pin status. When ASC pin is high the flag reports '1', otherwise it is '0'.	No	No	
GATE_LEVEL_LV	4	GATE status flag, monitor of the voltage on GATE pin. It is the output of a comparator with an hysteresis equal to V_{GATEth_ON} - V_{GATEth_OFF}. Specifically: • GATE_LEVEL_LV is set high when GATE is rising and overcome V_{GATEth_ON} threshold. • GATE_LEVEL_LV is set low when GATE is falling and it goes below V_{GATEth_OFF} threshold.	No	No	
LVReset	3	Set high after a SoftReset/Reset of the LV side.	Yes	Yes(1)	See details in Section 6.4.
REGERRL	2	It is set high when one or more misalignments have been found in the LV configuration registers.	Yes	Yes(1)	The device configuration must be repeated.

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Name	Bit	Fault/signal	Latched	Force “SafeState”	Note
COMERRL	1	Communication error on LV side. It is set high when LV side does not receive any response from HV side (e.g. VH supply is not provided) within HV WATCHDOG time frame.	Yes	No	If set, after HV WATCHDOG time, HV side enters in HW3PS or SAFESTATE based on DEFAULT pin.
SPI_HVbusy	0	The flag is set high if the data received through an SPI access to the HV configuration registers are not valid (CFGx, DIAGxCFGx, TEST1).	Yes	No	

1. *If current device’s state is HW3PS and this fault is detected, device remains in HW3PS state.*

9.2.12 STATUS5 register (LV side)

The STATUS5 is a read-only register and has the structure reported in Table 67.

Table 67. STATUS5 register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ADC							
ClearStatus	X	X	X	X	X	X	X	X
SoftReset/Reset	1	1	1	1	1	1	1	1

“ClearStatus” is obtained by SPI ResetStatus command or by SDReset.
“SoftReset” is obtained by SPI SoftReset command.
“Reset” is obtained by power-on of the LV side.
After the “ClearStatus” execution if ADC_EN=1 the value is the ADC converted data, otherwise it is 0xFF.
After the “SoftReset”/”Reset” execution if ADC_EN=1 the value is overwritten with the ADC converted data.
A description of STATUS5 register bits is provided in Table 68 .

Table 68. STATUS5 register description

Name	Bit	Information	Latched	Force “SafeState”	Note
ADC	7-0	ADC output data bits.	No	No	

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9.2.13 TEST1 register (HV side)

The TEST1 register has the structure reported in Table 69

Table 69. TEST1 register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ADCCHK	RSNSCHK	SNSCHK	MCPCHK	DESCHK	DEFAULTCHK	OUT1OUT2CHK	GATECHK
SoftReset/Reset	0	0	0	0	0	0	0	0

According to Table 70, setting one check bit of the register enables the related check mode:

Table 70. Check mode

Name	Bit	Fault/signal
ADC_CHK	7	ADC functionality
RSNSCHK	6	SENSE resistor
SNSCHK	5	SENSE comparator
MCPCHK	4	MILLER clamp driver
DESCHK	3	DESAT functionality
DEFAULTCHK	2	DEFAULT pin function
OUT1OUT2CHK	1	OUT1/OUT2 to gate path
GATECHK	0	DEFAULT pin function – test type definition

9.2.14 DIAGxCFGA and DIAGxCFGB registers

$\overline{\text{DIAG1}}$ and $\overline{\text{DIAG2}}$ fault pins can be independently associated to up to 16 different diagnostics or faults.

$\overline{\text{DIAG1}}$ configuration can be done setting DIAG1CFGA and DIAG1CFGB registers, which have the structure described in Table 71 and Table 72.

If a bit in DIAG1CFGA or DIAG1CFGB register is set high, the corresponding event turns on the $\overline{\text{DIAG1}}$ open-drain MOSFET.

Table 71. DIAG1CFGA register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DIAG1CFGA_7	DIAG1CFGA_6	DIAG1CFGA_5	DIAG1CFGA_4	DIAG1CFGA_3	DIAG1CFGA_2	DIAG1CFGA_1	DIAG1CFGA_0
SoftReset/Reset	0	1	0	1	0	0	0	0

Table 72. DIAG1CFGB register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DIAG1CFGB_7	DIAG1CFGB_6	DIAG1CFGB_5	DIAG1CFGB_4	DIAG1CFGB_3	DIAG1CFGB_2	DIAG1CFGB_1	DIAG1CFGB_0
SoftReset/Reset	0	1	0	0	1	0	0	0

$\overline{\text{DIAG2}}$ configuration can be done setting DIAG2CFGA and DIAG2CFGB registers, which have the structure described in Table 73 and Table 74.

If a bit in DIAG2CFGA or DIAG2CFGB register is set high, the corresponding events turn on the $\overline{\text{DIAG2}}$ open-drain MOSFET.

Table 73. DIAG2CFGA register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DIAG2CFGA_7	DIAG2CFGA_6	DIAG2CFGA_5	DIAG2CFGA_4	DIAG2CFGA_3	DIAG2CFGA_2	DIAG2CFGA_1	DIAG2CFGA_0

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	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SoftReset/Reset	0	0	1	0	1	1	0	1

Table 74. DIAG2CFGB register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DIAG2CFGB_7	DIAG2CFGB_6	DIAG2CFGB_5	DIAG2CFGB_4	DIAG2CFGB_3	DIAG2CFGB_2	DIAG2CFGB_1	DIAG2CFGB_0
SoftReset/Reset	1	0	0	0	0	0	1	1

The relation between DIAGxCFGA and DIAGxCFGB registers bits and fault events is described in Table 75 and Table 76.

Table 75. DIAG1CFGA and DIAG2CFGA registers

DIAGxCFGA bit #	Fault/status	Status register bit
0	Communication error on HV side	COMERRR
1	Overvoltage on VH or VL	OVLOH, OVLOL
2	Undervoltage on VH or VL	UVLOH, UVLOL
3	Register or configuration error on HV side	REGERRR
4	HV side reset	HVRESET
5	Thermal shutdown, thermal warning	TSD, TWN
6	Desaturation Detection	DESAT_OC
7	SENSE detection	SENSE_OC

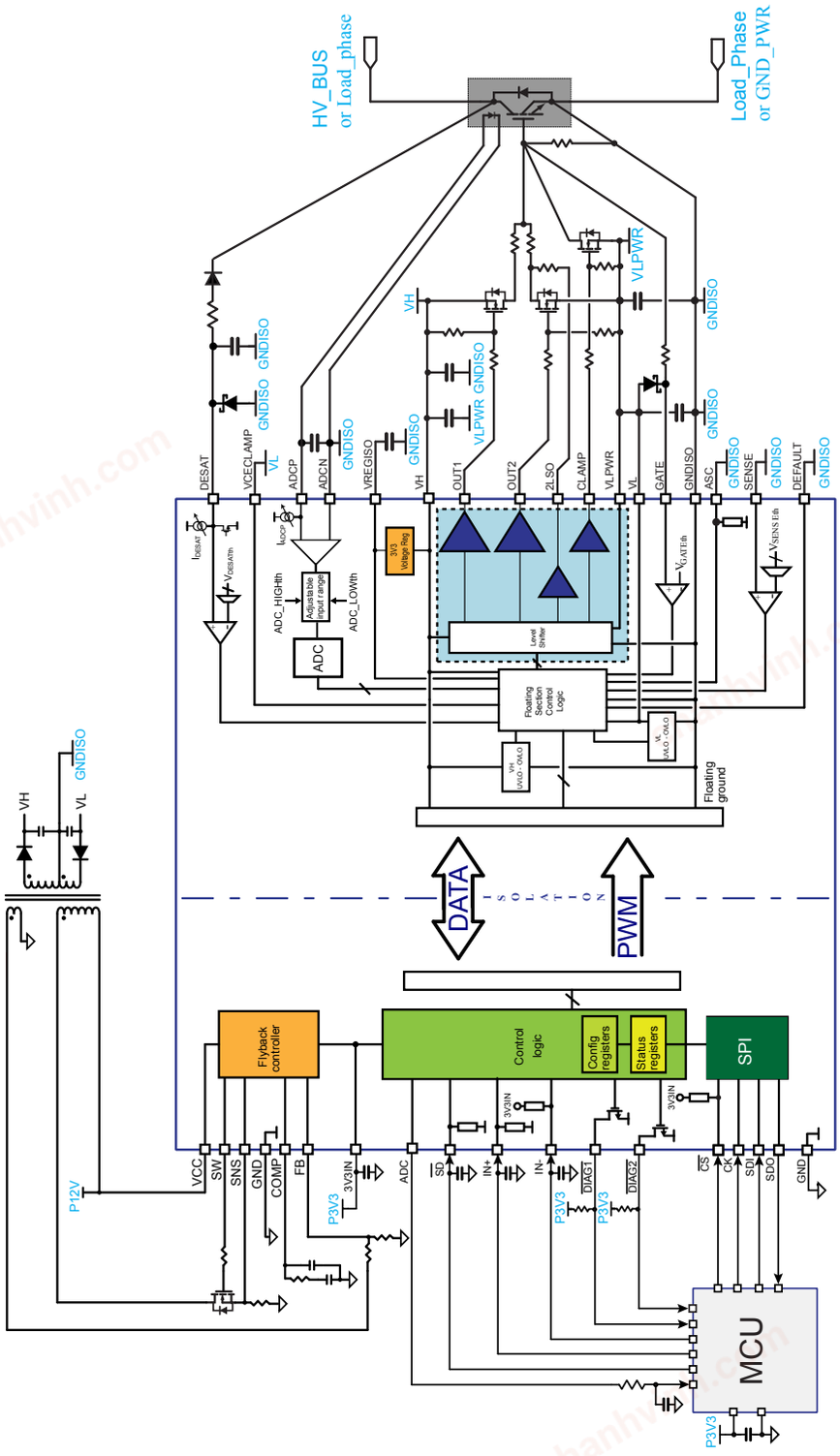
Table 76. DIAG1CFGB and DIAG2CFGB registers

DIAGxCFGB bit #	Fault	Status register bit
0	Register or configuration error on LV	REGERRL
1	Communication error on LV side	COMERRL
2	Deadtime violation	DT_ERR
3	SPI communication error	SPI_ERR
4	Gate level	GATE_LEVEL_LV
5	ASC level	ASC_LEVEL_LV
6	LV side reset	LVRESET
7	Flyback fault, UVLO on VCC, UVLO on 3V3IN	FLYBACK_FLT, UVLO_VCC, UVLO_3V3IN

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10 Typical application diagram

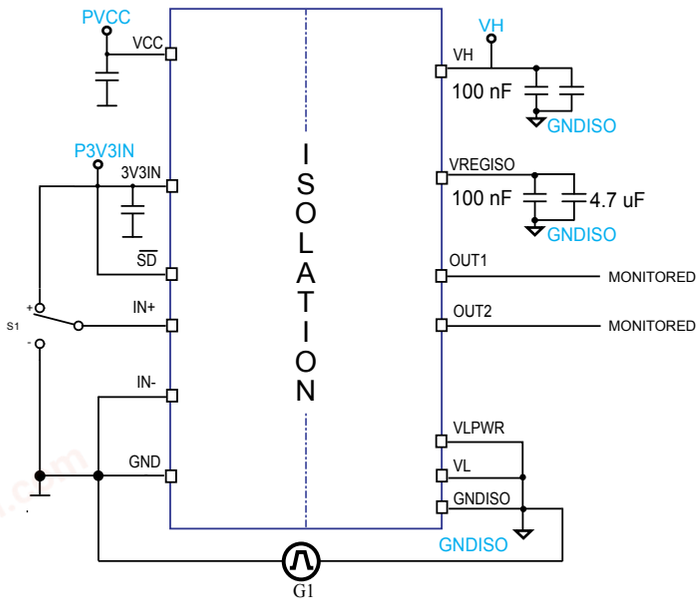
Figure 48. **Typical application diagram**



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11 Testing and characterization information

Figure 49. **CMTI test circuit**



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12 Package information

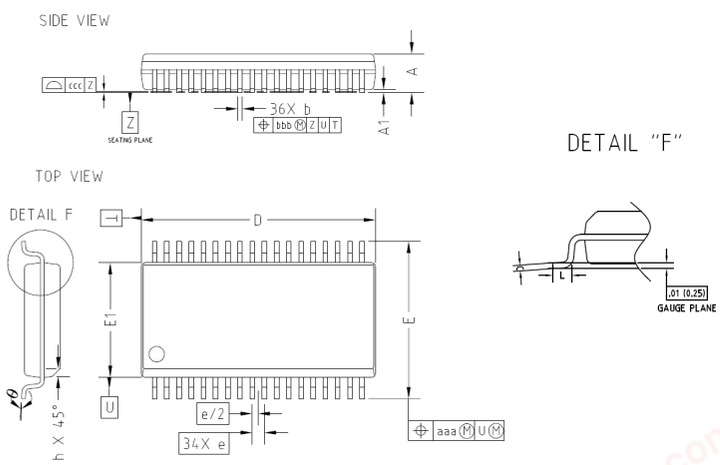
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

12.1 SO-36W package information

Table 77. SO-36W package dimensions

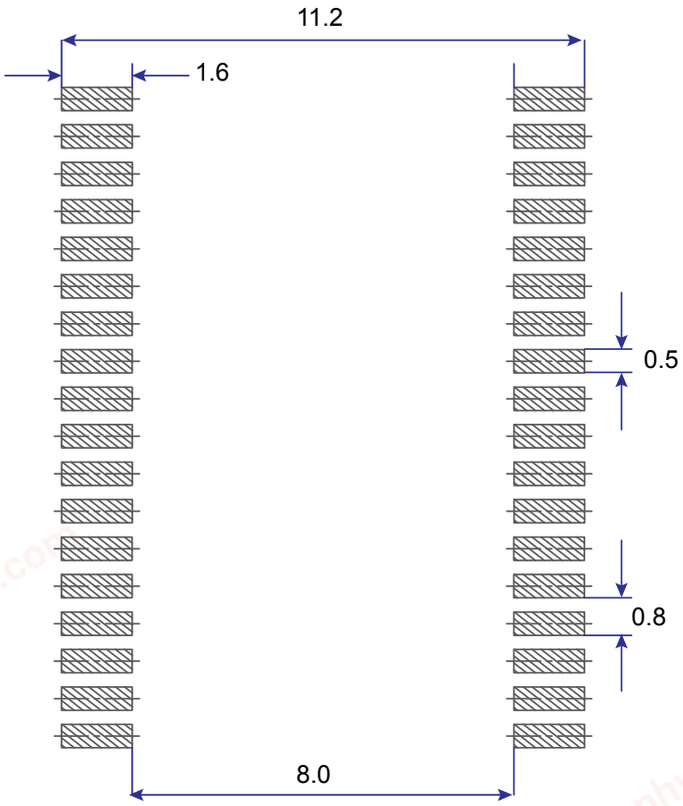
Symbol	Dimensions (mm)/Angles(Degree)			NOTES
	Min.	Typ.	Max.	
A			2.65	
A1	0.1		0.3	
b	0.25		0.35	
c	0.20		0.33	
D	15.20		15.60	
E1	7.40		7.60	
E	10.05		10.65	
e		0.8 BSC		
L	0.61		0.91	
h	0.25		0.75	
θ	0°		8°	
aaa		0.25		
bbb		0.25		
ccc		0.1		

Figure 50. SO-36W mechanical data



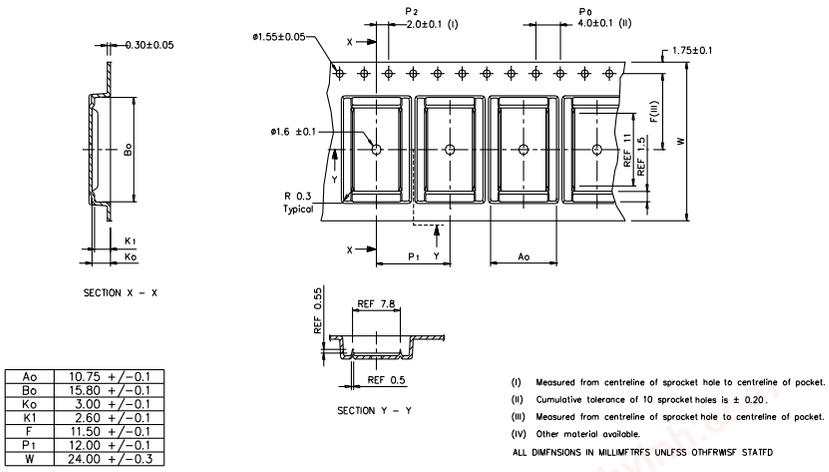
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Figure 51. **SO-36W suggested land pattern**



12.2 Tape and reel

Figure 52. **Carrier Tapes dimensions**



Ao	10.75 +/−0.1
Bo	15.80 +/−0.1
Ko	3.00 +/−0.1
K1	2.60 +/−0.1
F	11.50 +/−0.1
P1	12.00 +/−0.1
W	24.00 +/−0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

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Figure 53. **Reel dimensions**

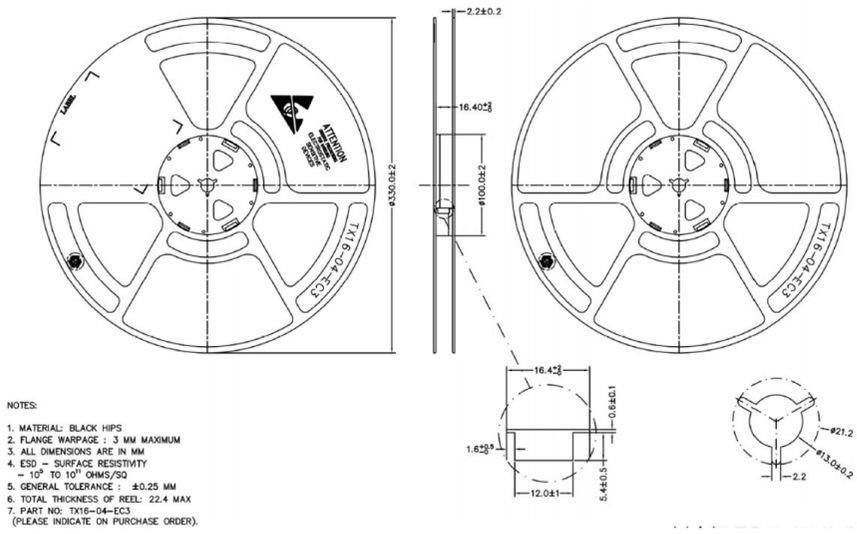
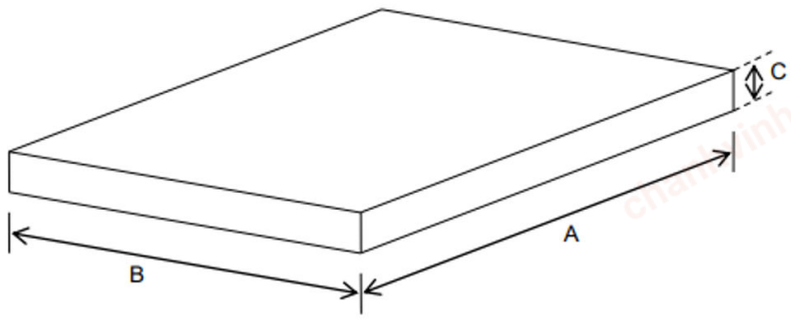


Figure 54. **Box dimensions**



Material code	A ± 2mm	B ± 2mm	C ± 2mm	Reel diameter	Reel width	Internal coating
3CP71972	340	340	340	13"	8,12,16,24	No carbon coating

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13 Ordering information

Table 78. **Order codes**

Order code	Package	Package marking	Packaging
STGAP4S	SO-36W	STGAP4S	Tube
STGAP4STR	SO-36W	STGAP4S	Tape and reel

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Revision history

Table 79. **Document revision history**

Date	Version	Changes
21-Dec-2021	1	Initial release.
26-Apr-2022	2	Added AEC-Q100 qualification, Typo correction in STATUS4.SPI_HVBusy: Latched = Yes, Added V_{DIAGx} to Table 4, Added Section 6.2.11 Flyback fault diagnostic, Added Section 7.2 Logic I/O interface to 5V logic signals
26-Ott-2022	3	Added descriptions in Section 7, Section 9. Modified description in Section 7.4, Section 7.13,Section 7.11,Section 7.12,Section 6.2.7,Table 64. Updated N_{UVP} parameter in Section 4.2 Typo correction in STAUS3.UVLO_3V3IN: Force SafeState = Yes, Figure 46, Figure 35. Added GATE, VREGISO to Table 4.
09-Mar-2023	4	Updated Figure 9, Figure 39, Figure 48, Figure 49; Updated VDE standard in Table 8; Modified description in Section 7.4; Added description in Section 7.15

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