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STGAP2SiCD

Datasheet

Galvanically isolated 4 A dual gate driver



Features

- High voltage rail up to 1200 V
- Driver current capability: 4 A sink/source @ 25 °C
- dV/dt transient immunity ±100 V/ns
- Overall input-output propagation delay: 75 ns
- Separate sink and source option for easy gate driving configuration
- 4 A Miller CLAMP
- UVLO function
- Configurable interlocking function
- Dedicated SD and BRAKE pins
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shutdown protection
- Standby function
- 6 kV galvanic isolation
- Wide Body SO-36W
- UL 1577 recognized

Application

- Motor driver for industrial drives, factory automation, home appliances and fans
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

Product status link
STGAP2SiCD

Product label
SUSTAINABLE TECHNOLOGY

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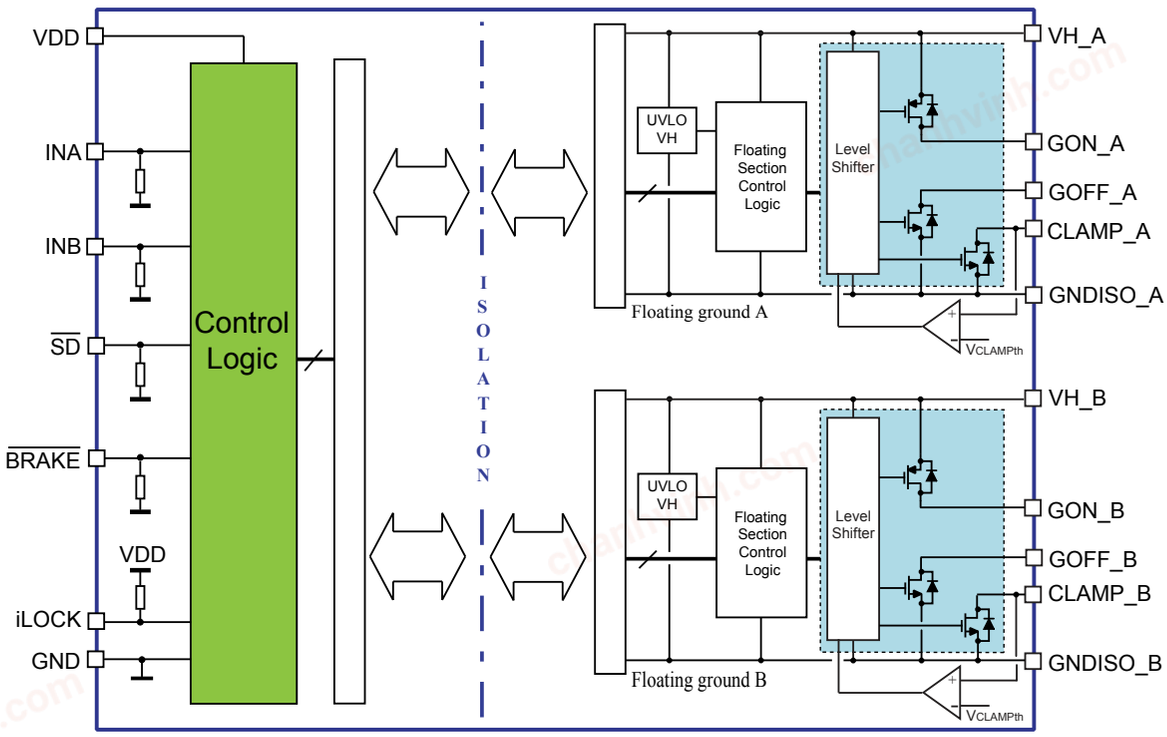
Description

The STGAP2SiCD is a dual gate driver for SiC MOSFETs which provides galvanic isolation between each gate driving channel and the low voltage control and interface circuitry. The gate driver is characterized by 4 A current capability and rail-to-rail outputs, making it suitable for mid and high power applications such as power conversion and industrial motor drivers inverters. The separated output pins allow to independently optimize turn-on and turn-off by using dedicated gate resistors, while the Miller CLAMP function allows avoiding gate spikes during fast commutations in half-bridge topologies. The device integrates protection functions: dedicated SD and BRAKE pins are available, UVLO and thermal shutdown are included to easily design high reliability systems. In half-bridge topologies the interlocking function prevents outputs from being high at the same time, avoiding shoot-through conditions in case of wrong logic input commands. The interlocking function can be disabled by a dedicated configuration pin, allowing independent and parallel operation of the two channels. The input to output propagation delay results are contained within 75 ns, providing high PWM control accuracy. A standby mode is available in order to reduce idle power consumption.

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1 Block diagram

Figure 1. **Block diagram**



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2 Pin description and connection diagram

Figure 2. **Pin connection (top view)**

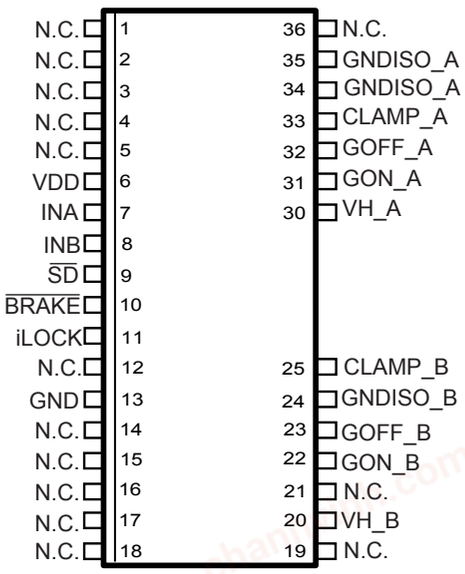


Table 1. **Pin description**

Pin number	Pin name	Type	Function
6	VDD	Power supply	Control logic supply voltage
7	INA	Logic input	Control logic input for Channel A, active high
8	INB	Logic input	Control logic input for Channel B, active high
9	$\overline{SD}$	Logic input	Shutdown input, active low
10	$\overline{BRAKE}$	Logic input	Control logic input, active low
11	iLOCK	Analog input	Interlocking enable/disable
13	GND	Power supply	Control logic ground
20	VH_B	Power supply	Channel B gate driving positive supply
22	GON_B	Analog output	Channel B Source output
25	CLAMP_B	Analog output	Channel B Miller Clamp
23	GOFF_B	Analog output	Channel B Sink output
24	GNDISO_B	Power supply	Channel B gate driving isolated ground
30	VH_A	Power supply	Channel A gate driving positive supply
31	GON_A	Analog output	Channel A Source output
33	CLAMP_A	Analog output	Channel A Miller Clamp
32	GOFF_A	Analog output	Channel A Sink output
34, 35	GNDISO_A (1)	Power supply	Channel A gate driving isolated ground
1, 2, 3, 4, 5, 12, 14, 15, 16, 17, 18	N.C.	Not connected.	

1. *Both GNDISO_A pins must be connected and shorted together.*

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3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND		-0.3	6.5	V
V_{LOGIC}	Logic pins voltage vs. GND		-0.3	6.5	V
iLOCK	Interlocking Enable vs. GND		-0.3	VDD + 0.3	V
VH_x	Positive supply voltage (VH_x vs GNDISO_x)		-0.3	28	V
V_{OUT}	Voltage on gate driver outputs (GON_x , GOFF_x , CLAMP_x vs GNDISO_x)		-0.3	VH_x + 0.3	V
T_J	Junction temperature		-40	150	°C
T_S	Storage temperature		-50	150	°C
ESD	HBM (human body model)		2		kV

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	SO-36W	52	°C/W

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3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND		3.1	5.5	V
VLOGIC	Logic pins voltage vs. GND		0	5.5	V
iLOCK	Interlocking Enable vs. GND		0	VDD	V
VH_x	Positive supply voltage (VH_x vs. GNDISO_x)			26	V
$GNDISO_{A-B}$(1)	Floating grounds differential voltage (GNDISO_A - GNDISO_B)		-1700	+1700	V
V_{IORM}	Primary to secondary ground (GND - GNDISO_A); (GND - GNDISO_B)		-1200	+1200	V
F_{SW}	Maximum switching frequency(2)			1	MHz
t_{OUT}	Output pulse width		100		ns
T_J	Operating junction temperature		-40	125	°C

1. *Characterization data, 1200 V max. tested in production.*
2. *Actual limit depends on power dissipation and T_J.*

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4 Electrical characteristics

Table 5. Electrical characteristics (T_J = 25 °C, VH_x = 18 V, VDD = 5 V unless otherwise specified)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics							
t_{Don}	INA, INB, SD, BRAKE	Input to output propagation delay ON	See Figure 8	50	75	90	ns
t_{Doff}	INA, INB, SD, BRAKE	Input to output propagation delay OFF	See Figure 8	50	75	90	ns
t_r		Rise time	C_L = 4.7 nF, See Figure 8		30		ns
t_f		Fall time			30		ns
MT		Matching time (1)				20	ns
$t_{deglitch}$	INA, INB, SD, BRAKE	Inputs deglitch filter			20	40	ns
CMTI(2)		Common-mode transient immunity, $\|dV_{ISO}/dt\|$	V_{CM} = 1500 V, see Figure 9	100			V/ns
Supply voltage							
VH_{on}		VH_x UVLO turn-on threshold		14.6	15.5	16.4	V
VH_{off}		VH_x UVLO turn-off threshold		13.9	14.8	15.7	V
V_{Hhyst}		VH_x UVLO hysteresis		600	750	950	mV
I_{QHU_A} I_{QHU_B}		VH undervoltage quiescent supply current	VH = 7 V		1.3	1.8	mA
I_{QH_A} I_{QH_B}		VH_x quiescent supply current			1.3	1.8	mA
I_{QHSBY_A} I_{QHSBY_B}		Standby VH_x quiescent supply current			400	550	µA
SafeClp		GOFF active clamp	I_{GOFF} = 0.2 A; VH floating		2	2.3	V
I_{QDD}		VDD quiescent supply current			1.8	2.4	mA
I_{QDDSBY}		Standby VDD quiescent supply current	Standby mode		40	80	µA
Logic Inputs							
V_{il}	INA, INB, SD, BRAKE	High level logic threshold voltage		0.29·VDD	0.33·VDD	0.37·VDD	V
V_{ih}	INA, INB, SD, BRAKE	Low level logic threshold voltage		0.62·VDD	0.66·VDD	0.72·VDD	V
I_{logic_h}	INA, INB, SD, BRAKE	Logic inputs high level input bias current	V_{logic} = 5 V	33	50	70	µA
I_{logic_l}	INA, INB, SD, BRAKE	Logic inputs low level input bias current	V_{logic} = 0 V			1	µA
R_{pd}	INA, INB, SD, BRAKE	Logic inputs pull-down resistor		70	100	150	kΩ
Interlocking							
iLOCKen	iLOCK	Interlockng enable voltage		0.7·VDD			V

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Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$iLOCK_{_h}$	iLOCK	iLOCK high level bias current	iLOCK = VDD			1	µA
$iLOCK_{_l}$	iLOCK	iLOCK low level bias current	iLOCK = GND	35	55	75	µA
$iLOCK_{_pu}$	iLOCK	iLOCK pull-up resistor		66	90	142	kΩ
Driver buffer section							
I_{GON}		Source short-circuit current	T_J = 25°C		4		A
			T_J = -40 / +125°C (2)	3		5	
V_{GONH}		Source output high level voltage	I_{GON} = 100 mA	VH-0.15	VH-0.12		V
R_{GON}		Source R_{DS_ON}	IG_{ON} = 100 mA		1.25	1.5	Ω
I_{GOFF}		Sink short-circuit current	T_J = 25°C		4		A
			T_J = -40 / +125°C (2)	3		5.5	
V_{GOFFL}		Sink output low level voltage	I_{GOFF} = 100 mA		110	120	mV
R_{GOFF}		Sink R_{DS_ON}	I_{GOFF} = 100 mA		1.1	1.2	Ω
Miller Clamp							
$V_{CLAMPth}$		CLAMP voltage threshold	V_{CLAMP} vs. GNDISO	1.3	2	2.6	V
I_{CLAMP}		CLAMP short-circuit current	V_{CLAMP} = 15 V				A
			T_J = 25°C		4		
			T_J = -40 ÷ +125°C (2)	2		5	
V_{CLAMP_L}		CLAMP low level output voltage	I_{CLAMP} = 100 mA		96	115	mV
R_{CLAMP}		CLAMP R_{DS_ON}	I_{CLAMP} = 100 mA		0.96	1.15	Ω
Overtemperature protection							
T_{SD}		Shutdown temperature (2)		170			°C
T_{hys}		Temperature hysteresis (2)			20		°C
Standby							
t_{STBY}		Standby time	See Section 6.3	200	280	500	µs
t_{WUP}		Wake-up time	See Section 6.3	10	20	35	µs
t_{awake}		Wake-up delay	See Section 6.3	90	140	200	µs
$t_{stbyfilt}$		Standby filter	See Section 6.3	200	280	800	ns

1. *MT = max ($|t_{Don(A)} - t_{Don(B)}|$, $|t_{Doff(A)} - t_{Doff(B)}|$, $|t_{Doff(A)} - t_{Don(B)}|$, $|t_{Doff(B)} - t_{Don(A)}|$)*
2. *Characterization data, not tested in production.*

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5 Isolation

Table 6. Isolation and safety-related specifications

Parameter	Symbol	Value	Unit	Conditions
Clearance (Minimum External Air Gap)	CLR	8	mm	Measured from input terminals to output terminals, shortest distance through air
Creepage (*) (Minimum External Tracking)	CPG	8	mm	Measured from input terminals to output terminals, shortest distance path along body
Comparative Tracking Index (Tracking Resistance)	CTI	≥ 400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 7. Isolation characteristics

Parameter	Symbol	Test Conditions	Characteristic	Unit
Maximum Working Isolation Voltage	V_{IORM}		1200	V_{PEAK}
Input to Output test voltage In accordance with VDE 0884-11	V_{PR}	Method a, Type test	1920	V_{PEAK}
		$V_{PR} = V_{IORM} \times 1.6$, $t_m = 10$ s		
		Partial discharge < 5 pC		
		Method b1, 100 % Production test	2250	V_{PEAK}
		$V_{PR} = V_{IORM} \times 1.875$, $t_m = 1$ s		
		Partial discharge < 5 pC		
Transient Overvoltage (Highest Allowable Overvoltage)	V_{IOTM}	$t_{ini} = 60$ s Type test	6000	V_{PEAK}
Maximum Surge Test Voltage	V_{IOSM}	Type test	6000	V_{PEAK}
Isolation Resistance	R_{IO}	V_{IO} = 500 V; Type test	$>10^9$	Ω

Table 8. Isolation voltage as per UL 1577

Description	Symbol	Characteristic	Unit
Isolation Withstand Voltage, 1min (Type test)	V_{ISO}	3535/5000	V_{rms}/ PEAK
Isolation Test Voltage, 1sec (100% production)	$V_{ISOtest}$	4242/6000	V_{rms}/ PEAK

Recognized under the UL 1577 Component Recognition Program - file number E362869

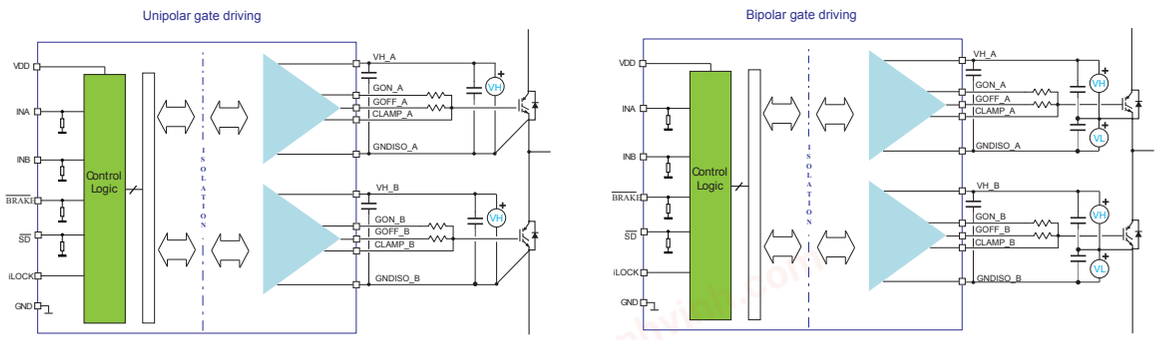
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6 Functional description

6.1 Gate driving power supply and UVLO

The STGAP2SiCD is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows to implement either unipolar or bipolar gate driving.

Figure 3. Power supply configuration for unipolar and bipolar gate driving



Undervoltage protection is available on VH_x supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH_x voltage goes below the VH_{off} threshold, the output buffer goes into “safe state”. When VH_x voltage reaches the VH_{on} threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH_x supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors, which are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value in the range between 1 µF and 10 µF should be placed close to it.

6.2 Power-up, power-down and ‘safe state’

The following conditions define the “safe state”:

- GOFF = ON state
- GON = high impedance

Such conditions are maintained at power-up of the isolated side (VH_x < VH_{on}) and during whole device power-down phase (VH < VH_{off}), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If VH_x positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in safe state, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage side the device output state depends on the input pins' status.

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6.3 Control Inputs

The device is controlled through the following logic inputs:

- SD: active low shutdown input;
- BRAKE: active low brake input;
- INA, INB: active high logic inputs for channel A and channel B driver outputs;
- iLOCK: used to enable or disable the interlocking protection.

The operation of the driver IOs is described in Table 9.

Table 9. Inputs truth table (applicable when device is not in UVLO or "safe state")

	Input pins(1)					Output pins	
	iLOCK	**SD**	**BRAKE**	**INA**	**INB**	**GOUT_A**	**GOUT_B**
	X	L	X	X	X	Low	Low
	X	H	L	X	X	Low	**HIGH**
	X	H	H	L	L	Low	Low
	X	H	H	H	L	**HIGH**	Low
	X	H	H	L	H	Low	**HIGH**
Interlocking	VDD	H	H	H	H	Low	Low
	GND	H	H	H	H	**HIGH**	**HIGH**

1. *X: Don't care*

A deglitch filter allows input signals with duration shorter than $t_{deglitch}$ to be ignored, thereby preventing noise spikes potentially present in the application from generating unwanted commutations.

6.4 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced into "safe state" until communication link is properly established again.

6.5 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the TSD temperature threshold, the device is forced into "safe state". The device operation is restored as soon as the junction temperature is lower than TSD - Thys.

6.6 Standby function

In order to reduce the power consumption of both control interface and gate driving sides the device can be put in standby mode. In standby mode the quiescent current from VDD and VH_x supply pins is reduced to I_{QDDS} and I_{QHS_x} respectively, and the output remains in 'safe state' (the output is actively forced low).

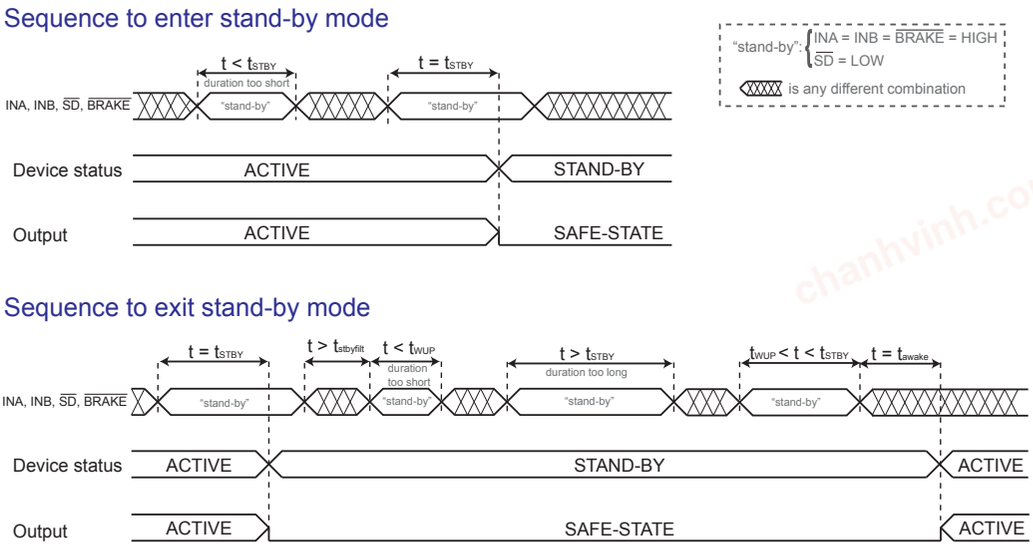
The way to enter standby is to keep the SD low while keeping the other input pins (INA, INB and BRAKE) high ("standby" value) for a time longer than t_{STBY}. During standby the inputs can change from the "standby" value.

To exit standby, inputs must be put in any combination different from the "standby" value for a time longer than $t_{stbyfilt}$, and then in the "standby" value for a time t such that $t_{WUP} < t < t_{STBY}$.

When the input configuration is changed from the "standby" value the output is enabled and set according to inputs state after a time t_{awake}.

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Figure 4. **Standby state sequences**



6.7 Interlocking function

The interlocking function prevents outputs GOUT_A and GOUT_B from being high at the same time, regardless of the status of the input pins INA and INB. In half-bridge topologies this protection avoids shoot-through in case wrong input signals are generated by the controller device. If the status of INA and INB is such to require both channels to be ON at the same time, the driver turns both channels off. In some topologies it is required to allow both channels to be ON at the same time: this can be achieved by disabling the interlocking function trough the iLOCK pin. The iLOCK pin is either connected to VDD, which enables the interlocking function, or to GND, which disables the interlocking function and allows parallel operation of Channel_A and Channel_B. Refer to Control Inputs for complete logic inputs truth table.

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7 Typical application diagram

Figure 5. Typical application diagram – Half-bridge configuration

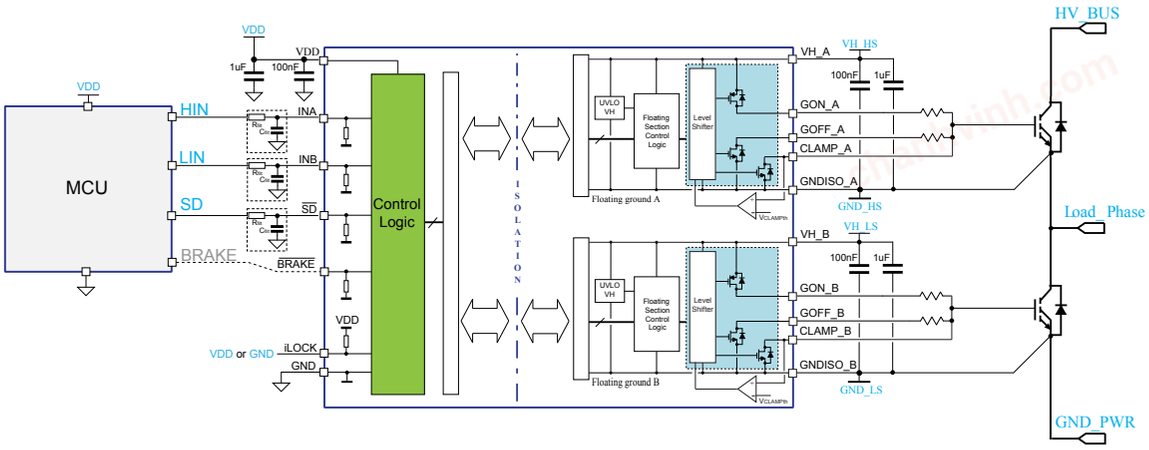
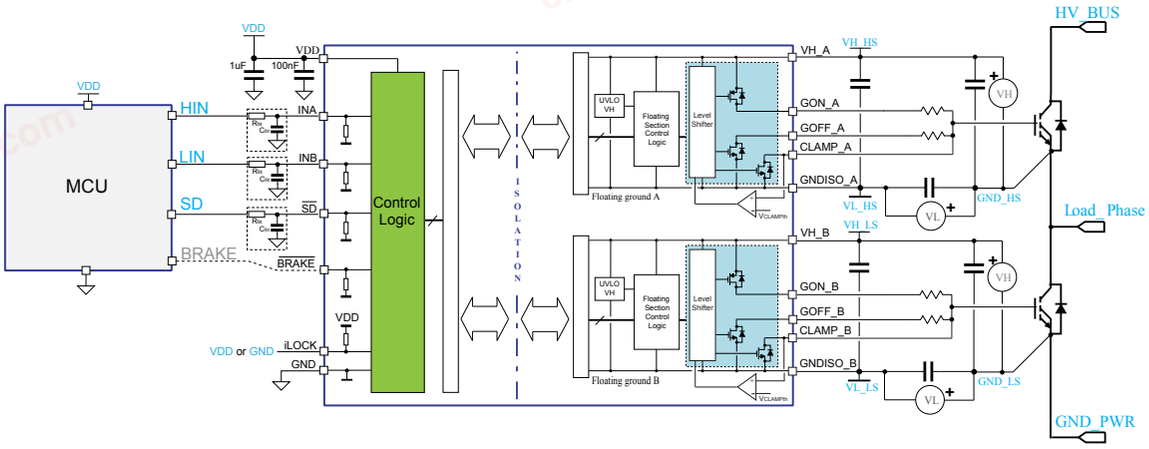


Figure 6. Typical application diagram – Half-bridge configuration with negative gate driving



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8 Layout

8.1 Layout guidelines and considerations

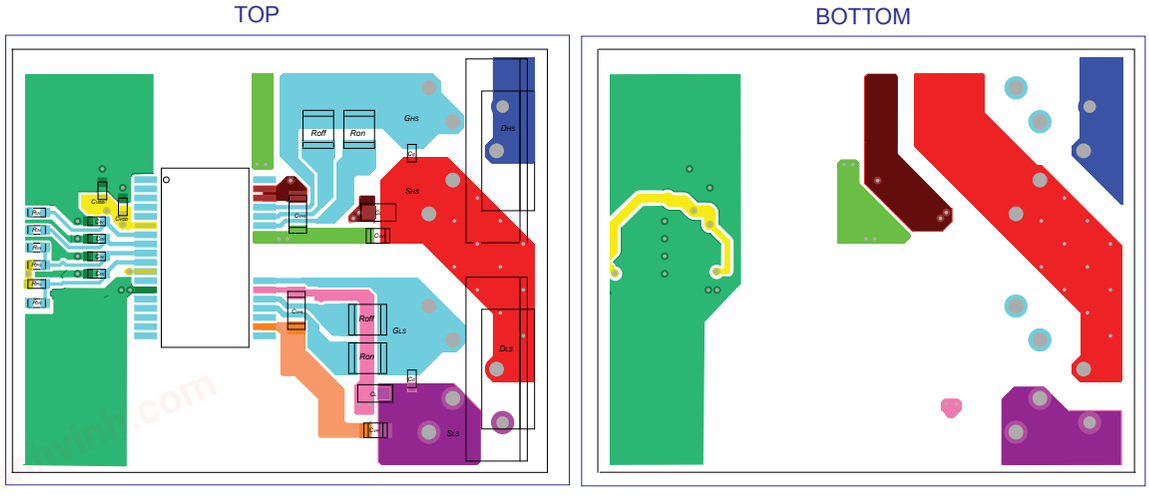
In order to optimize the PCB layout, the following considerations should be taken into account:

- SMD ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pin. A 100 nF capacitor must be placed between VDD and GND and between VH_x and GNDISO_x, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current a second capacitor with value in the range between 1 µF and 10 µF should also be placed close to the supply pins.
  - As a good practice it is suggested to add filtering capacitors close to logic inputs of the device (INA, INB, BRAKE, SD), in particular for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver, so to minimize the gate loop area and inductance that might cause noise or ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should be no trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH_x and GNDISO_x pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

8.2 Layout example

An example of STGAP2SiCD suggested half-bridge with negative gate driving PCB layout is shown in Figure 7 ; the main signals have been highlighted by different colors. It is recommended to follow this example for proper positioning and connection of filtering capacitors. It is recommended to follow this example for proper positioning and connection of filtering capacitors.

Figure 7. Suggested PCB layout for half-bridge configuration with negative driving voltage



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9 Testing and characterization information

Figure 8. **Timings definition**

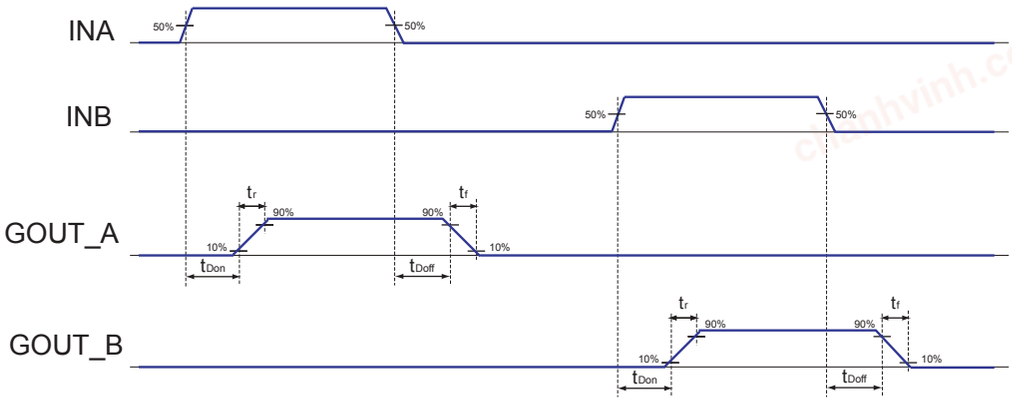
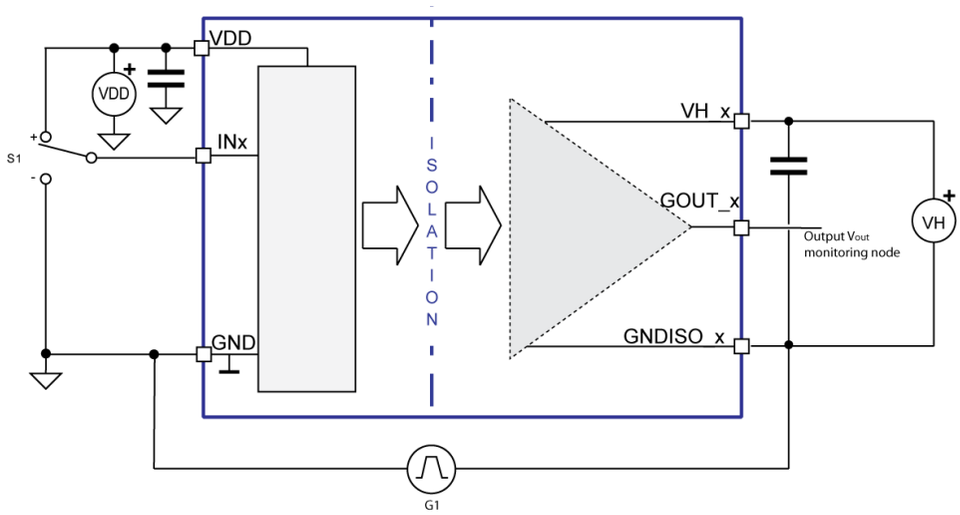


Figure 9. **CMTI test circuit**



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10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO-36W package information

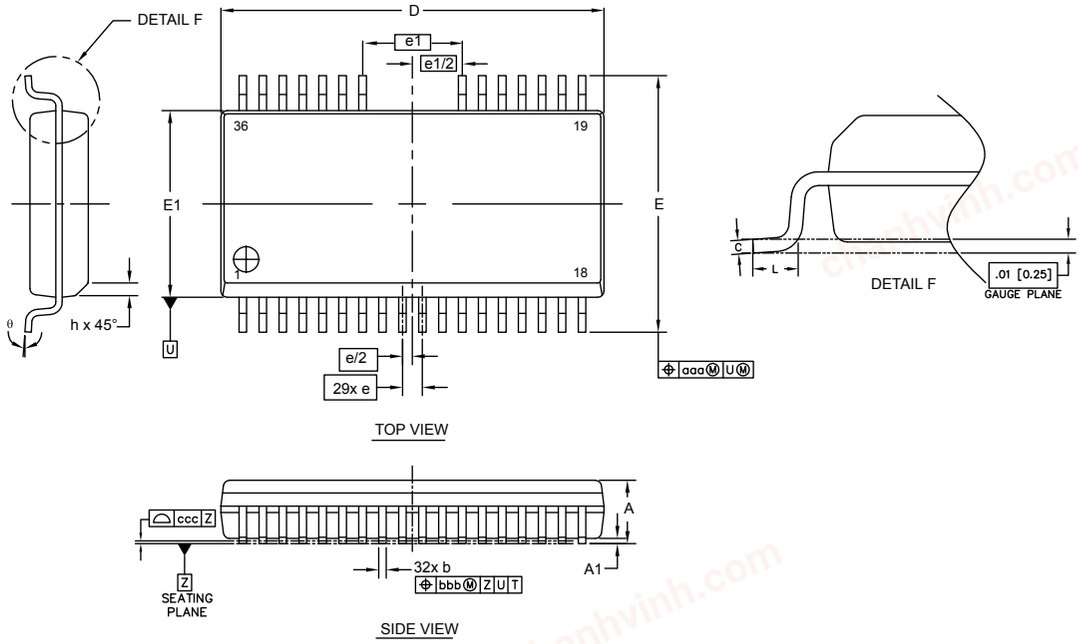
Table 10. SO-36W package dimensions

Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs are not to exceed 0.15 mm per side.

Dim.	mm			NOTES
	Min.	Typ.	Max.	
A			2.65	
A1	0.1		0.3	
b	0.25		0.35	
c	0.20		0.33	
D	15.20		15.60	
E1	7.4		7.6	
E	10.05		10.65	
e		0.80		
e1		4.00		
L	0.61		0.91	
h	0.25		0.75	
θ	0°		8°	
aaa		0.25		
bbb		0.25		
ccc		0.10		

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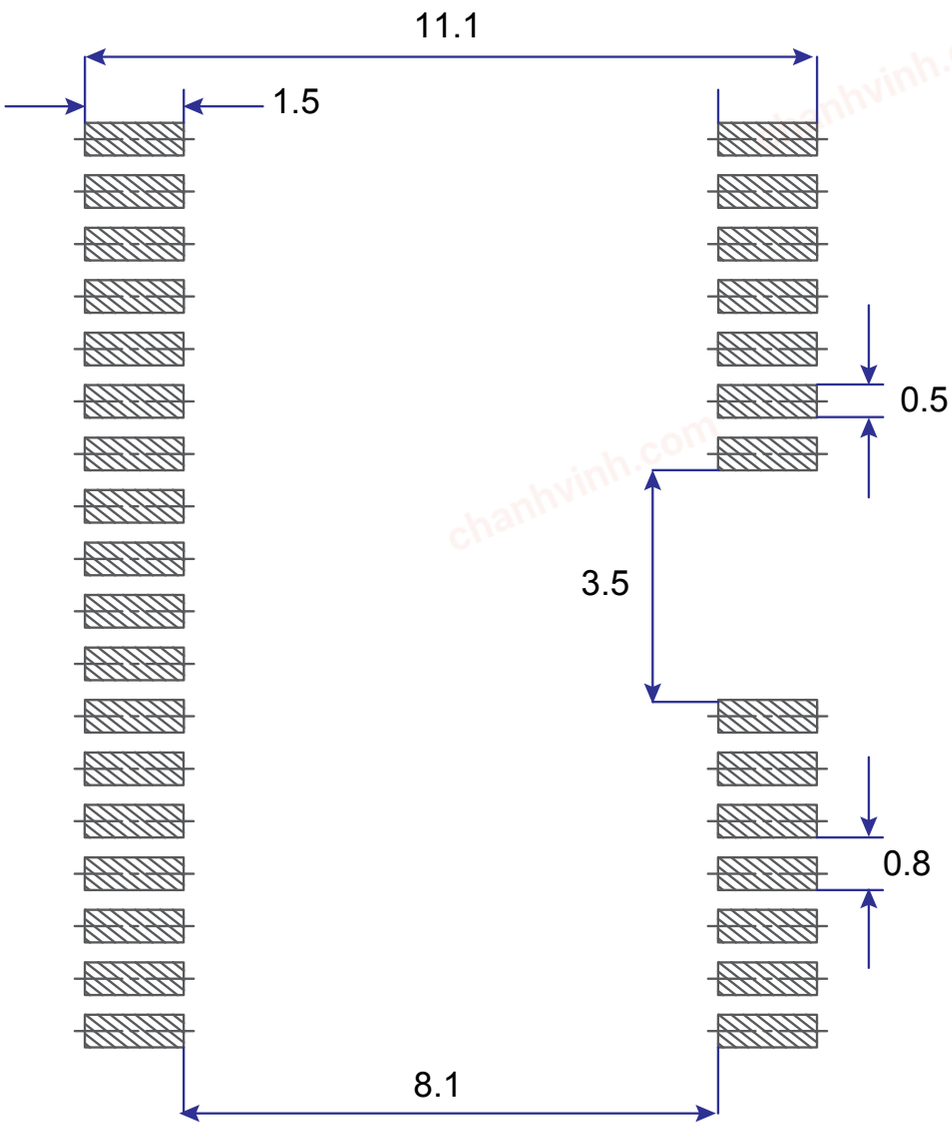
Figure 10. **SO-36W package outline**



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11 Suggested land pattern

Figure 11. **SO-36W suggested land pattern**



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12 Ordering information

Table 11. **Device summary**

Order code	Output configuration	Package	Package marking	Packaging
STGAP2SICD	Separated outputs and Miller CLAMP	SO-36W	GAP2ID	Tube
STGAP2SICDTR	Separated outputs and Miller CLAMP	SO-36W	GAP2ID	Tape and Reel

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Revision history

Table 12. **Document revision history**

Date	Version	Changes
18-Oct-2021	1	Initial release.
29-Sep-2022	2	Added UL file certification

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