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STGAP2GS

Datasheet

Galvanically isolated 3 A single gate driver for Enhancement mode GaN FETs



SO-8W

Product status link

STGAP2GS

Product label

SUSTAINABLE TECHNOLOGY

Features

- High voltage rail up to 1200 V
- Driver current capability: 2 A / 3 A source/sink @25 °C, VH = 6 V
- dV/dt transient immunity ±100 V/ns
- Input-output propagation delay: 45 ns
- Separate sink and source option for easy gate driving configuration
- UVLO function optimized for GaN
- Gate driving voltage up to 15 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shut-down protection
- Standby function
- Wide body SO-8W package

Application

- Motor driver for home appliances, factory automation, industrial drives and fans.
- 600/1200 V inverters
- Wireless chargers
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

Description

The STGAP2GS is a single gate driver which provides galvanic isolation between the gate driving channel and the low voltage control and interface circuitry.

The gate driver is characterized by 2 A source and 3 A sink capability and rail-to-rail outputs, making the device also suitable for mid and high power applications such as power conversion and motor driver inverters in industrial applications.

The device allows to independently optimize turn-on and turn-off by using dedicated gate resistors.

The device integrates protection functions including thermal shutdown and UVLO with optimized level for Enhancement-mode GaN FETs, which enables easy design high efficiency and reliable systems. Dual input pins allow the selection of signal polarity control and implementation of HW interlocking protection to avoid cross-conduction in case of controller malfunction.

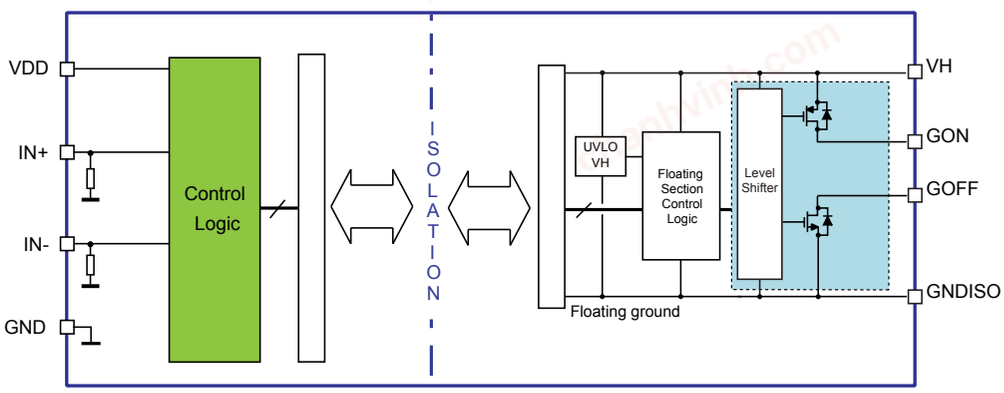
The input to output propagation delay results contained within 45 ns, providing high PWM control accuracy.

A standby mode is available to reduce idle power consumption.

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1 Block diagram

Figure 1. **STGAP2GS Block diagram**



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2 Pin description and connection diagram

Figure 2. **STGAP2GS Pin connection (top view)**

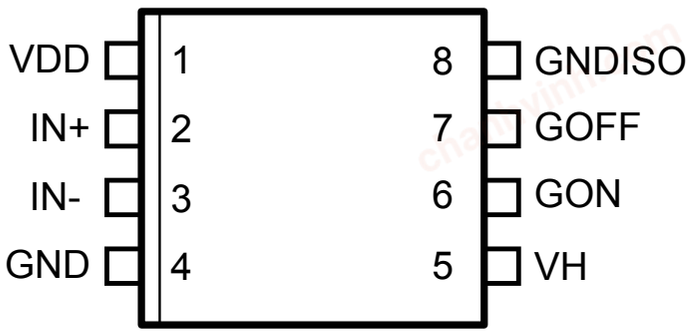


Table 1. **Pin Description**

Pin #	Pin name	Type	Function
1	VDD	Power supply	Driver logic supply voltage.
2	IN+	Logic input	Driver logic input, active high.
3	$\overline{\text{IN-}}$	Logic input	Driver logic input, active low.
4	GND	Power supply	Driver logic ground.
5	VH	Power supply	Gate driving positive voltage supply.
6	GON	Analog output	Source output.
7	GOFF	Analog output	Sink output.
8	GNDISO	Power supply	Gate driving Isolated ground.

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3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND		- 0.3	6	V
V_{LOGIC}	Logic pins voltage vs. GND		- 0.3	6	V
VH	Positive supply voltage (VH vs. GNDISO)		- 0.3	15	V
V_{OUT}	Voltage on gate driver outputs (GON, GOFF vs. GNDISO)		- 0.3	VH + 0.3	V
T_J	Junction temperature		- 40	150	°C
T_S	Storage temperature		- 50	150	°C
ESD	HBM (human body model)		2		kV

3.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND		3.1	5.5	V
V_{LOGIC}	Logic pins voltage vs. GND		0	5.5	V
VH	Positive supply voltage (VH vs. GNDISO)		Max(V_{Hon})	13	V
dVH/dt	VH Power-up transient	VH = 0 to 6 V	100		µs
F_{SW}	Maximum switching frequency.(1)			2	MHz
T_J	Operating Junction Temperature		-40	125	°C

1. *Actual limit depends on power dissipation and T_J*

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Test condition	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	*JEDEC 2s2p PCB in still air*	130	°C/W

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4 Electrical characteristics

Testing conditions: T_J = 25 °C, VH = 6 V, VDD = 5 V unless otherwise specified.
Typical values are intended at T_J = 25 °C.

Table 5. Electrical characteristics

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics							
t_{Don}	IN+, IN-	Input to output propagation delay ON	VDD = 5 V, T_J = 25°C	35	42	50	ns
			VDD = 5 V, -40°C ≤ T_J ≤ +125°C (1)	30		70	ns
			VDD = 3.3 V, T_J = 25°C	45	55	65	ns
			VDD = 3.3 V, -40°C ≤ T_J ≤ +125°C (1)	39		93	ns
t_{Doff}	IN+, IN-	Input to output propagation delay OFF	VDD = 5 V, T_J = 25°C	35	42	50	ns
			VDD = 5 V, -40°C ≤ T_J ≤ +125°C (1)	30		70	ns
			VDD = 3.3 V, T_J = 25°C	45	55	65	ns
			VDD = 3.3 V, -40°C ≤ T_J ≤ +125°C (1)	39		93	ns
t_r		Rise time	C_L= 4.7 nF see Figure 8		30		ns
t_f		Fall time			30		ns
PWD		Pulse Width Distortion $\lvert t_{Don} - t_{Doff} \rvert$				8	ns
CMTI (1)		Common-mode transient immunity, $\lvert d_{VISO/dt} \rvert$	V_{CM} = 1500 V, see Figure 9	100			V/ns
Supply voltage							
VH_{on}	VH	VH UVLO turn-on threshold		4.2	4.5	4.8	V
VH_{off}	VH	VH UVLO turn-off threshold		4.1	4.4	4.7	V
VH_{hyst}	VH	VH UVLO hysteresis		90	100	130	mV
I_{QH}	VH	VH quiescent supply current			1.3	1.8	mA
I_{QHSBY}	VH	Standby VH quiescent supply current	Standby mode		400	550	µA
SafeClp	GOFF	GOFF active clamp	I_{GOFF} = 0.2 A; VH floating		2	2.3	V
I_{QDD}	VDD	VDD quiescent supply current			1.0	1.3	mA

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Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{QDDSBY}	VDD	Standby VDD quiescent supply current	Standby mode		40	65	µA
Logic inputs							
V_{il}	IN+, IN-	Low-level logic threshold voltage		0.29·VDD	0.33·VDD	0.37·VDD	V
V_{ih}	IN+, IN-	High-level logic threshold voltage		0.58·VDD	0.66·VDD	0.70·VDD	V
I_{INh}	IN+, IN-	INx logic “1” input bias current	INx = 5 V	33	50	70	µA
I_{INl}	IN+, IN-	INx logic “0” input bias current	INx = GND			1	µA
R_{pd}	IN+, IN-	Inputs pull-down resistors	INx = 5 V	70	100	150	kΩ
Driver buffer section							
I_{GON}	GON	Source short-circuit current	T_J = 25 °C		2		A
			T_J = -40 ÷ +125 °C (1)	1.5		2.5	
V_{GONH}	GON	Source output high-level voltage	I_{GON} = 100 mA	VH-0.15	VH-0.12		V
R_{GON}	GON	Source R_{DS_ON}	I_{GON} = 100 mA		1.25	1.5	Ω
I_{GOFF}	GOFF	Sink short-circuit current	T_J = 25 °C		3		A
			T_J = -40 ÷ +125 °C (1)	2.25		3.75	
V_{GOFFL}	GOFF	Sink output low-level voltage	I_{GOFF} = 100 mA		60	80	mV
R_{GOFF}	GOFF	Sink R_{DS_ON}	I_{GOFF} = 100 mA		0.6	0.8	Ω
Overtemperature protection							
T_{SD}		Shutdown temperature (1)		170			°C
T_{hys}		Temperature hysteresis (1)			20		°C
Standby							
t_{STBY}		Standby time	See Section 6.6	200	280	500	µs
t_{WUP}		Wake-up time	See Section 6.6	10	20	35	µs
t_{awake}		Wake-up delay	See Section 6.6	1	2	3	µs
$t_{stbyfilt}$		Standby filter	See Section 6.6	200	280	800	ns

1. *Characterization data, not tested in production*

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5 Isolation

Table 6. Isolation and safety-related specifications

Parameter	Symbol	Value	Unit	Conditions
Clearance (Minimum External Air Gap)	CLR	8	mm	Measured from input terminals to output terminals, shortest distance through air
Creepage (*) (Minimum External Tracking)	CPG	8	mm	Measured from input terminals to output terminals, shortest distance path along body
Comparative Tracking Index (Tracking Resistance)	CTI	≥ 400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group	-	II	-	Material Group (DIN VDE 0110, 1/89, Table 1)

Table 7. Isolation characteristics

Parameter	Symbol	Test Conditions	Characteristic	Unit
Maximum Working Isolation Voltage	V_{IORM}	-	1200	V_{PEAK}
Input to Output test voltage In accordance with VDE 0884-11	V_{PR}	Method a, Type test	1920	V_{PEAK}
		$V_{PR} = V_{IORM} \times 1.6$, t_m = 10 s		
		Partial discharge < 5 pC		
		Method b1, 100 % Production test	2250	V_{PEAK}
		$V_{PR} = V_{IORM} \times 1.875$, t_m = 1 s		
		Partial discharge < 5 pC		
Transient Overvoltage (Highest Allowable Overvoltage)	V_{IOTM}	t_{ini} = 60 s; Type test	6000	V_{PEAK}
Maximum Surge TestVoltage	V_{IOSM}	Type test	6000	V_{PEAK}
Isolation Resistance	R_{IO}	V_{IO} = 500 V; Type test	$>10^9$	Ω

Table 8. Isolation voltage

Parameter	Symbol	Characteristic	Unit
Isolation Withstand Voltage, 1min (Type test)	V_{ISO}	3535/5000	V_{RMS}/V_{PEAK}
Isolation TestVoltage, 1sec (100% production)	$V_{ISOtest}$	4242/6000	V_{RMS}/V_{PEAK}

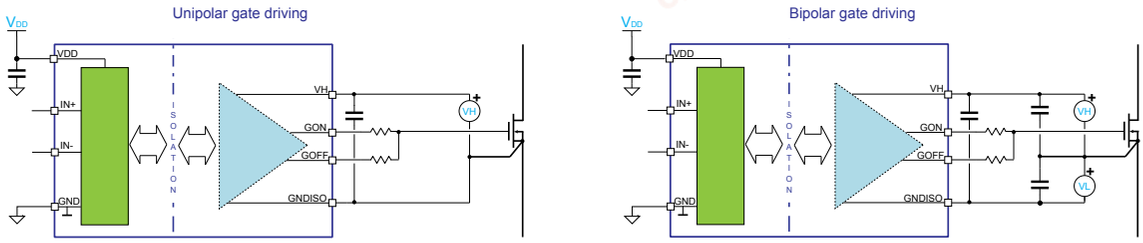
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6 Functional description

6.1 Gate driving power supply and UVLO

The STGAP2GS is a flexible and compact gate driver with 3 A output current and rail-to-rail outputs. The device allows implementation of either unipolar or bipolar gate driving.

Figure 3. Power supply configuration for unipolar and bipolar gate driving



Undervoltage protection is available on VH supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH voltage falls below the VH_{off} threshold, the output buffer enters a “safe state”. When VH voltage reaches the VH_{on} threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors and are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value in the range between 1 µF and 10 µF should be placed close to it.

6.2 Power-up, power-down and “safe state”

The following conditions define the “safe state”:

- GOFF = ON state;
- GON = High Impedance;

Such conditions are established at the end of the power-up of the isolated side ($VH < VH_{on}$) and maintained until the device power down phase ($VH < VH_{off}$), regardless of the value of the input pins.

When driving GaN switches, it is recommended to provide a smooth voltage transient to the VH supply pin during power ON, and to limit the VH rising slope according to Table 3.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If VH positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in safe state, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage sides, the device output state depends on the status of the input pins.

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6.3 Control inputs

The device is controlled through the IN+ and IN- logic inputs, in accordance with the truth table described in following Table 9

Table 9. STGAP2GS inputs truth table (applicable when device is not in UVLO or "safe state")

Input pins		Output pins	
IN+	IN-	GON	GOFF
L	L	OFF	ON
H	L	**ON**	**OFF**
L	H	OFF	ON
H	H	OFF	ON

6.4 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced in “safe state” until communication link is properly established again.

6.5 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the T_{SD} temperature threshold, the device is forced in “safe state”. The device operation is restored as soon as the junction temperature is lower than T_{SD}-T_{hys}.

6.6 Standby function

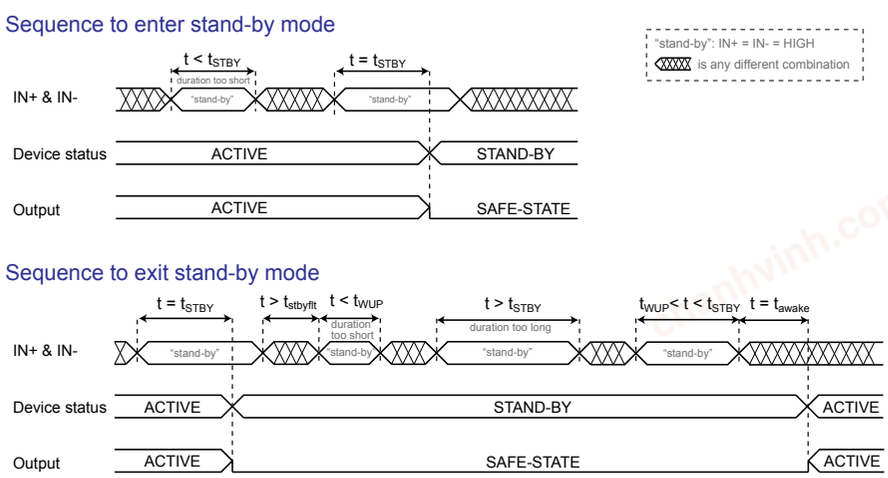
In order to reduce the power consumption of both control interface and gate driving sides the device can be put in standby mode. In standby mode the quiescent current from VDD and VH supply pins is reduced to I_{QDDSBY} and I_{QHSBY} respectively, and the output remains in “safe state” (the output is actively forced low).

The way to enter standby is to keep both IN+ and IN- high (“standby” value) for a time longer than t_{STBY}. During standby the inputs can change from the “standby” value.

To exit standby, IN+ and IN- must be put in any combination different from the “standby” value for a time longer than $t_{stbyfilt}$, and then in the “standby” value for a time t such that $t_{WUP} < t < t_{STBY}$.

When the input configuration is changed from the “standby” value the output is enabled and set according to inputs state after a time t_{awake}.

Figure 4. Standby state sequences



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7 Typical application

The STGAP2GS is design to drive Enhancement-mode GaN FETs, thanks to the separated turn-on and turn-off output pins and to the optimized UVLO protection. Since the threshold voltage of GaN HEMTs is typically lower than 2 V, attention must be paid to avoid induced turn on phenomena during high dV/dt transients. The most common solution is to differentiate the values of turn-on and turn-off gate resistors, making the turn-off resistor smaller than the turn-on one. In some cases, the use of negative driving might be needed (see Figure 6, depending on the GaN characteristic and working conditions. In all cases the use of a 10 kΩ pull-down resistor between the gate and Kelvin-Source pins is recommended, in order to avoid gate spikes while the driver is not yet powered on.

Optimal driving of GaN switches requires an optimized routing of gate loop with minimized parasitic inductance; in order to ease this task many GaN swithes comes with a dedicated Kelvin-Source pin dedicated for the gate driving. Also the current loop of the and power stage and the connection to the power bulk capacitor should be design with minimum loop inductance; some recommendations are provided in Section 8 .

Figure 5. Typical application diagram - Positive gate driving

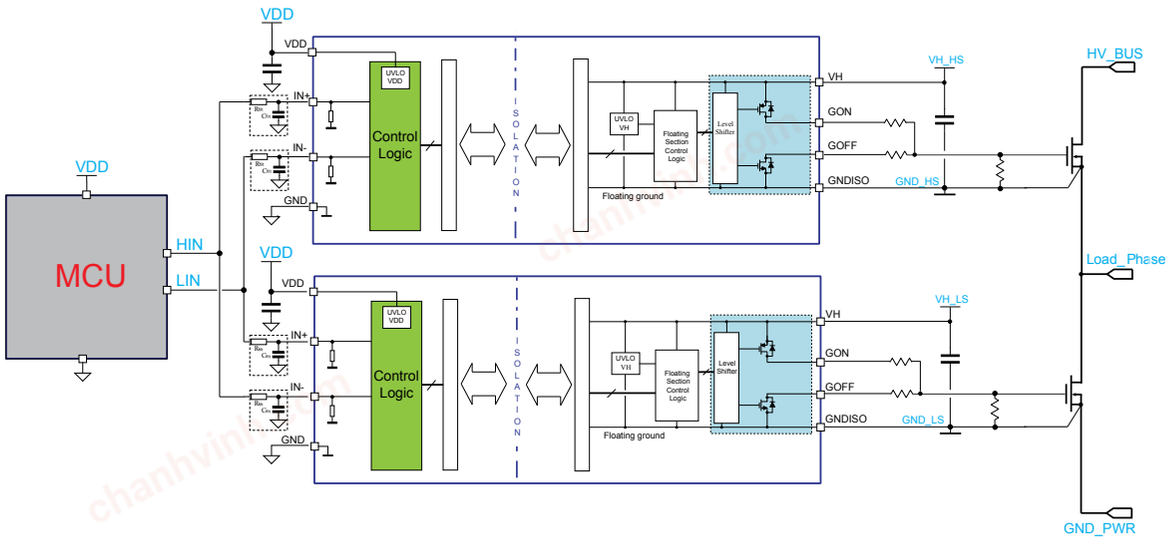
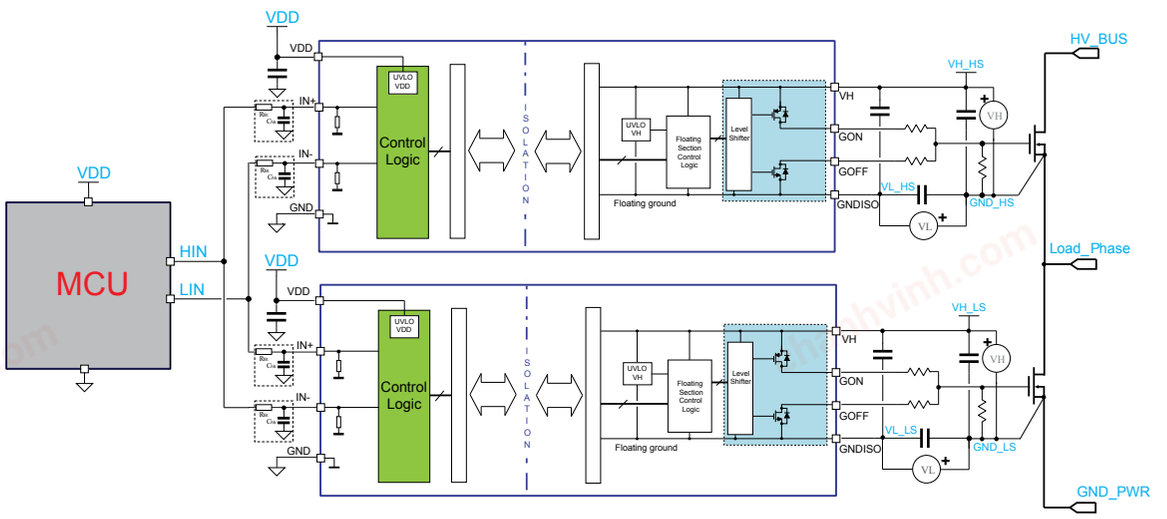


Figure 6. Typical application diagram - Negative gate driving



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8 Layout

8.1 Layout guidelines and considerations

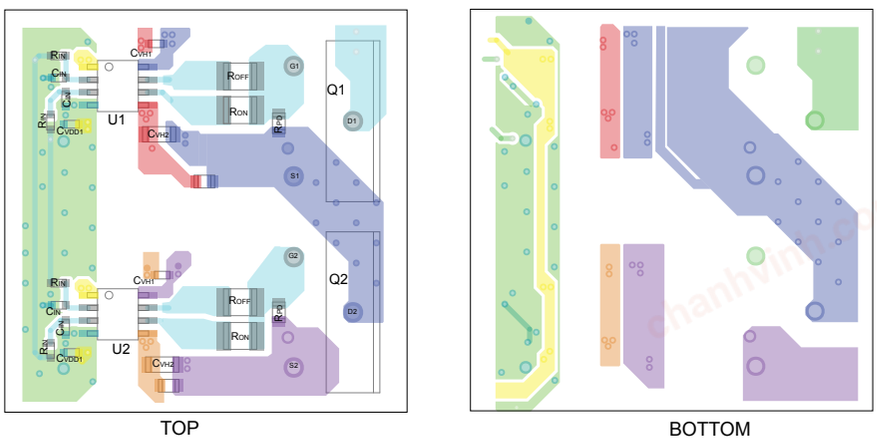
In order to optimize the PCB layout, the following considerations should be taken into account:

- The power transistors must be placed as close as possible to the gate driver, so to minimize the gate loop area and inductance that might cause noise, ringing and, in the worst cases, induced turn-on. Gate loop inductance is crucial especially in GaN applications, where the V_{GSth} is typically lower than other technologies. To further minimize gate loop inductance, it is recommended to use an inner plane layer to route the gate current return path (Kelvin-Source to GNDISO) flowing just underneath gate resistors. Adequate vias to connect to the plane shall be placed near driver and power switch source pins.
- When driving GaN switches the use of a 10 kΩ pull-down resistor between Gate and Kelvin-Source is also recommended. Such resistor should be placed close to the GaN pins.
- If the power transistor provides Kelvin-Source pin, it shall be used for gate driving while using the standard source pin(s) only for load current. The standard source pin(s) and the Kelvin-Source pin shall not be shorted together on PCB.
- If the power transistor does not provide Kelvin-Source pin, the net connecting the driver (GNDISO pin) to the power switch source pin shall use a dedicated trace/plane. The trace/plane shall start just on power switch source pin to minimize path sharing between gate current and load current.
- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pins. A 100 nF capacitor must be placed between VDD and GND and between VH and GNDISO, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current, a second capacitor with a value between 1 µF and 10 µF should also be placed close to the supply pins.
- It is good practice to add filtering capacitors close to logic inputs of the device (IN+, IN-), particularly for fast switching or noisy applications.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH and GNDISO pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

8.2 Layout example

An example of STGAP2GS half-bridge suggested PCB layout with main signals highlighted by different colors is shown in Figure 7. It is recommended to follow this example for correct positioning and connection of filtering capacitors.

Figure 7. Half-bridge suggested PCB layout



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9 Testing and characterization information

Figure 8. **Timings definition**

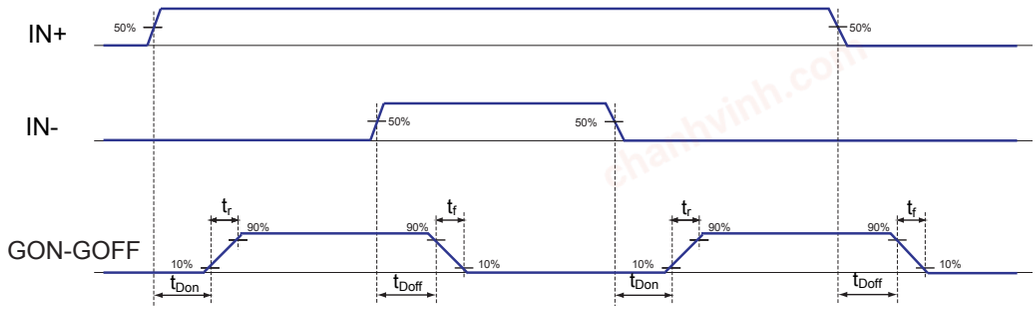
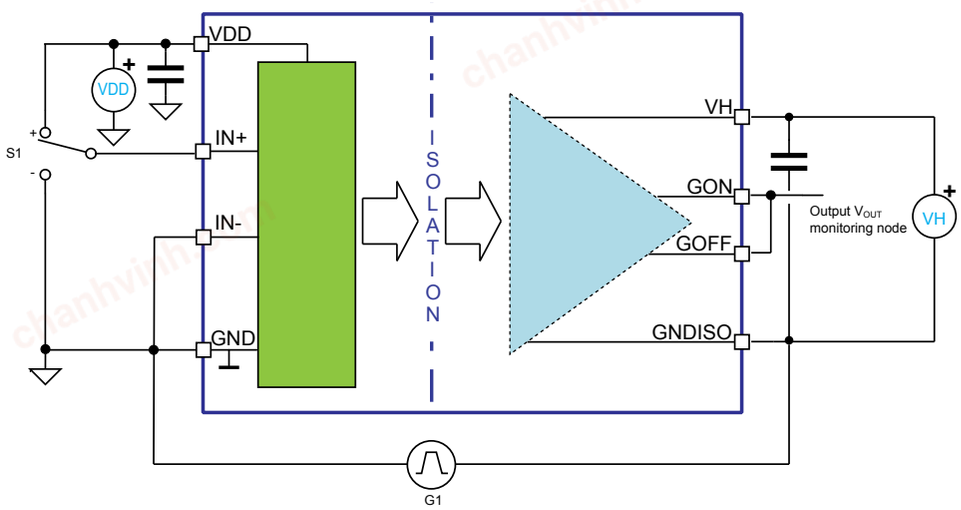


Figure 9. **CMTI test circuit**



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10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO-8W package information

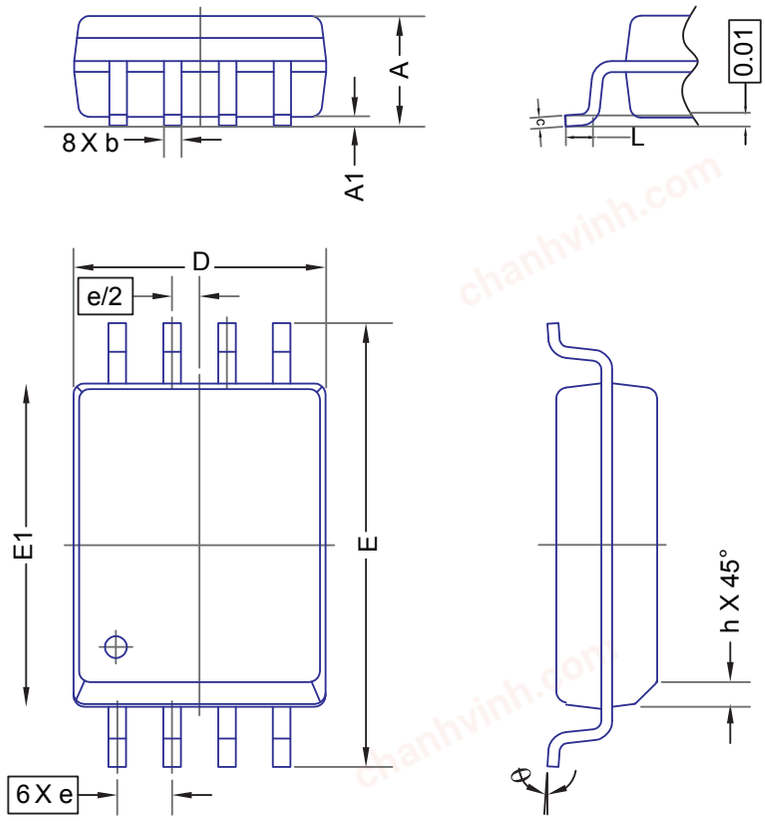
Table 10. SO-8W package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max
A	2.34		2.64
A1	0.1		0.3
b	0.3		0.51
c	0.2		0.33
D(1)	5.64		6.05
e		1.27 BSC	
E1	7.39		7.59
E	10.11		10.52
L	0.61		0.91
h	0.25		0.76
Θ	0°		8°
aaa		0.25	
bbb		0.25	
ccc		0.1	

1. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.*

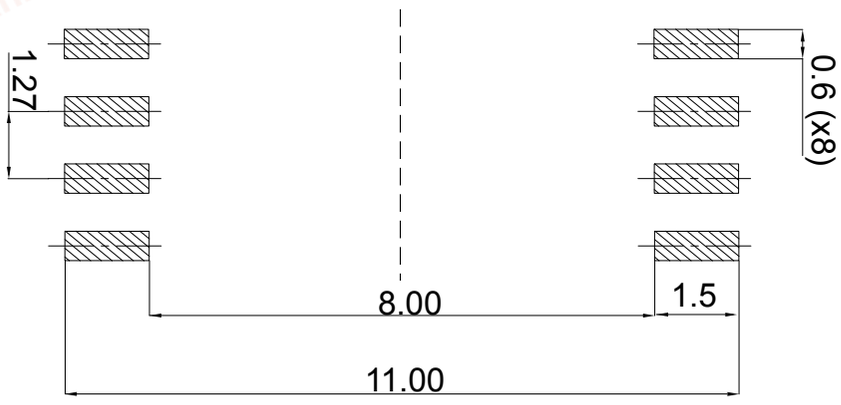
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Figure 10. **SO-8W mechanical data**



10.2 SO-8W suggested land pattern

Figure 11. **SO-8W suggested land pattern**



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11 Ordering information

Table 11. **Device summary**

Order code	Package	Package marking	Packaging
STGAP2GSC	SO-8	GAP2GS	Tube
STGAP2GSCTR	SO-8	GAP2GS	Tape and Reel

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Revision history

Table 12. **Document revision history**

Date	Version	Changes
21-Dec-2022	1	Initial release.

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