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STGAP1BS

Datasheet

Automotive galvanically isolated advanced single gate driver



SO24W

Product status link
STGAP1BS

Product label
SUSTAINABLE TECHNOLOGY

Features

- AEC-Q100 qualified
- High voltage rail up to 1500 V
- Driver current capability: 5 A sink/source current at 25 °C
- dV/dt transient immunity ±50 V/ns in full temperature range
- Overall input/output propagation delay: 100 ns
- Separate sink and source for easy gate driving configuration
- Negative gate drive ability
- Active Miller clamp
- Desaturation detection
- SENSE input
- V_{CE} active clamping
- Output 2-level turn-off
- Diagnostic status output
- UVLO and OVLO functions
- Programmable input deglitch filter
- Asynchronous stop command
- Programmable deadtime, with violation error
- SPI interface for parameters programming
- Temperature warning and shutdown protection
- Self-diagnostic routines for protection features
- Full effective fault protection

Applications

- 600/1200 V inverters
- Inverters for EV/HEV
- EV charging stations
- Industrial drives
- UPS equipment
- DC/DC converters
- Solar inverters

Description

The STGAP1BS is a galvanically isolated single gate driver for N-channel MOSFETs and IGBTs with advanced protection, configuration and diagnostic features. The architecture of the STGAP1BS isolates the channel from the control and the low voltage interface circuitry through true galvanic isolation.

The gate driver is characterized by 5 A capability, making the device also suitable for high power inverter applications such as motor drivers in hybrid and electric vehicles and in industrial drives. The output driver section provides a rail-to-rail output with the possibility to use a negative gate driver supply.

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The input to output propagation delay remains below 100 ns, providing high PWM control accuracy.

Protection functions such as the Miller clamp, desaturation detection, dedicated sense pin for overcurrent detection, output 2-level turn-off, V_{CE} overvoltage protection, UVLO and OVLO are included to easily design high reliability systems. Open drain diagnostic outputs are included and detailed device conditions can be monitored through the SPI.

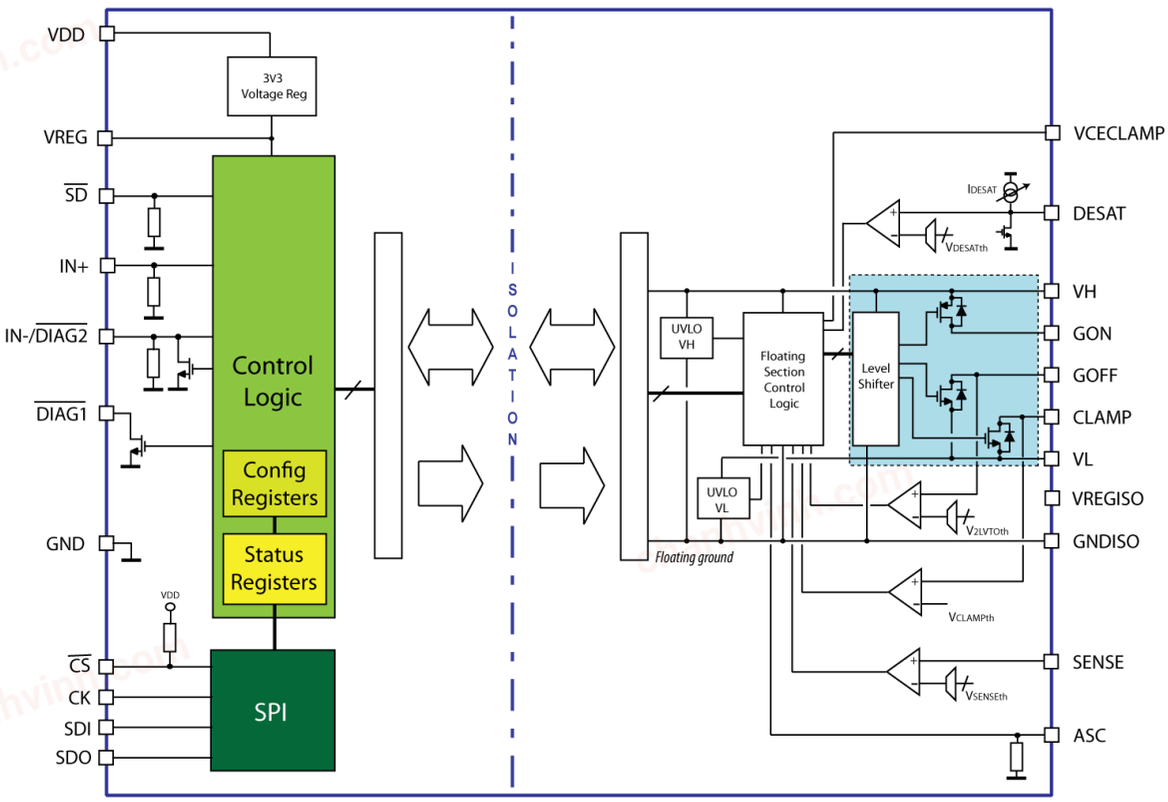
Each function parameter can be programmed via the SPI, making the device very flexible and allowing it to fit in a wide range of applications.

Separate sink and source outputs provide high flexibility and bill of material reduction for external components.

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1 Block diagram

Figure 1. **Block diagram**



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2 Pin connection

Figure 2. **Pin connection (top view)**

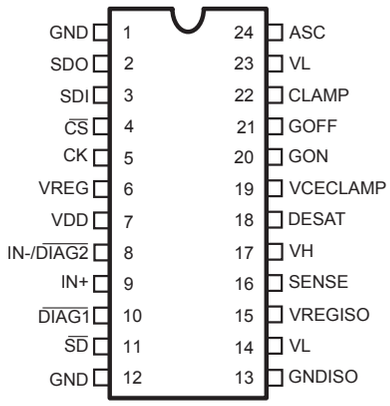


Table 1. **Pin description**

Pin no.	Pin name	Type	Function
7	VDD	Power supply	Power supply for low voltage section and internal 3.3 V regulator
6	VREG	Power supply	Internal 3.3 V regulator output and supply pin
11	$\overline{SD}$	Logic input	Shutdown input (active low)
9	IN+	Logic input	Gate command input
8	IN-/$\overline{DIAG2}$	Logic input/open drain output	Gate command input /open drain diagnostic output
10	$\overline{DIAG1}$	Open drain output	Open drain diagnostic output
1, 12	GND	Ground	Low voltage section ground
4	$\overline{CS}$	Logic input	SPI chip select (active low)
5	CK	Logic input	SPI clock
3	SDI	Logic input	SPI serial data input
2	SDO	Logic output	SPI serial data output
19	VCECLAMP	Analog input	V_{CE} active clamping protection
18	DESAT	Analog input/output	Desaturation protection
15	VREGISO	Power supply	Internal regulator output pin for decoupling
17	VH	Power supply	Positive power supply for high voltage section
20	GON	Analog output	Gate source output
21	GOFF	Analog output	Gate sink output
22	CLAMP	Analog output	Miller clamp
14, 23	VL	Power supply	Negative power supply or ground for high voltage section
13	GNDISO	Ground	High voltage section (isolated) ground
16	SENSE	Analog input	Sense input for overcurrent protection
24	ASC	Analog input	Asynchronous stop command

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3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
dV_{ISO}/dt	Common mode transient immunity	V_{CM} = 1500 V	-	50	V/ns
VDD	Low voltage section power supply voltage vs. GND	-	-0.30	6.50	V
VREG	Low voltage section internal regulator voltage vs. GND	-	-0.30	3.60	V
VREGISO	High voltage section internal regulator voltage vs. GNDISO	-	-0.30	3.60	V
V_{LOGIC}	Logic pins voltage vs. GND	-	-0.30	VDD + 0.30	V
VHL	Differential supply voltage (VH vs. VL)	-	-0.30	40	V
VH	Positive supply voltage (VH vs. GNDISO)	-	-0.30	40	V
VL	Negative supply voltage (VL vs. GNDISO)	-	-15	0.30	V
V_{OUT}	Voltage on gate driver outputs (GON, GOFF, CLAMP vs. VL)	-	VL - 0.30	VH + 0.30	V
V_{DESAT}	Voltage on DESAT pin vs. GNDISO	-	-0.30	VH + 0.30	V
V_{SENSE}	Voltage on SENSE pin vs. GNDISO	-	-2	$(VH + 0.30, 20)_{min}$	V
$V_{CECLAMP}$	Voltage on VCECLAMP pin vs. VL	-	VL - 0.30	VH + 0.30	V
V_{ASC}	Voltage on ASC pin vs. GNDISO	-	-0.30	VH + 0.30	V
I_{DIAGx}	Open drain DC output current	V_{DIAGx} < 0.8 V	-	20	mA
V_{DIAGx}	Open drain output voltage	-	-0.30	6.50	V
T_J	Junction temperature	-	-40	150	°C
T_S	Storage temperature	-	-50	150	°C
T_A	Ambient temperature	-	-40	125	°C
P_{Din}	Power dissipation input chip	-	-	65	mW
P_{Dout}	Power dissipation output chip	-	-	$(T_{J,max} - T_A)/R_{th(JA)} - P_{Din}$	W
dH/dt	Magnetic field immunity	-	-	100	A/(m·s)
ESD	Human body model	-	2		kV

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient(1)	65	°C/W

1. *The STGAP1BS mounted on the EVALSTGAP1BS rev 2.0 board (two-layer FR4 PCB).*

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3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
VH	17	Positive supply voltage (VH vs. GNDISO)	-	4.50(1)	36	V
VL	14, 23	Negative supply voltage (VL vs. GNDISO)	-	GNDISO - 10	GNDISO(2)	V
VHL	-	Differential supply voltage (VH vs. VL)	-	-	36	V
VDD	7	Low voltage section power supply voltage vs. GND	-	4.50	5.50	V
VREG	6	Low voltage section internal regulator voltage vs. GND	(3)	3.3 ±5%		V
V_{LOGIC}	2, 3, 4, 5, 8, 9, 11	Logic pins voltage vs. GND	-	-	$(VDD, 5)_{min}$	V
ASC	24	ASC pin voltage	-	GNDISO	$(VH, 15)_{min}$	V
$V_{DESATth}$	18	Desaturation protection threshold	DESAT enabled	-	VH - 1.50	V
f_{SW}	-	Maximum switching frequency(4)	-	-	150	kHz

1. *When UVLO is enabled, this value is $VH_{on,max}$*
2. *When UVLO is enabled, this value is $VL_{on,min}$*
3. *When VDD is connected to the VREG pin (refer to Section 6).*
4. *Actual limit depends on power dissipation constraints.*

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4 Electrical characteristics

4.1 AC operation

Table 5. AC operation electrical characteristics

(T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{deglitch}$	8, 9, 11	Input deglitch time	INfilter = '11'	50	70	90	ns
			INfilter = '01'	100	160	220	ns
			INfilter = '10'	420	500	580	ns
t_{INmin}		Minimum propagated input pulse	INfilter = '00' and (2LTO_EN = '1' or 2LTOtime = 0x0)	-	-	20	ns
t_{Don}	8, 9, 11, 20	Input to output propagation delay ON	Deglitch filter and 2LTO disabled	90	100	130	ns
t_{Doff}	8, 9, 11, 21	Input to output propagation delay OFF	Deglitch filter and 2LTO disabled	90	100	130	ns
t_r	20	GON rise time	VL = 0 V; C_L = 2 nF, 10% ÷ 90%	-	-	25	ns
t_f	21	GOFF rise time	VL = 0V C_L = 2 nF, 90% ÷ 10%	-	-	25	ns
PWD	8, 9, 11, 20, 21	Pulse width distortion $\|t_{Don} - t_{Doff}\|$	t_{IN} > 100 ns Deglitch filter and 2LTO disabled	-	4	10	ns
DT	8, 9, 20, 21	Deadtime	DTset = '01'	205	250	295	ns
			DTset = '10'	650	800	945	
			DTset = '11'	985	1200	1415	
$t_{release}$	11	Minimum flag release time	$\overline{SD}$ = '0', SD_FLAG = '1'	-	-	105	µs

4.2 DC operation

Table 6. DC operation electrical characteristics

(T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic inputs/output							
V_{ol}	2	SDO logic “0” output voltage	I = 4 mA	-	-	0.15	V
V_{oh}		SDO logic “1” output voltage	I = 4 mA	4.85	-	-	V
I_{INh}	8, 9	INx logic “1” input bias current	V_{IN} = 5 V (pin 8 used as IN-)	55	85	145	µA
I_{INl}		INx logic “0” input bias current	V_{IN} = 0 V (pin 8 used as IN-)	-	-	0.10	µA
I_{SDh}	11	$\overline{SD}$ logic “1” input bias current	V_{SD} = 5 V	55	85	145	µA
I_{SDl}		$\overline{SD}$ logic “0” input bias current	V_{SD} = 0 V	-	-	0.10	µA
R_{in_pd}	8, 9, 11	Input pull-down resistors	V_{IN} = 5 V (pin 8 used as IN-)	35	60	85	kΩ
R_{in_pu}	4	$\overline{CS}$ input pull-up resistor	$\overline{CS}$ = GND	35	55	80	kΩ

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Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{il}	3, 4, 5, 8, 9, 11	Low logic level voltage	-	0.29 · VDD	0.33 · VDD	0.37 · VDD	V
V_{ih}		High logic level voltage	-	0.62 · VDD	0.66 · VDD	0.79 · VDD	V
Driver buffer section							
I_{GON}	20	Source short-circuit current	T_{pulse} < 5 µs, DC = 1% T_j = 25 °C T_j = -40 - +125 °C	 2.50(1)	5	 7	A
I_{GOFF}	21	Sink short-circuit current	T_{pulse} < 5 µs, DC = 1% T_j = 25 °C T_j = -40 - +125 °C	 2.50(1)	5	 6	A
V_{GOFFL}	21	GOFF output low level voltage	I_{GOFF} = 0.1 A I_{GOFF} = 1 A	VL + 0.03 VL + 0.50	VL + 0.09 VL + 1	VL + 0.15 VL + 1.80	V
V_{GONH}	20	GON output high level voltage	I_{GON} = 0.1 A I_{GON} = 1 A	VH - 0.18 VH - 2.10	VH - 0.10 VH - 1.30	VH - 0.05 VH - 0.50	V
SafeClp	20, 21, 22	GOFF active clamp	I_{GOFF} = 0.2 A; VH floating; GON = GOFF = CLAMP	-	-	3	V
Supply voltage							
I_{REG}	6	VREG short-circuit current (see Section 7.3)	0.1 V < VREG < 3.0 V	-	60	120	mA
			VREG < 0.1 V	-	15	35	
VDD_{on}	7	VDD UVLO turn-on threshold	-	3.95	4.10	4.30	V
VDD_{off}		VDD UVLO turn-off threshold	-	3.65	3.80	4	V
VDD_{hys}		VDD UVLO hysteresis	-	0.15	-	-	V
OV_{VDDon}		VDD OVLO turn-on threshold	-	5.30	5.50	5.90	V
OV_{VDDoff}		VDD OVLO turn-off threshold	-	5.40	5.70	6.10	V
OV_{VDDhys}		VDD OVLO hysteresis	-	100	200	300	mV
I_{QDD}	7	VDD quiescent supply current	VDD = 5 V; $\overline{SD}$ = 5 V; INx = GND; f = 0 Hz	5.20	6.50	7.50	mA
			VDD = 5 V; $\overline{SD}$ = 5 V; $f_{SW} = f_{SW,max}$	6.00	8.50	9.50	mA
VH_{on}	17	VH UVLO turn-on threshold	VHONth = '01'	9.40	10	10.50	V
			VHONth = '10'	11.30	12	12.60	
			VHONth = '11'	13.15	14	14.70	
VH_{off}		VH UVLO turn-off threshold	VHONth = '01'	8.45	9	9.45	V
			VHONth = '10'	10.35	11	11.55	
			VHONth = '11'	12.25	13	13.65	
VH_{hyst}		VH UVLO hysteresis	-	0.70	1	1.30	V
VL_{on}	14, 23	VL UVLO turn-on threshold	VLONth = '01'	-3.15	-3	-2.80	V
			VLONth = '10'	-5.25	-5	-4.70	
			VLONth = '11'	-7.35	-7	-6.55	
VL_{off}		VL UVLO turn-off threshold	VLONth = '01'	-2.15	-2	-1.90	V
			VLONth = '10'	-4.25	-4	-3.80	

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Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
VL_{off}	14, 23	VL UVLO turn-off threshold	VLONth = '11'	-6.35	-6	-5.70	V
VL_{hys}		VL UVLO hysteresis	-	0.70	1	1.20	V
OV_{VHoff}	17	VH OVLO turn-off threshold	OVLO_EN = '1'	17.80	19	20	V
OV_{VHon}		VH OVLO turn-on threshold	OVLO_EN = '1'	16.90	18	18.90	V
OV_{VHhys}		VH OVLO hysteresis	OVLO_EN = '1'	0.60	1	1.30	V
OV_{VLoff}	14, 23	VL OVLO turn-off threshold	OVLO_EN = '1'	-10.50	-10	-9.40	V
OV_{VLon}		VL OVLO turn-on threshold	OVLO_EN = '1'	-9.45	-9	-8.55	V
OV_{VLhyst}		VL OVLO hysteresis	OVLO_EN = '1'	0.70	1	1.30	V
I_{QH}	17	VH quiescent supply current	$\overline{SD}$ = 5 V; IN+ = 5 V; IN- = GND	5	6.70	7.50	mA
I_{QL}	14, 23	VL quiescent supply current	VL = -5 V; $\overline{SD}$ = 5 V; IN+ = IN- = GND	300	420	550	µA
Desaturation protection							
$V_{DESATth}$	18	Desaturation threshold	DESATth = '000';	2.60	3	3.10	V
			DESATth = '001'	3.60	4	4.20	
			DESATth = '010'	4.60	5	5.30	
			DESATth = '011'	5.50	6	6.30	
			DESATth = '100'	6.50	7	7.40	
			DESATth = '101'	7.40	8	8.40	
			DESATth = '110'	8.30	9	9.40	
			DESATth = '111'	9.30	10	10.50	
$t_{DESfilter}$		DESAT pin deglitch filter	DESATth = '100'(2)	10	20	30	ns
I_{DESAT}		DESAT blanking charge current	DESATcur = '00'; V_{DESAT} = 0 V	220	250	265	µA
			DESATcur = '01'; V_{DESAT} = 0 V	440	500	525	
			DESATcur = '10'; V_{DESAT} = 0 V	660	750	800	
			DESATcur = '11'; V_{DESAT} = 0 V	885	1000	1050	
I_{DESoff}		DESAT blanking discharge current	V_{DESAT} = 8 V	50	70	90	mA
t_{BLK}	18	DESAT protection fixed blanking time	-	160	250	340	ns
t_{DESAT}		DESAT protection intervention time	V_{DESAT} = V_{DESAth} to GOFF 90% C_{LOAD} = 10 nF 2LTO disabled	80	150	220	ns
SENSE overcurrent function							
$V_{SENSEth}$	16	SENSE protection threshold	SENSEth = '000'	88	100	112	mV
			SENSEth = '001'	110	125	140	
			SENSEth = '010'	135	150	165	
			SENSEth = '011'	158	175	192	

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Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SENSEth}$	16	SENSE protection threshold	SENSEth = '100'	185	200	215	mV
			SENSEth = '101'	235	250	268	
			SENSEth = '110'	285	300	315	
			SENSEth = '111'	380	400	420	
t_{SENSE}		SENSE protection intervention time	SENSEth = '111' 0→1 V step on V_{SENSE} to GOFF 90%; C_{LOAD} = 10 nF 2LTO disabled	-	95	120	ns
2-level turn-off function							
V_{2LTOth}	21	2LTO threshold	2LTOth = '0000'	6.65	7.00	7.35	V
			2LTOth = '0001'	7.12	7.50	7.88	
			2LTOth = '0010'	7.60	8.00	8.40	
			2LTOth = '0011'	8.07	8.50	8.93	
			2LTOth = '0100'	8.55	9.00	9.45	
			2LTOth = '0101'	9.02	9.50	9.98	
			2LTOth = '0110'	9.50	10.00	10.50	
			2LTOth = '0111'	9.97	10.50	11.03	
			2LTOth = '1000'	10.45	11.00	11.55	
			2LTOth = '1001'	10.92	11.50	12.08	
			2LTOth = '1010'	11.40	12.00	12.60	
			2LTOth = '1011'	11.87	12.50	13.13	
			2LTOth = '1100'	12.35	13.00	13.65	
			2LTOth = '1101'	12.82	13.50	14.18	
			2LTOth = '1110'	13.30	14.00	14.70	
			2LTOth = '1111'	13.77	14.50	15.23	
$t_{2LTOtime}$	21	2LTO time	2LTOtime = '0001'	0.64	0.75	0.89	µs
			2LTOtime = '0010'	0.89	1.00	1.15	
			2LTOtime = '0011'	1.36	1.50	1.65	
			2LTOtime = '0100'	1.83	2.00	2.18	
			2LTOtime = '0101'	2.30	2.50	2.70	
			2LTOtime = '0110'	2.77	3.00	3.23	
			2LTOtime = '0111'	3.25	3.50	3.75	
			2LTOtime = '1000'	3.47	3.75	4.03	
			2LTOtime = '1001'	3.71	4.00	4.29	
			2LTOtime = '1010'	3.94	4.25	4.56	
			2LTOtime = '1011'	4.18	4.50	4.82	
			2LTOtime = '1100'	4.42	4.75	5.08	
			2LTOtime = '1101'	4.66	5.00	5.34	
			2LTOtime = '1110'	4.90	5.25	5.63	
			2LTOtime = '1111'	5.12	5.50	5.95	

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Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Diagnostic outputs							
$t_{DIAG1,2}$	8, 10	Fault event to $\overline{DIAGx}$ Low delay	Fault event to $\overline{DIAGx}$ 90%	-	5	-	µs
I_{DIAG1}		$\overline{DIAG1}$ low level sink current	V_{DIAG1} = 0.4 V	10	18	30	mA
I_{DIAG2}		$\overline{DIAG2}$ low level sink current	V_{DIAG2} = 0.4 V	10	18	30	mA
$R_{DIAG1,2}$		$\overline{DIAGx}$ pull-down resistor	-	300	550	800	kΩ
Clamp Miller function							
$V_{CLAMPth}$	22	CLAMP voltage threshold	CLAMP vs. GNDISO	1.70	2	2.30	V
I_{CLAMP}		Clamp short-circuit current	T_{pulse} < 5 µs, DC = 1% T_j = 25 °C T_j = -40 ÷ +125 °C	 2.50(1)	5	 6	A
V_{CLAMP_L}		Clamp low level output voltage	I_{CLAMP} = 1 A	VL + 0.50	VL + 1	VL + 1.80	V
VCE active clamping protection							
$V_{VCECLth}$	19	V_{CE} clamping threshold	-	VL + 1.20	VL + 1.60	VL + 2	V
$V_{VCECLhyst}$		V_{CE} clamping threshold hysteresis	-	0.30	0.50	0.60	V
$t_{VCECLoff}$	19	V_{CE} clamping time-out	-	2	2.30	2.60	µs
t_{VCECL}		V_{CE} clamping intervention time(2)	-	-	20	-	ns
ASC function							
V_{ASCl}	24	Low logic level voltage	-	0.80	1.10	1.40	V
V_{ASCh}		High logic level voltage	-	1.80	2.20	2.40	V
I_{ASCh}		ASC logic “1” input bias current	V_{ASC} = 5 V	55	100	145	µA
I_{ASCl}		ASC logic “0” input bias current	V_{ASC} = 0 V	-	-	0.10	µA
R_{ASC}		ASC pull-down resistors	V_{ASC} = 5 V	35	50	70	kΩ
t_{ASC}		ASC intervention time	V_{ASC} = 5 V	100	-	250	ns
Functionality checks							
t_{Gchk}	20, 21	Gate path check time (GON/GOFF)(3)	-	-	-	30	µs
V_{Gchk}	20	Gate path check voltage (GON)	-	0.7 x VH	0.76 x VH	0.84 x VH	V
t_{Rchk}	16	SENSE resistor check time	-	-	-	15	µs
$I_{GOFFchk}$	21	GOFF path check current	-	-420	-350	-280	µA
$I_{SENSERchk}$	16	SENSE resistor check current	V_{SENSE} < 1 V	8	10	12	µA
$t_{SENSEchk}$		SENSE comparator check time	-	-	-	15	µs
$t_{DESATchk}$	18	DESAT comparator check time	-	-	-	15	µs
Overtemperature protection							
T_{WN}	-	Warning temperature(2)	-	125	-	-	°C
T_{SD}	-	Shutdown temperature(2)	-	155	-	-	°C
T_{hys}	-	Temperature hysteresis(2)	-	-	20	-	°C

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Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Standby							
I_{STBY_VDD}	7	VDD standby current	VDD = 5 V	0.40	0.80	1	mA
t_{sleep}	-	Standby time	$\overline{SD}$ = '0', measured from $\overline{CS}$ rise	500	700	900	ns
t_{awake}	-	Logic wake-up time(2)	$\overline{SD}$ = '1'	5	-	-	µs
SPI (characterization data, not tested in production)							
t_{CKmax}	5	Maximum SPI clock frequency	-	5	-	-	MHz
t_{rCK} t_{fCK}		SPI clock rise and fall time	CL = 30 pF	-	-	25	ns
t_{hCK} t_{lCK}		SPI clock high and low time	-	75	-	-	ns
t_{setCS}	4	$\overline{CS}$ setup time	-	350	-	-	ns
t_{holCS}		$\overline{CS}$ hold time	-	10	-	-	ns
t_{desCS}		$\overline{CS}$ deselect time(4)	Local register read	800	-	-	ns
			Remote register read	30	-	-	µs
			Start configuration	22	-	-	
			Stop configuration	5	-	-	
			Reset status register	50	-	-	
					-	-	
			Any other command	700	-	-	ns
t_{setSDI}	3	SDI setup time	-	25	-	-	ns
t_{holSDI}		SDI hold time	-	20	-	-	ns
t_{enSDO}	2	SDO enable time	-	-	-	38	ns
t_{disSDO}		SDO disable time	-	-	-	47	ns
t_{vSDO}		SDO valid time	-	-	-	57	ns
t_{holSDO}		SDO hold time	-	37	-	-	ns
t_{SDLCSL}	4, 11	$\overline{SD}$ falling to $\overline{CS}$ falling	-	350	-	-	ns
t_{CSHSDH}	4, 11	$\overline{CS}$ rising to $\overline{SD}$ rising	-	350	-	-	ns

1. *Guaranteed by correlation.*
2. *Characterization data, not tested in production.*
3. *The actual waiting time depends on the gate charge size.*
4. *See Table 22 and Section 9.1.3 .*

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5 Isolation

Table 7. Isolation and safety-related specifications

Parameter	Symbol	Value	Unit	Conditions
Clearance (minimum external air gap)	CLR	8	mm	Measured from input terminals to output terminals, shortest distance through air
Creepage (minimum external tracking)	CPG	8	mm	Measured from input terminals to output terminals, shortest distance path along body
Comparative tracking index (tracking resistance)	CTI	≥ 400	-	DIN IEC 112/VDE 0303 Part 1
Isolation group	-	II	-	Material group (DIN VDE 0110, 1/89, Table 1)

Table 8. IEC 60747-5-2 isolation characteristics

Parameter	Symbol	Test conditions	Characteristic	Unit
Installation classification (EN 60664-1, Table 1[1]) For rated mains voltage ≤ 150 V_{rms} For rated mains voltage ≤ 300 V_{rms} For rated mains voltage ≤ 600 V_{rms}	-	-	 I - IV I - III I - II	-
Pollution degree (EN 60664-1)	-	-	2	-
Maximum working isolation voltage	V_{IORM}	-	1500	V_{PEAK}
Input to output test voltage as per IEC 60747-5-2	V_{PR}	Method a, type test $V_{PR} = V_{IORM} \times 1.6$, t_m = 10 s Partial discharge < 5 pC	2400	V_{PEAK}
		Method b1, 100 % production test $V_{PR} = V_{IORM} \times 1.875$, t_m = 1 s Partial discharge < 5 pC	2815	V_{PEAK}
Transient overvoltage as per IEC 60747-5-2 (highest allowable overvoltage)	V_{IOTM}	t_{ini} = 60 s; type test	4000	V_{PEAK}
Maximum surge isolation voltage	V_{IOSM}	Type test	4000	V_{PEAK}
Isolation resistance	R_{IO}	V_{IO} = 500 V at T_S; type test	$>10^9$	Ω

1. *For three-phase systems the values in the table refer to the line-to-neutral voltage.*

Table 9. UL 1577 isolation voltage ratings

Description	Symbol	Characteristic	Unit
Isolation withstand voltage, 1 min. (type test)	V_{ISO}	2500\3536	V_{rms}\V_{PEAK}
Isolation withstand test, 1 sec. (100% production)	$V_{ISOtest}$	3000\4245	V_{rms}\V_{PEAK}

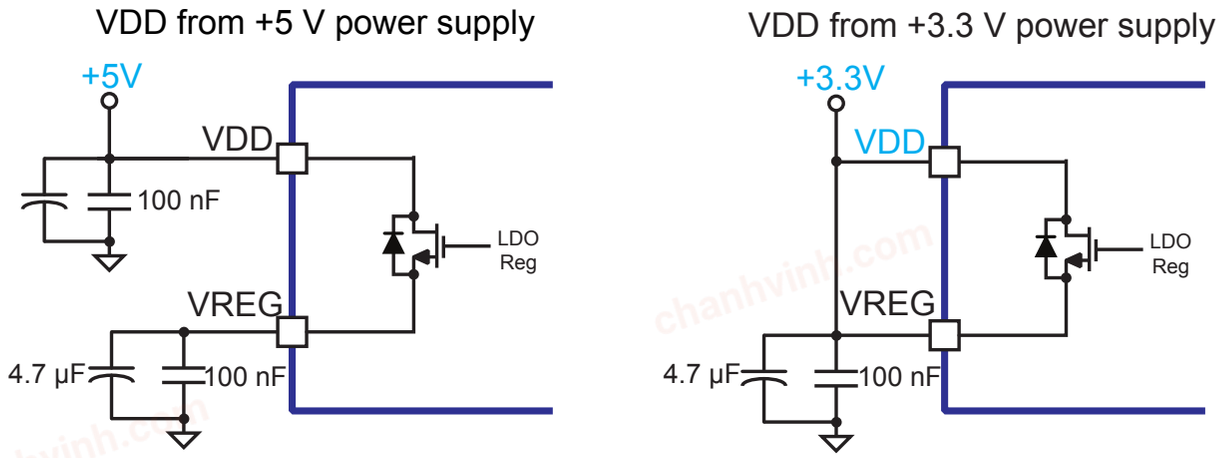
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6 Logic supply management

6.1 Low voltage section voltage regulator

The device integrates in the low voltage section a linear voltage regulator that can be used to obtain the 3.3 V logic core supply voltage from an external 5 V supply voltage. If an external 3.3 V supply voltage is available, the VDD and VREG must be shorted as shown in Figure 3. The logic IOs are referred to the VDD voltage (see Table 6 for details).

Figure 3. Low voltage section 3.3 V voltage regulator



Undervoltage protection is available on the VDD supply pin (disabled by default).

When the VDD voltage goes below the VDD_{off} threshold the device and its outputs goes in “safe state” (see Section 6.3) and the UVLOD status flag is forced low. Once the protection is triggered, the UVLOD flag is latched and the device remains in “safe state” until the UVLOD flag is not released. See Section 7.11 for indication on how the failure flags can be released.

This protection can be enabled writing the UVLOD_EN bit of the CFG1 register (disabled by default).

Overvoltage protection is available on the VDD supply pin.

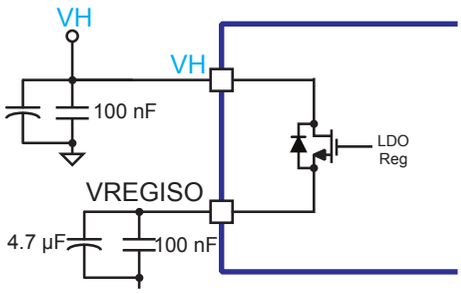
When the VDD voltage goes over the OV_{VDDoff} threshold, the device and its outputs go in “safe state” and the OVLOD status flag is set. The device remains in “safe state” and the OVLOD flag is latched, see Section 7.11 for indication on how the failure flags can be released.

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6.2 High voltage section voltage regulator

The device integrates in the high voltage section a linear voltage regulator that generates the 3.3 V logic core supply voltage from an external supply voltage connected to the VH pin.

Figure 4. High voltage section 3.3 V voltage regulator



If the voltage at the VREGISO pin goes below the minimum operating threshold which causes the logic reset, the REGERRR bit in the STATUS2 register is set high.

6.3 Power-up, power-down and “safe state”

The following conditions define the device's “safe state”:

- GOFF = ON state
- GON = high impedance
- CLAMP = ON state (if CLAMP < 'GNDISO + $V_{CLAMPth}$')
- DESAT = GNDISO (internal switch on and current generator off)

Such conditions are guaranteed at power-up of the isolated side (also for VH < VH_{on} and VL > VL_{on}) and during the whole device power-down phase (also for VH < VH_{off} and VL > VL_{off}), whatever the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage smaller than SafeClp when the VH voltage is not high enough to actively turn the GOFF N-channel MOSFET on.

If the VH positive supply pin is floating the GOFF pin is clamped to a voltage smaller than SafeClp.

After power-up of the isolated side the REGERRR status flag is latched and the device is forced in “safe state”. See Section 7.11 for indication on how the failure flags can be released.

After power-up of the low voltage side the REGERRL and UVLOD status flags are latched and the device is forced in “safe state”. See Section 7.11 for indication on how the failure flags can be released.

The UVLOH flag is also forced high at the power-up of the low voltage side, but its value is set to zero as soon as the isolated side power-up is completed.

6.4 Standby function

The device can be put in standby mode to reduce the power consumption on VDD via the SPI command “`Sleep`” (refer to Section 9.1.5).

The proper sequence is:

1. Pull-down the $\overline{SD}$ pin: the driver section will be put in “safe state”
2. Send a `Sleep` command
3. After a t_{sleep} time, the device can be considered in sleep mode.

To exit from the sleep mode, it is necessary to set the $\overline{SD}$ high for at least t_{awake} while keeping IN+ low.

After a t_{awake} time the device can accept new commands and the REGERRR bit is set to indicate that the device needs to be reprogrammed.

If the $\overline{SD}$ pin is raised while t_{sleep} is still not expired, the device returns to the operation mode within a t_{awake} time.

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7 Functional description

7.1 Inputs and outputs

The device is controlled through following logic inputs:

- $\overline{SD}$: active low shutdown input
- IN+: driver input
- $\overline{CS}$: active low chip select (SPI)
- SDI: serial data input (SPI)
- CK: serial clock (SPI)

And following logic outputs:

- SDO: serial logic output (SPI)
- $\overline{DIAG1}$: diagnostic signal (open drain)

And following IO pin:

- IN-/$\overline{DIAG2}$: driver input or diagnostic open drain output.

Logic input thresholds and output ranges vary according to VDD voltage. In particular, the device is designed to work with VDD supply voltages of 5 V or 3.3 V.

The operation of the driver IOs can be programmed through DIAG_EN bits as described in Table 10.

Table 10. Inputs true table (device NOT in “safe state”)

Bit in CFG1 register	Input pins			Output pins	
DIAG_EN	$\overline{SD}$	IN+	IN-	GON	GOFF
X	0	X	X	OFF	ON
0	1	0	0	OFF	ON
0	1	0	1	OFF	ON
0	1	1	0	ON	OFF
0	1	1	1	OFF	ON
1	1	0	X (1)	OFF	ON
1	1	1	X (1)	ON	OFF

1. *The IN-/$\overline{DIAG2}$ pin is used as the open drain output for diagnostic signaling (refer to Section 7.11*

A deglitch filter is applied to device inputs ($\overline{SD}$, IN+, IN-). Each input pulse, positive and negative, shorter than the programmed $t_{deglitch}$ value is neglected by internal logic. Deglitch time can be programmed as listed in Table 30.

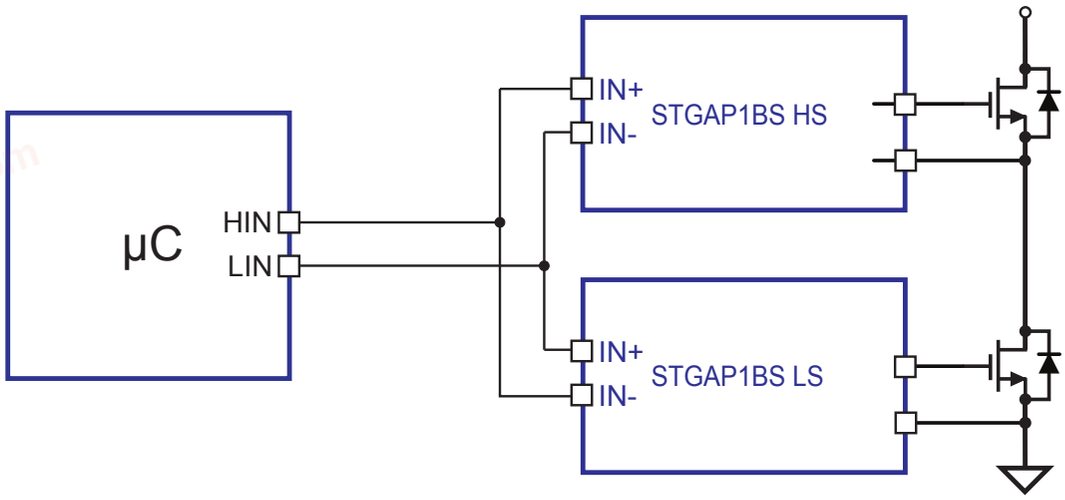
When the deglitch filter is disabled (INfilter = '00') and the 2-level turn-off function is disabled (2LTOtime = 0x0) or enabled only after a fault event (2LTO_EN = '1'), a minimum input pulse t_{INmin} is required to change the device output status. The minimum input pulse timing filters out both positive and negative pulses at the IN+, IN- and $\overline{SD}$ pins.

7.2 Deadtime and interlocking

When single gate drivers are used in half-bridge configuration, they usually do not allow preventing cross conduction in case of wrong input signals coming from the controller device. This limitation is due to the fact that each driver does not have the possibility to know the status of the input signal of the other companion driver in the same leg. Thanks to the availability of two input pins with opposite polarity the STGAP1BS allows implementing hardware interlocking that prevents cross conduction even in case of wrong input signals generated by the control unit. This functionality can be achieved by implementing the connection shown in Figure 5 and by configuring the IN-/$\overline{DIAG2}$ pin as input (which is its default configuration).

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Figure 5. **HW cross conduction prevention in half-bridge configuration with two single gate drivers**



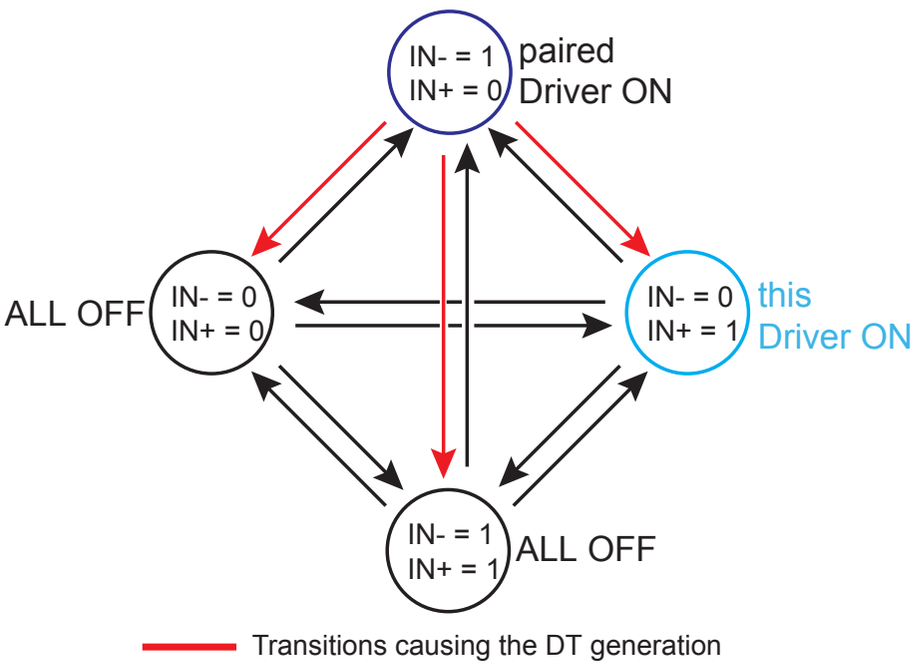
When such configuration is used, it is also possible to enable the STGAP1BS programmable deadtime feature, which guarantees that at least a DT time passes between the turn-off of one driver's output and the turn-on of the other driver. The deadtime value DT can be programmed through the SPI interface as shown in Table 29.

If the deadtime feature is enabled, a counter is started when the input status changes from < IN- = '1' and IN+ = '0' > to a different combination, which means that the other driver in the same leg is at the beginning of a turn-off (refer to Figure 6).

Once the counter is started it keeps counting regardless of any input variation until a DT time has passed, and during this time the driver prevents the turn-on of its output even if the controller tries to force the turn-on (inputs set to < IN- = '0' and IN+ = '1' >).

Once the programmed DT counter is expired, the driver immediately turns the output on as soon as a turn-on command is present at the input pins, and no extra delay is added.

Figure 6. **Transitions causing the DT generation**



Some examples of the device behavior when the deadtime feature is enabled are shown from Figure 7 to Figure 10.

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Figure 7. **Synchronous control signal edges**

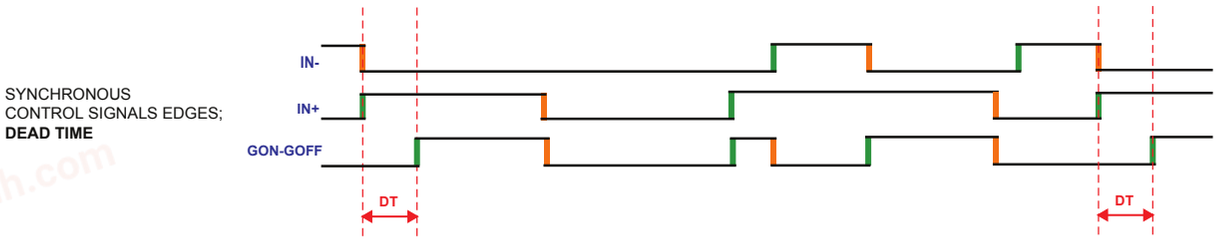


Figure 8. **Control edges signal overlapped, example 1**

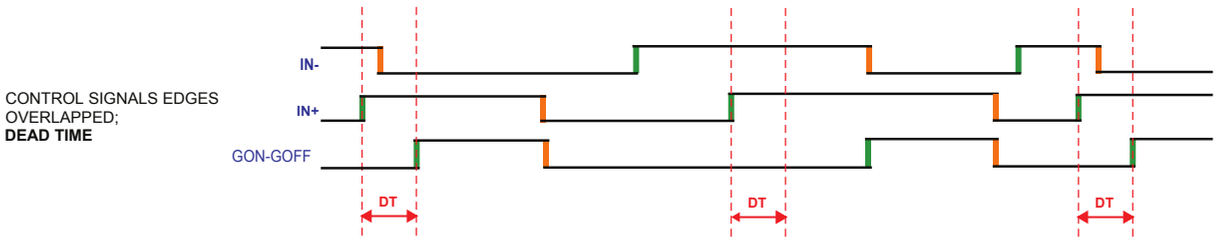


Figure 9. **Control edges signal overlapped, example 2**

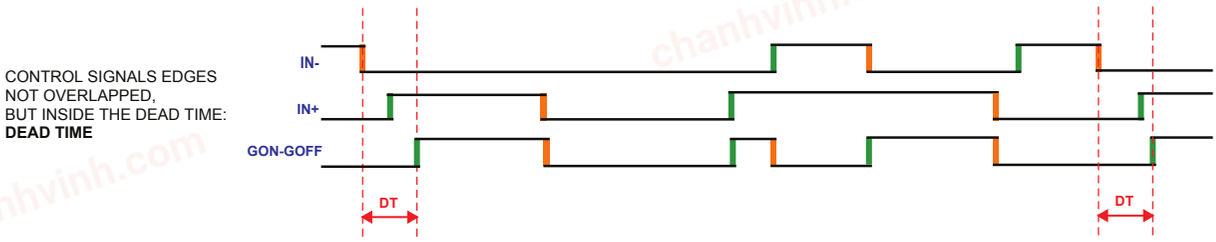
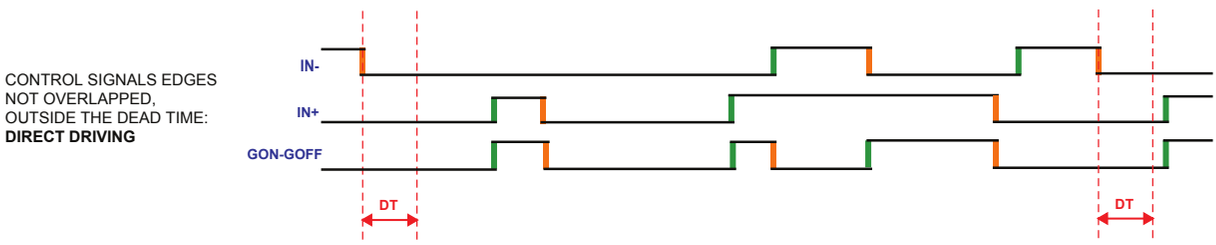


Figure 10. **Control edges signal not overlapped and outside DT (direct control)**



When the deadtime function is enabled, the STGAP1BS returns a “deadtime violation” fault when the control unit tries to turn on any of the drivers in one leg during the counting of the programmed DT time. If such event occurs the DT_ERR flag is set high and latched.

7.3 Hardware RESET

The device can be reset by forcing the VREG pin to ground through an external switch. The internal regulator is designed to stand this condition.

The maximum current required to force the VREG pin to ground is indicated by the parameter I_{REG}.

7.4 Power supply UVLO and OVLO

Undervoltage protection is available on both VH and VL supply pins.

The turn-on threshold can be programmed through the SPI writing the CFG4 register. A fixed 1 V hysteresis will set the respective turn-off threshold.

Both UVLO protections can be independently disabled by setting the proper value in the CFG4 register.

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When VH voltage goes below the VH_{off} threshold, the output buffer goes in “safe state” and the UVLOH status flag is forced high. If the UVLOIatch bit in the CFG4 register is set low (default), the UVLOH status flag is released when VH voltage reaches the VH_{on} threshold and the device returns to normal operation.

Otherwise, the UVLOH flag is latched and the device remains in “safe state” until the VH voltage reaches the VH_{on} threshold and the flag is released. See Section 7.11 for indication on how the failure flags can be released.

When VL voltage goes over the VL_{off} threshold, the output buffer goes in “safe state” and the UVLOL status flag is forced high. If the UVLOIatch bit in the CFG4 register is set low (default), the UVLOL status flag is released when VL voltage goes below the VLon threshold and the device returns to normal operation.

Otherwise. the UVLOL flag is latched and the device remains in “safe state” until the VL voltage goes below the VL_{on} threshold and the flag is released. See Section 7.11 for indication on how the failure flags can be released.

Overvoltage protection is available on both VH and VL supply pins. Both OVLO protections can be disabled by setting the proper value in the CFG4 register.

When the VH voltage goes over the OV_{VHoff} threshold, the output buffer goes in “safe state” and the OVLOH status flag is forced high. The OVLOH flag is latched and the device remains in “safe state” until VH voltage goes below the overvoltage threshold and the flag is released. See Section 7.11 for indication on how the failure flags can be released.

When VL voltage goes over the OV_{VLoff} threshold, the output buffer goes in “safe state” and the OVLOL status flag is forced high. The OVLOL flag is latched and the device remains in “safe state” until VH voltage goes below the overvoltage threshold and the flag is released. See Section 7.11 for indication on how the failure flags can be released.

7.5 Thermal warning and shutdown protection

The device provides a thermal warning and a thermal shutdown protection.

When junction temperature reaches the T_{WN} temperature threshold the TWN flag in the STATUS1 register is forced high. The TWN flag is released as soon as the junction temperature is lower than T_{WN} - T_{hys}.

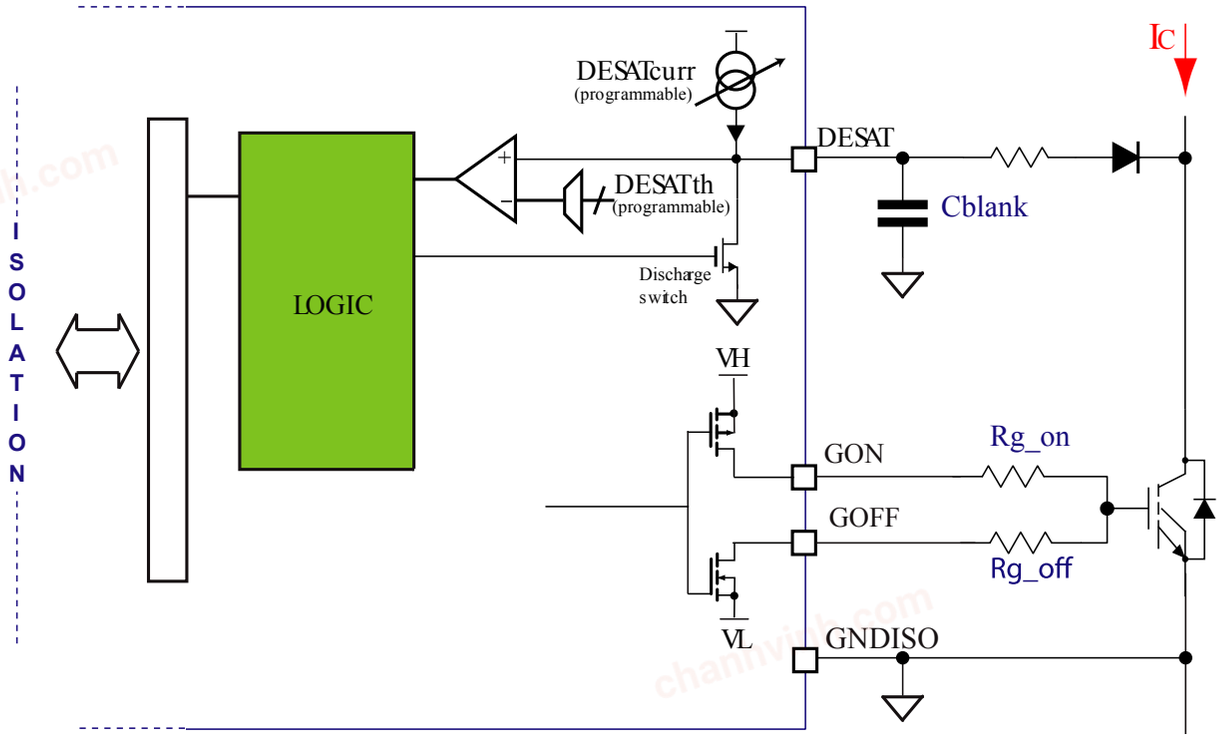
When junction temperature reaches the T_{SD} temperature threshold, the device is forced in “safe state” and the TSD flag in the STATUS1 register is forced high. The device operation is restored and the TSD flag is released as soon as the junction temperature is lower than T_{SD} - Thys.

7.6 Desaturation protection

This feature allows implementing an overload protection for the IGBT. The DESAT pin monitors the V_{CE} voltage of the IGBT while it is on, and if the protection threshold is reached, the IGBT is turned off.

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Figure 11. **Example of desaturation protection connection**



When the IGBT is off (GOFF output is activated) the DESAT pin is kept low internally and the external blanking capacitor connected to the DESAT pin is discharged (the internal current generator is fully switched off and the switch between DESAT and GNDISO pins is turned on).

When the GON output is activated the switch between DESAT and GNDISO pins is turned off and an internal programmable current generator (I_{DESAT}) starts charging the external blanking capacitor after a fixed blanking time t_{BLK}.

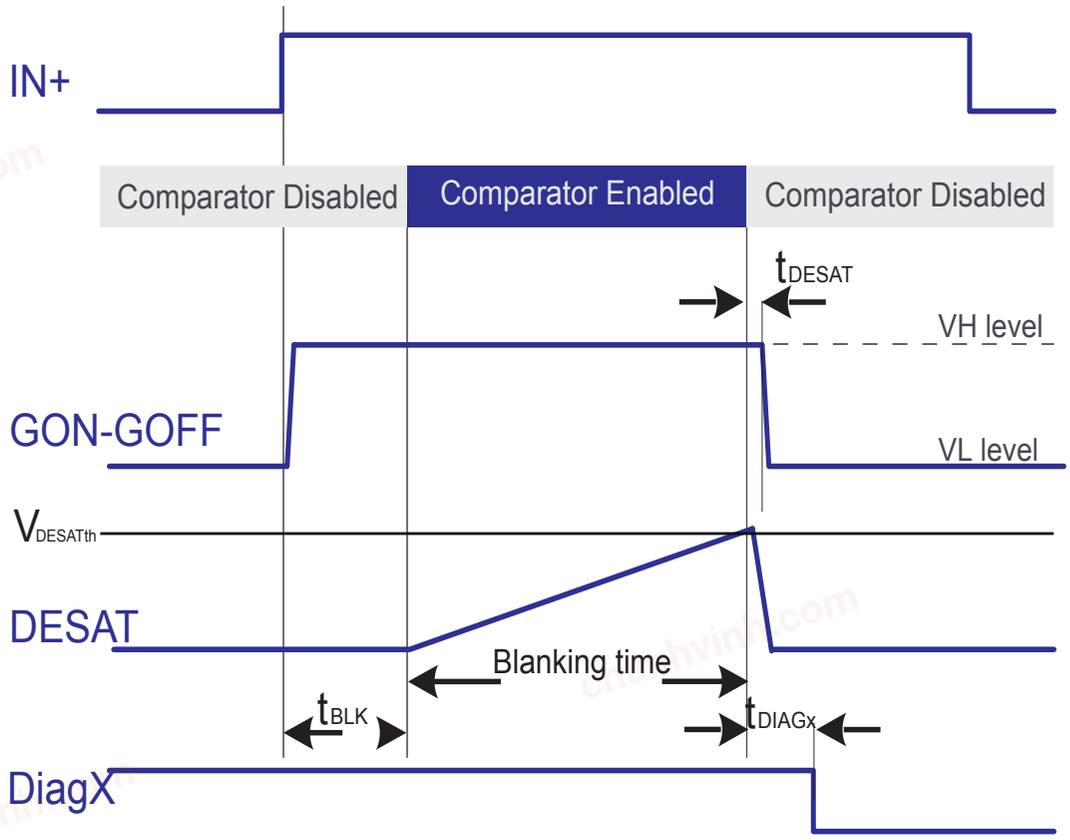
If a desaturation event occurs the V_{CE} voltage increases and the voltage at the DESAT pin reaches the desaturation threshold $V_{DESATth}$: the DESAT comparator output is set, the device is forced in “safe state” and the DESAT flag is forced high and latched.

The DESAT comparator is not active when the external IGBT is off or after desaturation detection (see Figure 12).

Both the $V_{DESATth}$ threshold and the I_{DESAT} blanking current are programmable through the SPI.

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Figure 12. **DESAT protection timing diagram**



A deglitch filter is applied to the DESAT pin. Each pulse exceeding the $V_{DESATth}$ for a time shorter than $t_{DESfilter}$ value shall not trigger the protection.

7.7 V_{CE} active clamping protection

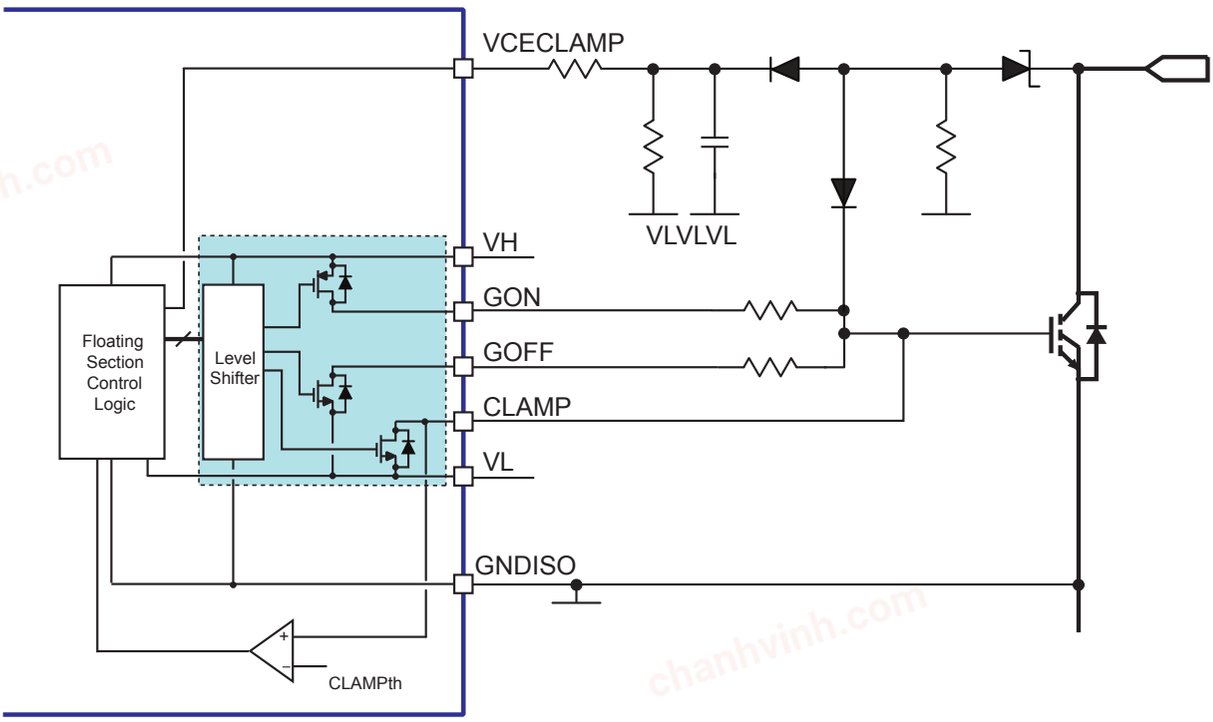
This protection is used to actively clamp the drain/collector overvoltage spikes during the MOSFET/IGBT turn-off. This feature allows using low turn-off resistor values leading lower turn-off losses, thus increasing efficiency, while limiting the maximum turn-off spike on the collector (or drain) within safe limits.

The direct feedback of the collector voltage to the device can for example be made via an element with avalanche characteristics such as a TVS. If the V_{CE} voltage exceeds the breakdown voltage of the TVS, the $V_{VCECLth}$ threshold voltage on the VCECLAMP is reached and the IC actively slows down the power switch turn-off to keep a safe condition.

The active limiting of the driver's turn-off current strongly reduces the current flowing through the TVS, thus preventing it from operating in overstressing conditions.

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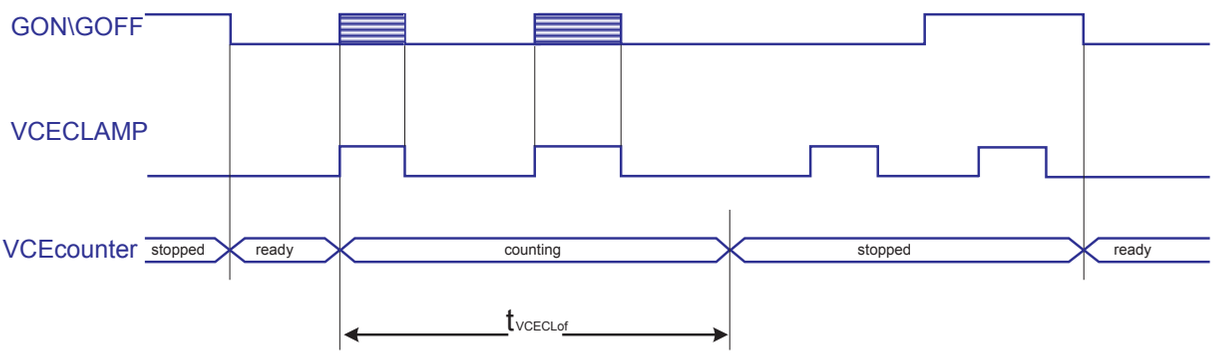
Figure 13. **Example of V_{CE} active clamping protection connection**



When the VCECLAMP is activated during the turn-off phase a watchdog timer starts inside the driver. This timer allows the VCECLAMP pin to act on the driver's output status for a $t_{VCECLoff}$ time maximum. After that time has expired, the driver continues the normal turn- off ignoring the VCECLAMP pin status. This assures that the protection is only acting to clamp inductive V_{CE} spikes during the turn-off.

The timer is reset and the VCECLAMP protection is enabled again at the beginning of the following turn-off sequence.

Figure 14. **VCECLAMP timing diagram**



The VCECLAMP pin is masked and has no effect on the driver's outputs status when the external MOSFET/IGBT is on.

The V_{CE} active clamping protection can be disabled connecting the VCECLAMP pin to VL.

7.8 SENSE overcurrent protection

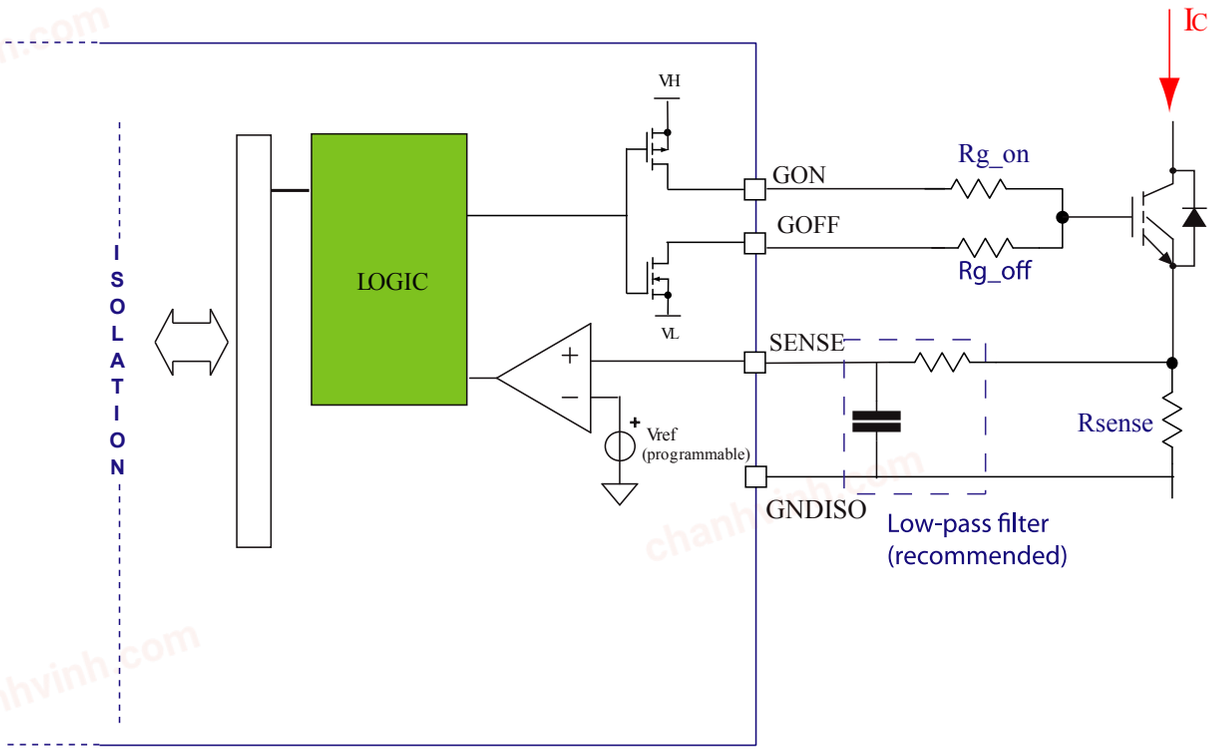
This function is suitable in applications in which it is possible to measure the load current through the use of a shunt resistor, or in applications that use IGBTs with the current sense pin available. The load current (or a fraction of it in case SenseFETs are used) is converted to voltage by an external shunt resistor and is fed to the SENSE pin (comparator input).

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When an overcurrent event occurs the sense voltage reaches the $V_{SENSEth}$ threshold, the device is forced in “safe state” and the SENSE status flag is forced high and latched.

The $V_{SENSEth}$ threshold is programmable through the SPI (refer to Section 9.2.2).

Figure 15. Example of SENSE overcurrent protection connection



7.9 Miller clamp function

The Miller clamp function allows the control of the Miller current during the power stage switching in half-bridge configurations. When the external power transistor is in the OFF state, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch in the same leg is being turned on, due to the C_{gc} capacitance.

During the turn-off period the gate of the external switch is monitored through the CLAMP pin.

The CLAMP switch is activated when gate voltage goes below the voltage threshold $V_{CLAMPth}$, thus creating a low impedance path between the switch gate and the VL pin.

This function can be disabled setting low the CLAMP_EN bit in the CFG5 register (high by default).

7.10 2-level turn-off function

If an overcurrent event happens, a large voltage overshoot exceeding V_{CE} absolute ratings may occur across the power switch during the turn-off, due to the parasitic stray inductances.

The 2-level turn-off function (2LTO) allows the reduction of the stressing overvoltage experienced by the power component in overcurrent condition by switching off the external power in two phases.

In the first phase, the GOFF voltage is actively forced to a programmable value V_{2LTOth}; after a programmable delay $t_{2LTOtime}$ the GOFF is forced to VL to complete the gate turn-off.

This allows to slow down the critical part of the turn-off transient, that may induce the overvoltage spikes.

The voltage level V_{2LTOth} and duration $t_{2LTOtime}$ of the intermediate off-level are programmable through the SPI.

It is possible to program when this feature takes place, refer to the following paragraphs.

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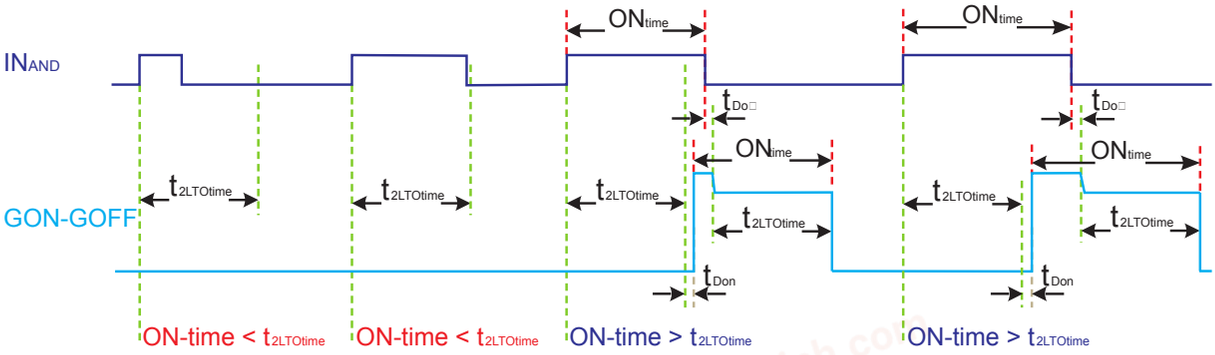
7.10.1 2-level turn-off function - Always

The 2LTO is performed at each turn-off transition (2LTO_EN = '0').

When 2LTO is used, at each transition the minimum on or off pulse width is determined by 2LTO time. Some sample waveforms are given in Figure 16 and Figure 17, where IN_{AND} represents the condition: < IN+ = 'H' and IN- = 'L' >.

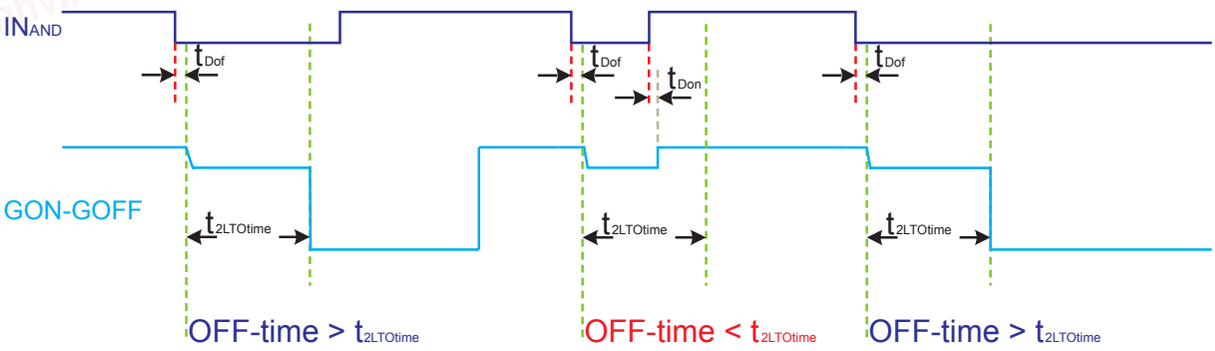
If a turn-on pulse is shorter than $t_{2LTOtime}$ it shall be ignored; turn-on pulses longer than $t_{2LTOtime}$ will determine a delay in the turn-on equal to $t_{2LTOtime}$ (see Figure 16).

Figure 16. Example of short turn-on pulses when 2LTO occurs at each cycle



When a turn-off pulse is detected the turn-off procedure starts immediately by forcing the V_{2LTOth} voltage on the GOFF pin. If the duration of the turn-off pulse is shorter than $t_{2LTOtime}$ the turn-off sequence is aborted by setting GOFF in high impedance and turning GON on again (see Figure 17).

Figure 17. Example of short turn-off pulse when 2LTO occurs at each cycle



When the 2LTO is used at each cycle, any event that forces the device to enter in “safe state” generates a driver switch off performing a 2LTO sequence.

7.10.2 2-level turn-off function - Fault

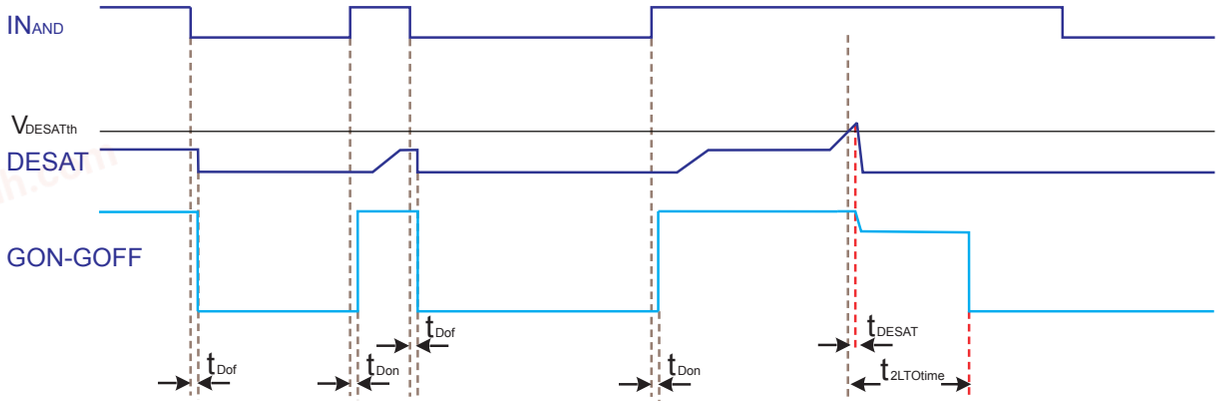
The 2LTO is performed only after a desaturation or overcurrent event (2LTO_EN = '1'). In such cases the device enters in “safe state” until the failure flag is released. See Section 7.11 for indication on how the failure flags can be released.

This configuration overrides some drawbacks of using the 2LTO at each turn-off, such as the minimum pulse width equal to $t_{2LTOtime}$ and the turn-on delay needed to avoid duty cycle distortion.

With this configuration the turn-off is only slowed down in case of desaturation or overcurrent events.

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Figure 18. **Example of operation with 2LTO in “Fault” mode**



7.10.3 2-level turn-off function - Never

The 2LTO function is disabled (2LTOtime = 0x0). In this case a standard turn-off sequence is used (directly lowering the gate voltage from VH to VL) also in case of desaturation or sense overcurrent events.

7.11 Failure management

The device provides advanced diagnostic through open drain outputs ($\overline{DIAG1}$/$\overline{DIAG2}$) and internal status registers. The $\overline{DIAG2}$ output shares the same pin of the IN- input (see Figure 1); the diagnostic signal through the pin is enabled through the DIAG_EN bit as described in Section 7.1 .

Status registers (STATUS1, STATUS2 and STATUS3) provide failures and status information as listed in respective paragraphs.

$\overline{DIAG1}$ and $\overline{DIAG2}$ pins can be programmed through the dedicated registers (DIAG1CFG and DIAG2CFG) to signal one or more failure conditions. The output value is the result of the NOR of the selected status bits: if one of the selected bits is high, the output is forced low.

Some of the failure conditions reported by the status registers are latched, i.e.: the flag is kept high even if the triggering condition is expired.

Different methods can be used to clear the failure flags contained in the status registers:

- **Using the ResetStatus command**

  The $\overline{SD}$ must be set low before giving this command and must remain low until the end of the command’s execution time.

  This is the recommended method, because guarantees that status registers are only cleared by direct intervention of the MCU.

  All flags in the StatusRegisters are released after a t_{desCS} time following the rise of the SPI $\overline{CS}$.

- **Forcing low the $\overline{SD}$ pin for at least $t_{release}$**

  All the flags are released at the rising edge of the $\overline{SD}$. This mode is enabled at device’s power-on, but it can be disabled by setting the $\overline{SD}$_FLAG configuration bit low during the configuration phase, and by doing this any possibility to clear a FLAG without direct intervention of the MCU is prevented. Even if the $\overline{SD}$_FLAG is set high, status registers are not cleared after the rising edge of the $\overline{SD}$ if a configuration sequence is executed (`StartConfig`, `StopConfig`). This is done to avoid clearing errors that may have been generated during the configuration procedure.

- **Using HW reset** (see Section 7.3)

  In this case the device behaves as after power-up sequence.

In any of the above cases, if the failure condition is still present, the respective flag is not released.

Selected failures force the device in “safe state”; the device remains in this state until the relative status flags are released. Refer to Table 49, Table 51 and Table 53 for details.

The possibility to clear status registers by setting the $\overline{SD}$ low allows operating the device also without using the SPI interface. In order to avoid an unintended clear of fault conditions it is recommended to disable this functionality by setting the $\overline{SD}$_FLAG = '0'.

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7.12 Asynchronous stop command

The ASC pin allows to turn-on the GON output acting directly on the isolated driver logic and regardless of the status of the input pins IN+, IN- and $\overline{SD}$. This pin is active high.

The status of this pin is mirrored in the ASC bit present in the STATUS2 register.

The power supply of the isolated section must be present (VH > VH_{on}).

In case UVLO on VH is not enabled, ASC function works for VH values within the recommended operating values.

This function works even if the VDD voltage is not available or is in UVLO condition.

The priority of such command is lower than that of DESAT and SENSE pins, so the ASC command is ignored in case of a desaturation or overcurrent fault. After such events the gate can be turned on again with a low-to-high transition of the ASC pin, or by clearing the fault condition (see Section 7.11).

7.13 Watchdog and echo

The isolated side provides a watchdog function in order to identify when it is no more able to communicate with the LV side. In this case the driver is automatically forced in “safe state” and the REGERRR flag is set.

When the LV side is in the standby mode, turned off or in hardware reset condition, the isolated side watchdog is still operative and the REGERRR flag is set.

The low voltage side provides a watchdog function in order to identify when it is no more able to communicate with the isolated side. In this case the REGERRL flag is set and the device is forced in “safe state”.

An echo function is implemented in order to check that input commands toward the gate are correctly propagated to the driver's output. In case something should prevent the correct propagation of the command, the driver is able to detect this condition and will start a new communication (echo) in order to set the desired output state. This process has typical duration of 4 µs.

7.14 Security check functions

The device allows verifying the gate and sense resistor connections and the functionality of SENSE and DESAT. This can be achieved through the following security checks:

- Logic inputs to isolated driver path
- GON to gate path
- GOFF to gate path
- SENSE comparator
- SENSE resistor
- DESAT comparator

The check modes are enabled through a dedicated configuration register TEST1 (refer to Section 9.2.9) and thus require entering in configuration mode.

Only one check mode at a time must be enabled. At the end of security check procedure, the TEST1 register must be set to 0x00 before running the device in normal mode.

It is recommended to clear the status register with the `ResetStatus` command before and after each check.

To prevent the $\overline{SD}$ from clearing the STATUS flags, set the $\overline{SD}$_FLAG = '0' as described in Section 7.11 .

7.14.1 Logic inputs to isolated driver path

The purpose of this security check is to verify the path integrity including the input buffer.

The check uses bit #[0] of the STATUS2 register, which contains information about the gate status request that the gate driver stage received from the logic inputs and reported. Please note that this value may differ from the actual GON and GOFF status, for example if some condition is forcing the device in “safe state”.

To perform this test, the following procedure has to be followed:

- Set $\overline{SD}$ = high, IN- = low and IN+ = low
- Set IN+ = high
- Wait at least t_{Gchk}

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- Read GATE bit in the STATUS2 register
  - GATE = '1' → OK
  - GATE = '0' → FAIL
- Set IN+ = low

During all the duration of the check the logic inputs have to follow the levels indicated by the procedure and must not be otherwise modified.

Please note that when IN+ is set high during the check, the gate may be forced high (GON turned on). The user test routine has to take into account this behavior.

7.14.2 GON to gate path check

The purpose of this security check is to verify the path integrity including the driver's GON output, the GON (turn-on) gate resistor, the power switch gate and the CLAMP pin (see Figure 19).

To perform this test, the following procedure has to be followed:

- Set $\overline{SD}$ = low
- Send `StartConfig` command
- Set GONCHK = '1'
- Send `StopConfig` command
- Wait at least t_{Gchk}
- Read TSD flag
  - TSD = '0' → OK ($V_{CLAMP} > V_{Gchk}$)
  - TSD = '1' → FAIL ($V_{CLAMP} < V_{Gchk}$)

Please note that during all the time the check is enabled the gate will be forced high (GON turned on) regardless the $\overline{SD}$ pin level. The user test routine has to take into account this behavior.

In any case, when GONCHK = '1', the protections SENSE and DESAT, if enabled, will continue to operate protecting the power switch regardless the $\overline{SD}$ pin.

7.14.3 GOFF to gate path check

The purpose of this security check is to verify the path integrity, including the driver's GOFF output, the GOFF (turn-off) gate resistor, the power switch gate, and the CLAMP pin (see Figure 19).

To perform this test, the following procedure has to be followed:

- Set $\overline{SD}$ = low
- Send `StartConfig` command
- Set GOFFCHK = '1'
- Send `StopConfig` command
- Wait at least $t_{Gchk} + t_{GATE_GOFFchk}$
- Read DESAT flag
  - DESAT = '0' → OK ($V_{CLAMP} < V_{CLAMPth}$)
  - DESAT = '1' → FAIL ($V_{CLAMP} > V_{CLAMPth}$)

During the check, a small current $I_{GOFFchk}$ will be sourced from the CLAMP pin while GOFF is on, keeping the gate low through the turn-off gate resistor.

To ensure the check result, some applicative conditions have to be verified:

- The bleeding resistor, sometimes present between the gate and source in the power switch, shall be higher than 8.2 kΩ.
- During the test, the power switch gate shall have the time to be charged up to $V_{CLAMPth}$ by $I_{GOFFchk}$. In case no bleeding resistor is present, this time can be roughly computed as:

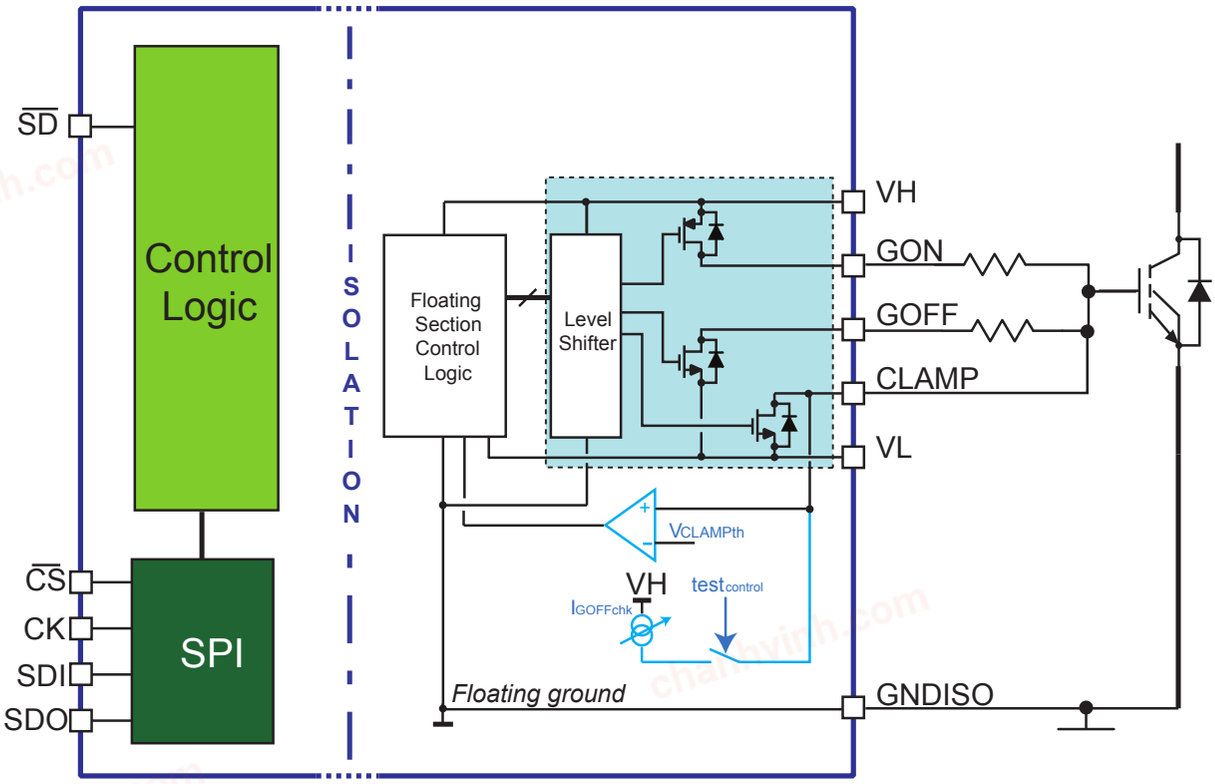
  $t_{GATE_GOFFchk} \approx C_{GATE} * (V_{CLAMPth} - VL) / I_{GOFFchk}$

  If a bleeding resistor is present or an additional push-pull circuit has been added, the time has to be computed with the adequate corrective factors.

If the check fails due to the lack of the GOFF resistor, the power switch gate will gradually rise up to VH with no protections of SENSE nor DESAT. The user test routine shall consider this behavior.

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Figure 19. **Gate paths check circuitry**



7.14.4 SENSE comparator check

The purpose of this security check is to verify the functionality of the sense comparator.

To enable this check, it is necessary to set SNSCHK = '1' and SENSE_EN = '1'.

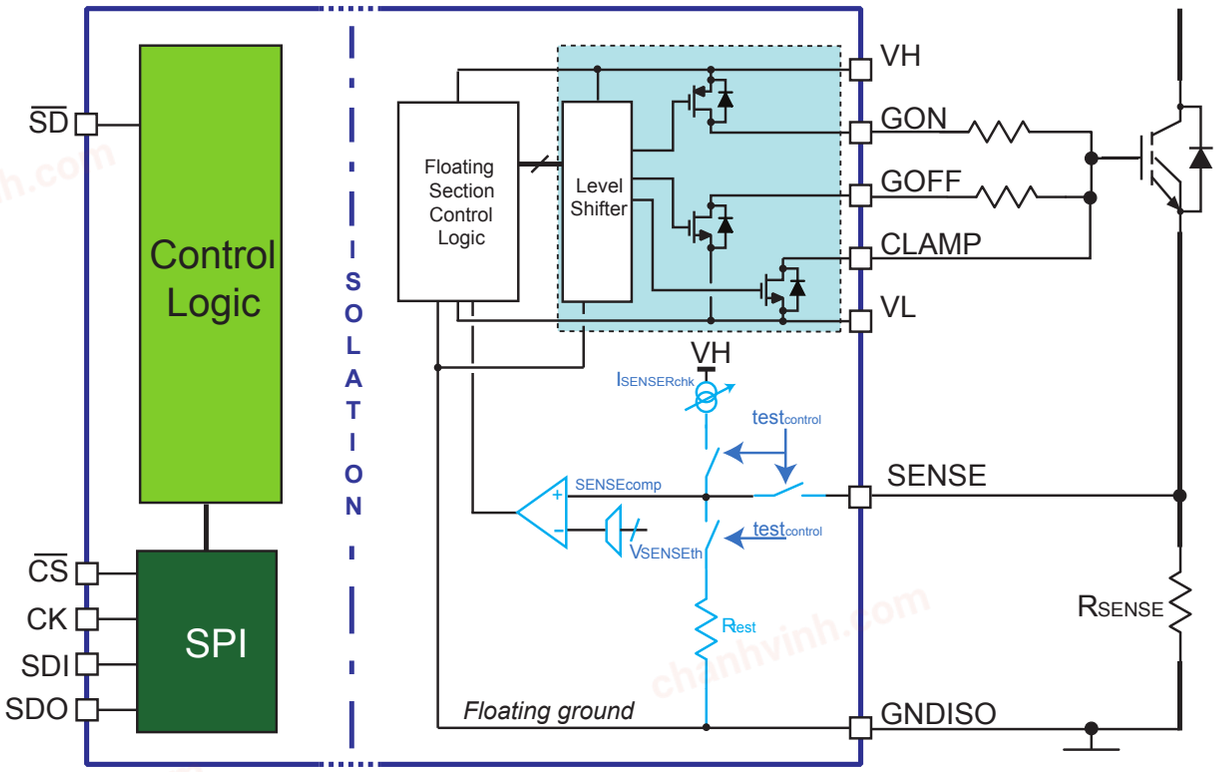
When this check is enabled the switch in series to the SENSE pin is open (see Figure 20); a SENSE fault (STATUS1 register) should be reported within $t_{SENSEchk}$, otherwise the SENSE comparator operation is compromised.

- $V_{SENSEcomp} > V_{SENSEth}$ → comparator OK → SENSE = '1'
- $V_{SENSEcomp} < V_{SENSEth}$ → comparator FAIL → SENSE = '0'

The SENSE fault generated by this test is latched and shall be cleared accordingly.

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Figure 20. **SENSE comparator and resistor check circuitry**



7.14.5 SENSE resistor check

The purpose of this security check is to verify the connection between the device and the sense shunt resistor and to verify the optional sense resistor filter network is not open.

To perform this test, the following procedure has to be followed:

- Set $\overline{SD}$ = low
- Send `StartConfig` command
- Set SENSE_EN = '1'
- Set RCHK= '1'
- Send `StopConfig` command
- Wait t_{Rchk} + $t_{SENSERchk}$
- Read SENSE flag
  - SENSE = '0' → OK (V_{SENSE} < $V_{SENSEth}$)
  - SENSE = '1' → FAIL (V_{SENSE} > $V_{SENSEth}$)

During the check a small current $I_{SENSERchk}$ is sourced from the SENSE pin (see Figure 20). If the sense resistor is not present or floating, SENSE pin voltage will rise and once $V_{SENSEth}$ is exceeded, a SENSE fault will be reported in the STATUS1 register within t_{Rchk}.

To ensure the check result, the following condition has to be verified:

- The SENSE flag read has to be delayed of $t_{SENSERchk}$, which is the time the customer filtering network takes to reach $V_{SENSEth}$ by the $I_{SENSERchk}$ current.

7.14.6 DESAT comparator check

The purpose of this security check is to verify the functionality of the desaturation comparator.

To perform this test, the following procedure has to be followed:

- Set $\overline{SD}$ = low
- Send `StartConfig` command

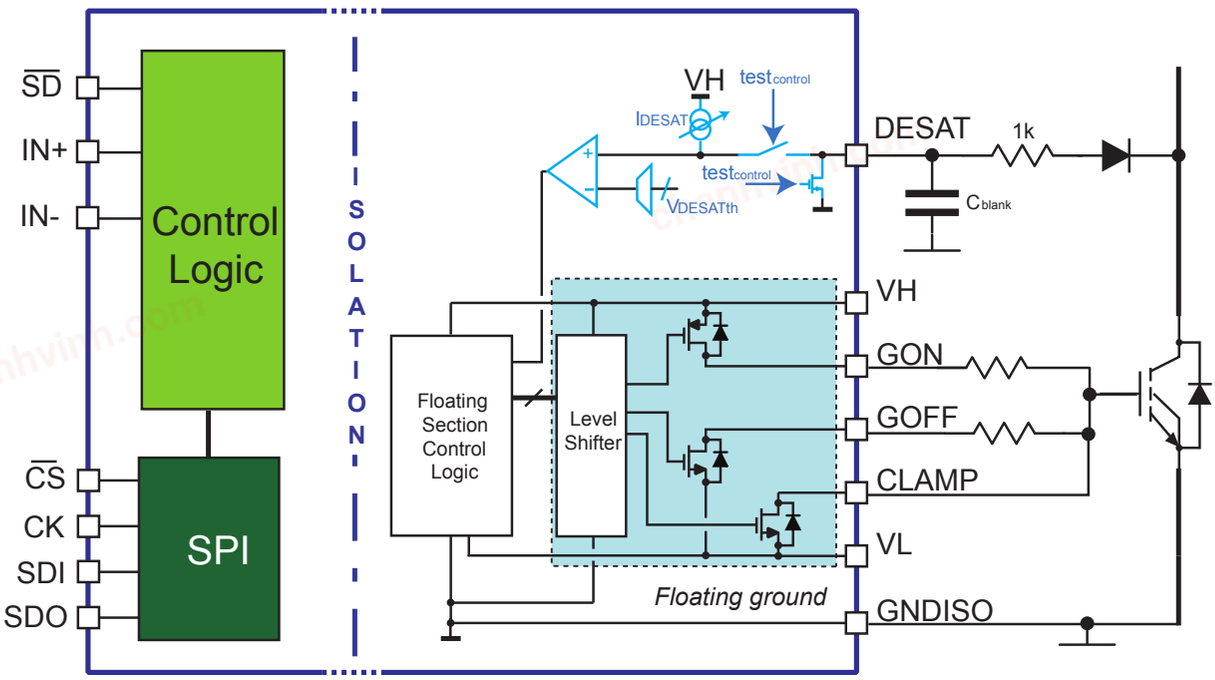
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- Set DESAT_EN = '1'
- Set DESCHK = '1'
- Send `StopConfig` command
- Set $\overline{SD}$ = high
- Wait 3 µs
- Apply at the inputs a gate turn on pulse longer than 500 ns
- Read DESAT flag
  - DESAT = '1' → OK ($V_{DESATcomp} > V_{DESATth}$)
  - DESAT = '0' → FAIL ($V_{DESATcomp} < V_{DESATth}$)

During this test GON is first turned on and then turned off as soon the test succeeds. In case the test should fail, the output remains on as long as the input signal remains high.

At the end of the check the DESAT fault remains set (it is latched), and it has to be cleared.

Figure 21. DESAT comparator check circuitry



7.15 Register corruption protection

All the configuration registers are protected against content corruption.

If the value of a local register is changed without a proper command is received (`WriteReg` or `GlobalReset`), the REGERRL flag is set high and the device is forced in “safe state”.

If the value of a remote register is changed without a proper command is received (`WriteReg` or `GlobalReset`), the REGERRR flag is set high and the device is forced in “safe state”.

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8 SPI interface

The IC communicates with an external MCU through a 16-bit SPI. This interface is used to set the device parameters and for advanced diagnostic.

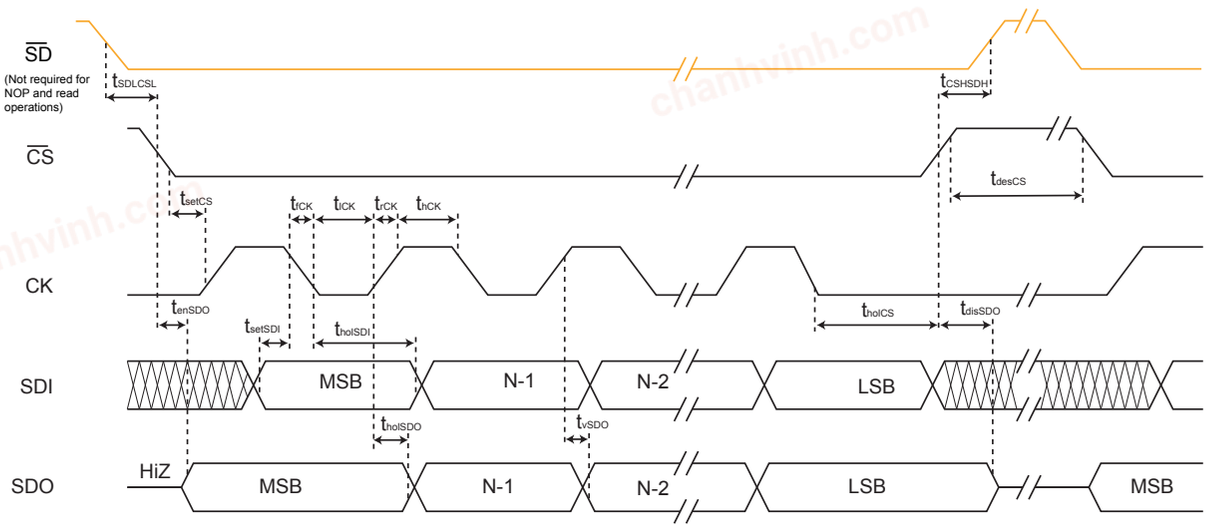
SPI commands are executed after the rising edge of the $\overline{CS}$, and adequate wait time must be respected before a new command is started by setting the $\overline{CS}$ low again. Refer to the t_{desCS} parameter in Table 6 for required wait time after each command.

The SPI I/O pins are:

- $\overline{CS}$: chip select (active low)
- CK: serial clock
- SDI: serial data input (MOSI)
- SDO: serial data output (MISO).

The interface is compliant with the SPI standard CPHA = 1 and CPOL = 0 (serial data is sampled on CK falling edge and it is updated on CK rising edge, at the $\overline{CS}$ falling edge the CK signal must be low) as shown in Figure 22.

Figure 22. SPI timings



The SPI interface can work up to 5 Mbps and provides the daisy chain feature.

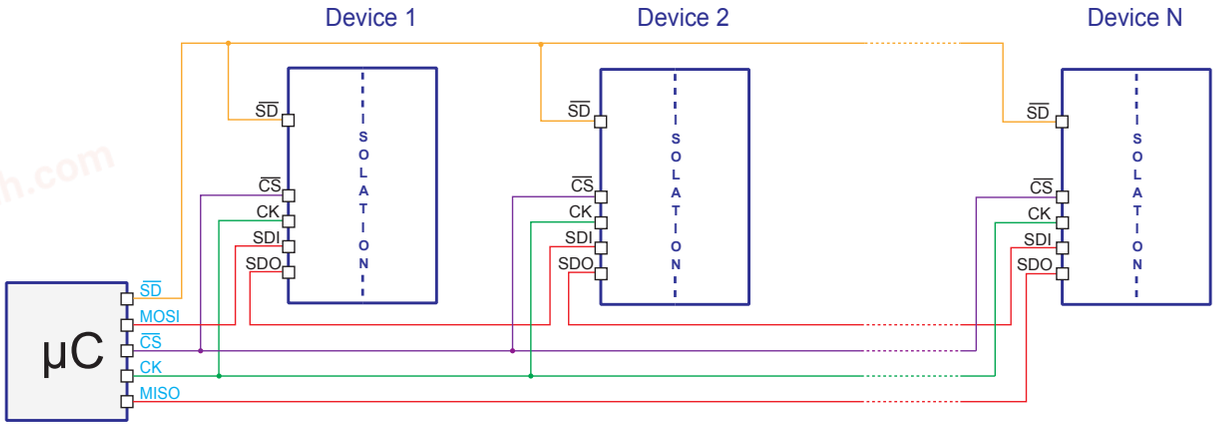
In order to guarantee a safe operation and robustness to electrical noise, the number of rising edges within a $\overline{CS}$ negative pulse must be multiple of 16, otherwise the communication cycle is ignored and a communication failure is indicated forcing high the SPI_ERR flag.

Any number of the STGAP1BS can be connected in daisy chain, and only 4 lines for the SPI and one for the $\overline{SD}$ are required in order to guarantee access to status and configuration registers of each device. An example of daisy chain configuration is shown in Figure 23.

In case that several STGAP1BS devices are connected in the SPI link, each of them can be configured in a different way by simply writing the desired data in each configuration and diagnostic register. This allows for example differentiating the configuration for high-side and low-side drivers.

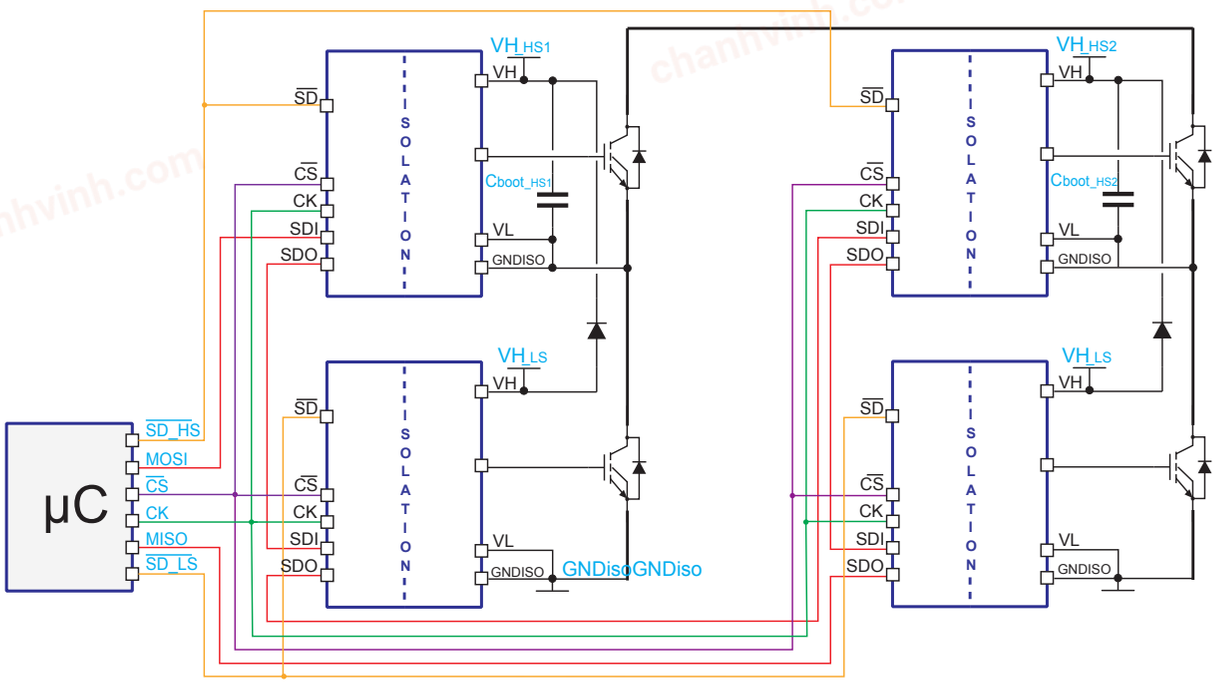
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Figure 23. **SPI daisy chain connection example**



In case a bootstrap capacitor and a diode are used to generate the VH supply voltage for the high-side drivers, it is recommended to have one dedicated $\overline{SD}$ line for all of the high- side drivers and another dedicated $\overline{SD}$ line for all of the low-side drivers. An example of such topology is shown in Figure 24.

Figure 24. **SPI daisy chain connection example when bootstrap technique is used for high-side drivers**



8.1 CRC protection

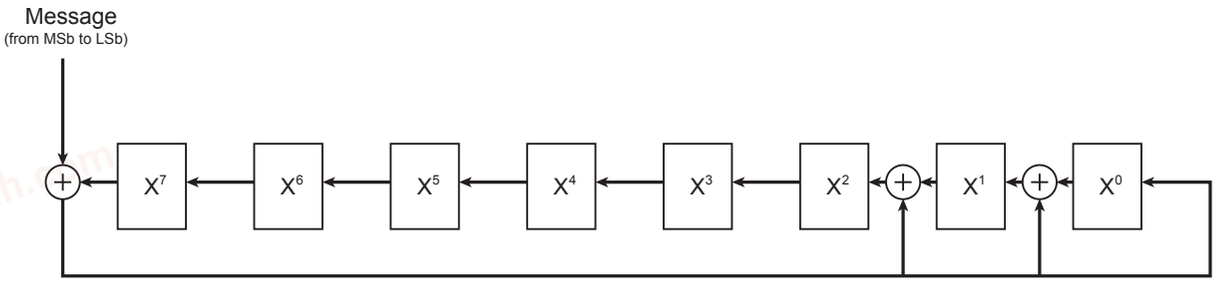
All the command and data bytes have to be followed by a CRC code. If the CRC_SPI bit is set high, this code is used to check the data byte is correct, otherwise the CRC byte is ignored. In this case the CRC byte must be transmitted by the host, but its value is unimportant.

A failure on the CRC check causes the respective data byte is ignored and the SPI_ERR flag is set high.

The polynomial generator of the CRC code is $X^8 + X^2 + X + 1$ corresponding to the block diagram in Figure 25.

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Figure 25. **Block diagram of the CRC generator**



The host must transmit to the device the inverted CRC code computed using the following procedure:

- Initialize CRC to all 1
- Start the calculation from the most significant bit of the message
- Invert the CRC result

In case of a `WriteReg` command, the CRC of the data byte (i.e.: the new register value) must be calculated initializing the computation system to the CRC of the command byte (i.e., the CRC is calculated on a 16-bit message composed by the command + data byte). This way a data byte cannot be accepted as a command byte and vice-versa. Some examples are listed in Table 11.

The device always transmits a response byte followed by a CRC computed using the same polynomial generator ($X^8 + X^2 + X + 1$). The CRC byte transmitted by the device is not inverted.

If no response is required, the word returned by the device has no meaning and it should be discarded. Some examples are listed in Table 12.

Table 11. **CRC byte examples (from host to device)**

Command	Command byte	Command CRC	Data byte	Data CRC
StopConfig	0x3A	0xAA	N.A.	N.A.
WriteReg(CFG1, 0x20)	0x8C	0xA1	0x20	0x82
WriteReg(CFG5, 0x06)	0x99	0xCA	0x06	0x66
ResetStatus	0xD0	0x32	N.A.	N.A.
ReadReg(CFG3)	0xBE	0x3F	N.A.	N.A.

Table 12. **CRC byte examples (from device to host)**

Data byte	Data CRC
0x00	0xF3
0xEA	0x6B
0xF5	0x36
0x2A	0x25

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9 Programming manual

9.1 SPI commands

Table 13. **SPI commands**

Command mnemonic	Command value								Action	Notes
StartConfig	0	0	1	0	1	0	1	0	Device configuration start	Enter CFG mode $\overline{SD}$ low only
StopConfig	0	0	1	1	1	0	1	0	Device configuration/check completed	Leave CFG mode $\overline{SD}$ low only
NOP	0	0	0	0	0	0	0	0	No operation	-
WriteReg	1	0	0	A	A	A	A	A	Write AAAAA register	CFG mode only
ReadReg	1	0	1	A	A	A	A	A	Read AAAAA register	-
ResetStatus	1	1	0	1	0	0	0	0	Reset all the status registers	$\overline{SD}$ low only
GlobalReset	1	1	1	0	1	0	1	0	Global reset	CFG mode only
Sleep	1	1	1	1	0	1	0	1	Device enters in standby mode	$\overline{SD}$ low only

9.1.1 StartConfig and StopConfig commands

Table 14. **StartConfig command synopsis**

Byte	1	2
To device	0010 1010	1101 1010(1)

1. *The CRC byte of the command, if the CRC check is disabled this byte is ignored.*

Table 15. **StopConfig command synopsis**

Byte	1	2
To device	0011 1010	1010 1010(1)

1. *The CRC byte of the command, if the CRC check is disabled this byte is ignored.*

Device parameters are configured by writing configuration values in configuration registers (CFGx and DIAGxCFG), which is only possible by entering in configuration mode.

To switch the device to the configuration mode the `StartConfig` command must be sent. This command is accepted when the $\overline{SD}$ line is low only. If the command has been correctly received and interpreted, the IC registers writing is enabled.

The $\overline{SD}$ pin must be kept low during the whole configuration procedure, which is terminated by the `StopConfig` command. If the $\overline{SD}$ pin is raised during the configuration procedure the device immediately quits the configuration mode causing a fault error indicated by the REGERRL and REGERRR bits. In this case all the changes operated on device configuration are undone and the previous configuration is restored.

At the end of the device setup, the `StopConfig` command has to be sent in order to quit the configuration mode and make all changes effective.

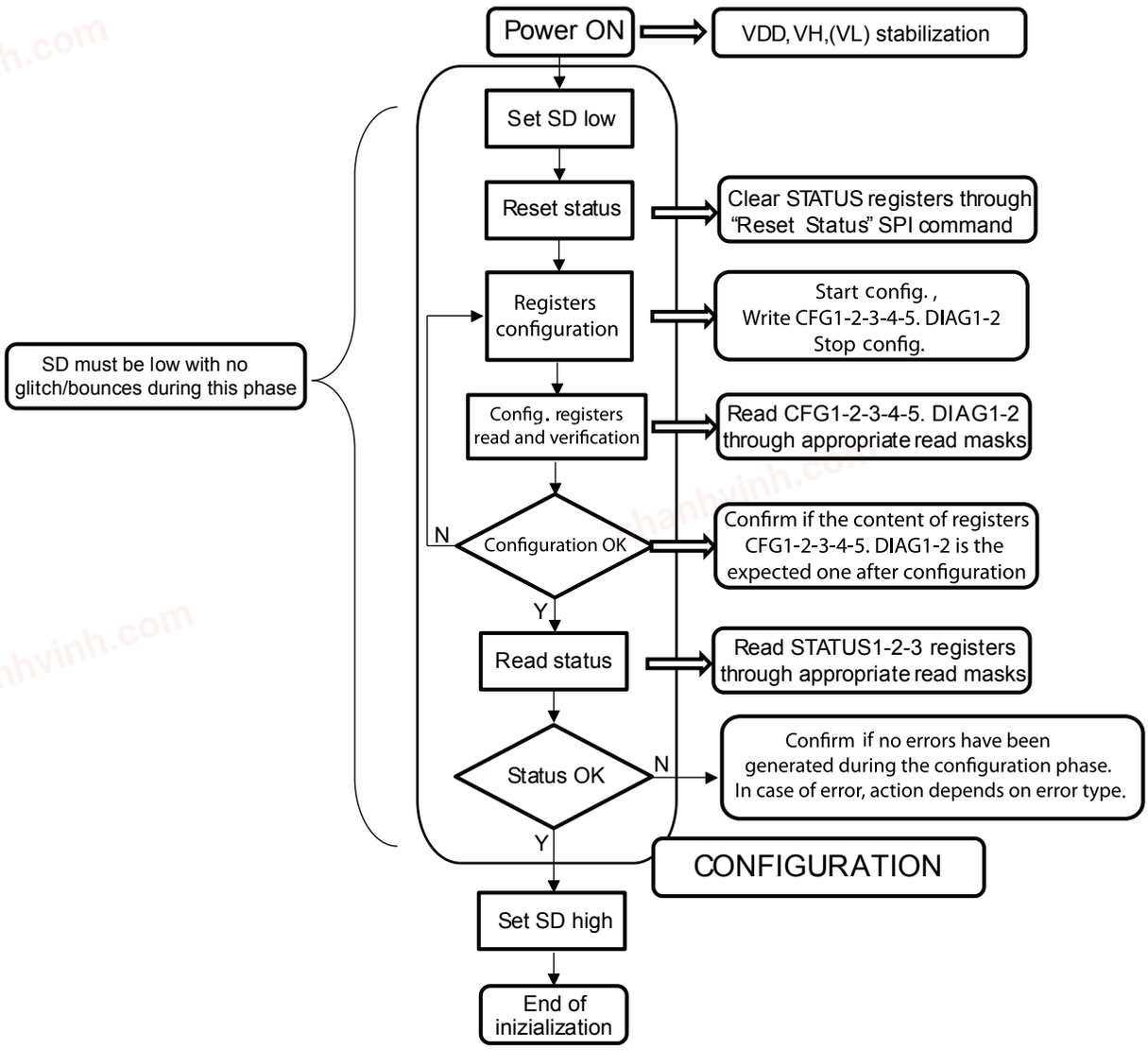
Configuration sequence must be repeated every time the power supply on either side (VDD or VH) is removed and then restored.

- VDD falling below critical value will result in the REGERRL flag being set in status registers after that the proper VDD level is restored.
- VH falling below critical value will result in the REGERRR flag being set in status registers.

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After that all supply voltages are supplied and stable, the configuration process can be executed. The flow chart shown in Figure 26 is recommended for the configuration. In this way it will be possible to check that the desired configuration has been correctly stored in the device at the end of the configuration sequence.

Figure 26. STGAP1BS recommended configuration flow



9.1.2 WriteReg command

Table 16. WriteReg command synopsis

Byte	1	2	3	4
To device	100A AAAA(1)	CCCC CCCC(2)	DDDD DDDD(3)	KKKK KKKK(4)

1. *The command byte where AAAAA is the address of the target register.*
2. *The CRC byte of the command, if the CRC check is disabled this byte is ignored.*
3. *Data to be written into the target register.*
4. *The CRC byte of the command and data, if the CRC check is disabled this byte is ignored.*

The device register can be written through the `WriteReg` command when the device is set in the configuration mode only (refer to Section 9.1.1), otherwise the write command is ignored and the SPI_ERR flag is forced low.

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The WriteReg command is followed by the data to be written into the target register. The CRC code following the data is based on both command and data bytes. In this way, in case of communication error, a data byte cannot be decoded as a command and vice-versa (refer to Section 8.1).

9.1.3 ReadReg command

Table 17. ReadReg command synopsis

Byte	1	2	3(1)	4
To device	101A AAAA(2)	CCCC CCCC(3)	0000 0000	CCCC CCCC(4)
From device	0000 0000	0000 0000	DDDD DDDD(5)	KKKK KKKK(6)

1. *Proper time have to be waited in order to allow the device to prepare the data.*
2. *The command byte where AAAAA is the address of the target register.*
3. *The CRC byte of the command, if the CRC check is disabled this byte is ignored.*
4. *The CRC byte of the NOP command.*
5. *Data read from the target register.*
6. *The CRC byte of the data.*

All the registers of the device can be read anytime, and this requires two accesses ($\overline{CS}$ must be asserted LOW and HIGH twice). In the first access the SPI host issues the ReadReg command (including the register address) and the CRC of the first byte, which will be ignored if SPI CRC is not enabled. After the command is received and decoded by the device, the register value and the respective CRC code is prepared for the transmission. The CRC polynomial used by the device during the transmission is different from the one used by the host, but the CRC code is not inverted before transmission (refer to Section 8.1).

The time required to obtain the reading result changes according to the side where the register is located. The reading of a local register (low voltage side) is available in 800 ns. The reading of a remote register (isolated side), if no communication error occurs between the two sides of the device, is available in 30 µs.

After the read result is ready it is stored in the SPI output buffer, and the host MCU will receive it as soon as it will send a new SPI command. Any command can be used for this purpose, including a NOP or the ReadReg command for the next register to be read.

Some status and configuration registers contain a reserved bit whose content is not predictable. In order to clearly identify the content of relevant information, the value read from each register should be masked with the appropriate masking code (see “Mask code” in Table 23).

9.1.4 ResetStatus and GlobalReset commands

Table 18. ResetStatus command synopsis

Byte	1	2
To device	1101 0000	0011 0010(1)

1. *The CRC byte of the command, if the CRC check is disabled this byte is ignored.*

The ResetStatus command is a specific reset command which acts on all status registers releasing all the latched flags. The command is executed only when the $\overline{SD}$ input is low, otherwise the SPI_ERR flag is forced low.

Table 19. GlobalReset command synopsis

Byte	1	2
To device	1110 1010	1001 0100(1)

1. *The CRC byte of the command, if the CRC check is disabled this byte is ignored.*

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The GlobalReset command reset all the registers to the default and releases all the failure flag (if latched). It can be sent when the device is in the configuration mode only, otherwise the command is ignored and the SPI_ERR flag is forced low.

9.1.5 Sleep command

Table 20. Sleep command synopsis

Byte	1	2
To device	1111 0101	1100 1001(1)

1. *The CRC byte of the command, if the CRC check is disabled this byte is ignored.*

The CRC byte of the command, if the CRC check is disabled this byte is ignored.

The command forces the device to switch in standby mode within a t_{sleep} period. The command is executed only when the $\overline{SD}$ pin in low, if the $\overline{SD}$ pin is high the command is ignored and the SPI_ERR flag is forced low.

Refer to Section 6.4 for the description of the standby mode.

9.1.6 NOP command

Table 21. NOP command synopsis

Byte	1	2
To device	0000 0000	0000 1100(1)

1. *The CRC byte of the command, if the CRC check is disabled this byte is ignored.*

The command does not modify the device status and does not generate any answer.

9.2 Register and flag descriptions

All device features can be configured through a set of 8-bit long registers. There are three different types of registers:

1. Local registers are located on the low voltage side
2. Remote registers are located on the isolated side
3. Shared registers are located both on the low voltage and isolated side and the value of the two copies is kept synchronized.

Table 22. Register map

Name	Side(1)	Structure							
-	-	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CFG1	L	CRC_SPI	UVLOD_EN	$\overline{SD}$_FLAG	DIAG_EN	DTset		INfilter	
CFG2	R	SENSEth			DESATcur		DESATth		
CFG3	R	2LTOth				2LTOtime			
CFG4	R	-	-	OVLO_EN	UVLOlatch	VLONth		VHONth	
CFG5	R	-	-	-	-	2LTO_EN	CLAMP_EN	DESAT_EN	SENSE_EN
STATUS1	L	OVLOH	OVLOL	DESAT	SENSE	UVLOH	UVLOL	TSD	TWN
STATUS2	L	-	-	-	-	-	REGERRR	ASC	GATE
STATUS3	L	-	-	-	DT_ERR	SPI_ERR	REGERRL	OVLOD	UVLOD
TEST1	R	-	-	-	GOFFCHK	GONCHK	DESCHK	SNSCHK	RCHK

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Name	Side[1]	Structure							
DIAG1CFG	L	DIAG1_7	DIAG1_6	DIAG1_5	DIAG1_4	DIAG1_3	DIAG1_2	DIAG1_1	DIAG1_0
DIAG2CFG	L	DIAG2_7	DIAG2_6	DIAG2_5	DIAG2_4	DIAG2_3	DIAG2_2	DIAG2_1	DIAG2_0

1. *R: remote (isolated side), L: local (low voltage side).*

Table 23. Registers access

Name	Address	Mask code
CFG1	0x0C	0xFF
CFG2	0x1D	0xFF
CFG3	0x1E	0xFF
CFG4	0x1F	0x3F
CFG5	0x19	0x0F
STATUS1	0x02	0xFF
STATUS2	0x01	0x07
STATUS3	0x0A	0x1F
TEST1	0x11	0x1F
DIAG1CFG	0x05	0xFF
DIAG2CFG	0x06	0xFF

9.2.1 CFG1 register (low voltage side)

The CFG1 register has the structure of Table 24.

Table 24. CFG1 register

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	CRC_SPI	UVLOD_EN	$\overline{SD}$_FLAG	DIAG_EN	DTset		INfilter	
Default/reset	0	0	1	0	00		00	

The CRC_SPI bit enables the CRC check on the SPI communication protocol.

Table 25. CRC enable

CRC_SPI	SPI communication protocol CRC enable
0	Disabled
1	Enabled

The UVLOD_EN bit enables the UVLO protection on VDD supply voltage.

Table 26. VDD supply voltage UVLO enable

UVLOD_EN	Supply voltage UVLOD enable
0	Disabled
1	Enabled

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The $\overline{SD}$_FLAG bit sets the $\overline{SD}$ pin functionality according to Table 27. When the reset of the failure flags through the $\overline{SD}$ pin is enabled, keeping low the $\overline{SD}$ pin for at least $t_{release}$ causes all the latched flags of the status registers to be released at the next $\overline{SD}$ rising edge.

Table 27. $\overline{SD}$ pin FAULT management

$\overline{SD}$_FLAG	$\overline{SD}$ pin functionality
0	$\overline{SD}$ pin do not reset STATUS registers
1	$\overline{SD}$ pin reset STATUS registers

The DIAG_EN bit sets if the IN-/$\overline{DIAG2}$ pin works as the input or open drain output according to Table 28. Refer to Section 7.1 for details.

Table 28. IN-/$\overline{DIAG2}$ pin functionality

DIAG_EN	IN-/$\overline{DIAG2}$ pin functionality
0	The IN-/$\overline{DIAG2}$ pin work as input
1	The IN-/$\overline{DIAG2}$ pin work as open drain output

The DTset bits set the deadtime value.

Table 29. Deadtime

DTset [1 ... 0]	Deadtime value [ns]	-
0	0	Disabled
0	1	250
1	0	800
1	1	1200

The INfilter bits set the input deglitch time $t_{deglitch}$ for the $\overline{SD}$, IN- and IN+ pins.

Table 30. Input deglitch time

INfilter [1 ... 0]		Input deglitch time value [ns]
0	0	Disabled
0	1	160
1	0	500
1	1	70

9.2.2 CFG2 register (isolated side)

The CFG2 register has the structure of Table 31.

Table 31. CFG2 register

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	SENSEth			DESATcur		DESATth		
Default/reset	000			00		100		

The SENSEth bits set the SENSE comparator threshold according to Table 32. Refer to Section 7.8 for details.

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Table 32. **SENSE threshold**

SENSEth [2 ... 0]			SENSE threshold value [mV]
0	0	0	100
0	0	1	125
0	1	0	150
0	1	1	175
1	0	0	200
1	0	1	250
1	1	0	300
1	1	1	400

The DESATcurr parameter sets the current sourced by the DESAT pin according to Table 33 and the DESATth parameter sets the DESAT comparator threshold according to Table 34. Refer to Section 7.6 for details.

Table 33. **DESAT current**

DESATcur [1 ... 0]	DESAT current value [µA]
0	250
0	1	500
1	0	750
1	1	1000

Table 34. **DESAT threshold**

DESATth [2 ... 0]			DESAT threshold value [V]
0	0	0	3
0	0	1	4
0	1	0	5
0	1	1	6
1	0	0	7
1	0	1	8
1	1	0	9
1	1	1	10

9.2.3 CFG3 register (isolated side)

The CFG3 register has the structure of Table 35.

Table 35. **CFG3 register**

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	2LTOth				2LTOtime			
Default/reset	0000				0000			

The 2LTOth parameter sets the voltage value which is actively forced during the 2-level turn- off sequence (refer to Section 7.10 for details).

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Table 36. **2LTOth**

2LTOth [3 ... 0]				2LTO threshold value [V]
0	0	0	0	7.00
0	0	0	1	7.50
0	0	1	0	8.00
0	0	1	1	8.50
0	1	0	0	9.00
0	1	0	1	9.50
0	1	1	0	10.00
0	1	1	1	10.50
1	0	0	0	11.00
1	0	0	1	11.50
1	0	1	0	12.00
1	0	1	1	12.50
1	1	0	0	13.00
1	1	0	1	13.50
1	1	1	0	14.00
1	1	1	1	14.50

The 2LTOtime parameter sets the duration of the 2-level turn-off sequence (refer to Section 7.10 for details). If the 2LTOtime is set to zero, the 2-level turn-off feature is disabled.

Table 37. **2-level turn-off time value**

2LTOtime [3 ... 0]				2-level turn-off time value [µs]
0	0	0	0	Disabled
0	0	0	1	0.75
0	0	1	0	1.00
0	0	1	1	1.50
0	1	0	0	2.00
0	1	0	1	2.50
0	1	1	0	3.00
0	1	1	1	3.50
1	0	0	0	3.75
1	0	0	1	4.00
1	0	1	0	4.25
1	0	1	1	4.50
1	1	0	0	4.75
1	1	0	1	5.00
1	1	1	0	5.25
1	1	1	1	5.50

9.2.4 CFG4 register (isolated side)

The CFG4 register has the structure of Table 38.

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Table 38. **CFG4 register**

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	OVLO_EN	UVLOlatch	VLONth		VHONth	
Default/reset	-	-	0	0	00		00	

The OVLO_EN bit enables the OVLO protection on the VH and VL power supply according to Table 39.

Table 39. **VH and VL supply voltages OVLO enable**

OVLO_EN	OVLO supply voltage enable
0	Disabled
1	Enabled

The UVLOlatch bit sets if the UVLO is latched or not (refer to Section 7.4 for details).

Table 40. **UVLO protection management**

UVLOlatch	UVLO protection management
0	UVLO protection is not latched
1	UVLO protection is latched

The VLONth bits set the UVLO threshold on the negative power supply according to Table 41.
Setting the parameter to zero disables the UVLO protection of the VL supply.

Table 41. **VL negative supply voltage UVLO threshold**

VLONth [1 ... 0]		Negative supply voltage UVLO threshold [V]
0	0	Disabled
0	1	-3
1	0	-5
1	1	-7

The VHONth bits set the UVLO threshold on the positive power supply according to Table 42.
Setting the parameter to zero disables the UVLO protection of the VH supply.

Table 42. **VH positive supply voltage UVLO threshold**

VHONth [1 ... 0]		Positive supply voltage UVLO threshold [V]
0	0	Disabled
0	1	10
1	0	12
1	1	14

9.2.5 CFG5 register (isolated side)

The CFG5 register has the structure of Table 43.

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Table 43. **CFG5 register**

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	2LTO_EN	CLAMP_EN	DESAT_EN	SENSE_EN
Default/reset	-	-	-	-	0	1	1	0

The 2LTO_EN bit sets when the feature takes place according to Table 44. Refer to Section 7.10 for details.

Table 44. **2LTO mode**

2LTO_EN	2LTO mode
0	2LTO always active
1	2LTO active only after a fault event

The 2LTOth bit sets the 2-level turn-off threshold according to Table 36 and the 2-level turn-off time according to Table 37.

The SENSE_EN bit sets if the sense overcurrent function is enabled or not (refer to Section 7.8 for details).

Table 45. **SENSE comparator enabling**

SENSE_EN	SENSE comparator status
0	SENSE comparator disabled
1	SENSE comparator enabled

The DESAT_EN bit sets if the desaturation protection is enabled or not (refer to Section 7.6 Section 7.6 for details).

Table 46. **DESAT comparator enabling**

DESAT_EN	DESAT comparator status
0	DESAT comparator disabled
1	DESAT comparator enabled

Set the CLAMP_EN bit to enable the Miller clamp feature (refer to Section 7.9 for details).

Table 47. **Miller clamp feature enabling**

CLAMP_EN	Miller clamp feature status
0	Miller clamp feature disabled
1	Miller clamp feature enabled

9.2.6 STATUS1 register (low voltage side)

The STATUS1 is a read only register that reports some device failure flags.

All flags are active high (the high value indicates a failure condition). The STATUS1 register has the structure of Table 48.

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Table 48. **STATUS1 register**

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	OVLOH	OVLOL	DESAT	SENSE	UVLOH	UVLOL	TSD	TWN
Default(1)	0	0	0	0	1	0	0	0
Reset	0	0	0	0	0	0	0	0

1. *Default value of the local copy of the register. The value will be updated according to the actual information from the isolated side. The default is forced at the device power-up, when the registers are reset all the flags are forced low (no failures).*

A description of the STATUS1 register bits is provided in Table 49.

Table 49. **STATUS1 register description**

Name	Bit	Fault	Latched	Force "safe state"	Note
OVLOH	7	VH overvoltage flag. It is forced high when VH is over OV_{VHoff} threshold.	Always	Yes	-
OVLOL	6	VL overvoltage flag. It is forced high when VL is over OV_{VLoff} threshold.	Always	Yes	-
DESAT	5	Desaturation flag. It is forced high when DESAT pin voltage reaches $V_{DESATth}$ threshold.	Always	Yes	-
SENSE	4	Sense flag. It is forced high when SENSE pin voltage reaches $V_{SENSEth}$ threshold.	Always	Yes	-
UVLOH	3	VH undervoltage flag. It is forced high when VH is below VHoff threshold.	When UVLOlatch is high only	Yes	If not latched (UVLOlatch low) UVLOH returns low when VH is over VH_{on} threshold.
UVLOL	2	VL undervoltage flag. It is forced high when VL is over VLoff threshold.	When UVLOlatchis high only	Yes	If not latched (UVLOlatch low) UVLOL returns low when VL is below VL_{on} threshold.
TSD	1	Thermal shutdown protection flag. It is forced high when overtemperature shutdown threshold is reached.	No (hysteresis)	Yes	-
TWN	0	Thermal warning flag. It is forced high when overtemperature shutdown threshold is reached.	No (hysteresis)	No	-

9.2.7 STATUS2 register (low voltage side)

The STATUS2 is a read only register. The STATUS2 register has the structure of Table 50.

Table 50. **STATUS2 register**

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	REGERRR	ASC	GATE
Default(1)	x	x	x	x	x	1	0	0

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-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	x	x	x	x	x	0	0	0

1. *Default value of the local copy of the register. The value will be updated according to the actual information from the isolated side. The default is forced at the device power-up, when the registers are reset all the flags are forced low (no failures).*

A description of the STATUS2 register bits is provided in Table 51.

Table 51. STATUS2 register description

Name	Bit	Fault	Latched	Force "safe state"	Note
REGERRR	2	Register or communication error on isolated side. It is forced high when: • Programming procedure is not correctly performed. • Isolated interface communication fails. • An unexpected register value change occurs in one of the remote registers. It is also latched at power-up/reset and from Sleep state.	Always	Yes	-
ASC	1	ASC pin status. When ASC pin is high, the flag reports '1', otherwise it is '0'.	No	No	See details in Section 7.12
GATE	0	Gate command flag. Flag is '1' when the requested output status from logic inputs is "ON" and '0' when requested output status is "OFF".	No	No	This bit is not indicated for real-time feedback of external gate status (Section 7.14)

9.2.8 STATUS3 register (low voltage side)

The STATUS3 is a read only register. The STATUS3 register has the structure of Table 52.

Table 52. STATUS3 register

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	DT_ERR	SPI_ERR	REGERRL	OVLOD	UVLOD
Default(1)	x	x	x	0	0	1	0	1
Reset	x	x	x	0	0	0	0	0

1. *The default is forced at the device power-up, when the registers are reset all the flags are forced low (no failures).*

A description of the STATUS3 register bits is provided in Table 53.

Table 53. STATUS3 register description

Name	Bit	Fault	Latched	Force "safe state"	Note
DT_ERR	4	Deadtime error flag. This bit is forced high when a violation of internal DT is detected.	Always	No	See details in Section 7.2
SPI_ERR	3	SPI communication error flag.	Always	No	-

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Name	Bit	Fault	Latched	Force “safe state”	Note
		It is forced high when the SPI communication fails cause: • Wrong CRC check. • Wrong number of CK rising edges. • Attempt to execute a not-allowed command. • Attempt to read, write or reset at a not- available address.			
REGERRL	2	Register or communication error on low voltage side. It is forced high when: • Programming procedure is not correctly performed. • Isolated interface communication fails. • An unexpected register value change occurs in one of the remote registers. It is latched at power-up/reset also.	Always	Yes	-
OVLOD	1	VDD overvoltage flag. It is forced high when VDD is over OVVDDoff threshold.	Always	Yes	-
UVLOD	0	VDD undervoltage flag. It is forced high when VDD is below VDDon threshold. It is latched at power-up/reset as well.	Always	Yes	-

9.2.9 TEST1 register (isolated side)

The TEST1 register has the structure of Table 54.

Table 54. TEST1 register

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	GOFFCHK	GONCHK	DESCHK	SNSCHK	RCHK
Default/reset	x	x	x	0	0	0	0	0

Setting an one check bit of the register enables the respective check mode.

Table 55. Check mode

Bit	Check mode
RCHK	SENSE resistor
SNSCHK	SENSE comparator
DESCHK	DESAT comparator
GONCHK	GON to gate path
GOFFCHK	GOFF to gate path

9.2.10 DIAG1CFG and DIAG2CFG registers (low voltage side)

The DIAG1CFG register has the structure of Table 56.

Table 56. DIAG1CFG register

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DIAG1_7	DIAG1_6	DIAG1_5	DIAG1_4	DIAG1_3	DIAG1_2	DIAG1_1	DIAG1_0

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-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default/reset	1	1	0	1	1	0	1	0

The DIAG2CFG register has the structure of Table 57.

Table 57. DIAG2CFG register

-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DIAG2_7	DIAG2_6	DIAG2_5	DIAG2_4	DIAG2_3	DIAG2_2	DIAG2_1	DIAG2_0
Default/reset	0	0	0	0	0	0	0	0

If a bit in the DIAG1CFG register is high, the corresponding fault events turn on the open drain connected to the DIAG1 pin forcing the output low.

If a bit in the DIAG2CFG register is high and the DIAG_EN bit is high, the corresponding fault events turn on the open drain connected to the DIAG2 pin forcing the output low.

The relationship between the DIAG1CFG and DIAG2CFG register bits and failure events is described in Table 58.

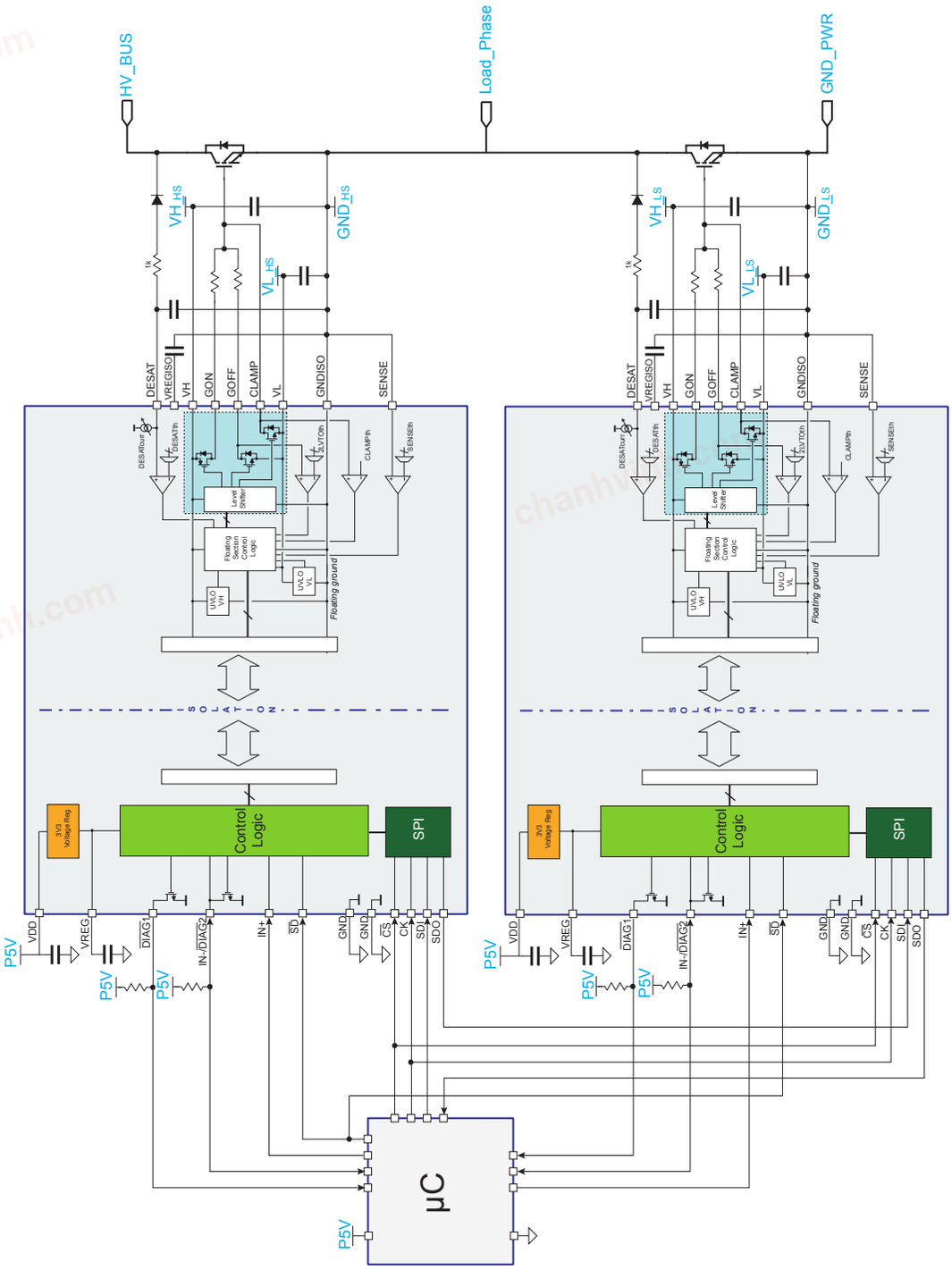
Table 58. Relation between DIAGxCFG bits and failure conditions

DIAGxCFG bit	Failure	Status registers bit
0	Thermal warning	TWN
1	Thermal shutdown	TSD
2	ASC feedback	ASC, DT_ERR
3	Desaturation and sense detection	DESAT, SENSE
4	Overvoltage failure	OVLOH, OVLOL
5	Undervoltage failure	UVLOH, UVLOL
6	VDD power supply failure	UVLOD, OVLOD
7	SPI communication error or register failure	SPI_ERR, REGERRL, REGERRR

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10 Typical application diagram

Figure 27. **Typical application diagram in half-bridge configuration**



Refer to Figure 13 in the dedicated Section 7.7 for the connection of the VCECLAMP pin.

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11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 SO24W package information

Figure 28. SO24W package outline

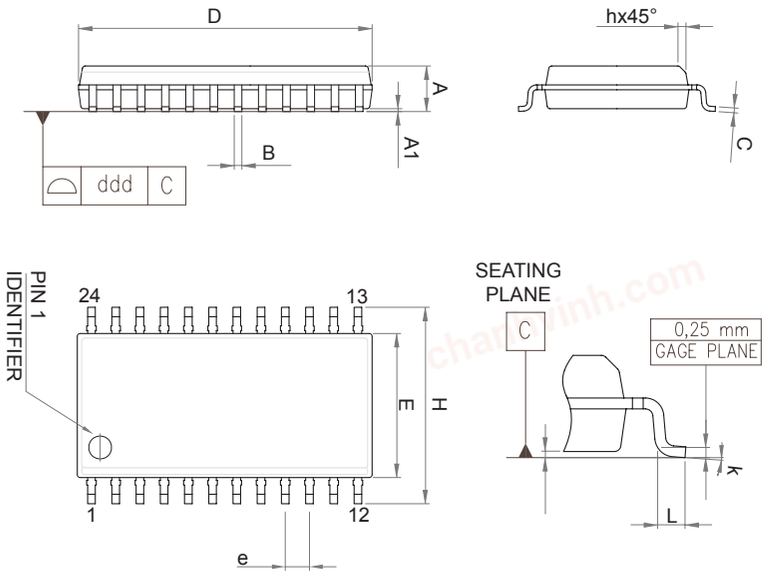


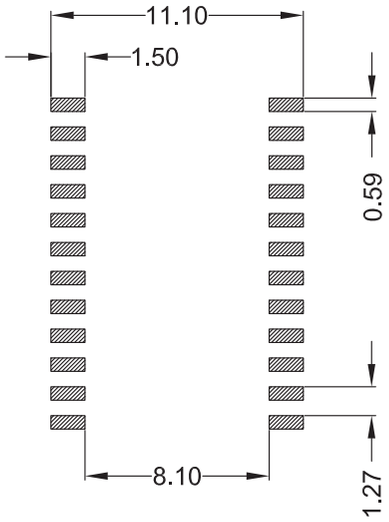
Table 59. SO24W package mechanical data

Symbol	Dimensions (mm)			Notes
	Min.	Typ.	Max.	
A	2.35	-	2.65	-
A1	0.10	-	0.30	-
B	0.33	-	0.51	-
C	0.23	-	0.32	-
D	15.20	-	15.60	(1)
E	7.40	-	7.60	-
e	-	1.27	-	-
H	10.00	-	10.65	-
h	0.25	-	0.75	-
L	0.40	-	1.27	-
K	0	-	8	Degrees
ddd	-	-	0.10	-

1. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.*

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Figure 29. **SO24W suggested land pattern**



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12 Ordering information

Table 60. **Device summary**

Order code	Package	Packing
STGAP1BS	SO24W	Tube
STGAP1BSTR	SO24W	Tape and reel

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Revision history

Table 61. **Document revision history**

Date	Version	Changes
06-Oct-2021	4	Cover package updated

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