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STGAP3S6I, STGAP3S6S
STGAP3SXI, STGAP3SXS

Datasheet

Galvanically isolated 6/10 A single gate drivers with protection features



SO-16W

Product status link
STGAP3S6I
STGAP3S6S
STGAP3SXI
STGAP3SXS

Product label
SUSTAINABLE TECHNOLOGY

Features

- High voltage rail up to 1200 V
- Driver current capability: 6/10 A sink/source @25 °C
- ±200 V/ns Common Mode Transient Immunity (CMTI)
- 75 ns input-output propagation delay
- Miller CLAMP driver for external N-channel MOSFET 0.3 A source/0.5 A sink
- Adjustable soft turn-off function
- VDD UVLO
- VH UVLO: IGBT and SiC variants
- Desaturation protection: IGBT and SiC variants
- Gate driving voltage up to 32 V
- Negative gate driving voltage up to -10 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shutdown protection
- Reinforced galvanic isolation:
  - Isolation voltage V_{ISO} = 5.7 kV_{RMS} (UL 1577)
  - Transient Overvoltage V_{IOTM} = 8 kV_{PEAK} (IEC 60747-17)
  - Max. Repetitive Isolation Voltage V_{IORM} = 1.2 kV_{PEAK} (IEC 60747-17)
- Wide body SO-16W package

Applications

- Motor driver for home appliances, factory automation, industrial drives, and fans
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power factor correction

Description

The STGAP3S is a family of protected single gate drivers that provides galvanic isolation between the gate driving channel and the low voltage control and interface circuitry.

The platform includes different options with 10 A and 6 A current capability, each of which is available with dedicated UVLO variants for SiC MOSFETs and IGBTs.

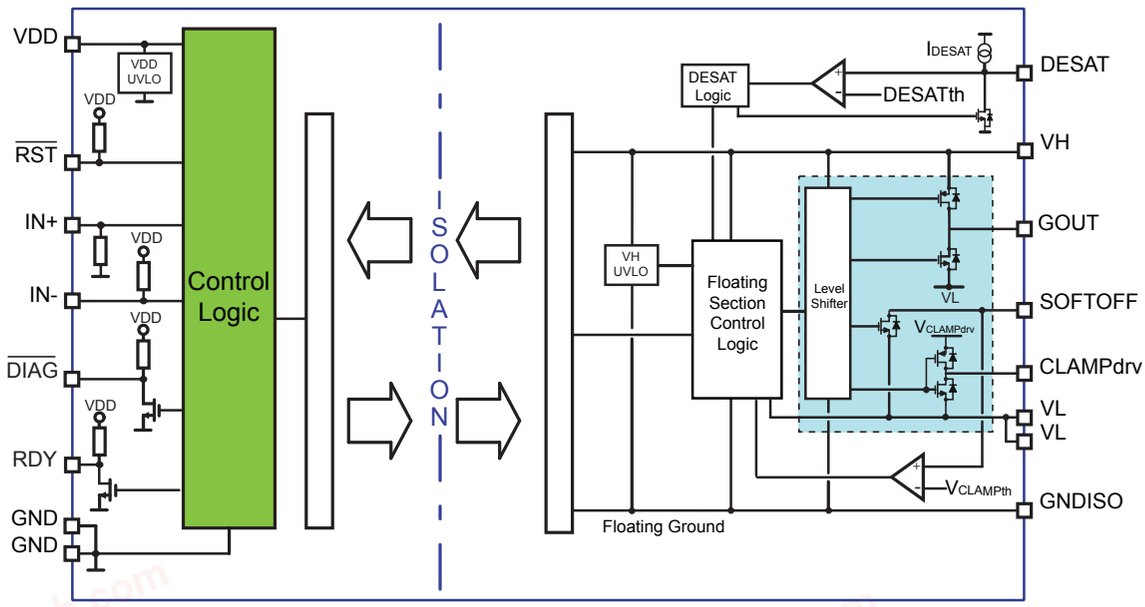
Ultrafast desaturation protection is also available with differentiated intervention thresholds and adjustable soft turn-off.

The availability of the Miller CLAMP and optional negative driving enables optimal driving performance.

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1 Block diagram

Figure 1. **Block diagram**



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2 Pin description and connection diagram

Figure 2. **Pin connection (top view)**

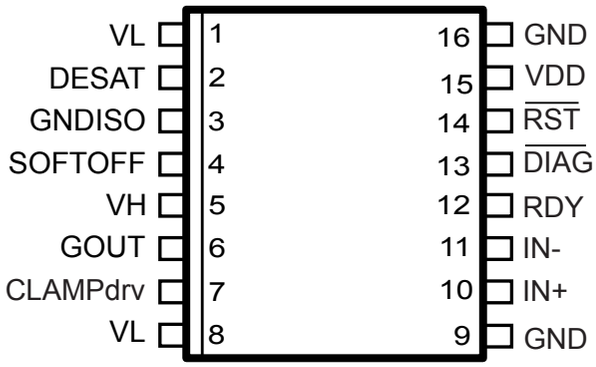


Table 1. **Pin description**

Pin #	Pin name	Type	Function
1, 8	VL	Power supply	Gate driving negative voltage supply
2	DESAT	Analog input	Desaturation protection input
3	GNDISO	Power supply	Gate driving isolated ground
4	SOFTOFF	Analog output	Soft turn-off
5	VH	Power supply	Gate driving positive voltage supply
6	GOUT	Analog output	Sink/source output
7	CLAMPdrv	Analog output	Active Miller clamp output driver
9, 16	GND	Power supply	Driver logic ground
10	IN+	Logic input	Driver logic input
11	IN-	Logic input	Driver logic input
12	RDY	Open drain	Diagnostic output (UVLO and overtemperature protection)
13	$\overline{\text{DIAG}}$	Open drain	Diagnostic output (Desat protection)
14	$\overline{\text{RST}}$	Logic input	Fault reset and shutdown logic input, active low
15	VDD	Power supply	Driver logic supply voltage

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3 Device ratings

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-0.3	6	V
V_{LOGIC}	Logic pins voltage (IN+, IN-, $\overline{RST}$) vs. GND	-0.3	6	V
VH	Positive supply voltage VH vs. GNDISO	-0.3	36	V
VL	Negative supply voltage VL vs. GNDISO	-15	0.3	V
V_{HL}	Differential supply voltage VH vs. VL	-0.3	36	V
V_{OUT}	Voltage on gate driver outputs (GOUT, CLAMP, SOFTOFF) vs. VL	VL - 0.3	VH + 0.3	V
$V_{CLAMPdrv}$	Voltage on CLAMPdrv output vs. VL	VL - 0.3	min(+20, VH + 0.3)	V
V_{DESAT}	Voltage on DESAT vs. GNDISO	-0.3	VH + 0.3	V
V_{DIAG}	Open drain output voltage vs. GND	-0.3	6.0	V
V_{RDY}	Open drain output voltage vs. GND	-0.3	6.0	V
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C
ESD	HBM (human body model)	2		kV

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction-to-ambient	SO-16W	74	°C/W

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3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	3.1	5.5	V
V_{LOGIC}	Logic pins (IN+, IN-, $\overline{RST}$) voltage vs. GND	0	5.5	V
VH	Positive supply voltage (VH vs. GNDISO)	5	32	V
VL	Negative supply voltage (VL vs. GNDISO)	-10	0	V
V_{HL}	Differential supply voltage (VH vs. VL)	-	32	V
$V_{DESATth}$	Threshold voltage of DESAT protection vs. GND	-	VH - 2	V
F_{SW}	Maximum switching frequency (1)	-	1	MHz
T_J	Operating junction temperature	-40	125	°C
T_{amb}	Ambient temperature	-40	125	°C

1. *Actual limit depends on power dissipation and T_J.*

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4 Electrical characteristics

Test conditions: T_J = 25 °C, VH = 15 V, VL = GNDISO, VDD = 5 V, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics							
t_{Don}	IN+, IN-	Input to output propagation delay ON	(1)	55	75	95	ns
t_{Doff}	IN+, IN-	Input to output propagation delay OFF	(1)	55	75	95	ns
t_r	GOUT	Rise time	STGAP3S6x (1) 20% to 80%, C_L = 4.7 nF	-	20	-	ns
			STGAP3SXx (1) 20% to 80%, C_L = 10 nF	-	20	-	
t_f	GOUT	Fall time	STGAP3S6x (1) 80% to 20%, C_L = 4.7 nF	-	18	-	ns
			STGAP3SXx (1) 80% to 20%, C_L = 10 nF	-	18	-	
PWD	GOUT	Pulse width distortion $\lvert t_{Don} - t_{Doff} \rvert$	t_{IN} > 100 ns	-	0	10	ns
t_{INmin}	IN+, IN-, $\overline{RST}$	Minimum propagated input pulse	C_L = 2 nF, R_{GON} = R_{GOFF} = 3.9 Ω	-	20	-	ns
CMTI (2)		Common-mode transient immunity $\lvert dV_{ISO}/dt \rvert$	V_{CM} = 1200 V, see Figure 17	200	-	-	V/ns
Supply voltage							
VDD_{on}	VDD	VDD UBLO turn-on threshold		2.85	2.95	3.05	V
VDD_{off}	VDD	VDD UVLO turn-off threshold		2.60	2.80	2.95	V
VDD_{hyst}	VDD	VDD UVLO hysteresis		130	160	190	mV
$t_{VDD-RDY}$	RDY	VDD UVLO to RDY low delay	See Figure 3	1.5	2.5	3.5	µs
$t_{VDD-GOUT}$	GOUT	VDD UVLO to GOUT low delay	See Figure 3	1.6	2.6	3.6	µs
I_{QDD}	VDD	VDD quiescent supply current	IN+ = 0	1.2	2.0	2.5	mA
			IN+ = RDY = VDD, IN- = GND	8	11	13	
VH_{on}	VH	VH UVLO turn-on threshold	STGAP3SxSx	12.9	13.6	14.3	V
			STGAP3SxIx	11.4	11.9	12.5	
VH_{off}	VH	VH UVLO turn-off threshold	STGAP3SxSx	12.2	12.8	13.4	V
			STGAP3SxIx	10.6	11.1	11.5	
VH_{hyst}	VH	VH UVLO hysteresis		0.6	0.8	1.0	V
t_{VH-RDY}	RDY	VH UVLO to RDY low delay	See Figure 4	10	15	20	µs
$t_{VH-GOUT}$	GOUT	VH UVLO to GOUT low delay	See Figure 4	1.5	2.5	3.5	µs
I_{QH}	VH	VH quiescent supply current	IN+ = GND	3	5	6	mA
SafeClp	GOUT	GOUT active clamp	I_{GOUT} = 0.2 A, VH floating	1.9	2.0	2.3	V

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Symbol	Pin	Parameter	Test conditions		Min.	Typ.	Max.	Unit
Logic inputs								
V_{il}	IN+, IN-, $\overline{RST}$	Low-level logic threshold voltage			0.29·VDD	0.33·VDD	0.37·VDD	V
V_{ih}	IN+, IN-, $\overline{RST}$	High-level logic threshold voltage			0.62·VDD	0.66·VDD	0.70·VDD	V
I_{IN+h}	IN+	IN+ logic “1” input bias current	IN+ = VDD		120	150	210	µA
I_{IN+l}	IN+	IN+ logic “0” input bias current	IN+ = GND		-	-	1	µA
R_{in_pd}	IN+	Input pull-down resistors	IN+ = 5 V		23	33	42	kΩ
I_{IN-l}	IN-, $\overline{RST}$	IN-, $\overline{RST}$ logic “0” input bias current	IN-, $\overline{RST}$ = GND		40	55	70	µA
I_{IN-h}	IN-, $\overline{RST}$	IN-, $\overline{RST}$ logic “1” input bias current	IN-, $\overline{RST}$ = VDD		-	-	1	µA
R_{in_pu}	IN-, $\overline{RST}$	Input pull-up resistors	IN+ = GND		70	90	125	kΩ
t_{rst}	$\overline{RST}$	Minimum pulse width to rest $\overline{DIAG}$	(3)		240	500	800	ns
Driver buffer section								
I_{GON}	GOUT	Source short-circuit current	STGAP3S6x	T_J = 25 °C	4.8	6.0	6.9	A
				-40 °C ≤ T_J ≤ 125 °C (2)	4.3	-	7.6	
			STGAP3SXx	T_J = 25 °C	8	10	11.5	A
				-40 °C ≤ T_J ≤ 125 °C (2)	7	-	13	
V_{GON}	GOUT	GOUT output high-level voltage	STGAP3S6x	I_{GON} = 100 mA	0.09	0.10	0.11	V
			STGAP3SXx	I_{GON} = 100 mA	0.05	0.07	0.08	
R_{DON}	GOUT	Source R_{DS_ON}	STGAP3S6x	I_{GON} = 100 mA	0.86	0.96	1.10	Ω
			STGAP3SXx	I_{GON} = 100 mA	0.50	0.65	0.80	
I_{GOFF}	GOUT	Sink short-circuit current	STGAP3S6x	T_J = 25 °C	5.2	6.0	6.8	A
				-40 °C ≤ T_J ≤ 125 °C (2)	4.5	-	7.9	
			STGAP3SXx	T_J = 25 °C	8	10	11.5	A
				-40 °C ≤ T_J ≤ 125 °C (2)	6.8	-	12.8	
V_{GOFF}	GOUT	Sink output low-level voltage	STGAP3S6x	I_{GOFF} = 100 mA	0.05	0.07	0.09	V
			STGAP3SXx	I_{GOFF} = 100 mA	0.03	0.05	0.07	
R_{DOFF}	GOUT	Sink R_{DS_ON}	STGAP3S6x	I_{GOFF} = 100 mA	0.55	0.70	0.85	Ω
			STGAP3SXx	I_{GOFF} = 100 mA	0.35	0.50	0.65	
External Miller clamp driver								
$V_{CLAMPth}$	CLAMPdrv	CLAMP voltage threshold vs. VL			1.8	2.0	2.2	V
$I_{CLAMPsource}$	CLAMPdrv	CLAMP source short-circuit current	T_J = 25 °C		215	280	355	mA
			-40 °C ≤ T_J ≤ 125 °C (2)		188	-	386	
$I_{CLAMPsink}$	CLAMPdrv	CLAMP sink short-circuit current	T_J = 25 °C		370	450	530	mA
			-40 °C ≤ T_J ≤ 125 °C (2)		313	-	590	
$V_{CLAMPdrv_H}$	CLAMPdrv	CLAMP high-level output vs. VL	No load, V_{HL} ≥ 11.5 V		10.5	11.5	13.0	V

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Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CLAMPdrv_H}$	CLAMPdrv	CLAMP high-level output vs. VL	No load, V_{HL} < 7.5 V	-	VH - 1	-	V
$V_{CLAMPdrv_L}$	CLAMPdrv	CLAMP low-level output vs. VL	I_{CLAMP} = 10 mA	-	60	-	mV
$t_{CLAMPdrv}$	CLAMPdrv	Miller clamp driver intervention time		-	50	-	ns
Desaturation protection							
$V_{DESATth}$	DESAT	Desaturation threshold	STGAP3SxSx	5.70	6.00	6.30	V
			STGAP3SxIx	8.55	9.00	9.45	
I_{DESAT}	DESAT	DESAT blanking charge current	V_{DESAT} = 0 V	0.93	1.00	1.10	mA
I_{DESoff}	DESAT	DESAT blanking discharge current	V_{DESAT} = 8 V, IN+ = GND	110	150	195	mA
$t_{DESfilter}$	DESAT	DESAT pin deglitch filter	Step on DESAT pin: 0 → ($V_{DESATth}$+ 1 V)	-	120	-	ns
t_{BLK}	DESAT	DESAT protection fixed blanking time	(3)	180	200	220	ns
t_{DESAT}	DESAT	DESAT protection intervention time	(3) Step on DESAT pin: 0 → ($V_{DESATth}$+ 1 V) Time from step to SOFTOFF / GOUT 90%, No load	80	150	220	ns
t_{DIAG}	$\overline{DIAG}$	DESAT event to $\overline{DIAG}$ low delay	(3)	-	-	2.5	µs
SOFTOFF							
I_{STO}	SOFTOFF	Soft turn-off current on fault conditions	T_J = 25 °C	700	800	900	mA
			-40 °C ≤ T_J ≤ 125 °C (2)	550	-	1100	
$t_{SOFTOFF}$	SOFTOFF	Soft turn-off time	(3)	4	5	6	µs
Overtemperature protection							
T_{SD}		Shutdown temperature		164	-	-	°C
T_{hys}		Temperature hysteresis		-	20	-	°C
t_{OT-RDY}		Overtemperature to RDY low delay	See Figure 12	10	15	20	µs
$t_{OT-GOUT}$		Overtemperature to GOUT low delay	See Figure 12	1.5	2.5	3.5	µs
Diagnostic							
I_{DIAG}	$\overline{DIAG}$	$\overline{DIAG}$ low-level sink current	V_{DIAG} = 0.4 V	20	30	40	mA
I_{RDY}	RDY	RDY low-level sink current	V_{RDY} = 0.4 V	20	30	40	mA
R_{DIAG_pu}	$\overline{DIAG}$, RDY	$\overline{DIAG}$ & RDY pull-up resistor	$\overline{DIAG}$, RDY = GND	35	55	72	kΩ

1. *See Figure 16.*
2. *Characterization data, not tested in production.*
3. *See Figure 11.*

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5 Isolation

Table 6. Isolation and safety specifications

Symbol	Parameter	Test conditions	Value	Unit
General				
CLR	Clearance (Minimum external air gap)	Measured from input terminals to output terminals, shortest distance trough air	8	mm
CPG	Creepage (Minimum external tracking)	Measured from input terminals to output terminals, shortest distance path along body	8	mm
CTI	Comparative tracking index (Tracking resistance)	IEC 60112	≥ 400	V
-	Material group	According to IEC 60664-1	II	-
-	Overvoltage category per IEC 60664-1	Rated mains voltages ≤ 150 V_{RMS}	I - IV	-
		Rated mains voltages ≤ 300 V_{RMS}	I - IV	-
		Rated mains voltages ≤ 600 V_{RMS}	I - IV	-
		Rated mains voltages ≤ 1000 V_{RMS}	I - III	-
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive isolation voltage	AC voltage	1200	V_{PEAK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave)	850	V_{RMS}
		DC voltage	1200	V_{PEAK}
V_{PR}	Partial discharge test voltage	Method a, type and sample test $V_{PR} = V_{IORM} \times 1.6$, $t_m = 10$ s Partial discharge < 5 pC	1920	V_{PEAK}
		Method b1, 100% production test $V_{PR} = V_{IORM} \times 1.875$, $t_m = 1$ s Partial discharge < 5 pC	2250	V_{PEAK}
V_{IOTM}	Maximum transient isolation voltage	Method a, type and sample test $t_{ini} = 60$ s	8000	V_{PEAK}
$V_{IOTM,test}$	Transient isolation voltage test	Method b1, 100% production test $V_{IOTM,test} = V_{IOTM} \times 1.2$, $t_{ini} = 1$ s	9600	V_{PEAK}
V_{IMP}	Maximum impulse voltage	Type test; tested in air 1.2/50 µs waveform per IEC 62368-1	8000	V_{PEAK}
V_{IOSM}	Maximum surge isolation voltage	Type test; tested in oil 1.2/50 µs waveform per IEC 62368-1	12800	V_{PEAK}
R_{IO}	Isolation resistance	Type test; $V_{IO} = 500$ V $T_{amb} = 25$ °C	> 10^{12}	Ω
		Type and sample test; $V_{IO} = 500$ V 100 °C ≤ $T_{amb} \le T_S = 150$ °C	> 10^{11}	
		Type and sample test; $V_{IO} = 500$ V $T_{amb} = T_S = 150$ °C	> 10^{9}	
C_{IO}	Barrier capacitance, input to output	Typical value, not tested in production	1	pF

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Symbol	Parameter	Test conditions	Value	Unit
UL-1577				
V_{ISO}	Isolation withstand voltage	60 s; type test	5700 / 8061	V_{RMS} / V_{PEAK}
$V_{ISO,test}$	Isolation voltage test	1 s; 100% production	6840 / 9674	V_{RMS} / V_{PEAK}

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6 Functional description

The STGAP3S is a family of fully protected single gate drivers with integrated galvanic isolation that relies on state-of-the-art capacitive communication. The device is able to work with high voltage rails up to 1200 V and is offered in several variants with 6 A and 10 A output current capability and dedicated UVLO and DESAT options for IGBTs and SiC MOSFETs.

The control interface side consists of two gate drive input pins (IN+, IN-), a fault reset and shutdown input pin ($\overline{RST}$), and two open drain output pins for desaturation protection ($\overline{DIAG}$) and for UVLO and overtemperature protections (RDY).

The dual inputs pins allow the selection of gate driving control signal polarity control and the implementation of HW interlocking protection to avoid cross conduction in case of controller malfunction.

The driving side consists of the gate control pin (GOUT), the desaturation protection pin (DESAT), a pin for adjustable soft turn-off protection (SOFTOFF) and a pin for the optional negative supply pin (VL).

The ultrafast DESAT protection event is latched and a turn-off strategy can be implemented by the tunable SOFTOFF function, to maximize the protection turn-off speed while avoiding excessive collector overvoltage spikes. The fault condition is notified to the control device by an open drain diagnostic pin ($\overline{DIAG}$).

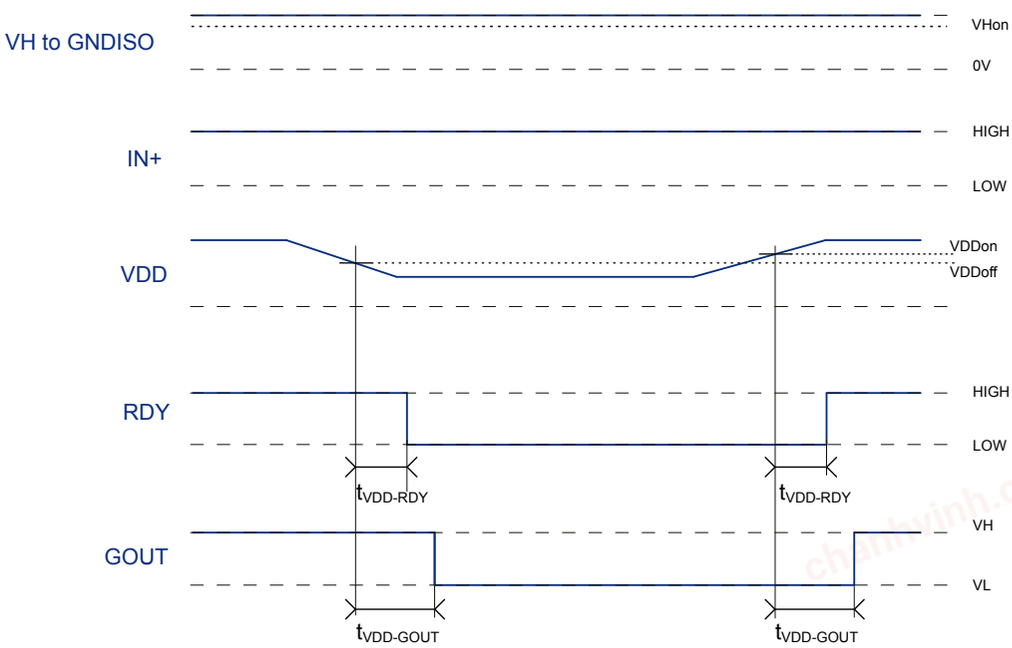
The undervoltage lock out (UVLO) feature prevents the external power switch to be actuated with insufficient gate voltage, the UVLO event is notified through a diagnostic open drain pin (RDY).

The Miller clamp driver function enables the use of fast switching speeds while preventing the unwanted induced turn-on side effect.

6.1 Power supplies and UVLO

Undervoltage lockout (UVLO) protection is available on both the control interface supply voltage VDD (see Figure 3) and on the driving side supply voltage VH (see Figure 4). A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

Figure 3. UVLOD protection timings



There are two options for the UVLOH threshold:

- The threshold of STGAP3S6I and STGAP3SXI suitable for driving IGBTs and Si MOSFETs.
- The threshold of STGAP3S6S and STGAP3SXS suitable for driving SiC MOSFETs.

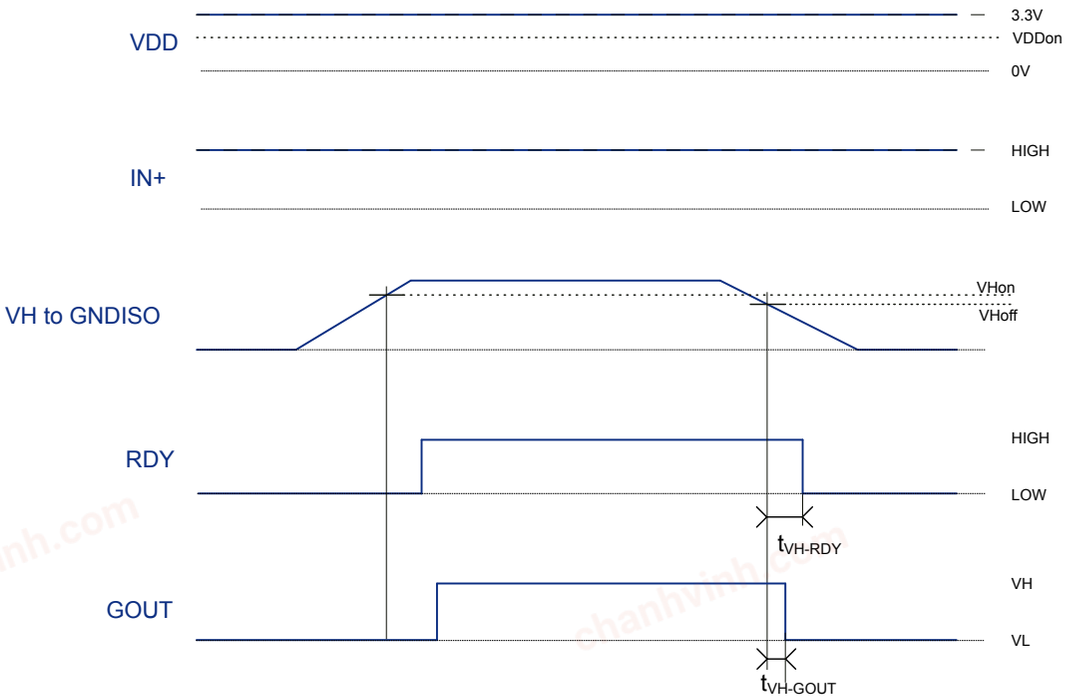
When the VH voltage falls below the VH_{off} threshold, the output buffer enters a “safe state”. When the VH voltage reaches the VH_{on} threshold, the device returns to normal operation and sets the output according to actual input pins status.

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The VDD and VH supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering.

The best filtering is obtained by using low-ESR SMT ceramic capacitors and are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with a value in the range between 1 µF and 10 µF should be placed close to it.

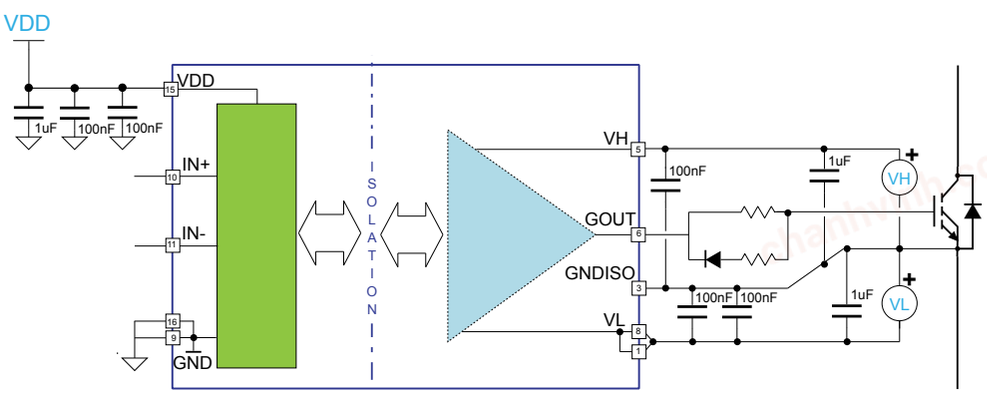
Figure 4. UVLOH protection timings



The driver allows to implement either unipolar gate driving or bipolar gate driving for the power switch.

In the case of bipolar gate driving (see Figure 5), the negative supply voltage shall be connected between the GNDISO and VL pins. The use of a negative gate driving can further mitigate the risk of induced turn-on due to Miller effect in hard-switching conditions, and can also help to increase the turn-off speed of the power switch.

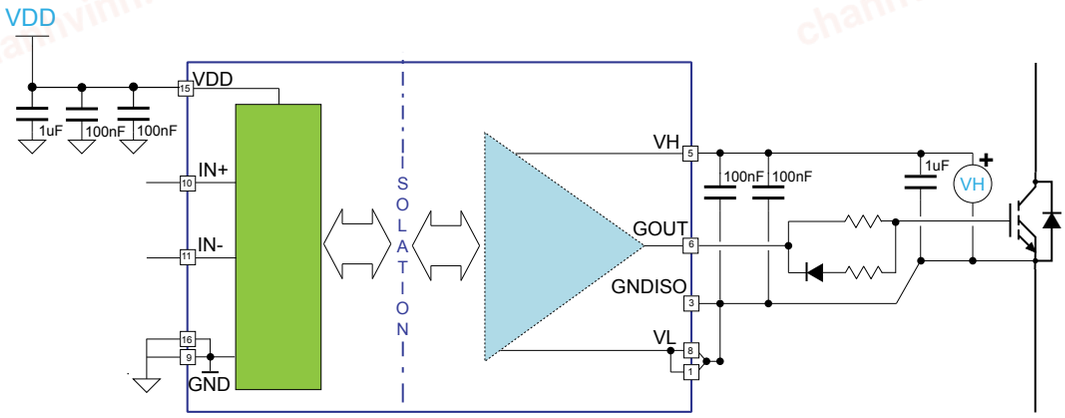
Figure 5. Power supply configuration for bipolar gate driving



If a unipolar gate driving is used (see Figure 6), the GNDISO and VL pins shall be connected together by means of short traces.

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Figure 6. **Power supply configuration for unipolar gate driving**



6.2 Power-up, power-down, and “safe state”

There is no required power-on or power-off sequencing of the supply pins, as long as the device is operated within the maximum recommended values.

If the primary side is not supplied, or one of the driver’s protection is triggered (VDD UVLO, VH UVLO, DESAT, Overtemperature) the device enters in “safe state”.

The following conditions define the “safe state”:

- GOUT: forced to VL;
- SOFTOFF: forced to VL;
- DESAT: forced to GNDISO (internal switch on);
- CLAMPdrv: forced to V_{CLAMP_H}.

Such conditions are maintained at power-up of the device and during the whole device power-down phase (VH < VH_{off} and VDD < VDD_{off}), regardless of the value of the input pins.

The device integrates a structure that clamps the driver output to a voltage not higher than SafeClp when the VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If the VH positive supply pin is floating or not supplied, the GOUT pin is clamped to a voltage smaller than SafeClp.

At the power-up, the diagnostic pin RDY is forced to GND and remains in such condition until both VDD and VH rise above the relative $UVLO_{on}$ thresholds.

After power-up of both the isolated and low voltage side, the device output state depends on the input pins status.

6.3 Control inputs

The device is controlled through the following logic inputs:

- IN+ and IN-: driver inputs
- $\overline{RST}$: Active low shutdown input.

And the following logic outputs:

- $\overline{DIAG}$: desaturation event diagnostic signal (open drain)
- RDY: diagnostic power-good signal (open drain).

The device is designed to work with 5 V or 3.3 V VDD supply voltage, and in order to maximize noise margin the logic input thresholds vary according to VDD voltage. The I/Os IN-, $\overline{DIAG}$, RDY, and $\overline{RST}$ have a weak internal pull-up resistor, while IN+ has a weak internal pull-down resistor in order to force the output to switch off the external power device in case of floating inputs.

The truth table, Table 7, describes how the outputs are driven by the logics inputs.

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Table 7. Truth table (applicable when device is not in UVLO or "safe state")

Input pins			Output pin
$\overline{RST}$	IN+	IN-	GOUT
L	X (1)	X (1)	LOW
H	L	L	**HIGH**
H	H	L	LOW
H	L	H	LOW
H	H	H	

1. *Do not care.*

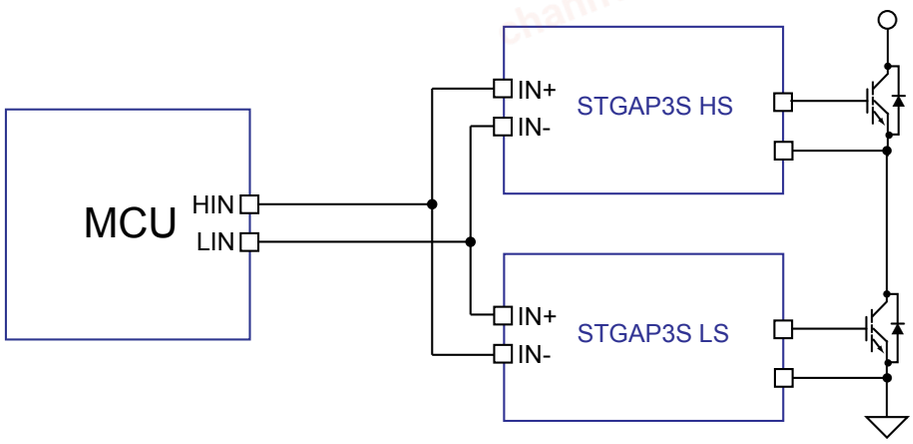
A deglitch filter is applied to device inputs ($\overline{RST}$, IN+, IN-). Each input pulse, positive or negative, shorter than t_{INmin} is neglected by internal logic. This minimum input pulse timing filters out both positive and negative pulses at the IN+, IN-, and $\overline{RST}$ pins.

6.3.1 Anti cross conduction interlocking

When single gate drivers are used in half-bridge configuration, they usually do not allow preventing cross conduction in case of wrong input signals coming from the controller device. Indeed, each driver does not have the possibility to know the status of the input signal of the other companion driver in the same leg. Thanks to the availability of two input pins with opposite polarity, the STGAP3S allows implementing a hardware interlocking that prevents cross conduction even in case of wrong input signals generated by the control unit.

This functionality can be achieved by implementing the connection shown in Figure 7.

Figure 7. Hardware cross conduction prevention in half-bridge configuration with two single gate drivers



6.4 Miller clamp function

The Miller clamp function allows the mitigation of the Miller current during the power stage hard-switching commutations in half-bridge configurations.

When the driven power switch is in the OFF state the driver operates to avoid the induced turn-on phenomenon that may occur due to C_{GD} capacitance during the turn-off of the other switch in the same leg.

The 6 A and 10 A variants feature a Miller CLAMP pre-driver, suitable for driving an external low voltage N-channel MOSFET. This gives maximum flexibility in terms of the CLAMP current capability, and even more importantly, allows to implement very short connection between the CLAMP MOSFET and the power-switch Gate and Source pins. This is crucial to maintain the CLAMP loop inductance small and thus avoid ringing and oscillations that affect EMI performance and efficiency.

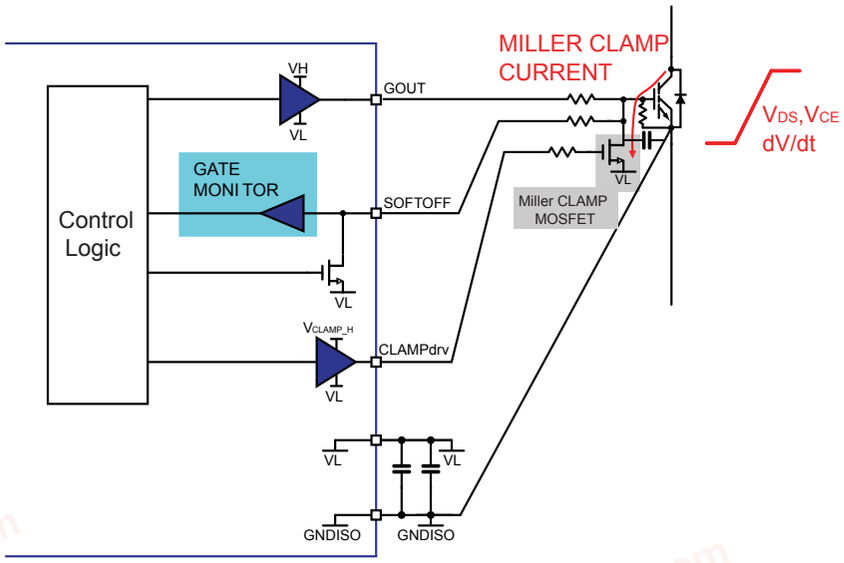
In some cases, when layout constraints do not allow for optimal loop inductance minimization, it can be beneficial to add a small resistor (< 1 Ω) between the Miller CLAMP Drain and the power switch Gate in order to damp residual oscillations.

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6.4.1 Miller clamp driver

In the STGAP3S variants that feature a Miller clamp pre-driver, the gate voltage of the external switch is monitored by the SOFTOFF pin (see Figure 8). The connection of this pin to the power switch gate by means of a resistor is therefore mandatory in order to use the Miller clamp function.

Figure 8. External Miller CLAMP driver, schematic principle

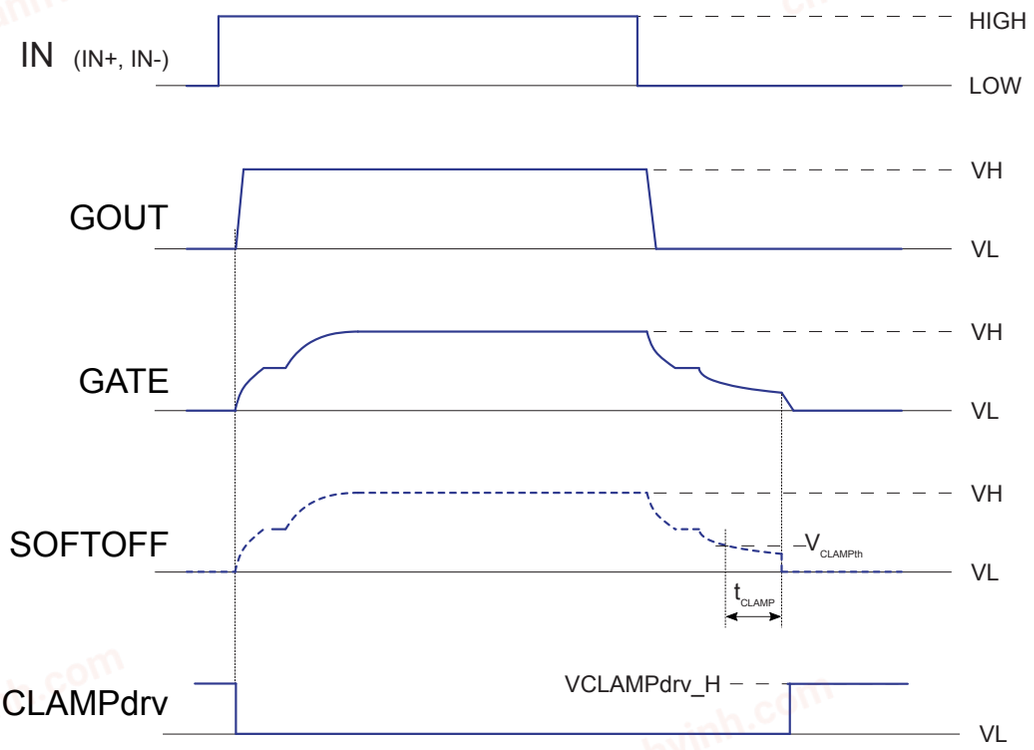


During a standard turn-off commutation, the gate of the external Clamp switch is activated when the voltage on the SOFTOFF pin goes below the $V_{CLAMPth}$ threshold voltage (refer to Figure 9).

The CLAMPdrv pin can drive an external low-voltage N-channel MOSFET, thus creating a low impedance path between the switch gate and VL pin.

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Figure 9. **External Miller CLAMP driver, timings definition**



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6.5 Desaturation protection

This feature allows implementing an overload and short-circuit protection for the external power switch.

The DESAT pin monitors the drain/collector during the ON time (see Figure 10), and if the protection threshold is reached the external power switch is turned off. The DESAT fault is notified to the control side, which turns on the dedicated $\overline{DIAG}$ diagnostic pin.

When the external power switch is off (GOUT = LOW), the DESAT pin is kept low by the internal N-channel discharge MOSFET, to maintain the external blanking capacitor connected to the DESAT pin discharged.

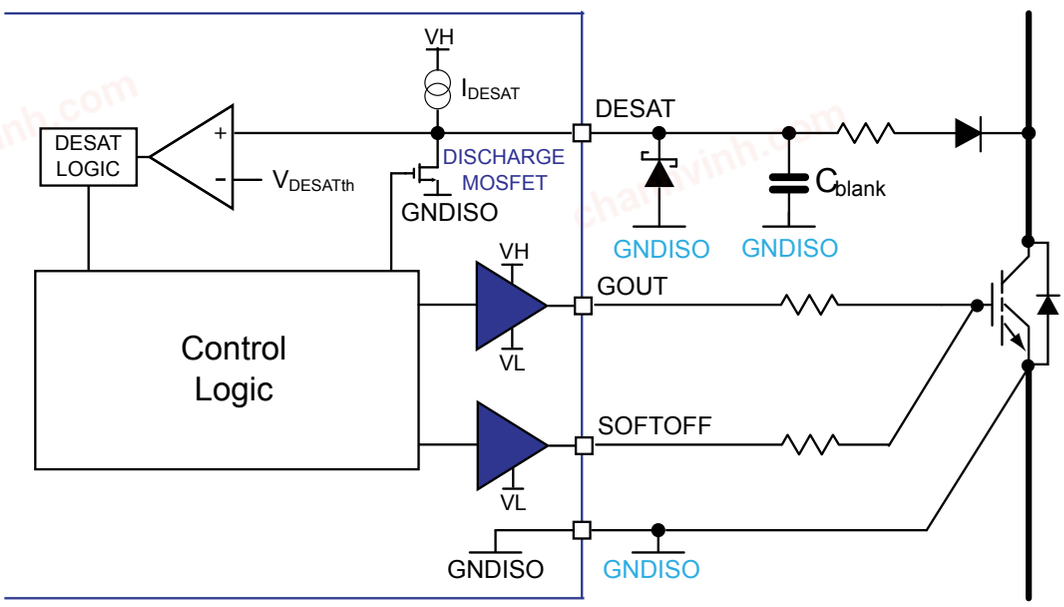
As soon as the external power switch turn-on command is received (GOUT = HIGH), a fixed blanking time with t_{BLK} duration is executed, after which the internal discharge switch between the DESAT and GNDISO pins is turned off allowing the internal current generator (I_{DESAT}) to charge the external blanking capacitor.

A deglitch filter is implemented on the DESAT pin: each pulse exceeding the $V_{DESATth}$ for a time shorter than $t_{DESfilter}$ does not triggers the protection.

If a desaturation event occurs the V_{CE}/V_{DS} voltage increases and when the voltage at the DESAT pin reaches the desaturation threshold $V_{DESATth}$, the protection is triggered and after a t_{DESAT} time the output is turned off and the device is forced in “safe state”. The open drain $\overline{DIAG}$ pin is set low within a t_{DIAG} time after the triggering of the protection.

The protection is latched and can only be reset by forcing the $\overline{RST}$ pin low for at least t_{rst} time.

Figure 10. DESAT protection connection diagram, adjustable soft turn-off



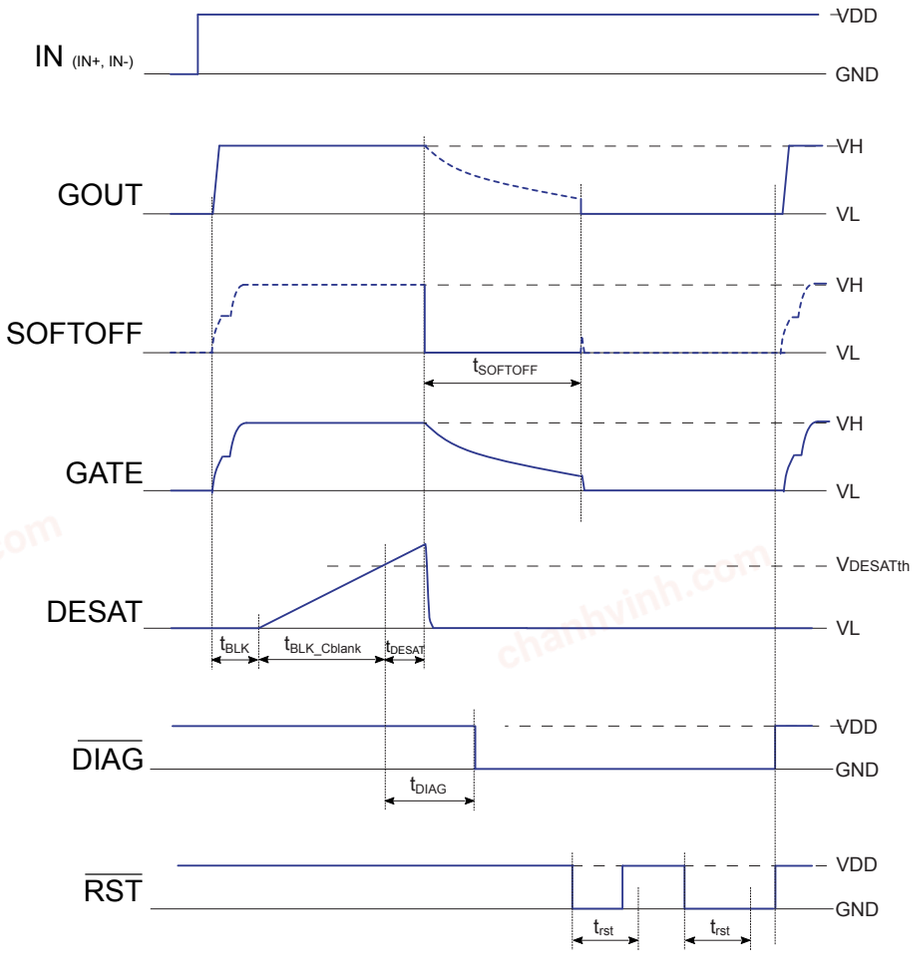
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6.5.1 Adjustable soft turn-off function

The STGAP3S6 and STGAP3SX feature an adjustable soft turn-off function, for optimized overload and short-circuit protection.

The timing diagrams for these parts are shown in Figure 11.

Figure 11. DESAT protection timings, adjustable soft turn-off



The soft turn-off function can be used to slow down the turn-off of the external MOSFET/IGBT when a desaturation event is triggered. This allows the reduction of the dangerous overvoltage spike on the drain/collector.

The soft turn-off function switches off the external power MOSFET/IGBT; a dedicated N-channel MOSFET connected to the SOFTOFF pin. The connection of the SOFTOFF pin to the external power MOSFET/IGBT gate through a resistor is mandatory in order to execute the turn-off when DESAT is triggered.

Thanks to the dedicated SOFTOFF pin, the STGAP3S offers the great advantage to fine-tune the turn-off speed in case of overload or short-circuit condition, thus allowing to find the best compromise between the reduction of the drain/collector overvoltage spike and the effective protection of the power switch from the excessive power dissipation caused by the overload. The optimal turn-off speed can be achieved by selecting the proper value of the soft turn-off external resistor.

As soon as a DESAT event is triggered, GOUT is immediately set in high impedance, the SOFTOFF internal MOSFET is turned on, and the SoftOff timer is started. This condition executes a controlled speed turn-off, which continues until one of the following conditions is verified:

- The SoftOff timer expires after a $t_{SOFTOFF}$ time from the DESAT triggering.
- The voltage on the external power switch reaches the $V_{CLAMPth}$ voltage threshold.

Afterwards, the SOFTOFF internal MOSFET is turned-off while the GOUT pin is actively forced low in order to complete the turn-off of the external power MOSFET/IGBT.

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6.6 Watchdog

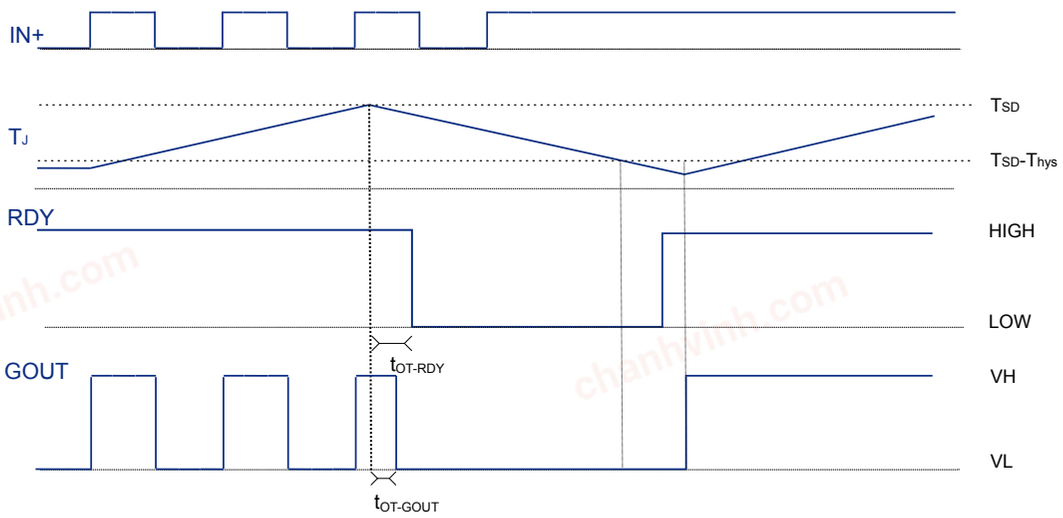
A watchdog function is implemented in the driver in order to identify when it is not able to communicate, for example because the supply voltage is not present on the control side or on the driving side.

If the control side supply is missing or in UVLO condition, the driving side immediately sets the output low and goes in “safe state”. If the driving side supply is missing, or in UVLO condition, the driver goes in “safe state” and the open drain RDY diagnostic pin is turned on after a t_{VH-RDY} time. This condition is maintained until a communication link is properly established.

6.7 Thermal shutdown protection

The device provides a thermal shutdown protection. When the junction temperature reaches the T_{SD} temperature threshold, the device is forced in “safe state”. The device operation is restored as soon as the junction temperature is lower than 'T_{SD} - T_{hys}'.

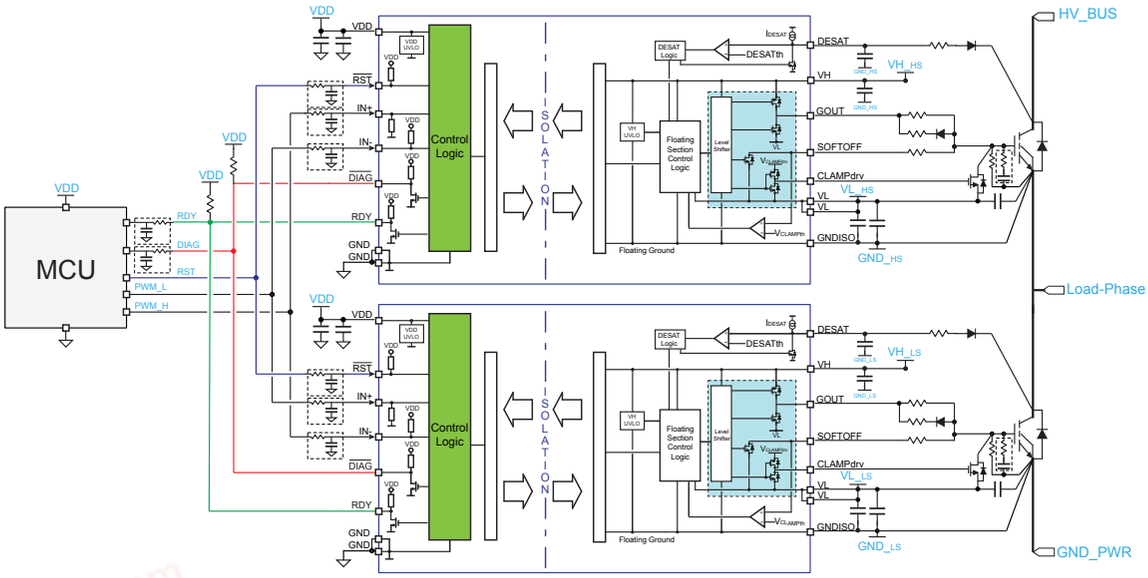
Figure 12. Overtemperature protection timings



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7 Typical application diagram

Figure 13. **Typical application diagram - external Miller clamp and SOFTOFF**



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8 PCB layout

8.1 Layout guidelines and considerations

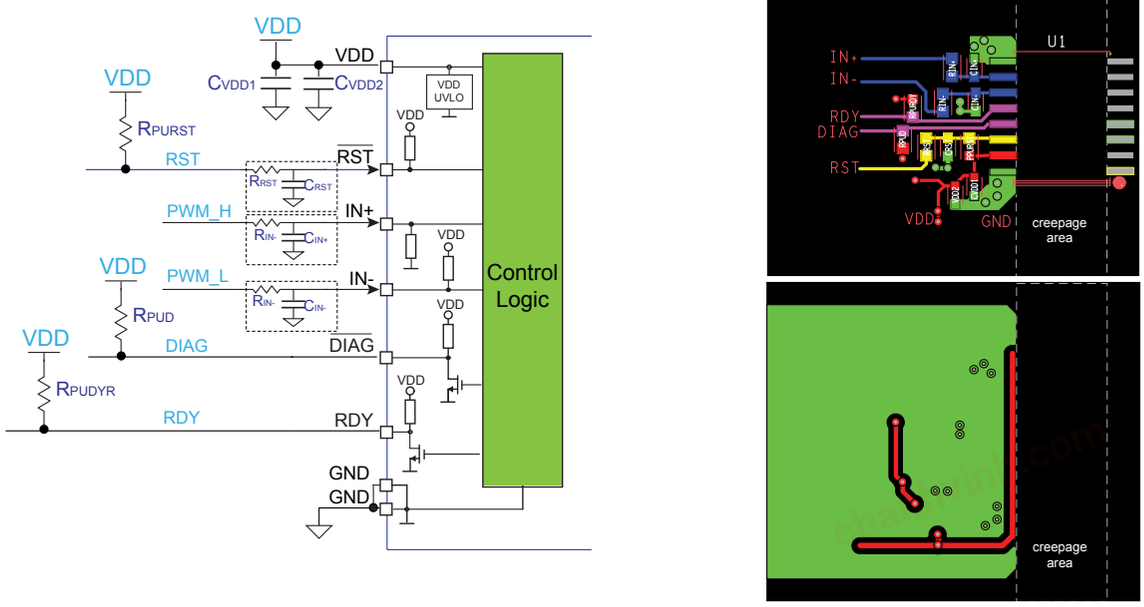
In order to optimize the PCB layout, the following considerations should be considered:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pin. In order to filter high-frequency noise and spikes, a 100 nF capacitor must be placed between VDD and GND, between VH and GNDISO, and between VL and GNDISO, as close as possible to device pins. In order to provide local storage for pulsed current, a second capacitor with a value between 1 µF and 10 µF should also be placed close to the supply pins.
- It is good practice to add filtering capacitors close to logic inputs of the device (IN+, IN-), particularly for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver to minimize the gate loop area and inductance that might carry noise or cause ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH and GNDISO pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

8.2 Layout example

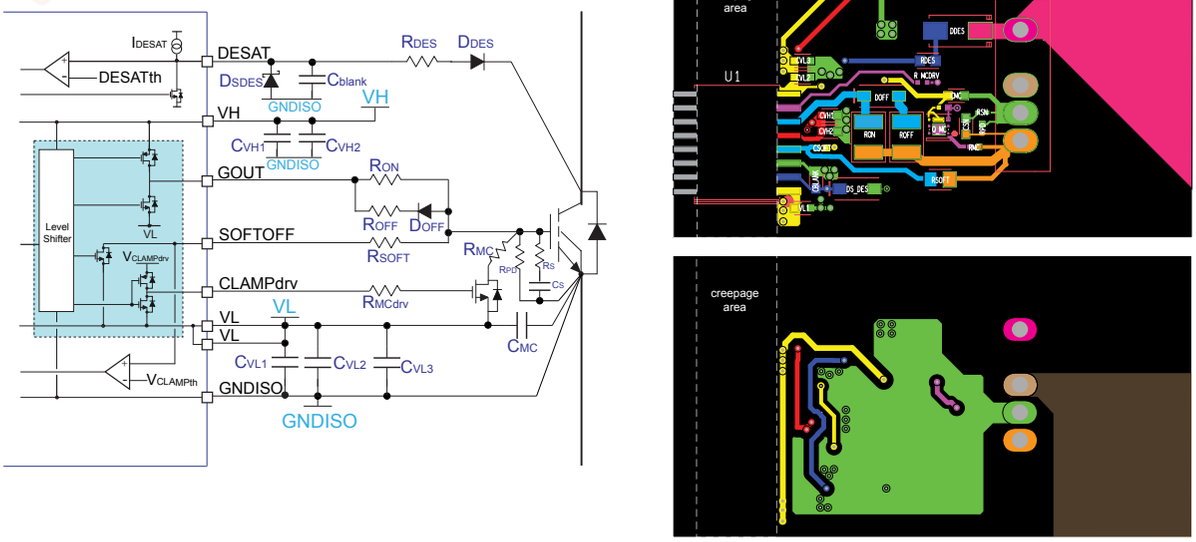
An example of STGAP3S suggested PCB layout with main signals highlighted by different colors is shown in Figure 14 and Figure 15. It is recommended to follow this example for optimal positioning and connection of external components, filtering and bypass capacitors in particular.

Figure 14. Reference layout - control side (top and bottom view)



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Figure 15. **Reference layout - gate driving side (top and bottom view)**



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9 Unused functions

The following table lists the connections to be performed when one or more functions of the devices are unused.

Table 8. Unused functions connections

Unused functionality	Connections	Notes
Desaturation protection	• Connect DESAT to GNDISO • Leave $\overline{\text{DIAG}}$ floating • Connect SOFTOFF to VL only if Miller CLAMP is not used	If Miller CLAMP function is used, connect SOFTOFF pin to power switch gate by means of a resistor R ≥ 10 Ω.
Miller CLAMP	• Leave CLAMPdrv floating • Connect SOFTOFF to VL only if Desaturation Protection is not used	If desaturation protection is used, connect SOFTOFF pin to power switch gate by means of a properly dimensioned resistor.
UVLO and thermal shutdown reporting	• Leave RDY floating	UVLO and thermal shutdown protections are always active. Leave RDY floating only if reporting of the activation of such protections to the control unit is not needed by the application.

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10 Testing and characterization information

Figure 16. **Input to output timings definition**

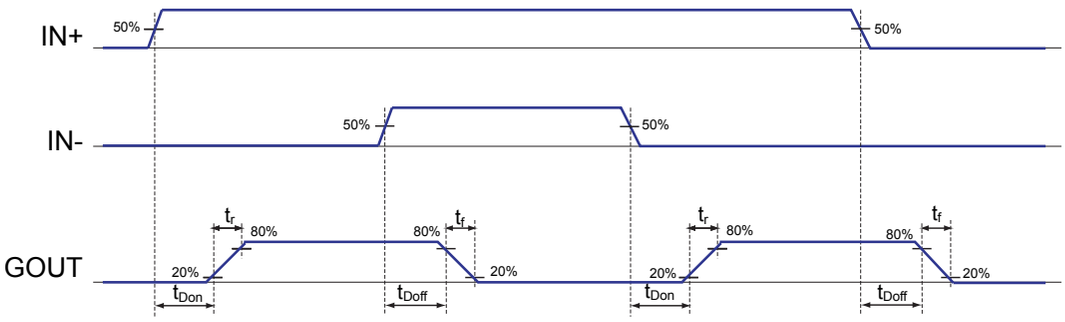
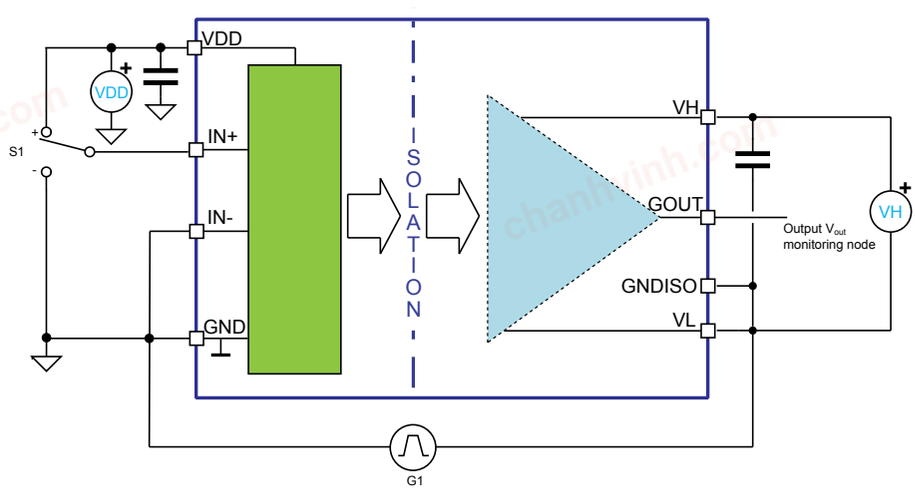


Figure 17. **CMTI test circuit**



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11 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 SO-16W package information

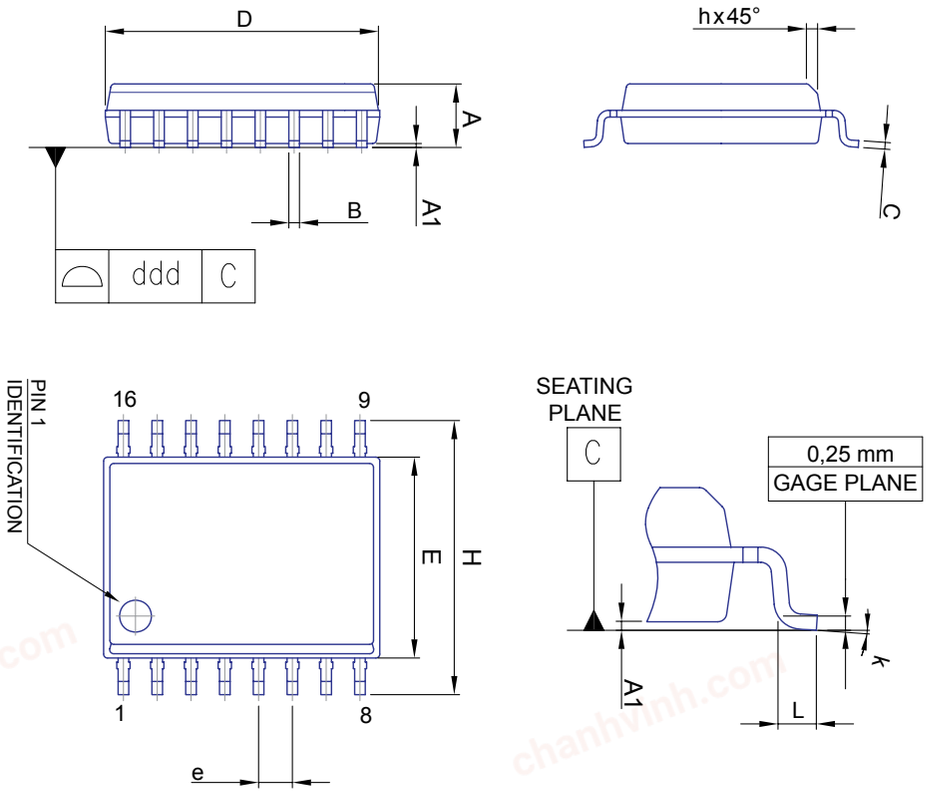
Table 9. SO-16W package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	2.35	-	2.65
A1	0.10	-	0.30
B	0.33	-	0.51
C	0.23	-	0.32
D (1)	10.10	-	10.50
E	7.40	-	7.60
e		1.27	
H	10.00	-	10.65
h	0.25	-	0.75
L	0.40	-	1.27
k (2)	0		8
ddd		0.25	

1. *Dimension “D” does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.*
2. *Degrees.*

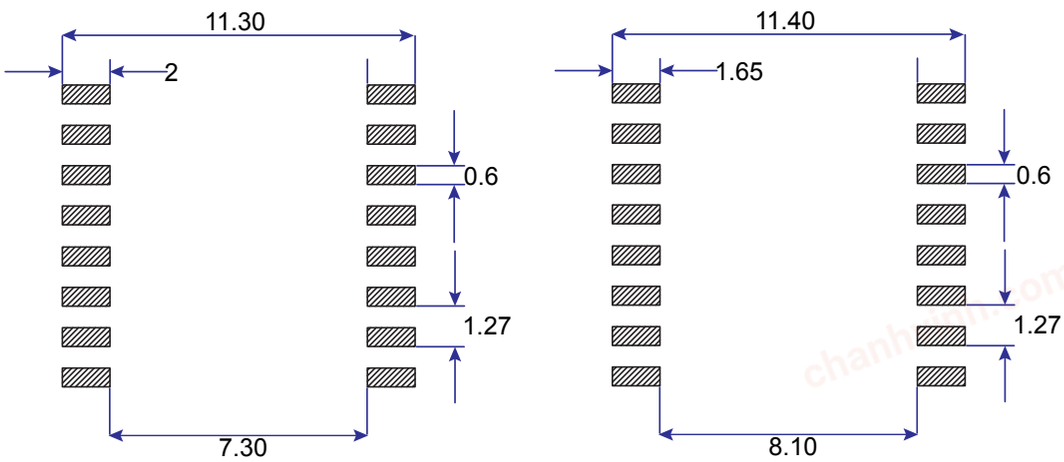
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Figure 18. **SO-16W mechanical data**



11.2 SO-16W suggested land pattern

Figure 19. **SO-16W suggested land pattern**



IPC-SM-782A
7.3 mm CLEARANCE/CREEPAGE

HV/ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

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12 Ordering information

Table 10. **Device summary**

Order code	Driving stage	UVLO	SOFTOFF	Package	Package marking	Packing
STGAP3S6I	±6 A CLAMP driver	IGBT	Tunable	SO-16W	GAP3S6I	Tube
STGAP3S6ITR	±6 A CLAMP driver	IGBT	Tunable	SO-16W		Tape and reel
STGAP3SXI	±10 A CLAMP driver	IGBT	Tunable	SO-16W	GAP3SXI	Tube
STGAP3SXITR	±10 A CLAMP driver	IGBT	Tunable	SO-16W		Tape and reel
STGAP3S6S	±6 A CLAMP driver	SiC	Tunable	SO-16W	GAP3S6S	Tube
STGAP3S6STR	±6 A CLAMP driver	SiC	Tunable	SO-16W		Tape and reel
STGAP3SXS	±10 A CLAMP driver	SiC	Tunable	SO-16W	GAP3SXS	Tube
STGAP3SXSTR	±10 A CLAMP driver	SiC	Tunable	SO-16W		Tape and reel

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Revision history

Table 11. **Document revision history**

Date	Version	Changes
23-Oct-2024	1	Initial release.
26-Nov-2024	2	Updated Table 2: removed T_{amb}, Table 5: added t_{INmin} test conditions, Table 6: removed sample test in R_{IO} test conditions at T_{amb} = 25 °C, Table 10: update package marking. Updated Figure 5, and Figure 12.

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