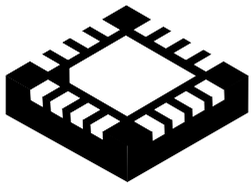
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STCC2540

USB charging controller with integrated power switch

Datasheet - production data



VFQFPN 16L 3 x 3 x 0.8 mm

Features

- Compliant with USB charging specifications BC1.2, USB 2.0 and USB 3.0 standards
- Compliant with Chinese telecommunications industry standard YD/T 1591-2009
- Compatible with proprietary charging mode (Apple® 1 A / 2 A, BlackBerry®, Korean tablets)
- Wide bandwidth, low-loss USB 2.0 data switch
- Integrated V_{BUS} power switch with low R_{ON} of 65 mΩ
- Constant current mode overcurrent protection
- Soft-start to limit inrush current
- Adjustable current limit up to 2.8 A
- Short-circuit, thermal and undervoltage protection
- Reverse voltage and reverse current protection
- Deglitched fault reporting output
- Supports remote wakeup in S3
- Charging indication output in DCP and CDP modes
- Package: VFQFPN 16L 3 x 3 x 0.8 mm with exposed pad
- Temperature range: -40 up to 85 °C
- UL and CB recognized components (UL file number: E354278)

Applications

- USB ports / hubs
- Personal computers, all-in-one PCs
- Monitors
- Notebooks, ultrabooks
- Tablet PCs
- Universal wall charging adapters

Description

The STCC2540 device integrates, in one package, a USB charger controller, a wide bandwidth data switch, and a high current power switch. The device emulates several profiles compatible with the USB battery charging standard, BC1.2, Chinese telecommunications standard YD/T 1591-2009, and proprietary charger modes.

The device asserts the charging flag in DCP modes if the charging current is higher than the threshold. In CDP mode, it asserts the charging flag after the CDP negotiation if the charging current is higher than the threshold.

After the current drops below the threshold, the output is deasserted, allowing the host to turn off the high power DC-DC converter and reduce overall consumption in S4/S5 states, which is critical when the host is battery supplied.

This is information on a product in full production. www.st.com

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1 Functional description

The STCC2540 device integrates, in one package, a complete solution to charge portable devices through USB ports, including:

- Charger emulator compatible with USB battery charging BC1.2 standard, Chinese telecommunications standard YD/T 1591-2009 and proprietary charger such as Apple® divider mode, BlackBerry® and Korean tablet charging mode.
- 3 control pins, CTL1, CTL2, CTL3 allowing the host to select the emulation profile. These pins may be controlled directly from the host USB controller or from the embedded controller.
- USB data switch with wide bandwidth up to 1100 MHz compliant with USB 2.0 standard. This wide bandwidth switch features low capacitance and low R_{ON} resistance, allowing signals to pass with minimum edge and phase distortion.
- N-channel power switch with low R_{ON} resistance of 65 mΩ typ., high current limiter accuracy and high current output capability, 2.5 A typ. The current limit threshold can be adjusted with a good accuracy by an external resistor in the range 500 mA to 2.8 A (max.).
  Constant current mode protection is used to protect the device and the host system against overcurrent or short-circuit. Other protection includes reverse current and reverse voltage protection, undervoltage lockout and thermal shutdown.
- A deglitched output ($\overline{\text{FAULT}}$) reporting the failure events of overcurrent, thermal shutdown and reverse current (backdrive) to V_{IN}.
- Charging current sensing circuit. The output $\overline{\text{CHARGING}}$ is asserted if charging current is above 20 mA in CDP and DCP modes.
  In CDP mode the charging flag is s asserted only if the CDP handshaking between the portable device and the host is performed before the current is above threshold.
  After the current drops below threshold, the output $\overline{\text{CHARGING}}$ is deasserted. The host system can then disable the high power DC-DC converter and thus reduce the power consumption. This is crucial when the host is battery supplied.
- An enable input (EN) to enable/disable the device.

The device is offered in a small, RoHS compliant VFQFPN 16L (3 x 3 x 0.8 mm) package with an exposed pad for effective cooling.

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Figure 1. Block diagram

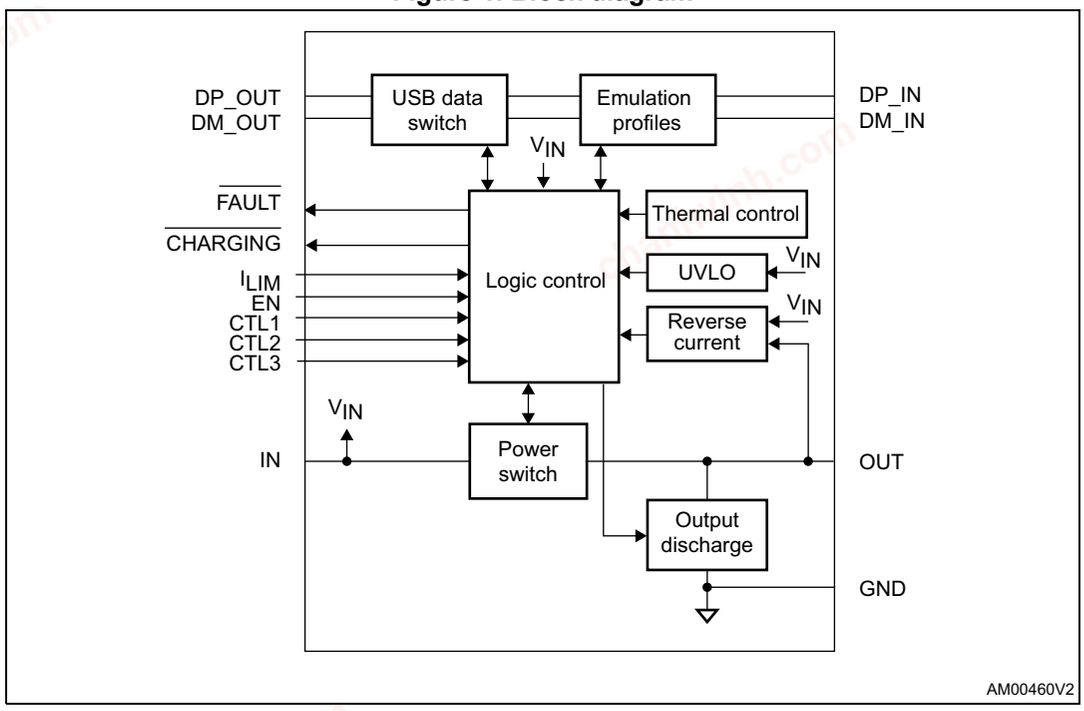
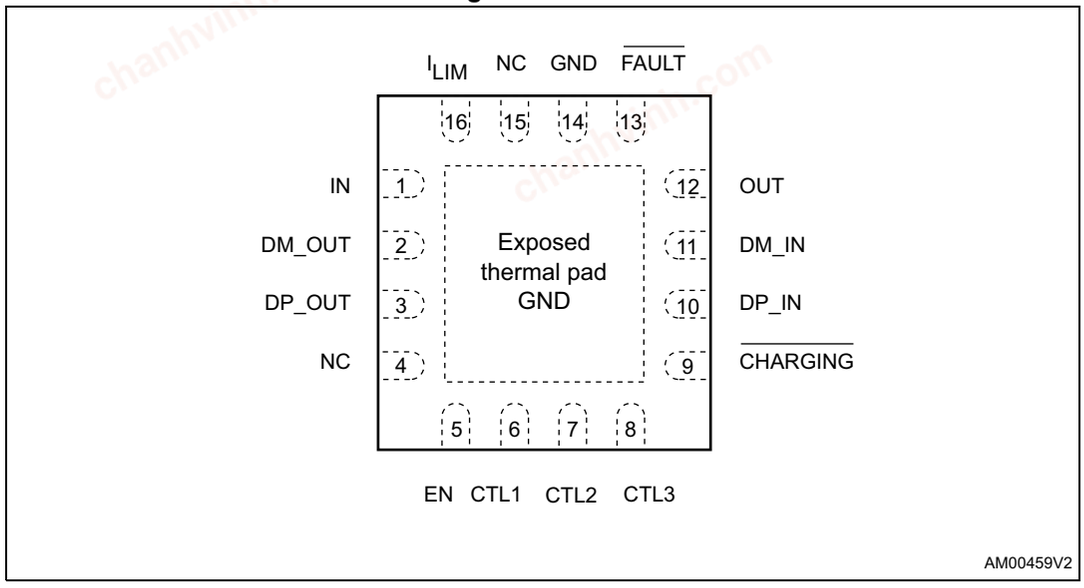


Figure 2. Pinout



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2 Pin description

Table 1. Pin description

Pin no.	Name	Type	Description
1	IN	PWR	Device and USB port power supply input
2, 3	DM_OUT, DP_OUT	I/O	USB 2.0 data connection to system USB transmitter (DM = D-, DP = D+)
4	NC	-	Not connected
5	EN	I	Logic level control input. When EN is low, power switch, data switch and emulator are OFF.
6, 7, 8	CTL1, CTL2, CTL3	I	Logic level control inputs to select charger mode (see *Table 5*).
9	$\overline{\text{CHARGING}}$	O	Active low open drain output, asserted when charging current is detected.
10, 11	DP_IN, DM_IN	I/O	USB 2.0 data connection to system USB connector (DM = D-, DP = D+)
12	OUT	PWR	USB port power supply output (V_{BUS})
13	$\overline{\text{FAULT}}$	O	Active low open drain output, asserted when overcurrent, overtemperature or reverse voltage are detected.
14	GND	-	Ground
15	NC	-	Not connected
16	I_{LIM}	I	Current limit threshold programming resistor terminal.

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3 Absolute maximum ratings and operating conditions

Stressing the device beyond the rating listed in *Table 2: Absolute maximum ratings (AMR)* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in *Table 3: Operating conditions* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{IN}, V_{OUT}	Supply voltage	-0.3 to 6.5	V
V_{EN}, V_{CTLx}	Logical input voltage	-0.3 to 6.5	
$V_{\overline{FAULT}}$, $V_{\overline{CHARGING}}$	Pull-up voltage ($\overline{FAULT}$, $\overline{CHARGING}$)	-0.3 to 6.5	
V_{DP_OUT}, V_{DM_OUT}, V_{DP_IN}, V_{DM_IN}	Data switch pin voltage to ground	-0.3 to V_{IN} +0.3	
I_{DP_OUT}, I_{DM_OUT}, I_{DP_IN}, I_{DM_IN}	Data switch current, switch ON	±50	mA
$I_{O(OUT)}$	Maximum power switch output current, power switch ON	Internally limited	-
$I_{O(\overline{FAULT})}$, $I_{O(\overline{CHARGING})}$	Logical output sink current	25	mA
T_{STG}	Storage temperature (V_{IN} OFF)	-55 to +150	°C
T_{SLD}	Lead solder temperature for 10 seconds temperature (V_{IN} OFF)(1)	260	
R_{thja}	Thermal resistance junction-to-ambient VFQFPN 16L(2)	60	°C/W
T_j	Maximum junction temperature (internally limited)	-40 to T_{STOP}	°C
$V_{ESD(OUT, DP_IN, DM_IN)}$	IEC61000-4-2 contact discharge (OUT, DP_IN, DM_IN pins)	8	kV
V_{ESD}	JEDEC human body model (all pins)(3)	2	
	JEDEC machine model (all pins)	200	V

1. Reflow at temperature of 255 to 260 °C for time < 30 seconds (total thermal budget not to exceed 180 °C for a period from 90 to 150 seconds).
2. R_{th} are typical values, given when mounted on a 4-layer PCB with vias.
3. Measured in recommended application circuit with 1 µF ceramic capacitor + 150 µF low ESR electrolytic capacitor connected between OUT and GND pins (see *Figure 4: Typical application diagram*).

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{IN}	Supply voltage	4.5 to 5.5	V
T_A	Ambient operating temperature	-40 to +85	°C
T_J	Junction operating temperature	-40 to +125	

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4 Electrical characteristics

Table 4. Electrical characteristics V_{IN} = 4.5 to 5.5 V, -40 °C < T_J < 125 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current consumption						
I_{ACTIVE}	Supply current in active state (EN = 1)	Mode CDP (111)		110	160	µA
		Mode SDP (110 - 010)		100	150	
		Mode DCP auto-detect (001) – Divider mode – BC1.2		 260 110	 290 180	
		Mode DCP BC1.2 (100)		110	180	
		Mode DCP divider (101)		210	290	
$I_{DISABLED}$	Supply current in disable state	EN = 0, T_J = 25 °C		0.2	5	
		T_J = 125 °C			60	
Power switch - DC parameters						
R_{ON}	Static on-resistance	T_J = 25 °C		65		mΩ
		-40 °C < T_J < 125 °C			95	
$\lvert I_{REVERSE} \rvert$	Reverse leakage current in disabled state (absolute value)	V_{OUT} = 5.5 V, V_{IN} = 0, V_{EN} = 0, T_J = 25 °C, measured at IN		1	5	µA
		T_J = 125 °C, other conditions the same as above			70	
$V_{REVERSE}$	Reverse voltage protection threshold (V_{OUT} - V_{IN})	V_{UVLO} < V_{IN} < V_{OUT}, EN = 1, power switch ON -> OFF		60		mV
I_{OS}	Current limiter threshold	R_{ILIM} = 96 kΩ	340	500	625	mA
		R_{ILIM} = 33 kΩ	1290	1450	1595	
		R_{ILIM} = 19.6 kΩ	2255	2450	2645	
		R_{ILIM} = 17.2 kΩ		2800		
T_{STOP}	Thermal shutdown threshold		140	150	160	°C
T_{HYST}	Thermal shutdown hysteresis			20		
$_{I}EN$	EN input leakage current	V_{IN} = 5.5 V, V_{EN} = 0 V or 5 V	-1		1	µA
V_{EN}	Enable input turn-on, turn-off threshold voltage		0.4		1.6	V
$V_{HYST(EN)}$	Enable input turn-on, turn-off voltage hysteresis			500		mV
$V_{OL(\overline{FAULT})}$	$\overline{FAULT}$ output low voltage	$I_{\overline{FAULT}}$ = 1 mA			180	

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Table 4. Electrical characteristics V_{IN} = 4.5 to 5.5 V, -40 °C < T_J < 125 °C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{OL(\overline{FAULT})}$	$\overline{FAULT}$ output leakage current	V_{IN} = 5.5 V, $V_{\overline{FAULT}}$ = 5 V			1	µA
$t_{\overline{FAULT}}$	$\overline{FAULT}$ output deglitch delay	$\overline{FAULT}$ assertion / deassertion delay in overcurrent condition	7	9	12	ms
V_{UVLO}	Undervoltage lockout	V_{IN} rising	3.9	4.1	4.3	V
$V_{HYST(UVLO)}$	Undervoltage lockout hysteresis	T_J = 25 °C		100		mV
Power switch - AC parameters(1)						
t_{ON}	Turn on, EN to OUT delay	C_{LOAD} = 1 µF, R_{LOAD} = 100 Ω		0.8		ms
t_{OFF}	Turn off, EN to OUT delay			0.3		
t_R	OUT (V_{BUS}) rise time	C_{LOAD} = 1 µF, R_{LOAD} = 100 Ω		0.4		
t_F	OUT (V_{BUS}) fall time			0.2		
t_{IOS}	Current limiter response time to short-circuit	V_{IN} = 5.5 V		3.5		µs
Output discharge						
$R_{DISCHARGE}$	Discharge resistor		140	200	300	Ω
High-speed data switch - DC parameters						
R_{ON}	Data switch on-resistance	Switch closed, V_{IN} = 5 V, I_S = 8 mA, test voltage on DP_OUT, DM_OUT = 0.4 V		2.5	4	Ω
R_{ON}	Data switch on-resistance	Switch closed, V_{IN} = 5 V, I_S = 8 mA, test voltage on DP_OUT, DM_OUT = 3 V		2.7	4	
I_{OFF}	OFF state leakage current	V_{EN} = 0 V, VDP/DM_IN = 3.6 V, VDP/DM_OUT = 0 V, measure IDP/DM_OUT			1.5	µA
High-speed data switch - AC parameters(1)						
X_{TALK}	DP, DM crosstalk	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF, V_S = 1 V_{rms}, signal = 0 dBm, f = 250 MHz		47		dB
O_{IRR}	OFF state isolation	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF, V_S = 1 V_{rms}, signal = 0 dBm, f = 250 MHz		17		
B_w	Bandwidth -3 dB	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF, signal = 0 dBm		1100		MHz
Charger emulator - BC1.2 DCP mode						
R_{DCP_RES}	DP_IN to DM_IN short resistance	CTLx configured for DCP BC1.2		100	170	Ω

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Table 4. Electrical characteristics V_{IN} = 4.5 to 5.5 V, -40 °C < T_J < 125 °C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Charger emulator - divider mode						
V_{DM}	DM_IN output voltage	Device set to DCP auto-detect mode or divider mode, V_{IN} = 5.0 V	1.96	2	2.04	V
V_{DP}	DP_IN output voltage		2.65	2.7	2.75	
R_{DM}	DM_IN output resistance	Device set to DCP auto-detect mode or divider mode		27		kΩ
R_{DP}	DP_IN output resistance			27		
Charger emulator - BC1.2 CDP mode						
V_{DM_SRC}	Voltage source on DM_IN for CDP detection	V_{DP_IN} = 0.6 V, device in CDP BC1.2 mode	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN rising voltage threshold to turn on V_{DM_SRC}	I_{DM_IN} = -250 µA, device in CDP BC1.2 mode	0.25	0.32	0.4	
$V_{DAT_REF_HYST}$	V_{DAT_REF} hysteresis			30		mV
V_{LGC_SRC}	DP_IN rising voltage threshold to turn off V_{DM_SRC}		0.8		1	V
$V_{LGC_SRC_HYST}$	V_{LGC_SRC} hysteresis			30		mV
I_{DP_SINK}	DP_IN sink current	0.4 < V_{DP_IN} < 0.8 V, device in CDP BC1.2 mode	50	75	150	µA
Charger emulator - timings						
$t_{CHG_DGL_ON}$	Charging indication ON deglitch delay	From I_{OUT} > I_{OUT_TH} to $\overline{CHARGING}$ asserted		0.5		s
$t_{CHG_DGL_OFF}$	Charging indication OFF deglitch delay	From I_{OUT} < I_{OUT_TH} to $\overline{CHARGING}$ deasserted		5		
$t_{VDM_SRC_ON}$	DM_IN voltage source turn-on time	From V_{DP_IN} 0 V -> 0.6 V to V_{DM_IN} = V_{DM_SRC}, CTLx configured for CDP BC1.2		8		ms
$t_{VDM_SRC_OFF}$	DM_IN voltage source turn-off time	From V_{DP_IN} 0.6 V -> 0 V to V_{DM_IN} = 0 V, CTLx configured for CDP BC1.2		1.3		
t_{VBUS_REAPP}	OUT discharge pulse width	From V_{OUT} falls to 0.7 V during discharge to V_{OUT} returning to 90%.	300	350	400	

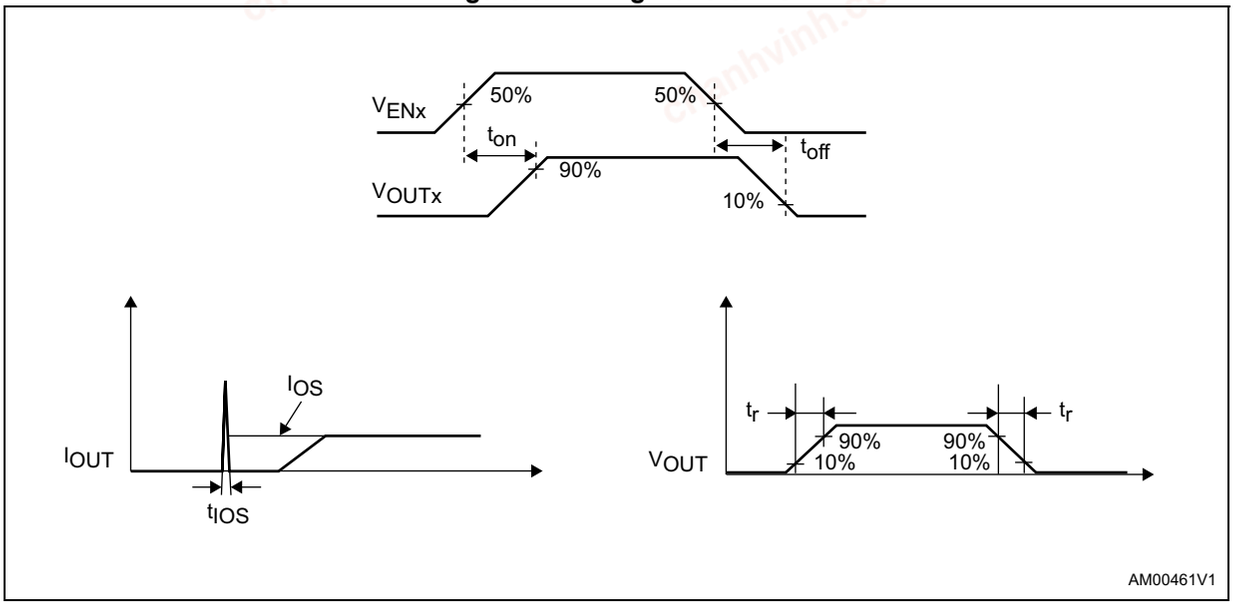
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Table 4. Electrical characteristics V_{IN} = 4.5 to 5.5 V, -40 °C < T_J < 125 °C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Charger emulator - control pins CTLx						
V_{CTLx}	CTLx pins threshold voltage		0.4		1.6	V
$V_{HYST(CTLx)}$	Hysteresis voltage on CTLx pins			500		mV
I_{CTLx}	Leakage current	V_{IN} = 5.5 V, V_{CTLx} = 0 V or 5 V	-1		1	µA
Charger emulator - charging indication						
I_{OUT_TH}	Output current threshold for charging detection	DCP mode, CDP mode		20		mA
$V_{OL(\overline{CHARGING})}$	$\overline{CHARGING}$ output low voltage	Charging detected (I_{OUT} > I_{OUT_TH}), $I_{\overline{CHARGING}}$ = 1 mA			180	mV
$I_{OL(\overline{CHARGING})}$	$\overline{CHARGING}$ output leakage current	V_{IN} = 5.5 V, $V_{\overline{CHARGING}}$ = 5 V			1	µA

1. Guaranteed by design. Not tested in production.

Figure 3. Timing waveforms



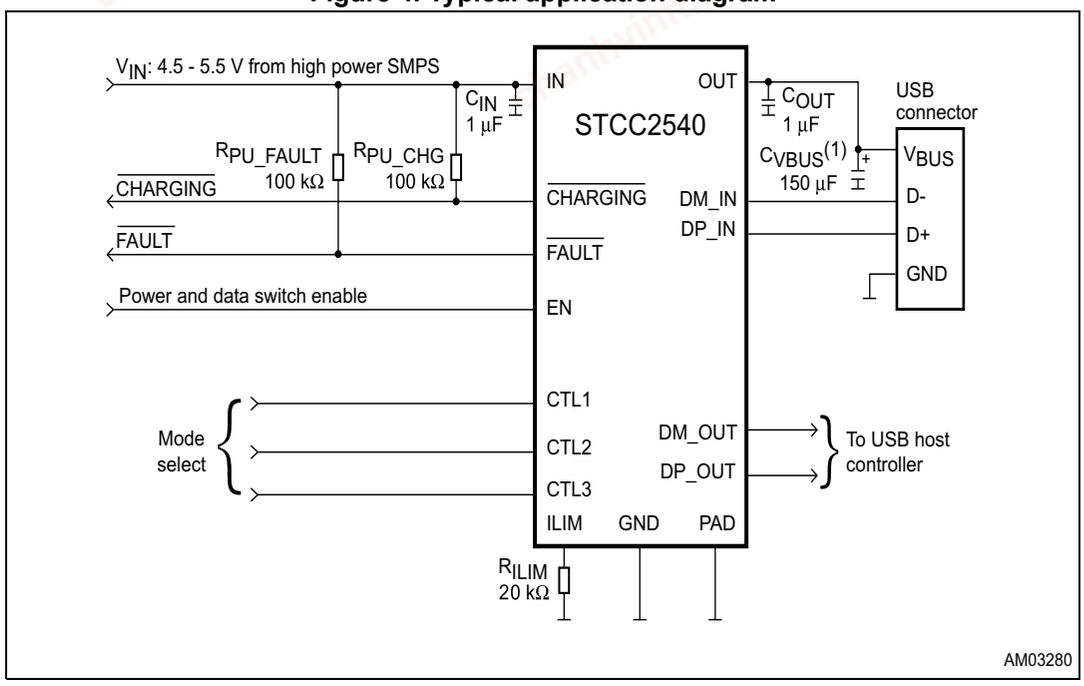
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5 Application information

The STCC2540 device is designed to be implemented into the PC on a USB port in order to emulate the wall charger adapter when the PC is in standby mode or OFF, and to allow higher charge current when the USB interface is used for data communication. In order to handle these functionalities, the STCC2540 device relies on USB BC1.2 specifications, Chinese telecommunications industry standard YD/T 1591-2009, and proprietary implementations.

- BC1.2 charging profiles are
  - CDP: charging downstream port providing data communication plus charging (active USB data communications with 1.5 A support)
  - SDP: standard downstream port providing data communication with no charging (active USB 3.0 data communications with 900 mA support or USB 2.0 data communications with 500 mA support)
  - DCP: dedicated charging port (wall charger emulation with no data communication and 500 mA to 1.5 A support)
- Chinese telecommunications standard
  - D+ and D- shorted to allow charging
- Apple divider mode (2 A max. current)
- BlackBerry emulator mode
- Legacy mode (allowing 500 mA charging current)
- Korean tablet charging mode (D+ and D- shorted and pulled up to a certain voltage)

Figure 4. Typical application diagram



1. C_{VBUS} required by the USB specification.

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5.1 Supported modes

For more information refer to *Section 5.4: State machine*.

The STCC2540 device supports the following modes:

- SDP BC1.2
- CDP BC1.2
- SDP with remote wakeup for all USB devices
- CDP with remote wakeup for low-speed USB devices with automatic transition to DCP auto mode if a full-speed/high-speed USB device attached or after a USB device detached.
- DCP auto-detect: this mode permits auto-detection of charging modes between DCP BC1.2 (shorted D+, D-) and divider charging mode. It also supports BlackBerry charging mode and can charge legacy devices and Korean tablets.
- Forced DCP BC1.2 mode
- Forced DCP divider mode

The auto-detect mode starts in divider mode. If charging negotiation attempt is detected, there is an automatic transition to DCP BC1.2 mode. It is preceded by V_{BUS} discharge pulse to initialize the proper BC1.2 handshake process. If the BC1.2 device is detached, the circuit automatically returns to divider mode after a 10 s (typ.) timeout.

Note: From an application point of view it means that after removing one device the user should wait for approx. 15 s before attaching another device.

Selection between these modes is done through the CTLx control pins. The CTLx pins may be controlled by the host in different ways:

- GPIO from embedded controller
- Hardware signals from USB host controller (SLP_S3#, SLP_S4#) and AC_adapter signal from embedded controller
- Hardware signals SUSPEND from embedded controller and AC_ADAPTER.

Table 5. Truth table control pins CTLx(1)

Host state	CTL1	CTL2	CTL3	Mode description
	0	0	0	Device off, output discharge
S0, S1, (S3)(2)	1	1	0	SDP
S0, S1, (S3)(2)	1	1	1	CDP BC1.2 with charging detection.
S3, (S0, S1)(2)	0	1	0	SDP with remote wakeup for all USB devices
S3	0	1	1	CDP with remote wakeup for low-speed USB devices / DCP auto mode for full-speed or high-speed USB devices or after a USB device detached.
S4, S5	0	0	1	DCP auto-detect mode without remote wakeup, with charging detection
S4, S5	1	0	1	Forced DCP divider mode with charging detection
S4, S5	1	0	0	Forced DCP BC1.2 mode with charging detection

1. On the transition from the CTLx = 111 to CTLx = 001, a synchronous transition of the CTL1 and CTL2 must be ensured.
2. See *Section 5.2* for further information.

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5.2 Remote wakeup in S3

For more information refer to *Section 5.4: State machine*.

If the CTLx pins are controlled by hardware signals (such as SLP_Sx# or SUSPEND), the CTLx combination changes when host transitions from S0 to S3 and back. In this case, the STCC2540 device can support remote wakeup of portable devices for the following transitions (i.e. no V_{BUS} discharge pulse and data switch ON):

- SDP S0 (CTLx = 110) to and from SDP S3 (CTLx = 010) for all USB devices
- SDP (CTLx = x10) and CDP S0 (CTLx = 111) to and from CDP S3 (CLx = 011) for low-speed USB devices only.

If the host system is in S3 mode (CTLx = 011), the system automatically turns into DCP auto mode for already attached full-speed / high-speed USB devices or after any USB device is detached. Thus, already attached full-speed / high-speed devices or newly attached devices are charged without the need of CTLx transition.

If the S0 to S3 transition is managed by GPIO from the embedded controller, the easiest solution is to keep the same levels on the CTLx pins (SDP or CDP modes). Therefore, remote wakeup in S3 is supported for all USB devices but the system does not automatically turn into DCP auto mode.

5.3 V_{BUS} discharge

The V_{BUS} discharge pulse lasts for 350 ms typ. (t_{VBUS_REAPP}) and is performed for any transitions between the modes listed in *Table 5*, except the modes allowing remote wakeup in S3 [transitions (x10) and (111) to/from (011)] (see *Section 5.4*).

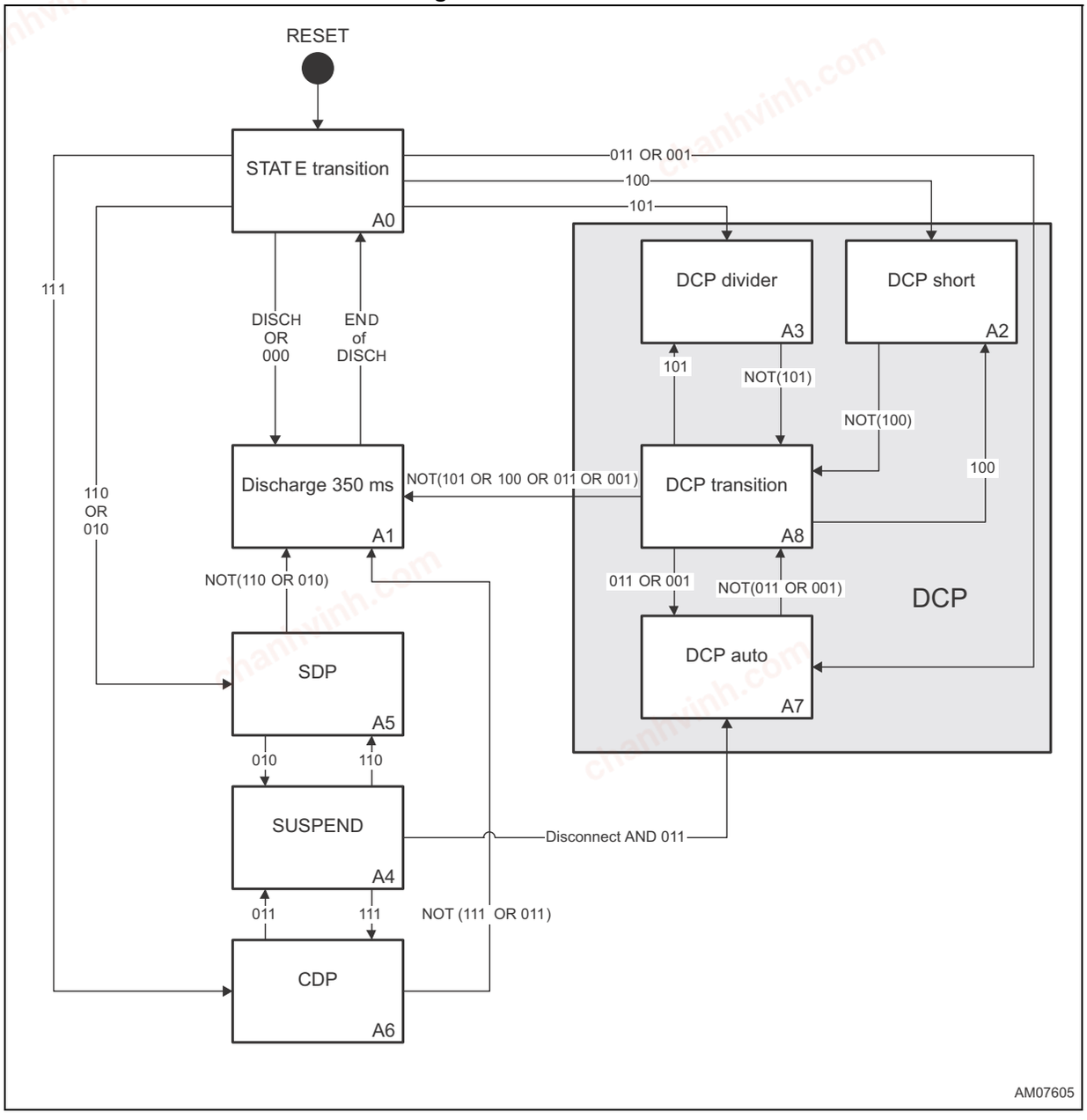
Permanent output discharge is provided in following modes:

- EN = 0, CTLx = xxx (ignored)
- EN = 1, CTLx = 000.

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5.4 State machine

Figure 5. State machine



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5.5 Charging detection

The STCC2540 device continuously monitors the current drawn by the portable device. While programmed in CDP or DCP mode, the STCC2540 device sends a charging flag to the system if the current through the USB power switch is above the charging threshold, set at 20 mA typ.: open drain active low output $\overline{\text{CHARGING}}$ is asserted.

Note: In CDP mode, the charging flag is asserted only if the CDP handshaking between the portable device and the host is performed before the current is above the threshold.

If a device is charging (CDP mode) while the system is turned off and the battery supplied, the risk is that the charging process stops before the end of charge due to the system power-off. To avoid this, the flag $\overline{\text{CHARGING}}$ can be used by the host to prevent the switching-off of the high power DC-DC converter when the host goes to S5 state, even if battery supplied.

After the charging current drops below the threshold and the deglitch delay expires, the $\overline{\text{CHARGING}}$ output is deasserted.

5.6 Power switch

Overcurrent conditions

When an overcurrent condition is detected, the device maintains a constant output current and reduces the voltage accordingly. There are two overload conditions:

- The first occurs when a short-circuit or a partial short-circuit is already present when the device is being powered-up or enabled. The output voltage is held near zero potential with respect to ground and the STCC2540 device ramps the output current to I_{OS} until the overload condition is removed or the device starts thermal cycle.
- The second condition is when a short-circuit, a partial short-circuit, or a transient overload occurs while the device is already enabled and powered-on. The STCC2540 device responds to an overcurrent condition within time t_{IOS}. The current-sense amplifier is overdriven during this time and momentarily disables the internal current limit MOSFET. It then recovers and ramps the output current to I_{OS}. Similar to previous conditions, it limits output current to I_{OS} until the overload condition is removed or thermal cycle starts.

Thermal protection

The STCC2540 device has an internal thermal sensing circuit which monitors the operating temperature of the circuit. It disables the power switch operation if the die temperature exceeds temperature threshold T_{STOP}, set at 150 °C. The switch turns on if the temperature has cooled down by 20 °C.

Undervoltage lockout

The UVLO circuit disables the circuit until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop during turn-on.

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$\overline{\text{FAULT}}$ functionality

The $\overline{\text{FAULT}}$ open drain active low output is asserted during overcurrent or overtemperature conditions. Signal is asserted until the fault is removed.

For overcurrent conditions, the STCC2540 device is designed to eliminate false $\overline{\text{FAULT}}$ reporting, by using an internal deglitch delay (9 ms typ.).

In the case of overtemperature, there is no deglitch delay and the $\overline{\text{FAULT}}$ signal is asserted immediately. It is deasserted with a delay after the device has cooled down and begins to turn on. This unidirectional glitch immunity prevents $\overline{\text{FAULT}}$ oscillation during an overtemperature event.

In the case of a fault condition, the host may disable the power switch by toggling EN input to logic low.

Current limit programming

The current limit can be adjusted by an external resistor in the range 500 mA to 2.8 A (max.). The programming resistor may be calculated using these equations:

Equation 1

$$I_{OS(typ)} = \frac{48000}{R_{ILIM}} (mA,\ k\Omega)$$

Equation 2

$$I_{OS(min)} = \frac{48000}{R_{ILIM}^{1.037}} (mA,\ k\Omega)$$

Equation 3

$$I_{OS(max)} = \frac{48000}{R_{ILIM}^{0.962}} (mA,\ k\Omega)$$

Equation 2 and *Equation 3* allow the minimum and maximum variation to be estimated around the typical value predefined by the external resistor, R_{ILIM}, given in *Equation 1*.

Equation 2 and *Equation 3* do not take into consideration external resistor variations.

5.7 Enable input

The enable input (EN, active high) serves to turn off the STCC2540 device and achieve the lowest current consumption.

The behavior of the STCC2540 in disabled state (EN = 0) is following:

- Power switch, USB data switch and emulation profiles are turned off
- Output discharge circuit is turned on
- The $\overline{\text{FAULT}}$ and $\overline{\text{CHARGING}}$ flags are cleared (the $\overline{\text{FAULT}}$ and $\overline{\text{CHARGING}}$ outputs are set to Hi-Z mode).

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5.8 Input and output capacitors

For proper functionality, the STCC2540 device requires two 1 µF decoupling ceramic capacitors C_{IN} and C_{OUT} (see *Figure 4*). These capacitors should be placed as close as possible to the corresponding pins.

The electrolytic capacitor C_{VBUS} (see *Figure 4*) is required by the USB specification to suppress the voltage and current transients caused by hot plugging/unplugging the peripheral devices. This capacitor should be placed as close as possible to the USB connector. The recommended value is 150 µF, low ESR type is preferred.

If the V_{IN} supply path is longer than approx. 150 mm, an additional capacitor is required and should be connected in parallel with the C_{IN} to suppress V_{IN} overvoltage transients caused by supply path inductance and fast current changes. The minimum value is 10 µF, and a low ESR type is preferred.

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6 Typical operating characteristics

Figure 6. Power switch ON resistance vs. temperature

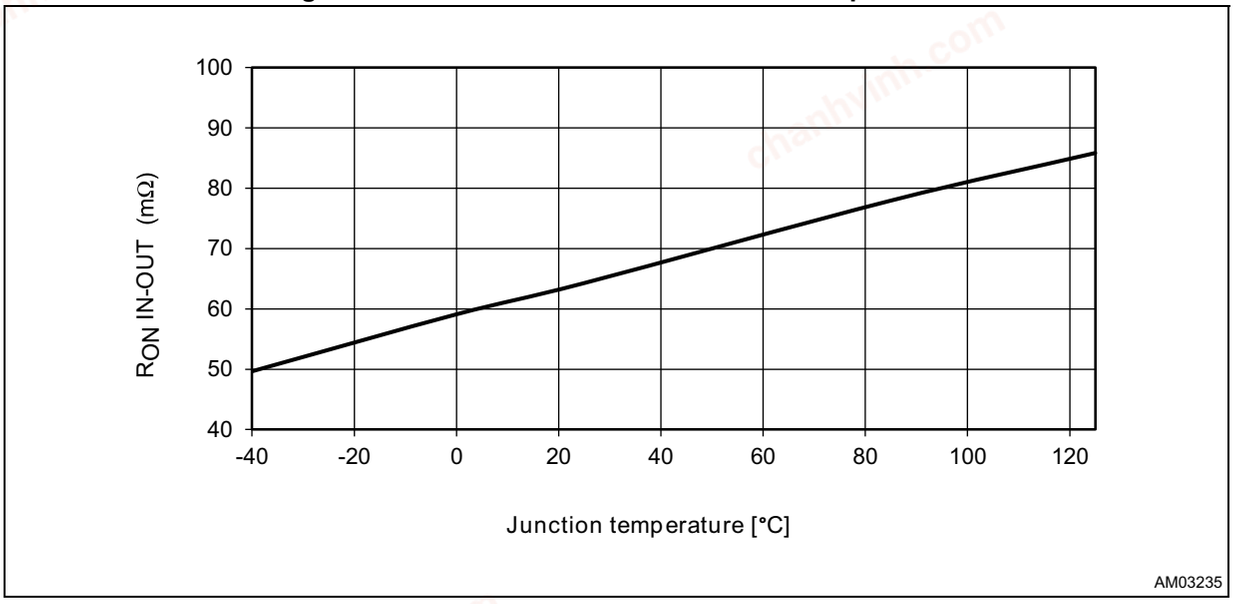
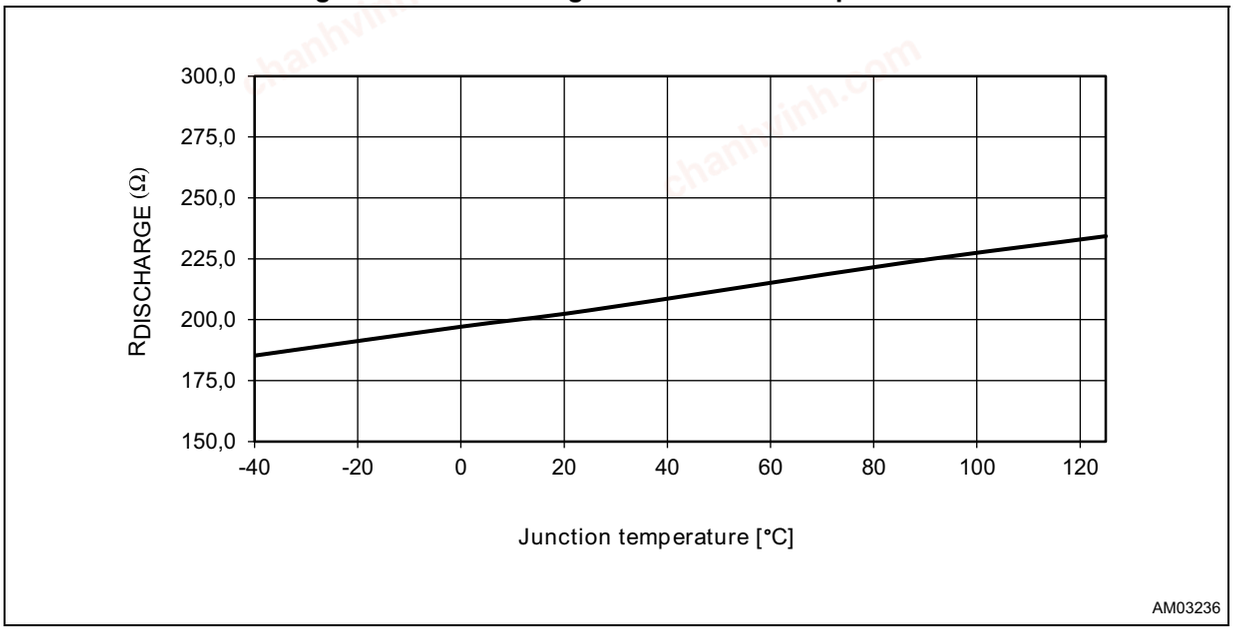


Figure 7. OUT discharge resistance vs. temperature



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Figure 8. OUT short-circuit current limit vs. temperature (R_{ILIM} = 96 kΩ)

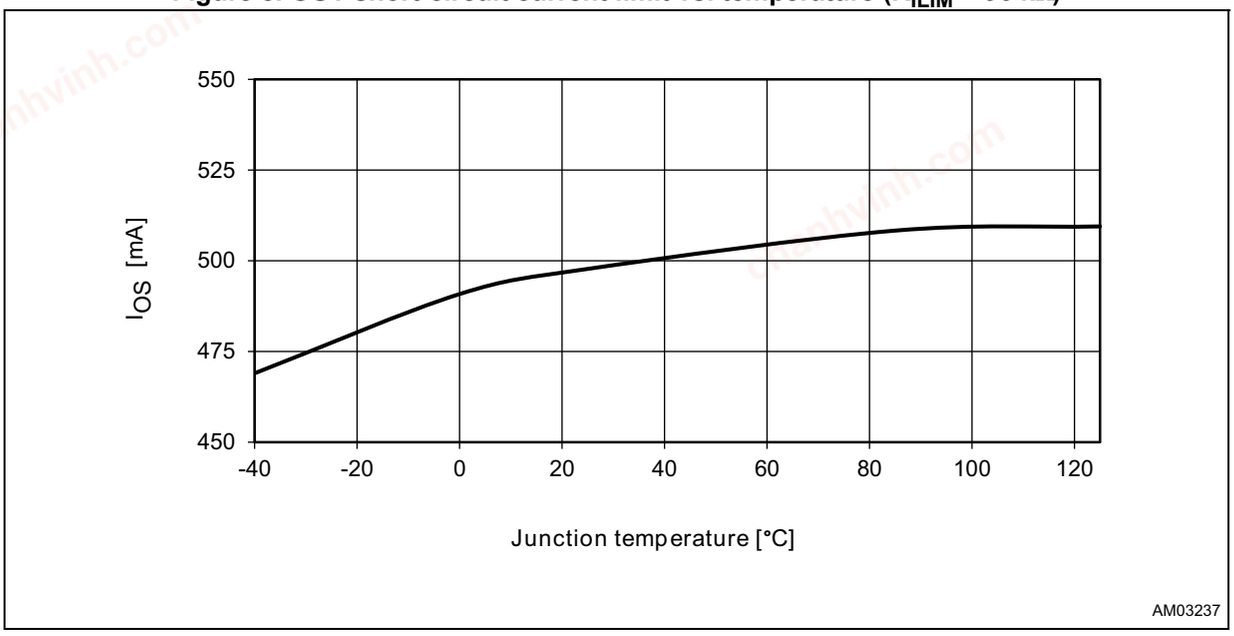
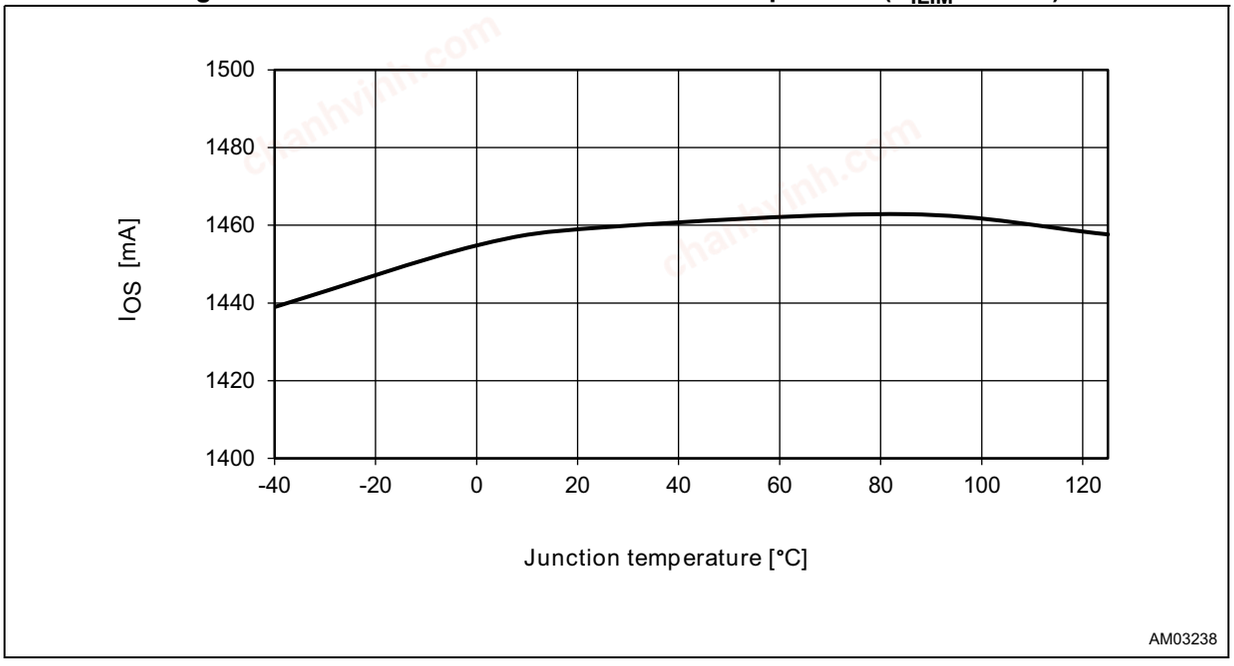


Figure 9. OUT short-circuit current limit vs. temperature (R_{ILIM} = 33 kΩ)



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Figure 10. OUT short-circuit current limit vs. temperature (R_{ILIM} = 19.6 kΩ)

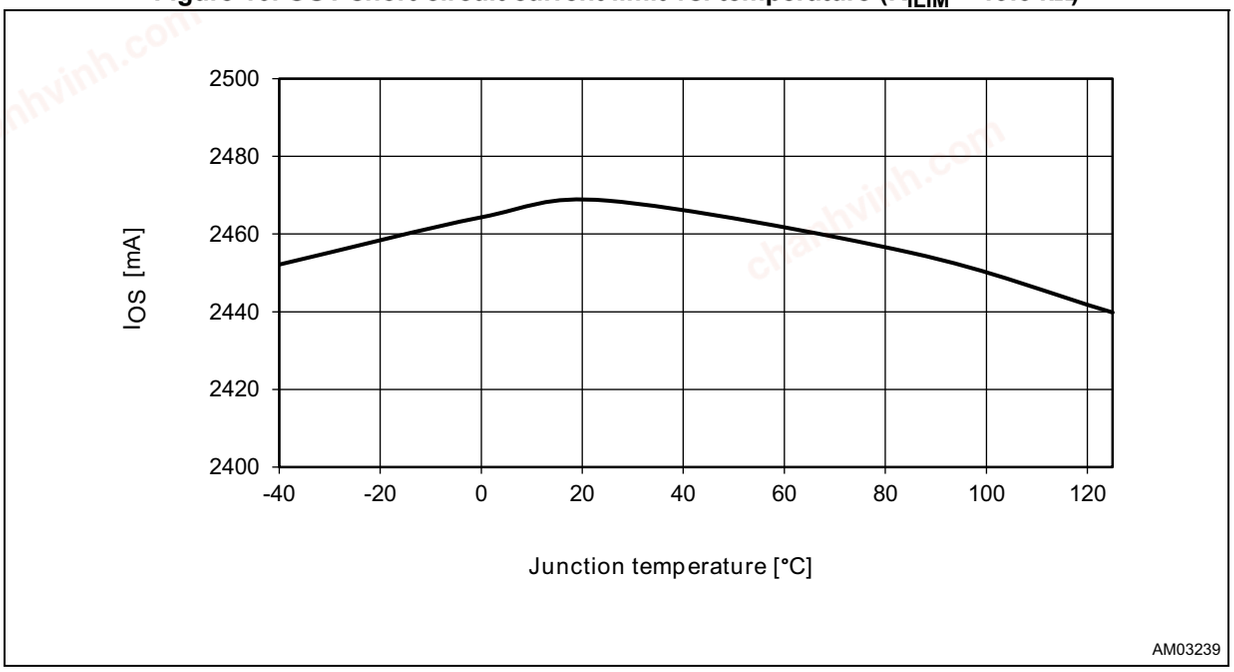
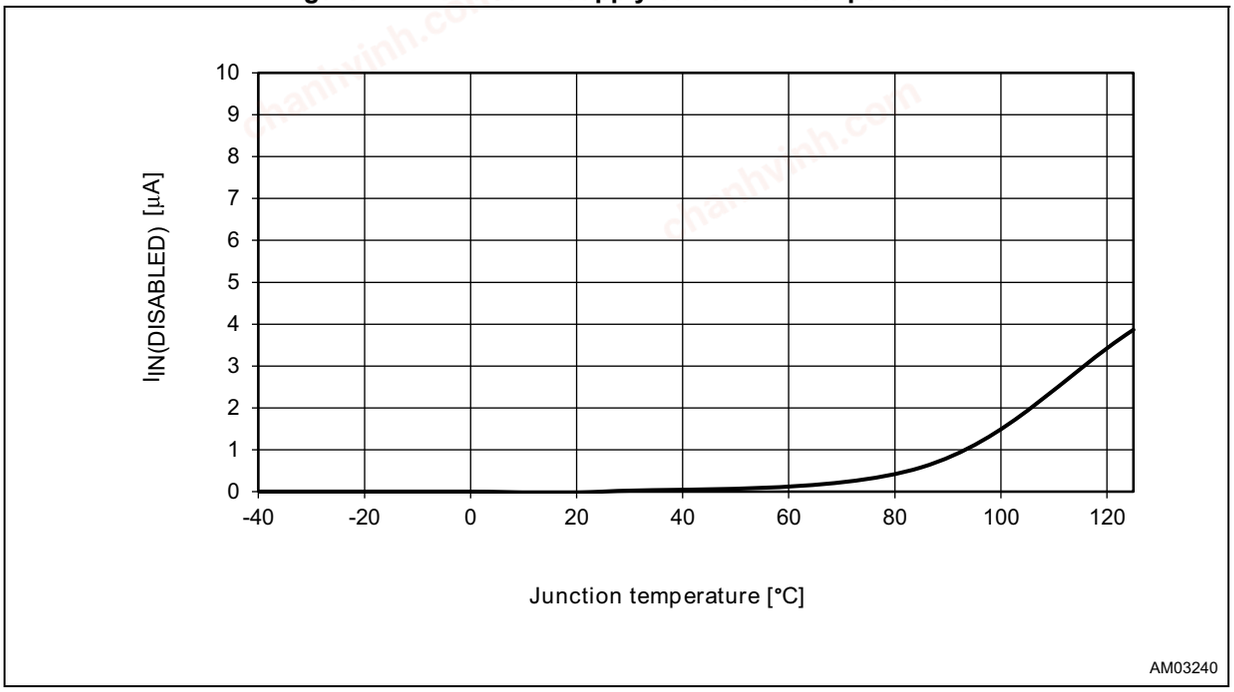


Figure 11. Disabled IN supply current vs. temperature



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Figure 12. Enabled IN supply current vs. temperature (SDP mode)

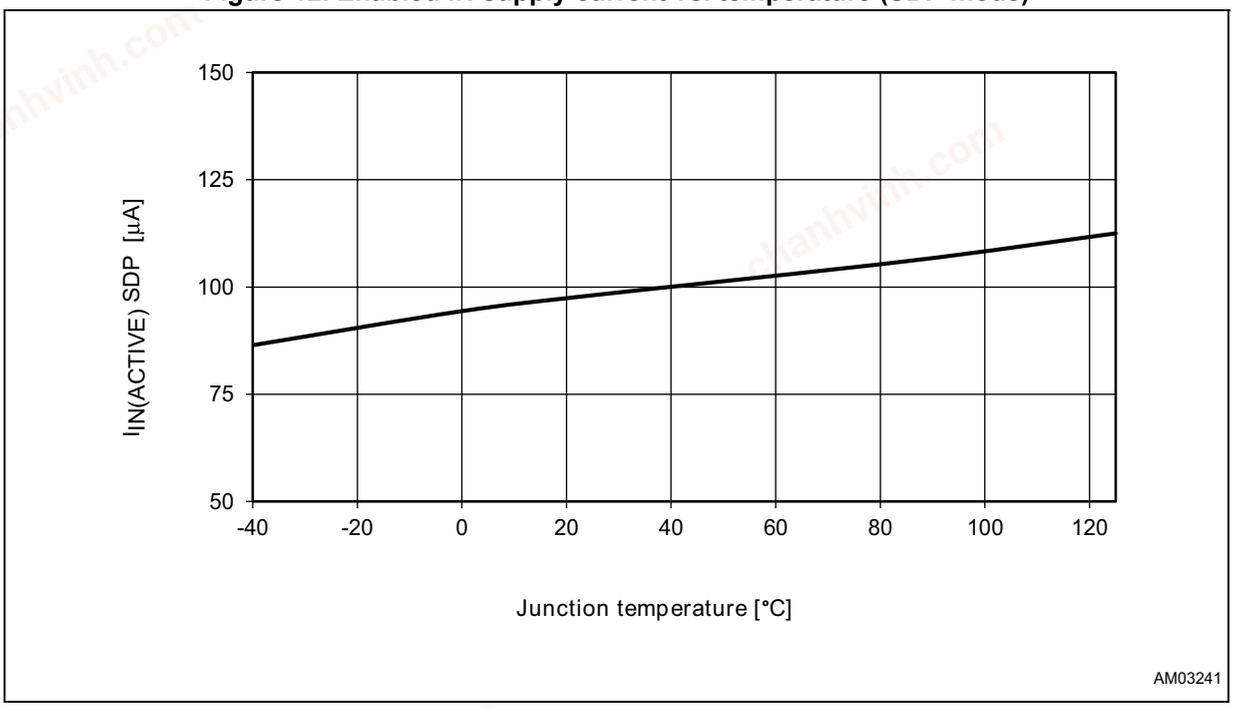
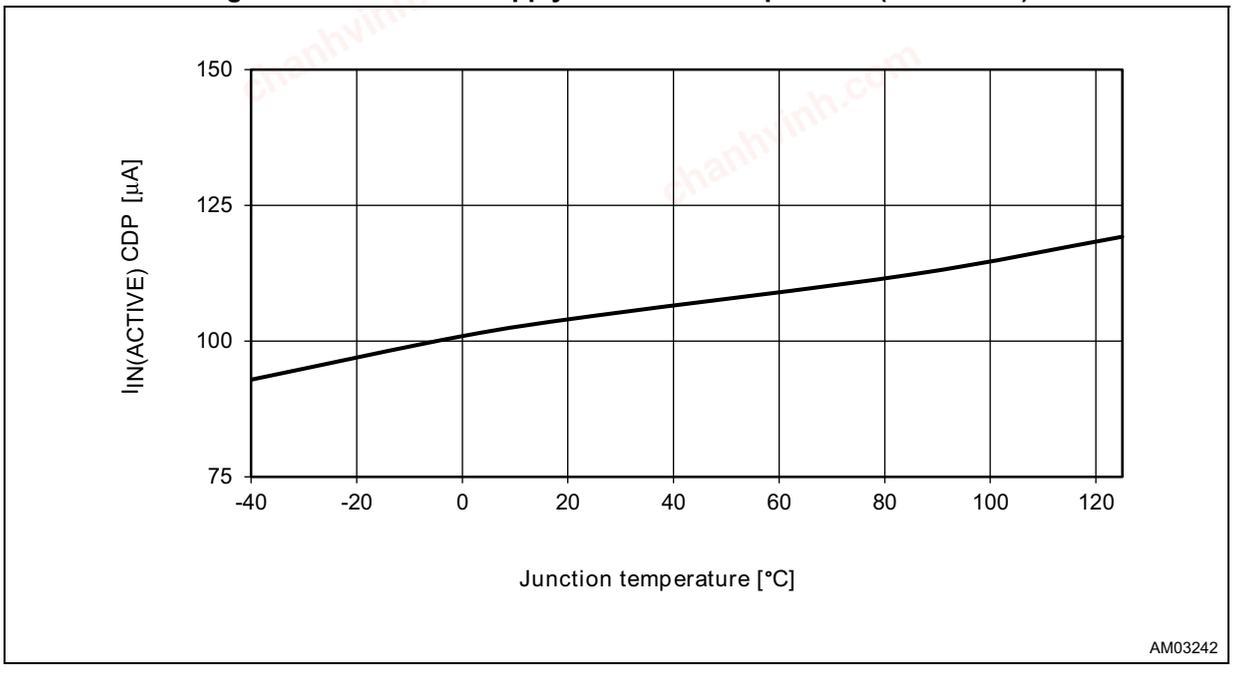


Figure 13. Enabled IN supply current vs. temperature (CDP mode)



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Figure 14. Enabled IN supply current vs. temperature (DCP auto-mode)

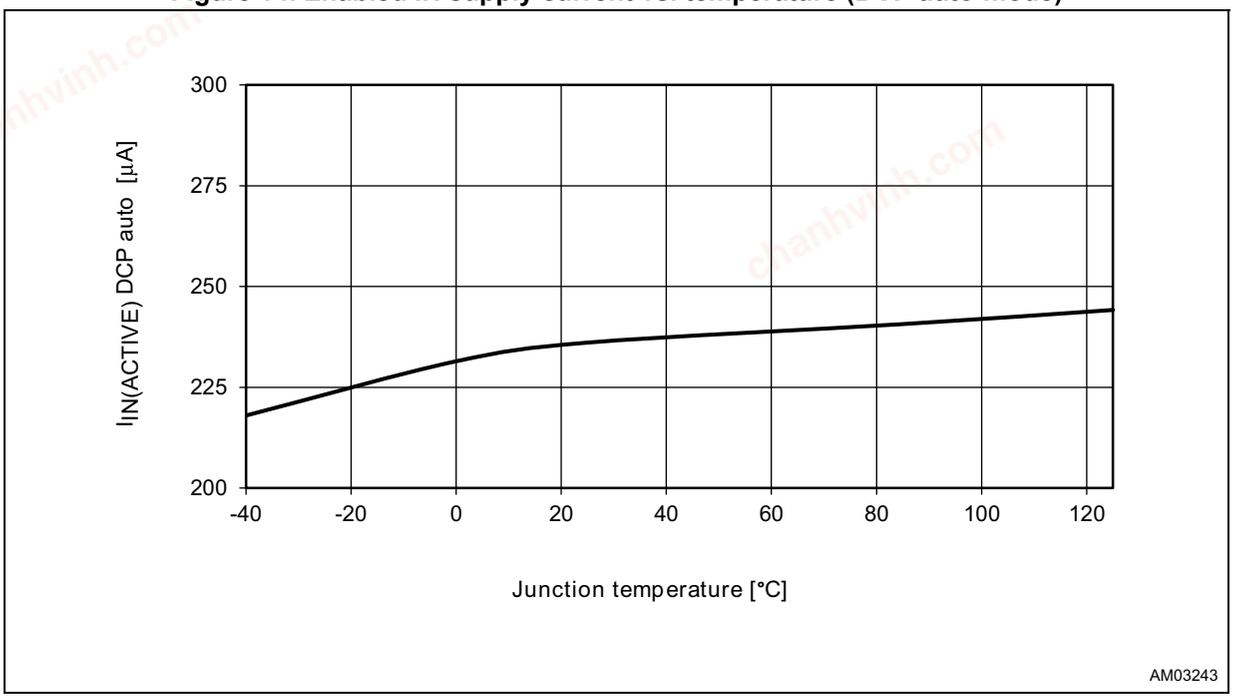
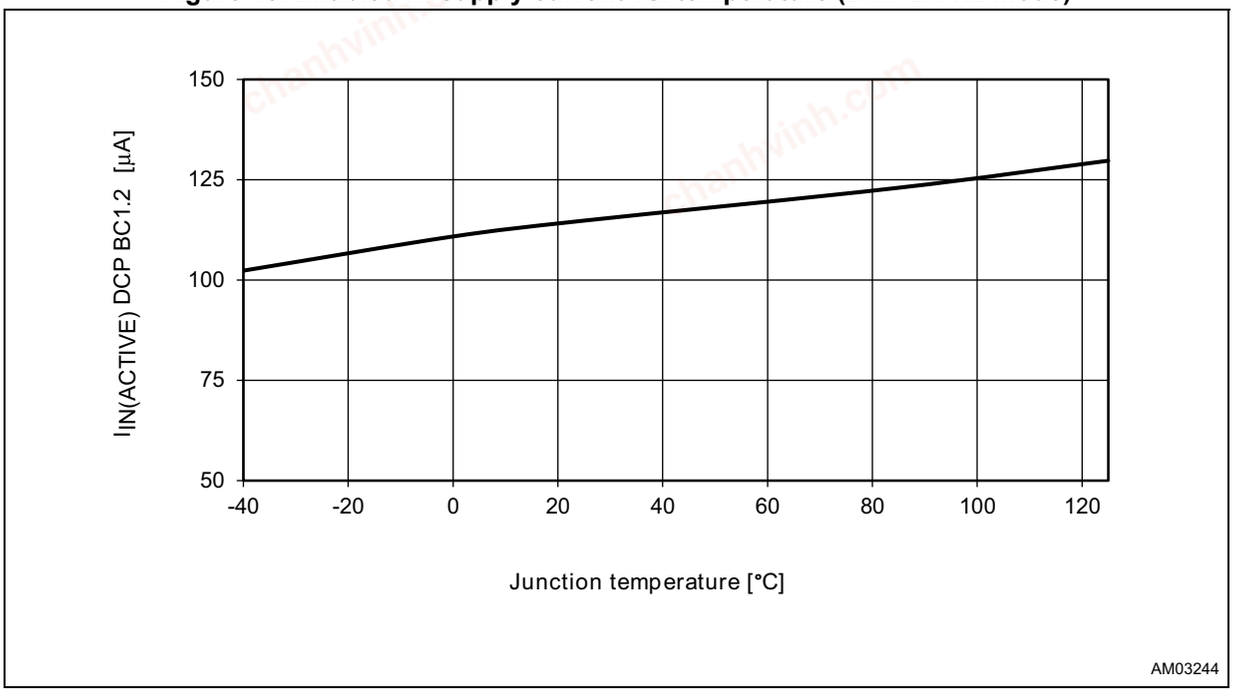


Figure 15. Enabled IN supply current vs. temperature (DCP BC1.2 mode)



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Figure 16. Enabled IN supply current vs. temperature (DCP divider mode)

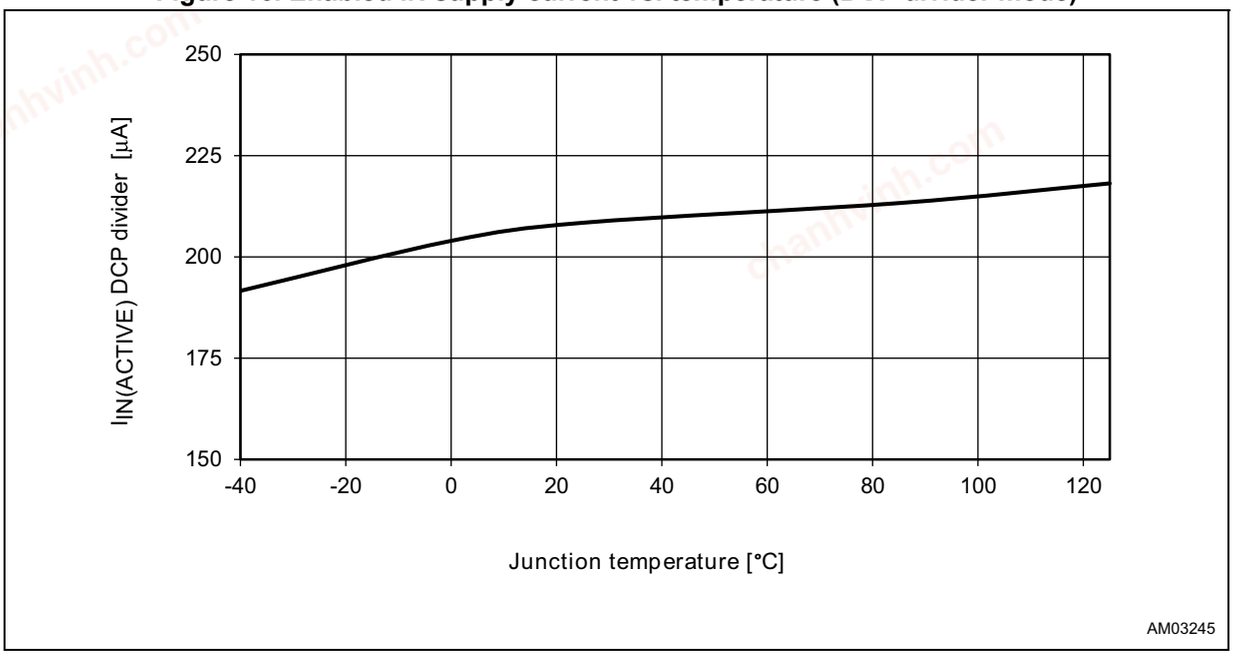
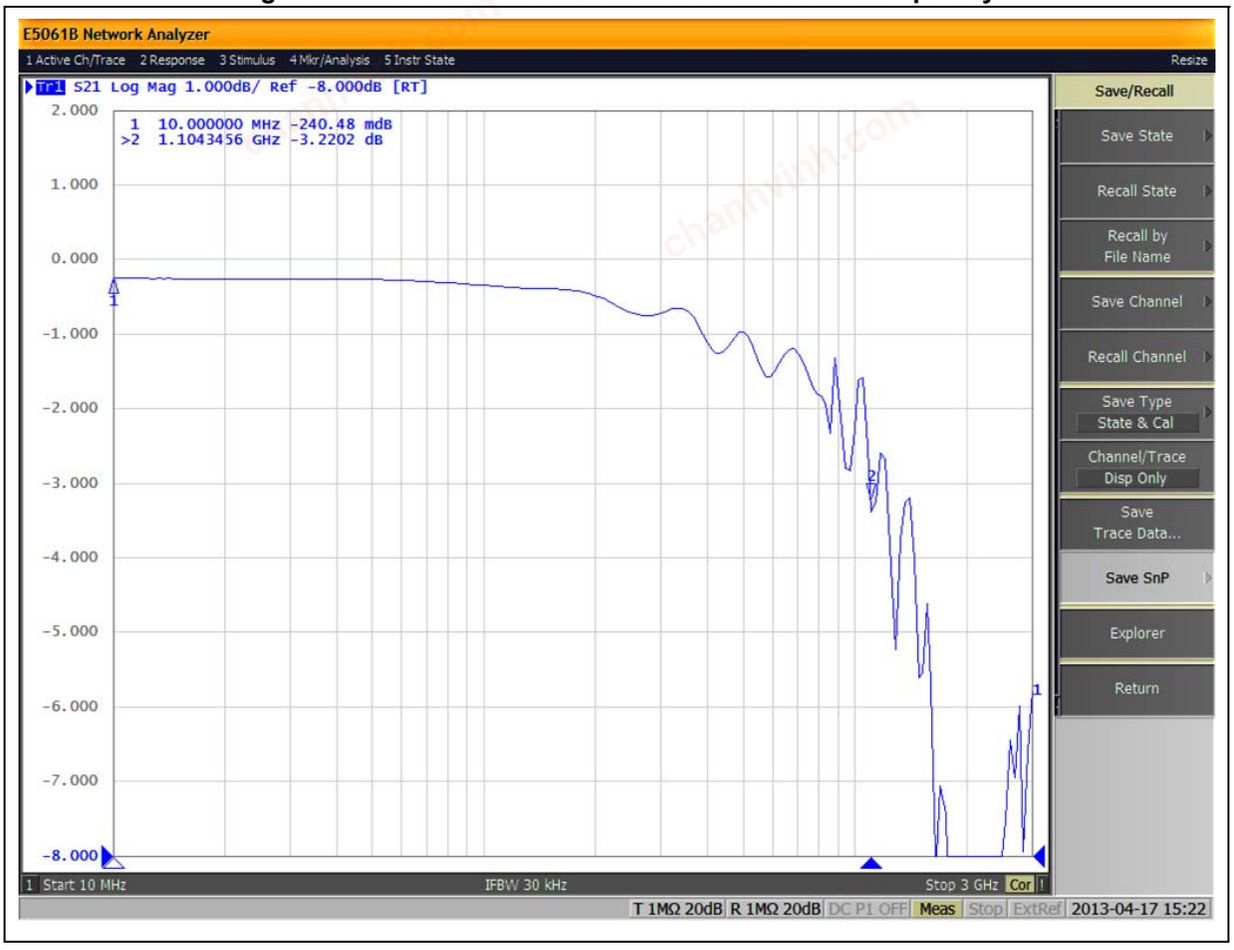


Figure 17. Data switch transfer characteristics vs. frequency



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Figure 18. Eye diagram using USB compliance test pattern - without STCC2540 (deskew line + cable)

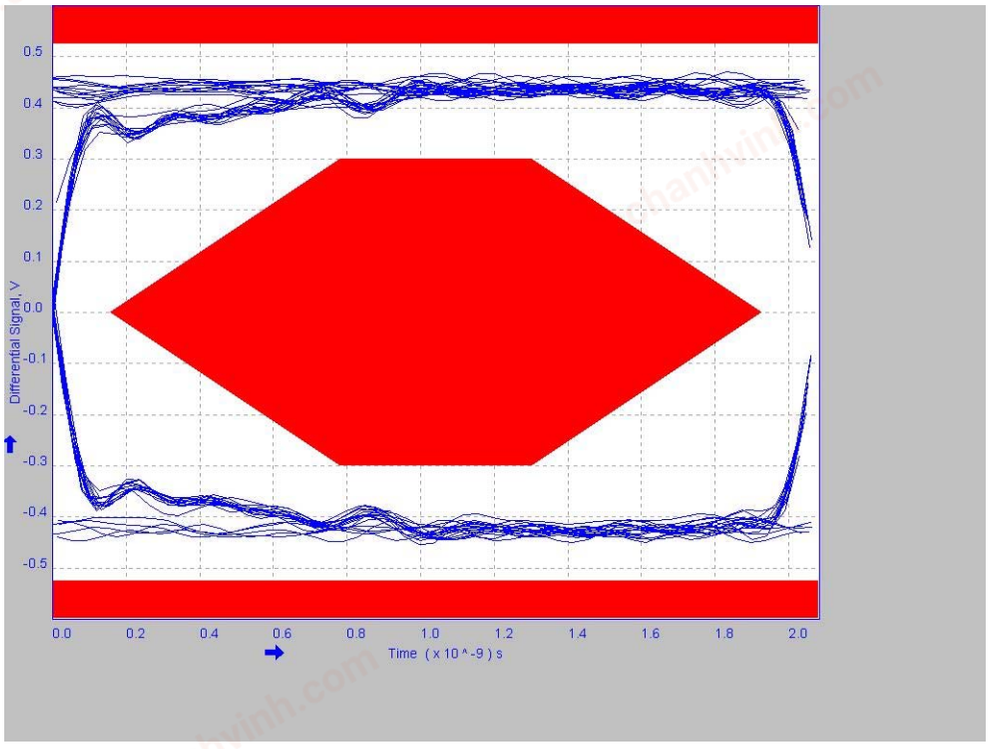
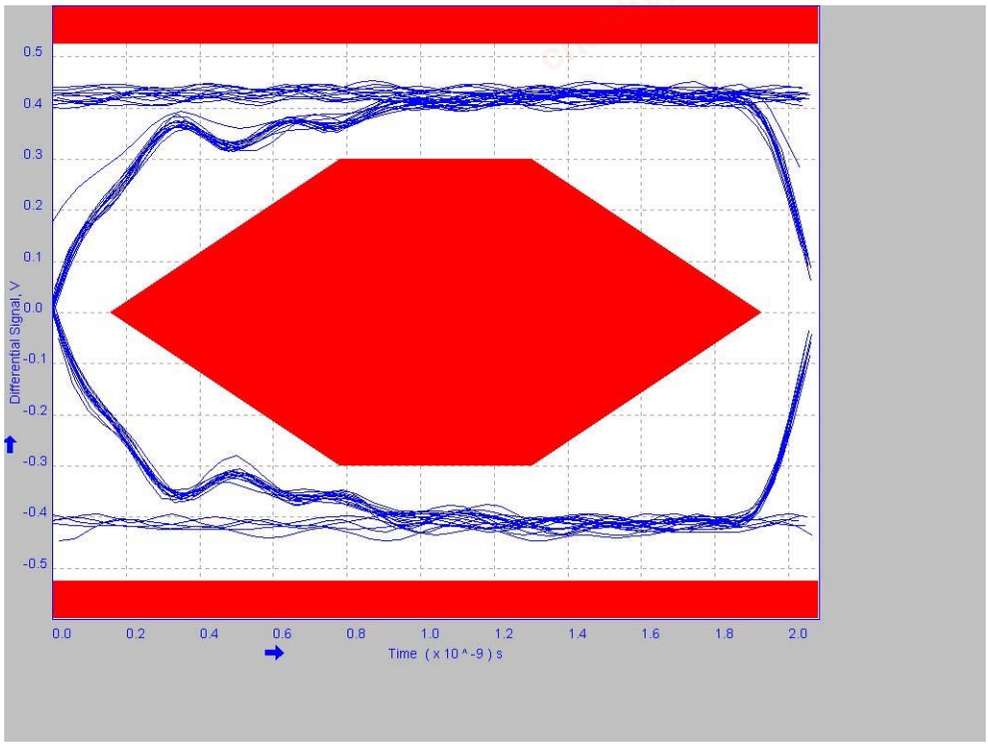


Figure 19. Eye diagram using USB compliance test pattern - with STCC2540 (STCC2540 + cable)



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Figure 20. Turn-on response (R_{ILIM} = 20 kΩ, R_{LOAD} = 5 Ω, C_{LOAD} = 150 µF)

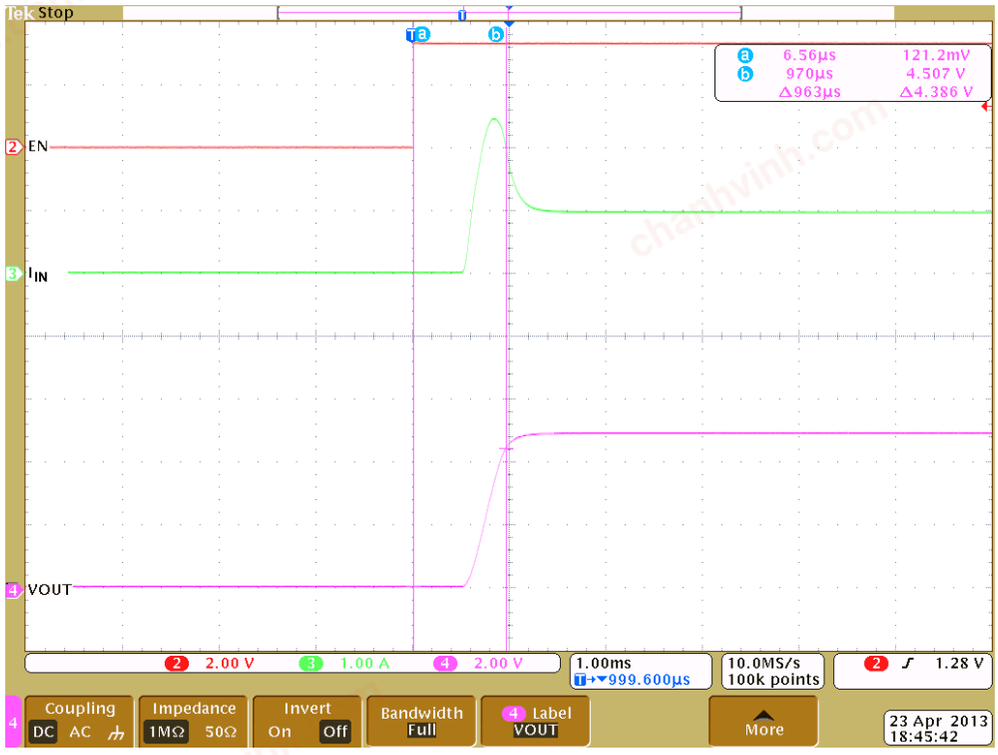
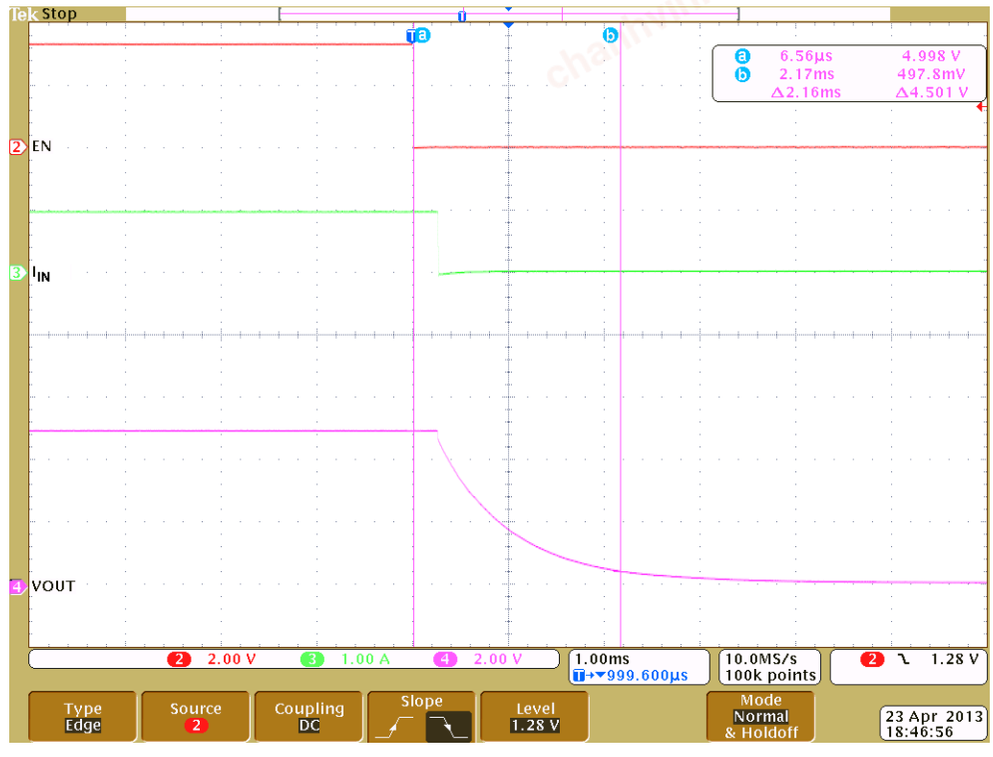


Figure 21. Turn-off response (R_{LOAD} = 5 Ω, C_{LOAD} = 150 µF)



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Figure 22. Device enabled into short-circuit (R_{ILIM} = 80.6 kΩ)

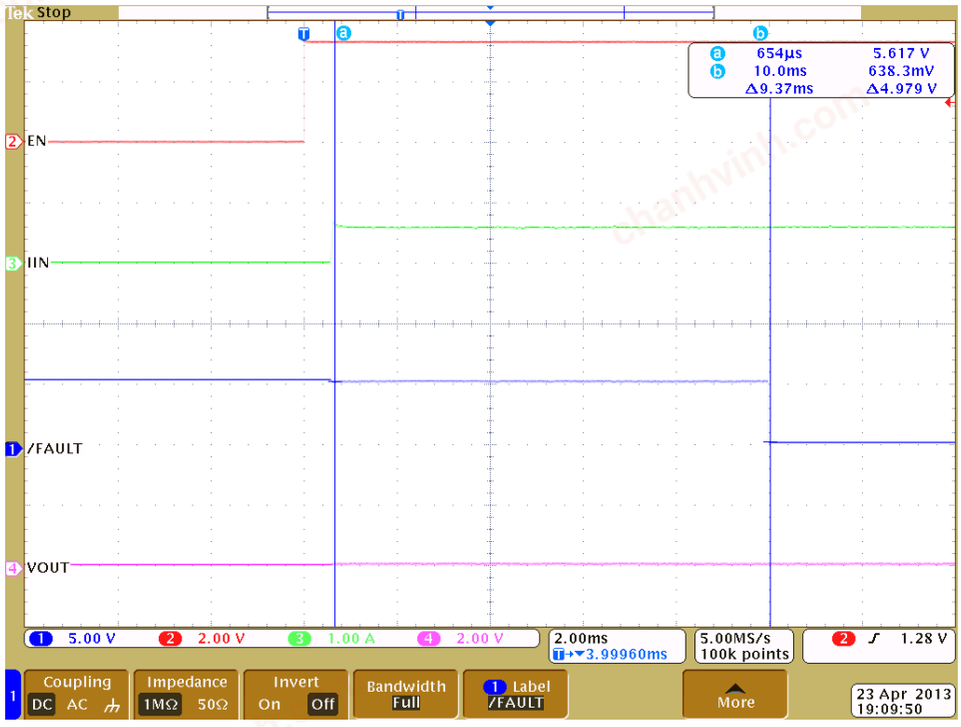
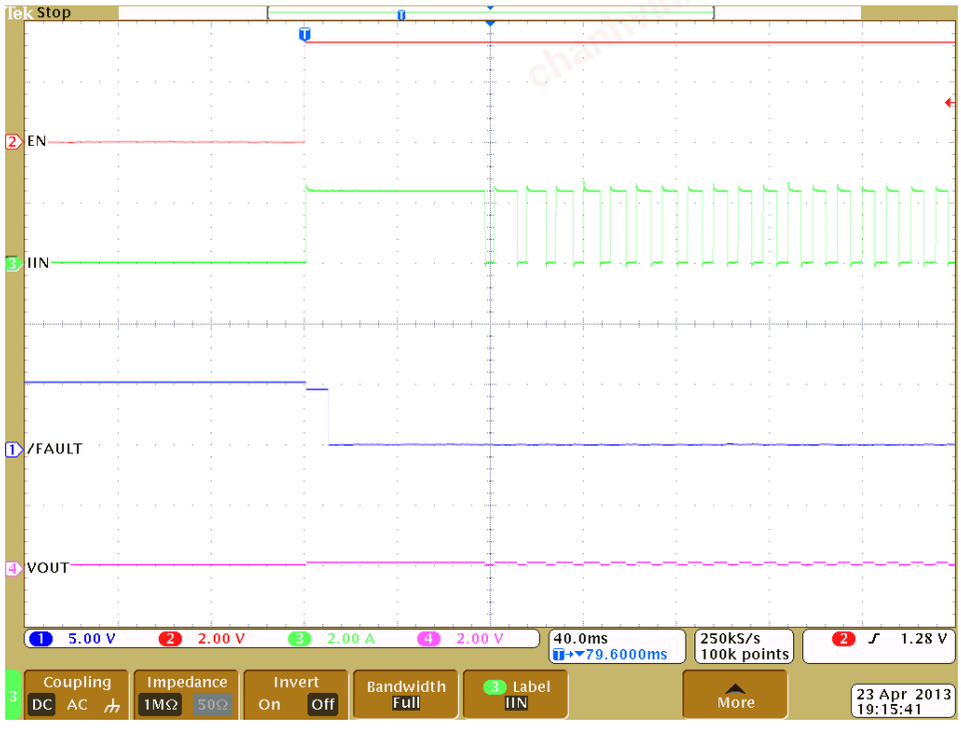
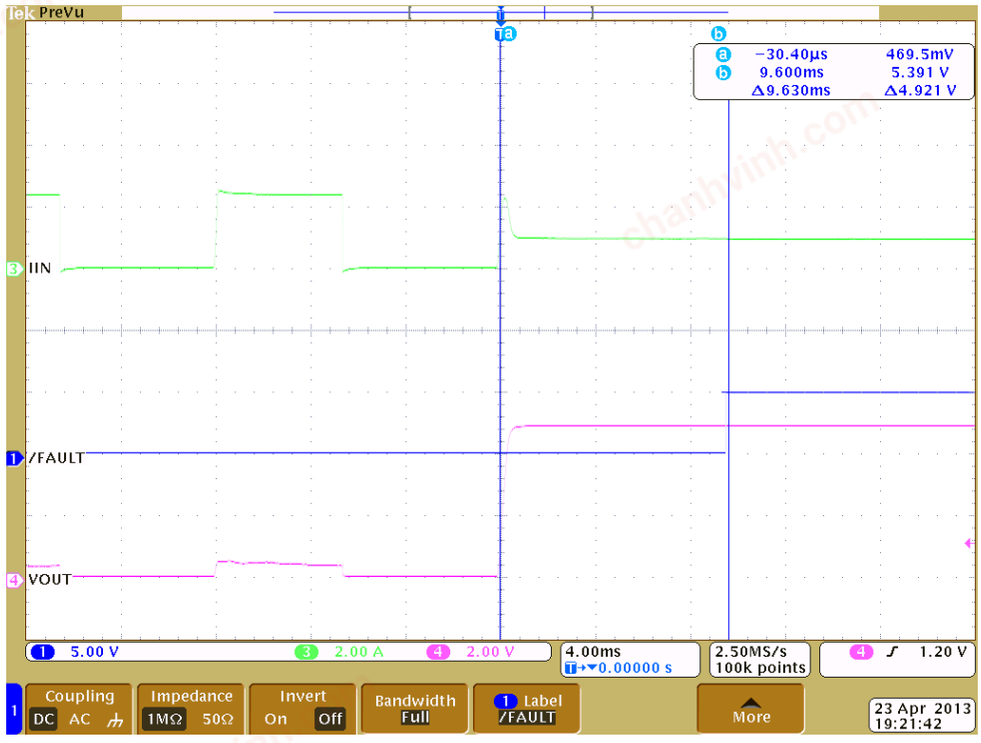


Figure 23. Device enabled into short-circuit - thermal cycling (R_{ILIM} = 20 kΩ)



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Figure 24. Short-circuit to full load recovery (R_{ILIM} = 20 kΩ, R_{LOAD} = 5 Ω, C_{LOAD} = 150 µF)

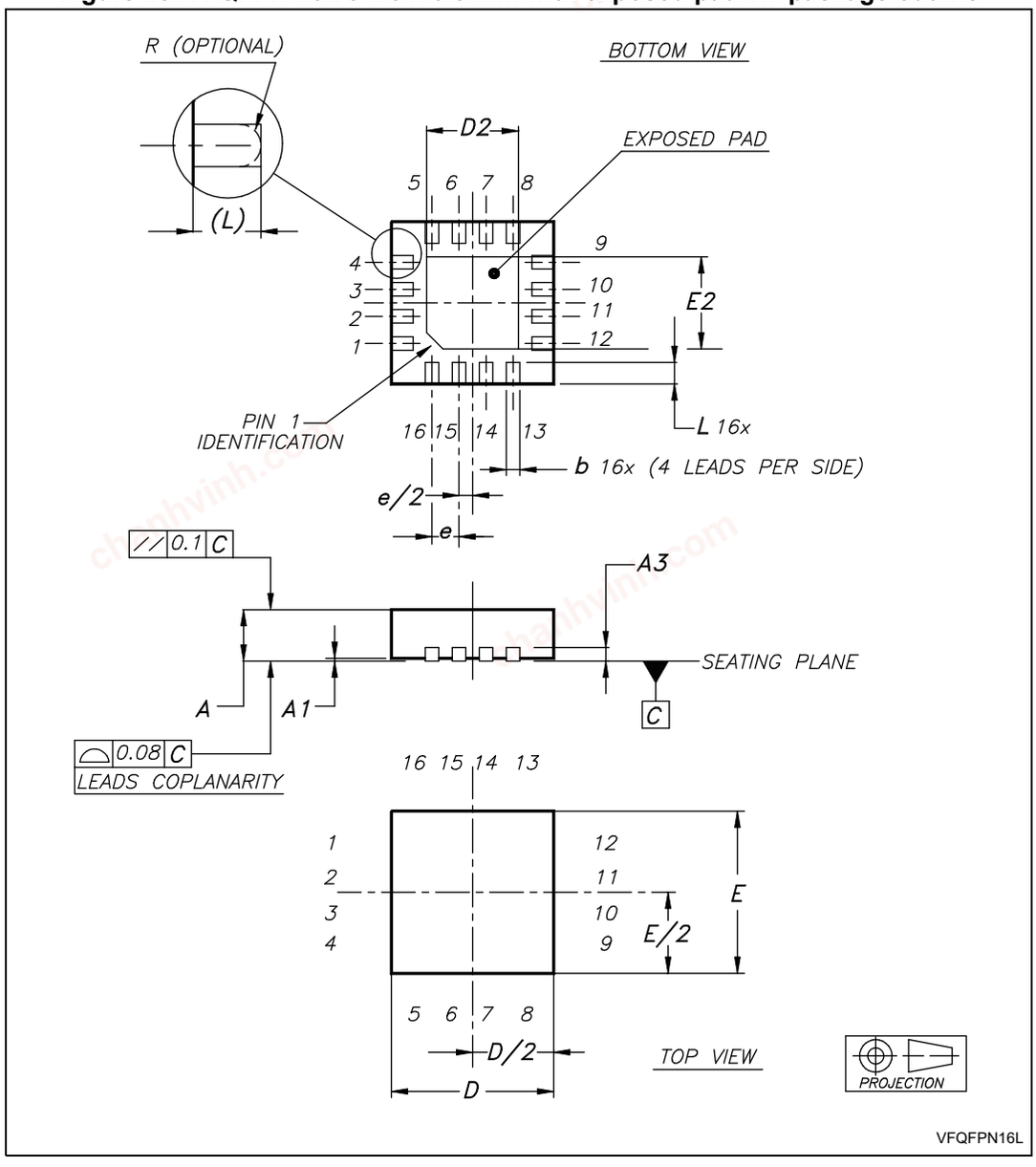


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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 25. VFQFPN 16L 3 x 3 x 0.8 mm with exposed pad 1.7 package outline



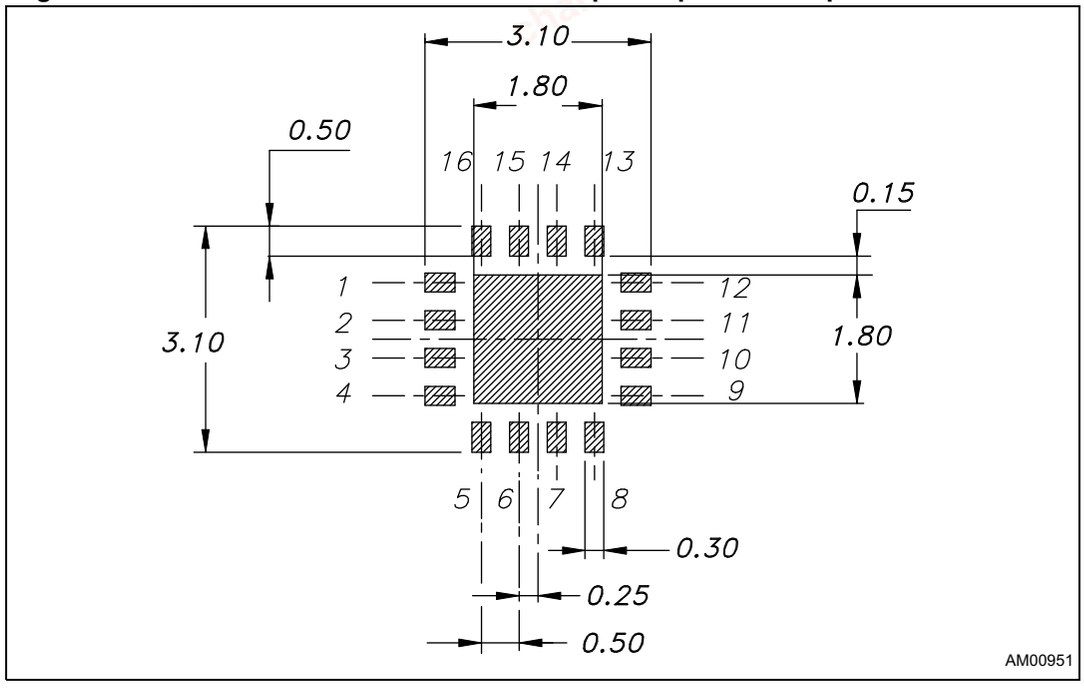
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Table 6. VFQFPN 16L 3 x 3 x 0.8 mm with exposed pad 1.7 package mechanical data(1), (2), (3), (4)

Symbol	Dimensions			Notes
	Data book (mm)			
	Nom.	Min.	Max.	
A	0.75	0.70	0.80	
A1	0.02	0	0.05	
A3	0.20			
b	0.25	0.18	0.30	
D	3	2.90	3.10	
D2	1.70	1.50	1.80	
E	3	2.90	3.10	
E2	1.70	1.50	1.80	
e	0.50			
L	0.40	0.30	0.50	(5)

1. VFQFPN - standard for “thermally enhanced very thin fine pitch quad flat package no leads”.
2. The lead size is comprehensive of the thickness of the lead finishing material.
3. Dimensions do not include mold protrusion, not to exceed 0.15 mm.
4. Package outline exclusive of metal burr dimensions.
5. The value of “L”, a JEDEC norm, is min. 0.35 – max. 0.45.

Figure 26. VFQFPN 16L 3 x 3 x 0.8 mm with exposed pad 1.7 footprint recommended



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8 Ordering information

Table 7. Order codes

Order code	Temperature range	Marking	Package	Packaging
STCC2540IQTR	-40 to 85 °C	2540CC	VFQFPN 16L	Tape and reel

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9 Revision history

Table 8. Document revision history

Date	Revision	Changes
29-May-2013	1	Initial release.
24-Jun-2013	2	Updated *Features on page 1* (added “CB” components). Updated *Section 1: Functional description* (replaced 1000 MHz by 1100 MHz). Updated *Table 2* (added note *3.*). Updated *Table 4* (updated parameters and conditions for $\lvert I_{REVERSE} \rvert$, IEN, IOL($\overline{FAULT}$), I_{CTLx}, IOL($\overline{CHARGING}$), added typ. value for X_{TALK}, $O_{IRR, and}$ B_{w}, removed t_{PD} and t_{SK} symbols). Added *Figure 4 on page 11*. Added *Note:* in *Section 5.1: Supported modes*. Added *Section 5.8: Input and output capacitors*. Added *Section 6: Typical operating characteristics*.
06-Dec-2013	3	Updated *Table 4* (updated min. conditions for I_{OS} - R_{ILIM} 96 kΩ and R_{ILIM} 33 kΩ). Updated *Table 5* (updated Host state column, added footnote *1.* and *2.*below table). Updated *Section 5.7* (replaced equation by *Equation 1* to *Equation 3*). Minor modifications throughout document.
06-Jan-2014	4	Corrected units in *Table 4 on page 7* (replaced “W” by “Ω “ in $R_{DISCHARGE}$, R_{ON} and R_{DCP_RES} symbols).
08-Jan-2014	5	Updated *Section : Features on page 1* (removed “2.5 A” from “Integrated V_{BUS} power switch with low R_{ON} of 65 mΩ“ replaced “2.5 A” by “2.8 A (max.)” in “Adjustable current limit”) . Added *List of figures on page 3*. Updated *Section 1: Functional description on page 3* [replaced “2.5 A” by “2.8 A (max.)”]. Updated *Table 4 on page 7* (added “R_{ILIM} = 17.2 kΩ“ and typ. conditions of “R_{ILIM} = 17.2 kΩ“ for I_{OS} symbol). Updated *Section : Current limit programming on page 16* [replaced “2.5 A (typ.)” by “2.8 A (max.)”].
25-Feb-2014	6	Removed *List of figures on page 3* *Section 5.6: Power switch*: updated *Equation 2* and *Equation 3* and added explanation of same. *Table 7: Order codes*: updated “marking” of STCC2540IQTR

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