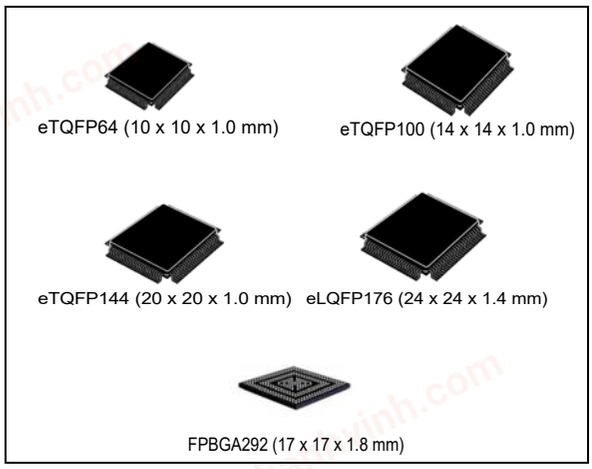
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SPC584Cx, SPC58ECx

SPC58 C Line - 32 bit Power Architecture automotive MCU Dual z4 cores 180 MHz, 4 MBytes Flash, HSM, ASIL-B

Datasheet - production data



Features

- AEC-Q100 qualified
- High performance e200z420n3 dual core
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 180 MHz
  - Variable Length Encoding (VLE)
- 4224 KB (4096 KB code flash + 128 KB data flash) on-chip flash memory: supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 176 KB HSM dedicated flash memory (144 KB code + 32 KB data)
- 384 KB on-chip general-purpose SRAM (in addition to 128 KB core local data RAM: 64 KB included in each CPU)
- Multi-channel direct memory access controller (eDMA) with 64 channels
- 1 interrupt controller (INTC)
- Comprehensive new generation ASIL-B safety concept
  - ASIL-B of ISO 26262
  - FCCU for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Cyclic redundancy check (CRC) unit
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Body cross triggering unit (BCTU)
  - Triggers ADC conversions from any eMIOS channel
  - Triggers ADC conversions from up to 2 dedicated PIT_RTIs
- Enhanced modular IO subsystem (eMIOS): up to 64 timed I/O channels with 16-bit counter resolution
- Enhanced analog-to-digital converter system with:
  - 3 independent fast 12-bit SAR analog converters
  - 1 supervisor 12-bit SAR analog converter
  - 1 10-bit SAR analog converter with STDBY mode support
- Communication interfaces
  - 18 LINFlexD modules
  - 8 deserial serial peripheral interface (DSPI) modules
  - 8 MCAN interfaces with advanced shared memory scheme and ISO CAN-FD support
  - Dual-channel FlexRay controller
  - 1 ethernet controller 10/100 Mbps, compliant IEEE 802.3-2008
- Low power capabilities
  - Versatile low power modes
  - Ultra low power standby with RTC
  - Smart Wake-up Unit for contact monitoring
  - Fast wakeup schemes
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell

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- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART
- Junction temperature range -40 °C to 150 °C

Table 1. Device summary

Package	Part number					
	2 MB		3 MB		4 MB	
	Single core	Dual core	Single core	Dual core	Single core	Dual core
eTQFP64	SPC584C70E1	SPC58EC70E1	SPC584C74E1	SPC58EC74E1	SPC584C80E1	SPC58EC80E1
eTQFP100	SPC584C70E3	SPC58EC70E3	SPC584C74E3	SPC58EC74E3	SPC584C80E3	SPC58EC80E3
eTQFP144	SPC584C70E5	SPC58EC70E5	SPC584C74E5	SPC58EC74E5	SPC584C80E5	SPC58EC80E5
eLQFP176	SPC584C70E7	SPC58EC70E7	SPC584C74E7	SPC58EC74E7	SPC584C80E7	SPC58EC80E7
FPBGA292	SPC584C70C3	SPC58EC70C3	SPC584C74C3	SPC58EC74C3	SPC584C80C3	SPC58EC80C3

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1 Introduction

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

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2 Description

The SPC584Cx and SPC58ECx microcontroller is the first in a new family of devices superseding the SPC564Cx and SPC56ECx family. SPC584Cx and SPC58ECx builds on the legacy of the SPC564Cx and SPC56ECx family, while introducing new features coupled with higher throughput to provide substantial reduction of cost per feature and significant power and performance improvement (MIPS per mW). On the SPC584Cx and SPC58ECx device, there are two processor cores e200z420 and one e200z0 core embedded in the Hardware Security Module.

2.1 Device feature summary

Table 2 lists a summary of major features for the SPC584Cx and SPC58ECx device. The feature column represents a combination of module names and capabilities of certain modules. A detailed description of the functionality provided by each on-chip module is given later in this document.

Table 2. Features List

Feature	Description
SPC58 family	40 nm
Number of Cores	2
Local RAM	2x 64 KB Data
Single Precision Floating Point	Yes
SIMD	No
VLE	Yes
Cache	8 KB Instruction
	4 KB Data
MPU	Core MPU: 24 per CPU
	System MPU: 24 per XBAR
Semaphores	Yes
CRC Channels	2 x 4
Software Watchdog Timer (SWT)	3
Core Nexus Class	3+
Event Processor	4 x SCU
	4 x PMC
Run control Module	Yes
System SRAM	384 KB (including 256 KB of standby RAM)
Flash	4096 KB code / 128 KB data
Flash fetch accelerator	2 x 4 x 256-bit
DMA channels	64

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Table 2. Features List (continued)

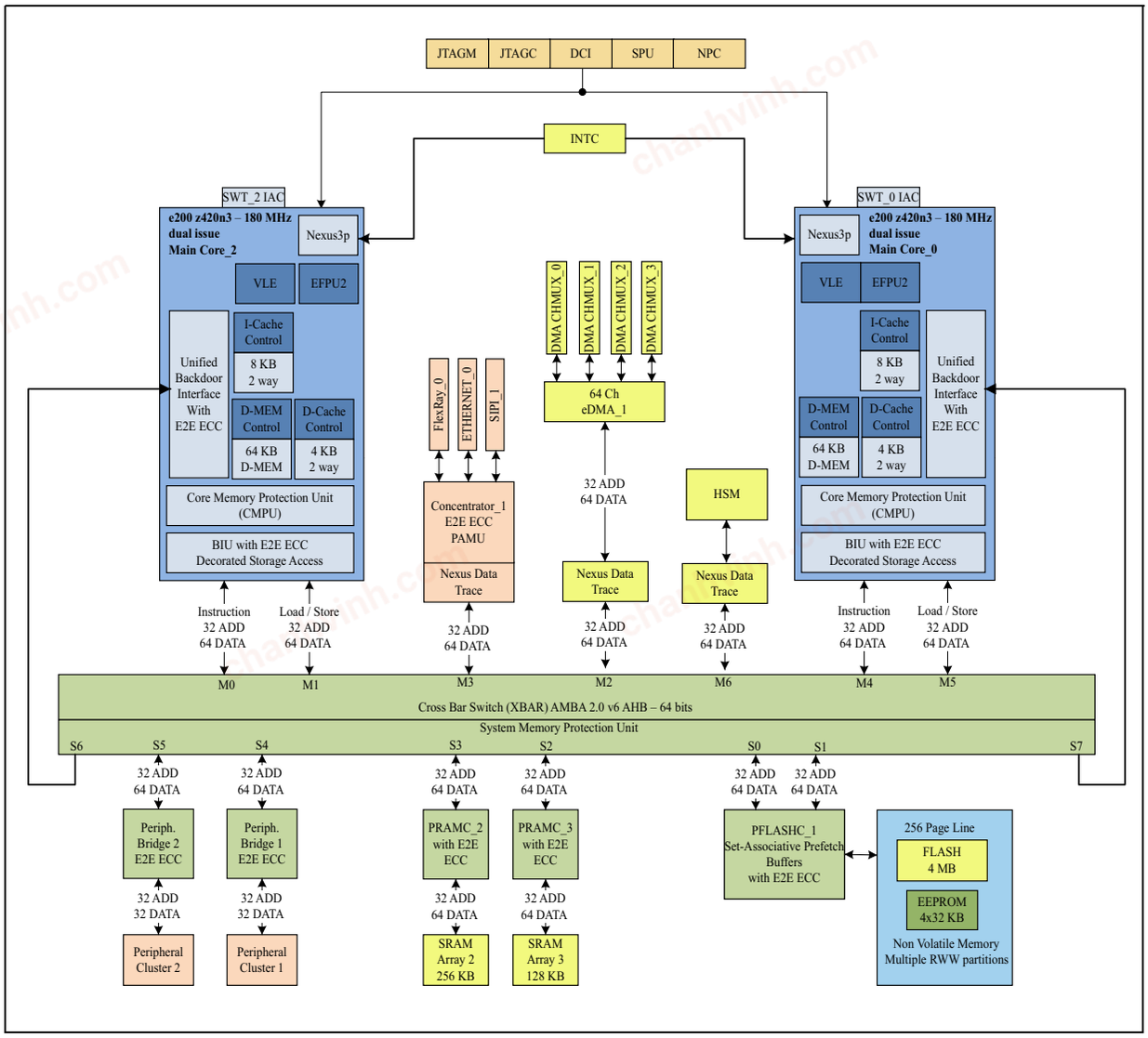
Feature	Description
DMA Nexus Class	3
LINFlexD	18
MCAN (ISO CAN-FD compliant)	8
DSPI	8
I2C	1
FlexRay	1 x Dual channel
Ethernet	1 MAC with Time Stamping, AVB and VLAN support
SIPI / LFAST Debugger	High Speed
System Timers	8 PIT channels
	4 AUTOSAR® (STM)
	RTC/API
eMIOS	2 x 32 channels
BCTU	64 channels
Interrupt controller	1 x 568 sources
ADC (SAR)	5
Temp. sensor	Yes
Self Test Controller	Yes
PLL	Dual PLL with FM
Integrated linear voltage regulator	Yes
External Power Supplies	5 V, 3.3 V
Low Power Modes	HALT Mode
	STOP Mode
	Smart Standby with output controller, analog and digital inputs
	Standby Mode

2.2 Block diagram

The figures below show the top-level block diagrams.

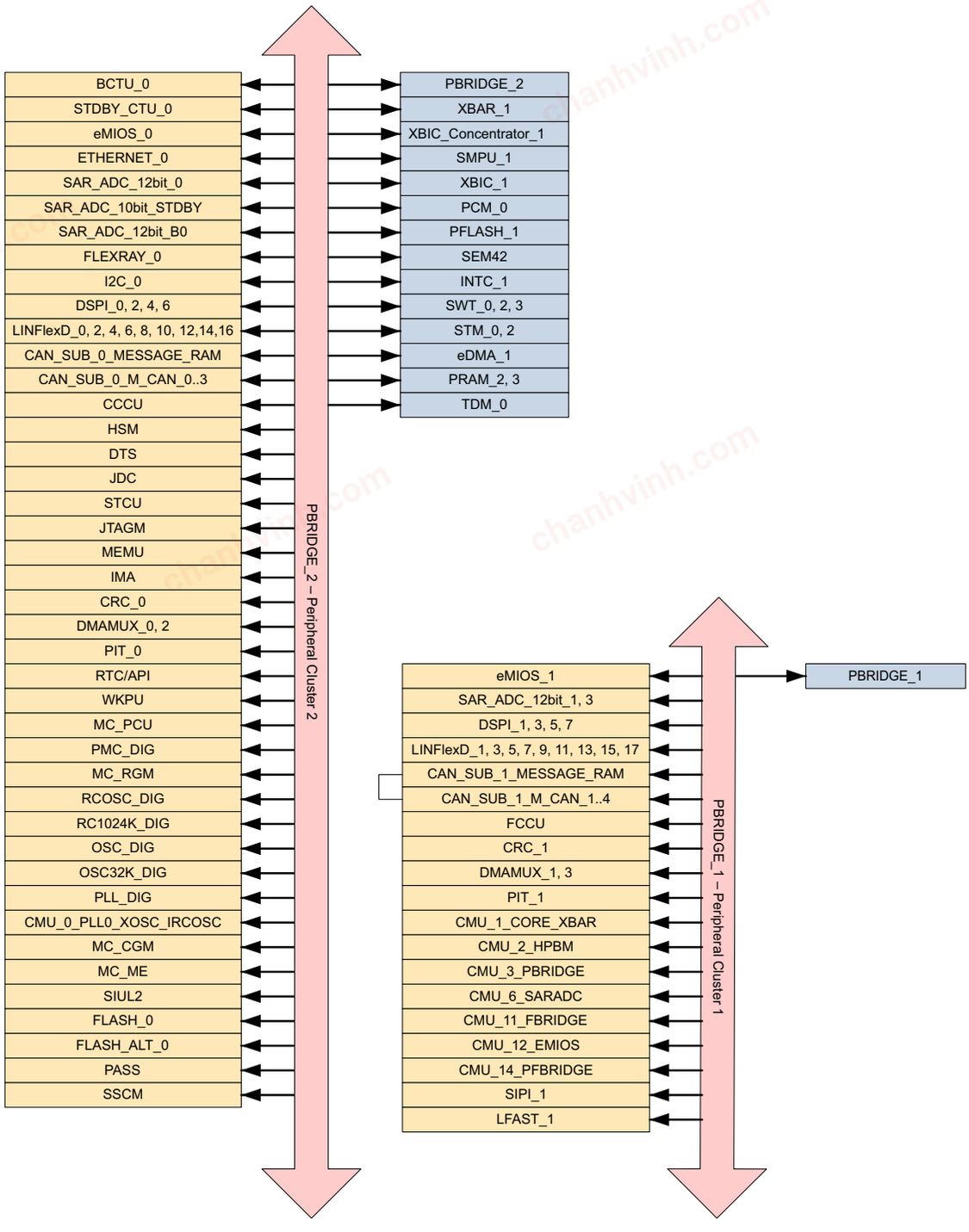
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Figure 1. Block diagram



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Figure 2. Periphery allocation



Note: In this diagram, ON-platform modules are shown in orange color and OFF-platform modules are shown in blue color.

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2.3 Features overview

On-chip modules within SPC584Cx and SPC58ECx include the following features:

- Two main CPUs, dual issue, 32-bit CPU core complexes (e200z4).
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - 64 KB local data RAM for Core_0 and Core_2
  - 8 KB I-Cache and 4 KB D-Cache for Core_0 and Core_2
- 4224 KB (4096 KB code flash + 128 KB data flash) on-chip flash memory
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 176 KB HSM dedicated flash memory (144 KB code + 32 KB data)
- 384 KB on-chip general-purpose SRAM (+ 128 KB local data RAM: 64 KB included in each CPU)
- Multi channel direct memory access controllers
  - 64 eDMA channels
- One interrupt controller (INTC)
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Hardware security module (HSM) with HW cryptographic co-processor
- System integration unit lite (SIUL)
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART.
- Hardware support for safety ASIL-B level related applications
- Enhanced modular IO subsystem (eMIOS): up to 64 (2 x 32) timed I/O channels with 16-bit counter resolution
  - Buffered updates
  - Support for shifted PWM outputs to minimize occurrence of concurrent edges
  - Supports configurable trigger outputs for ADC conversion for synchronization to channel output waveforms
  - Shared or independent time bases
  - DMA transfer support available
- Body cross triggering unit (BCTU)
  - Triggers ADC conversions from any eMIOS channel
  - Triggers ADC conversions from up to 2 dedicated PIT_RTIs
  - One event configuration register dedicated to each timer event allows to define the corresponding ADC channel
  - Synchronization with ADC to avoid collision
- Enhanced analog-to-digital converter system with:
  - Three independent fast 12-bit SAR analog converters

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  - One supervisor 12-bit SAR analog converter
  - One 10-bit SAR analog converter with STDBY mode support
- Eight deserial serial peripheral interface (DSPI) modules
- Eighteen LIN and UART communication interface (LINFlexD) modules
  - LINFlexD_0 is a Master/Slave
  - All others are Masters
- Eight modular controller area network (MCAN) modules, all supporting flexible data rate (ISO CAN-FD compliant)
- Dual-channel FlexRay controller
- One ethernet controller 10/100 Mbps, compliant IEEE 802.3-2008
  - IEEE 1588-2008 Time stamping (internal 64-bit time stamp)
  - IEEE 802.1AS and IEEE 802.1Qav (AVB-Feature)
  - IEEE 802.1Q VLAN tag detection
  - IPv4 and IPv6 checksum modules
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard.
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1 and IEEE 1149.7), 2-pin JTAG interface.
- Standby power domain with smart wake-up sequence

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3 Package pinouts and signal descriptions

Refer to the SPC584Cx and SPC58ECx IO_ Definition document.

It includes the following sections:

1. Package pinouts
2. Pin descriptions
   a) Power supply and reference voltage pins
   b) System pins
   c) LVDS pins
   d) Generic pins

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4 Electrical characteristics

4.1 Introduction

The present document contains the target Electrical Specification for the 40 nm family 32-bit MCU SPC584Cx and SPC58ECx products.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

The electrical parameters shown in this document are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 3* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 3. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design validation on a small sample size from typical devices.
D	Those parameters are derived mainly from simulations.

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4.2 Absolute maximum ratings

Table 4 describes the maximum ratings for the device. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Stress beyond the listed maxima, even momentarily, may affect device reliability or cause permanent damage to the device.

Table 4. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{DD_LV}	SR	D	Core voltage operating life range(1)	—	–0.3	—	1.4	V
$V_{DD_HV_IO_MAIN}$ $V_{DD_HV_IO_FLEX}$ $V_{DD_HV_OSC}$ $V_{DD_HV_FLA}$	SR	D	I/O supply voltage(2)	—	–0.3	—	6.0	V
$V_{SS_HV_ADV}$	SR	D	ADC ground voltage	Reference to digital ground	–0.3	—	0.3	V
$V_{DD_HV_ADV}$	SR	D	ADC Supply voltage(2)	Reference to $V_{SS_HV_ADV}$	–0.3	—	6.0	V
$V_{SS_HV_ADR_S}$	SR	D	SAR ADC ground reference	—	–0.3	—	0.3	V
$V_{DD_HV_ADR_S}$	SR	D	SAR ADC voltage reference(2)	Reference to $V_{SS_HV_ADR_S}$	–0.3	—	6.0	V
V_{SS}-$V_{SS_HV_ADR_S}$	SR	D	$V_{SS_HV_ADR_S}$ differential voltage	—	–0.3	—	0.3	V
V_{SS}-$V_{SS_HV_ADV}$	SR	D	$V_{SS_HV_ADV}$ differential voltage	—	–0.3	—	0.3	V
V_{IN}	SR	D	I/O input voltage range(2)(3) (4)	—	–0.3	—	6.0	V
				Relative to V_{ss}	–0.3	—	—	
				Relative to $V_{DD_HV_IO}$ and $V_{DD_HV_ADV}$	—	—	0.3	
T_{TRIN}	SR	D	Digital Input pad transition time(5)	—	—	—	1	ms
I_{INJ}	SR	T	Maximum DC injection current for each analog/digital PAD(6)	—	–5	—	5	mA

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Table 4. Absolute maximum ratings (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_{STG}	SR	T	Maximum non-operating Storage temperature range	—	–55	—	125	°C
T_{PAS}	SR	C	Maximum non-operating temperature during passive lifetime	—	–55	—	150(7)	°C
$T_{STORAGE}$	SR	—	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	—	20	years
T_{SDR}	SR	T	Maximum solder temperature Pb-free packaged(8)	—	—	—	260	°C
MSL	SR	T	Moisture sensitivity level(9)	—	—	—	3	—
T_{XRAY} dose	SR	T	Maximum cumulated XRAY dose	Typical range for X-rays source during inspection:80 ÷ 130 KV; 20 ÷ 50 µA	—	—	1	grey

1. V_{DD_LV}: allowed 1.335 V - 1.400 V for 60 seconds cumulative time at the given temperature profile. Remaining time allowed 1.260 V - 1.335 V for 10 hours cumulative time at the given temperature profile. Remaining time as defined in *Section 4.3: Operating conditions*.
2. V_{DD_HV}: allowed 5.5 V – 6.0 V for 60 seconds cumulative time at the given temperature profile, for 10 hours cumulative time with the device in reset at the given temperature profile. Remaining time as defined in *Section 4.3: Operating conditions*.
3. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3 V can be used for nominal calculations.
4. Relative value can be exceeded if design measures are taken to ensure injection current limitation (parameter IINJ).
5. This limitation applies to pads with digital input buffer enabled. If the digital input buffer is disabled, there are no maximum limits to the transition time.
6. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 4.8.3: I/O pad current specifications*.
7. 175°C are allowed for limited time. Mission profile with passive lifetime temperature >150°C have to be evaluated by ST to confirm that are granted by product qualification.
8. Solder profile per IPC/JEDEC J-STD-020D.
9. Moisture sensitivity per JDEC test method A112.

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4.3 Operating conditions

Table 5 describes the operating conditions for the device, and for which all the specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

Table 5. Operating conditions

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
F_{SYS}(2)	SR	P	Operating system clock frequency(3)	—	—	—	180	MHz
$T_{A_125\ Grade}$(4)	SR	D	Operating Ambient temperature	—	–40	—	125	°C
$T_{J_125\ Grade}$(4)	SR	P	Junction temperature under bias	T_A = 125 °C	–40	—	150	°C
$T_{A_105\ Grade}$(4)	SR	D	Ambient temperature under bias	—	–40	—	105	°C
$T_{J_105\ Grade}$(4)	SR	D	Operating Junction temperature	T_A = 105 °C	–40	—	130	°C
V_{DD_LV}	SR	P	Core supply voltage(5)	—	1.14	1.20	1.26(6) (7)	V
$V_{DD_HV_IO_MAIN}$ $V_{DD_HV_IO_FLEX}$ $V_{DD_HV_FLA}$ $V_{DD_HV_OSC}$	SR	P	IO supply voltage	—	3.0	—	5.5	V
$V_{DD_HV_ADV}$	SR	P	ADC supply voltage	—	3.0	—	5.5	V
$V_{SS_HV_ADV}$- V_{SS}	SR	D	ADC ground differential voltage	—	–25	—	25	mV
$V_{DD_HV_ADR_S}$	SR	P	SAR ADC reference voltage	—	3.0	—	5.5	V
$V_{DD_HV_ADR_S}$- $V_{DD_HV_ADV}$	SR	D	SAR ADC reference differential voltage	—	—	—	25	mV
$V_{SS_HV_ADR_S}$	SR	P	SAR ADC ground reference voltage	—	$V_{SS_HV_ADV}$			V

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Table 5. Operating conditions (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
$V_{SS_HV_ADR_S}$- $V_{SS_HV_ADV}$	SR	D	$V_{SS_HV_ADR_S}$ differential voltage	—	–25	—	25	mV
V_{RAMP_HV}	SR	D	Slew rate on HV power supply	—	—	—	100	V/ms
V_{IN}	SR	P	I/O input voltage range	—	0	—	5.5	V
I_{INJ1}	SR	T	Injection current (per pin) without performance degradation(8) (9) (10)	Digital pins and analog pins	–3.0	—	3.0	mA
I_{INJ2}	SR	D	Dynamic Injection current (per pin) with performance degradation(10) (11)	Digital pins and analog pins	–10	—	10	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The maximum number of PRAM wait states has to be configured accordingly to the system clock frequency. Refer to *Table 6*.
3. Maximum operating frequency is applicable to the cores and platform of the device. See the Clock Chapter in the Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
4. In order to evaluate the actual difference between ambient and junction temperatures in the application, refer to *Section 5.6: Package thermal characteristics*.
5. Core voltage as measured on device pin to guarantee published silicon performance.
6. Core voltage can exceed 1.26 V with the limitations provided in *Section 4.2: Absolute maximum ratings*, provided that HVD134_C monitor reset is disabled.
7. 1.260 V - 1.290 V range allowed periodically for supply with sinusoidal shape and average supply value below or equal to 1.236 V at the given temperature profile.
8. Full device lifetime. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Section 4.2: Absolute maximum ratings* for maximum input current for reliability requirements.
9. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current will be injected through the clamp diode to the supply rails. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
10. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 4.8.3: I/O pad current specifications*.
11. Positive and negative Dynamic current injection pulses are allowed up to this limit. I/O and ADC specifications are not granted. See the dedicated chapters for the different specification limits. See the Absolute Maximum Ratings table for maximum input current for reliability requirements. Refer to the following pulses definitions: Pulse1 (ISO 7637-2:2011), Pulse 2a(ISO 7637-2:2011 5.6.2), Pulse 3a (ISO 7637-2:2011 5.6.3), Pulse 3b (ISO 7637-2:2011 5.6.3).

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Table 6. PRAM wait states configuration

PRAMC WS	Clock Frequency (MHz)
1	≤ 180
0	≤ 120

4.3.1 Power domains and power up/down sequencing

The following table shows the constraints and relationships for the different power domains. Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting ‘ok’. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Table 7. Device supply relation during power-up/power-down sequence

		Supply2				
		V_{DD_LV}	$V_{DD_HV_IO_FLEX}$	$V_{DD_HV_IO_MAIN}$ $V_{DD_HV_FLA}$ $V_{DD_HV_OSC}$	$V_{DD_HV_ADV}$	$V_{DD_HV_ADR}$
Supply1	$V_{DD_HV_IO_FLEX}$	ok		not allowed	ok	ok
	$V_{DD_HV_IO_MAIN}$ $V_{DD_HV_FLA}$ $V_{DD_HV_OSC}$	ok	ok		ok	ok
	$V_{DD_HV_ADV}$	ok	ok	not allowed		ok
	$V_{DD_HV_ADR}$	ok	ok	not allowed	not allowed	

During power-up, all functional terminals are maintained in a known state as described in the device pinout Microsoft Excel file attached to the IO_Definition document.

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4.4 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device:

- All ESD testing are in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits,
- Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which include the complete DC parametric and functional testing at room temperature and hot temperature, maximum DC parametric variation within 10% of maximum specification”.

Table 8. ESD ratings

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(1)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(2)	T	All pins	500	V
	T	Corner Pins	750	V

1. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing.
2. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level.

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4.5 Electromagnetic compatibility characteristics

EMC measurements at IC-level IEC standards are available from STMicroelectronics on request.

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4.6 Temperature profile

The device is qualified in accordance to AEC-Q100 Grade1 requirements, such as HTOL 1,000 h and HTDR 1,000 hrs, T_J = 150 °C.

Mission profile exceeding AEC-Q100 Grade 1, and with junction Temperature equal to or lower than 150 °C have to be evaluated by ST to confirm that are covered by product qualification. Contact your STMicroelectronics Sales representative for validation.

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4.7 Device consumption

Table 9. Device consumption

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
I_{DD_LKG}(2),(3)	CC	C	Leakage current on the V_{DD_LV} supply	T_J = 40 °C	—	—	14	mA
		D		T_J = 25 °C	—	—	10	
		D		T_J = 55 °C	—	—	20	
		D		T_J = 95 °C	—	—	50	
		D		T_J = 120 °C	—	—	90	
		P		T_J = 150 °C	—	—	180	
I_{DD_LV}(3)	CC	P	Dynamic current on the V_{DD_LV} supply, very high consumption profile(4)	—	—	—	210	mA
I_{DD_HV}	CC	P	Total current on the V_{DD_HV} supply(4)	f_{MAX}	—	—	64	mA
$I_{DD_LV_GW}$	CC	T	Dynamic current on the V_{DD_LV} supply, gateway profile(5)	—	—	—	170	mA
$I_{DD_HV_GW}$	CC	T	Dynamic current on the V_{DD_HV} supply, gateway profile(5)	—	—	—	37	mA
$I_{DD_LV_BCM}$	CC	T	Dynamic current on the V_{DD_LV} supply, body profile(6)	—	—	—	150	mA
$I_{DD_HV_BCM}$	CC	T	Dynamic current on the V_{DD_HV} supply, body profile(6)	—	—	—	44	mA
$I_{DD_MAIN_CORE_AC}$	CC	T	Main Core dynamic current(7)	f_{MAX}	—	—	50	mA
$I_{DD_HSM_AC}$	CC	T	HSM platform dynamic operating current(8)	$f_{MAX}/2$	—	—	20	mA
I_{DDHALT}(9)	CC	T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	71	100	mA
I_{DDSTOP}(10)	CC	T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	15	30	mA

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Table 9. Device consumption (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
$I_{DDSTBY8}$	CC	D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 8 KB RAM(11)	T_J = 25 °C	—	85	160	µA
		C		T_J = 40 °C	—	—	250	
		D		T_J = 55 °C	—	—	370	
		D		T_J = 120 °C	—	1.2	2.2	mA
		P		T_J = 150 °C	—	2.9	5.0	
$I_{DDSTBY32}$	CC	D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 32 KB RAM(11)	T_J = 25 °C	—	100	180	µA
		C		T_J = 40 °C	—	—	270	
		D		T_J = 55 °C	—	—	410	
		D		T_J = 120 °C	—	—	2.4	mA
		P		T_J = 150 °C	—	—	5.5	
$I_{DDSTBY256}$	CC	D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 256 KB RAM(11)	T_J = 25 °C	—	150	250	µA
		C		T_J = 40 °C	—	—	390	
		D		T_J = 55 °C	—	—	590	
		D		T_J = 120 °C	—	2.0	3.5	mA
		P		T_J = 150 °C	—	5.1	8	
$I_{DDSSWU1}$	CC	D	SSWU running over all STANDBY period with OPC/TU commands execution and keeping ADC off(12)	T_J = 40 °C	—	1.0	3.5	mA
$I_{DDSSWU2}$	CC	D	SSWU running over all STANDBY period with OPC/TU/ADC commands execution and keeping ADC on(13)	T_J = 40 °C	—	3.5	5.0	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. The leakage considered is the sum of core logic and RAM memories. The contribution of analog modules is not considered, and they are computed in the dynamic I_{DD_LV} and I_{DD_HV} parameters.
3. I_{DD_LKG} (leakage current) and I_{DD_LV} (dynamic current) are reported as separate parameters, to give an indication of the consumption contributors. The tests used in validation, characterization and production are verifying that the total consumption (leakage+dynamic) is lower or equal to the sum of the maximum values provided (I_{DD_LKG} + I_{DD_LV}). The two parameters, measured separately, may exceed the maximum reported for each, depending on the operative conditions and the software profile used.
4. Use case: 2 x e200Z4 @180 MHz, HSM @90 MHz, all IPs clock enabled, Flash access with prefetch disabled, Flash consumption includes parallel read and program/erase, all SARADC in continuous conversion, DMA continuously triggered by ADC conversion, 4 DSPI / 8 CAN / 2 LINFlex and 2 DSPI transmitting, 2 x EMIOS running (8 channels in OPWMT mode), FIRC, SIRC, FXOSC, PLL0-1 running. The switching activity estimated for dynamic consumption does not include I/O toggling, which is highly dependent on the application. Details of the software configuration are available separately. The total device consumption is I_{DD_LV} + I_{DD_HV} + I_{DD_LKG} for the selected temperature.
5. Gateway use case: Two cores running at 160 MHz, DMA, PLL, FLASH read only 25%, 8xCAN, 1xEthernet, HSM, 2xSARADC.
6. BCM use case: One Core running at 160 MHz, no lockstep no, DMA, PLL, FLASH read only 25%, 2xCAN, HSM, 4xSARADC.

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7. Dynamic consumption of one core, including the dedicated I/D-caches and I/D-MEMS contribution.
8. Dynamic consumption of the HSM module, including the dedicated memories, during the execution of Electronic Code Book crypto algorithm on 1 block of 16 byte of shared RAM.
9. Flash in Low Power. Sysclk at 160 MHz, PLL0_PHI at 160 MHz, XTAL at 40 MHz, FIRC 16 MHz ON, RCOSC1M off. FlexCAN: instances: 0, 1, 2, 3, 4, 5, 6, 7 ON (configured but no reception or transmission), Ethernet ON (configured but no reception or transmission), ADC ON (continuously converting). All others IPs clock-gated.
10. Sysclk = RC16 MHz, RC16 MHz ON, RC1 MHz ON, PLL OFF. All possible peripherals off and clock gated. Flash in power down mode.
11. STANDBY mode: device configured for minimum consumption, RC16 MHz off, RC1 MHz on, OSC32K off, SSWU off.
12. SSWU1 mode adder: FIRC = ON, SSWU clocked at 8 MHz and running over all STANDBY period, ADC off. The total standby consumption can be obtained by adding this parameter to the IDDSTBY parameter for the selected memory size and temperature.
13. SSWU2 mode adder: FIRC = ON, SSWU clocked at 8 MHz and running over all STANDBY period, ADC on in continuous conversion. The total standby consumption can be obtained by adding this parameter to the I_{DDSTBY} parameter for the selected memory size and temperature.

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4.8 I/O pad specification

The following table describes the different pad type configurations.

Table 10. I/O pad specification descriptions

Pad type	Description
Weak configuration	Provides a good compromise between transition time and low electromagnetic emission.
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
Strong configuration	Provides fast transition speed; used for fast interface.
Very strong configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface including Ethernet and FlexRay interfaces requiring fine control of rising/falling edge jitter.
Differential configuration	A few pads provide differential capability providing very fast interface together with good EMC performances.
Input only pads	These low input leakage pads are associated with the ADC channels.
Standby pads	These pads (LP pads) are active during STANDBY. They are configured in CMOS level logic and this configuration cannot be changed. Moreover, when the device enters the STANDBY mode, the pad-keeper feature is activated for LP pads. It means that: – if the pad voltage level is above the pad keeper high threshold, a weak pull-up resistor is automatically enabled – if the pad voltage level is below the pad keeper low threshold, a weak pull-down resistor is automatically enabled. For the pad-keeper high/low thresholds please consider (VDD_HV_IO_MAIN / 2) +/-20%.

Note: Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin. PMC_DIG_VSIO register has to be configured to select the voltage level (3.3 V or 5.0 V) for each IO segment.

Logic level is configurable in running mode while it is CMOS not-configurable in STANDBY for LP (low power) pads, so if a LP pad is used to wakeup from STANDBY, it should be configured as CMOS also in running mode in order to prevent device wrong behavior in STANDBY.

4.8.1 I/O input DC characteristics

The following table provides input DC electrical characteristics, as described in *Figure 3*.

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Figure 3. I/O input electrical characteristics

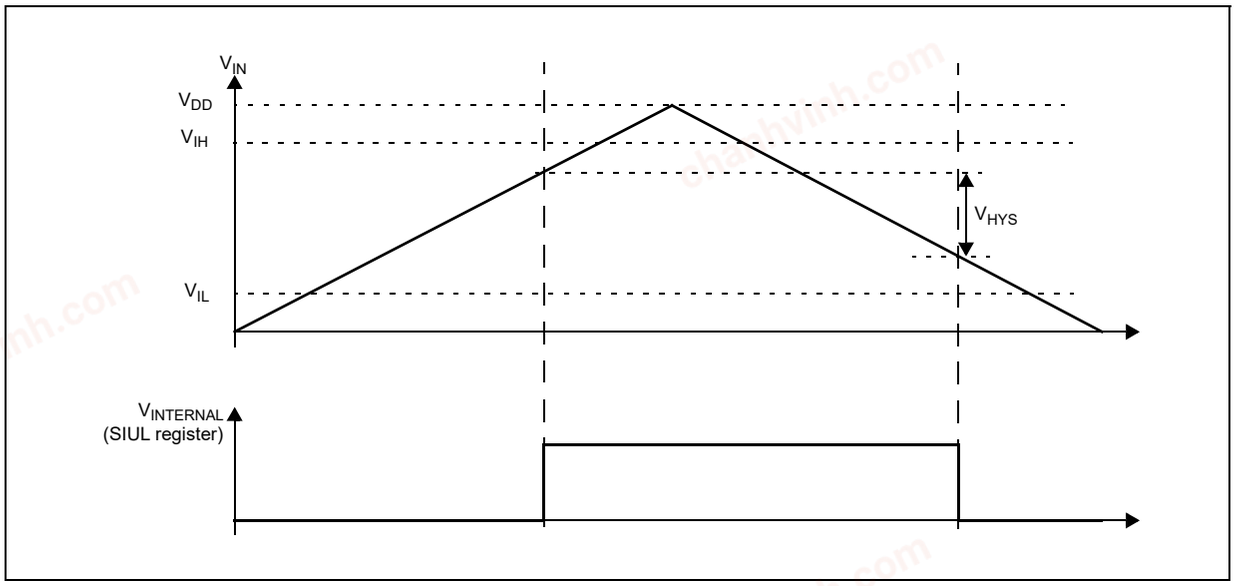


Table 11. I/O input electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{ihttl}	SR	P	Input high level TTL	—	2	—	$V_{DD_HV_IO}$ + 0.3	V
V_{ilttl}	SR	P	Input low level TTL	—	–0.3	—	0.8	V
V_{hysttl}	CC	C	Input hysteresis TTL	—	0.3	—	—	V
CMOS								
V_{ihcmos}	SR	P	Input high level CMOS	—	0.65 * V_{DD}	—	$V_{DD_HV_IO}$ + 0.3	V
V_{ilcmos}	SR	P	Input low level CMOS	—	–0.3	—	0.35 * V_{DD}	V
$V_{hyscmos}$	CC	C	Input hysteresis CMOS	—	0.10 * V_{DD}	—	—	V
COMMON								
I_{LKG}	CC	P	Pad input leakage	INPUT-ONLY pads T_J = 150 °C	—	—	200	nA
I_{LKG}	CC	P	Pad input leakage	STRONG pads T_J = 150 °C	—	—	1,000	nA
I_{LKG}	CC	P	Pad input leakage	VERY STRONG pads, T_J = 150 °C	—	—	1,000	nA

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Table 11. I/O input electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
C_{P1}	CC	D	Pad capacitance	—	—	—	10	pF
V_{drift}	CC	D	Input V_{il}/V_{ih} temperature drift	In a 1 ms period, with a temperature variation <30 °C	—	—	100	mV
W_{FI}	SR	C	Wakeup input filtered pulse(1)	—	—	—	20	ns
W_{NFI}	SR	C	Wakeup input not filtered pulse(1)	—	400	—	—	ns

1. In the range from W_{FI} (max) to W_{NFI} (min), pulses can be filtered or not filtered, according to operating temperature and voltage. Refer to the device pinout IO definition excel file for the list of pins supporting the wakeup filter feature.

Table 12. I/O pull-up/pull-down electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{WPU}	CC	T	Weak pull-up current absolute value	V_{IN} = 1.1 V(1)	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD_HV_IO}$(2)	15	—	—	
R_{WPU}	CC	D	Weak Pull-up resistance	$V_{DD_HV_IO}$ = 5.0 V ± 10%	33	—	93	KΩ
R_{WPU}	CC	D	Weak Pull-up resistance	$V_{DD_HV_IO}$ = 3.3 V ± 10%	19	—	62	KΩ
I_{WPD}	CC	T	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD_HV_IO}$(1)	—	—	130	µA
		P		V_{IN} = 0.9 V(2)	15	—	—	
R_{WPD}	CC	D	Weak Pull-down resistance	$V_{DD_HV_IO}$ = 5.0 V ± 10%	29	—	60	KΩ
R_{WPD}	CC	D	Weak Pull-down resistance	$V_{DD_HV_IO}$ = 3.3 V ± 10%	19	—	60	KΩ

1. Maximum current when forcing a change in the pin level opposite to the pull configuration.
2. Minimum current when keeping the same pin level state than the pull configuration.

Note: When the device enters into standby mode, the LP pads have the input buffer switched-on. As a consequence, if the pad input voltage VIN is $V_{SS}<V_{IN}<V_{DD_HV}$, an additional consumption can be measured in the VDD_HV domain. The highest consumption can be seen around mid-range (VIN ~=VDD_HV/2), 2-3mA depending on process, voltage and temperature.

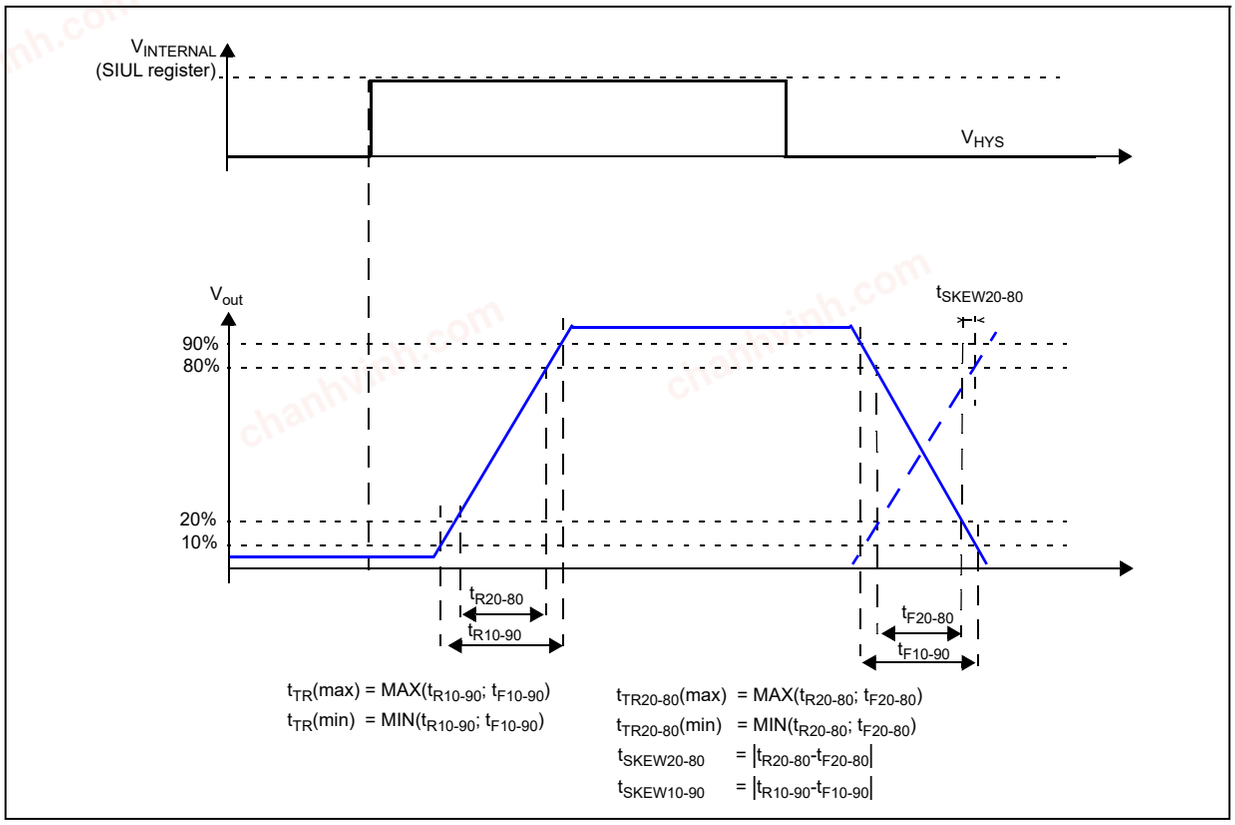
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This situation may occur if the PAD is used as a ADC input channel, and $V_{SS}<V_{IN}<V_{DD_HV}$. The applications should ensure that LP pads are always set to VDD_HV or VSS, to avoid the extra consumption. Please refer to the device pinout IO definition excel file to identify the low-power pads which also have an ADC function.

4.8.2 I/O output DC characteristics

Figure 4 provides description of output DC electrical characteristics.

Figure 4. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 13* provides output driver characteristics for I/O pads when in WEAK/SLOW configuration.
- *Table 14* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 15* provides output driver characteristics for I/O pads when in STRONG/FAST configuration.
- *Table 16* provides output driver characteristics for I/O pads when in VERY STRONG/VERY FAST configuration.

Note: 10%/90% is the default condition for any parameter if not explicitly mentioned differently.

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Table 13. WEAK/SLOW I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_W}	CC	D	Output low voltage for Weak type PADs	I_{ol} = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.1*V_{DD}	V
V_{oh_W}	CC	D	Output high voltage for Weak type PADs	Ioh = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V
$R_{_W}$	CC	P	Output impedance for Weak type PADs	V_{DD} = 5.0 V ± 10%	380	—	1040	Ω
				V_{DD} = 3.3 V ± 10%	250	—	700	
F_{max_W}	CC	T	Maximum output frequency for Weak type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	2	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	1	MHz
t_{TR_W}	CC	T	Transition time output pin weak configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V + 10% V_{DD} = 3.3 V + 10%	25	—	120	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10 % V_{DD} = 3.3 V ± 10 %	50	—	240	ns
$\lvert t_{SKEW_W} \rvert$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%
I_{DCMAX_W}	CC	D	Maximum DC current	V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.5	mA

Table 14. MEDIUM I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_M}	CC	D	Output low voltage for Medium type PADs	I_{ol} = 2.0 mA V_{DD} =5.0 V ± 10 % V_{DD} =3.3 V ± 10 %	—	—	0.1*V_{DD}	V
V_{oh_M}	CC	D	Output high voltage for Medium type PADs	I_{oh}=2.0 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V

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Table 14. MEDIUM I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$R_{_M}$	CC	P	Output impedance for Medium type PADs	V_{DD} = 5.0 V ± 10%	90	—	260	Ω
				V_{DD} = 3.3 V ± 10%	60	—	170	
F_{max_M}	CC	T	Maximum output frequency for Medium type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	12	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10 % V_{DD} = 3.3 V ± 10 %	—	—	6	MHz
t_{TR_M}	CC	T	Transition time output pin MEDIUM configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	8	—	30	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	12	—	60	ns
$\lvert t_{SKEW_M} \rvert$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%
I_{DCMAX_M}	CC	D	Maximum DC current	V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	2	mA

Table 15. STRONG/FAST I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_S}	CC	D	Output low voltage for Strong type PADs	I_{ol} = 8.0 mA V_{DD} = 5.0 V ± 10%	—	—	0.1*V_{DD}	V
				I_{ol} = 5.5 mA V_{DD} =3 .3 V ± 10%	—	—	0.15*V_{DD}	V
V_{oh_S}	CC	D	Output high voltage for Strong type PADs	I_{oh} = 8.0 mA V_{DD} = 5.0 V ± 10%	0.9*V_{DD}	—	—	V
				I_{oh} = 5.5 mA V_{DD} = 3.3 V ± 10%	0.85*V_{DD}	—	—	V
$R_{_S}$	CC	P	Output impedance for Strong type PADs	V_{DD} = 5.0 V ± 10%	20	—	65	Ω
				V_{DD} = 3.3 V ± 10%	28	—	90	

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Table 15. STRONG/FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{max_S}	CC	T	Maximum output frequency for Strong type PADs	CL = 25 pF V_{DD}=5.0 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD}=5.0 V ± 10%	—	—	25	MHz
				CL = 25 pF V_{DD} = 3.3 V ± 10%	—	—	25	MHz
				CL = 50 pF V_{DD} = 3.3 V ± 10%	—	—	12.5	MHz
t_{TR_S}	CC	T	Transition time output pin STRONG configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V ± 10%	3	—	10	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	5	—	16	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	1.5	—	15	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	2.5	—	26	
I_{DCMAX_S}	CC	D	Maximum DC current	V_{DD} = 5 V ± 10%	—	—	8	mA
				V_{DD} = 3.3 V ± 10%	—	—	5.5	
$\lvert t_{SKEW_S} \rvert$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%

Table 16. VERY STRONG/VERY FAST I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_V}	CC	D	Output low voltage for Very Strong type PADs	I_{ol} = 9.0 mA V_{DD} =5.0 V ± 10%	—	—	0.1*V_{DD}	V
				I_{ol} = 9.0 mA V_{DD} =3.3 V ± 10%	—	—	0.15*V_{DD}	V
V_{oh_V}	CC	D	Output high voltage for Very Strong type PADs	I_{oh} = 9.0 mA V_{DD} = 5.0 V ± 10%	0.9*V_{DD}	—	—	V
				I_{oh} = 9.0 mA V_{DD} = 3.3 V ± 10%	0.85*V_{DD}	—	—	V
$R_{_V}$	CC	P	Output impedance for Very Strong type PADs	V_{DD} = 5.0 V ± 10%	20	—	60	Ω
				V_{DD} = 3.3 V ± 10%	18	—	50	

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Table 16. VERY STRONG/VERY FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{max_V}	CC	T	Maximum output frequency for Very Strong type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10%	—	—	25	MHz
				CL = 25 pF V_{DD} = 3.3 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD} = 3.3 V ± 10%	—	—	25	MHz
t_{TR_V}	CC	T	10–90% threshold transition time output pin VERY STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	1	—	6	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	3	—	12	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	1.5	—	6	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	3	—	11	
$t_{TR20\text{-}80_V}$	CC	T	20–80% threshold transition time output pin VERY STRONG configuration (Flexray Standard)	CL = 25 pF V_{DD} = 5.0 V ± 10%	0.8	—	4.5	ns
				CL = 15 pF V_{DD} = 3.3 V ± 10%	1	—	4.5	
t_{TRTTL_V}	CC	T	TTL threshold transition time for output pin in VERY STRONG configuration (Ethernet standard)	CL = 25 pF V_{DD} = 3.3 V ± 10%	0.88	—	5	ns
$\Sigma t_{TR20\text{-}80_V}$	CC	T	Sum of transition time 20–80% output pin VERY STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	—	—	9	ns
				CL = 15 pF V_{DD} = 3.3 V ± 10%	—	—	9	
$\lvert t_{SKEW_V} \rvert$	CC	T	Difference between rise and fall delay	CL = 25 pF V_{DD} = 5.0 V ± 10%	0	—	1.2	ns
I_{DCMAX_V}	CC	D	Maximum DC current	V_{DD} = 5.0 V±10% V_{DD} = 3.3 V ± 10%	—	—	9	mA

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4.8.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in the device pinout Microsoft Excel file attached to the IO_Definition document.

Table 17 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{RMSSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided on the I/O Signal Description table.

Table 17. I/O consumption

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
Average consumption(2)								
I_{RMSSEG}	SR	D	Sum of all the DC I/O current within a supply segment	—	—	—	80	mA
I_{RMS_W}	CC	D	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz, V_{DD} = 5.0 V ± 10 %	—	—	1.1	mA
				C_L = 50 pF, 1 MHz, V_{DD} = 5.0 V ± 10 %	—	—	1.1	
				C_L = 25 pF, 2 MHz, V_{DD} = 3.3 V ± 10 %	—	—	1.0	
				C_L = 25 pF, 1 MHz, V_{DD} = 3.3 V ± 10%	—	—	1.0	
I_{RMS_M}	CC	D	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	mA
				C_L = 50 pF, 6 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	
				C_L = 25 pF, 12 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	
				C_L = 25 pF, 6 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	
I_{RMS_S}	CC	D	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	
				C_L = 25 pF, 12.5 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	

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Table 17. I/O consumption (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
I_{RMS_V}	CC	D	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	
				C_L = 25 pF, 50 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	
Dynamic consumption(3)								
I_{DYN_SEG}	SR	D	Sum of all the dynamic and DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	195	mA
				V_{DD} = 3.3 V ± 10%	—	—	150	
I_{DYN_W}	CC	D	Dynamic I/O current for WEAK configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	16.7	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	16.8	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
I_{DYN_M}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	18.2	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	18.4	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	14.3	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	16.4	
I_{DYN_S}	CC	D	Dynamic I/O current for STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	57	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	63.5	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	31	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	33.5	

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Table 17. I/O consumption (continued)

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
I_{DYN_V}	CC	D	Dynamic I/O current for VERY STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	62	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	70	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	52	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	55	

1. I/O current consumption specifications for the 4.5 V $\leq V_{DD_HV_IO} \leq$ 5.5 V range are valid for VSIO_[VSIO_xx] = 1, and VSIO[VSIO_xx] = 0 for 3.0 V $\leq V_{DD_HV_IO} \leq$ 3.6 V.
2. Average consumption in one pad toggling cycle.
3. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

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4.9 Reset pad (PORST) electrical characteristics

The device implements dedicated bidirectional reset pins as below specified. $\overline{\text{PORST}}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 KΩ.

Figure 5. Startup Reset requirements

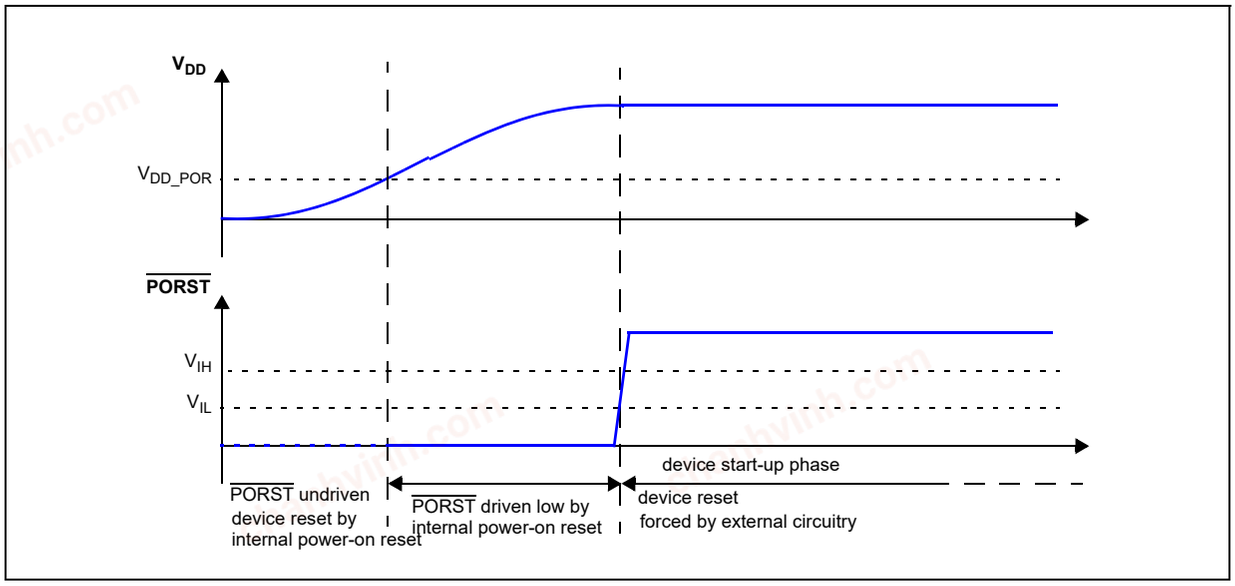


Figure 6 describes device behavior depending on supply signal on PORST:

1. $\overline{\text{PORST}}$ low pulse has too low amplitude: it is filtered by input buffer hysteresis. Device remains in current state.
2. $\overline{\text{PORST}}$ low pulse has too short duration: it is filtered by low pass filter. Device remains in current state.
3. $\overline{\text{PORST}}$ low pulse is generating a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least WFRST. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until WNFRST. Device state is unknown. It may either be reset or remains in current state depending on extra condition (temperature, voltage, device).
   c) $\overline{\text{PORST}}$ asserted for longer than WNFRST. Device is under reset.

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Figure 6. Noise filtering on reset signal

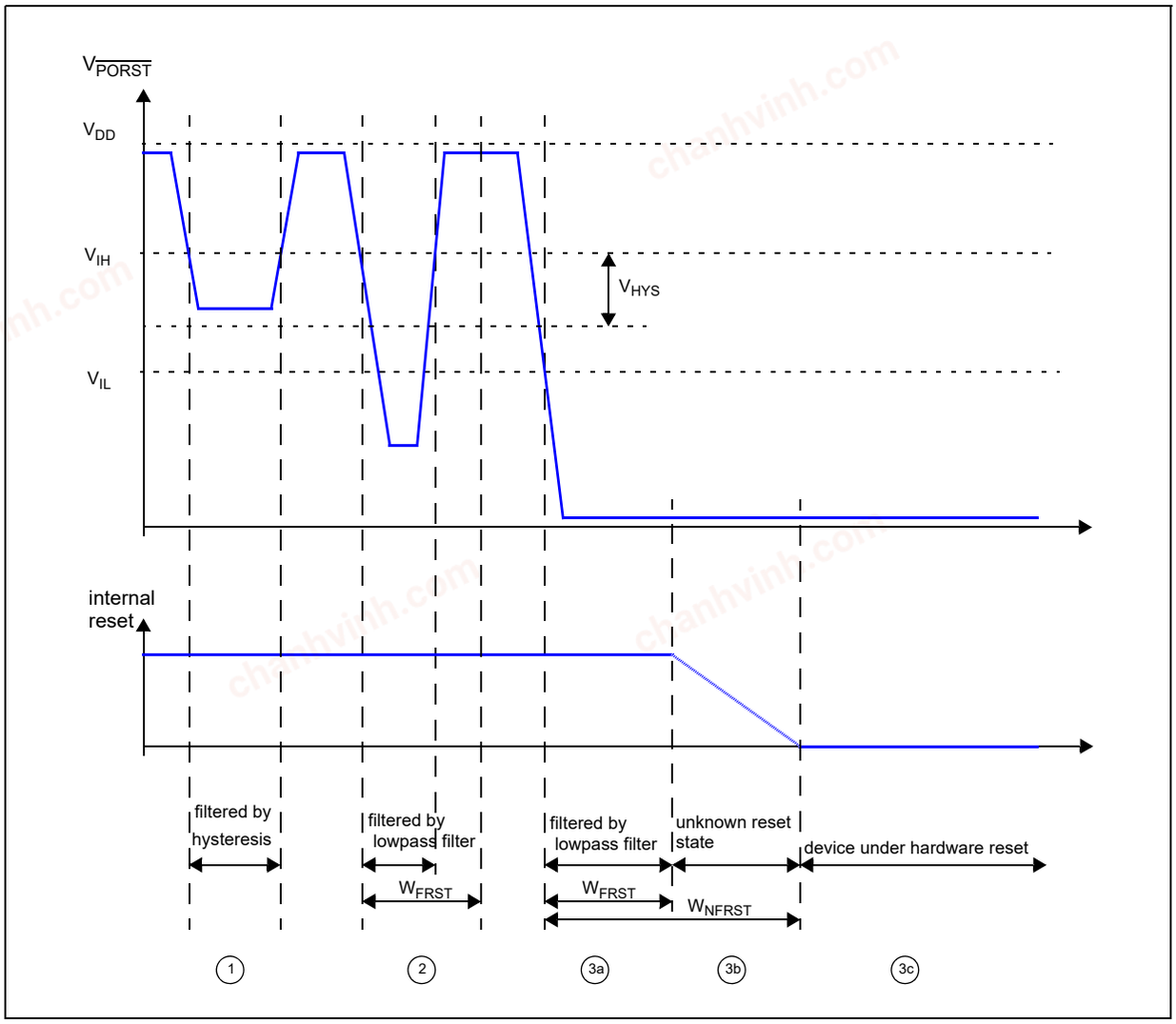


Table 18. Reset PAD electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IHRES}	SR	P	Input high level TTL	V_{DD_HV} = 5.0 V ± 10% V_{DD_HV} = 3.3 V ± 10%	2	—	$V_{DD_HV_IO}$ +0.3	V
V_{ILRES}	SR	P	Input low level TTL	V_{DD_HV} = 5.0 V ± 10%	-0.3	—	0.8	V
				V_{DD_HV} = 3.3 V ± 10%	-0.3	—	0.6	
V_{HYSRES}	CC	C	Input hysteresis TTL	V_{DD_HV} = 5.0 V ± 10%	0.3	—	—	V
				V_{DD_HV} = 3.3 V ± 10%	0.2	—	—	
V_{DD_POR}	CC	D	Minimum supply for strong pull-down activation	V_{DD_HV} = 5.0 V ± 10%	—	—	1.6	V
				V_{DD_HV} = 3.3 V ± 10%	—	—	1.05	

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Table 18. Reset PAD electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{OL_R}	CC	P	Strong pull-down current (1)	V_{DD_HV} = 5.0 V ± 10%	12	—	—	mA
				V_{DD_HV} = 3.3 V ± 10%	8	—	—	
I_{WPU}	CC	P	Weak pull-up current absolute value	V_{IN} = 1.1 V(2) V_{DD_HV} = 5.0 V ± 10%	—	—	130	µA
		P		V_{IN} = 1.1 V V_{DD_HV} = 3.3 V ± 10%	—	—	70	
		P		V_{IN} = 0.69 * $V_{DD_HV_IO}$(3) V_{DD_HV} = 5.0 V ± 10%	15	—	—	
		P		V_{IN} = 0.69 * $V_{DD_HV_IO}$ V_{DD_HV} = 3.3 V ± 10%	15	—	—	
I_{WPD}	CC	P	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD_HV_IO}$(2) V_{DD_HV} = 5.0 V ± 10%	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD_HV_IO}$(2) V_{DD_HV} = 3.3 V ± 10%	—	—	80	
		P		V_{IN} = 0.9 V V_{DD_HV} = 5.0 V ± 10%	15	—	—	
		P		V_{IN} = 0.9 V $V_{DD_HVDD_HV}$ = 3.3 V ± 10%	15	—	—	
W_{FRST}	CC	P	Input filtered pulse	V_{DD_HV} = 5.0 V ± 10%	—	—	500	ns
		P		V_{DD_HV} = 3.3 V ± 10%	—	—	600	
W_{NFRST}	CC	P	Input not filtered pulse	V_{DD_HV} = 5.0 V ± 10%	2000	—	—	ns
		P		V_{DD_HV} = 3.3 V ± 10%	3000	—	—	

1. I_{ol_r} applies to PORST: Strong Pull-down is active on PHASE0 for PORST. Refer to the device pinout IO definition excel file for details regarding pin usage.
2. Maximum current when forcing a change in the pin level opposite to the pull configuration.
3. Minimum current when keeping the same pin level state than the pull configuration.

Table 19. Reset Pad state during power-up and reset

PAD	POWER-UP State	RESET state	DEFAULT state(1)	STANDBY state
PORST	Strong pull-down	Weak pull-down	Weak pull-down	Weak pull-up

1. Before SW Configuration. Please refer to the Device Reference Manual, Reset Generation Module (MC_RGM) Functional Description chapter for the details of the power-up phases.

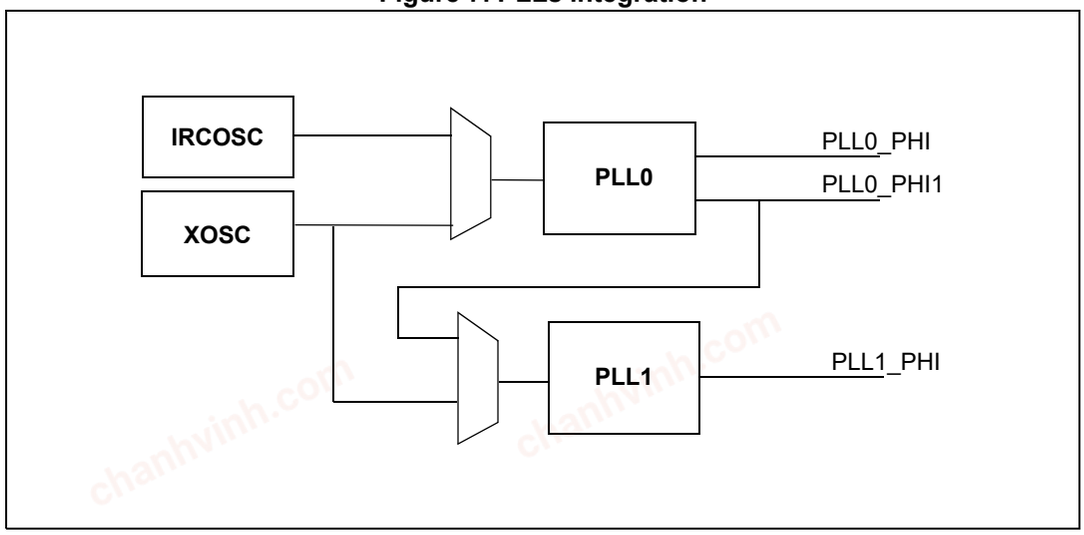
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4.10 PLLs

Two phase-locked loop (PLL) modules are implemented to generate system and auxiliary clocks on the device.

Figure 7 depicts the integration of the two PLLs. Refer to device Reference Manual for more detailed schematic.

Figure 7. PLLs integration



4.10.1 PLL0

Table 20. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock(1)	—	8	—	44	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle(1)	—	40	—	60	%
f_{INFIN}	SR	—	PLL0 PFD (Phase Frequency Detector) input clock frequency	—	8	—	20	MHz
$f_{PLL0VCO}$	CC	P	PLL0 VCO frequency	—	600	—	1400	MHz
$f_{PLL0PHI0}$	CC	D	PLL0 output frequency	—	4.762	—	400	MHz
$f_{PLL0PHI1}$	CC	D	PLL0 output clock PHI1	—	20	—	175(2)	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL0PHI0SPJ}\rvert$(3)	CC	T	PLL0_PHI0 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI0}$ = 400 MHz, 6-sigma pk-pk	—	—	200	ps

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Table 20. PLL0 electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$(3)	CC	D	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma pk-pk	—	—	300(4)	ps
$\Delta_{PLL0LTJ}$(3)	CC	D	PLL0 output long term jitter(4) f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
				16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
				long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	CC	D	PLL0 consumption	FINE LOCK state	—	—	6	mA

1. PLL0IN clock retrieved directly from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.
2. If the PLL0_PHI1 is used as an input for PLL1, then the PLL0_PHI1 frequency shall obey the maximum input frequency limit set for PLL1 (87.5 MHz, according to *Table 21*).
3. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
4. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.20 V±5%, with frequency below PLL bandwidth (40 kHz) will be filtered.

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4.10.2 PLL1

PLL1 is a frequency modulated PLL with Spread Spectrum Clock Generation (SSCG) support.

Table 21. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL1IN}	SR	—	PLL1 input clock(1)	—	37.5	—	87.5	MHz
Δ_{PLL1IN}	SR	—	PLL1 input clock duty cycle(1)	—	35	—	65	%
f_{INFIN}	SR	—	PLL1 PFD (Phase Frequency Detector) input clock frequency	—	37.5		87.5	MHz
$f_{PLL1VCO}$	CC	P	PLL1 VCO frequency	—	600	—	1400	MHz
$f_{PLL1PHI0}$	CC	D	PLL1 output clock PHI0	—	4.762	—	F_{SYS}(2)	MHz
$t_{PLL1LOCK}$	CC	P	PLL1 lock time	—	—	—	50	µs
$f_{PLL1MOD}$	CC	T	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	CC	T	PLL1 modulation depth (when enabled)	Center spread(3)	0.25	—	2	%
				Down spread	0.5	—	4	%
$\lvert\Delta_{PLL1PHI0SPJ}\rvert$(4)	CC	T	PLL1_PHI0 single period peak to peak jitter	$f_{PLL1PHI0}$ = 200 MHz, 6-sigma	—	—	500(5)	ps
I_{PLL1}	CC	D	PLL1 consumption	FINE LOCK state	—	—	5	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external FXOSC clock. Input characteristics are granted when using internal PPL0 or external oscillator is used in functional mode.
2. Refer to *Section 4.3: Operating conditions* for the maximum operating frequency.
3. The device maximum operating frequency F_{SYS} (max) includes the frequency modulation. If center modulation is selected, the FSYS must be below the maximum by MD (Modulation Depth Percentage), such that FSYS(max)=FSYS(1+MD%). Refer to the Reference Manual for the PLL programming details.
4. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
5. 1.25 V±5%, application noise below 40 kHz at V_{DD_LV} pin - no frequency modulation.

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4.11 Oscillators

4.11.1 Crystal oscillator 40 MHz

Table 22. External 40 MHz oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{XTAL}	CC	D	Crystal Frequency Range(1)	—	4(2)	8	MHz
					>8	20	
					>20	40	
t_{cst}	CC	T	Crystal start-up time (3),(4)	T_J = 150 °C	—	5	ms
t_{rec}	CC	D	Crystal recovery time(5)	—	—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage(6) (External Reference)	V_{REF} = 0.29 * $V_{DD_HV_OSC}$	V_{REF} + 0.75	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage(6) (External Reference)	V_{REF} = 0.29 * $V_{DD_HV_OSC}$	—	V_{REF} - 0.75	V
C_{S_EXTAL}	CC	D	Total on-chip stray capacitance on EXTAL pin(7)	—	3	7	pF
C_{S_XTAL}	CC	D	Total on-chip stray capacitance on XTAL pin(7)	—	3	7	pF
g_m	CC	P	Oscillator Transconductance	f_{XTAL} = 4 – 8 MHz freq_sel[2:0] = 000	3.9	13.6	mA/V
		D		f_{XTAL} = 5 - 10 MHz freq_sel[2:0] = 001	5	17.5	
		D		f_{XTAL} = 10 – 15 MHz freq_sel[2:0] = 010	8.6	29.3	
		P		f_{XTAL} = 15 - 20 MHz freq_sel[2:0] = 011	14.4	48	
		D		f_{XTAL} = 20 - 25 MHz freq_sel[2:0] = 100	21.2	69	
		D		f_{XTAL} = 25 – 30 MHz freq_sel[2:0] = 101	27	86	
		D		f_{XTAL} = 30 - 35 MHz freq_sel[2:0] = 110	33.5	115	
		P		f_{XTAL} = 35 - 40 MHz freq_sel[2:0] = 111	33.5	115	
V_{EXTAL}	CC	D	Oscillation Amplitude on the EXTAL pin after startup(8)	T_J = –40 °C to 150 °C	0.5	1.8	V

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Table 22. External 40 MHz oscillator electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{HYS}	CC	D	Comparator Hysteresis	T_J = –40 °C to 150 °C	0.1	1.0	V
I_{XTAL}	CC	D	XTAL current[8],[9]	T_J = –40 °C to 150 °C	—	14	mA

1. The range is selectable by UTEST miscellaneous DCF client XOSC_FREQ_SEL.
2. The XTAL frequency, if used to feed the PPL0 (or PLL1), shall obey the minimum input frequency limit set for PLL0 (or PLL1).
3. This value is determined by the crystal manufacturer and board design, and it can potentially be higher than the maximum provided.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
6. Applies to an external clock input and not to crystal mode.
7. See crystal manufacturer's specification for recommended load capacitor (C_L) values. The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
8. Amplitude on the EXTAL pin after startup is determined by the ALC block, that is the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
9. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator.

4.11.2 Crystal Oscillator 32 kHz

Table 23. 32 kHz External Slow Oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{sxosc}	SR	T	Slow external crystal oscillator frequency	—	—	32768	—	Hz
g_{msxosc}	CC	P	Slow external crystal oscillator transconductance	—	9.5	—	32	µA/V
V_{sxosc}	CC	T	Oscillation Amplitude	—	0.5	—	1.7	V
I_{sxoosc}	CC	D	Oscillator consumption	—	—	—	9	µA
T_{sxosc}	CC	T	Start up time	—	—	—	2	s

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4.11.3 RC oscillator 16 MHz

Table 24. Internal RC oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation without temperature compensation	T < 150 °C	–5	—	5	%
δf_{var_T}	CC	T	IRC frequency variation with temperature compensation	T < 150 °C	–3	—	3	%
δf_{var_SW}		T	IRC software trimming accuracy	Trimming temperature	–0.5	±0.3	0.5	%
T_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs
T_{start_T}	CC	T	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs
I_{FIRC}	CC	T	Current consumption on HV power supply (1)	After T_{start_T}	—	—	1200	µA

1. The actual consumption difference can be higher due to additional consumption of core logic clocked by RCOSC16M.

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4.11.4 Low power RC oscillator

Table 25. 1024 kHz internal RC oscillator electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{sirc}	CC	T	Slow Internal RC oscillator frequency	—	—	1024	—	kHz
δf_{var_T}	CC	P	Frequency variation across temperature	–40 °C < T < 150 °C	–9	—	+9	%
δf_{var_V}	CC	P	Frequency variation across voltage	–40 °C < T < 150 °C	–5	—	+5	%
I_{sirc}	CC	T	Slow Internal RC oscillator current	T = 55 °C	—	—	6	µA
T_{sirc}	CC	T	Start up time, after switching ON the internal regulator.	—	—	—	12	µS

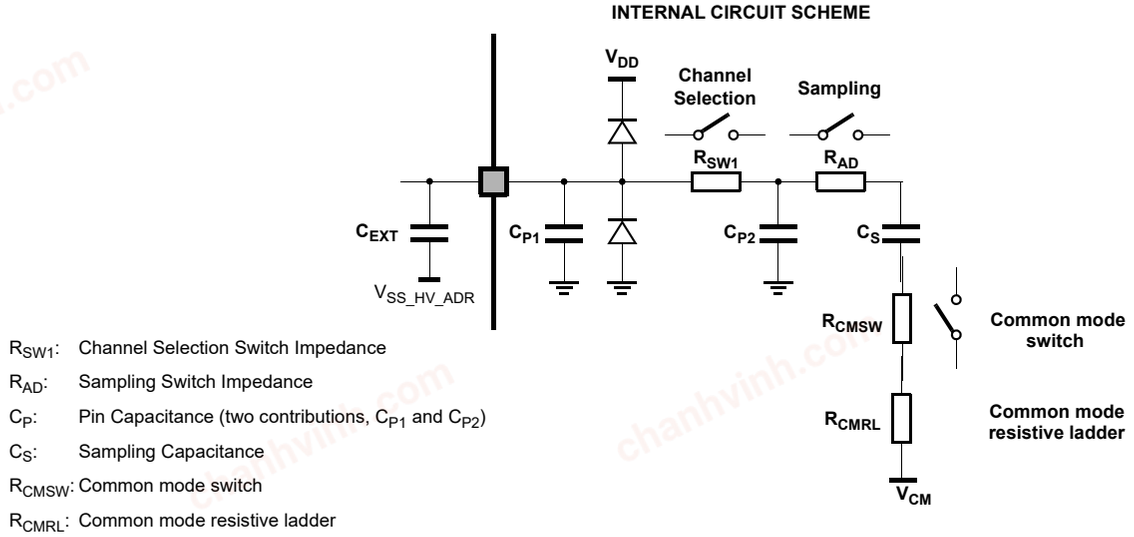
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4.12 ADC system

4.12.1 ADC input description

Figure 8 shows the input equivalent circuit for SARn and SARB channels.

Figure 8. Input equivalent circuit (Fast SARn and SARB channels)



R_{SW1}: Channel Selection Switch Impedance
R_{AD}: Sampling Switch Impedance
C_P: Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S: Sampling Capacitance
R_{CMSW}: Common mode switch
R_{CMRL}: Common mode resistive ladder
V_{CM}: Common mode voltage (~0.5 V_{DD})
C_{EXT}: External capacitance

The above scheme can be used as approximation circuitry for external filtering definition.

All specifications in the following table are valid for the full input voltage range for the analog inputs.

Table 26. ADC pin specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$R_{20K\Omega}$	CC	D	Internal voltage reference source impedance.	—	16	30	KΩ
I_{LKG}	CC	—	Input leakage current, two ADC channels on input-only pin.	See IO chapter *Table 11: I/O input electrical characteristics*, parameter I_{LKG}.			
I_{INJ1}	SR	—	Injection current on analog input preserving functionality at full or degraded performances.	See Operating Conditions chapter *Table 5: Operating conditions*, I_{INJ1} parameter.			
C_{HV_ADC}	SR	D	$V_{DD_HV_ADV}$ external capacitance.	See Power Management chapter *Table 34: External components integration*, C_{ADC} parameter.			
C_{P1}	CC	D	Pad capacitance	See IO chapter *Table 11: I/O input electrical characteristics*, parameter C_{P1}.			

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Table 26. ADC pin specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
C_{P2}	CC	D	Internal routing capacitance	SARB channels	—	2	pF
				SARn 10bit channels	—	0.5	
				SARn 12bit channels	—	1	
C_S	CC	D	SAR ADC sampling capacitance	SARn 12bit	—	5	pF
				SARn 10bit	—	2	
R_{SWn}	CC	D	Analog switches resistance	SARB channels	0	1.8	kΩ
				SARn 10bit channels	0	0.8	
				SARn 12bit channels	0	1.8	
R_{AD}	CC	D	ADC input analog switches resistance	SARn 12bit	—	0.8	kΩ
				SARn 10bit	—	3.2	
R_{CMSW}	CC	D	Common mode switch resistance	Sum of the two resistances	—	9	kΩ
R_{CMRL}	CC	D	Common mode resistive ladder				kΩ
R_{SAFEPD}(1)	CC	D	Discharge resistance for ADC input-only pins (strong pull-down for safety)	$V_{DD_HV_IO}$ = 5.0 V ± 10%	—	300	W
				$V_{DD_HV_IO}$ = 3.3 V ± 10%	—	500	W
A_{BGAP}	CC	D	ADC digital bandgap accuracy		-1.5	+1.5	%
C_{EXT}	SR	—	External capacitance at the pad input pin	To preserve the accuracy of the ADC, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible. This capacitor contributes to attenuating the noise present on the input pin. The impedance relative to the signal source can limit the ADC's sample rate.			

1. It enables discharge of up to 100 nF from 5 V every 300 ms. Refer to the device pinout Microsoft Excel file attached to the IO_Definition document for the pads supporting it.

4.12.2 SAR ADC 12-bit electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Note: The functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maximum may affect device reliability or cause permanent damage to the device.

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Table 27. SARn ADC electrical specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{ADCK}	SR	P	Clock frequency	Standard frequency mode	7.5	13.33	MHz
		T		High frequency mode	>13.33	16.0	
$t_{ADCINIT}$	SR	—	ADC initialization time	—	1.5	—	µs
$t_{ADCBIASINIT}$	SR	—	ADC BIAS initialization time	—	5	—	µs
$t_{ADCPRECH}$	SR	T	ADC decharge time	Fast SAR	$1/f_{ADCK}$	—	µs
				Slow SAR (SARDAC_B)	$2/f_{ADCK}$	—	
ΔV_{PRECH}	SR	D	Decharge voltage precision	T_J < 150 °C	0	0.25	V
$R_{20K\Omega}$	CC	D	Internal voltage reference source impedance	—	16	30	KΩ
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS_HV_ADR}$, 1/3 * $V_{DD_HV_ADR}$, 2/3 * $V_{DD_HV_ADR}$, $V_{DD_HV_ADR}$)	–0.20	0.20	V

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Table 27. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$t_{ADCSAMPLE}$	SR	P	ADC sample time(1)	Fast SAR – 12-bit configuration	$6/f_{ADCK}$	—	µs
		D		Fast SAR – 10-bit configuration mode 1(2) (Standard frequency mode only)	$6/f_{ADCK}$		
				Fast SAR – 10-bit configuration mode 2(3) (Standard frequency mode only)	$5/f_{ADCK}$		
				Fast SAR – 10-bit configuration mode 3(4) (High frequency mode only)	$6/f_{ADCK}$		
				Slow SAR (SARADC_B) – 12-bit configuration	$12/f_{ADCK}$		
				Slow SAR (SARADC_B) – 10-bit configuration mode 1(2) (Standard frequency mode only)	$12/f_{ADCK}$		
				Slow SAR (SARADC_B) – 10-bit configuration mode 2(3) (Standard frequency mode only)	$10/f_{ADCK}$		
				Slow SAR (SARADC_B) – 10-bit configuration mode 3(4) (High frequency mode only)	$12/f_{ADCK}$		
				Conversion of BIAS test channels through 20 kΩ input.	$40/f_{ADCK}$		
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration	$12/f_{ADCK}$	—	µs
		D		10-bit configuration	$10/f_{ADCK}$	—	
$I_{ADCREFH}$(5),(6)	CC	T	ADC high reference current	Run mode (average across all codes)	—	7	µA
				Power Down mode	—	1	
$I_{ADCREFL}$(6)	CC	D	ADC low reference current	Run mode $V_{DD_HV_ADR_S} \leq 5.5$ V	—	15	µA
				Power Down mode $V_{DD_HV_ADR_S} \leq 5.5$ V	—	1	
I_{ADV_S}(6)	CC	P	$V_{DD_HV_ADV}$ power supply current	Run mode	—	4.0	mA
		D		Power Down mode	—	0.04	

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Table 27. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
TUE_{12}	CC	T	Total unadjusted error in 12-bit configuration(7)	T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V, $V_{DD_HV_ADR_S}$ > 3 V	–4	4	LSB (12b)
		P		T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V, $V_{DD_HV_ADR_S}$ > 3 V	–6	6	
		T		T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V, 3 V > $V_{DD_HV_ADR_S}$ > 2 V	–6	6	
		D		High frequency mode, T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V, $V_{DD_HV_ADR_S}$ > 3 V	–12	12	
TUE_{10}	CC	D	Total unadjusted error in 10-bit configuration(7)	Mode 1, T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V $V_{DD_HV_ADR_S}$ > 3 V	–1.5	1.5	LSB (10b)
		D		Mode 1, T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V, 3 V > $V_{DD_HV_ADR_S}$ > 2 V	–2.0	2.0	
		C		Mode 2, T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V $V_{DD_HV_ADR_S}$ > 3 V	–3.0	3.0	
		C		Mode 3, T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V $V_{DD_HV_ADR_S}$ > 3 V	–4.0	4.0	

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Table 27. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{12}	CC	D	TUE degradation due to $V_{DD_HV_ADR}$ offset with respect to $V_{DD_HV_ADV}$	$V_{IN} < V_{DD_HV_ADV}$ $V_{DD_HV_ADR} - V_{DD_HV_ADV} \in$ [0:25 mV]	–1	1	LSB (12b)
				$V_{IN} < V_{DD_HV_ADV}$ $V_{DD_HV_ADR} - V_{DD_HV_ADV} \in$ [25:50 mV]	–2	2	
				$V_{IN} < V_{DD_HV_ADV}$ $V_{DD_HV_ADR} - V_{DD_HV_ADV} \in$ [50:75 mV]	–4	4	
				$V_{IN} < V_{DD_HV_ADV}$ $V_{DD_HV_ADR} - V_{DD_HV_ADV} \in$ [75:100 mV]	–6	6	
				$V_{DD_HV_ADV} < V_{IN} < V_{DD_HV_ADR}$ $V_{DD_HV_ADR} - V_{DD_HV_ADV} \in$ [0:25 mV]	–2.5	2.5	
				$V_{DD_HV_ADV} < V_{IN} < V_{DD_HV_ADR}$ $V_{DD_HV_ADR} - V_{DD_HV_ADV} \in$ [25:50 mV]	–4	4	
				$V_{DD_HV_ADV} < V_{IN} < V_{DD_HV_ADR}$ $V_{DD_HV_ADR} - V_{DD_HV_ADV} \in$ [50:75 mV]	–7	7	
				$V_{DD_HV_ADV} < V_{IN} < V_{DD_HV_ADR}$ $V_{DD_HV_ADR} - V_{DD_HV_ADV} \in$ [75:100 mV]	–12	12	
DNL(8)	CC	P	Differential non-linearity	Standard frequency mode, $V_{DD_HV_ADV} > 4$ V $V_{DD_HV_ADR_S} > 4$ V	–1	2	LSB (12b)
		T		High frequency mode, $V_{DD_HV_ADV} > 4$ V $V_{DD_HV_ADR_S} > 4$ V	–1	2	

1. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Refer to *Figure 8* for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
2. Mode1: 6 sampling cycles + 10 conversion cycles at 13.33 MHz.
3. Mode2: 5 sampling cycles + 10 conversion cycles at 13.33 MHz.
4. Mode3: 6 sampling cycles + 10 conversion cycles at 16 MHz.
5. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
6. Current parameter values are for a single ADC.

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7. TUE is granted with injection current within the range defined in *Table 26*, for parameters classified as T and D.
8. DNL is granted with injection current within the range defined in *Table 26*, for parameters classified as T and D.

4.12.3 SAR ADC 10-bit electrical specification

The ADC comparators are 10-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Note: The functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maximum may affect device reliability or cause permanent damage to the device.

Table 28. ADC-Comparator electrical specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{ADCK}	SR	P	Clock frequency	Standard frequency mode	7.5	13.33	MHz
		T		High frequency mode	>13.33	16.0	
$t_{ADCINIT}$	SR	—	ADC initialization time	—	1.5	—	µs
$t_{ADCBIASINIT}$	SR	—	ADC BIAS initialization time	—	5	—	µs
$t_{ADCINITSBY}$	SR	—	ADC initialization time in standby	Standby Mode	8	—	µs
$t_{ADCPRECH}$	SR	T	ADC precharge time	Fast channel	$1/f_{ADCK}$	—	µs
				Standard channel	$2/f_{ADCK}$	—	
ΔV_{PRECH}	SR	D	Precharge voltage precision	T_J < 150 °C	0	0.25	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time(1)	10-bit ADC mode, Fast channel	$5/f_{ADCK}$(2)	—	µs
				10-bit ADC mode, Standard channel	$6/f_{ADCK}$	—	µs
$t_{ADCEVAL}$	SR	P	ADC evaluation time	10-bit ADC mode	$10/f_{ADCK}$	—	µs
		D		ADC comparator mode	$2/f_{ADCK}$	—	
$I_{ADCREFH}$(3),(4)	CC	T	ADC high reference current	Run mode (average across all codes)	—	7	µA
				Power Down mode	—	1	
				ADC comparator mode	—	19.5	
$I_{ADCREFL}$(5)	CC	D	ADC low reference current	Run mode $V_{DD_HV_ADR_S} \leq 5.5$ V	—	15	µA
				Power Down mode $V_{DD_HV_ADR_S} \leq 5.5$ V	—	1	
				ADC comparator mode	—	20.5	

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Table 28. ADC-Comparator electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{ADV_S}(5)	CC	P	$V_{DD_HV_ADV}$ power supply current	Run mode	—	4	mA
		D		Power Down mode	—	0.04	
TUE_{10}	CC	T	Total unadjusted error in 10-bit configuration(6)	T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V, $V_{DD_HV_ADR_S}$ > 3 V	–2	2	LSB (10b)
		P		T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V, $V_{DD_HV_ADR_S}$ > 3 V	–3	3	
		T		T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V, 3 V > $V_{DD_HV_ADR_S}$ > 2 V	–3	3	
		D		High frequency mode, T_J < 150 °C, $V_{DD_HV_ADV}$ > 3 V, $V_{DD_HV_ADR_S}$ > 3 V	–3	3	
ΔTUE_{10}	CC	D	TUE degradation due to $V_{DD_HV_ADR}$ offset with respect to $V_{DD_HV_ADV}$	V_{IN} < $V_{DD_HV_ADV}$ $V_{DD_HV_ADR}$ – $V_{DD_HV_ADV}$ ∈ [0:25 mV]	–1.0	1.0	LSB (10b)
				V_{IN} < $V_{DD_HV_ADV}$ $V_{DD_HV_ADR}$ – $V_{DD_HV_ADV}$ ∈ [25:50 mV]	–2.0	2.0	
				V_{IN} < $V_{DD_HV_ADV}$ $V_{DD_HV_ADR}$ – $V_{DD_HV_ADV}$ ∈ [50:75 mV]	–3.5	3.5	
				V_{IN} < $V_{DD_HV_ADV}$ $V_{DD_HV_ADR}$ – $V_{DD_HV_ADV}$ ∈ [75:100 mV]	–6.0	6.0	
				$V_{DD_HV_ADV}$ < V_{IN} < $V_{DD_HV_ADR}$ $V_{DD_HV_ADR}$ – $V_{DD_HV_ADV}$ ∈ [0:25 mV]	–2.5	2.5	
				$V_{DD_HV_ADV}$ < V_{IN} < $V_{DD_HV_ADR}$ $V_{DD_HV_ADR}$ – $V_{DD_HV_ADV}$ ∈ [25:50 mV]	–4.0	4.0	
				$V_{DD_HV_ADV}$ < V_{IN} < $V_{DD_HV_ADR}$ $V_{DD_HV_ADR}$ – $V_{DD_HV_ADV}$ ∈ [50:75 mV]	–7.0	7.0	
				$V_{DD_HV_ADV}$ < V_{IN} < $V_{DD_HV_ADR}$ $V_{DD_HV_ADR}$ – $V_{DD_HV_ADV}$ ∈ [75:100 mV]	–12.0	12.0	

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Table 28. ADC-Comparator electrical specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
DNL[7]	CC	P	Differential non-linearity std. mode	Standard frequency mode, $V_{DD_HV_ADV}$ > 4 V $V_{DD_HV_ADR_S}$ > 4 V	–1	2	LSB (10b)
		T		High frequency mode, $V_{DD_HV_ADV}$ > 4 V $V_{DD_HV_ADR_S}$ > 4 V	–1	2	

1. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Refer to *Figure 8* for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
2. In case the ADC is used as Fast Comparator the sampling time is $t_{ADCSAMPLE} = 2/f_{ADCK}$.
3. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
4. Current parameter values are for a single ADC.
5. All channels of all SAR-ADC12bit and SAR-ADC10bit are impacted with same degradation, independently from the ADC and the channel subject to current injection.
6. TUE is granted with injection current within the range defined in *Table 26*, for parameters classified as T and D.
7. DNL is granted with injection current within the range defined in *Table 26*, for parameters classified as T and D.

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4.13 Temperature Sensor

The following table describes the temperature sensor electrical characteristics.

Table 29. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	—	Temperature monitoring range	—	–40	—	150	°C
T_{SENS}	CC	T	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	P	Accuracy	T_J < 150 °C	–3	—	3	°C

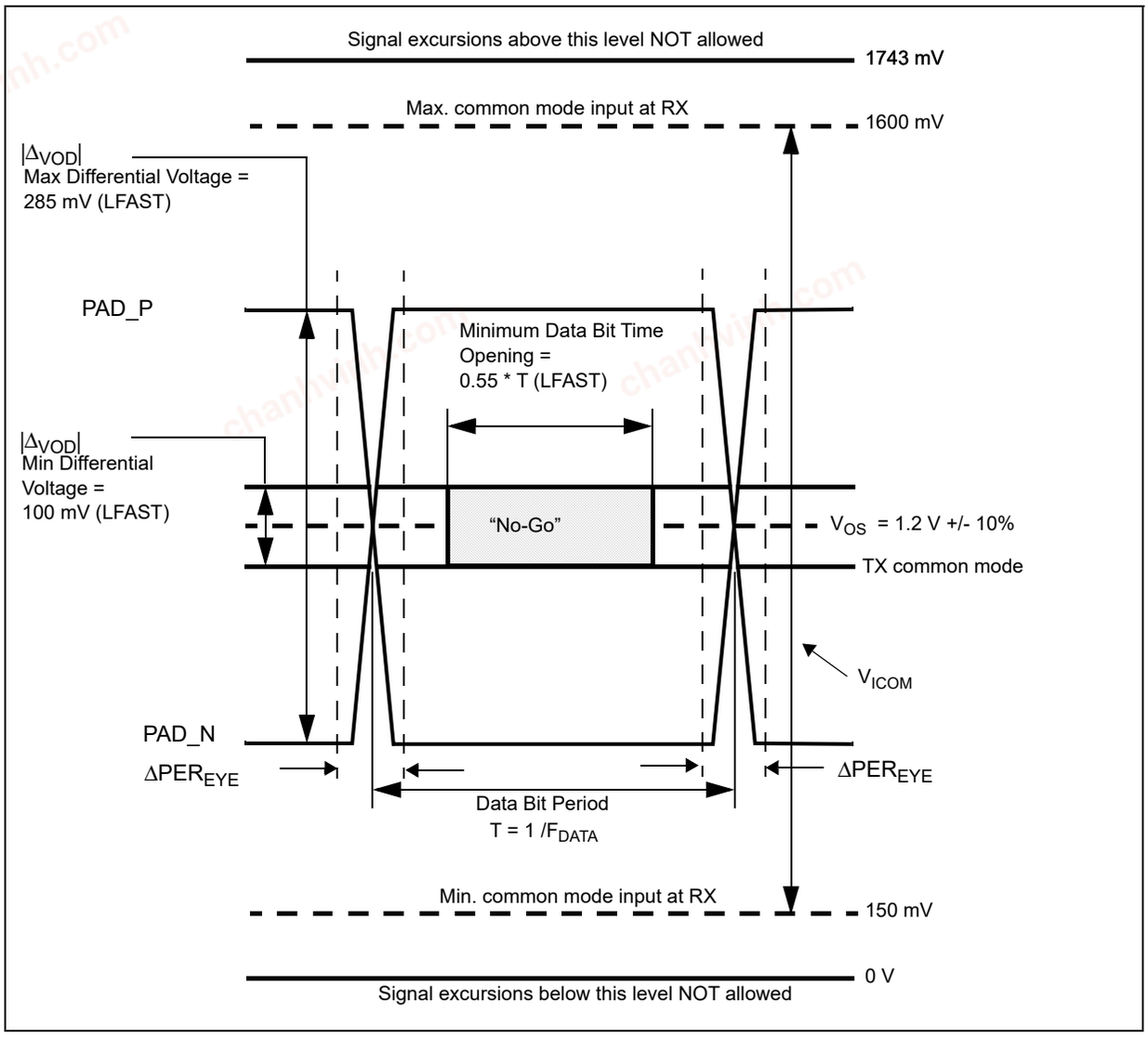
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4.14 LFAST pad electrical characteristics

The LFAST(LVDS Fast Asynchronous Serial Transmission) pad electrical characteristics apply to high-speed debug serial interfaces on the device.

4.14.1 LFAST interface timing diagrams

Figure 9. LFAST LVDS timing definition



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Figure 10. Power-down exit time

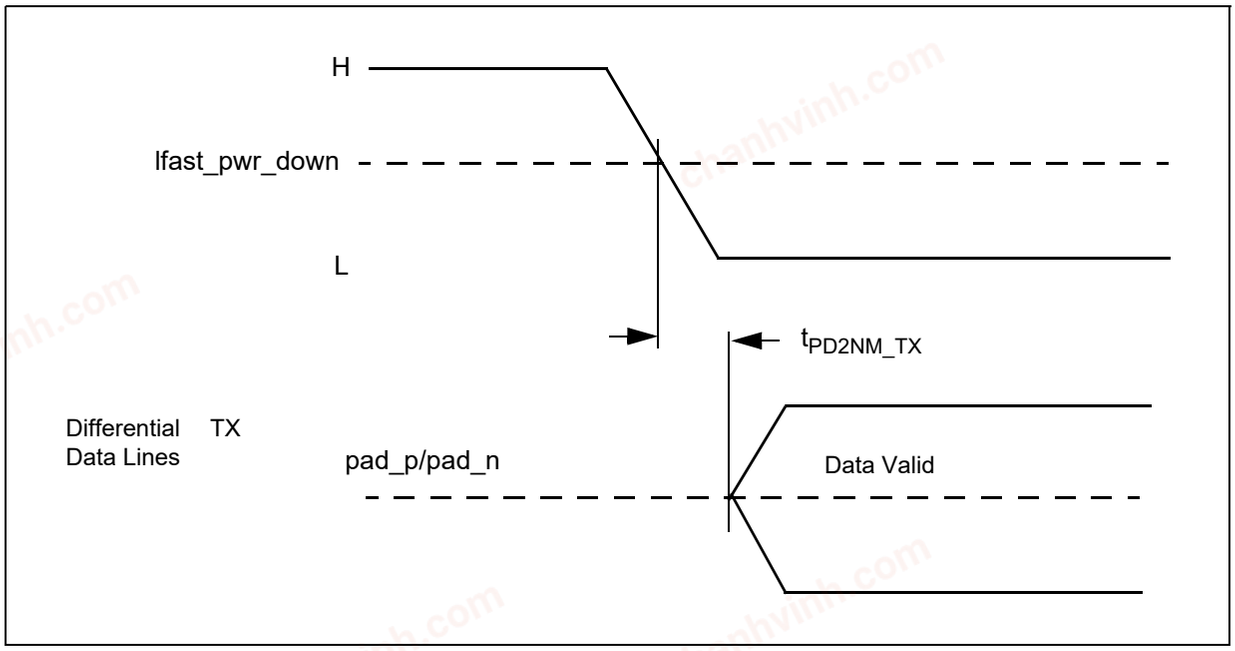
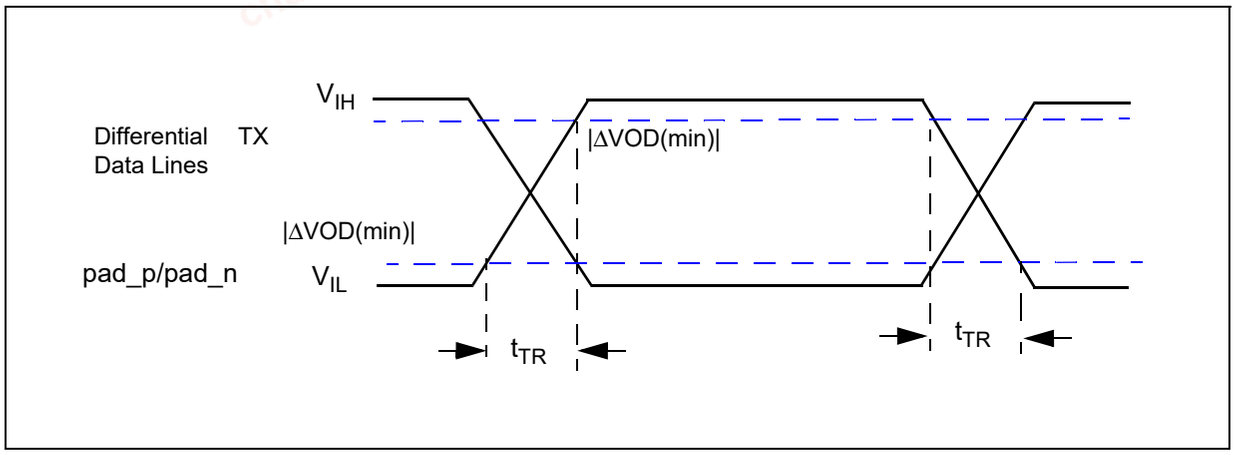


Figure 11. Rise/fall time



4.14.2 LFAST LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 30. LVDS pad startup and receiver electrical characteristics

Symbol[1],[2]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
STARTUP[3],[4]								
t_{STRT_BIAS}	CC	T	Bias current reference startup time[5]	—	—	0.5	4	µs
t_{PD2NM_TX}	CC	T	Transmitter startup time (power down to normal mode)[6]	—	—	0.4	2.75	µs

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Table 30. LVDS pad startup and receiver electrical characteristics (continued)

Symbol[1],[2]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{SM2NM_TX}	CC	T	Transmitter startup time (sleep mode to normal mode)[7]	Not applicable to the MSC/DSPI LVDS pad	—	0.4	0.6	µs
t_{PD2NM_RX}	CC	T	Receiver startup time (power down to normal mode)[8]	—	—	20	40	ns
t_{PD2SM_RX}	CC	T	Receiver startup time (power down to sleep mode)[9]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	CC	D	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)								
Z_0	SR	D	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	SR	D	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER								
V_{ICOM}	SR	T	Common mode voltage	—	0.15 (10)	—	1.6[11]	V
$\|\Delta_{VI}\|$	SR	T	Differential input voltage[12]	—	100	—	—	mV
V_{HYS}	CC	T	Input hysteresis	—	25	—	—	mV
R_{IN}	CC	D	Terminating resistance	$V_{DD_HV_IO}$ = 5.0 V ± 10% -40 °C < T_J < 150 °C	80	—	150	Ω
				$V_{DD_HV_IO}$ = 3.3 V ± 10% -40 °C < T_J < 150 °C	80	—	175	
C_{IN}	CC	D	Differential input capacitance[13]	—	—	3.5	6.0	pF
I_{LVDS_RX}	CC	C	Receiver DC current consumption	Enabled	—	—	1.6	mA
I_{PIN_RX}	CC	D	Maximum consumption on receiver input pin	Δ_{VI} = 400 mV, R_{IN} = 80 Ω	—	—	5	mA

1. The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST & High-speed Debug (HSD) LVDS pad.
2. All LVDS pad electrical characteristics are valid from -40 °C to 150 °C.
3. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-speed Debug modules. The value of the LCR bits for the LFAST/HSD modules don't take effect until the corresponding SIUL2 MSCR ODC bits are set to LFAST LVDS mode. Startup times for MSC/DSPI LVDS are defined after 2 peripheral bridge clock delay after selecting MSC/DSPI LVDS in the corresponding SIUL2 MSCR ODC field.
4. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
5. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
6. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
7. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.

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8. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
9. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
10. Absolute min = 0.15 V – (285 mV/2) = 0 V
11. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
12. Value valid for LFAST mode. The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing.
13. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions.

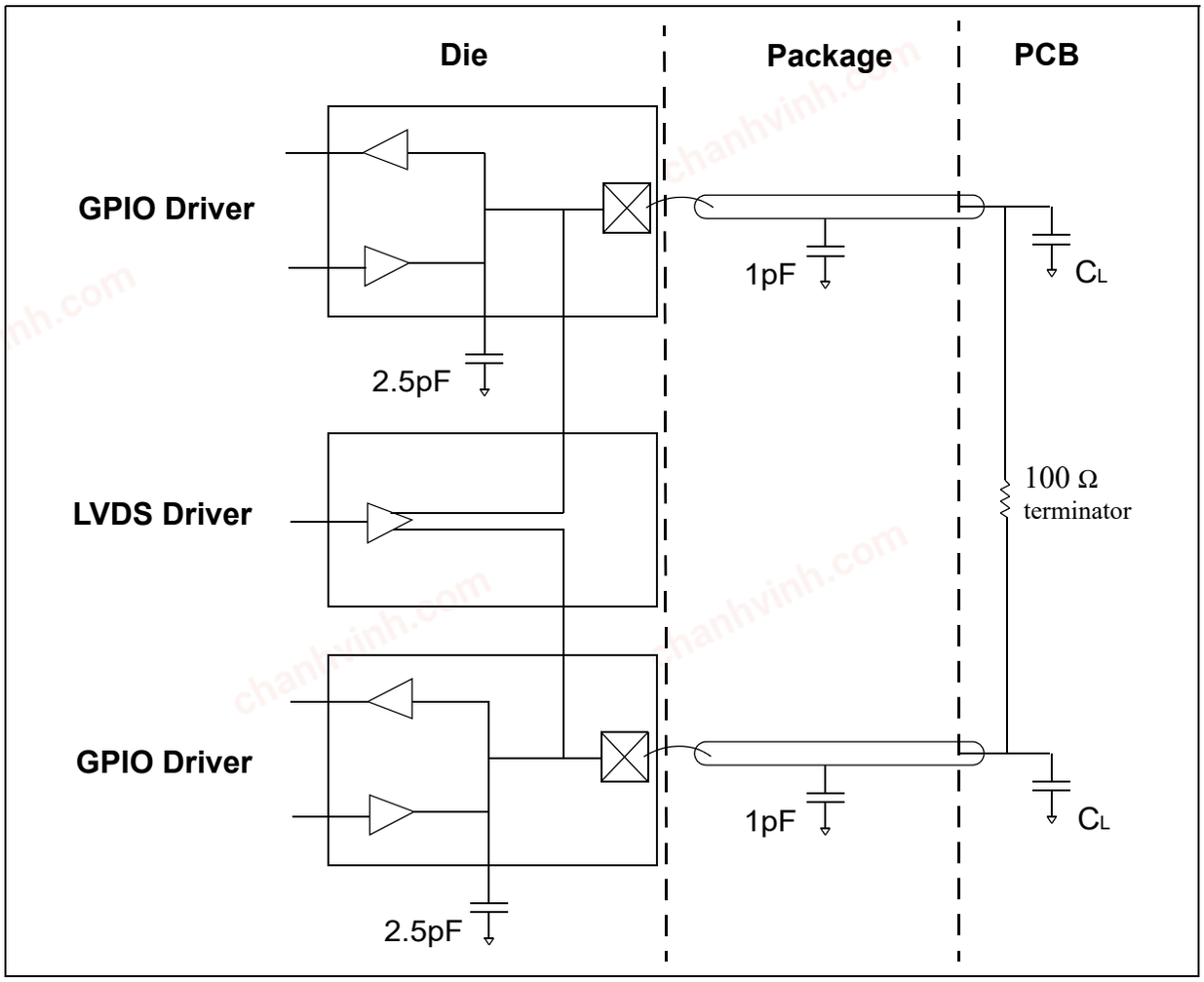
Table 31. LFAST transmitter electrical characteristics

Symbol[1],[2],[3]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{DATA}	SR	D	Data rate	—	—	—	320	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|\Delta_{VOD}\|$	CC	P	Differential output voltage swing (terminated)[4],[5]	—	110	—	285	mV
t_{TR}	CC	T	Rise time from -|ΔVOD(min)| to +|ΔVOD(min)|. Fall time from +|ΔVOD(min)| to -|ΔVOD(min)|	—	0.26	—	1.25	ns
C_L	SR	D	External lumped differential load capacitance[4]	$V_{DD_HV_IO}$ = 4.5 V	—	—	6.0	pF
				$V_{DD_HV_IO}$ = 3.0 V	—	—	4.0	
I_{LVDS_TX}	CC	C	Transmitter DC current consumption	Enabled	—	—	3.6	mA
I_{PIN_TX}	CC	D	Transmitter DC current sourced through output pin	—	1.1		2.85	mA

1. This table is applicable to LFAST LVDS pads used in LFAST configuration (SIUL2_MSCR_IO_n.ODC=101).
2. The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values shown in *Figure 12*.
3. All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from -40 °C to 150 °C.
4. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 12*.
5. Valid for maximum external load C_L.

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Figure 12. LVDS pad external load diagram



4.14.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

Table 32. LFAST PLL electrical characteristics

Symbol[1]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{RF_REF}	SR	D	PLL reference clock frequency (CLKIN)	—	10[2]	—	30	MHz
ERR_{REF}	CC	D	PLL reference clock frequency error	—	-1	—	1	%
DC_{REF}	CC	D	PLL reference clock duty cycle (CLKIN)	—	30	—	70	%
PN	CC	D	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	-58	dBc
f_{VCO}	CC	P	PLL VCO frequency	—	312	—	320[3]	MHz
t_{LOCK}	CC	D	PLL phase lock	—	—	—	150[4]	µs

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Table 32. LFAST PLL electrical characteristics (continued)

Symbol[1]		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
ΔPER_{REF}	SR	T	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 20 MHz	—	—	350	ps
		T		Long term, f_{RF_REF} = 20 MHz	-500	—	500	ps
ΔPER_{EYE}	CC	T	Output Eye Jitter (peak to peak)[5]	—	—	—	400	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.
2. If the input frequency is lower than 20 MHz, it is required to set a input division factor of 1.
3. The 320 MHz frequency is achieved with a 20 MHz reference clock.
4. The total lock time is the sum of the coarse lock time plus the programmable lock delay time 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device (to set the PLL enable bit).
5. Measured at the transmitter output across a 100 Ω termination resistor on a device evaluation board. See *Figure 12*.

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4.15 Power management

The power management module monitors the different power supplies as well as it generates the required internal supplies. The device can operate in the following configurations:

Table 33. Power management regulators

Device	External regulator	Internal SMPS regulator	Internal linear regulator external ballast	Internal linear regulator internal ballast	Auxiliary regulator	Clamp regulator	Internal standby regulator(1)
SPC584Cx SPC58ECx	—	—	X	X(2)	X	X	X

1. Standby regulator is automatically activated when the device enters standby mode.
2. The operability of the device with internal ballast can be limited by the maximum thermal dissipation of the device in the application. The internal ballast option is available only on specific devices, contact the local sales.

4.15.1 Power management integration

Use the integration schemes provided below to ensure the proper device function, according to the selected regulator configuration.

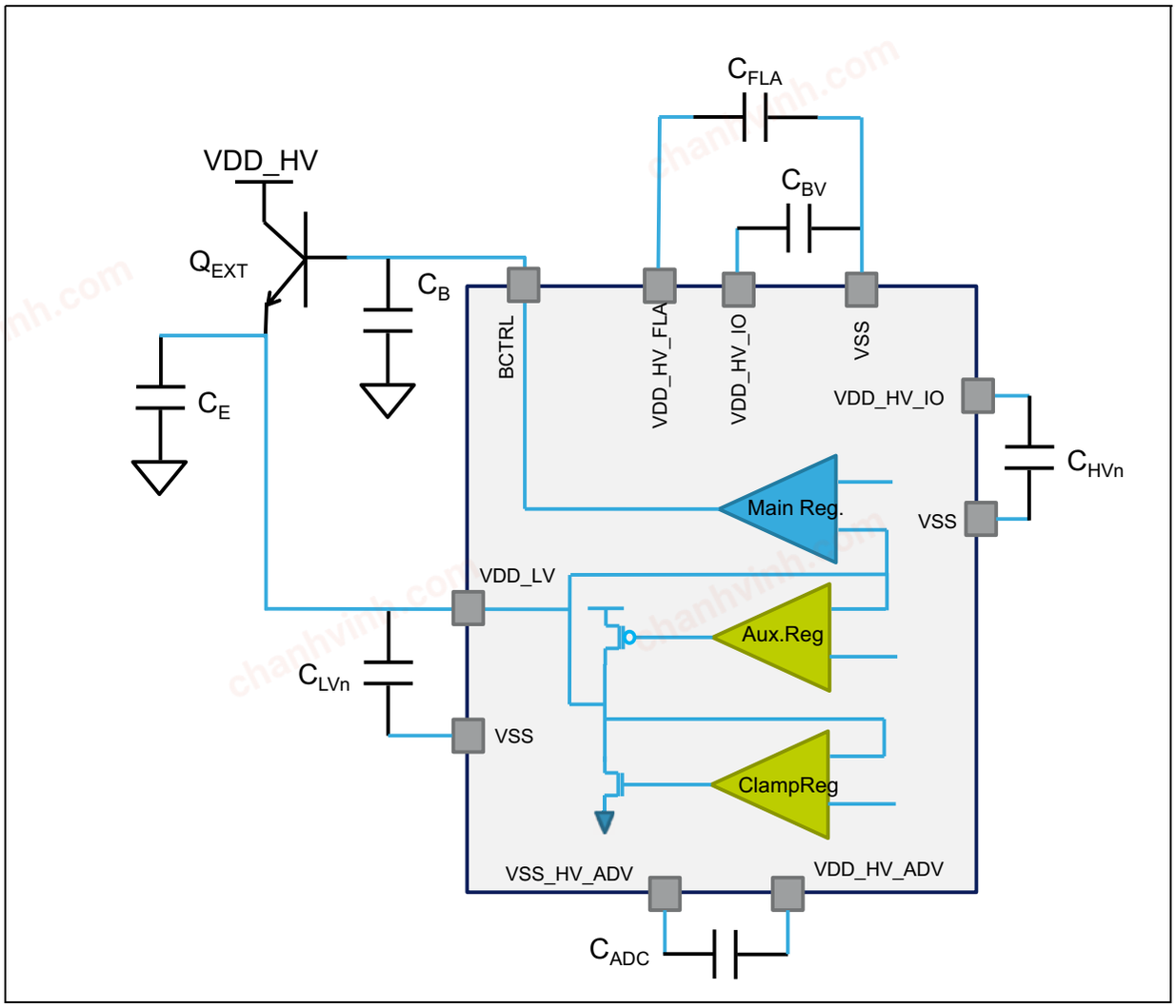
The internal regulators are supplied by $V_{DD_HV_IO_MAIN}$ supply and are used to generate V_{DD_LV} supply.

Place capacitances on the board as near as possible to the associated pins and limit the serial inductance of the board to less than 5 nH.

It is recommended to use the internal regulators only to supply the device itself.

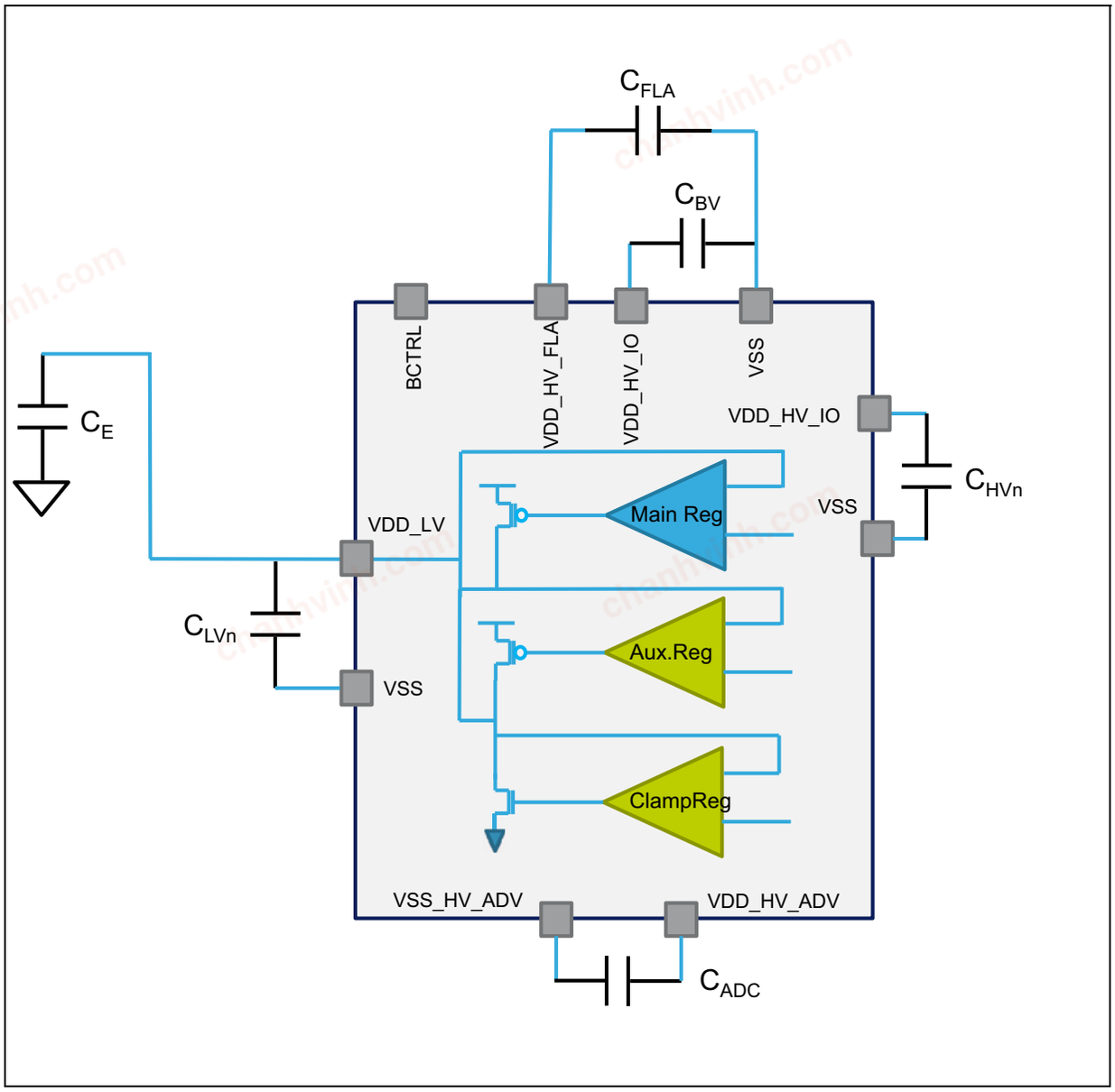
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Figure 13. Internal regulator with external ballast mode



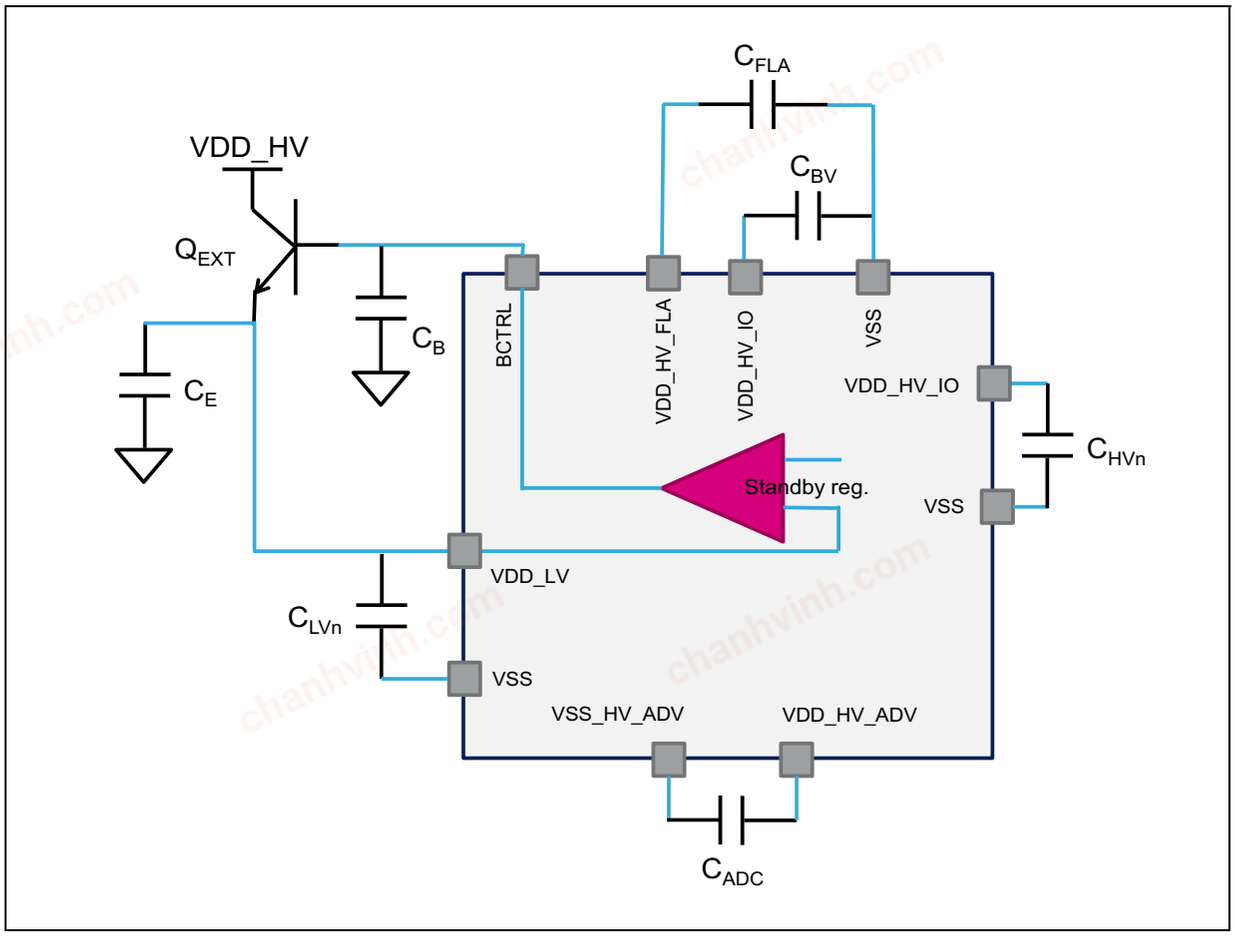
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Figure 14. Internal regulator with internal ballast mode



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Figure 15. Standby regulator with external ballast mode



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Figure 16. Standby regulator with internal ballast mode

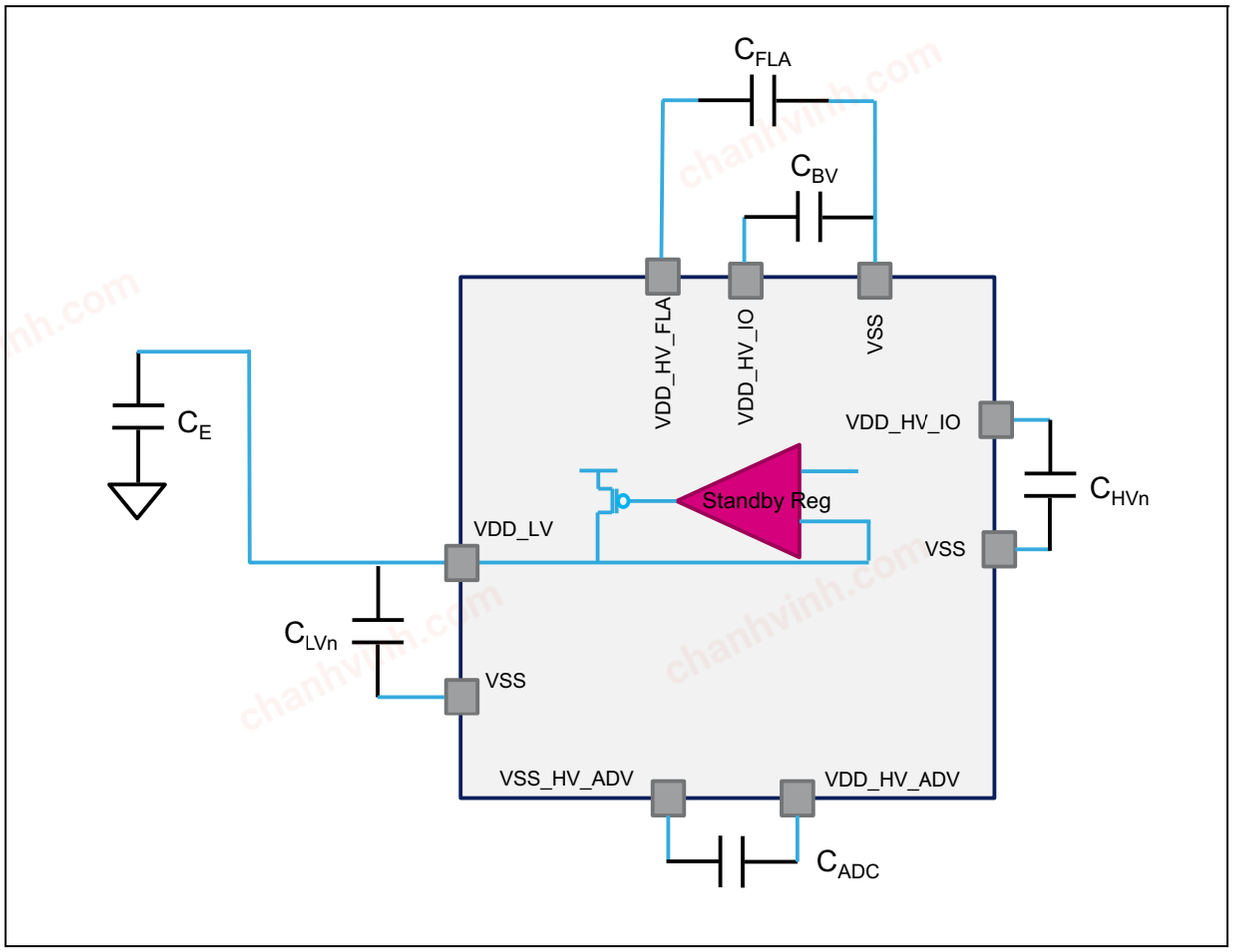


Table 34. External components integration

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
Common Components								
C_E	SR	D	Internal voltage regulator stability external capacitance[2] [3]	—	1.1	2.2	3.0	µF
R_E	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	5	—	50	mΩ
C_{LVn}	SR	D	Internal voltage regulator decoupling external capacitance [2] [4] [5]	Each V_{DD_LV}/V_{SS} pair	—	100	—	nF
R_{LVn}	SR	D	Stability capacitor equivalent serial resistance	—	—	—	50	mΩ
C_{BV}	SR	D	Bulk capacitance for HV supply [2]	on one $V_{DD_HV_IO_MAIN}/V_{SS}$ pair	—	4.7	—	µF
C_{HVn}	SR	D	Decoupling capacitance for ballast and IOs [2]	on all $V_{DD_HV_IO}/V_{SS}$ and $V_{DD_HV_ADR}/V_{SS}$ pairs	—	100	—	nF

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Table 34. External components integration (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{FLA}	SR	D	Decoupling capacitance for Flash supply [2][6]	—	—	10	—	nF
C_{ADC}	SR	D	ADC supply external capacitance[2] [6]	$V_{DD_HV_ADV}/V_{SS_HV_ADV}$ pair	—	1.5	—	µF
Internal Linear Regulator with External Ballast Mode								
Q_{EXT}	SR	D	Recommended external NPN transistors	NJD2873T4, BCP68, 2SCR574D				
V_Q	SR	D	External NPN transistor collector voltage	—	2.0	—	$V_{DD_HV_IO_MAIN}$	V
C_B	SR	D	Internal voltage regulator stability external capacitance on ballast base [2] [7]	—	—	2.2	—	µF
R_B	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	5	—	50	mΩ

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_J = –40 / 150 °C, unless otherwise specified.
2. Recommended X7R or X5R ceramic –50% / +35% variation across process, temperature, voltage and after aging.
3. CE capacitance is required both in internal and external ballast mode.
4. For noise filtering, add a high frequency bypass capacitance of 10 nF.
5. For applications it is recommended to implement at least 5 C_{LV} capacitances.
6. Recommended X7R capacitors. For noise filtering, add a high frequency bypass capacitance of 100 nF.
7. CB capacitance is required if only the external ballast is implemented.

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4.15.2 Voltage regulators

Table 35. Linear regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{MREG}	CC	P	Main regulator output voltage	Power-up, before trimming, no load	1.14	1.22	1.30	V
	CC	P		After trimming, maximum load	1.09	1.19	1.24	
IDD_{MREG}	CC	T	Main regulator current provided to V_{DD_LV} domain The maximum current supported is the sum of the Main Regulator and the Auxiliary Regulator maximum current both regulators are working in parallel.	Internal ballast	—	—	325	mA
				External ballast	—	—	450	
IDD_{CLAMP}	CC	D	Main regulator rush current sinked from $V_{DD_HV_IO_MAIN}$ domain during V_{DD_LV} domain loading	Power-up condition	—	—	150	mA
ΔIDD_{MREG}	CC	T	Main regulator output current variation	20 µs observation window	-100	—	100	mA
$I_{MREGINT}$	CC	D	Main regulator current consumption	I_{MREG} = max	—	—	17	mA
		D		I_{MREG} = 0 mA	—	—	—	

Table 36. Auxiliary regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{AUX}	CC	P	Aux regulator output voltage	After trimming, internal regulator mode	1.09	1.19	1.22	V
IDD_{AUX}	CC	T	Aux regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
ΔIDD_{AUX}	CC	T	Aux regulator current variation	20 µs observation window	-100	—	100	mA
I_{AUXINT}	CC	D	Aux regulator current consumption	I_{MREG} = max	—	—	1.1	mA
		D		I_{MREG} = 0 mA	—	—	1.1	

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Table 37. Clamp regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{CLAMP}	CC	P	Clamp regulator output voltage	After trimming, internal regulator mode	1.18	1.22	1.33	V
ΔIDD_{CLAMP}	CC	T	Clamp regulator current variation	20 µs observation window	-100	—	100	mA
$I_{CLAMPINT}$	CC	D	Clamp regulator current consumption	I_{MREG} = 0 mA	—	—	0.7	mA

Table 38. Standby regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{SBY}	CC	P	Standby regulator output voltage	After trimming, maximum load	1.02	1.06	1.26	V
IDD_{SBY}	CC	T	Standby regulator current provided to V_{DD_LV} domain	External Ballast	—	—	50	mA
				Internal Ballast	—	—	10	

4.15.3 Voltage monitors

The monitors and their associated levels for the device are given in *Table 39*. *Figure 17* illustrates the workings of voltage monitoring threshold.

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Figure 17. Voltage monitor threshold definition

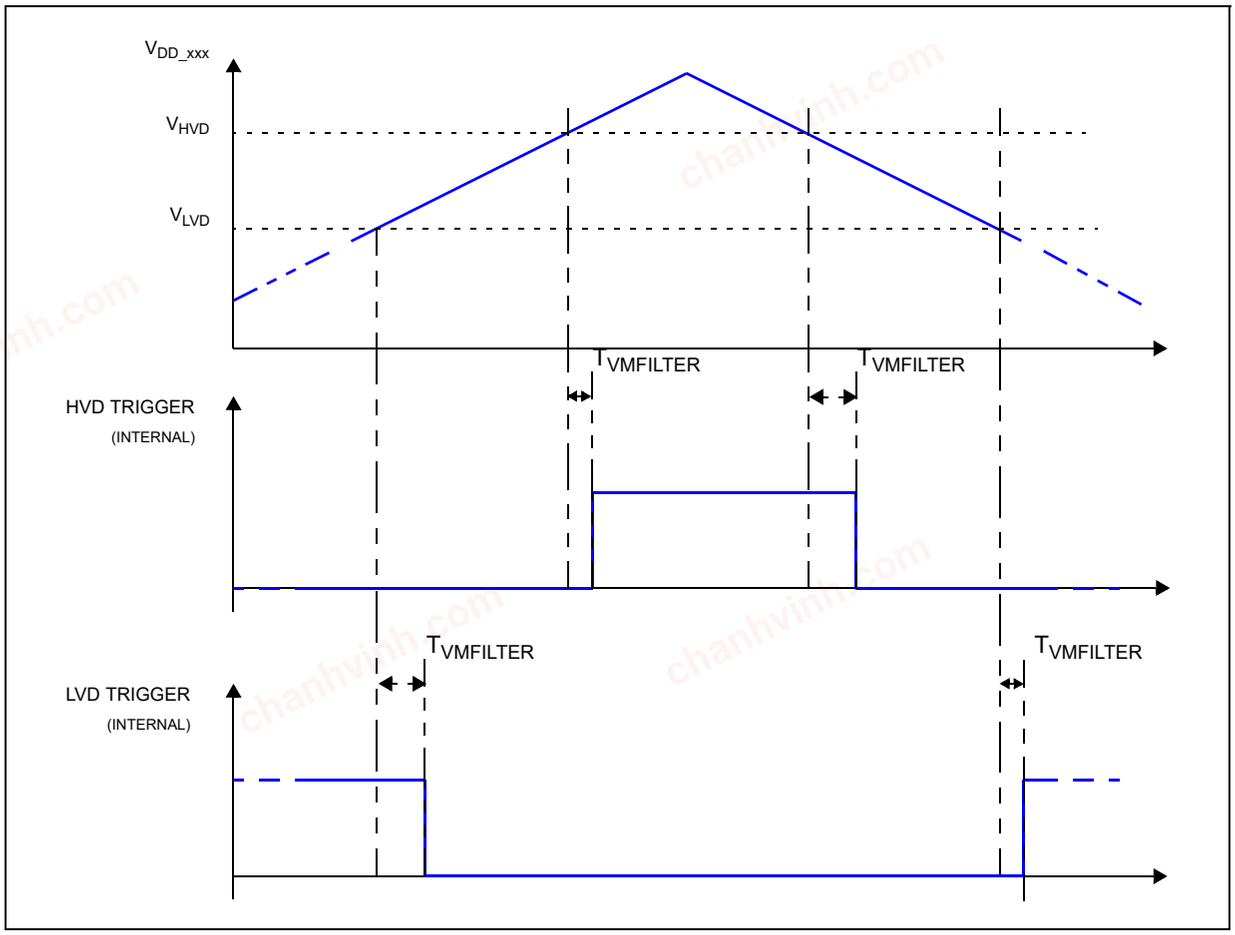


Table 39. Voltage monitor electrical characteristics

Symbol	C		Supply/Parameter[1]	Conditions	Value[2]			Unit
					Min	Typ	Max	
PowerOn Reset HV								
V_{POR200_C}	CC	P	$V_{DD_HV_IO_MAIN}$	—	1.80	2.18	2.40	V
Minimum Voltage Detectors HV								
V_{MVD270_C}	CC	P	$V_{DD_HV_IO_MAIN}$	—	2.71	2.76	2.80	V
V_{MVD270_F}	CC	P	$V_{DD_HV_FLA}$	—	2.71	2.76	2.80	V
V_{MVD270_SBY}	CC	P	$V_{DD_HV_IO_MAIN}$ (in Standby)	—	2.68	2.76	2.84	V
Low Voltage Detectors HV								
V_{LVD290_C}	CC	P	$V_{DD_HV_IO_MAIN}$	—	2.89	2.94	2.99	V
V_{LVD290_F}	CC	P	$V_{DD_HV_FLA}$	—	2.89	2.94	2.99	V
V_{LVD290_AS}	CC	P	$V_{DD_HV_ADV}$ (ADCSAR pad)	—	2.89	2.94	2.99	V
V_{LVD290_IF}	CC	P	$V_{DD_HV_IO_FLEX}$	—	2.89	2.94	2.99	V
V_{LVD400_AS}	CC	P	$V_{DD_HV_ADV}$ (ADCSAR pad)	—	4.15	4.23	4.31	V

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Table 39. Voltage monitor electrical characteristics (continued)

Symbol		C	Supply/Parameter[1]	Conditions	Value[2]			Unit
					Min	Typ	Max	
V_{LVD400_IM}	CC	P	$V_{DD_HV_IO_MAIN}$	—	4.15	4.23	4.31	V
V_{LVD400_IF}	CC	P	$V_{DD_HV_IO_FLEX}$	—	4.15	4.23	4.31	V
High Voltage Detectors HV								
V_{HVD400_IF}	CC	P	$V_{DD_HV_IO_FLEX}$	—	3.68	3.75	3.82	V
Upper Voltage Detectors HV								
V_{UVD600_F}	CC	P	$V_{DD_HV_FLA}$	—	5.72	5.82	5.92	V
V_{UVD600_IF}	CC	P	$V_{DD_HV_IO_FLEX}$	—	5.72	5.82	5.92	V
PowerOn Reset LV								
V_{POR031_C}	CC	P	V_{DD_LV}	—	0.29	0.60	0.97	V
Minimum Voltage Detectors LV								
V_{MVD082_C}	CC	P	V_{DD_LV}	—	0.85	0.88	0.91	V
V_{MVD094_C}	CC	P	V_{DD_LV}	—	0.98	1.00	1.02	V
V_{MVD094_FA}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V
V_{MVD094_FB}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V
Low Voltage Detectors LV								
V_{LVD100_C}	CC	P	V_{DD_LV}	—	1.06	1.08	1.11	V
V_{LVD100_SB}	CC	P	V_{DD_LV} (In Standby)	—	0.99	1.01	1.03	V
V_{LVD100_F}	CC	P	V_{DD_LV} (Flash)	—	1.08	1.10	1.12	V
High Voltage Detectors LV								
V_{HVD134_C}	CC	P	V_{DD_LV}	—	1.28	1.31	1.33	V
Upper Voltage Detectors LV								
V_{UVD140_C}	CC	P	V_{DD_LV}	—	1.34	1.37	1.39	V
V_{UVD140_F}	CC	P	V_{DD_LV} (Flash)	—	1.34	1.37	1.39	V
Common								
$T_{VMFILTER}$	CC	D	Voltage monitor filter[3]	—	5	—	25	µs

1. Even if LVD/HVD monitor reaction is configurable, the application ensures that the device remains in the operative condition range, and the internal LVDx monitors are disabled by the application. Then an external voltage monitor with minimum threshold of VDD_LV(min) = 1.08 V measured at the device pad, has to be implemented.
For HVDx, if the application disables them, then they need to grant that VDD_LV and VDD_HV voltage levels stay withing the limitations provided in *Section 4.2: Absolute maximum ratings*.
2. The values reported are Trimmed values, where applicable.
3. See *Figure 17*. Transitions shorter than minimum are filtered. Transitions longer than maximum are not filtered, and will be delayed by $T_{VMFILTER}$ time. Transitions between minimum and maximum can be filtered or not filtered, according to temperature, process and voltage variations.

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4.16 Flash

The following table shows the Wait State configuration.

Table 40. Wait State configuration

APC	RWSC	Frequency range (MHz)
000(1)	0	f≤30
	1	f≤60
	2	f≤90
	3	f≤120
	4	f≤150
	5	f≤180
100(2)	0	f≤30
	1	f≤60
	2	f≤90
	3	f≤120
	4	f≤150
	5	f≤180
001(3)	2	55<f≤80
	3	55<f≤120
	4	55<f≤160
	5	55<f≤180

1. STD pipelined, no address anticipation.
2. No pipeline (STD + 1 Tck).
3. Pipeline with 1 Tck address anticipation.

The following table shows the Program/Erase Characteristics.

Table 41. Flash memory program and erase specifications

Symbol	Characteristics(1)(2)	Value								Unit
		Typ(3)	C	Initial max			Typical end of life(4)	Lifetime max(5)		C	
				25 °C (6)	All temp (7)	C		< 1 K cycles	≤ 250 K cycles		
$t_{dwprogram}$	Double Word (64 bits) program time in Data Flash - EEPROM (partitions 2&3) [Packaged part]	43	C	130	—	—	140	500		C	µs
$t_{pprogram}$	Page (256 bits) program time	72	C	240	—	—	240	1000		C	µs

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Table 41. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1][2]	Value									Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C [6]	All temp [7]	C		< 1 K cycles	≤ 250 K cycles		
$t_{pprogrameep}$	Page (256 bits) program time Data Flash - EEPROM (partitions 2&3) [Packaged part]	83	C	264	—	—	276	1000		C	µs
$t_{qprogram}$	Quad Page (1024 bits) program time	220	C	1040	1200	P	850	2000		C	µs
$t_{qprogrameep}$	Quad Page (1024 bits) program time Data Flash - EEPROM (partitions 2&3) [Packaged part]	245	C	1140	1320	P	978	2000		C	µs
$t_{16kpperase}$	16 KB block pre-program and erase time	190	C	450	500	P	190	1000	—	C	ms
$t_{32kpperase}$	32 KB block pre-program and erase time	260	C	520	600	P	230	1200	—	C	ms
$t_{64kpperase}$	64 KB block pre-program and erase time	390	C	700	750	P	420	1600	—	C	ms
$t_{128kpperase}$	128 KB block pre-program and erase time	670	C	1300	1600	P	800	4000	—	C	ms
$t_{256kpperase}$	256 KB block pre-program and erase time	1050	C	1800	2400	P	1600	4000	—	C	ms
$t_{16kprogram}$	16 KB block program time	25	C	45	50	P	40	1000	—	C	ms
$t_{32kprogram}$	32 KB block program time	50	C	90	100	P	75	1200	—	C	ms
$t_{64kprogram}$	64 KB block program time	100	C	175	200	P	150	1600	—	C	ms
$t_{128kprogram}$	128 KB block program time	200	C	350	430	P	300	2000	—	C	ms
$t_{256kprogram}$	256 KB block program time	400	C	700	850	P	590	4000	—	C	ms
$t_{32kprogrameep}$	Program 32 KB Data Flash - EEPROM (partition 2) [Packaged part]	60	C	105	120	P	110	1750		C	ms
$t_{32keraseeep}$	Erase 32 KB Data Flash - EEPROM (partition 2) [Packaged part]	345	C	700	825	P	800	3600		C	ms
$t_{16kprogrameep}$	Program 16 KB Data Flash - EEPROM (partition 3) [Packaged part]	30	C	52	58	P	64	1750		C	ms
$t_{16keraseeep}$	Erase 16 KB Data Flash - EEPROM (partition 3) [Packaged part]	220	C	495	550	P	400	3600		C	ms

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Table 41. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1][2]	Value									Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C [6]	All temp [7]	C		< 1 K cycles	≤ 250 K cycles		
t_{tr}	Program rate[8]	2.2	C	2.8	3.40	C	2.4	—		C	s/MB
t_{pr}	Erase rate[8]	4.8	C	7.2	9.6	C	6.4	—		C	s/MB
t_{tprfm}	Program rate Factory Mode[8]	1.12	C	1.4	1.6	C	—	—		C	s/MB
t_{erfm}	Erase rate Factory Mode[8]	4.0	C	5.2	5.8	C	—	—		C	s/MB
$t_{ffprogram}$	Full flash programming time[9]	7.5	C	11.9	14.6	P	10.3	—	—	C	s
$t_{fferase}$	Full flash erasing time[9]	18.6	C	28.7	33.0	P	25.2	—	—	C	s
t_{ESRT}	Erase suspend request rate[10]	200	T	—	—	—	—	—		—	µs
t_{PSRT}	Program suspend request rate[10]	30	T	—	—	—	—	—		—	µs
t_{AMRT}	Array Integrity Check - Margin Read suspend request rate	15	T	—	—	—	—	—		—	µs
t_{PSUS}	Program suspend latency[11]	—	—	—	—	—	—	12		T	µs
t_{ESUS}	Erase suspend latency[11]	—	—	—	—	—	—	22		T	µs
t_{AIC0S}	Array Integrity Check (4.0 MB, sequential)[12]	25	T	—	—	—	—	—	—	—	ms
$t_{AIC256KS}$	Array Integrity Check (256 KB, sequential)[12]	1.5	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array Integrity Check (4.0 MB, proprietary)[12]	4.0	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (4.0 MB, sequential)[12]	70	T	—	—	—	—	—	—	—	ms
$t_{MR256KS}$	Margin Read (256 KB, sequential)[12]	4.0	T	—	—	—	—	—	—	—	ms

1. Characteristics are valid both for Data Flash and Code Flash, unless specified in the characteristics column.
2. Actual hardware operation times; this does not include software overhead.
3. Typical program and erase times assume nominal supply values and operation at 25 °C.
4. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
5. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
6. Initial factory condition: < 100 program/erase cycles, 25 °C typical junction temperature and nominal (± 5%) supply voltages.

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7. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, –40 °C < TJ < 150 °C junction temperature and nominal (± 5%) supply voltages.
8. Rate computed based on 256 KB sectors.
9. Only code sectors, not including EEPROM.
10. Time between suspend resume and next suspend. Value stated actually represents Min value specification.
11. Timings guaranteed by design.
12. AIC is done using system clock, thus all timing is dependent on system frequency and number of wait states. Timing in the table is calculated at max frequency.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 42. Flash memory Life Specification

Symbol	Characteristics(1) (2)	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles
$N_{CER128K}$	128 KB CODE Flash endurance	1	—	100	—	Kcycles
$N_{CER256K}$	256 KB CODE Flash endurance	1	—	100	—	Kcycles
	256 KB CODE Flash endurance(3)	10	—	100	—	Kcycles
N_{DER32K}	32 KB DATA EEPROM Flash endurance	250	—	—	—	Kcycles
N_{DER16K}	16 KB HSM DATA EEPROM Flash endurance	100	—	—	—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—	—	—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	20	—	—	—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—	—	—	Years
t_{DR250k}	Minimum data retention Blocks with 100,001 - 250,000 P/E cycles	10	—	—	—	Years

1. Program and erase cycles supported across specified temperature specifications.
2. It is recommended that the application enables the core cache memory.
3. 10K cycles on 4-256 KB blocks is not intended for production. Reduced reliability and degraded erase time are possible.

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4.17 AC Specifications

All AC timing specifications are valid up to 150 °C, except where explicitly noted.

4.17.1 Debug and calibration interface timing

4.17.1.1 JTAG interface timing

Table 43. JTAG pin AC electrical characteristics

#	Symbol		C	Characteristic	Value(1),(2)		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	100	—	ns
2	t_{JDC}	CC	T	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	15(3)	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	CC	D	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	600(4)	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See *Table 44* for functional specifications.
2. JTAG timing specified at $V_{DD_HV_IO_JTAG}$ = 4.0 to 5.5 V and max. loading per pad type as specified in the I/O section of the datasheet.
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

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Figure 18. JTAG test clock input timing

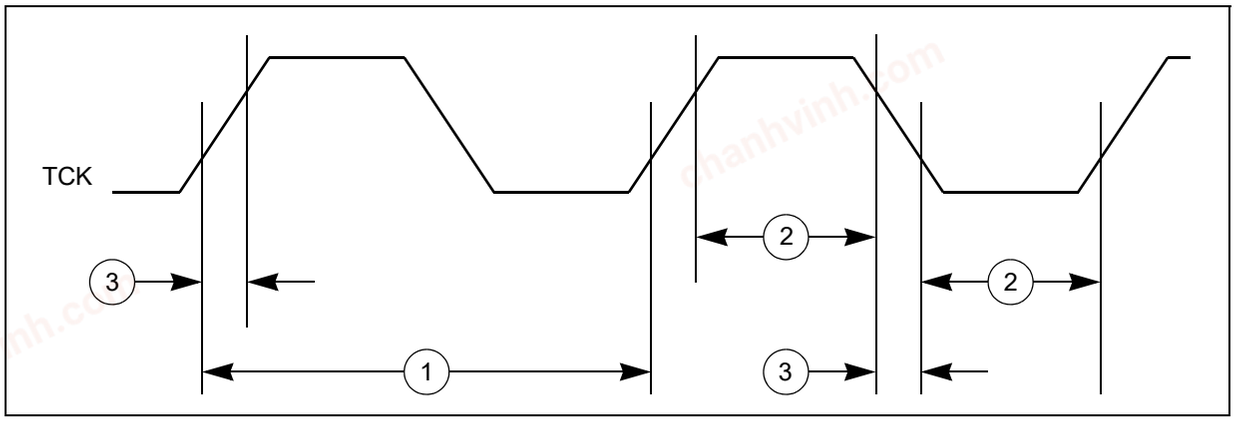
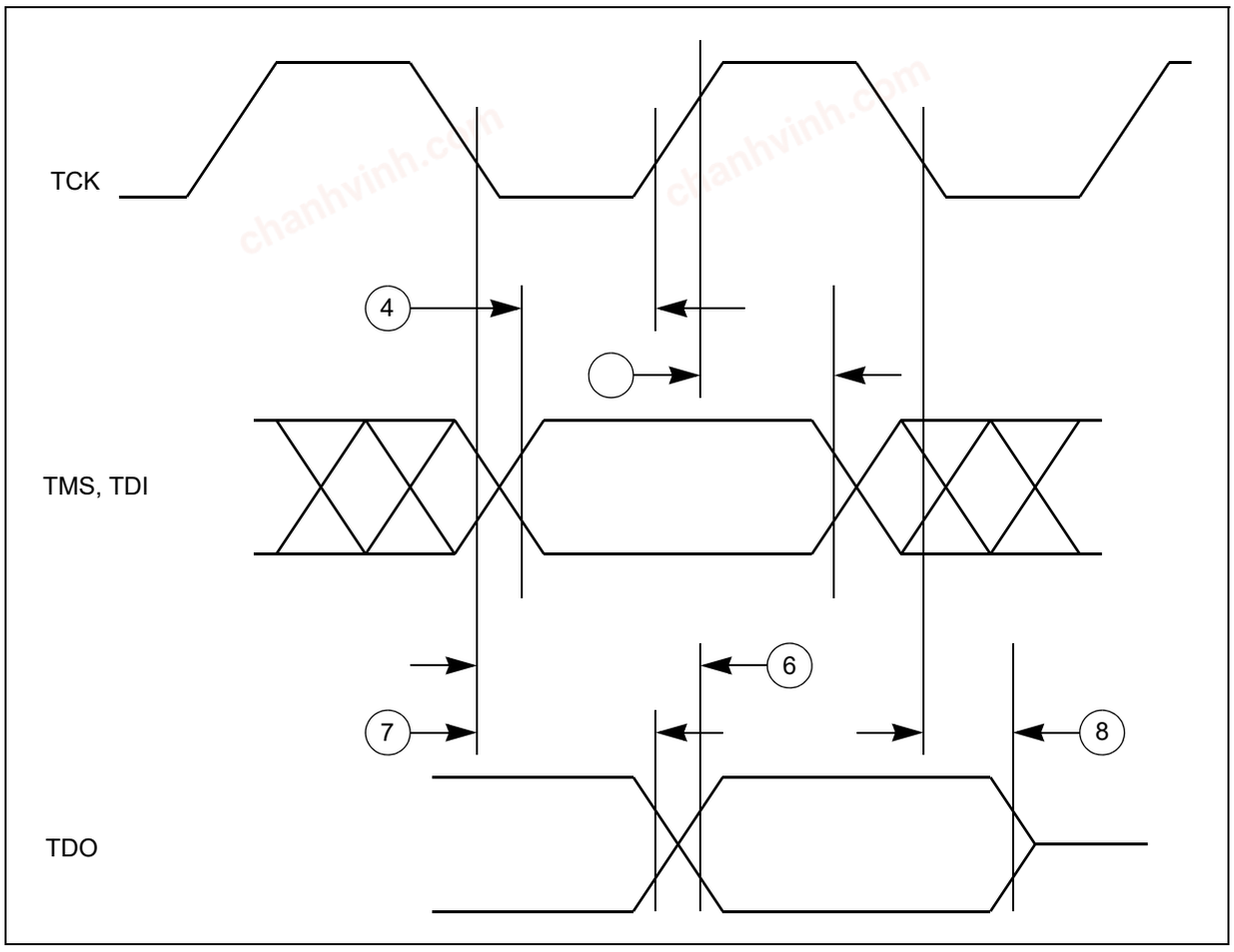


Figure 19. JTAG test access port timing



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Figure 20. JTAG JCOMP timing

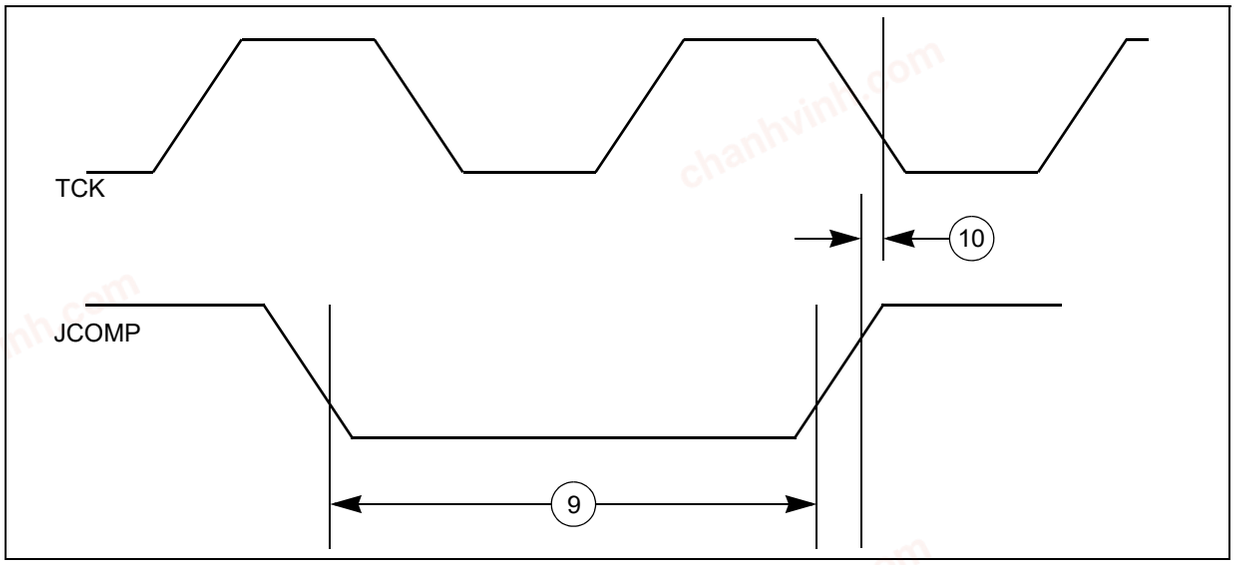
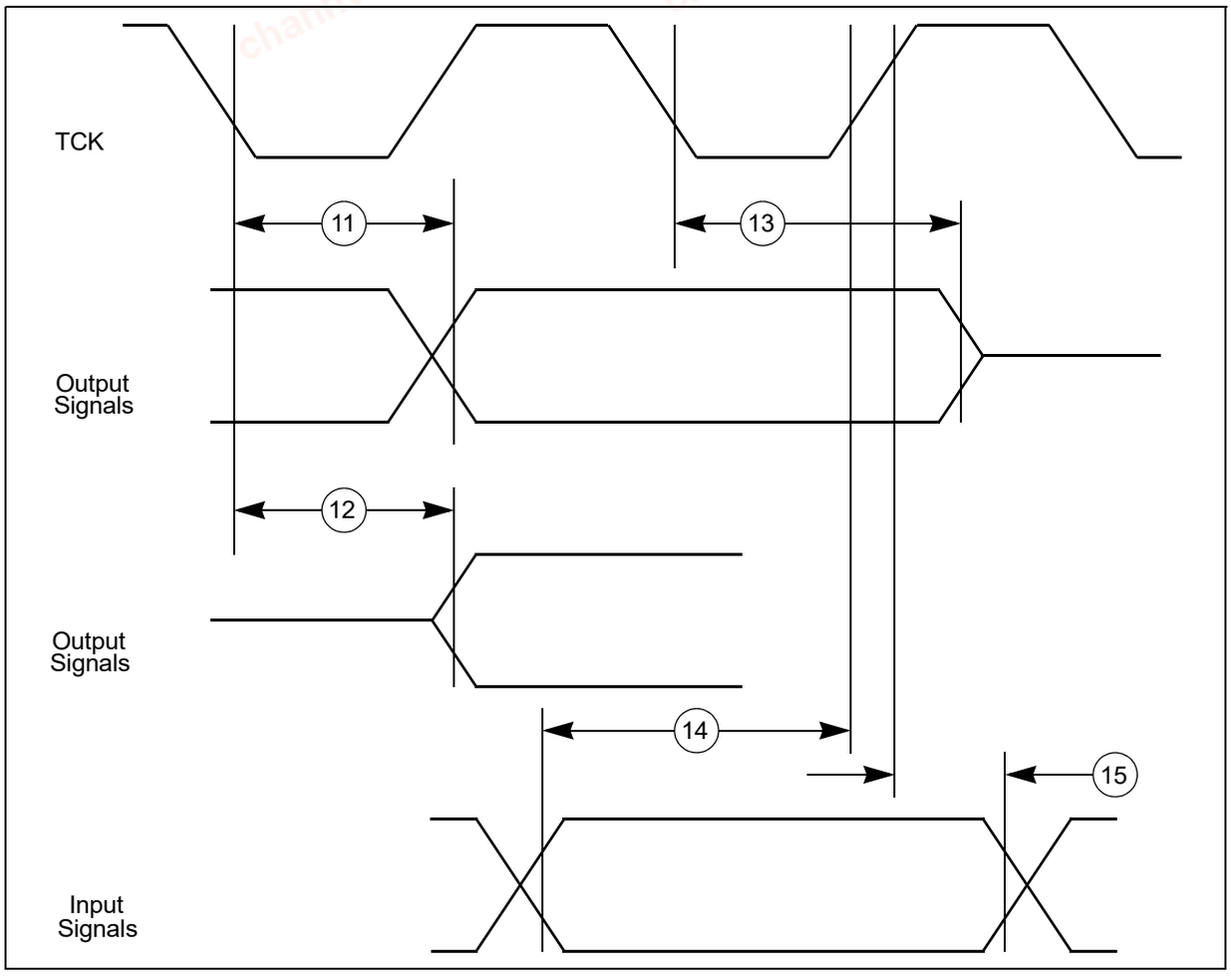


Figure 21. JTAG boundary scan timing



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4.17.1.2 Nexus interface timing

Table 44. Nexus debug port timing

#	Symbol		C	Characteristic	Value(1)		Unit
					Min	Max	
7	t_{EVTIPW}	CC	D	$\overline{EVTI}$ pulse width	4	—	t_{CYC}(2)
8	t_{EVTOPW}	CC	D	$\overline{EVTO}$ pulse width	40	—	ns
9	t_{TCYC}	CC	D	TCK cycle time	2(3),(4)	—	t_{CYC}(2)
				Absolute minimum TCK cycle time(5) (TDO sampled on posedge of TCK)	40(6)	—	ns
				Absolute minimum TCK cycle time(7) (TDO sampled on negedge of TCK)	20(6)	—	
11	t_{NTDIS}	CC	D	TDI data setup time	5	—	ns
12	t_{NTDIH}	CC	D	TDI data hold time	5	—	ns
13	t_{NTMSS}	CC	D	TMS data setup time	5	—	ns
14	t_{NTMSH}	CC	D	TMS data hold time	5	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK(8)	—	16	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	2.25	—	ns

1. Nexus timing specified at $V_{DD_HV_IO_JTAG}$ = 3.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.
2. t_{CYC} is system clock period.
3. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
4. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
5. This value is TDO propagation time 36 ns + 4 ns setup time to sampling edge.
6. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This value is TDO propagation time 16 ns + 4 ns setup time to sampling edge.
8. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

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Figure 22. Nexus output timing

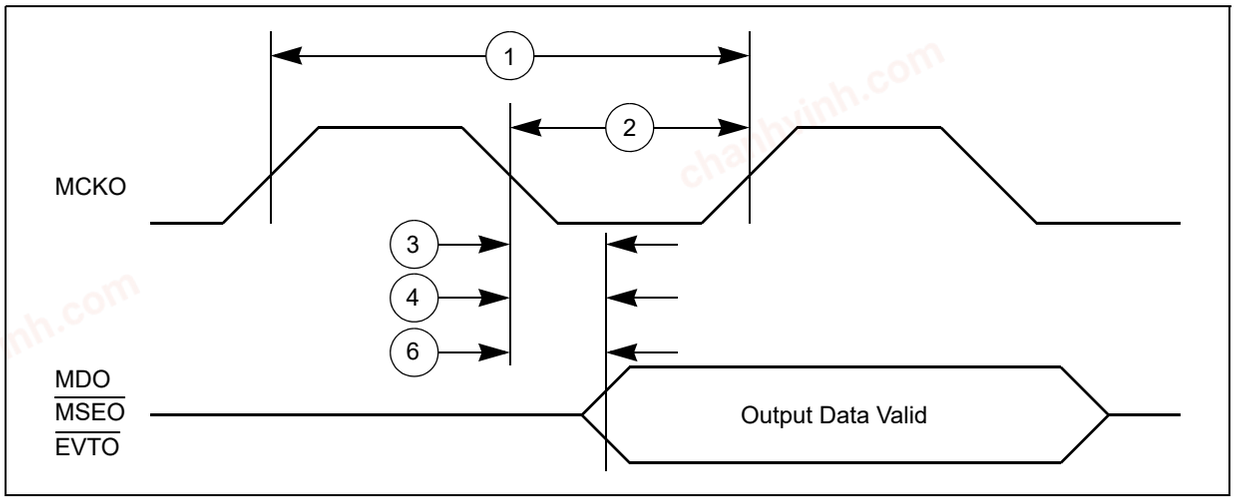
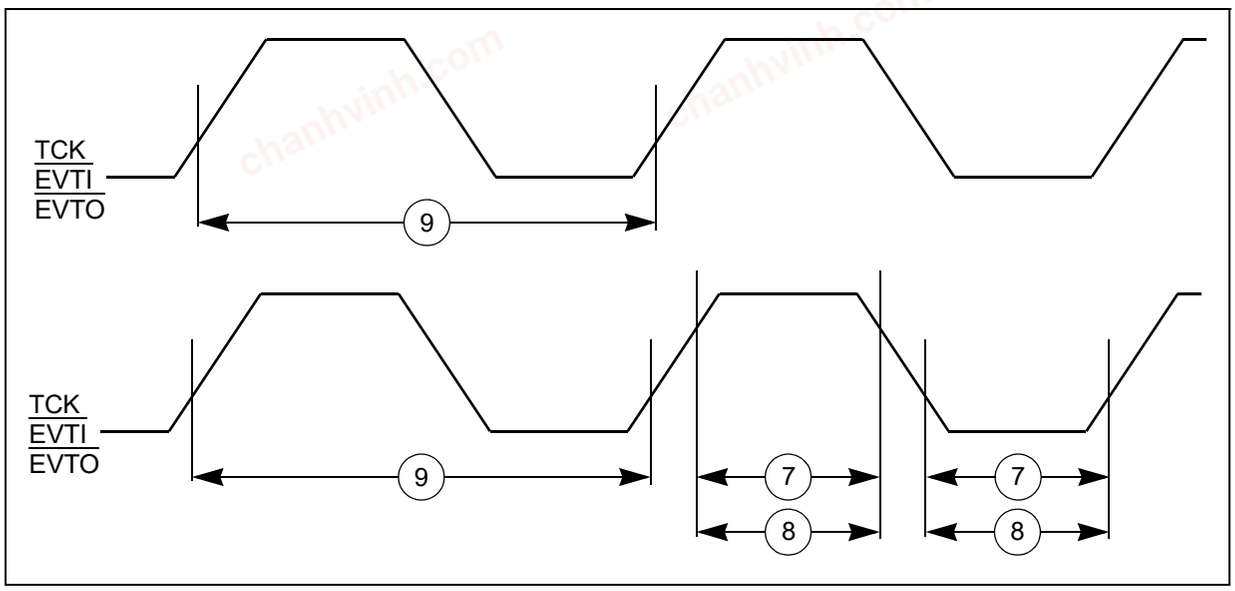
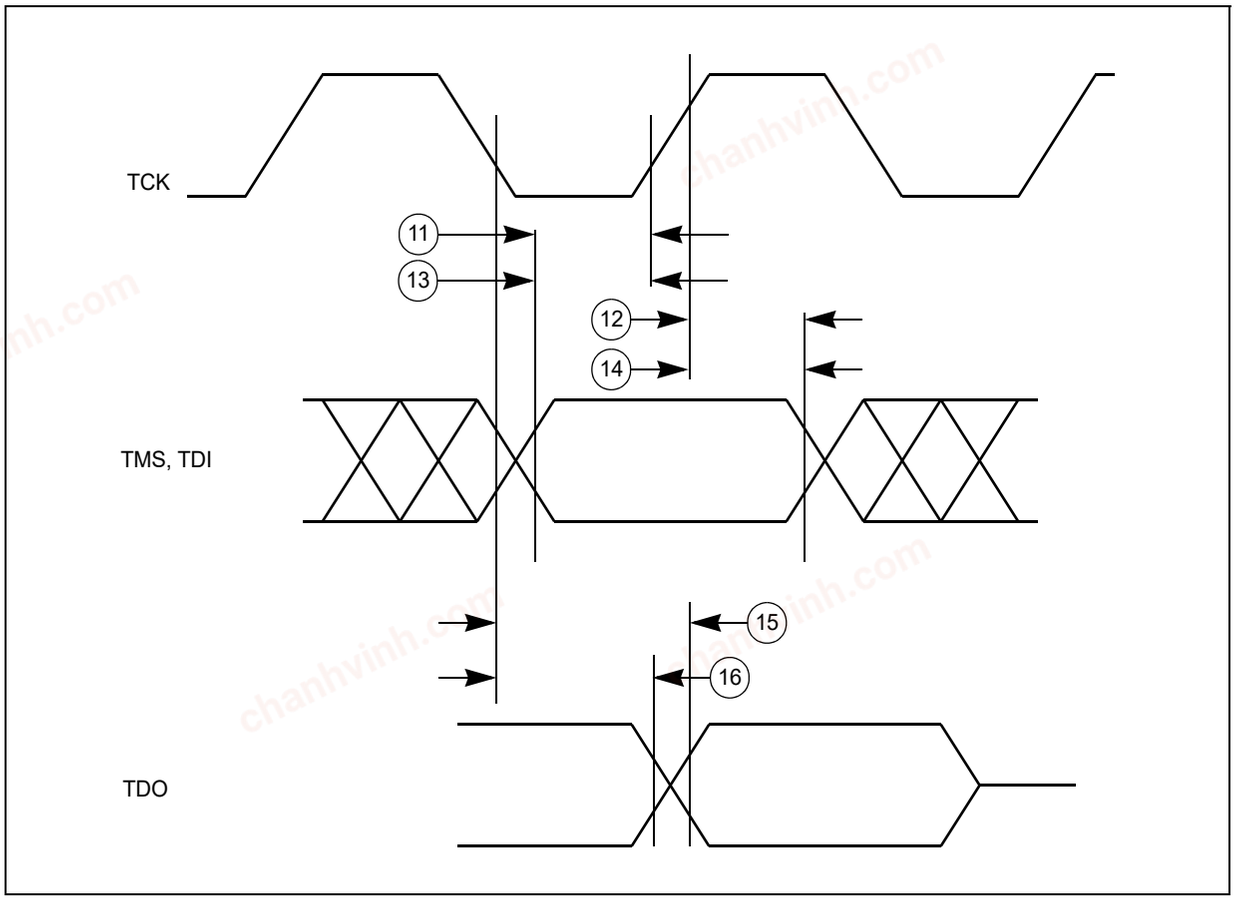


Figure 23. Nexus event trigger and test clock timings



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Figure 24. Nexus TDI, TMS, TDO timing



4.17.1.3 External interrupt timing (IRQ pin)

Table 45. External interrupt timing

Characteristic	Symbol	Min	Max	Unit
IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}
IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}
IRQ Edge to Edge Time(1)	t_{ICYC}	6	—	t_{cyc}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

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Figure 25. External interrupt timing

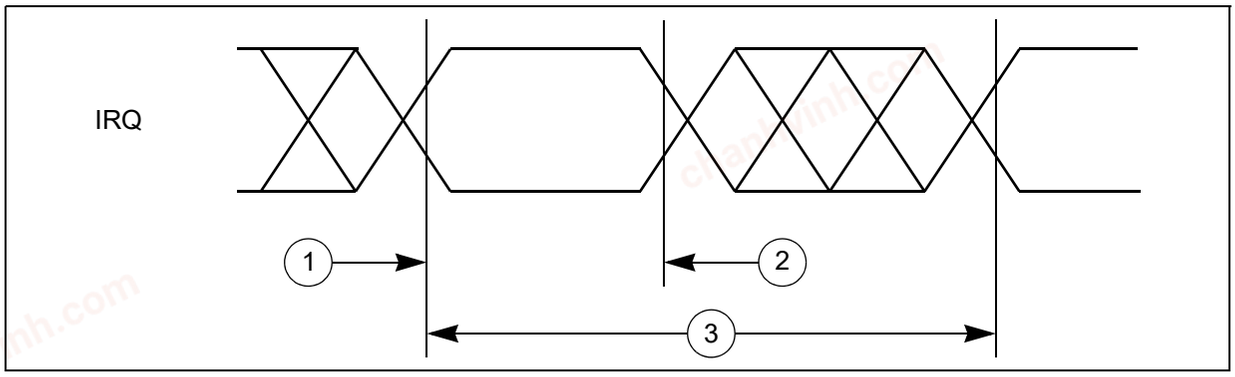
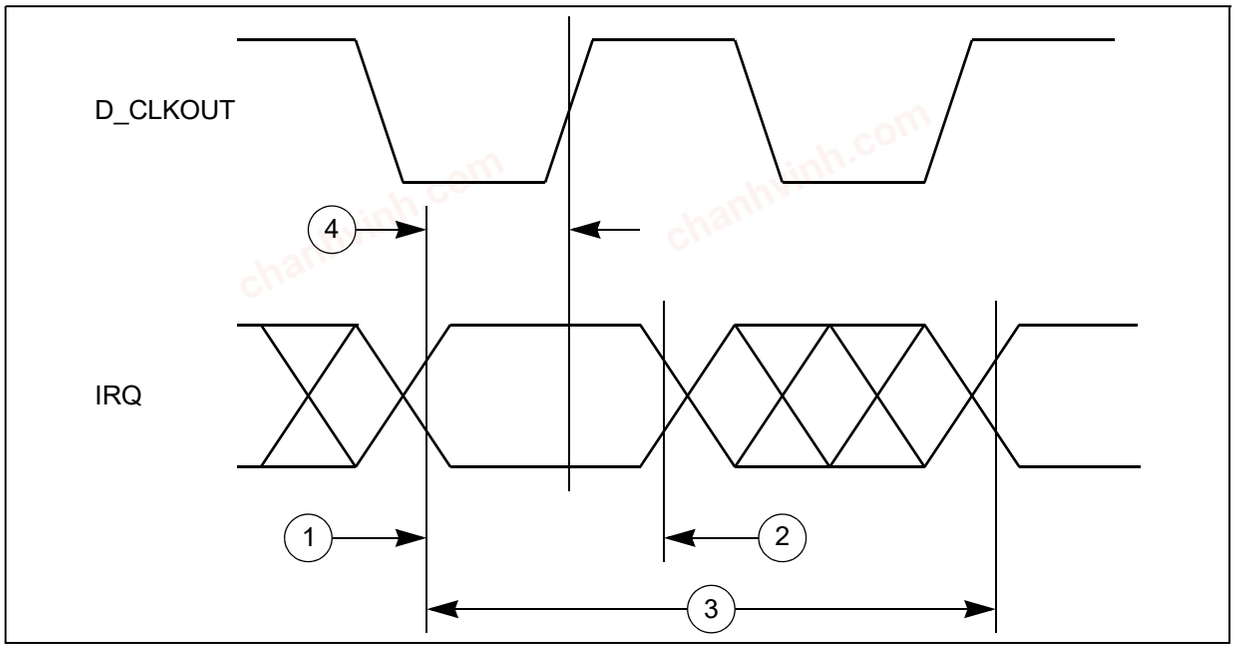


Figure 26. External interrupt timing



4.17.2 DSPI timing with CMOS pads

DSPI channel frequency support is shown in *Table 46*.

Timing specifications are shown in the tables below.

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Table 46. DSPI channel frequency support

DSPI use mode[1]			Max usable frequency (MHz)[2],[3]
CMOS (Master mode)	Full duplex – Classic timing (*Table 47*)	DSPI_0, DSPI_1, DSPI_2, DSPI_3, DSPI_5, DSPI_6, DSPI_7	10
		DSPI_4	17
	Full duplex – Modified timing (*Table 48*)	DSPI_0, DSPI_1, DSPI_2, DSPI_3, DSPI_5, DSPI_6, DSPI_7	10
		DSPI_4	30
	Output only mode (SCK/SOUT/PCS) (*Table 47* and *Table 48*)	DSPI_0, DSPI_1, DSPI_2, DSPI_3, DSPI_5, DSPI_6, DSPI_7	10
		DSPI_4	30
	Output only mode TSB mode (SCK/SOUT/PCS)	DSPI_0, DSPI_1, DSPI_2, DSPI_3, DSPI_5, DSPI_6, DSPI_7	10
		DSPI_4	30
CMOS (Slave mode Full duplex) (*Table 49*)		—	16

1. Each DSPI module can be configured to use different pins for the interface. Refer to the device pinout Microsoft Excel file attached to the IO_Definition document for the available combinations. It is not possible to reach the maximum performance with every possible combination of pins.
2. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
3. Maximum usable frequency does not take into account external device propagation delay.

4.17.2.1 DSPI master mode full duplex timing with CMOS pads

4.17.2.1.1 DSPI CMOS master mode – classic timing

Note: In the following table, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

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Table 47. DSPI CMOS master classic timing (full duplex and output only)
MTFE = 0, CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive(2)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	59.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	ns
					Strong	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	
					Medium	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
4	t_{SDC}	CC	D	SCK duty cycle(6)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time(7)	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time(7)	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns

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Table 47. DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1 (continued)

#	Symbol	C	Characteristic	Condition		Value(1)		Unit
				Pad drive(2)	Load (C_L)	Min	Max	
SIN setup time								
7	t_{SUI}	CC	D	SIN setup time to SCK(8)	SCK drive strength			
				Very strong	25 pF	25.0	—	ns
				Strong	50 pF	31.0	—	
				Medium	50 pF	52.0	—	
SIN hold time								
8	t_{HI}	CC	D	SIN hold time from SCK(8)	SCK drive strength			
				Very strong	0 pF	–1.0	—	ns
				Strong	0 pF	–1.0	—	
				Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	D	SOUT data valid time from SCK(9), (10)	SOUT and SCK drive strength			
				Very strong	25 pF	—	7.0	ns
				Strong	50 pF	—	8.0	
				Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	D	SOUT data hold time after SCK(9)	SOUT and SCK drive strength			
				Very strong	25 pF	–7.7	—	ns
				Strong	50 pF	–11.0	—	
				Medium	50 pF	–15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL voltage thresholds.
9. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

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10. Due to timing delay, a slave could not have enough margin while sampling and only for the following DSPI4 PAD combinations: (SOUT: PAD[63] and SCK: PAD[57] or PAD[137] or PAD[161] or PAD[208]) the Tsuo values have to be increased by 2.5ns. For all the other DSPI pads combinations the Tsuo has to be increased by 1.5ns.

Figure 27. DSPI CMOS master mode — classic timing, CPHA = 0

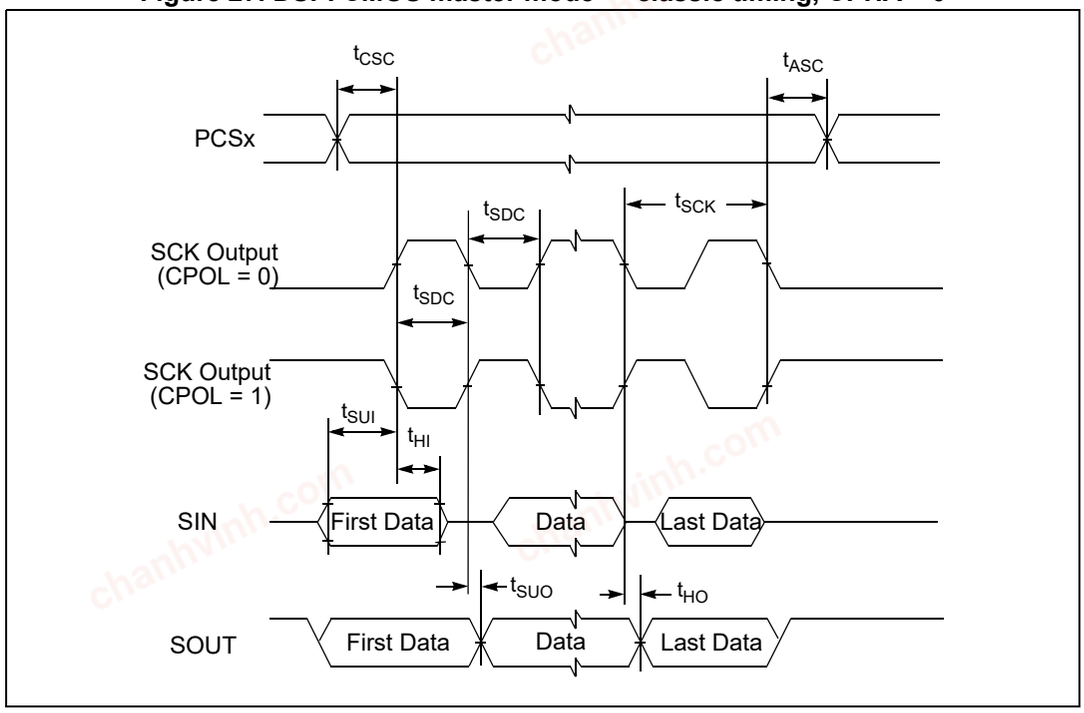
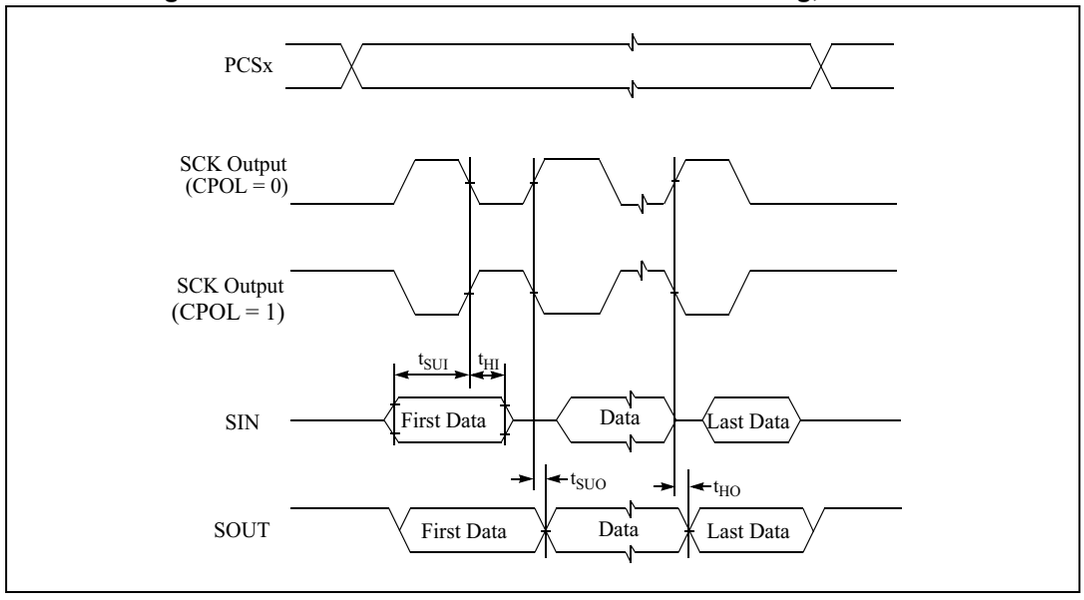
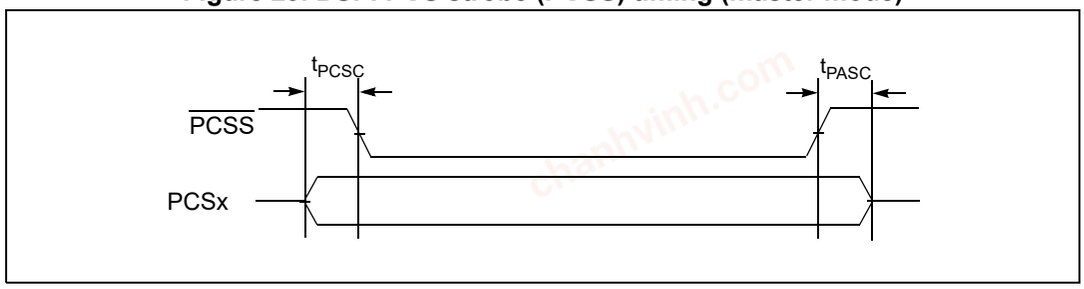


Figure 28. DSPI CMOS master mode — classic timing, CPHA = 1



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Figure 29. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



4.17.2.1.2 DSPI CMOS master mode — modified timing

Note: In the following table, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 48. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive(2)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	ns
					Strong	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	
					Medium	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	

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Table 48. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive[2]	Load (C_L)	Min	Max	
4	t_{SDC}	CC	D	SCK duty cycle[6]	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[7]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[7]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK CPHA = 0[8]	SCK drive strength				
					Very strong	25 pF	$25 - (P^{(9)} \times t_{SYS}^{(4)})$	—	ns
					Strong	50 pF	$31 - (P^{(9)} \times t_{SYS}^{(4)})$	—	
					Medium	50 pF	$52 - (P^{(9)} \times t_{SYS}^{(4)})$	—	
				SIN setup time to SCK CPHA = 1[8]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK CPHA = 0[8]	SCK drive strength				
					Very strong	0 pF	$-1 + (P^{(9)} \times t_{SYS}^{(3)})$	—	ns
					Strong	0 pF	$-1 + (P^{(9)} \times t_{SYS}^{(3)})$	—	
					Medium	0 pF	$-1 + (P^{(9)} \times t_{SYS}^{(3)})$	—	
				SIN hold time from SCK CPHA = 1[8]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	

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Table 48. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol	C	Characteristic	Condition		Value[1]		Unit
				Pad drive[2]	Load (C_L)	Min	Max	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 0[10], [11]	SOUT and SCK drive strength			
					Very strong	25 pF	—	7.0 + t_{SYS}[4]	ns
					Strong	50 pF	—	8.0 + t_{SYS}[4]	
					Medium	50 pF	—	16.0 + t_{SYS}[4]	
				SOUT data valid time from SCK CPHA = 1[10][11]	SOUT and SCK drive strength			
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 0[11]	SOUT and SCK drive strength			
					Very strong	25 pF	–7.7 + t_{SYS}[4]	—	ns
					Strong	50 pF	–11.0 + t_{SYS}[4]	—	
					Medium	50 pF	–15.0 + t_{SYS}[4]	—	
				SOUT data hold time after SCK CPHA = 1[11]	SOUT and SCK drive strength			
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL voltage thresholds.
9. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

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10. Due to timing delay, a slave could not have enough margin while sampling and only for the following DSPI4 PAD combinations: (SOUT: PAD[63] and SCK: PAD[57] or PAD[137] or PAD[161] or PAD[208]) the Tsuo values have to be increased by 2.5ns. For all the other DSPI pads combinations the Tsuo has to be increased by 1.5ns.
11. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 30. DSPI CMOS master mode — modified timing, CPHA = 0

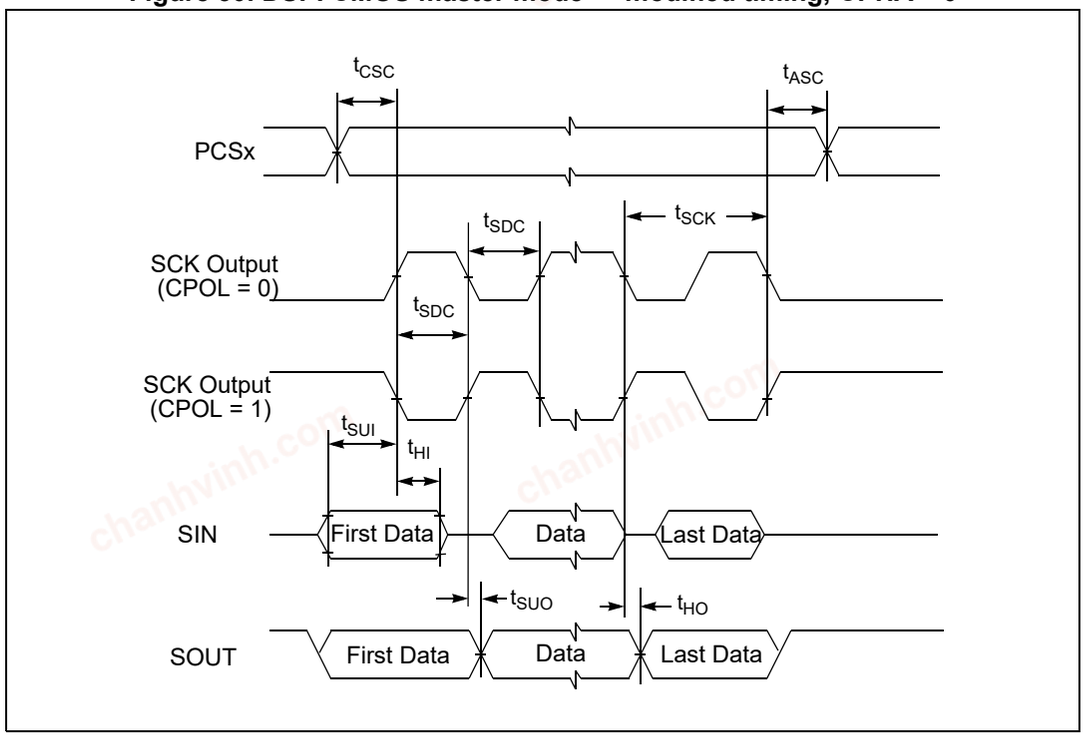
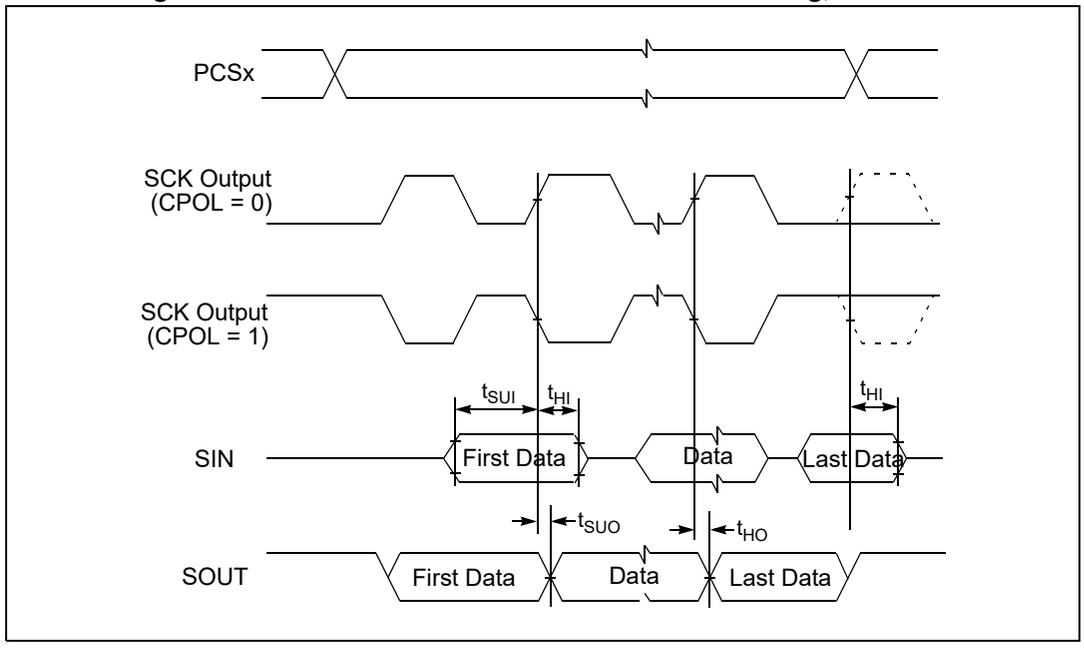
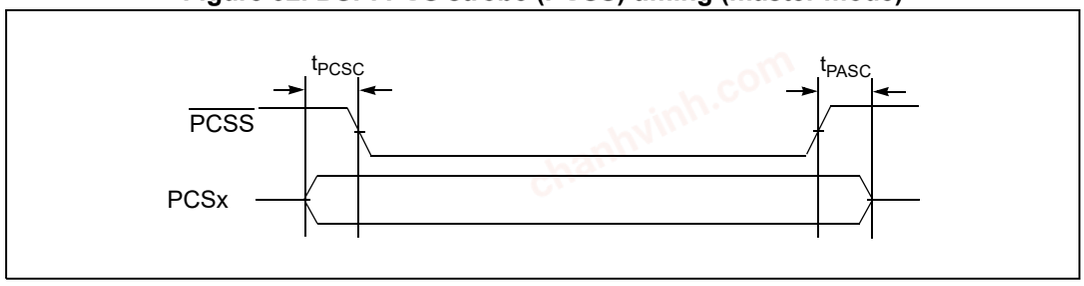


Figure 31. DSPI CMOS master mode — modified timing, CPHA = 1



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Figure 32. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



4.17.2.2 Slave mode timing

Table 49. DSPI CMOS slave timing — full duplex — normal and modified transfer formats (MTFE = 0/1)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
1	t_{SCK}	CC	D	SCK Cycle Time(1)	—	—	62	—	ns
2	t_{CSC}	SR	D	$\overline{SS}$ to SCK Delay(1)	—	—	16	—	ns
3	t_{ASC}	SR	D	SCK to $\overline{SS}$ Delay(1)	—	—	16	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle(1)	—	—	30	—	ns
5	t_A	CC	D	Slave Access Time(1) (2) (3) ($\overline{SS}$ active to SOUT driven)	Very strong	25 pF	—	50	ns
					Strong	50 pF	—	50	ns
					Medium	50 pF	—	60	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time(1) (2) (3) ($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very strong	25 pF	—	5	ns
					Strong	50 pF	—	5	ns
					Medium	50 pF	—	10	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs(1)	—	—	10	—	ns
10	t_{HI}	CC	D	Data Hold Time for Inputs(1)	—	—	10	—	ns
11	t_{SUO}	CC	D	SOUT Valid Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	—	30	ns
					Strong	50 pF	—	30	ns
					Medium	50 pF	—	50	ns
12	t_{HO}	CC	D	SOUT Hold Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	2.5	—	ns
					Strong	50 pF	2.5	—	ns
					Medium	50 pF	2.5	—	ns

1. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL voltage thresholds.
2. All timing values for output signals in this table, are measured to 50% of the output voltage.
3. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

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Figure 33. DSPI slave mode — modified transfer format timing (MFTE = 0/1) CPHA = 0

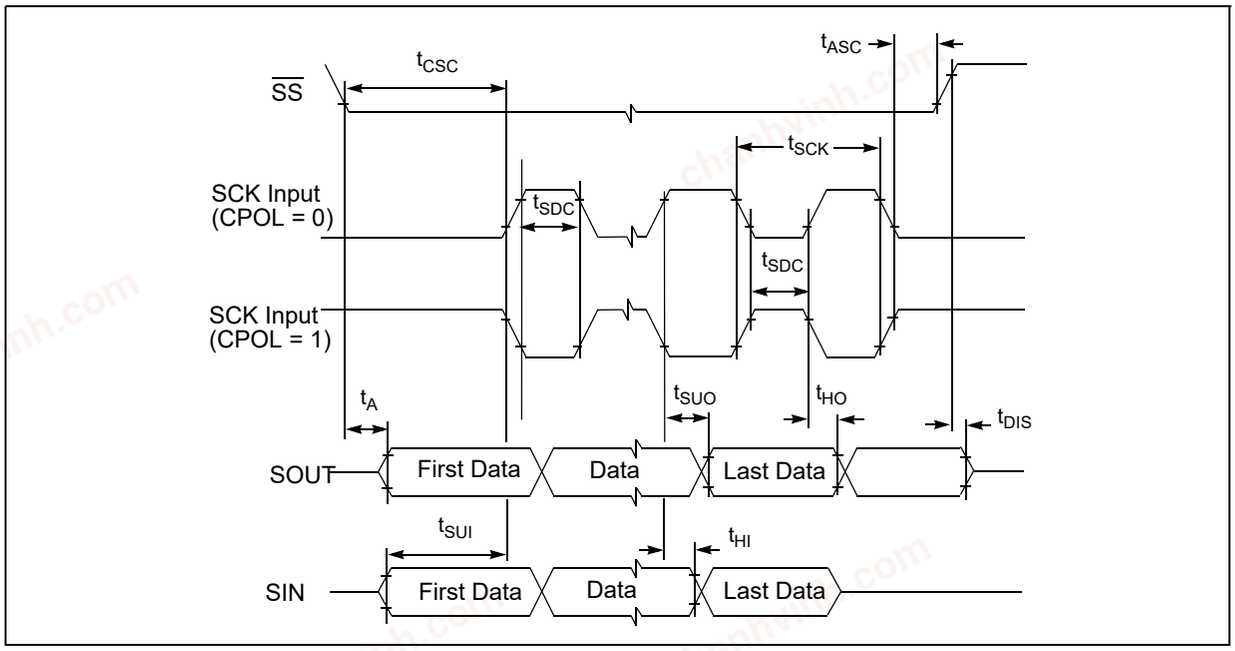
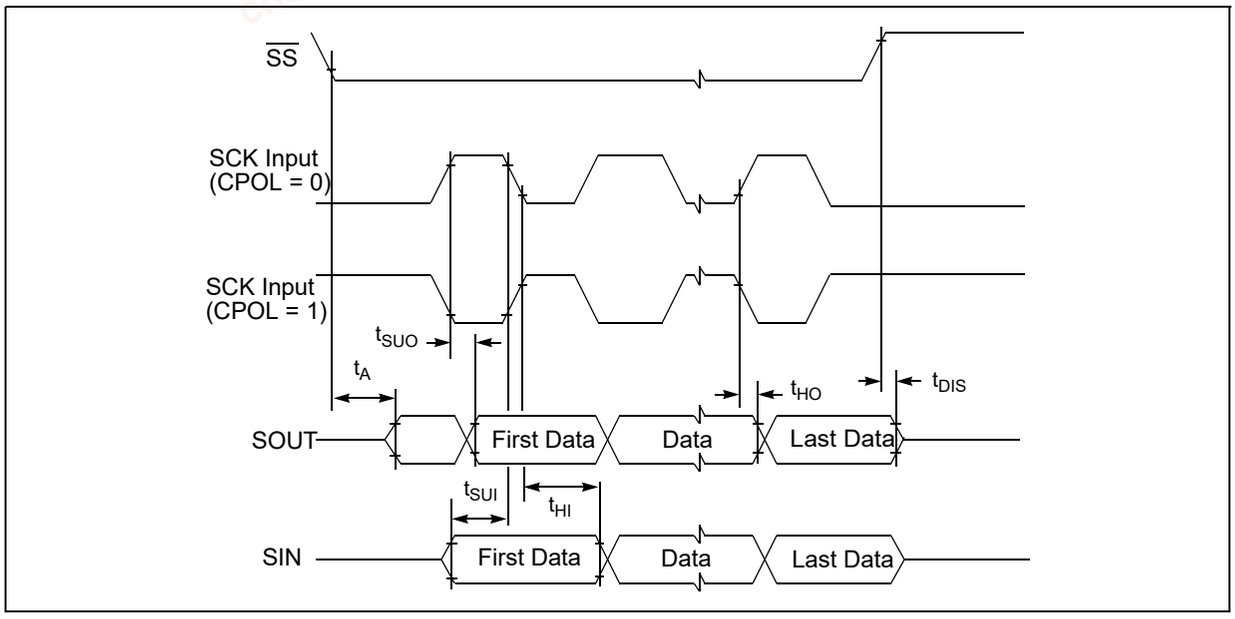


Figure 34. DSPI slave mode — modified transfer format timing (MFTE = 0/1) CPHA = 1



4.17.3 Ethernet timing

The Ethernet provides both MII and RMII interfaces. The MII and RMII signals can be configured for either CMOS or TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V. Please check the device pinout details to review the packages supporting MII and RMII.

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4.17.3.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

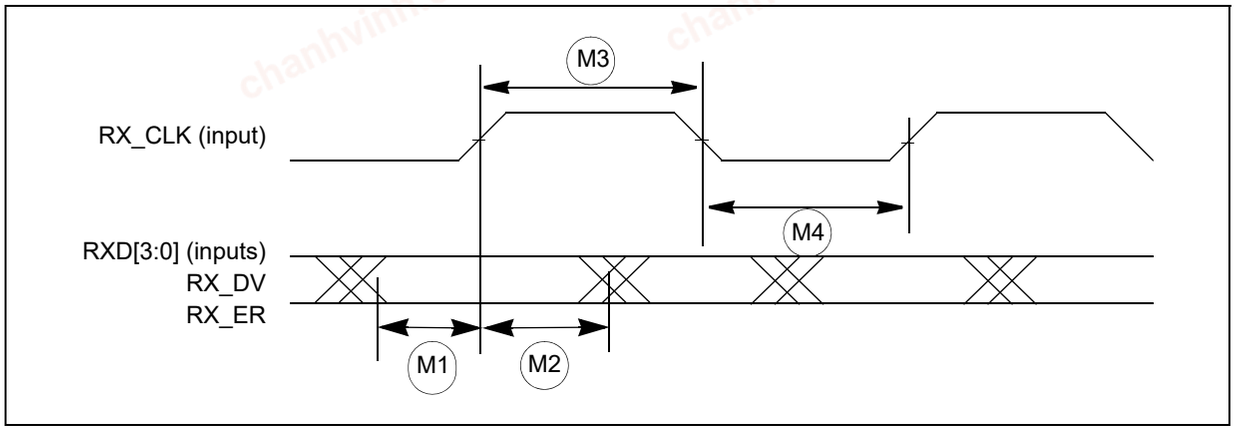
The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Note: In the following table, all timing specifications are referenced from RX_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

Table 50. MII receive signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M1	CC	D	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	CC	D	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	CC	D	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	CC	D	RX_CLK pulse width low	35%	65%	RX_CLK period

Figure 35. MII receive signal timing diagram



4.17.3.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This option allows the use of non-compliant MII PHYs.

Refer to the SPC584Cx and SPC58ECx 32-bit Power Architecture microcontroller *reference manual's* Ethernet chapter for details of this option and how to enable it.

Note: In the following table, all timing specifications are referenced from TX_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.

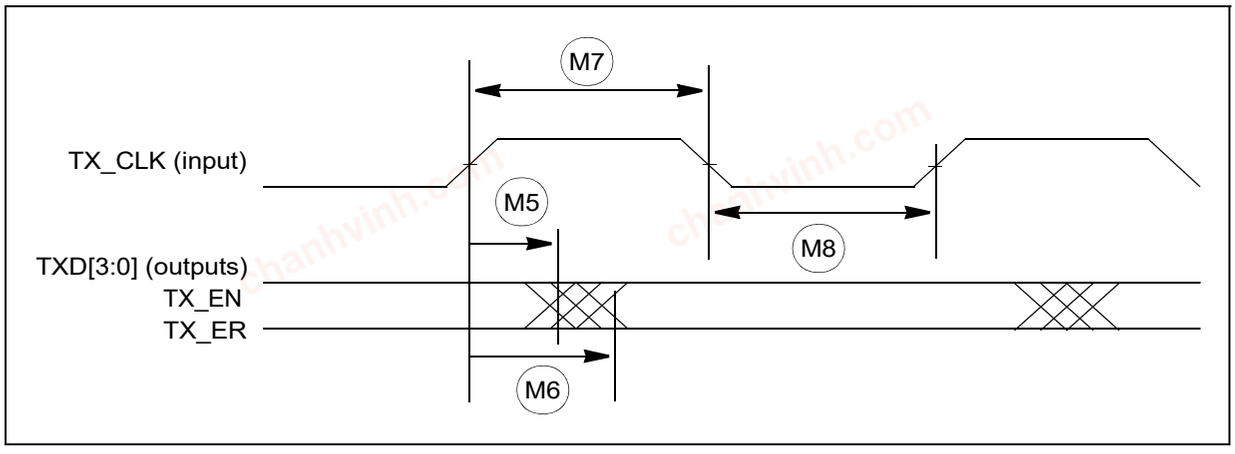
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Table 51. MII transmit signal timing

Symbol		C	Characteristic	Value(1)		Unit
				Min	Max	
M5	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	CC	D	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	CC	D	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	CC	D	TX_CLK pulse width low	35%	65%	TX_CLK period

1. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value

Figure 36. MII transmit signal timing diagram

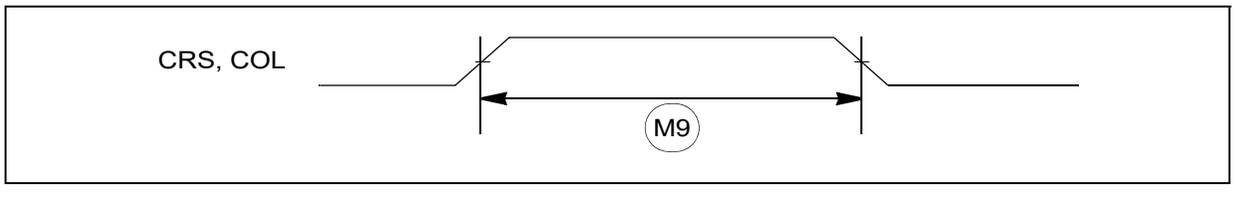


4.17.3.3 MII async inputs signal timing (CRS and COL)

Table 52. MII async inputs signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M9	CC	D	CRS, COL minimum pulse width	1.5	—	TX_CLK period

Figure 37. MII async inputs timing diagram

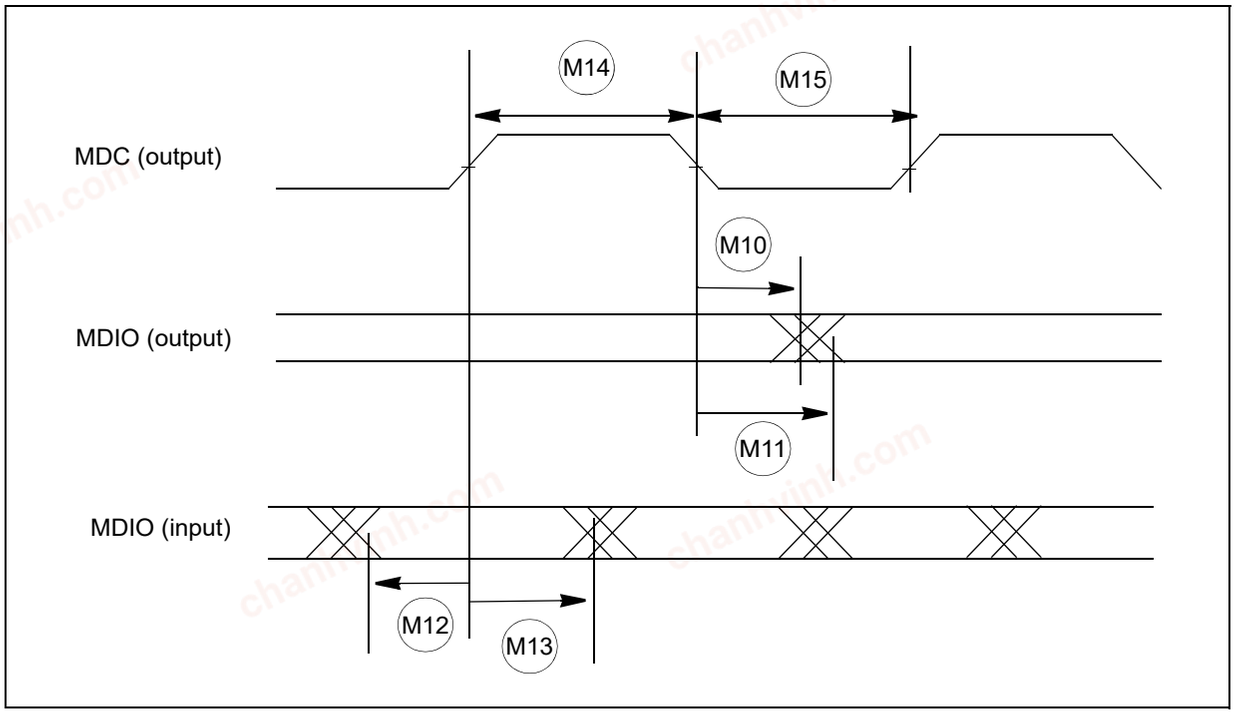


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4.17.3.4 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Figure 38. MII serial management channel timing diagram



4.17.3.5 MII and RMII serial management channel timing (MDIO and MDC)

The Ethernet functions correctly with a maximum MDC frequency of 2.5 MHz.

Note: In the following table, all timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Table 53. MII serial management channel timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

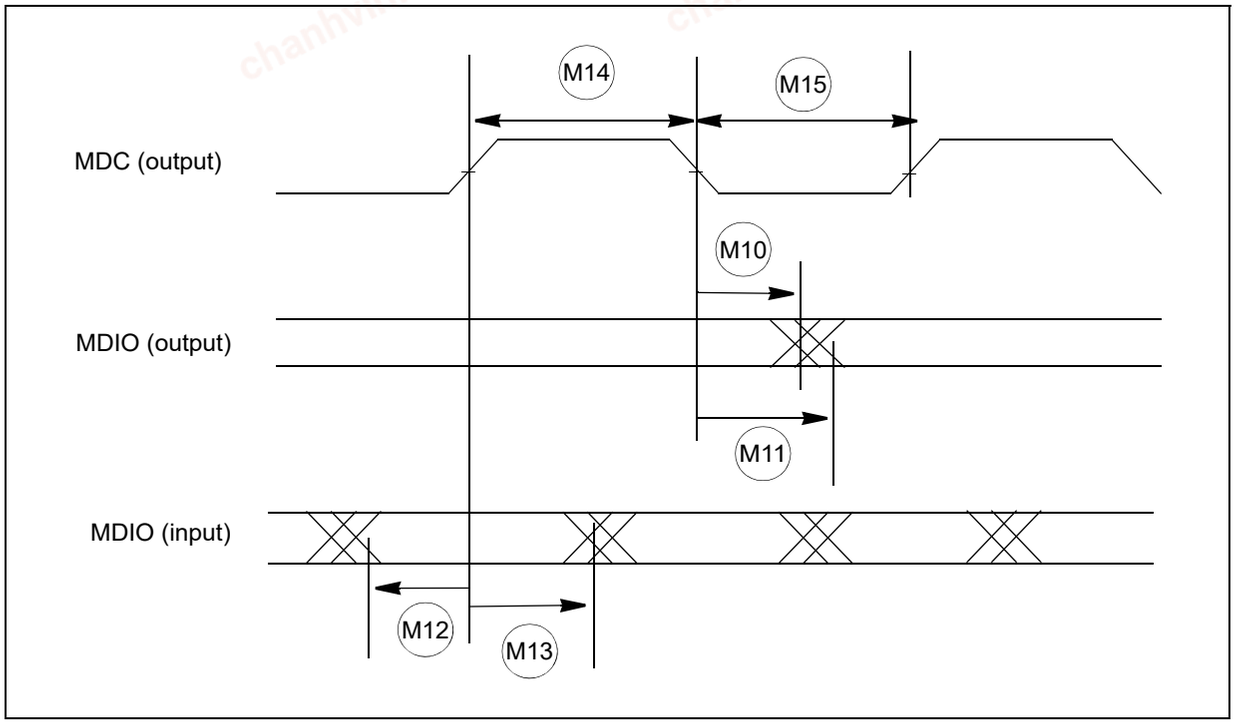
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Note: In the following table, all timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Table 54. RMII serial management channel timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
M10	CC	D	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	D	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	D	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	D	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	D	MDC pulse width high	40%	60%	MDC period
M15	CC	D	MDC pulse width low	40%	60%	MDC period

Figure 39. MII serial management channel timing diagram



4.17.3.6 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

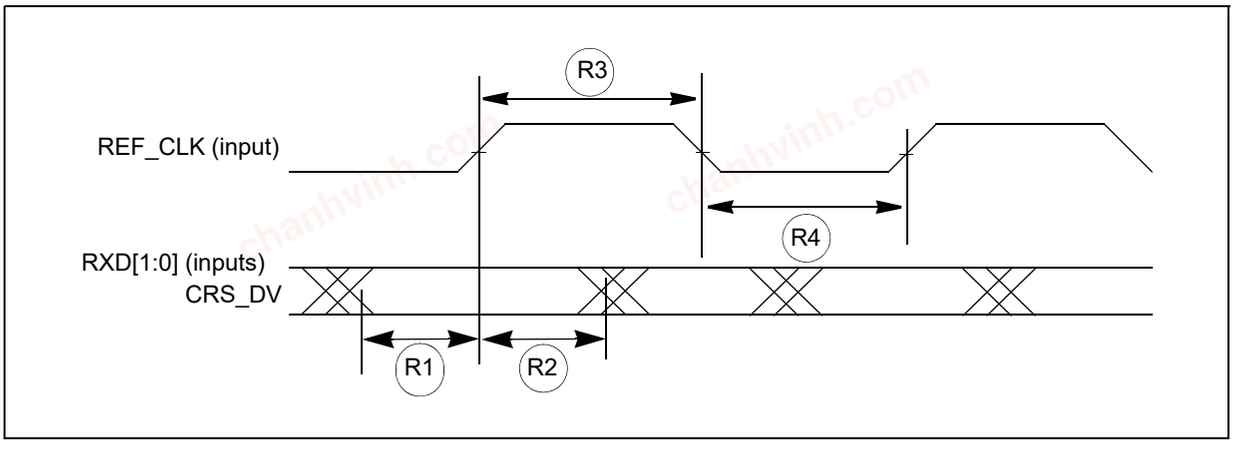
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Note: In the following table, all timing specifications are referenced from REF_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

Table 55. RMII receive signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
R1	CC	D	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	CC	D	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

Figure 40. RMII receive signal timing diagram



4.17.3.7 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. This option allows the use of non-compliant RMII PHYs.

Note: In the following table, all timing specifications are referenced from REF_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.

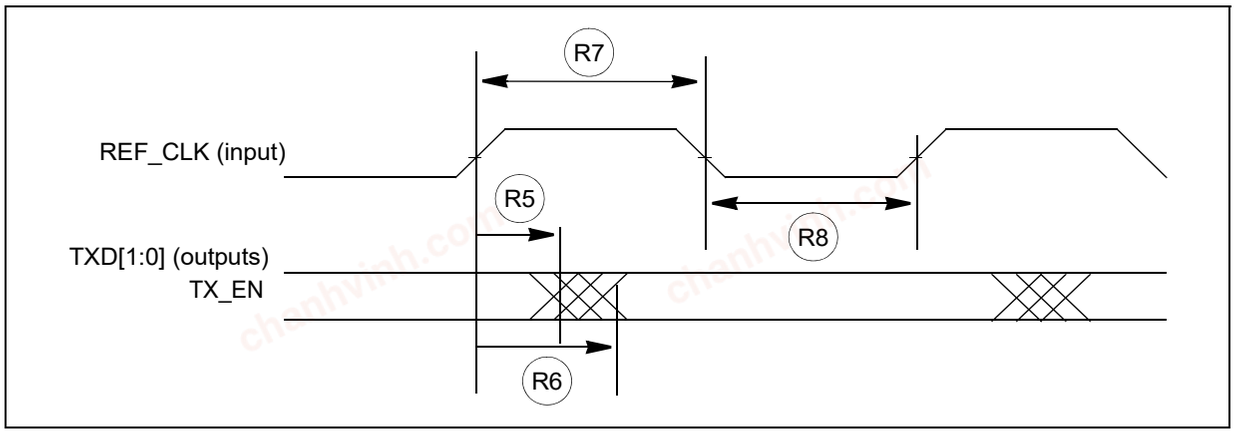
RMII transmit signal valid timing specified is considering the rise/fall time of the ref_clk on the pad as 1ns.

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Table 56. RMII transmit signal timing

Symbol		C	Characteristic	Value		Unit
				Min	Max	
R5	CC	D	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	CC	D	REF_CLK to TXD[1:0], TX_EN valid	—	14	ns
R7	CC	D	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	CC	D	REF_CLK pulse width low	35%	65%	REF_CLK period

Figure 41. RMII transmit signal timing diagram



4.17.4 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals.

These are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

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4.17.4.1 TxEN

Figure 42. TxEN signal

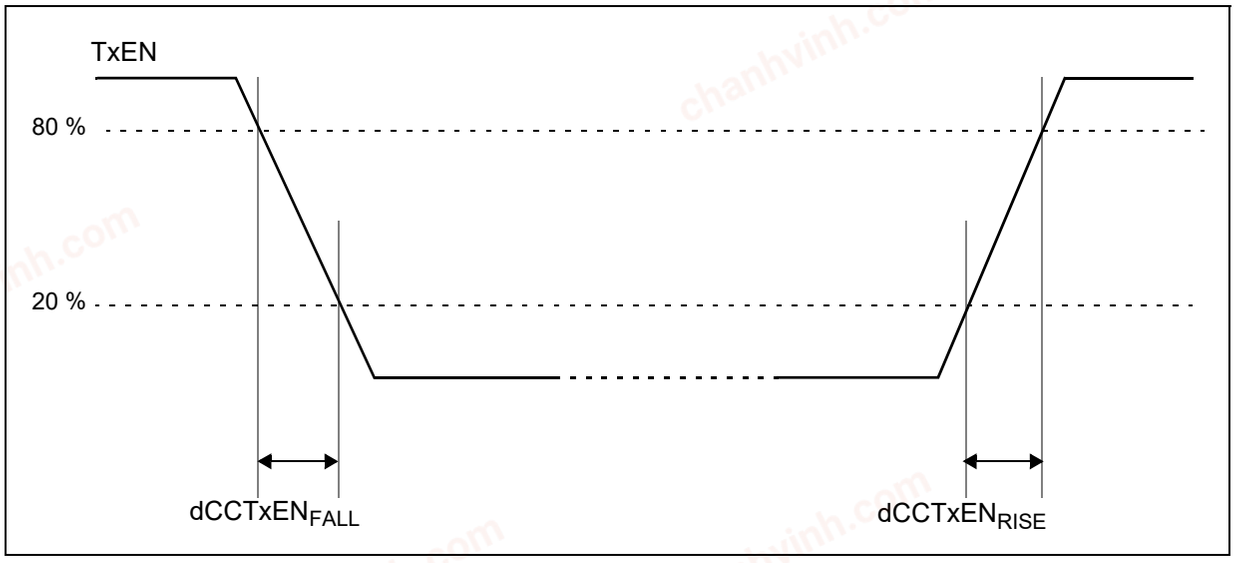


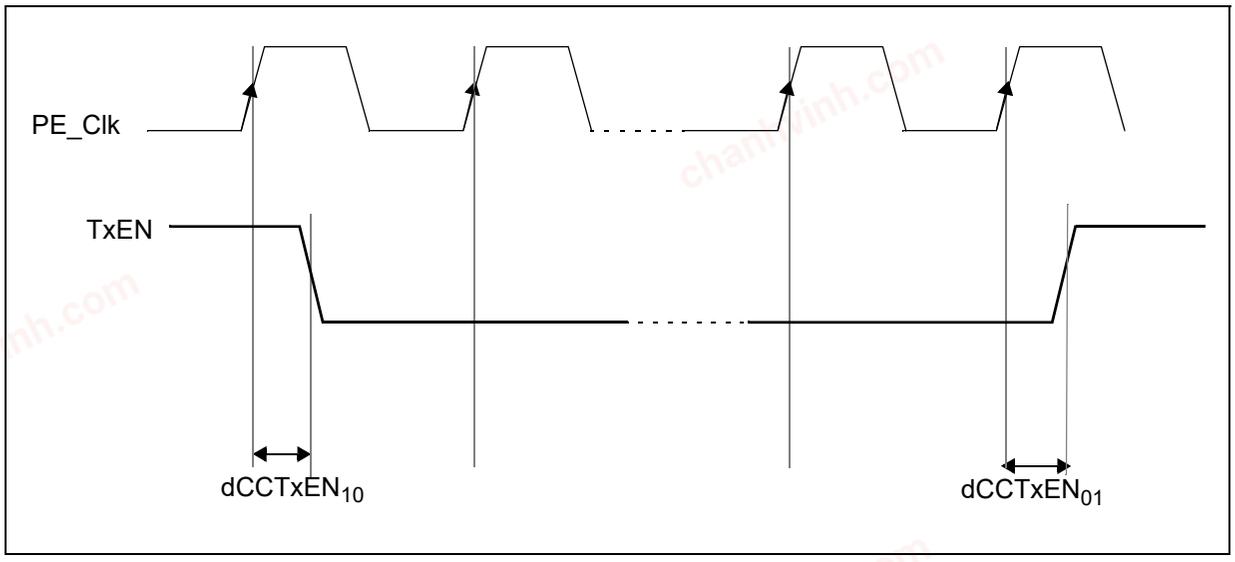
Table 57. TxEN output characteristics

Symbol		C	Characteristic[1] [2]	Value		Unit
				Min	Max	
dCCTxEN$_{RISE25}$	CC	D	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN$_{FALL25}$	CC	D	Fall time of TxEN signal at CC	—	9	ns
dCCTxEN$_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxEN$_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. TxEN pin load maximum 25 pF.
2. Pad configured as VERY STRONG.

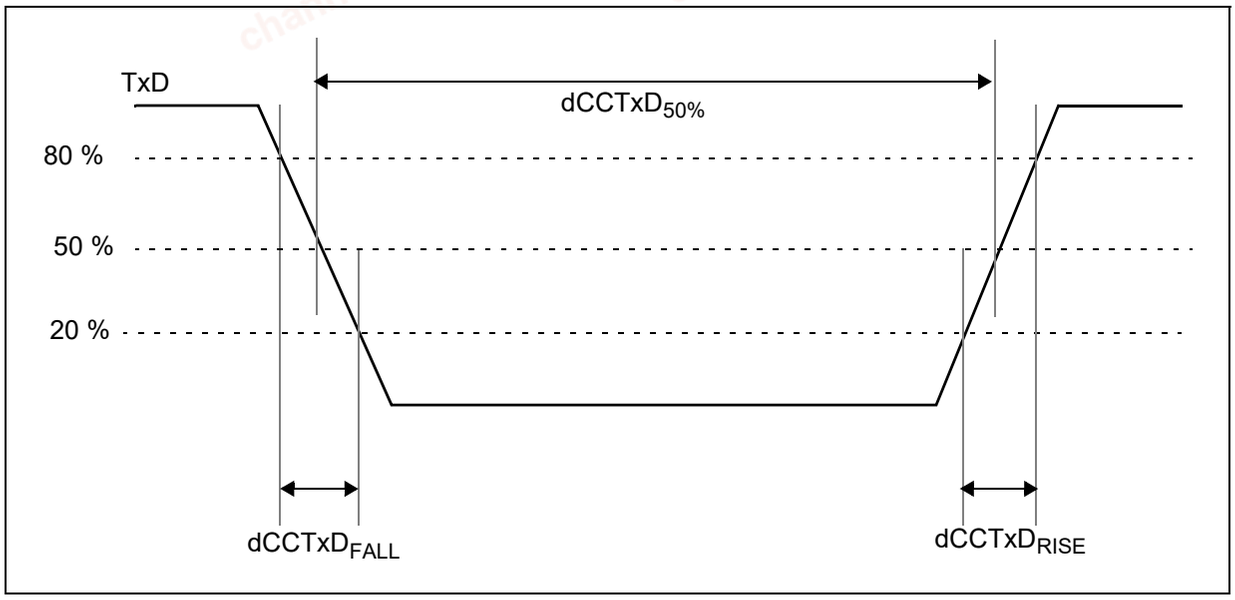
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Figure 43. TxEN signal propagation delays



4.17.4.2 TxD

Figure 44. TxD signal



Note: In the following table, specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10 pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.

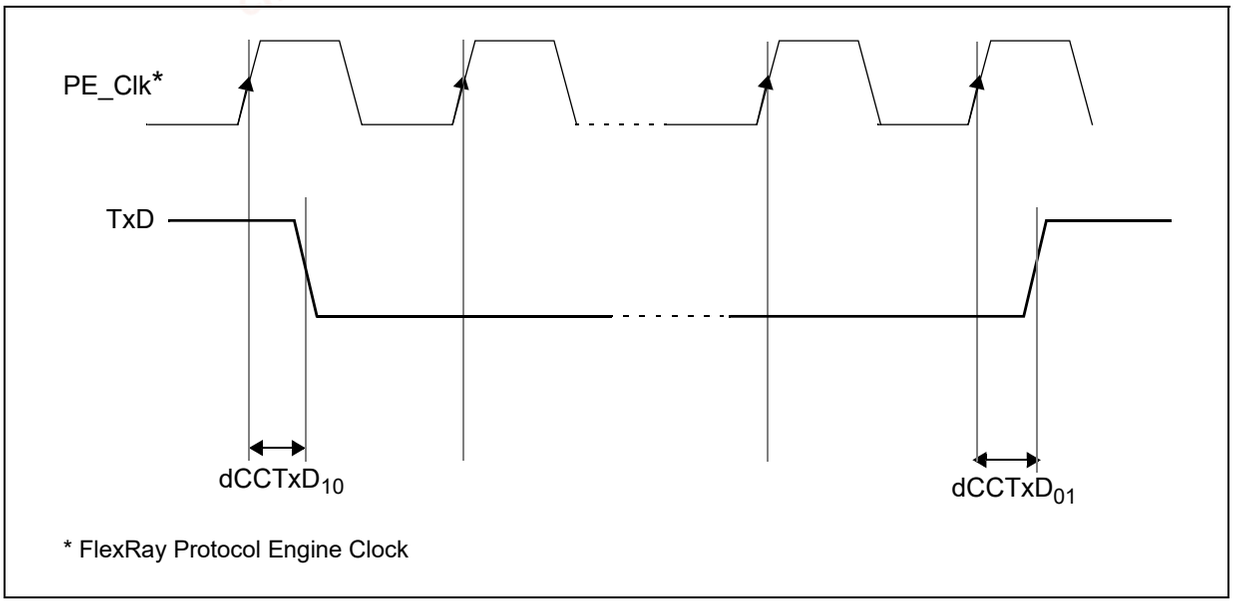
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Table 58. TxD output characteristics

Symbol		C	Characteristic[1],[2]	Value		Unit
				Min	Max	
dCCTxAsym	CC	D	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ – 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	D	Sum of Rise and Fall time of TxD signal at the output pin[3]	—	9[4]	ns
		D		—	9[5]	
$dCCTxD_{01}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	D	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. TxD pin load maximum 25 pF.
2. Pad configured as VERY STRONG.
3. Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.
4. $V_{DD_HV_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF.
5. $V_{DD_HV_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF.

Figure 45. TxD Signal propagation delays



4.17.4.3 RxD

Table 59. RxD input characteristics

Symbol		C	Characteristic	Value		Unit
				Min	Max	
C_CCRxD	CC	D	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	CC	D	Threshold for detecting logic high	35	70	%

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Table 59. RxD input characteristics (continued)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
uCCLogic_0	CC	D	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	CC	D	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	CC	D	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns
dCCRxAsymAccept15	CC	D	Acceptance of asymmetry at receiving CC with 15 pF load	–31.5	44	ns
dCCRxAsymAccept25	CC	D	Acceptance of asymmetry at receiving CC with 25 pF load	–30.5	43	ns

4.17.5 CAN timing

The following table describes the CAN timing.

Table 60. CAN timing

Symbol		C	Parameter	Condition	Value			Unit
					Min	Typ	Max	
$t_{P(RX:TX)}$	CC	D	CAN controller propagation delay time standard pads	Medium type pads 25pF load	—	—	70	ns
	CC	D		Medium type pads 50pF load	—	—	80	
	CC	D		STRONG, VERY STRONG type pads 25pF load	—	—	60	
	CC	D		STRONG, VERY STRONG type pads 50pF load	—	—	65	
$t_{PLP(RX:TX)}$	CC	D	CAN controller propagation delay time low power pads	Medium type pads 25pF load	—	—	90	ns
	CC	D		Medium type pads 50pF load	—	—	100	
	CC	D		STRONG, VERY STRONG type pads 25pF load	—	—	80	
	CC	D		STRONG, VERY STRONG type pads 50pF load	—	—	85	

4.17.6 UART timing

UART channel frequency support is shown in the following table.

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Table 61. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20
100	16	3:1 majority voting	6.25
	8		12.5
	6	Limited voting on one sample with configurable sampling point	16.67
	5		20
	4		25

4.17.7 I2C timing

The I^2C AC timing specifications are provided in the following tables.

Note: In the following table, I2C input timing is valid for Automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% – 90%).

Table 62. I2C input timing specifications – SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	PER_CLK Cycle(1)
2	—	CC	D	Clock low time	8	—	PER_CLK Cycle
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	D	Data hold time	0.0	—	ns
5	—	CC	D	Clock high time	4	—	PER_CLK Cycle
6	—	CC	D	Data setup time	0.0	—	ns
7	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	2	—	PER_CLK Cycle

1. PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Note: In the following table:

- *All output timing is worst case and includes the mismatching of rise and fall times of the output pads.*

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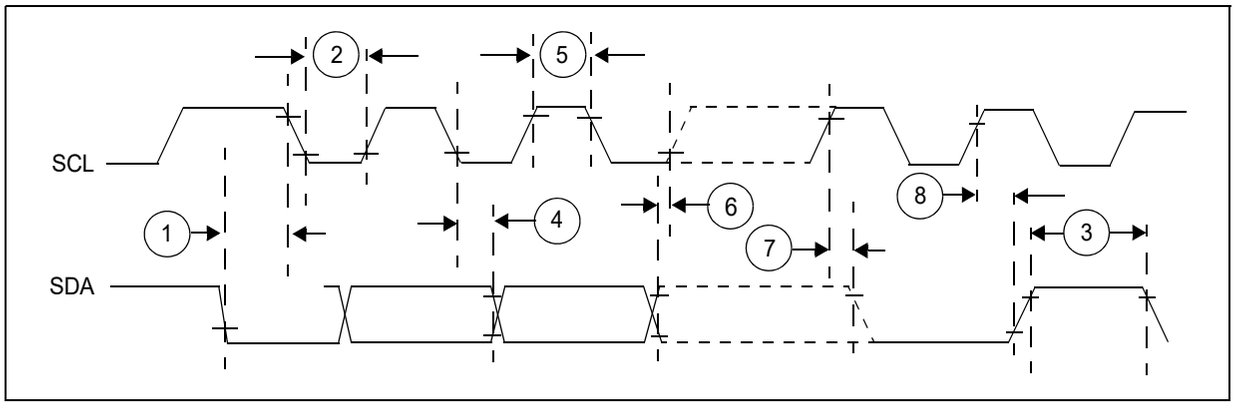
- *Output parameters are valid for CL = 25 pF, where CL is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.*
- *Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.*
- *Programming the IBFD register (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.*

Table 63. I2C output timing specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	6	—	PER_CLK Cycle(1)
2	—	CC	D	Clock low time	10	—	PER_CLK Cycle
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	D	Data hold time	7	—	PER_CLK Cycle
5	—	CC	D	Clock high time	10	—	PER_CLK Cycle
6	—	CC	D	Data setup time	2	—	PER_CLK Cycle
7	—	CC	D	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	10	—	PER_CLK Cycle

1. PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Figure 46. I^2C input/output timing



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5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

The following table lists the case numbers for SPC584Cx and SPC58ECx.

Table 64. Package case numbers

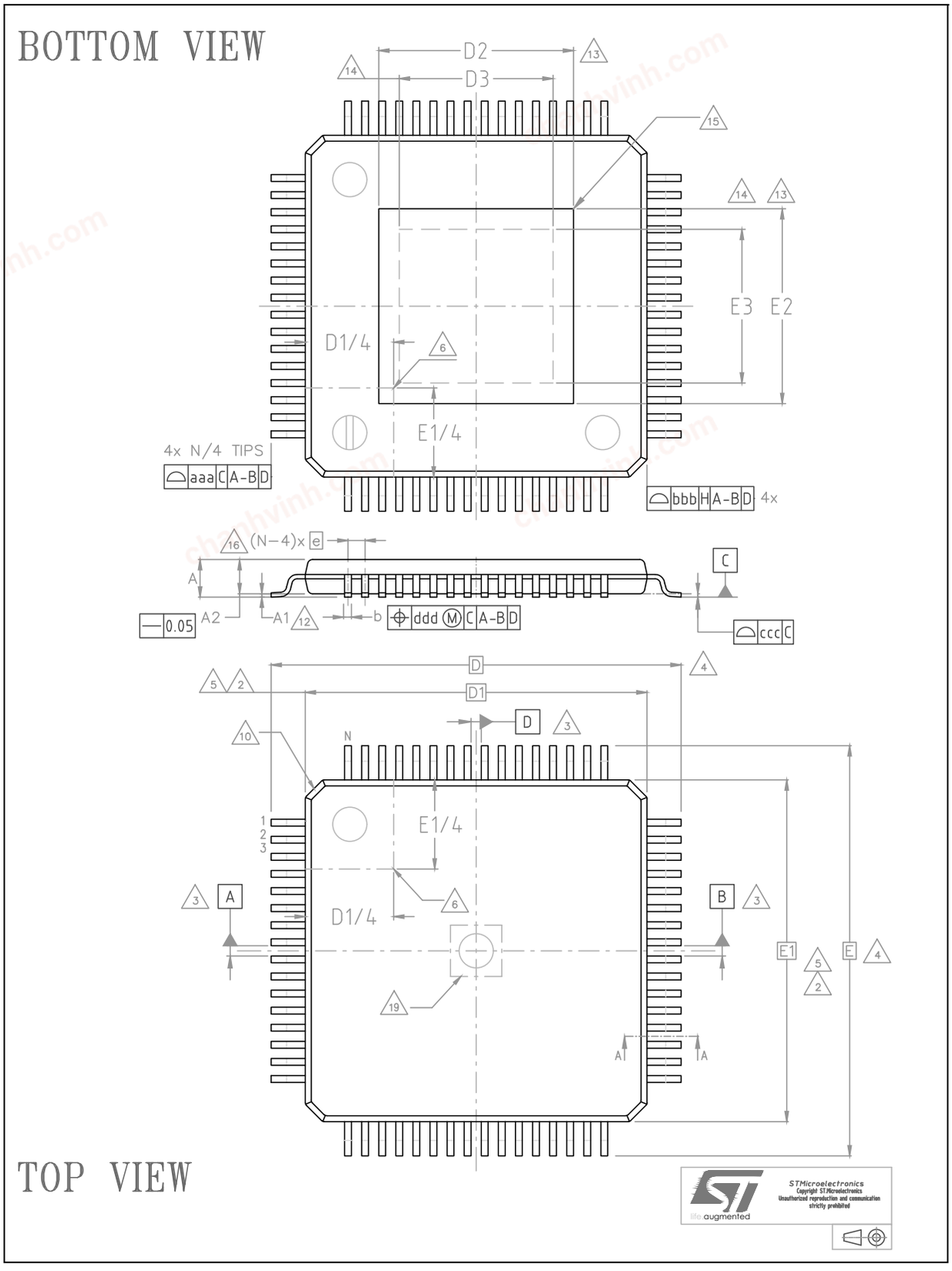
Package type	Device type
eTQFP64	Production
eTQFP100	Production
eTQFP144	Production
eLQFP176	Production
FPBGA292	Production

5.1 eTQFP64 package information

Refer to *Section 5.1.1: Package mechanical drawings and data information* for full description of below figures and table notes.

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Figure 47. eTQFP64 package outline



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Figure 48. eTQFP64 section A-A

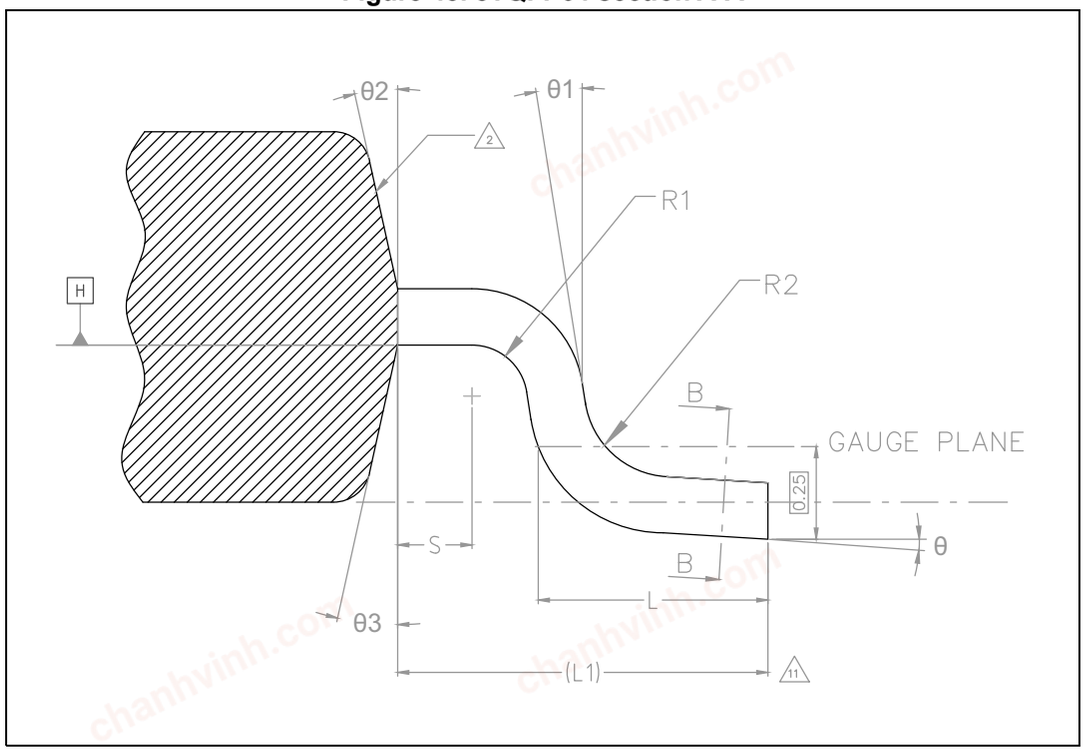
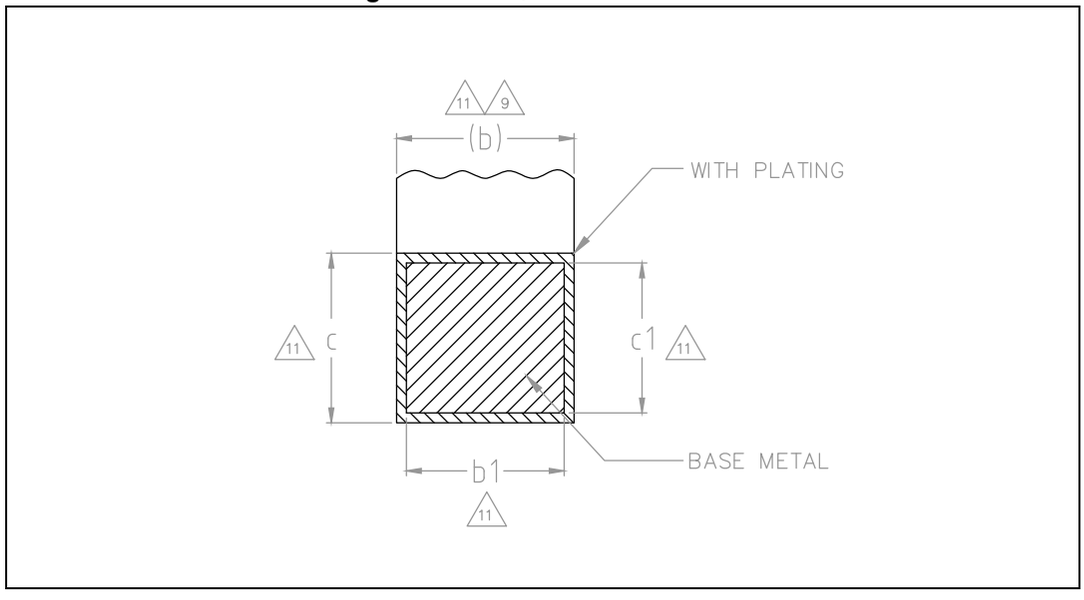


Figure 49. eTQFP64 section B-B



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Table 65. eTQFP64 package mechanical data

Symbol	Dimensions[7],[17]		
	Min.	Typ.	Max.
Θ	0°	3.5°	7°
Θ1	0°	—	—
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A[15]	—	—	1.20
A1[12]	0.05	—	0.15
A2[15]	0.95	1.00	1.05
b[8],[9],[11]	0.17	0.22	0.27
b1[11]	0.17	0.20	0.23
c[11]	0.09	—	0.20
c1[11]	0.09	—	0.16
D[4]	12 BSC		
D1[2],[5]	10 BSC		
D2[13]	—	—	6.93
D3[14]	5.25	—	—
e	0.50 BSC		
E[4]	12 BSC		
E1[2],[5]	10 BSC		
E2[13]	—	—	6.93
E3[14]	5.25	—	—
L	0.45	0.60	0.75
L1	1 REF		
N[16]	64		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
aaa[1],[18]	0.20		
bbb[1],[18]	0.20		
ccc[1],[18]	0.08		
ddd[1],[18]	0.08		

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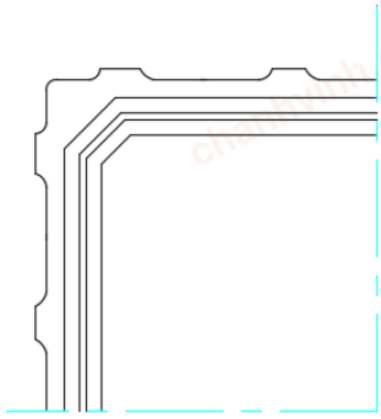
5.1.1 Package mechanical drawings and data information

The following notes are related to *Figure 47*, *Figure 48*, *Figure 49* and *Table 65*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC584Cx and SPC58ECx is as *Figure 50*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 66*.
19. Notch may be present in this area (MAX 1.5 mm square) if center top gate molding technology is applied. Resin gate residual not protruding out of package top surface.

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Figure 50. eTQFP64 leadframe pad design



Note: number, dimensions and positions of grooves are for reference only.

Table 66. eTQFP64 symbol definitions

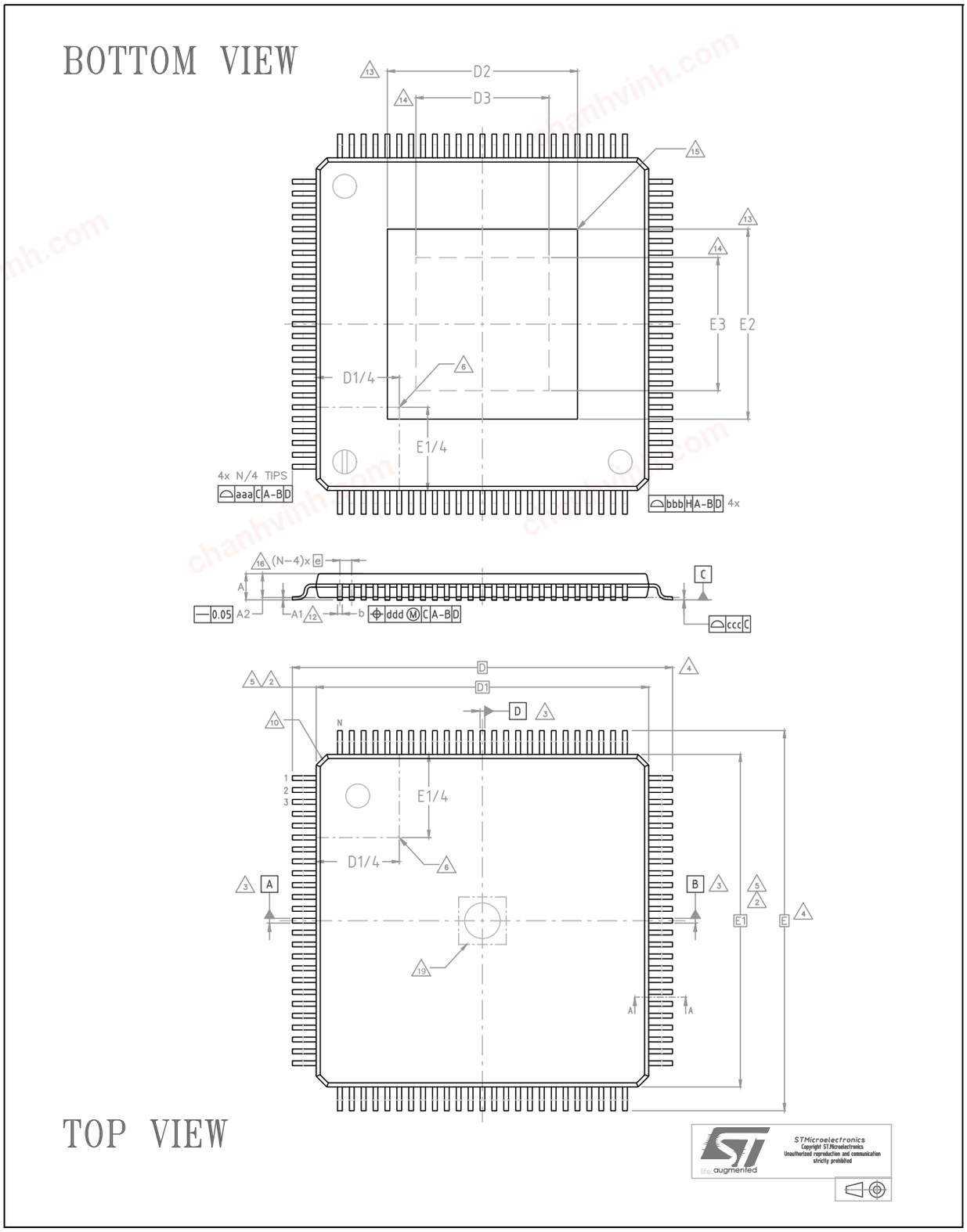
Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.2 eTQFP100 package information

Refer to *Section 5.2.1: Package mechanical drawings and data information* for full description of below figures and table notes.

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Figure 51. eTQFP100 package outline



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Figure 52. eTQFP100 section A-A

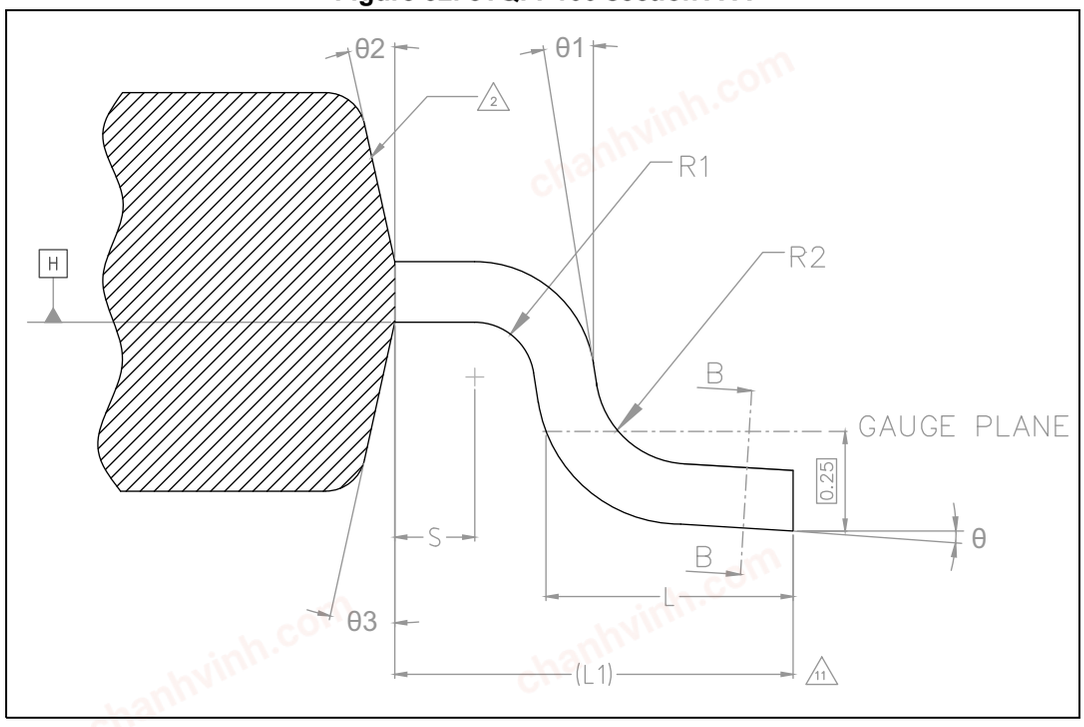
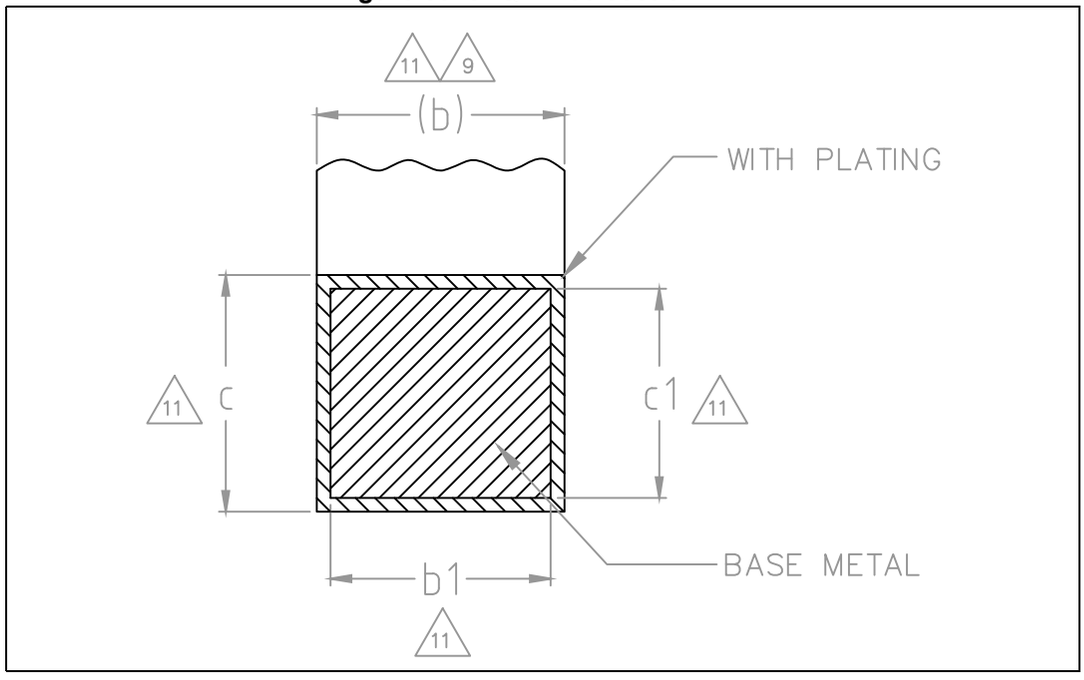


Figure 53. eTQFP100 section B-B



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Table 67. eTQFP100 package mechanical data

Symbol	Dimensions[7],[17]		
	Min.	Typ.	Max.
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	10°	12°	14°
θ3	10°	12°	14°
A[15]	—	—	1.20
A1[12]	0.05	—	0.15
A2[15]	0.95	1.00	1.05
b[8],[9],[11]	0.17	0.22	0.27
b1[11]	0.17	0.20	0.23
c[11]	0.09	—	0.20
c1[11]	0.09	—	0.16
D[4]	16.00 BSC		
D1[2],[5]	14.00 BSC		
D2[13]	—	—	6.77
D3[14]	5.10	—	—
e	0.50 BSC		
E[4]	16.00 BSC		
E1[2],[5]	14.00 BSC		
E2[13]	—	—	6.77
E3[14]	5.10	—	—
L	0.45	0.60	0.75
L1	1.00 REF		
N[16]	100		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
aaa[1],[18]	0.20		
bbb[1],[18]	0.20		
ccc[1],[18]	0.08		
ddd[1],[18]	0.08		

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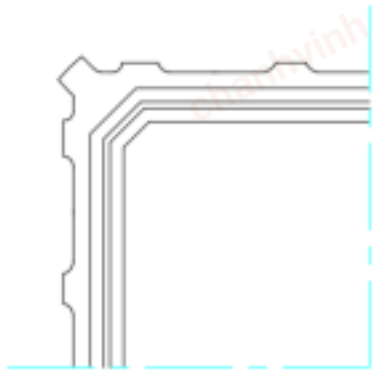
5.2.1 Package mechanical drawings and data information

The following notes are related to *Figure 51*, *Figure 52*, *Figure 53* and *Table 67*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC584Cx and SPC58ECx is as *Figure 54*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 68*.
19. Notch may be present in this area (MAX 2.0 mm square) if center top gate molding technology is applied. Resin gate residual not protruding out of package top surface.

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Figure 54. eTQFP100 leadframe pad design



Note: number, dimensions and positions of grooves are for reference only.

Table 68. eTQFP100 symbol definitions

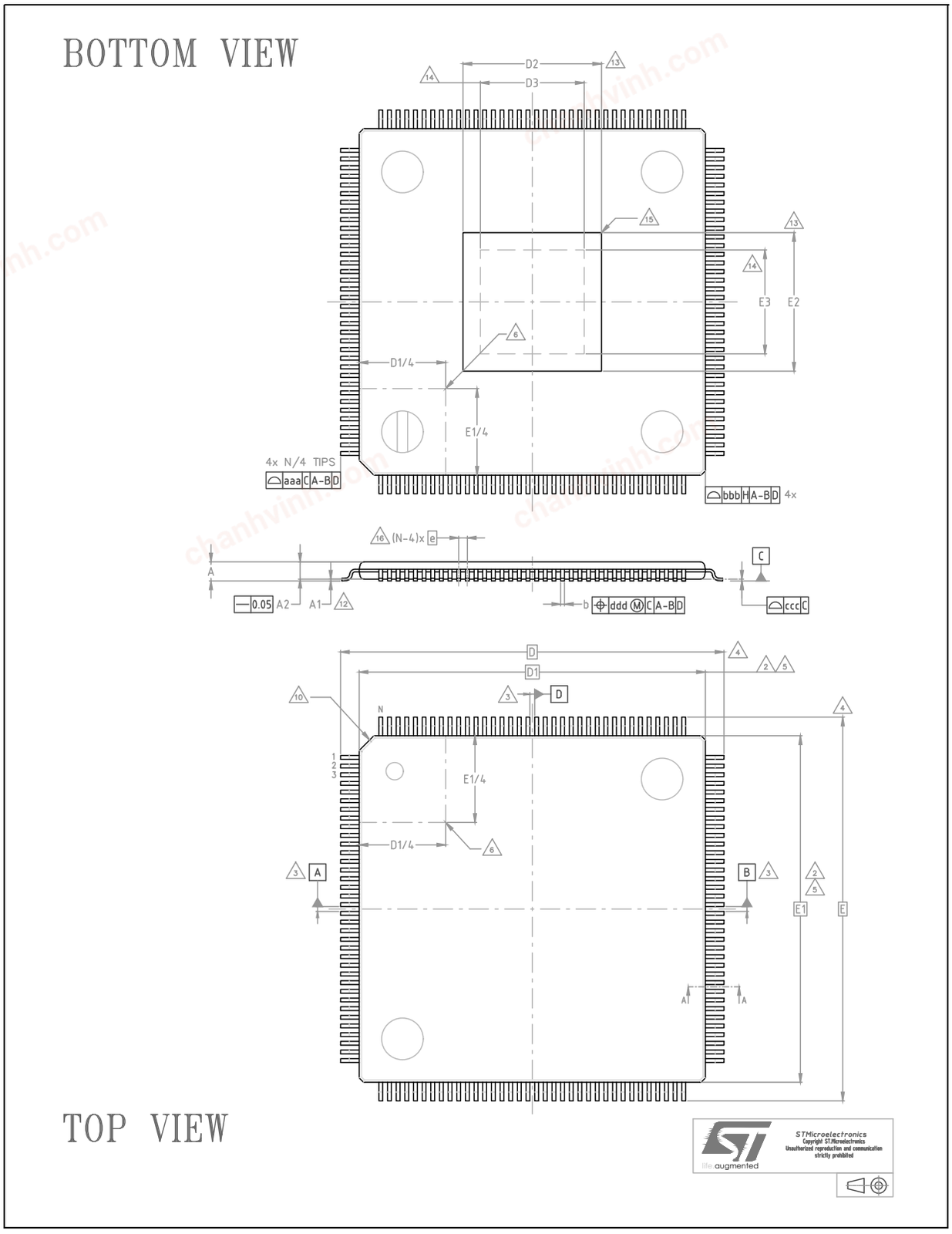
Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.3 eTQFP144 package information

Refer to *Section 5.3.1: Package mechanical drawings and data information* for full description of below figures and table notes.

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Figure 55. eTQFP144 package outline



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Figure 56. eTQFP144 section A-A

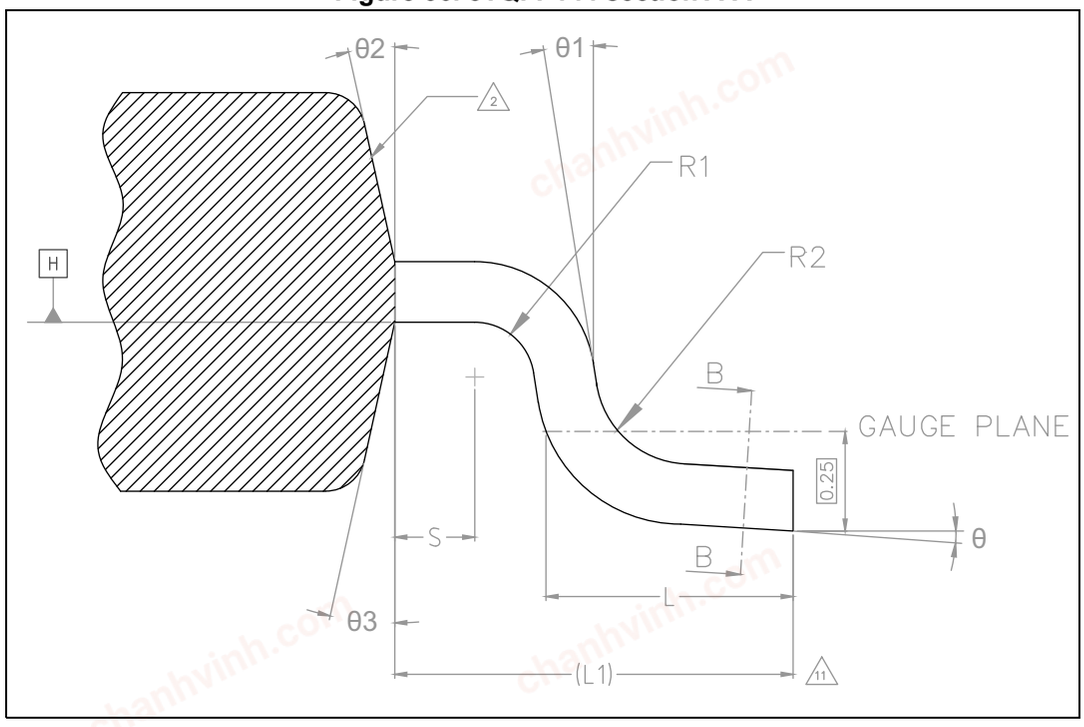
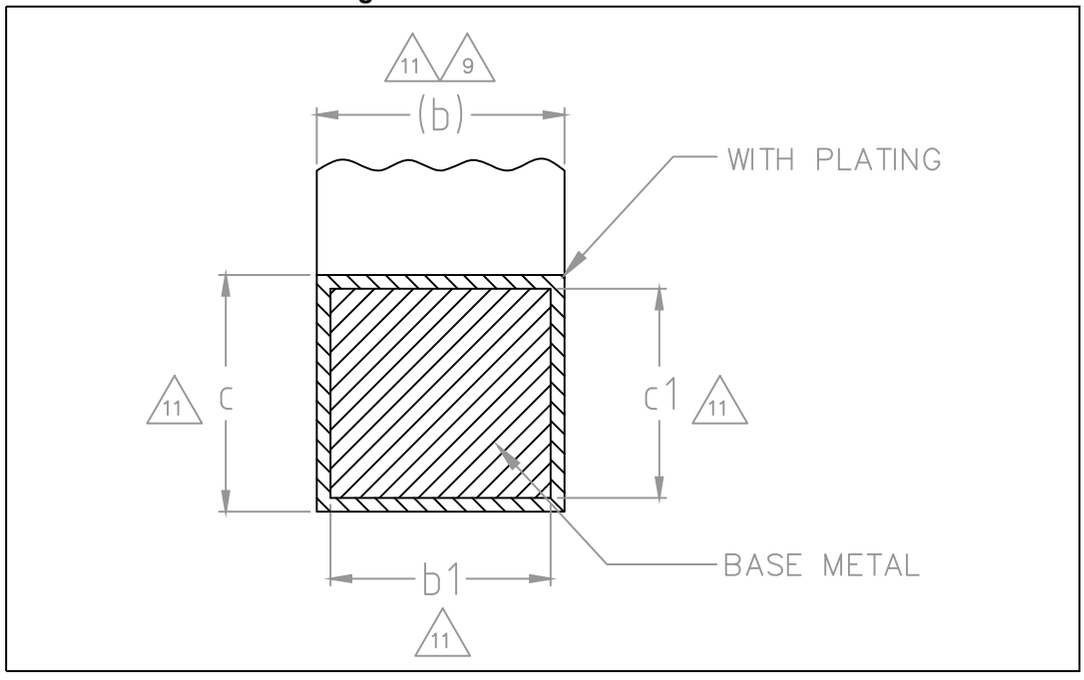


Figure 57. eTQFP144 section B-B



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Table 69. eTQFP144 package mechanical data

Symbol	Dimensions[7],[17]		
	Min.	Typ.	Max.
θ	0.0°	3.5°	7.0°
θ1	0.0°	—	—
θ2	10.0°	12.0°	14.0°
θ3	10.0°	12.0°	14.0°
A[15]	—	—	1.20
A1[12]	0.05	—	0.15
A2[15]	0.95	1.00	1.05
b[8],[9],[11]	0.17	0.22	0.27
b1[11]	0.17	0.20	0.23
c[11]	0.09	—	0.20
c1[11]	0.09	—	0.16
D[4]	—	22.00 BSC	—
D1[2],[5]	—	20.00 BSC	—
D2[13]	—	—	6.76
D3[14]	5.10	—	—
E[4]	—	22.00 BSC	—
E1[2],[5]	—	20.00 BSC	—
E2[13]	—	—	6.76
E3[14]	5.10	—	—
e	0.50 BSC		
L	0.45	0.60	0.75
L1	—	1.00 REF	—
N[16]	144		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
aaa[1],[18]	0.20		
bbb[1],[18]	0.20		
ccc[1],[18]	0.08		
ddd[1],[18]	0.08		

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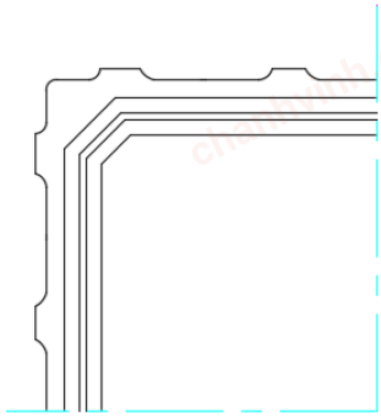
5.3.1 Package mechanical drawings and data information

The following notes are related to *Figure 55*, *Figure 56*, *Figure 57* and *Table 69*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC584Cx and SPC58ECx is as *Figure 58*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 70*.

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Figure 58. eTQFP144 leadframe pad design



Note: number, dimensions and positions of grooves are for reference only.

Table 70. eTQFP144 symbol definitions

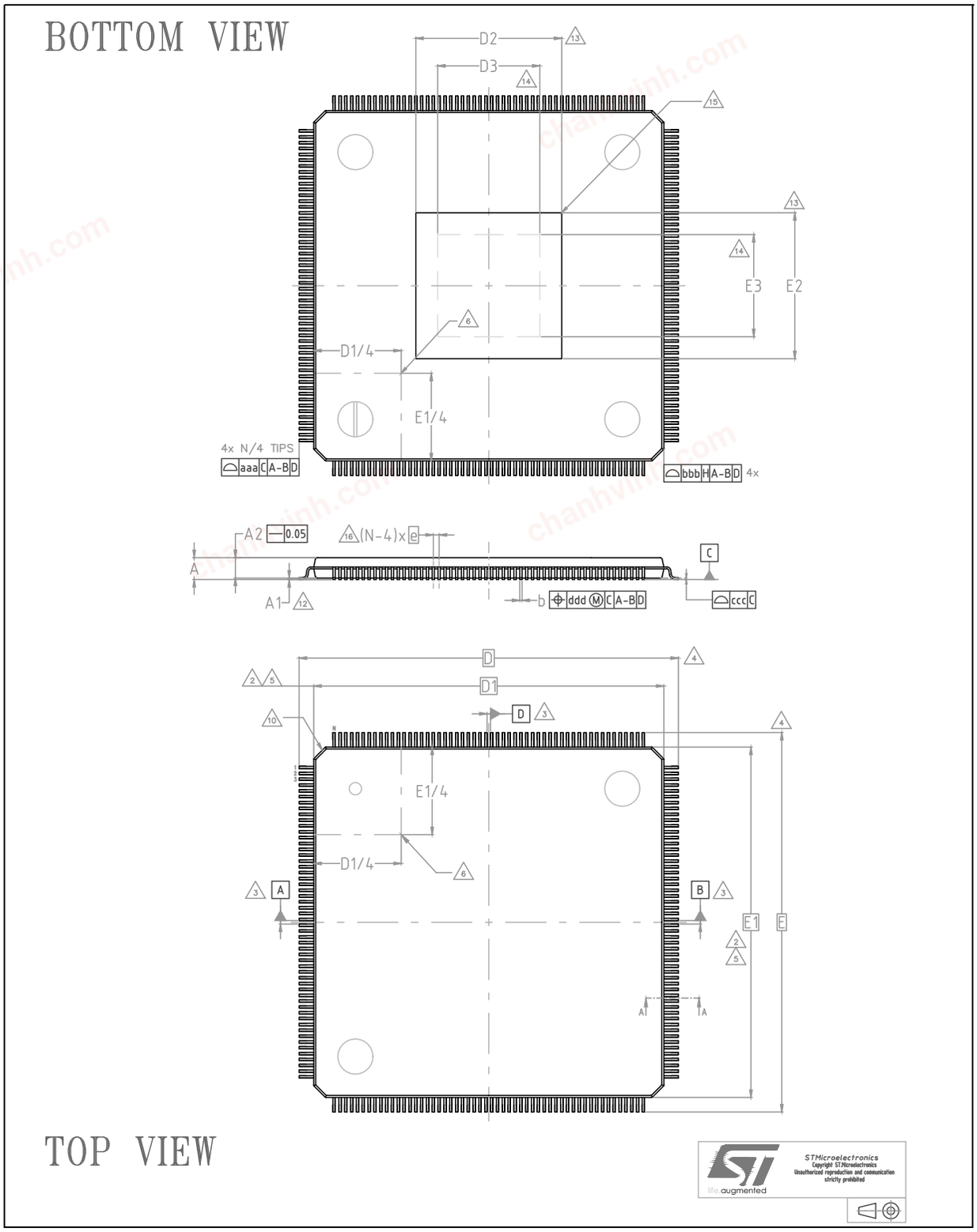
Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.4 eLQFP176 package information

Refer to *Section 5.4.1: Package mechanical drawings and data information* for full description of below figures and table notes.

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Figure 59. eLQFP176 package outline



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Figure 60. eLQFP176 section A-A

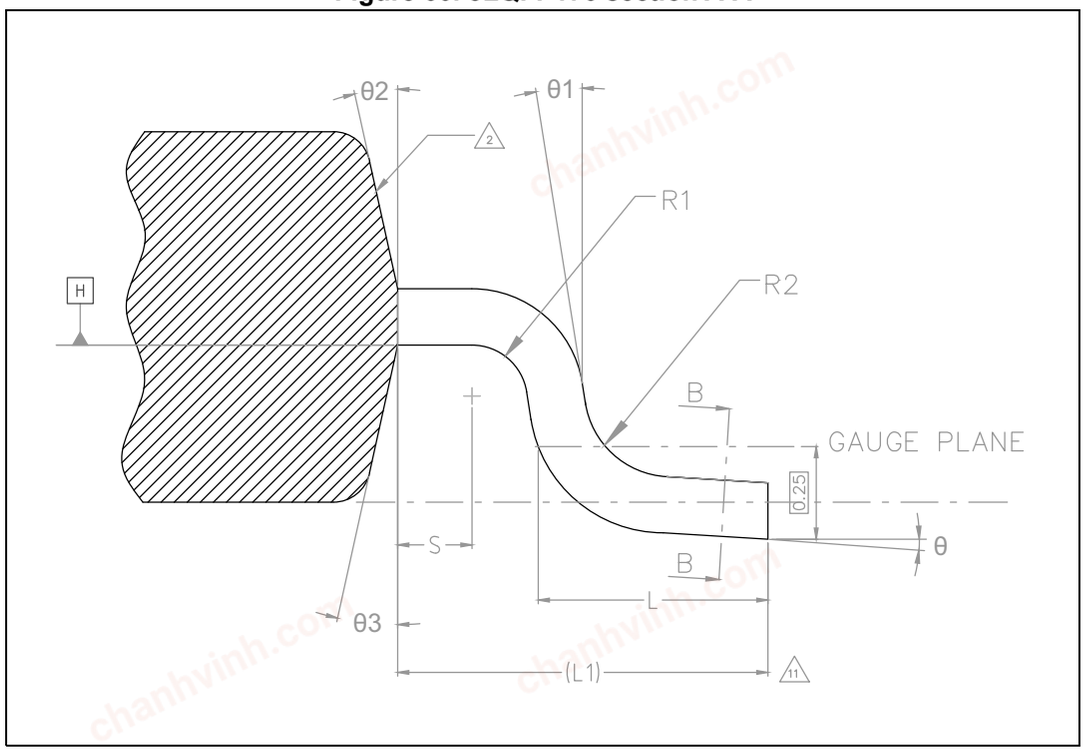
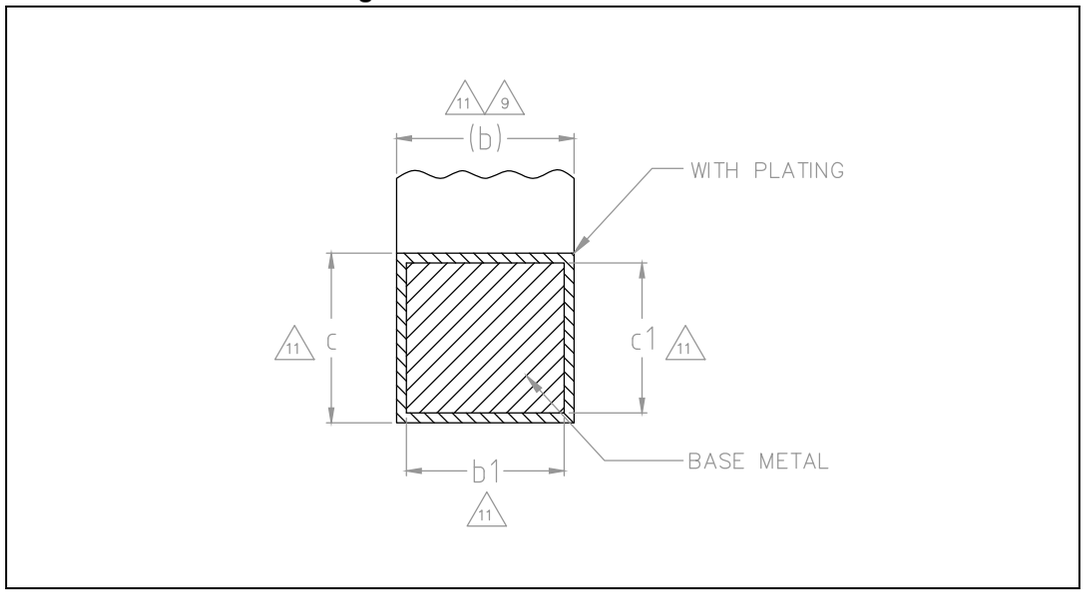


Figure 61. eLQFP176 section B-B



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Table 71. eLQFP176 package mechanical data

Symbol	Dimensions[7],[17]		
	Min.	Nom.	Max.
Θ	0°	3.5°	7°
Θ1	0°	—	—
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A[15]	—	—	1.60
A1[12]	0.05	—	0.15
A2[15]	1.35	1.40	1.45
b[8],[9],[11]	0.17	0.22	0.27
b1[11]	0.17	0.20	0.23
c[11]	0.09	—	0.20
c1[11]	0.09	—	0.16
D[4]	26.00 BSC		
D1[2],[5]	24.00 BSC		
D2[13]	—	—	7.77
D3[14]	6.10	—	—
e	0.50 BSC		
E[4]	26.00 BSC		
E1[2],[5]	24.00 BSC		
E2[13]	—	—	7.77
E3[14]	6.10	—	—
L	0.45	0.60	0.75
L1	1.00 REF		
N[16]	176		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	
aaa[1],[18]	0.20		
bbb[1],[18]	0.20		
ccc[1],[18]	0.08		
ddd[1],[18]	0.08		

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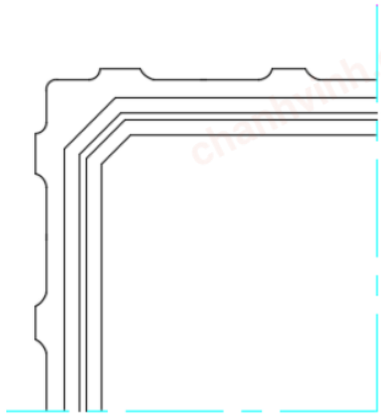
5.4.1 Package mechanical drawings and data information

The following notes are related to *Figure 59*, *Figure 60*, *Figure 61* and *Table 71*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC584Cx and SPC58ECx is as *Figure 62*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 72*.

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Figure 62. eLQFP176 leadframe pad design



Note: number, dimensions and positions of grooves are for reference only.

Table 72. eLQFP176 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.5 FPBGA292 package information

Refer to *Section 5.5.1: Package mechanical drawings and data information* for full description of below figures and table notes.

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Figure 63. FPBGA292 package outline

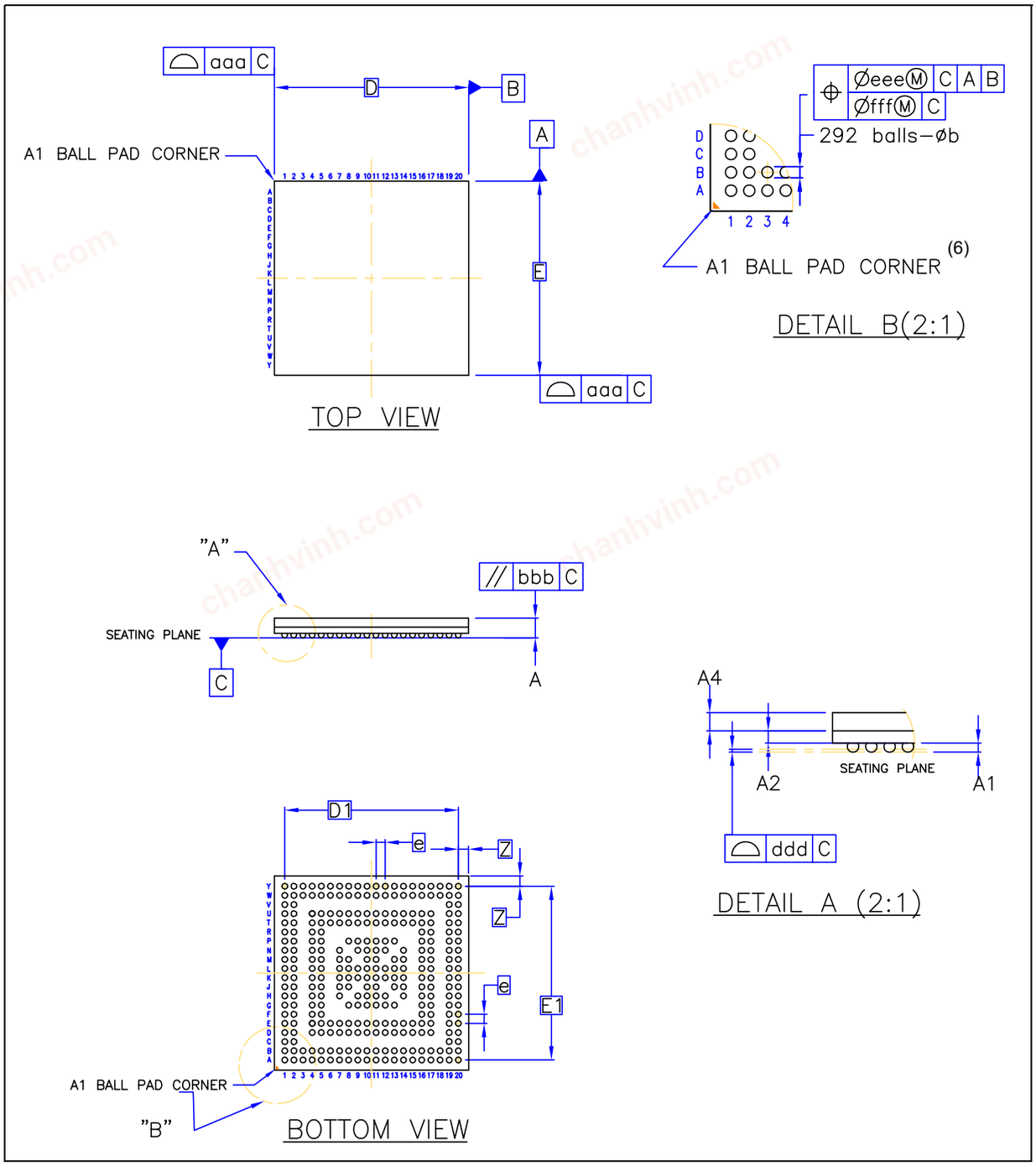


Table 73. FPBGA292 package mechanical data

Symbol	Dimensions (in millimeter)		
	Min.	Typ.	Max.
A(1)	–	–	1.8
A1	0.35	–	–

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Table 73. FPBGA292 package mechanical data (continued)

Symbol	Dimensions (in millimeter)		
	Min.	Typ.	Max.
A2	–	0.53	–
A4	–	–	0.80
D	16.85	17.00	17.15
D1	–	15.20	–
E	16.85	17.00	17.15
E1	–	15.20	–
e	–	0.80	–
b(2)	0.50	0.55	0.60
Z	–	0.90	–
aaa	–	–	0.15
bbb	–	–	0.10
ddd(3)	–	–	0.12
eee(4)	–	–	0.15
fff(5)	–	–	0.08

5.5.1 Package mechanical drawings and data information

The following notes are related to *Figure 63* and *Table 73*:

1. FPBGA stands for Fine Pitch Plastic Ball Grid Array.
   Fine pitch: e < 1.00 mm pitch.
   Low Profile: The total profile height (Dim A) is measured from the seating plane to the top of the component.
   The maximum total package height is calculated by the following methodology (tolerance values):

$$Amax = A_1(TYP) + A_2(TYP) + A_4(TYP) + \sqrt{(A_1)^2 + (A_2)^2 + (A_4)^2}$$

2. The typical ball diameter before mounting is 0.55mm.
3. Ref. JEDEC MO_219G_BGA Low Profile, Fine Pitch Ball Grid Array Family, 0.80MM Pitch (SQ. & RECT.)
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

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6. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

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5.6 Package thermal characteristics

The following tables describe the thermal characteristics of the device. The parameters in this chapter have been evaluated by considering the device consumption configuration reported in the *Section 4.7: Device consumption*.

5.6.1 eTQFP64

Table 74. Thermal characteristics for 64 exposed pad eTQFP package

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board (2s2p) (External Ballast)	26.1	°C/W
				Four layer board (2s2p) (Internal Ballast)	28.6	
$R_{\theta JB}$	CC	D	Junction-to-board[3]	External Ballast	6.9	°C/W
				Internal Ballast	9.9	
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	External Ballast	8.6	°C/W
				Internal Ballast	11.8	
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	External Ballast	1	°C/W
				Internal Ballast	4	
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection (External Ballast)	1	°C/W
				Natural convection (Internal Ballast)	3.6	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.6.2 eTQFP100

Table 75. Thermal characteristics for 100 exposed pad eTQFP package

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board (2s2p) (External Ballast)	25.8	°C/W
				Four layer board (2s2p) (Internal Ballast)	28.5	

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Table 75. Thermal characteristics for 100 exposed pad eTQFP package (continued)

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JB}$	CC	D	Junction-to-board[3]	External Ballast	9.5	°C/W
				Internal Ballast	12.7	
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	External Ballast	8.6	°C/W
				Internal Ballast	11.9	
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	External Ballast	1	°C/W
				Internal Ballast	4	
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection (External Ballast)	1	°C/W
				Internal Ballast	3.6	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.6.3 eTQFP144

Table 76. Thermal characteristics for 144 exposed pad eTQFP package

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board (2s2p) (External Ballast)	25.5	°C/W
				Four layer board (2s2p) (Internal Ballast)	28.2	
$R_{\theta JB}$	CC	D	Junction-to-board[3]	External Ballast	10.2	°C/W
				Internal Ballast	13.4	
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	External Ballast	8.7	°C/W
				Internal Ballast	12	
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	External Ballast	1	°C/W
				Internal Ballast	4	
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection (External Ballast)	1	°C/W
				Natural convection (Internal Ballast)	3.6	

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1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.6.4 LQFP176

Table 77. Thermal characteristics for 176 exposed pad LQFP package

Symbol		C	Parameter(1)	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Four layer board (2s2p) (External Ballast)	24	°C/W
				Four layer board (2s2p) (Internal Ballast)	26.1	
$R_{\theta JB}$	CC	D	Junction-to-board(3)	External Ballast	10.9	°C/W
				Internal Ballast	13.9	
$R_{\theta JCtop}$	CC	D	Junction-to-case top(4)	External Ballast	10.2	°C/W
				Internal Ballast	13.2	
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom(5)	External Ballast	1	°C/W
				Internal Ballast	3.7	
Ψ_{JT}	CC	D	Junction-to-package top(6)	Natural convection External Ballast	1	°C/W
				Internal Ballast	3.5	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

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5.6.5 FPBGA292

Table 78. Thermal characteristics for 292-pin FPBGA

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection [2]	Four layer board (2s2p) (External Ballast)	24.4	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	External Ballast	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[4]	External Ballast	9	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[5]	Natural convection (External Ballast)	1.1	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.6.6 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

Equation 1
$$T_J = T_A + (R_{\theta JA} * P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The differences between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leaves the planes virtually disconnected, the thermal performance is also greatly reduced.

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As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2

$$T_J = T_B + (R_{\theta JB} * P_D)$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit

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board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5

$$T_J = T_B + (\Psi_{JPB} \times P_D)$$

where:

T_T = thermocouple temperature on bottom of the package (°C)

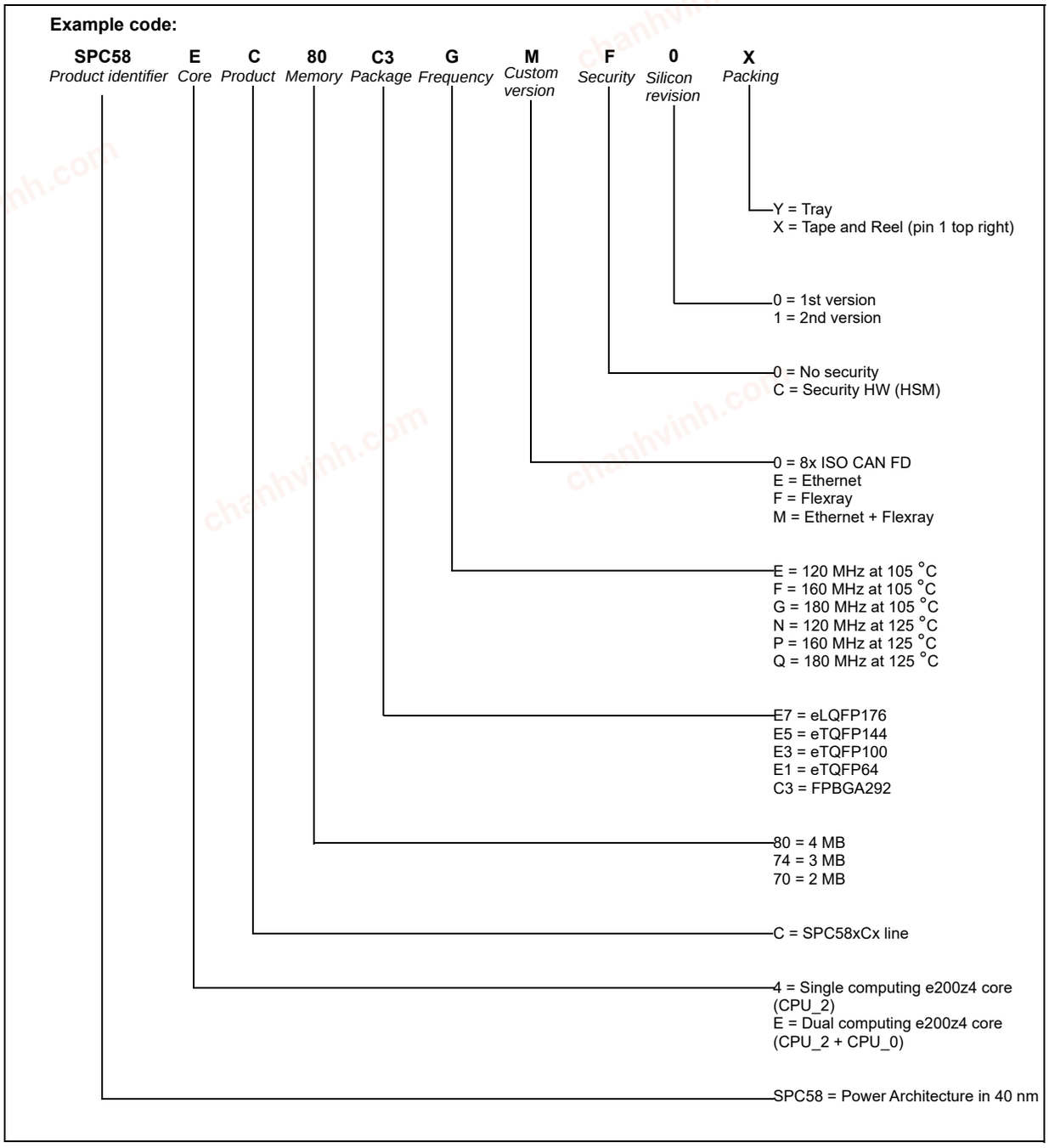
Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

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6 Ordering information

Figure 64. Commercial product scheme



Note: Please contact your ST sales office to ask for the availability of a particular commercial product.

Features (for instance, flash, RAM or peripherals) not included in the commercial product cannot be used.
ST cannot be called to take any liability for features used outside the commercial product.

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Table 79. Code Flash Options FOTA (KByte)

SPC58xC80 (4M)	SPC58xC74 (3M)(1)	SPC58xC70 (2M)(1)	Partition	Start address	End address
16	16	16	1	0x00FC0000	0x00FC3FFF
16	16	16	0	0x00FC4000	0x00FC7FFF
16	16	16	1	0x00FC8000	0x00FCBFFF
16	16	16	0	0x00FCC000	0x00FCFFFF
32	32	32	0	0x00FD0000	0x00FD7FFF
32	32	32	1	0x00FD8000	0x00FDFFFF
64	64	64	0	0x00FE0000	0x00FEFFFF
64	64	64	0	0x00FF0000	0x00FFFFFF
128	128	128	0	0x01000000	0x0101FFFF
128	128	128	1	0x01020000	0x0103FFFF
256	256	256	0	0x01040000	0x0107FFFF
256	256	256	0	0x01080000	0x010BFFFF
256	256	256	0	0x010C0000	0x010FFFFF
256	256	NA	0	0x01100000	0x0113FFFF
256	256	NA	0	0x01140000	0x0117FFFF
256	NA	NA	0	0x01180000	0x011BFFFF
256	NA	NA	0	0x011C0000	0x011FFFFF
256	256	256	1	0x01200000	0x0123FFFF
256	256	256	1	0x01240000	0x0127FFFF
256	256	256	1	0x01280000	0x012BFFFF
256	256	NA	1	0x012C0000	0x012FFFFF
256	256	NA	1	0x01300000	0x0133FFFF
256	NA	NA	1	0x01340000	0x0137FFFF
256	NA	NA	1	0x01380000	0x013BFFFF

1. The user must use this mapping without mixing it with the Contiguous one in *Table 80*.

Table 80. Code Flash Options contiguous (KByte)

SPC58xC80 (4M)	SPC58xC74 (3M)(1)	SPC58xC70 (2M)(1)	Partition	Start address	End address
16	16	16	1	0x00FC0000	0x00FC3FFF
16	16	16	0	0x00FC4000	0x00FC7FFF
16	16	16	1	0x00FC8000	0x00FCBFFF
16	16	16	0	0x00FCC000	0x00FCFFFF
32	32	32	0	0x00FD0000	0x00FD7FFF

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Table 80. Code Flash Options contiguous (KByte) (continued)

SPC58xC80 (4M)	SPC58xC74 (3M)(1)	SPC58xC70 (2M)(1)	Partition	Start address	End address
32	32	32	1	0x00FD8000	0x00FDFFFF
64	64	64	0	0x00FE0000	0x00FEFFFF
64	64	64	0	0x00FF0000	0x00FFFFFF
128	128	128	0	0x01000000	0x0101FFFF
128	128	128	1	0x01020000	0x0103FFFF
256	256	256	0	0x01040000	0x0107FFFF
256	256	256	0	0x01080000	0x010BFFFF
256	256	256	0	0x010C0000	0x010FFFFF
256	256	256	0	0x01100000	0x0113FFFF
256	256	256	0	0x01140000	0x0117FFFF
256	256	256	0	0x01180000	0x011BFFFF
256	256	NA	0	0x011C0000	0x011FFFFF
256	256	NA	1	0x01200000	0x0123FFFF
256	256	NA	1	0x01240000	0x0127FFFF
256	256	NA	1	0x01280000	0x012BFFFF
256	NA	NA	1	0x012C0000	0x012FFFFF
256	NA	NA	1	0x01300000	0x0133FFFF
256	NA	NA	1	0x01340000	0x0137FFFF
256	NA	NA	1	0x01380000	0x013BFFFF

1. The user must use this mapping without mixing it with the FOTA one in *Table 79*.

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Table 81. RAM options

SPC58EC80	SPC584C80	SPC58EC74	SPC584C74	SPC58EC70	SPC584C70	Type	Start address	End address
512(1)	384(1)	416(1)	320(1)	320(1)	256(1)			
8	8	8	8	8	8	PRAMC_2 (STBY)	0x400A8000	0x400A9FFF
24	24	24	24	24	24	PRAMC_2 (STBY)	0x400AA000	0x400AFFFF
160	160	160	160	160	160	PRAMC_2 (STBY)	0x400B0000	0x400D7FFF
64	64	64	64	NA	NA	PRAMC_2 (STBY)	0x400D8000	0x400E7FFF
32	32	32	NA	NA	NA	PRAMC_3	0x400E8000	0x400EFFFF
32	32	NA	NA	NA	NA	PRAMC_3	0x400F0000	0x400F7FFF
63,75	NA	NA	NA	NA	NA	PRAMC_3	0x400F8000	0x40107EFF
0,25	0,25	0,25	0,25	0,25	0,25	PRAMC_3	0x40107F00	0x40107FFF
64	NA	64	NA	64	NA	D-MEM CPU_0	0x50800000	0x5080FFFF
64	64	64	64	64	64	D-MEM CPU_2	0x52800000	0x5280FFFF

1. RAM size is the sum of TCM and SRAM.

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7 Revision history

Table 82. Document revision history

Date	Revision	Changes
13-May-2016	1	Initial version.
07-June-2016	2	Added Microsoft Excel® workbook file attached to this document version 5.0 (dated 14 April 2016). For details on the changes, refer to the sheet "Revision History".
24-Mar-2017	3	*Chapter 3: Electrical characteristics* *Section 4.1: Introduction*: – Removed text “The IPs and...for the details”. – Removed the two notes. *Section 4.2: Absolute maximum ratings* – Added text “Exposure to absolute ... reliability” – Added text “even momentarily” *Table 4: Absolute maximum ratings*: – Updated values in conditions column. – Added parameter T_{TRIN} – For parameter “T_{STG}”, maximum value updated from “175” to “125” – Added new parameter “T_{PAS}” – For parameter “I_{INJ}”, description updated from “maximum...PAD” to “maximum DC...pad” *Section 4.3: Operating conditions*: *Table 5: Operating conditions*: – Added footnote “The maximum number...” to parameter F_{SYS}. – For parameter “V_{DD_LV}”, changed the classification from “D” to “P” *Table 7: Device supply relation during power-up/power-down sequence*: Parameter “V_{DD_LV}” removed Renamed “Wait State configuration” table to *Table 6: PRAM wait states configuration* *Section 4.7: Device consumption*: *Table 8: Device consumption*: Values updated for the following parameters: – Max value of “$I_{DD_MAIN_CORE_AC}$” updated to “50” – Min and Max value of “I_{DDHALT}” updated from “74” and “115” to “71” and “100” respectively – Min and Max value of “I_{DDSTOP}” updated from “18” and “45” to “15” and “30” respectively *Section 4.8: I/O pad specification*: – Replaced all occurrences of “50 pF load” with “CL=50pF”. – Removed note “The external ballast....” *Section 4.8.2: I/O output DC characteristics*: Added note “10%/90% is the....”

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Table 82. Document revision history (continued)

Date	Revision	Changes
24-Mar-2017	3 (cont'd)	*Table 13: WEAK/SLOW I/O output characteristics*: – For parameter "F_{max_W}", updated condition "25 pF load" to "CL=25pF" – For parameter "t_{TR_S}", changed min value (25 pF load) from "4" to "3" – Changed min value (50 pF load) from "6" to "5" *Table 10: I/O pad specification descriptions*: Description of "Standby pads" updated from "Some pads are...weak-pull currents" to "These pads are...CMOS threshold" *Table 15: STRONG/FAST I/O output characteristics*: Parameter "I_{DCMAX_S}" updated: – Condition added "V_{DD}=5V±10% Condition added "V_{DD}=3.3V±10% – Max value updated to 5.5mA *Table 17: I/O consumption*: Updated all the max values of parameters I_{DYN_W} and I_{DYN_M} *Section 3.9: Reset pad (PORST) electrical characteristics*: *Table 19: Reset Pad state during power-up and reset*: Added this table. *Section 3.10: PLLs*: *Table 20: PLL0 electrical characteristics*: – Classification of parameter "I_{PLL0}" changed from "C" to "T". – Footnote "Jitter values...CLKOUT pin" added for parameters: $\lvert\Delta_{PLL0PHI0SPJ}\rvert$ $\lvert\Delta_{PLL0PHI1SPJ}\rvert$ $\Delta_{PLL0LTJ}$ *Table 21: PLL1 electrical characteristics*: – Classification of parameter "I_{PLL1}" changed from "C" to "T". – Footnote "Jitter values...CLKOUT pin" added for parameter "$\lvert\Delta_{PLL1PHI0SPJ}\rvert$" *Section 4.11: Oscillators*: Renamed section "RC oscillator 1024 kHz" to *Section 4.11.4: Low power RC oscillator* *Table 22: External 40 MHz oscillator electrical specifications*: – Classification for parameters "C_{S_EXTAL}" and "C_{S_EXTAL}" changed from "T" to "D". – Updated classification, conditions, min and max values for parameter "g_m". – For parameters "C_{S_EXTAL}" and "C_{S_EXTAL}", text "QFP" and "BGA" removed. Only QFP values remain. – Min nd Max value of parameters C_{S_EXTAL} updated from "1.5" and "3.2" to "3" and "7" respectively. – Min nd Max value of parameters C_{S_XTAL} updated from "1.5" and "3.2" to "3" and "7" respectively. – For parameter "gm", classification changed from "D" to "P" for frequency "15-20 MHz" – For parameter "gm", classification changed from "P" to "D" for frequency "20-25 MHz"

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Table 82. Document revision history (continued)

Date	Revision	Changes
24-Mar-2017	3 (cont'd)	*Table 24: Internal RC oscillator electrical specifications*: – For parameter "I_{FIRC}", replaced max value of 300 with 600 and added footnote to the description. – Min, Typ and Max value of "δf_{var_SW}" updated from "-1", "-", "1" to "-0.5", "$\pm$0.3" and "0.5" respectively. *Table 23: 32 kHz External Slow Oscillator electrical specifications*: For parameter "gmsxosc", changed the cassification to "P". *Table 25: 1024 kHz internal RC oscillator electrical characteristics*: For parameter "δf_{var_T}", and "δf_{var_V}" changed the classification to "P". *Section 4.12: ADC system*: *Table 26: ADC pin specification*: – For I_{LKG}, changed condition "C" to "—". – Added table footnote "This parameter ...3 dB less" to parameters - $SNR_{DIFF150}$, $SNR_{DIFF333,}$ and SNR_{SE150} – Added footnote "When using a GAIN ... resolution of 15 bits" to parameter "RESOLUTION". – Added footnote "Conversion offset ... offset error" to parameter V_{OFFSET}. – Removed footnote "SNR value guaranteed ... frequency range" from parameters- $SNR_{DIFF150}$ and $SNR_{DIFF333.}$ – In V_{cmrr}, changed "SR" to "CC" and "D" to "T" – Changed min value from "1.5" to "—" in parameter "I_{ADV_D}" – Changed min value from "3" to "—" in parameter "ΣI_{ADR_D}". – Added footnote "Consumption is given ... set-up" to parameter "ΣI_{ADR_D}" – Removed footnote "Sampling is .... $f_{ADCD_M}/2$" – Updated footnote "S/D ADC is ...12 dB" *Table 27: SARn ADC electrical specification*: – Classification for parameter "$I_{ADCREFH}$" changed from "C" to "T". – For parameter f_{ADCK} (High frequency mode), changed min value from "7.5" to "> 13.33". – Deleted footnote "Values are subject to change (possibly improved to ±2 LSB) after characterization" *Table 28: ADC-Comparator electrical specification*: – Classification for parameter "$I_{ADCREFH}$" changed from "C" to "T" – Removed table footnote "Values are subject to change (possibly improved to ±2 LSB) after characterization" Updated *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)* *Section 3.13: Temperature sensor*: *Table 29: Temperature sensor electrical characteristics*: For "temperature monitoring range", classification removed (was C)

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Table 82. Document revision history (continued)

Date	Revision	Changes
24-Mar-2017	3 (cont'd)	*Section 4.14: LFAST pad electrical characteristics*: *Table 32: LFAST PLL electrical characteristics*: – Min and Max value of parameter "ERR_{REF}" updated from "TBD" to "-1" and "+1" respectively – Max value of parameter "PN" updated from "TBD" to "-58" – Frequency of parameter "ΔPER_{REF}" updated from "10MHz" to "20MHz". – Max value of parameter "ΔPER_{REF}" for condition "Single period" updated from "TBD" to "350" – Min and Max value of parameter "ΔPER_{REF}" for condition "Long period" updated from "TBD" to "-500" and "+500" respectively. *Section 4.15: Power management*: *Table 33: Power management regulators*: Removed text "In parts packaged with LQFP176, the auxiliary and clamp regulators cannot be enabled" from note 2. *Table 32: External components Integration*: – For PMOS, replaced "STT4P3LLH6" with "PMPB100XPEA" – For NMOS, replaced "STT6N3LLH6" with "PMPB55XNEA" – Added table footnote to typ value of C_{S2}. – Removed table footnote "External components number....." *Table 35: Linear regulator specifications*: Classification of parameter "IDD_{MREG}" changed from "T" to "P". *Table 36: Auxiliary regulator specifications*: Classification of parameter "IDD_{AUX}" changed from "T" to "P". *Table 38: Standby regulator specifications*: Classification of parameter "IDD_{SBY}" changed from "T" to "P". *Figure 17: Voltage monitor threshold definition*: Updated the figure. *Table 39: Voltage monitor electrical characteristics*: – For V_{POR031_C}, changed the max value from 0.85 to 0.97. – For $T_{VMFILTER}$, replaced T with D. – Min value of "V_{POR200_C}" updated from "1.96" to "1.80" – Max value of "V_{POR031_C}" updated from ".85" "0.97" – Min value of "V_{MVD270_SBY}" updated from "2.71" to "2.68" – Max value of "V_{MVD270_SBY}" updated from "2.80" "2.84" – Changed the min value of parameter V_{POR200_C} from "1.96" to "1.80" – Changed the max value of parameter V_{POR031_C} from "0.85" to "0.97" – Changed the condition of parameter $T_{VMFILTER}$ from "T" to "D" *Section 4.17: AC Specifications*: *Table 44: Nexus debug port timing*: Classification of parameters "t_{EVTIPW}" and "t_{EVTOPW}" changed from "P" to "D". *Table 46: DSPI channel frequency support*: Added column to show slower and faster frequencies. *Table 49: DSPI CMOS slave timing — full duplex — normal and modified transfer formats (MTFE = 0/1)*: Added column to show slower and faster frequencies. *Table 47: DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1*: Changed the Min value of tSCK (very strong) from 33 to 59.

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Table 82. Document revision history (continued)

Date	Revision	Changes
24-Mar-2017	3 (cont'd)	*Section 4: Package information*: Updated – *Table 65: eTQFP64 package mechanical data* – *Figure 47: eTQFP64 package outline* – *Table 66: eTQFP100 package mechanical data* *Section 5.6: Package thermal characteristics*: *Table 74: Thermal characteristics for 64 exposed pad eTQFP package*, *Table 75: Thermal characteristics for 100 exposed pad eTQFP package*, *Table 76: Thermal characteristics for 144 exposed pad eTQFP package*, *Table 77: Thermal characteristics for 176 exposed pad LQFP package*: Updated the following parameter values with External and Internal ballast values: – $R_{\theta JA}$ – $R_{\theta JB}$ – $R_{\theta JCtop}$ – $R_{\theta JCbottom}$ – Ψ_{JT} Removed parameter "$R_{\theta JMA}$" *Table 78: Thermal characteristics for 292-pin FPBGA*: External ballast value updated for the following parameters: – $R_{\theta JA}$ – $R_{\theta JB}$ – $R_{\theta JC}$ – Ψ_{JT} Removed parameter "$R_{\theta JMA}$". *Chapter 5: Ordering information*: *Figure 64: Commercial product scheme*: – Core option "4" updated from "Single computing e200z4 core" to "Single computing e200z4 core(CPU_2)" – Core option "E" updated from "Dual computing e200z4 core" to "Dual computing e200z4 core(CPU_2+CPU_0)" Added new tables: – *Table 79: Code Flash Options FOTA (KByte)* – *Table 81: RAM options* Changed Microsoft Excel® workbook attached to this document (was SPC584Cx_SPC58ECx_IO_Definition_v5.xlsx dated 14 April 2016). For details, refer to the sheet Revision History of the attached file "SSPC584Cx_SPC58ECx_IO_Definition_v6.xlsx".

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Table 82. Document revision history (continued)

Date	Revision	Changes
04-Feb-2018	4	*Features*: Added AEC-Q100 qualified and updated core name to “e200z420n3” (was “e200z4d”). *Chapter 3: Package pinouts and signal descriptions*: Rephrased introduction sentence since the pinout excel file will no longer be attached to the datasheet *Chapter 3: Electrical characteristics*: Reformated note from introduction *Table 3: Parameter classifications*: Updated the description of classification tag “T” *Section 4.3: Operating conditions*: Replaced reference to IO_definition excel file by "the device pinout IO definition excel file" *Table 5: Operating conditions*: – Removed note “Core voltage as ....” – Added parameter I_{INJ2} – Removed parameter “V_{RAMP_LV}” – Updated the table footnote “Positive and negative Dynamic current....” for all Chorus devices *Table 6: PRAM wait states configuration*: Renamed the “Wait State configuration” table to “PRAM wait state configuration” *Table 8: Device consumption*: “I_{DD_LKG}” and “I_{DD_LV}”: Added footnote “I_{DD_LKG} and I_{DD_LV} are reported as...” Updated: I_{DD_LKG}, $I_{DDSTBY8}$ and $I_{DDSTBY256}$ for all conditions Updated some typical values for $I_{DDSTBY8}$ and $I_{DDSTBY256}$ Replaced all references to the IO_definitions excel file by “the device pinout IO definition excel file *Table 10: I/O pad specification descriptions*: Changed “the CMOS threshold” by “(VDD_HV_IO_MAIN / 2) +/-20%” at Standby pads type *Table 15: STRONG/FAST I/O output characteristics*: updated values for t_{TR_S} for condition CL = 25 pF and CL = 50 pF *Table 16: VERY STRONG/VERY FAST I/O output characteristics*: – “$t_{TR20-80}$” replaced by “t_{TR20-8_V}” – “t_{TRTTL}” replaced by “t_{TRTTL_V}” – “$\Sigma t_{TR20-80}$” replaced by “$\Sigma t_{TR20-80_V}$” *Table 18: Reset PAD electrical characteristics*: replaced reference to IO_definition excel file by "Refer to the device pinout IO definition excel file" *Table 20: PLL0 electrical characteristics*: – $\lvert\Delta_{PLL0PHI0SPJ}\rvert$: changed “T” by “D” and added pk-pk to Conditions value – $\lvert\Delta_{PLL0PHI1SPJ}\rvert$: added pk-pk to Conditions value *Table 20: PLL0 electrical characteristics* and *Table 21: PLL1 electrical characteristics*: Added “f_{INFIN}”, Symbol “f_{INFIN}”: changed “C” by “—” in column “C”

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Table 82. Document revision history (continued)

Date	Revision	Changes
04-Feb-2018	4 (Cont')	*Table 22: External 40 MHz oscillator electrical specifications*: Changed table footnote 3 by: This value is determined by the crystal manufacturer and board design, and it can potentially be higher than the maximum provided. *Table 23: 32 kHz External Slow Oscillator electrical specifications*: Updated the parameter symbols and added "CC" to T_{sxosc}. *Table 26: ADC pin specification*: – Updated Max value for C_S and C_{P2} – Added electrical specification for $R_{20K\Omega}$ symbol – Changed Max value = 1 by 2 for Cp2 SARB channels *Table 27: SARn ADC electrical specification*: – Added symbols tADCINIT and tADCBIASINIT – Column "C" splitted and added "D" for I_{ADV_S} *Table 28: ADC-Comparator electrical specification*: – Added new parameter "$t_{ADCINITSBY}$". – Set min = $5/f_{ADCK}$ µs with footnote "In case the ADC is used as Fast Comparator the sampling time is $t_{ADCSAMPLE} = 2/f_{ADCK}$" – Set min = $6/f_{ADCK}$ for ADC comparator mode, at symbol $t_{ADCSAMPLE}$ – Column "C" splitted and added "D" for I_{ADV_S} *Section 4.14: LFAST pad electrical characteristics*: Introduction paragraph: – 1st sentence: hidden text "both the SIPI and" – all 2nd sentence hidden: "The same LVDS.. tables" *Figure 9: LFAST LVDS timing definition*: Added conditional tag to hide: – 400 mV p-p (MSC/DSPI) – 0.50 * T (MSC/DSPI) – (MSC/DSPI) *Figure 17: Voltage monitor threshold definition*: Right blue line adjusted on the top figure *Section 4.15.1: Power management integration*: added sentence "It is recommended...device itself" for all devices *Table 35: Linear regulator specifications*: updated values for symbol "ΔIDD_{MREG}" *Table 34: External components integration*: Updated Min and Max values at symbol C_E to 1.1 and 3.0 respectively *Table 40: Wait State configuration*: Updated this table by adding APC parameter and frequency ranges *Section 4.17.5: CAN timing*: added section *Table 57: TxEN output characteristics*: added table footnote "Pad configured as VERY STRONG. *Table 58: TxD output characteristics*: changed note 3 to apply to the whole table *Table 60: CAN timing*: added columns for "CC" and "D"

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Table 82. Document revision history (continued)

Date	Revision	Changes
04-Feb-2018	4 (Cont')	*Table 46: DSPI channel frequency support*: Added DSPI_5 to lower frequency and removed it from higher frequency *Table 65: eTQFP64 package mechanical data*: Removed θ, θ1, θ2, θ3 *Table 69: FPBGA292 package mechanical data*: updated Amax formula in table footnote 2 *Figure 64: Commercial product scheme*: – Removed Packing option R – Set Y as example Packing option X: Replaced "90°" by "(pin 1 top right)" *Table 81: RAM options*: Updated some values of SPC58EC80 and SPC4C80 devices
25-Sep-2018	5	Following are the changes in this version of the Datasheet: *Section 4.7: Device consumption* *Table 9: Device consumption*: – Updated all maximum values for $I_{DDSTBY8}$, $I_{DDSTBY32}$ and $I_{DDSTBY256}$ parameters – Updated table footnote 4 *Section 3.10: PLLs* *Table 20: PLL0 electrical characteristics*: The maximum value of $f_{PLL0PHI0}$ is changed from "400" to "FSYS" with a footnote. *Section 4.11: Oscillators* *Table 22: External 40 MHz oscillator electrical specifications*: table footnote 1 updated: "DCF clients XOSC_LF_EN and XOSC_EN_40MHZ" changed by "XOSC_FREQ_SEL" *Section 4.12: ADC system* *Table 28: ADC-Comparator electrical specification*: Added "ADC comparator mode" condition to the following two parameters: $I_{ADCREFH}$ Min: - and Max: 19.5 µA $I_{ADCREFL}$ Min: - and Max: 20.5 µA *Section 4.14: LFAST pad electrical characteristics* Updated *Figure 9: LFAST LVDS timing definition* *Section 4.15: Power management* *Table 34: External components integration*: Added "2SCR574D" to "Q_{EXT}" parameter.

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Table 82. Document revision history (continued)

Date	Revision	Changes
25-Sep-2018	5	*Section 4.16: Flash* *Table 40: Wait State configuration*: Updated this table by adding APC parameter and frequency ranges. *Section 4: Package information* Updated *Section 4.3: eTQFP144 package information* Updated *Section 4.4: eLQFP176 package information* *Section 5: Ordering information* *Figure 64: Commercial product scheme*: updated example code for Silicon revision value and Packing value *Table 81: RAM options*: Split the last PRAMC_3 line into 2 lines
16-Jun-2020	6	Throughout document: Formatting and editorial changes. The following are the changes in this version of the Datasheet: Updated the sub-title for Cover page Updated package information on Cover page. Updated *Chapter 1: Introduction*: Removed “Document overview” section title. Updated section 1.2 Description to *Chapter 2: Description* *Chapter 4: Electrical characteristics*: *Section 4.2: Absolute maximum ratings*: *Table 4: Absolute maximum ratings*: Added cross reference to footnote(2) to all V_{DD_HV*} and V_{IN} *Section 4.3: Operating conditions*: – *Table 5: Operating conditions*: $V_{DD_HV_ADR_S}$: removed line for C condition. – *Table 7: Device supply relation during power-up/power-down sequence*: changed $V_{DD_HV_IO_}$ to $V_{DD_HV_IO_FLEX}$. Updated *Section 4.6: Temperature profile* *Section 4.7: Device consumption*: *Table 9: Device consumption*: move table footnote *1.* from table title to “Value”. *Section 4.9: Reset pad (PORST) electrical characteristics* – *Figure 5: Startup Reset requirements*: deleted V_{DDMIN}

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Table 82. Document revision history (continued)

Date	Revision	Changes
16-Jun-2020	6	*Section 4.10: PLLs* *Section 4.10.1: PLL0*: *Table 20: PLL0 electrical characteristics*: – Changed condition from T to D for $\|\Delta_{PLL0PHI1SPJ}\|$, $\Delta_{PLL0LTJ}$ and I_{PLL0}. – Updated Max value for $f_{PLL0PHI0}$ symbol and removed the footnote. *Section 4.10.2: PLL1*: *Table 21: PLL1 electrical characteristics*: changed condition from T to D for I_{PLL1} *Section 4.11: Oscillators* *Section :* : *Table 24: Internal RC oscillator electrical specifications*: – Updated *1.* – Updated Max value for I_{FIRC}. *Section 4.12: ADC system*: *Section 4.12.1: ADC input description* *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)*: added parameter "C_{EXT}: external capacitance" and component to scheme. *Table 26: ADC pin specification*: added row for symbol "C_{EXT} / SR". *Section 4.14: LFAST pad electrical characteristics* *Section 4.14.2: LFAST LVDS interface electrical characteristics*: *Table 30: LVDS pad startup and receiver electrical characteristics* – Removed the last sentence of Note "Total internal capacitance...". – Move table footnote *1.* and *2.* from table title to "Symbol". *Table 31: LFAST transmitter electrical characteristics* – Move table footnote *1.*, *2.* and *3.* from table title to "Symbol". *Table 32: LFAST PLL electrical characteristics* – Move table footnote *1.* from table title to "Symbol". *Section 4.15: Power management* *Section 4.15.1: Power management integration*: *Table 34: External components integration*: – Updated Conditions for C_{BV}. – Updated notes content and numbering – Updated Min value for R_E – Updated Typ value for C_{LVN} – Added note 2 for C_{FLA} – Added note 6 for C_{ADC} – Updated Min value for R_B

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Table 82. Document revision history (continued)

Date	Revision	Changes
16-Jun-2020	6 (cont'd)	*Section 4.15.3: Voltage monitors*: *Table 39: Voltage monitor electrical characteristics*: added footnote "Even if LVD/HVD..." *Section 4.16: Flash* *Table 40: Wait State configuration*: for APC=001 changed the minimum frequency from 40 to 55 MHz *Section 4.17: AC Specifications* *Section 4.17.2.1.1: DSPI CMOS master mode – classic timing* – *Table 47: DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1*: added footnote "Due to timing delay...". – *Table 48: DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1*: added footnote "Due to timing delay...". – Updated *Figure 28: DSPI CMOS master mode — classic timing, CPHA = 1* *Section 4.17.3.7: RMII transmit signal timing (TXD[1:0], TX_EN)*: added Note "RMII transmit...as 1ns". *Chapter 5: Package information* Added introduction sentence in each Package section. Added sub-section "Package mechanical drawings and data information" and introduction sentence to the notes list. *Table 64: Package case numbers*: removed package reference column. *Section 5.1: eTQFP64 package information* Updated *Figure 47: eTQFP64 package outline* Added *Figure 48: eTQFP64 section A-A* Added *Figure 49: eTQFP64 section B-B* *Table 65: eTQFP64 package mechanical data*: – updated table, notes content and numbering – updated min. dimensions for D3 and E3 Moved notes to new section *Section 5.1.1: Package mechanical drawings and data information*: Added *Figure 50: eTQFP64 leadframe pad design* Added *Table 66: eTQFP64 symbol definitions* *Section 5.2: eTQFP100 package information* Updated *Figure 51: eTQFP100 package outline* Added *Figure 52: eTQFP100 section A-A* Added *Figure 53: eTQFP100 section B-B* *Table 67: eTQFP100 package mechanical data*: updated table, notes content and numbering. Moved notes to new section *Section 5.2.1: Package mechanical drawings and data information*:

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Table 82. Document revision history (continued)

Date	Revision	Changes
16-Jun-2020	6 (cont'd)	Added *Figure 54: eTQFP100 leadframe pad design* Added *Table 68: eTQFP100 symbol definitions* *Section 5.3: eTQFP144 package information* Updated *Figure 55: eTQFP144 package outline* Added *Figure 56: eTQFP144 section A-A* Added *Figure 57: eTQFP144 section B-B* *Table 69: eTQFP144 package mechanical data*: updated table, notes content and numbering. Moved notes to new section *Section 5.3.1: Package mechanical drawings and data information*: Added *Figure 58: eTQFP144 leadframe pad design* Added *Table 70: eTQFP144 symbol definitions* *Section 5.4: eLQFP176 package information*: Updated *Figure 59: eLQFP176 package outline* Added *Figure 60: eLQFP176 section A-A* Added *Figure 61: eLQFP176 section B-B* *Table 71: eLQFP176 package mechanical data*: updated table, notes and numbering. Moved notes to new section *Section 5.4.1: Package mechanical drawings and data information* Added *Figure 62: eLQFP176 leadframe pad design* Added *Table 72: eLQFP176 symbol definitions* *Section 5.5: FPBGA292 package information* Updated *Figure 63: FPBGA292 package outline* *Table 73: FPBGA292 package mechanical data*: updated table and notes. Moved notes to new section *Section 5.5.1: Package mechanical drawings and data information* *Section 5.6: Package thermal characteristics* *Table 74: Thermal characteristics for 64 exposed pad eTQFP package*: updated values for $R_{\theta JA}$, $R_{\theta JB}$, $R_{\theta JCtop}$ and Ψ_{JT}. *Table 75: Thermal characteristics for 100 exposed pad eTQFP package*: updated values. *Table 76: Thermal characteristics for 144 exposed pad eTQFP package*: updated values. *Table 77: Thermal characteristics for 176 exposed pad LQFP package*: – $R_{\theta JA}$, $R_{\theta JCtop}$,$R_{\theta JB}$, $R_{\theta JCbottom}$ updated value. – Ψ_{JT} updated Conditions and value. *Section 5.6.5: FPBGA292*: updated package name. *Table 78: Thermal characteristics for 292-pin FPBGA*: updated values.

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Table 82. Document revision history (continued)

Date	Revision	Changes
16-Jun-2020	6 (cont'd)	*Chapter 6: Ordering information* Updated *Figure 64: Commercial product scheme* *Table 79: Code Flash Options FOTA (KByte)* – Renamed the Table to Code Flash Options FOTA (KByte) – Updated partition for start addresses 0x00FC0000, 0x00FC4000, 0x00FC8000 and 0x00FCC000 Added *Table 80: Code Flash Options contiguous (KByte)*
31-Jul-2020	7	The following are the changes in this version of the Datasheet: *Chapter 5: Package information* *Table 65: eTQFP64 package mechanical data*: – Updated values of min dimension for D3 and E3 to 5.9. – Updated value for ddd to 0.07. *Chapter 6: Ordering information* *Table 79: Code Flash Options FOTA (KByte)*: Added note, "The user must use this mapping without mixing it with the Contiguous one in Table 80" to SPC58xC74 (3M) and SPC58xC70 (2M). *Table 80: Code Flash Options contiguous (KByte)*: Added note, "The user must use this mapping without mixing it with the FOTA one in Table 79" to SPC58xC74 (3M) and SPC58xC70 (2M).
07-May-2021	8	The following are the changes in this version of the Datasheet: *Section 4.16: Flash* *Table 41: Flash memory program and erase specifications* Program rate symbol "tprr" is changed to "ttr" *Chapter 5: Package information* *Table 65: eTQFP64 package mechanical data*: – Updated values of min dimension for D3 and E3 to 5.25. – Updated values of max dimension for D2 and E2 to 6.93. – Updated value for ddd to 0.08. *Figure 51: eTQFP100 package outline*: updated. *Section 5.2.1: Package mechanical drawings and data information*: – Added note *19.*

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